
142
PROM PROGRAMMER
16DEC80 -
96 SHEETS • 5 x 5 QUAD
10⅛ x 7⅞ • 53-110
NATIONAL
NATIONAL BLANK BOOK COMPANY, INC.
Holyoke, Massachusetts 01040•Made in USA

PROM Programmer Manual Vol 2

INDEX

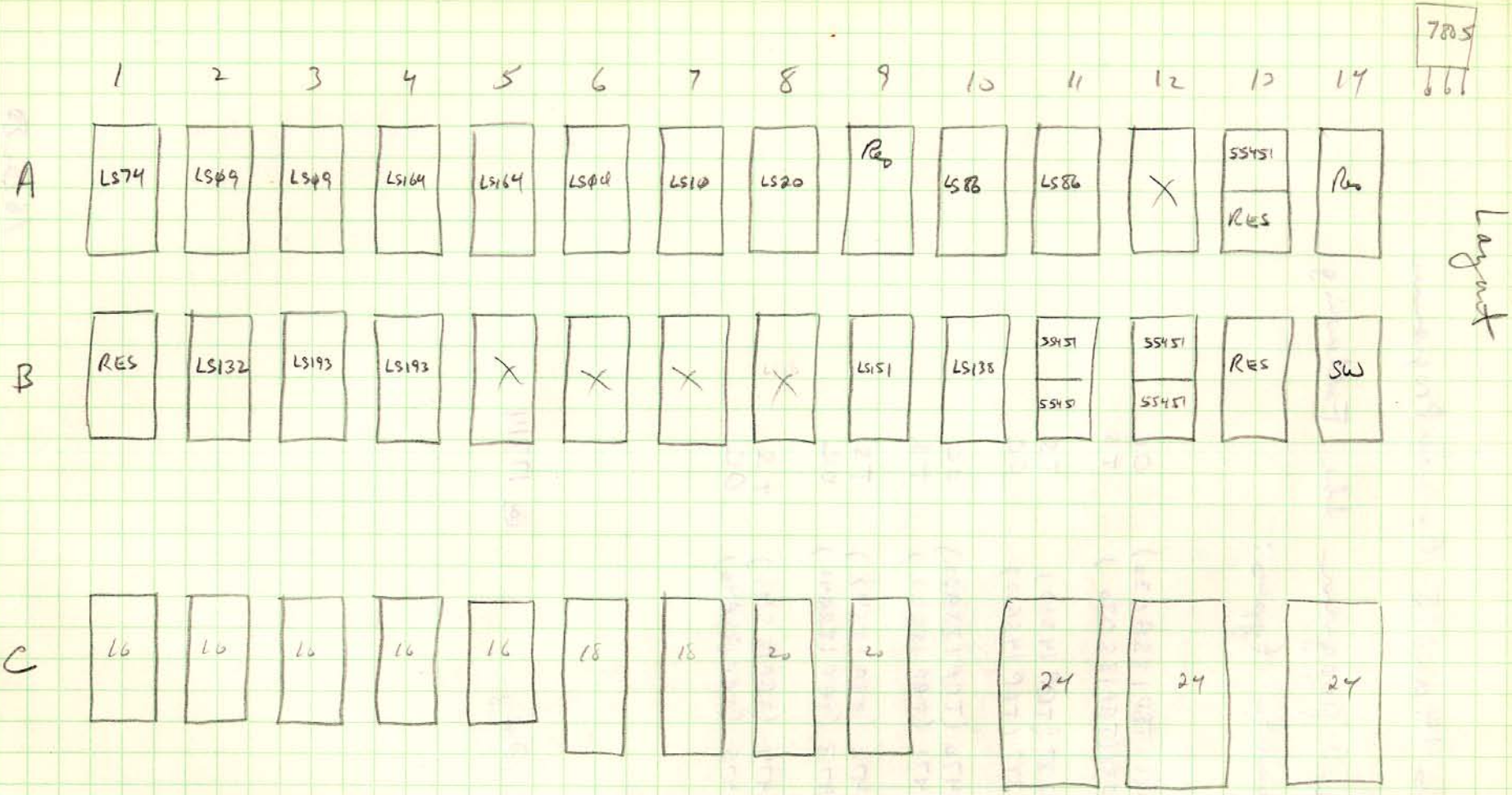
TI Series 14 and 18 Generic Programmer

This card will program the Following Texas Instruments types:

32x8	74S188 (TBP18SA030)	OC
	74S288 (TBP18S030)	TS
256x4	74S287 (TBP14S10)	TS
	74S387 (TBP14SA10)	OC
256x8	74S470 (TBP18SA22)	OC
	74S471 (TBP18S22)	TS
512x8	74S472 (TBP18S42)	TS
	74S473 (TBP18SA42)	OC
512x8	74S474 (TBP18S46)	TS
	74S475 (TBP18SA46)	OC

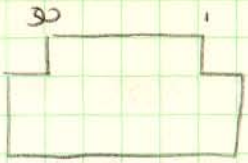
$ID = 22_8$ @ 177111

16 Dec 80
ABO


785
661
1 2 3 4 5 6 7 8 9 10 11 12 13 14
A
LS74 LS09 LS09 LS164 LS164 LS08 LS10 LS20 RES LS86 LS86 X 55451 RES RES
B
RES LS132 LS193 LS193 X X X X LS151 LS138 55451 55451 55451 55451 RES SW
C
16 16 16 16 16 18 18 20 20 24 24 24
Layout

100 Pin Connector

Top Side CT



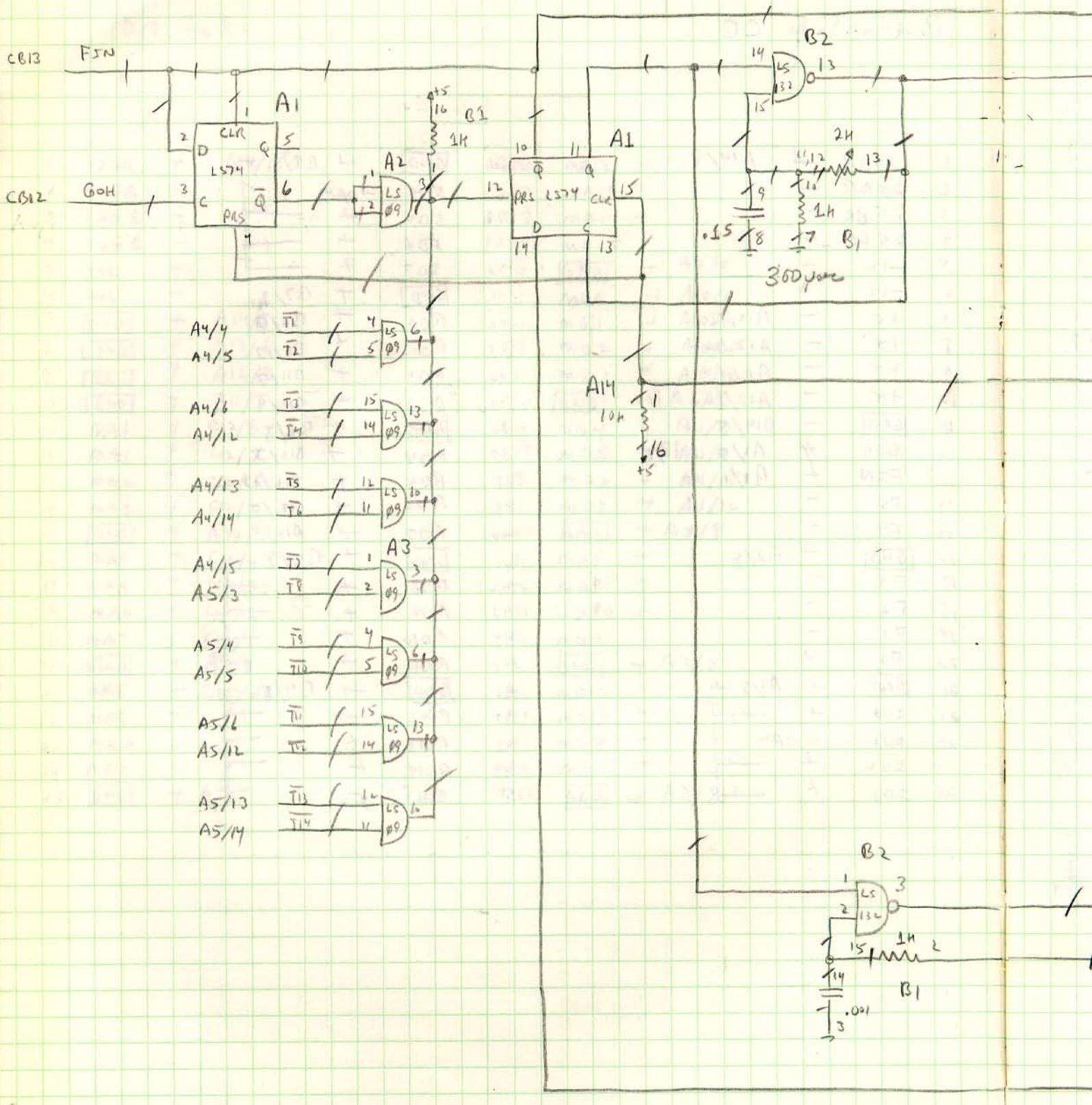
1	+25A	+	A14/15
2	+25A	-	
3	+25B	-	
4	+25B	-	
5	+12	-	
6	+12	-	
7	GND	+	A14/8
8	GND	+	A13/8
9	GND	+	A12/8
10	GND	+	A11/8
11	MA0	+	C12/8
12	MA1	+	C12/7
13	MA2	+	C12/6
14	MA3	+	C12/5
15	GND	+	A10/8
16	MA4	+	C12/4
17	AA5	+	C12/3
18	MA6	+	C12/2
19	MA7	+	C12/1
20	GND	+	A9/8
21	AA8	+	C12/23
22	MA9	-	
23	MA10	-	
24	MA11	-	
25	GND	+	A8/8
26	MA12	-	
27	MA13	-	
28	MA14	-	
29	MA15	-	
30	GND	+	A7/8
31	MD0	+	A10/1
32	MD1	+	A10/4
33	MD2	+	A10/15
34	MD3	+	A10/12
35	GND	+	A6/8
36	MD4	+	A11/1
37	MD5	+	A11/4
38	MD6	+	A11/15
39	MD7	+	A11/12
40	GND	+	A5/8
41	MD8	-	
42	MD9	-	
43	MD10	-	
44	MD11	-	
45	GND	+	A4/8
46	MD12	-	
47	MD13	-	
48	MD14	-	
49	MD15	-	
50	GND	+	A3/8

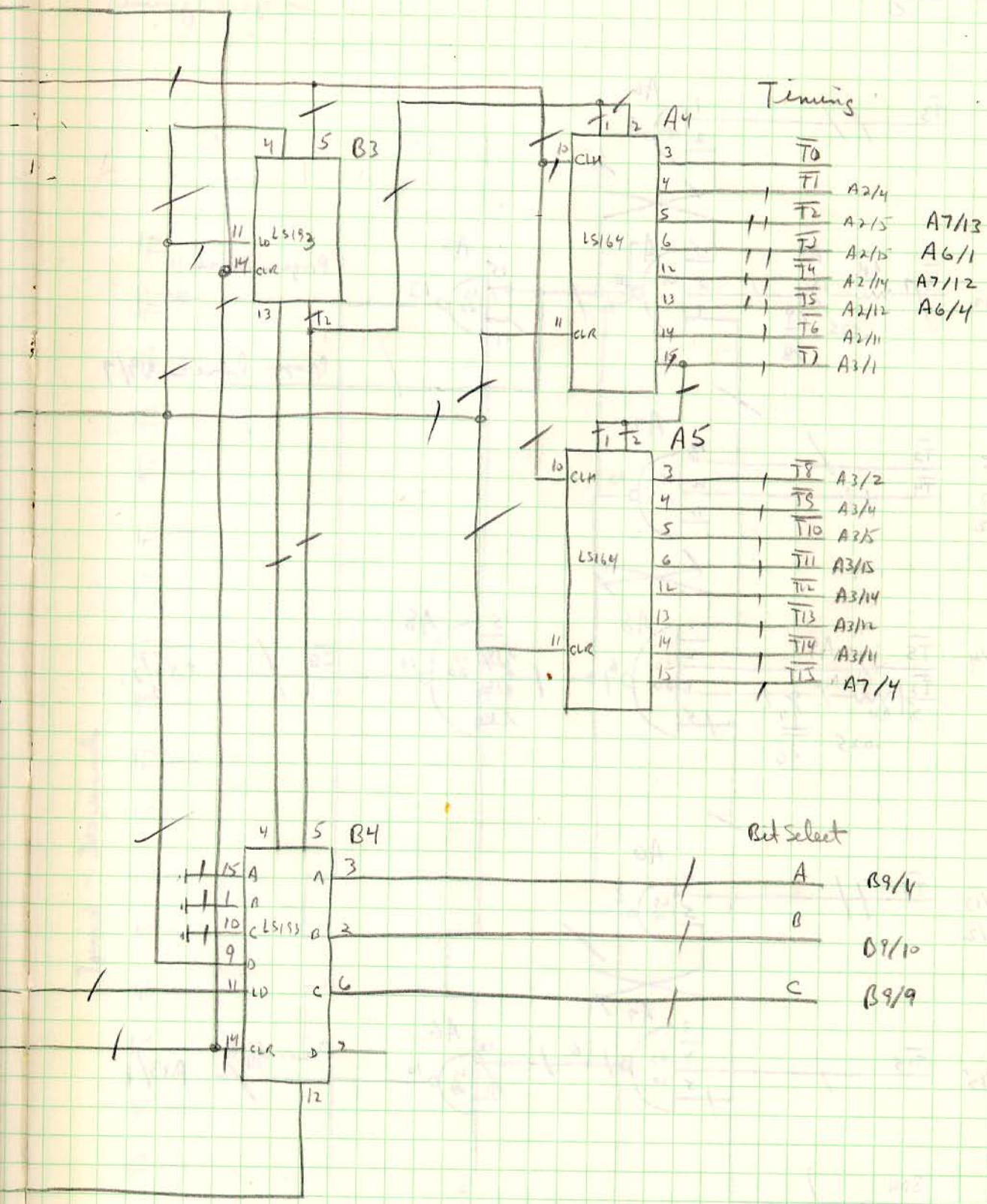
Bottom Side CB

1	25AR	⊥	A14/8
2	25AR	—	
3	25BR	—	
4	25BR	—	
5	−12	—	
6	−12	—	
7	+5	—	A13/16
8	+5	—	A12/16
9	+5	—	A11/16
10	+5	—	A10/16
11	GND	—	B14/8
12	60H	#	A1/3 A8/5
13	FIN	⊥	A1/1
14	F5	—	
15	F4	—	
16	GND	⊥	A2/8
17	F3	—	
18	F2	—	
19	F1	—	
20	F0	—	
21	GND	⊥	A1/8
22	ID0	⊥	
23	ID1	—	open
24	ID2	⊥	
25	ID3	⊥	
26	GND	⊥	B8/8
27	ID4	—	open
28	ID5	⊥	
29	ID6	⊥	
30	ID7	⊥	
31	GND	⊥	B7/8
32	RD0	⊥	B11/3
33	RD1	⊥	B11/13
34	RD2	⊥	B11/7
35	RD3	⊥	B11/9
36	GND	⊥	B6/8
37	RD4	⊥	B12/3
38	RD5	⊥	B12/13
39	RD6	⊥	B12/7
40	RD7	⊥	B12/9
41	GND	⊥	B5/8
42	RD8	⊥	
43	RD9	⊥	
44	RD10	⊥	
45	RD11	⊥	
46	GND	⊥	B4/8
47	RD12	⊥	
48	RD13	⊥	
49	RD14	⊥	
50	RD15	⊥	

16 Dec 80
ARD

Scan Timer


CB13
FIN
CB12
60H
A1
LS74
CLR
D
C
PRS
Q
A2
LS
00
B1
1K
+5
16
A1
LS74
PRS
CLR
B2
LS
32
2K
.15
1K
B1
360 pps
A14
10K
A4/4
A4/5
A4/6
A4/12
A4/13
A4/14
A4/15
A5/3
A5/4
A5/5
A5/6
A5/12
A5/13
A5/14
A3
B2
LS
32
1K
B1
.001


Timing
A4
LS164
CLR
T0
T1
T2
T3
T4
T5
T6
T7
A2/4
A2/5
A2/15
A2/14
A2/12
A2/11
A3/1
A7/13
A6/1
A7/12
A6/4
A5
LS164
CLR
T8
T9
T10
T11
T12
T13
T14
T15
A3/2
A3/4
A3/5
A3/15
A3/14
A3/12
A3/11
A7/4
B3
LS193
LD
CLR
B4
LS153
A
B
C
D
LD
CLR
Bit Select
A
B
C
B9/4
B9/10
B9/9

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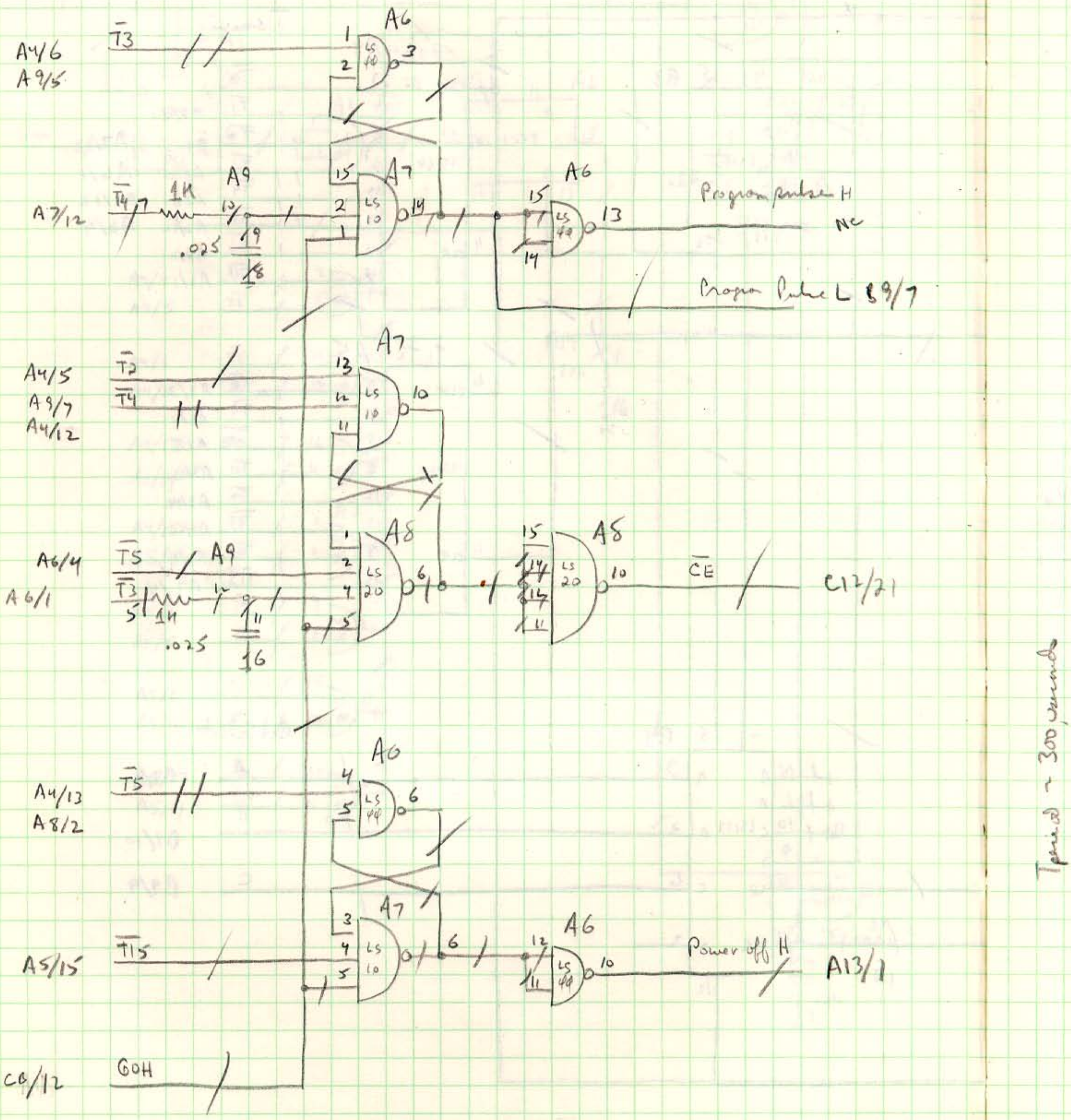
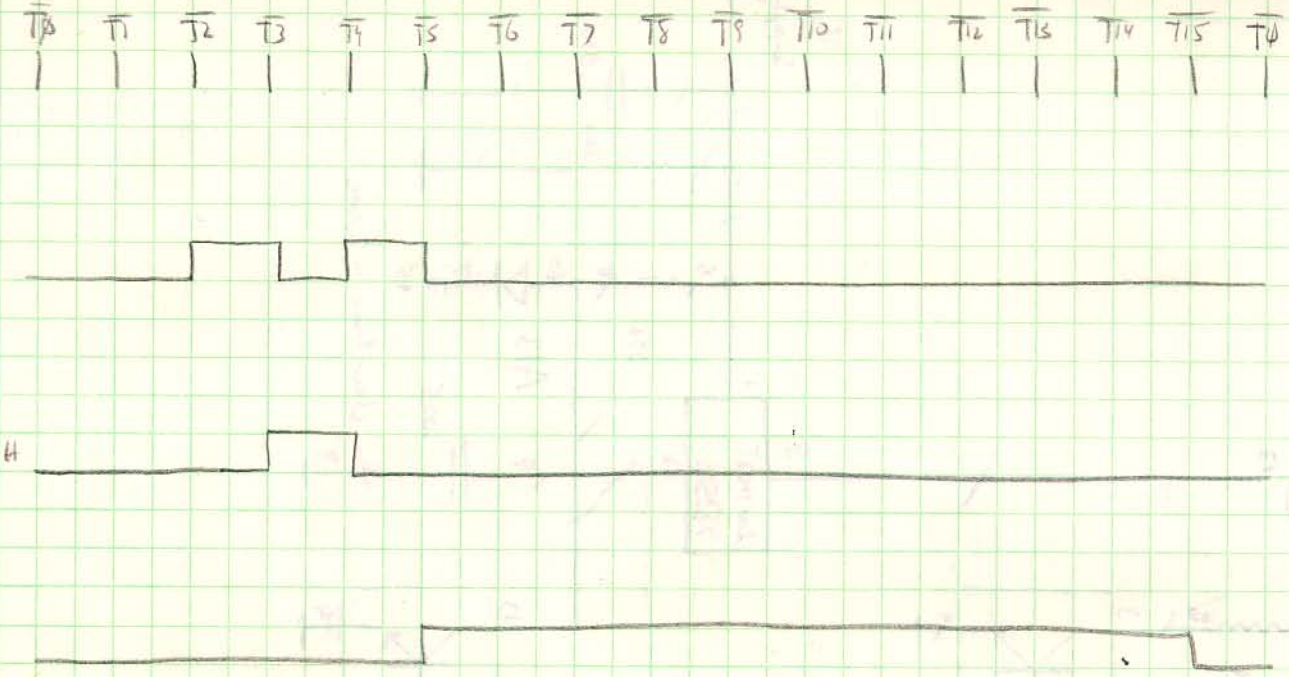
ARD

Pulse timing



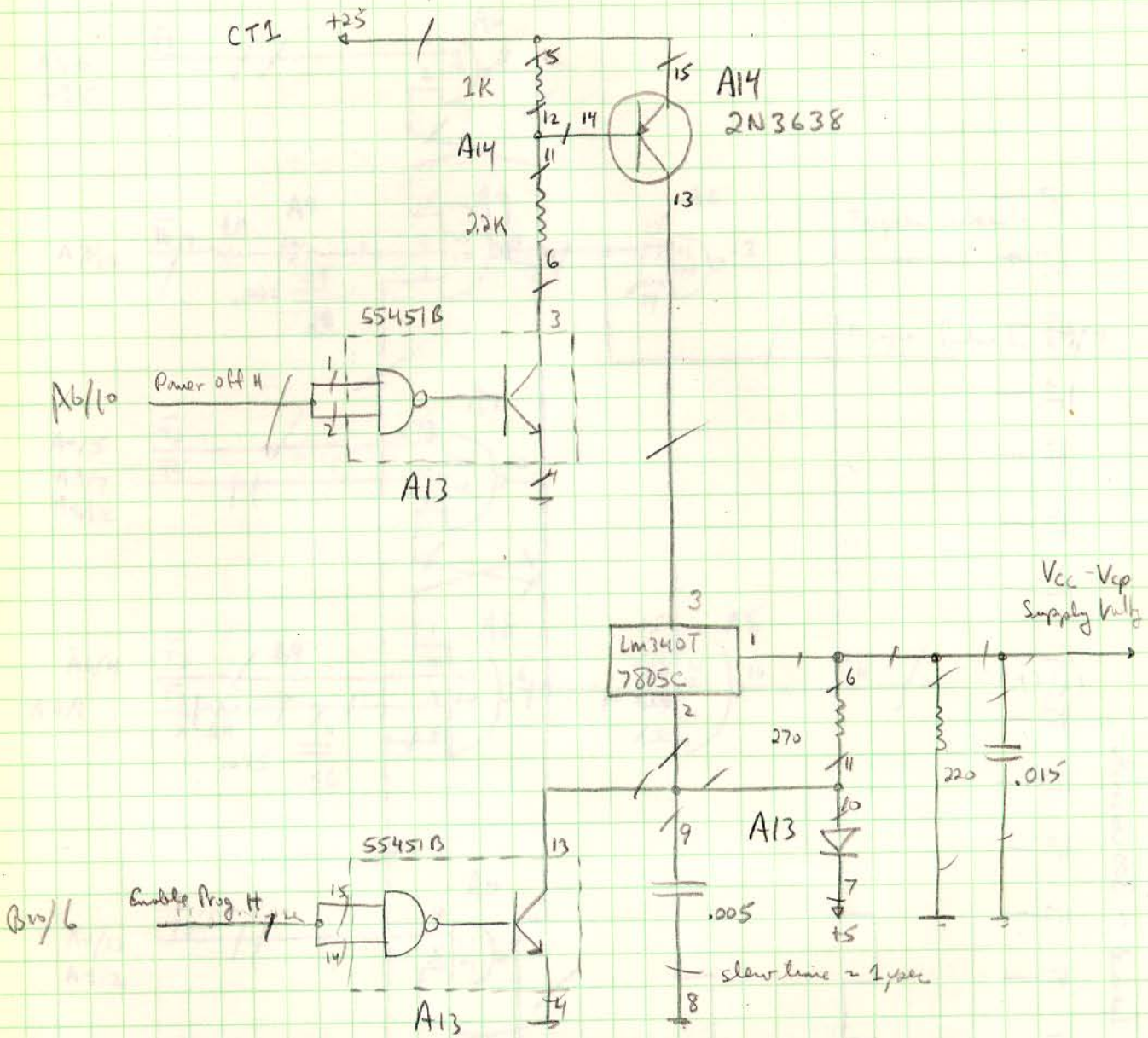
Timing diagram

Period ~ 300 seconds

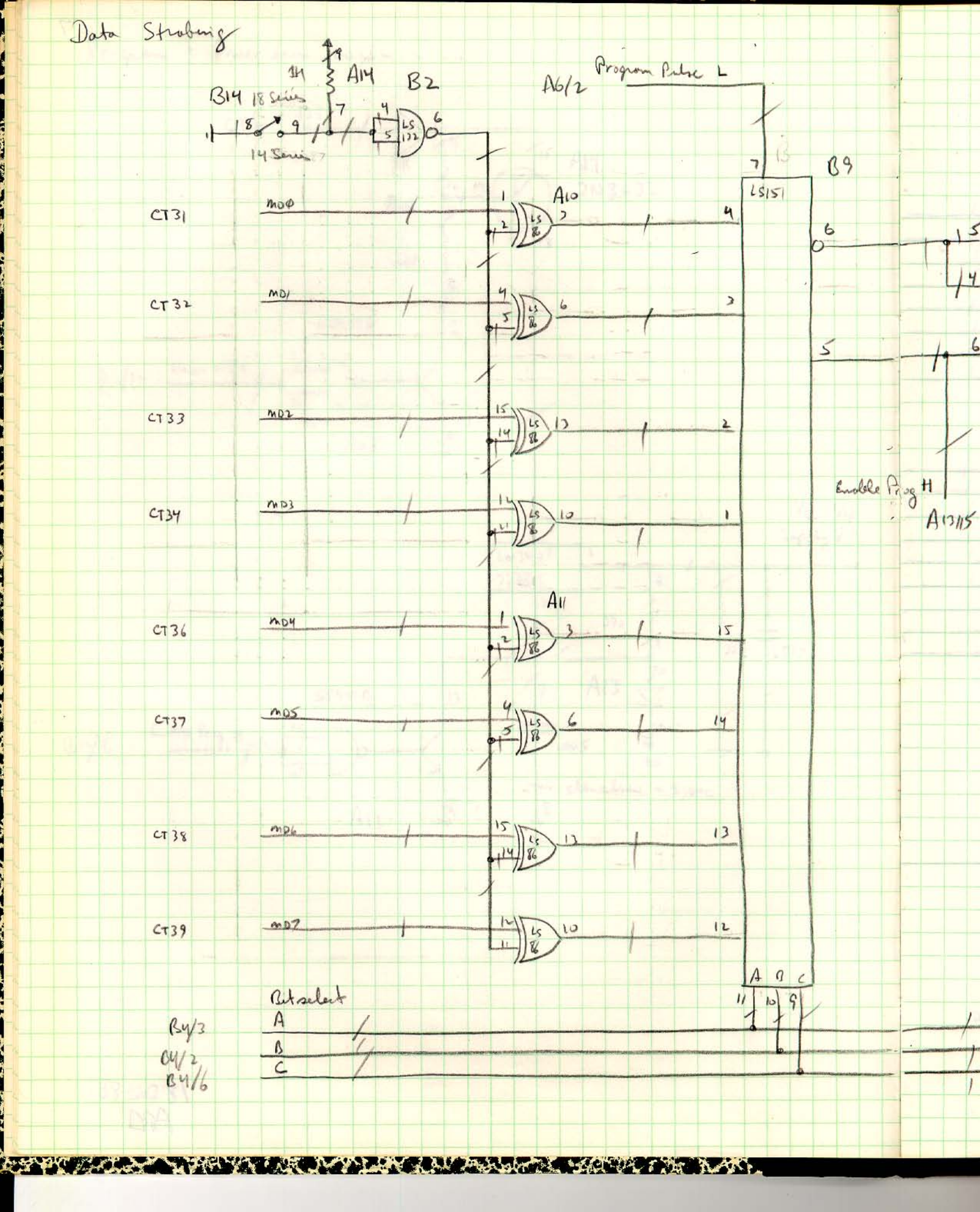


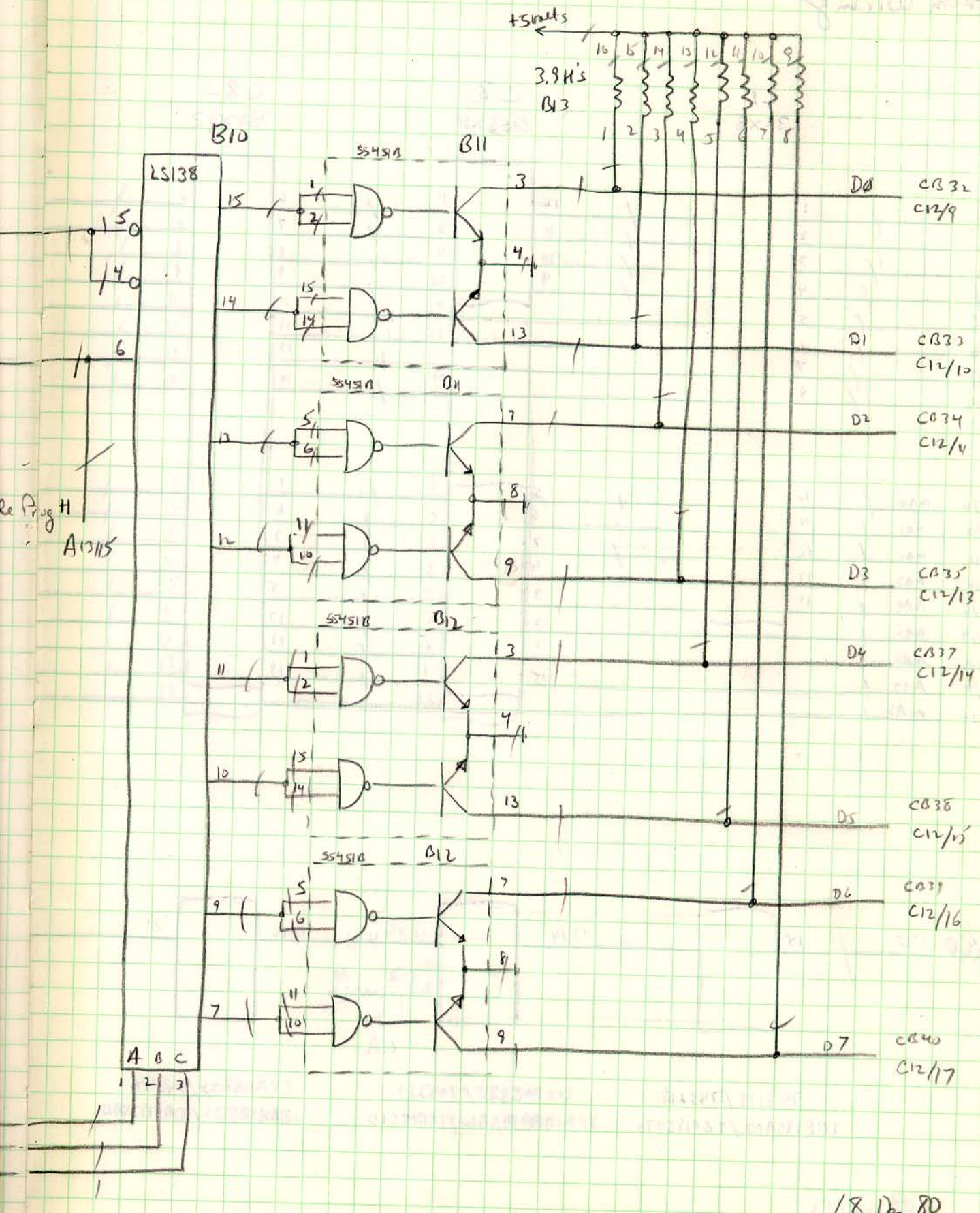
Aug 28 1981

Program & Power down Logic

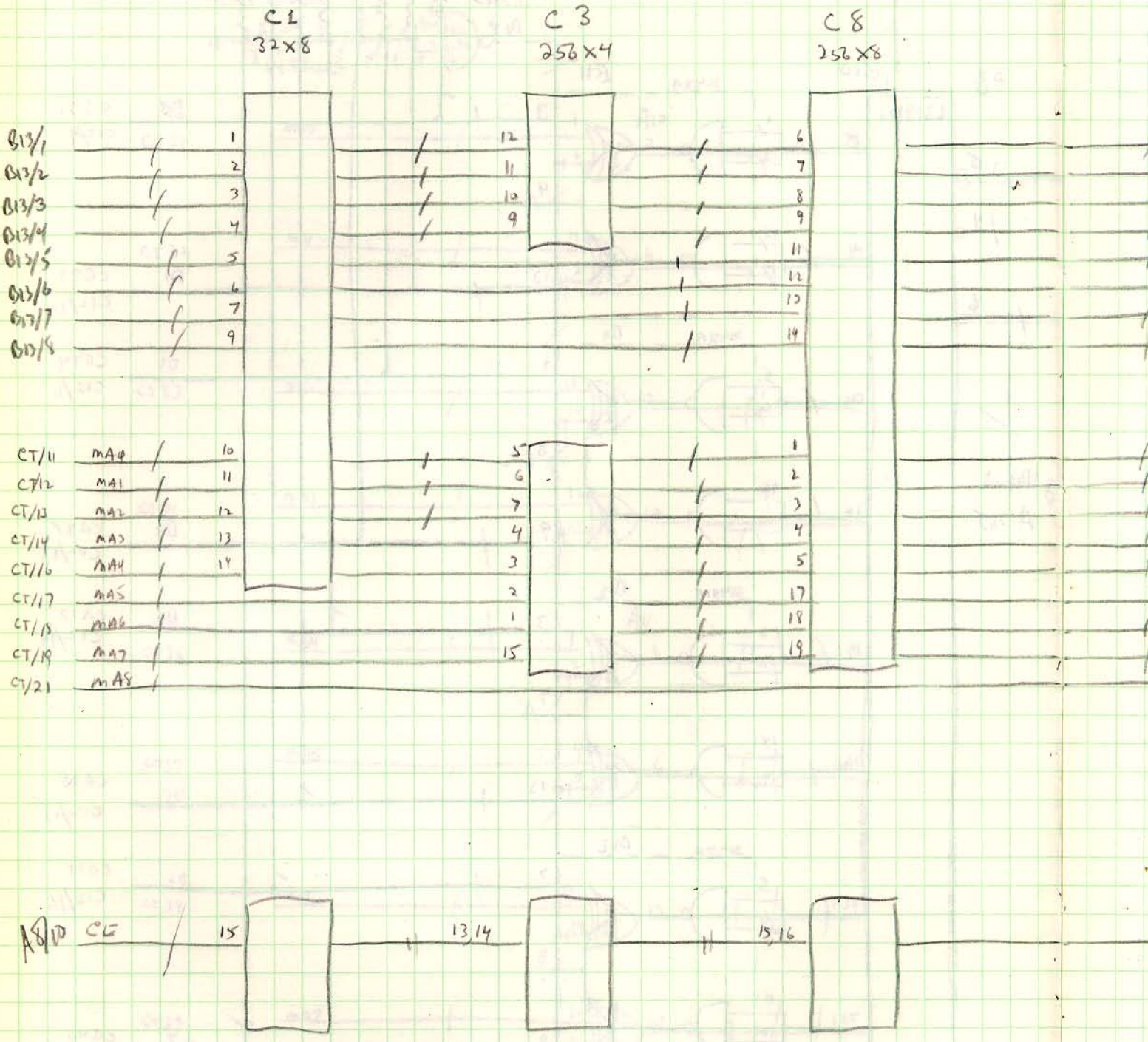


Data Strobing




+5volts
3.9K's
B13
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
B10
LS138
B11
5451B
B11
5451B
B12
5451B
B12
5451B
D0
D1
D2
D3
D4
D5
D6
D7
CB32
C12/9
CB33
C12/10
CB34
C12/4
CB35
C12/13
CB37
C12/14
CB38
C12/15
CB39
C12/16
CB40
C12/17
A13115
A B C
18 Dec 80
ABD

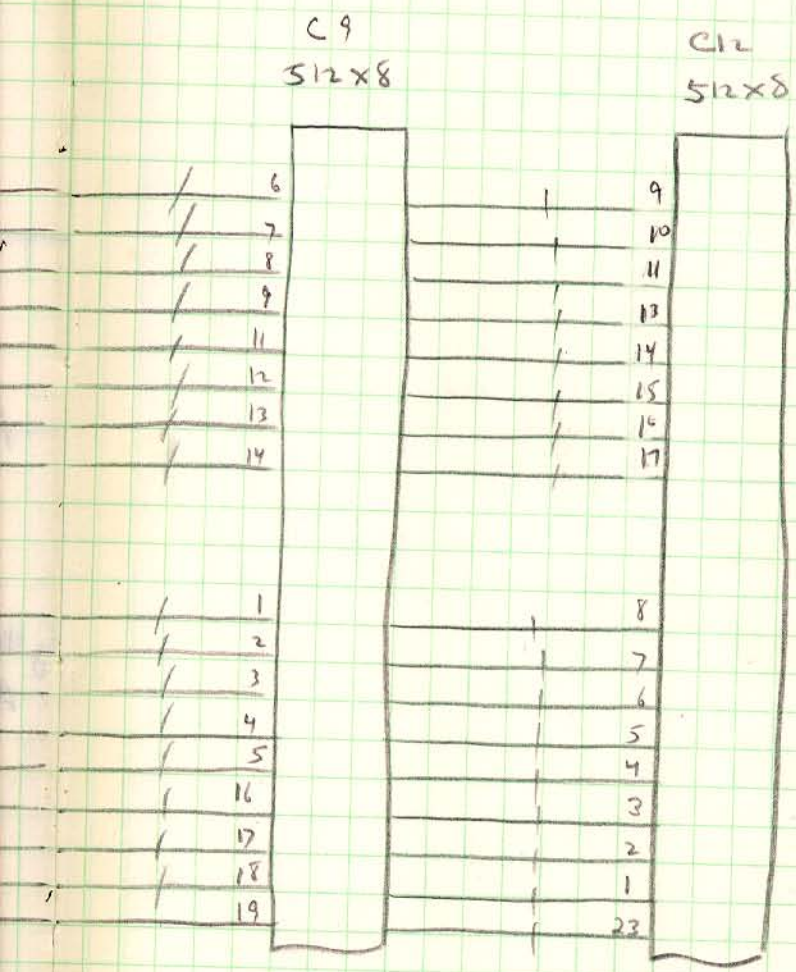
PROM Wiring

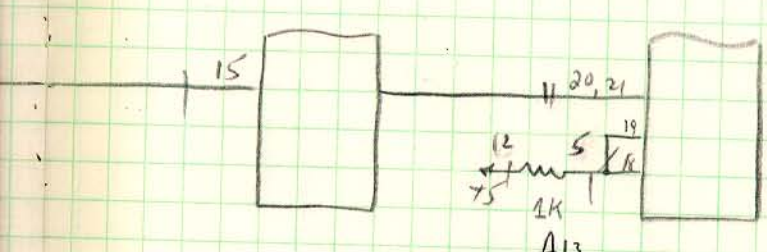


74S188/74S288
TBP18SA030/TBP18S030

74S387/74S287
TBP14SA10/TBP14S10

74S470/74S471
TBP18SA22/TBP18S22





A13

74S472/74S473
TBP 18S42 / TBP18SA42

74S474/74S475
TBP 18S46 / TBP18SA46

18 Dec 80
ARD

IC Locations

A1	74LS74	5
A2	74LS09	5
A3	74LS09	5
A4	74LS164	5
A5	74LS164	5
A6	74LS00	6
A7	74LS10	6
A8	74LS20	6
A9	Resistors	6
A10	74LS86	8
A11	74LS86	8
A12	———	
A13	75451 / Res	7
A14	Resistors	5, 7, 8

B1	Resistor	5
B2	74LS132	5, 8
B3	74LS193	5
B4	74LS193	5
B5	———	
B6	———	
B7	———	
B8	———	
B9	74LS151	8
B10	74LS138	8
B11	75451's	8
B12	75451's	8
B13	Resistors	8
B14	Switch	8

Prom Sockets

C1	S188 / 18SA030	S288 / 18S030	9
C2			
C3	S287 / 14S10	S387 / 14SA10	9
C4			
C5			
C6			
C7			
C8	S470 / 18SA42	S471 / 18S22	9
C9	S472 / 18S42	S473 / 18SA42	9
C11			
C12	S474 / 18S46	S475 / 18SA46	9
C14			

26 Dec 80
ABD

Wiring completed 26 Dec 80 ABD

Circuit operational 14 Jan 81 ABD

Expanded PRAM Card

Designed as a replacement for PROM and RAM during system development.

The Board contains 64K bytes of 70NS memory which may be configured as 64K bytes or 32K words.

Individual 4K byte Banks may be read enabled, write enabled, Read/Write enabled or disabled to match a system configuration.

Board ID # is 201 (Byte 177111)

	F_x	43	210
RUN Code	=	00	xxx
Load PRAM	=	10	xxx
Load Access Codes	=	11	xxx

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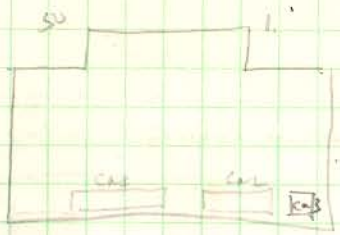
Board Layout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	240	189	32	139	157	ø8	6167	6167	6167	6167	6167	6167	6167	6167	244	244
B	X	189	32	139	157	Rev	6167	6167	6167	6167	6167	6167	6167	6167	244	244
E		74	157	ø4	X											
C	X	Rev	32	139	157	Rev	6167	6167	6167	6167	6167	6167	6167	6167	244	244
D	X	123	ø8	139	157	ø8	6167	6167	6167	6167	6167	6167	6167	6167	244	244

100 pin Connector

Top Side CT (Right to left)



1	+25 A	–		26	MA12	–	D5/2	
2	+25 A	–		27	MA13	–	D5/5	
3	+25 B	–		28	MA14	–	D5/14	
4	+25 B	–		29	MA15	–	D5/11	
5	+12	–		30	GND			
6	+12	–		31	MD0	–	C15/2	A2/4
7	GND			32	MD1	–	C15/4	A2/6
8	GND			33	MD2	–	C15/6	A2/10
9	GND			34	MD3	–	C15/8	A2/12
10	GND			35	GND			
11	MA0	–	A5/2	36	MD4	–	C15/17	B2/4
12	MA1	–	A5/5	37	MD5	–	C15/15	B2/6
13	MA2	–	A5/14	38	MD6	–	C15/13	B2/10
14	MA3	–	A5/11	39	MD7	–	C15/11	B2/12
15	GND			40	GND			
16	MA4	–	B5/2	41	MD8	–		
17	MA5	–	B5/5	42	MD9	–		
18	MA6	–	B5/14	43	MD10	–		
19	MA7	–	B5/11	44	MD11	–		
20	GND			45	GND			
21	MA8	–	C5/2	46	MD12	–		
22	MA9	–	C5/5	47	MD13	–		
23	MA10	–	C5/14	48	MD14	–		
24	MA11	–	C5/11	49	MD15	–		
25	GND			50	GND			

Bottom side CB

1	2SAR	–	
2	2S AR	–	
3	2S BR	–	
4	2S BR	–	
5	–12	–	
6	–12	–	
7	+5	–	
8	+5	–	
9	+5	–	
10	+5	–	
11	GND		
12	GOH	–	C2/3
13	FIN	–	C2/2
14	F5	–	NC
15	F4	–	E4/5
16	GND		
17	F3	–	E4/3
18	F2	–	CN1/49
19	F1	–	CN1/47
20	F0	–	CN1/45
21	GND		
22	ID0	–	
23	ID1	–	
24	ID2	–	
25	ID3	–	
26	GND		
27	ID4	–	
28	ID5	–	
29	ID6	–	
30	ID7	–	
31	GND		
32	RD0	–	A15/18 A1/18
33	RD1	–	A15/16 A1/16
34	RD2	–	A15/14 A1/14
35	RD3	–	A15/12 A1/12
36	GND		
37	RD4	–	A15/3 A1/3
38	RD5	–	A15/5 A1/5
39	RD6	–	A15/7 A1/7
40	RD7	–	A15/9 A1/9
41	GND		
42	RD8	–	
43	RD9	–	
44	RD10	–	
45	RD11	–	
46	GND		
47	RD12	–	
48	RD13	–	
49	RD14	–	
50	RD15	–	

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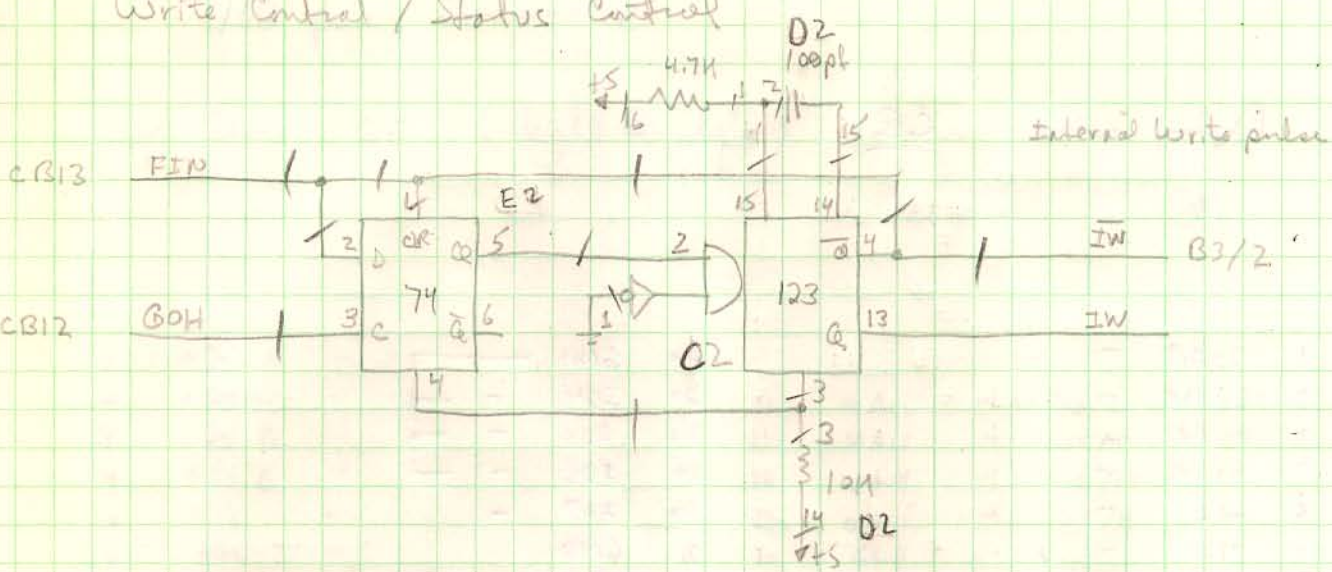
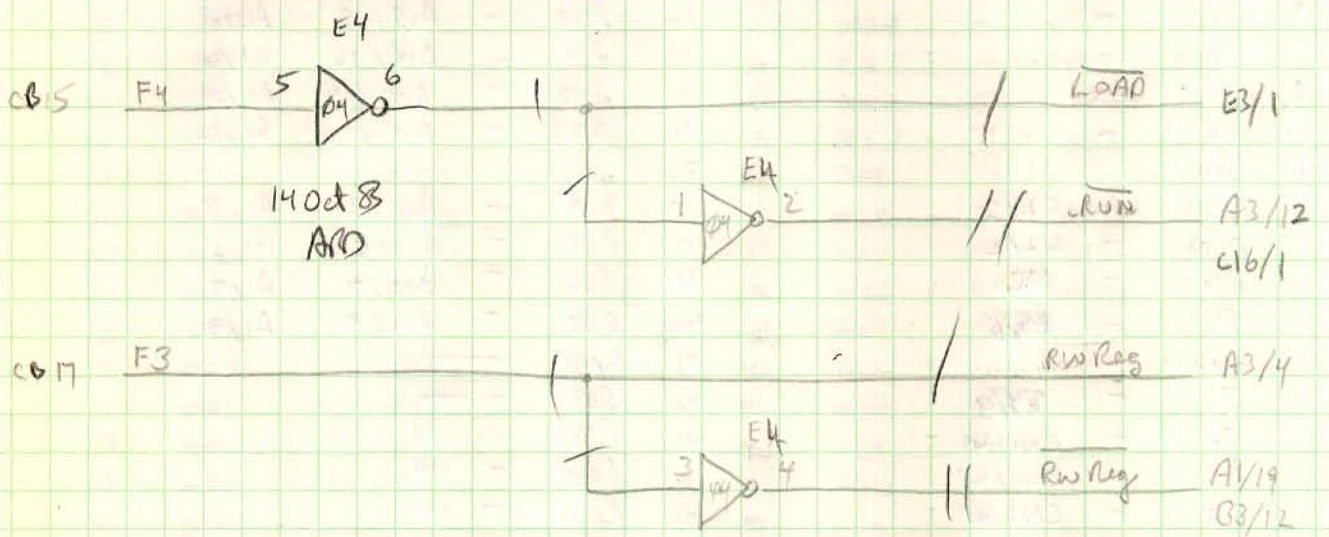
Write Control / Status Control





I/O Connectors

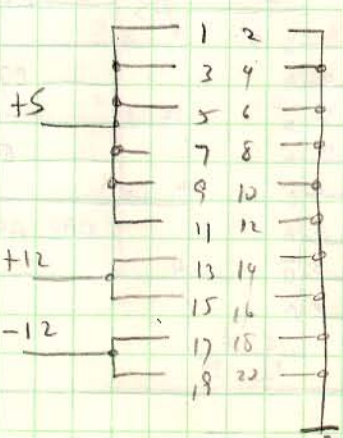
CN1

A5/3	—	AX0	—	1	2	—	
A5/6	—	AX1	—	3	4	—	
A5/13	—	AX2	—	5	6	—	
A5/10	—	AX3	—	7	8	—	
B5/3	—	AX4	—	9	10	—	
B5/6	—	AX5	—	11	12	—	
B5/13	—	AX6	—	13	14	—	
B5/10	—	AX7	—	15	16	—	
C5/3	—	AX8	—	17	18	—	
C5/6	—	AX9	—	19	20	—	
C5/13	—	AX10	—	21	22	—	
C5/10	—	AX11	—	23	24	—	
D5/3	—	AX12	—	25	26	—	
D5/6	—	AX13	—	27	28	—	
D5/13	—	AX14	—	29	30	—	
D5/10	—	AX15	—	31	32	—	
			—	33	34	—	
B3/14	—	$\overline{XR}$	—	35	36	—	
B3/5	—	$\overline{XW}$	—	37	38	—	
A3/2	—	$\overline{WS}$/B	—	39	40	—	
C3/4	—	$\overline{XRCS}$	—	41	42	—	
D3/14	—	$\overline{XWCS}$	—	43	44	—	
C020	—	F0	—	45	46	—	
C019	—	F1	—	47	48	—	
C018	—	F2	—	49	50	—	

CN2

C16/2	—	DX0	—	1	2	—	
C16/4	—	DX1	—	3	4	—	
C16/6	—	DX2	—	5	6	—	
C16/8	—	DX3	—	7	8	—	
C16/17	—	DX4	—	9	10	—	
C16/15	—	DX5	—	11	12	—	
C16/13	—	DX6	—	13	14	—	
C16/11	—	DX7	—	15	16	—	
D16/2	—	DX8	—	17	18	—	
D16/4	—	DX9	—	19	20	—	
D16/6	—	DX10	—	21	22	—	
D16/8	—	DX11	—	23	24	—	
D16/17	—	DX12	—	25	26	—	
D16/15	—	DX13	—	27	28	—	
D16/13	—	DX14	—	29	30	—	
D16/11	—	DX15	—	31	32	—	
			—	33	34	—	
A2/5	—	$\overline{SP0}$	—	35	36	—	
A2/7	—	$\overline{SP1}$	—	37	38	—	
A2/9	—	$\overline{SP2}$	—	39	40	—	
A2/11	—	$\overline{SP3}$	—	41	42	—	
B2/5	—	$\overline{SP4}$	—	43	44	—	
B2/7	—	$\overline{SP5}$	—	45	46	—	
B2/9	—	$\overline{SP6}$	—	47	48	—	
B2/11	—	$\overline{SP7}$	—	49	50	—	

CN3 (Power Connector)



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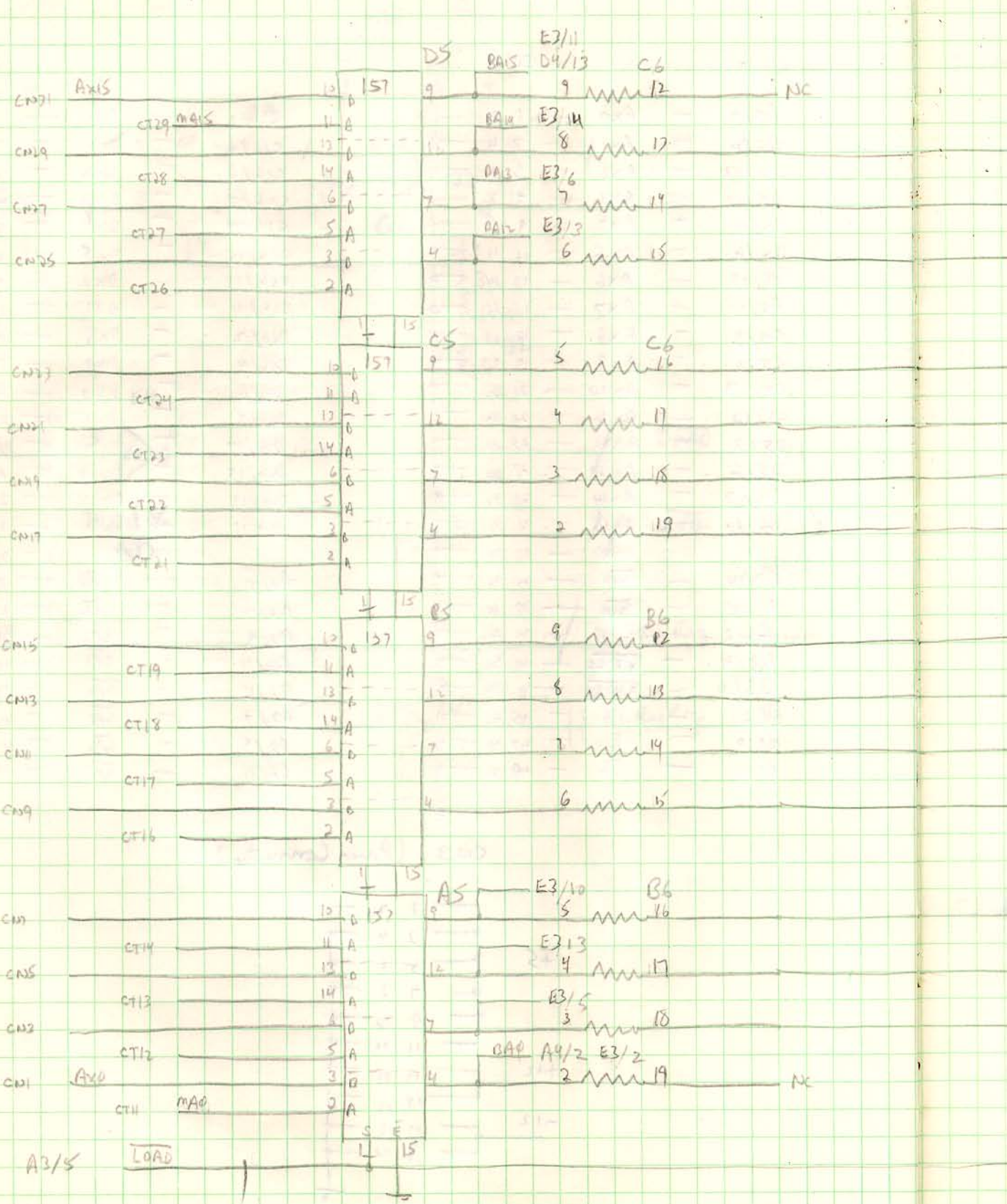
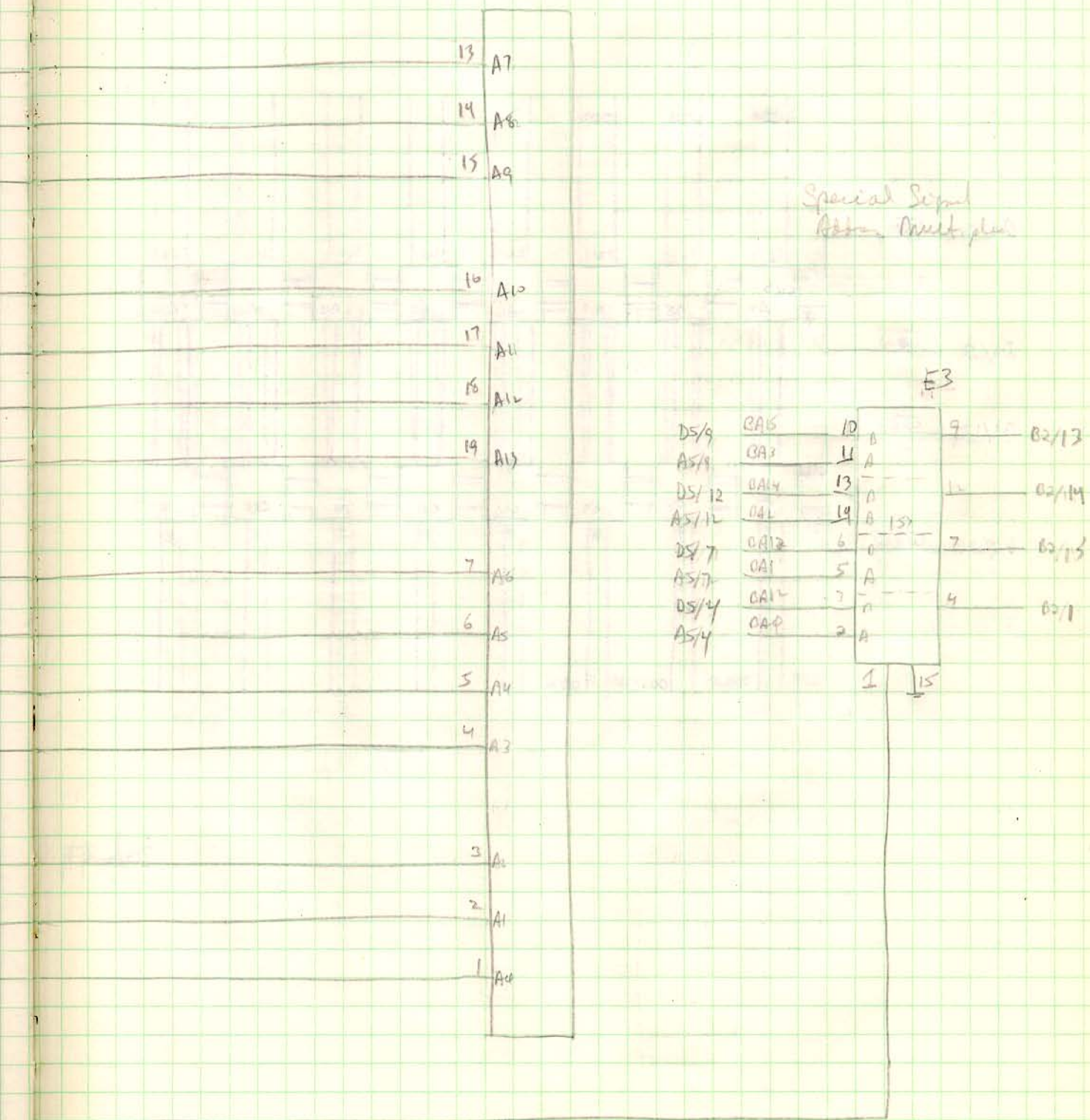
Address Multiplexer

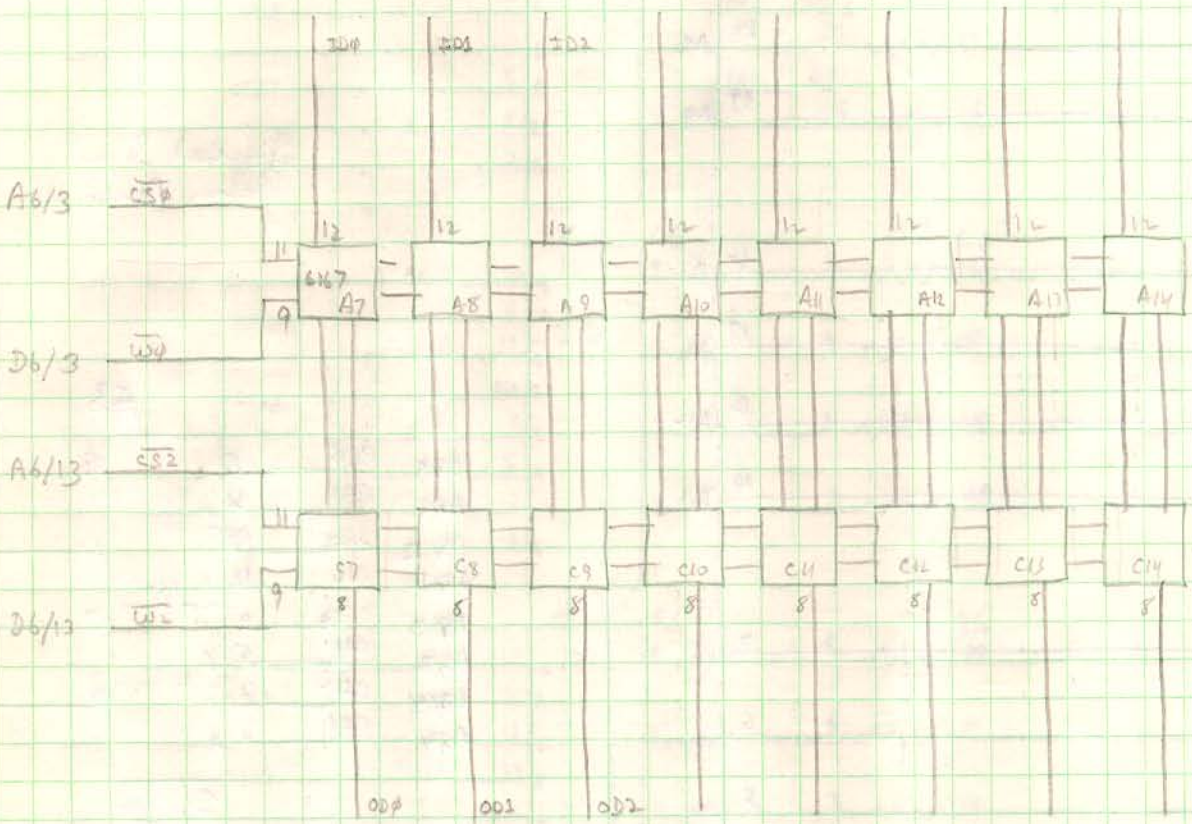


(32) 2167/6167 16K×1 RAM

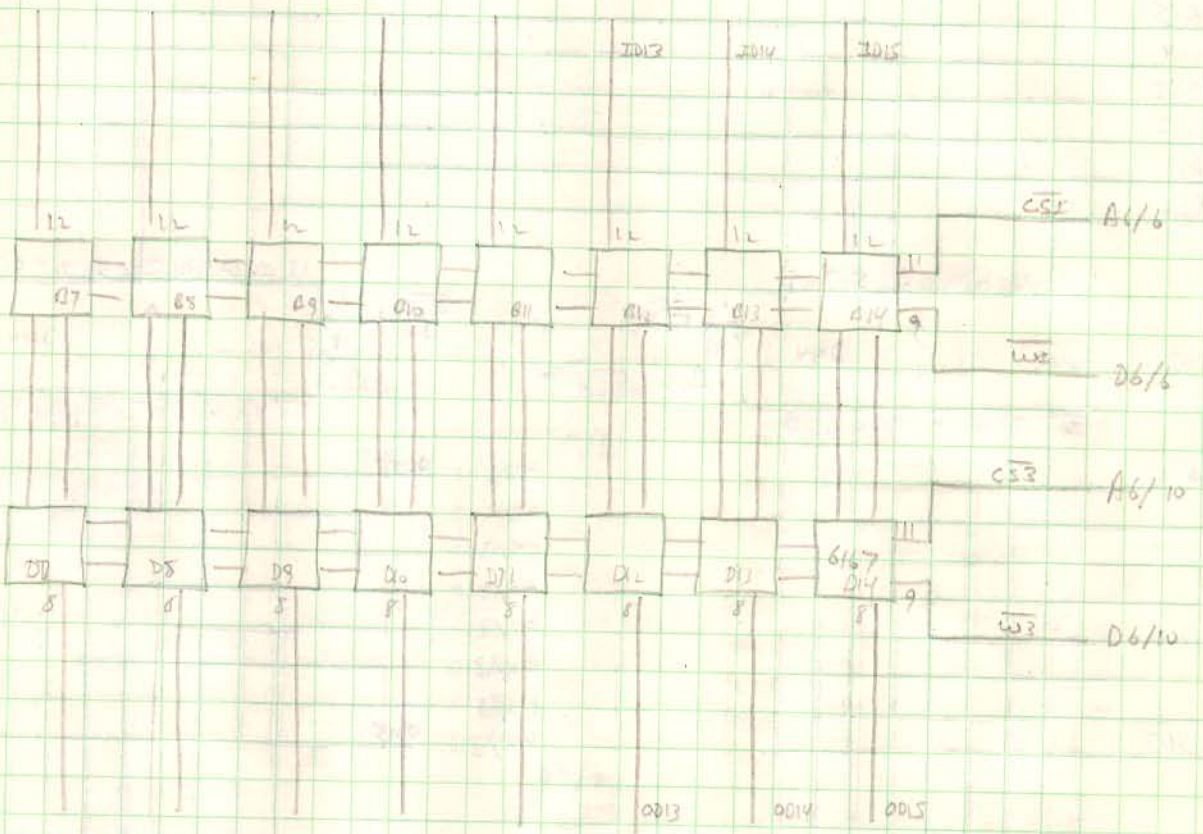


23 July
ARO

Memory Organization



Input



Output

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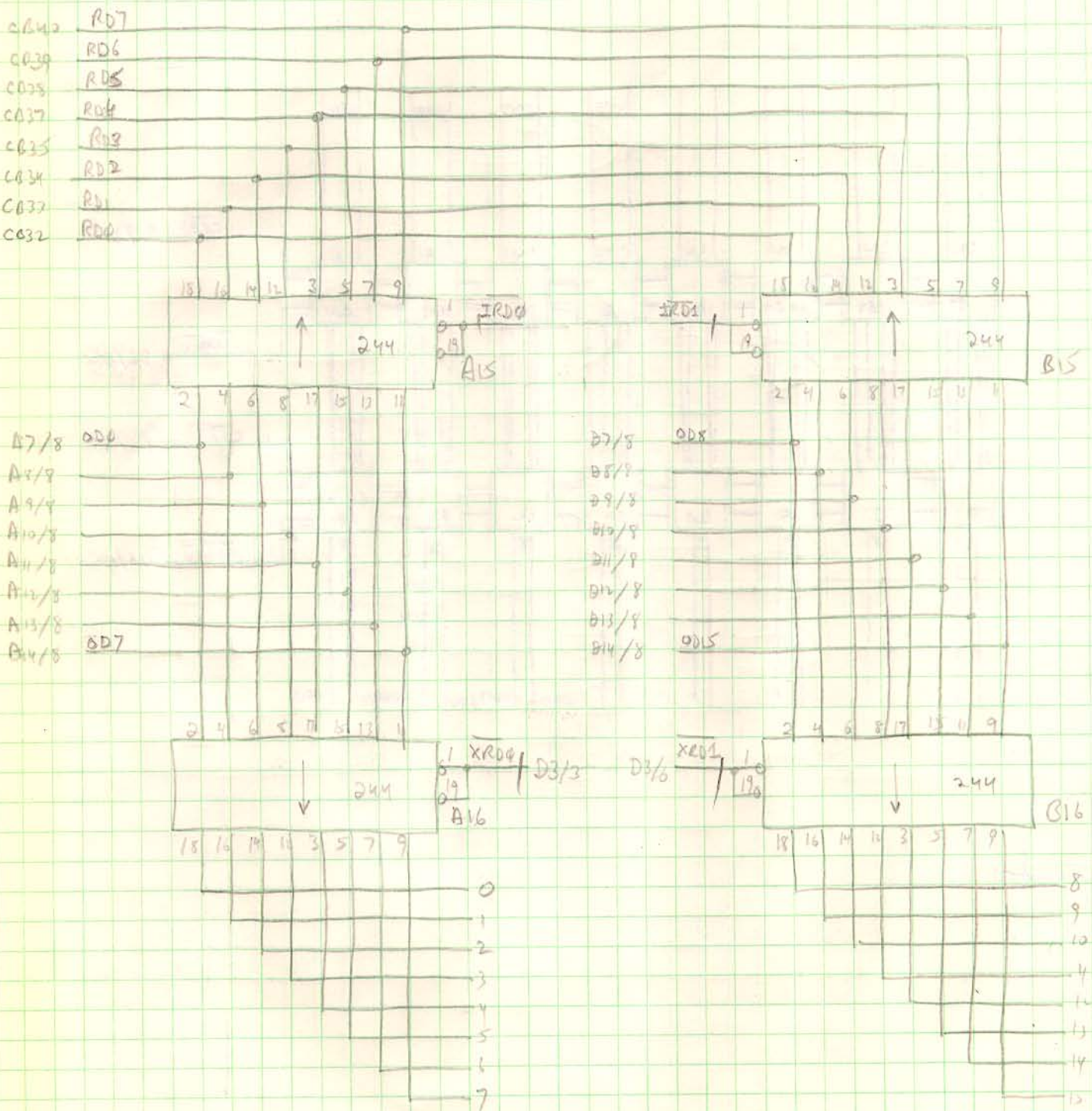
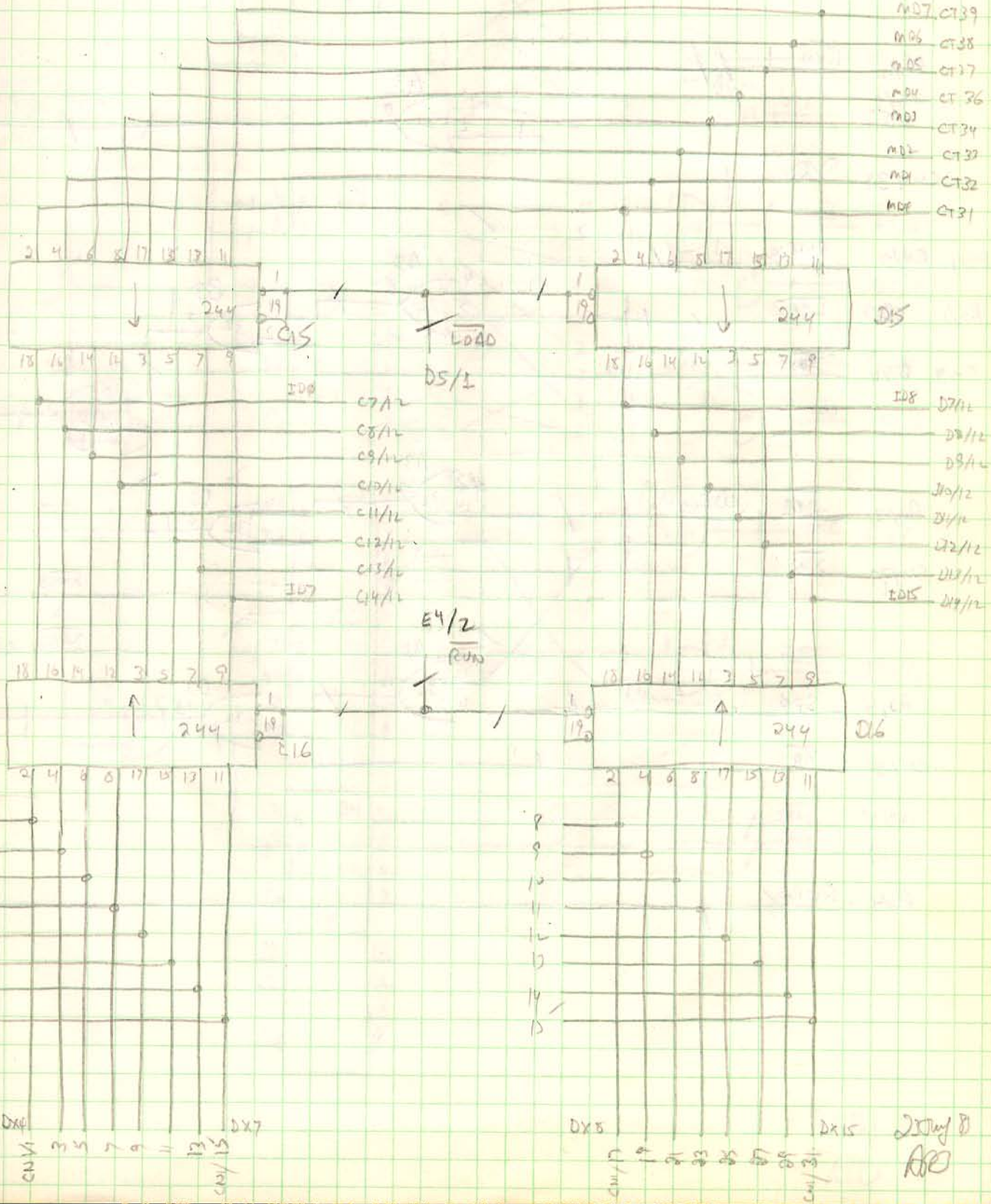
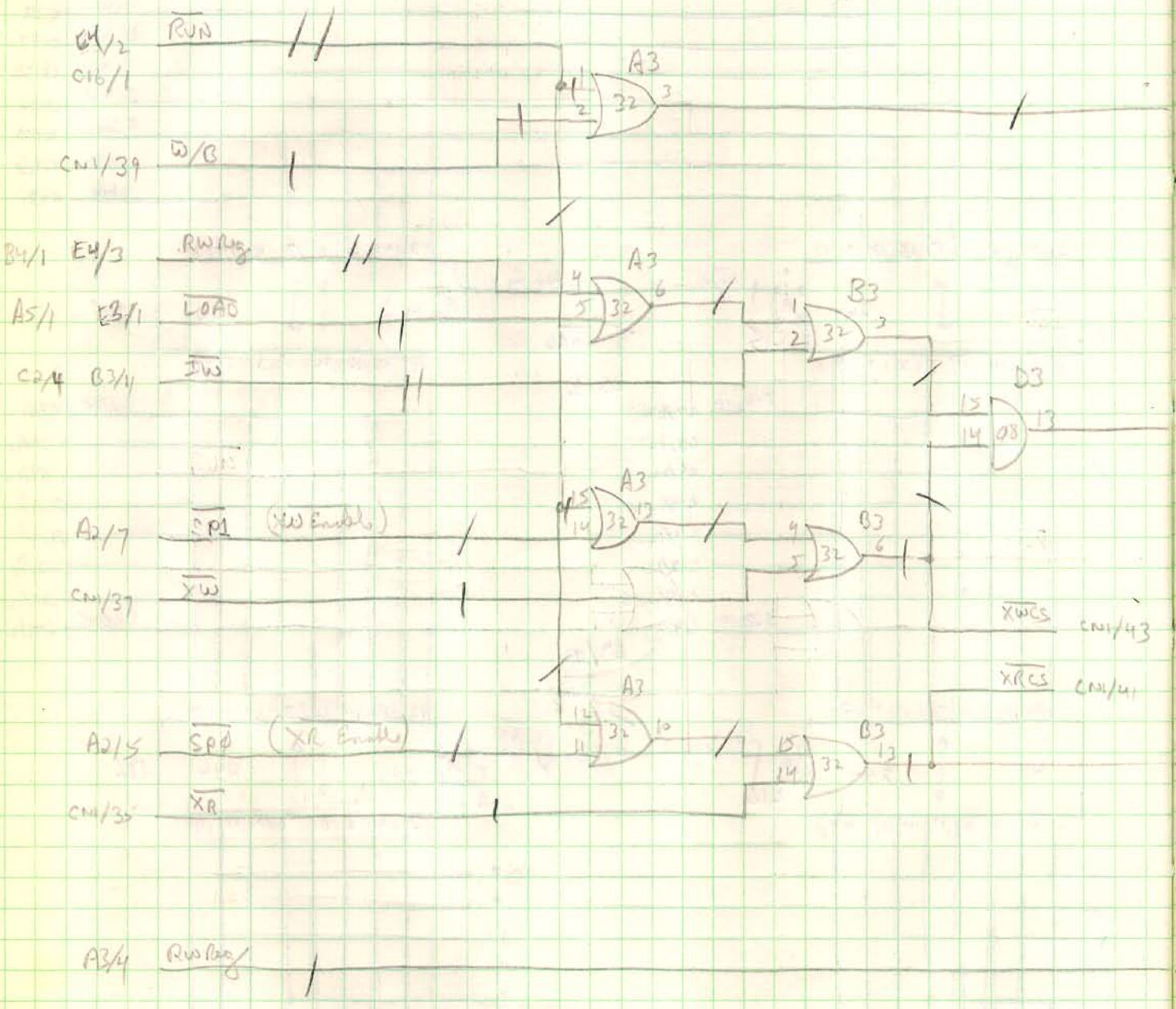
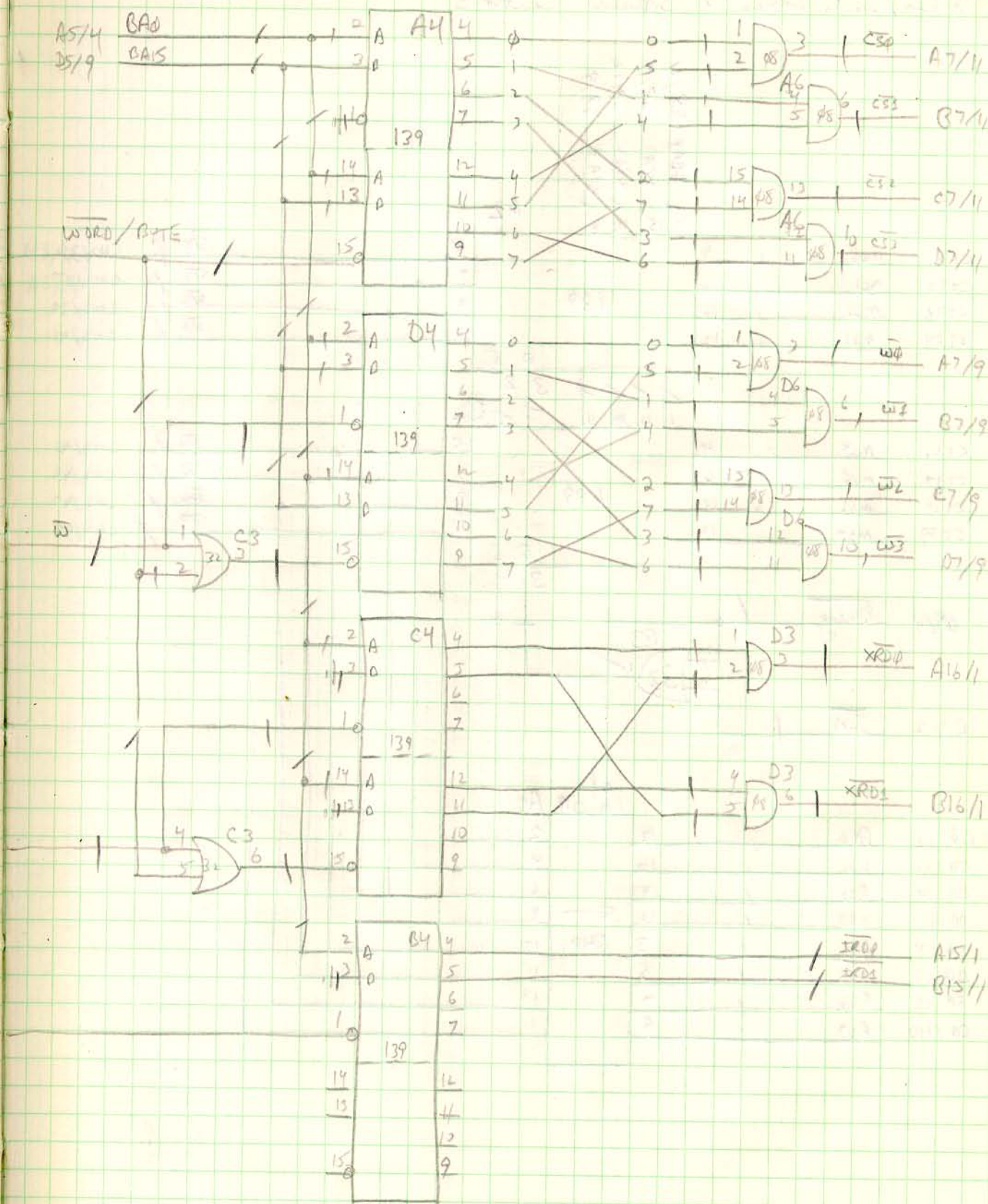
Data Multiplexers




MD7 CT39
MD6 CT38
MD5 CT37
MD4 CT36
MD3 CT34
MD2 CT33
MD1 CT32
MD0 CT31
244
C15
LOAD
DS/1
D15
IDØ
IØ7
C7A/12
C8/12
C9/12
C10/12
C11/12
C12/12
C13/12
C14/12
ID8
ID15
D7/12
D8/12
D9/12
D10/12
D11/12
D12/12
D13/12
D14/12
E4/2
READ
C16
D16
DX4
DX7
DX8
DX15
DXMy 80
ABC

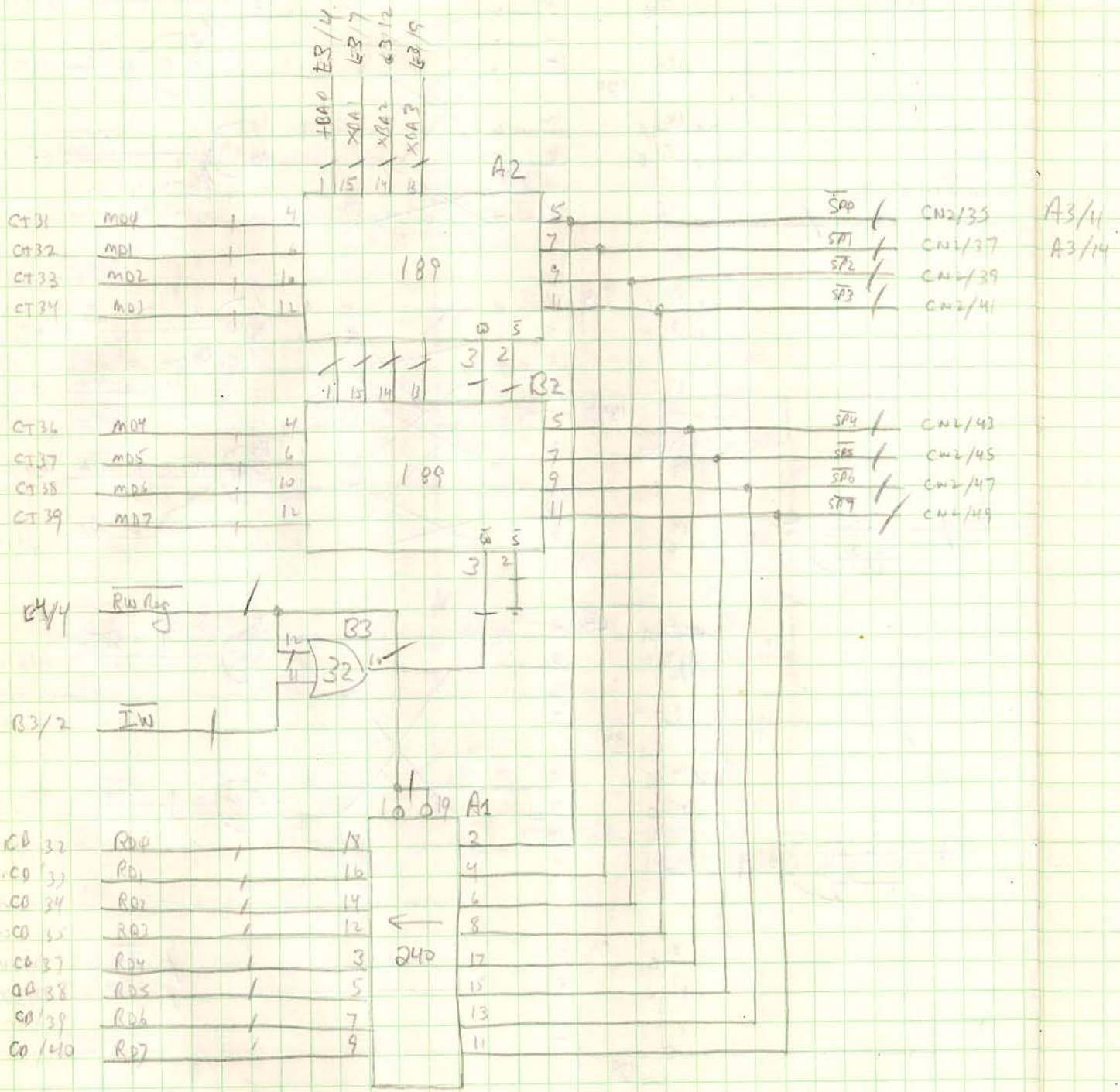
Memory Select Logic / Buffer Control




A5/4
D5/9
BA0
BA15
A4
139
WORD/BYTE
D4
W
C3
C4
B4
A7/11
B7/11
C7/11
D7/11
A7/9
B7/9
C7/9
D7/9
A16/1
B16/1
A15/1
B15/1

23 July 83

X Read/Write Enables & Special Controls



A3/11
A3/14

23 July 80
ABB

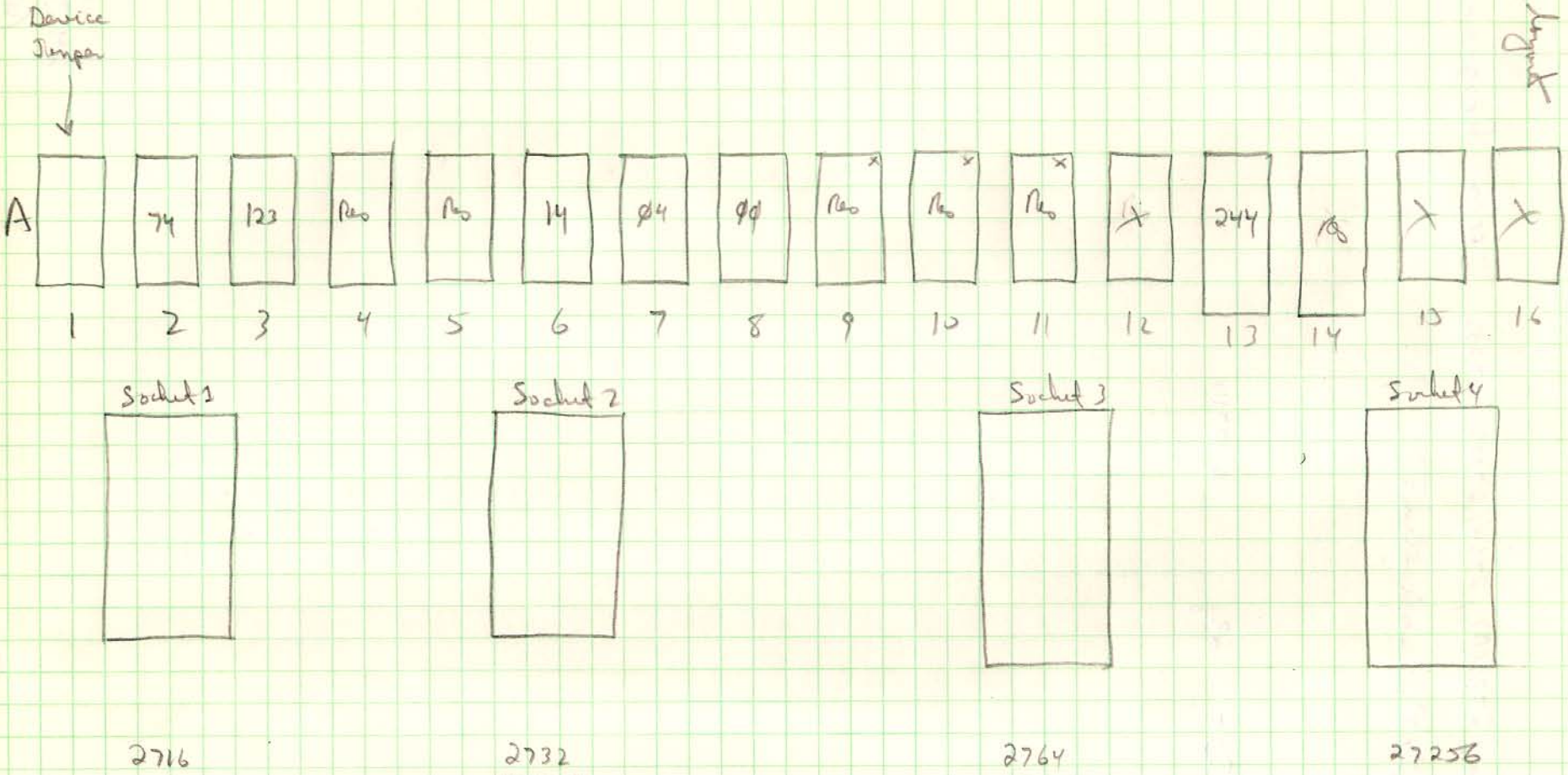
2716/2732(A)/2764/27128/27256 EPROM Programmer

(Intel specifications)

ID = 23_8 @ 177111

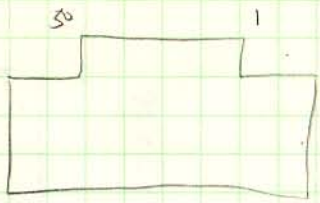
24 July 81
ARO

Board layout



100pin I/O Connectors

Top Side CT (Right to left)



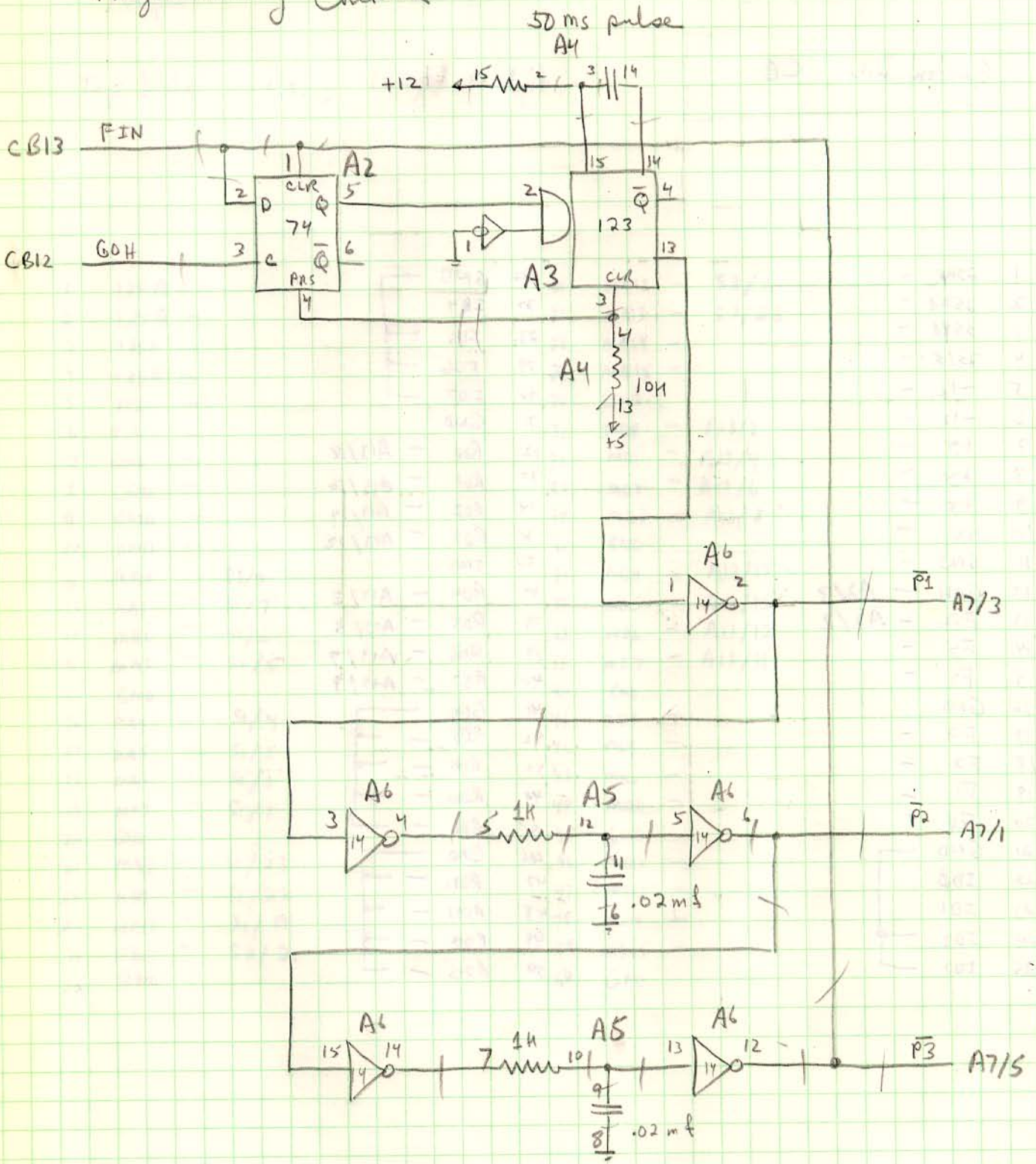
1	+25A	—	
2	+25A	—	
3	+25B	—	
4	+25B	—	
5	+12	—	
6	+12	—	
7	GND	—	
8	GND	—	
9	GND	—	
10	GND	—	
11	MA0	—	S1/8
12	MA1	—	S1/7
13	MA2	—	S1/6
14	MA3	—	S1/5
15	GND		
16	MA4	—	S1/4
17	MA5	—	S1/3
18	MA6	—	S1/2
19	MA7	—	S1/1
20	GND		
21	MA8	—	S1/23
22	MA9	—	S1/22
23	MA10	—	S1/19
24	MA11	—	S2/21
25	GND		
26	MA12	—	S3/2
27	MA13	—	S3/26
28	MA14	—	
29	MA15	—	
30	GND		
31	MD0	—	A13/2
32	MD1	—	A13/4
33	MD2	—	A13/6
34	MD3	—	A13/8
35	GND		
36	MD4	—	A13/17
37	MD5	—	A13/15
38	MD6	—	A13/13
39	MD7	—	A13/11
40	GND		
41	MD8	—	
42	MD9	—	
43	MD10	—	
44	MD11	—	
45	GND		
46	MD12	—	
47	MD13	—	
48	MD14	—	
49	MD15	—	
50	GND		

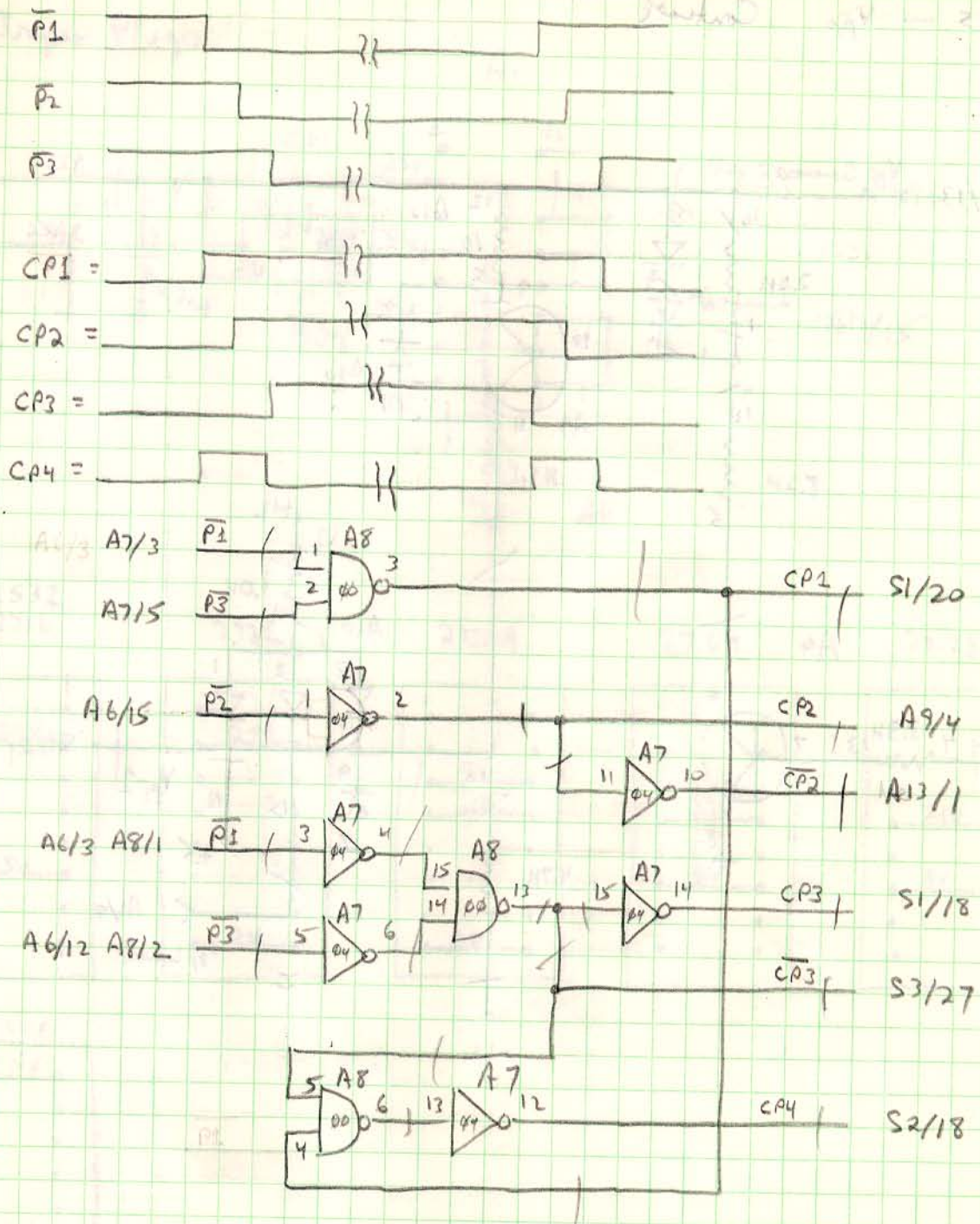
Bottom Side CB

1	25AR	–
2	25AR	–
3	25BR	–
4	25BR	–
5	–12	–
6	–12	–
7	+5	–
8	+5	–
9	+5	–
10	+5	–
11	GND	
12	GOH	– A2/3
13	FIN	– A2/2
14	F5	–
15	F4	–
16	GND	
17	F3	–
18	F2	–
19	F1	–
20	F0	–
21	GND	
22	ID0	
23	ID1	
24	ID2	
25	ID3	
26	GND	
27	ID4	
28	FD5	
29	FD6	
30	FD7	
31	GND	
32	RD0	– A13/18
33	RD1	– A13/16
34	RD2	– A13/14
35	RD3	– A13/12
36	GND	
37	RD4	– A13/3
38	RD5	– A13/5
39	RD6	– A13/7
40	RD7	– A13/9
41	GND	
42	RD8	–
43	RD9	–
44	RD10	–
45	RD11	–
46	GND	
47	RD12	–
48	RD13	–
49	RD14	–
50	RD15	–

24 July 83
ARO

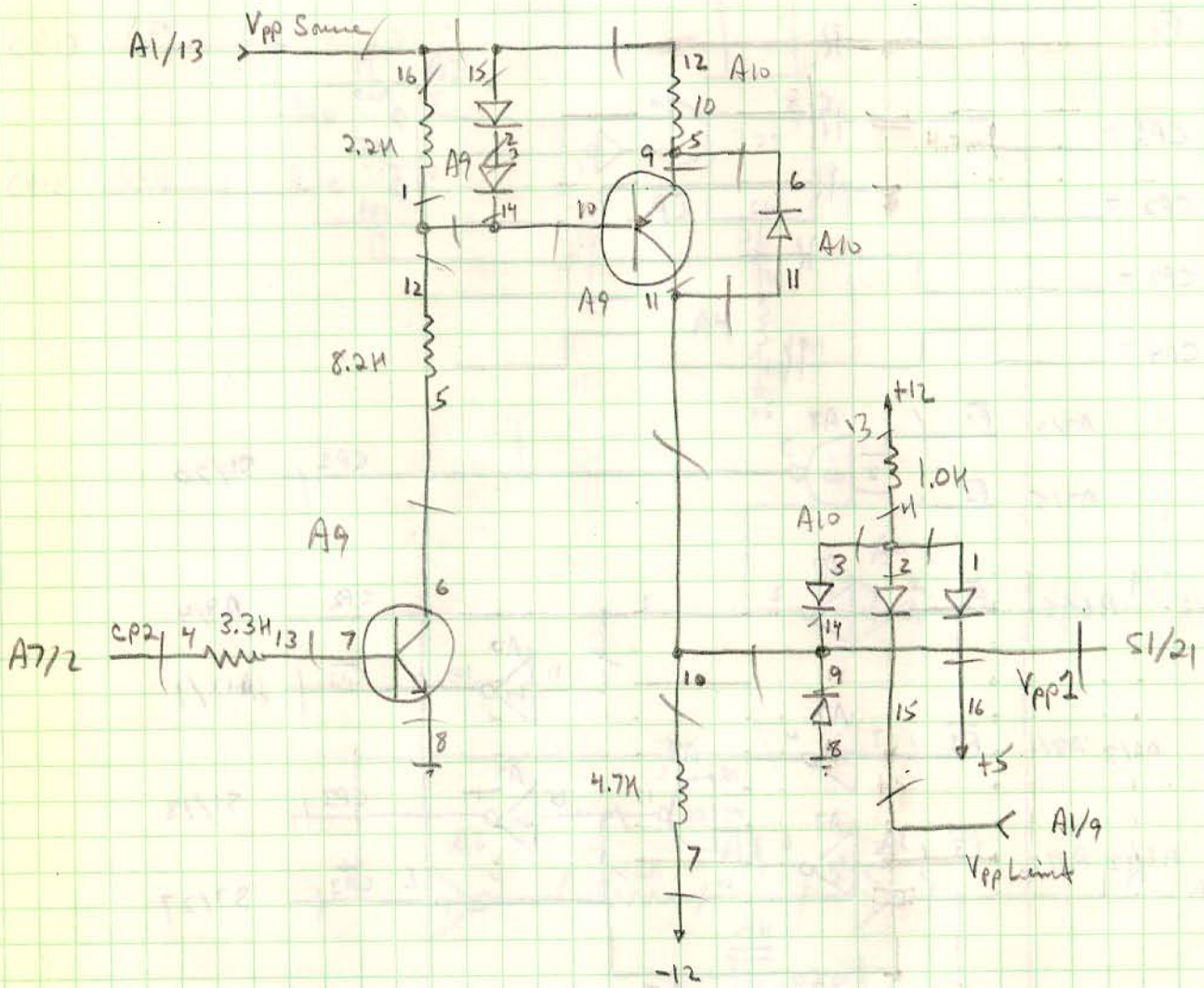
Programming Control




P̄1
P̄2
P̄3
CP1 =
CP2 =
CP3 =
CP4 =
A7/3
A7/5
A6/15
A6/3 A8/1
A6/12 A8/2
A8
A7
CP1
S1/20
CP2
A9/4
CP̄2
A13/1
CP3
S1/18
CP̄3
S3/27
CP4
S2/18

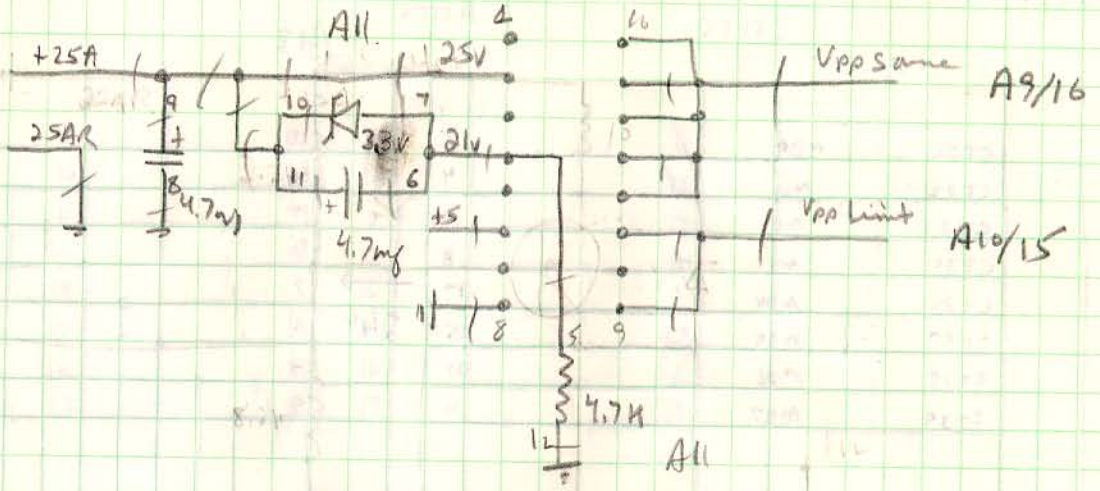
24 JUL 83
BRD

+5 — V_{PP} Control

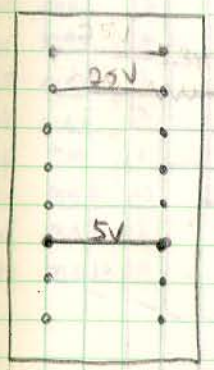


Jumper Plugs

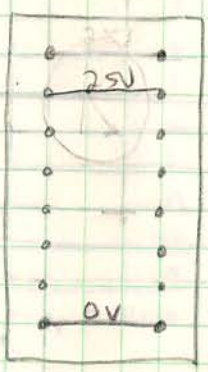
A1



2532
2716

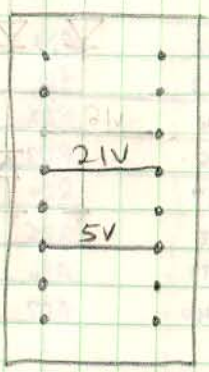


2732

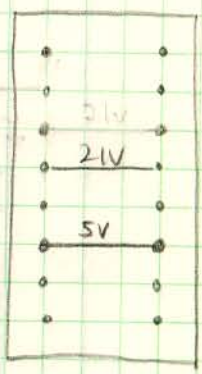


2732A

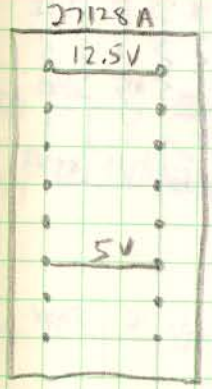
2764



27128

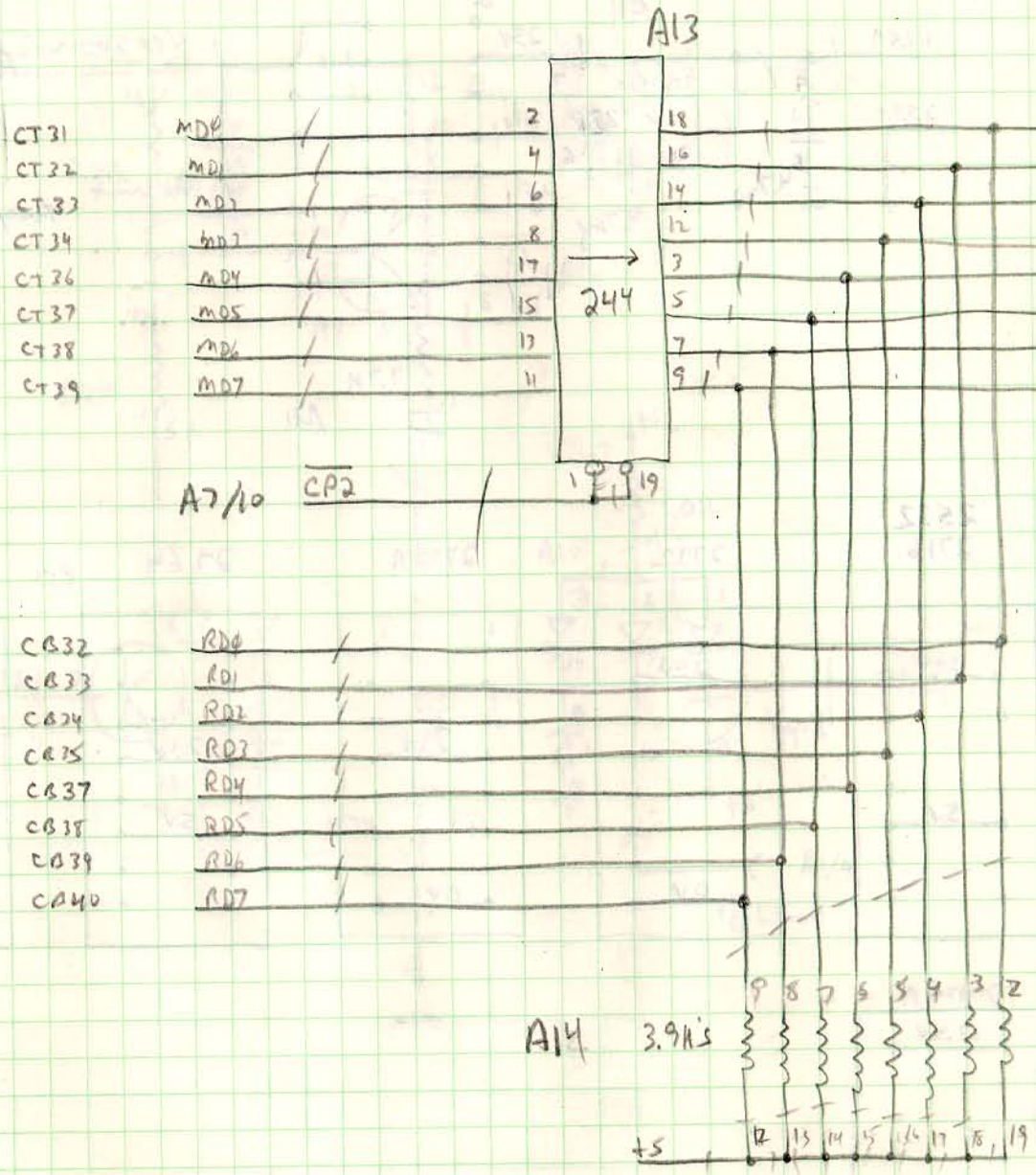


27128A



24 July 83

Data Driver & EPROM Socket Wiring

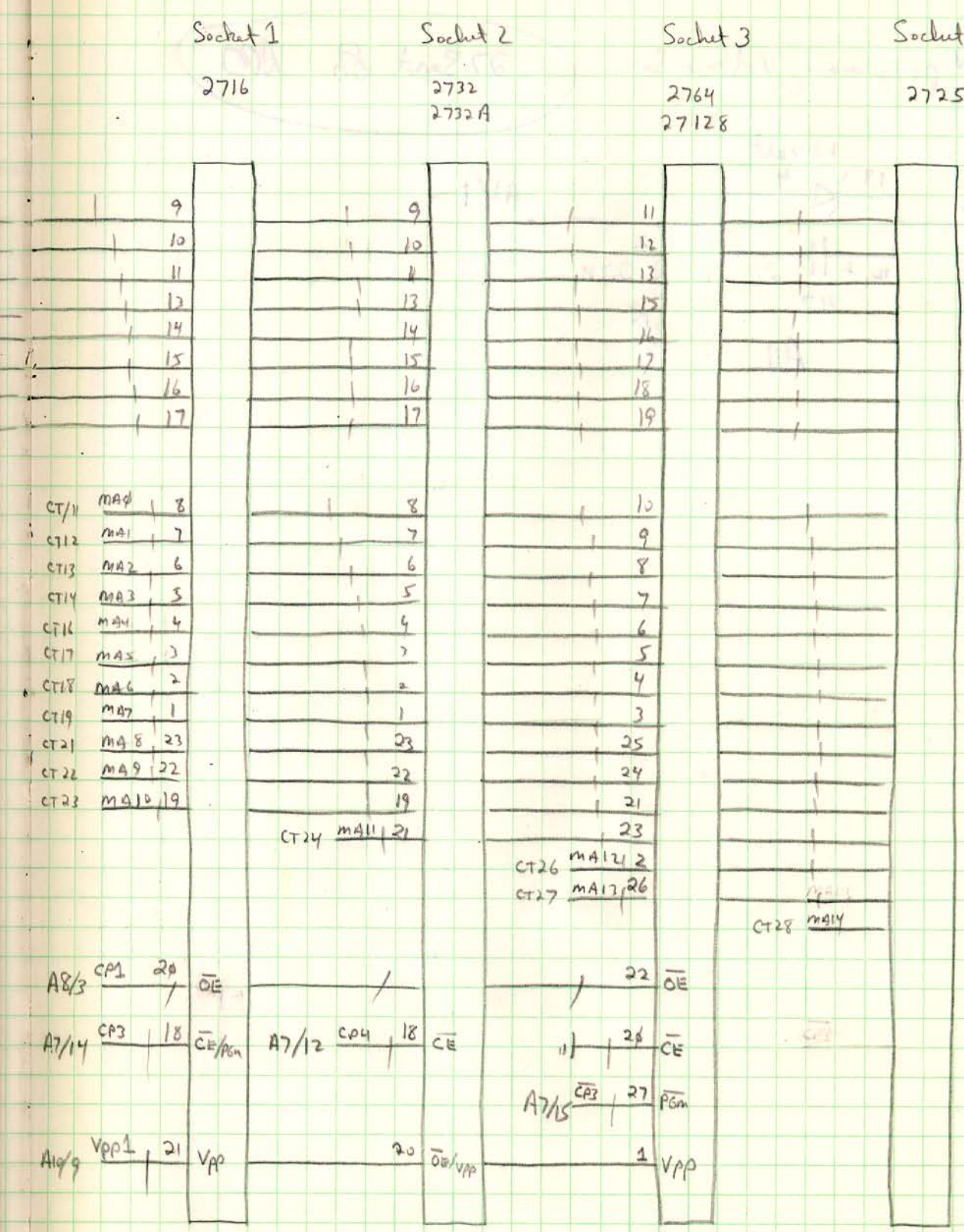


CT/11 MA
CT12 MA
CT13 MA
CT14 MA
CT16 MA
CT17 MA
CT18 MA
CT19 M
CT21 M
CT22 M
CT23 M

A8/3 CP

A7/14 CP

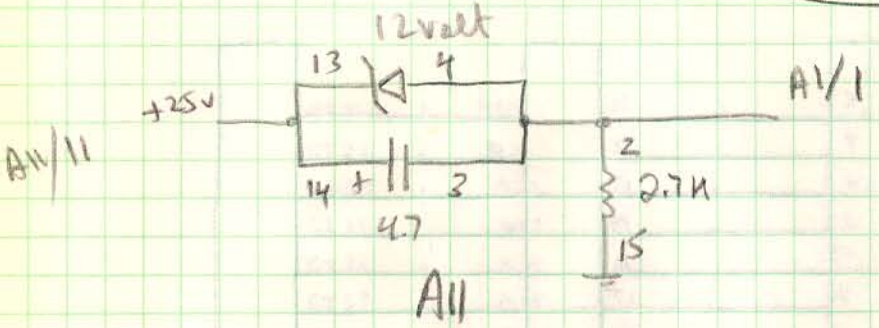
A10/9 VP



24 July 83
ASD

12.5 V Programming Voltage Source

27 Sept 88 ARD



B. 2716 Programming

Initially, and after each erasure, all bits of the 2716 are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The 2716 is programmed by applying a 50 ms, TTL programming pulse to the $\overline{CE}$/PGM pin with the $\overline{OE}$ input high and the V_{PP} supply at 25V ± 1V. Any location may be programmed at any time—either individually, sequentially, or randomly. The programming time for a single bit is only 50 ms and for all bits is approximately 100 and 50 seconds for the 2716. The detailed programming specifications and timing waveforms are given in the following tables and figures.

CAUTION: The V_{CC} and V_{PP} supplied must be sequenced on and off such that V_{CC} is applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} to prevent damage to the 2716. The maximum allowable voltage during programming which may be applied to the V_{PP} with respect to ground is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding the 26-volt maximum specification. For convenience in programming, the 2716 may be verified with the V_{PP} supply at 25V ± 1V. During normal read operation, however, V_{PP} must be at V_{CC}.

2716 PROGRAM CHARACTERISTICS(1)

T_A = 25°C ±5°C, V_{CC}[2] = 5V ±5%, V_{PP}[2,3] = 25V ±1V

D.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Input Current (for Any Input)			10	µA	V_{IN} = 5.25V/0.45
I_{PP1}	V_{PP} Supply Current			5	mA	$\overline{CE}$/PGM = V_{IL}
I_{PP2}	V_{PP} Supply Current During Programming Pulse			30	mA	$\overline{CE}$/PGM = V_{IH}
I_{CC}	V_{CC} Supply Current			100	mA	
V_{IL}	Input Low Level	-0.1		0.8	V	
V_{IH}	Input High Level	2.0		V_{CC}+1	V	

A.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{AH}	Address Hold Time	2			µs	
t_{OEH}	$\overline{OE}$ Hold Time	2			µs	
t_{DH}	Data Hold Time	2			µs	
t_{DF}	Output Enable to Output Float Delay	0		120	ns	$\overline{CE}$/PGM = V_{IL}
t_{OE}	Output Enable to Output Delay			120	ns	$\overline{CE}$/PGM = V_{IL}
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

NOTES:
1. Intel's standard product warranty applies only to devices programmed to specifications described herein.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The 2716/2758 must not be inserted into or removed from a board with V_{PP} at 25 ±1V to prevent damage to the device.
3. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification.

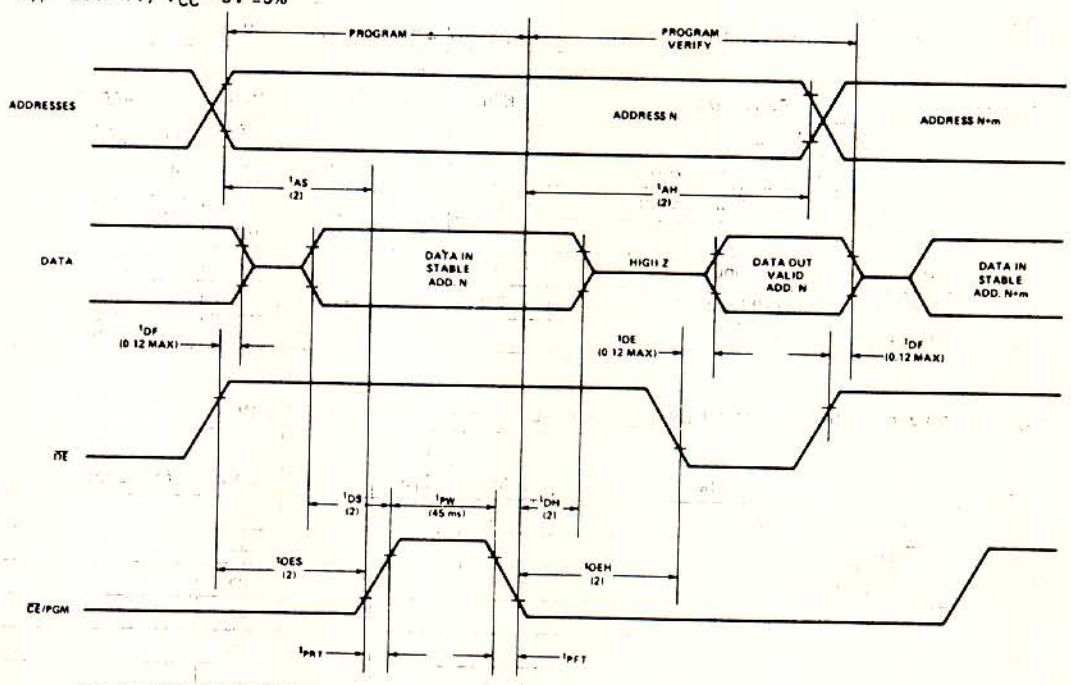
A.C. Conditions of Test:

V_{CC} ..... 5V ± 5%
V_{PP} ..... 25V ± 1V
Input Rise and Fall Times (10% to 90%) ..... 20 ns

Input Pulse Levels ..... 0.8V to 2.2V
Input Timing Reference Level ..... 1V and 2V
Output Timing Reference Level ..... 0.8V and 2V

PROGRAMMING WAVEFORMS

V_{PP} = 25V ±1V, V_{CC} = 5V ±5%



NOTE ALL TIMES SHOWN IN PARENTHESES ARE MINIMUM TIMES AND ARE μSEC UNLESS OTHERWISE NOTED

C. 2732 Programming

Initially, and after each erasure, all bits of the 2732 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2732 is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 25V. It is required that a 0.1 μF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2732 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple 2732s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2732s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2732s.

Program Inhibit

Programming of multiple 2732s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel 2732s may be common. A TTL level program pulse applied to a 2732's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 25V will program that 2732. A high level $\overline{CE}$ input inhibits the other 2732s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.8V to 2.2V
Input Timing Reference Level.....1V and 2V
Output Timing Reference Level.....0.8V and 2V

PROGRAMMING[1]

D.C. PROGRAMMING CHARACTERISTICS: $T_A = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$

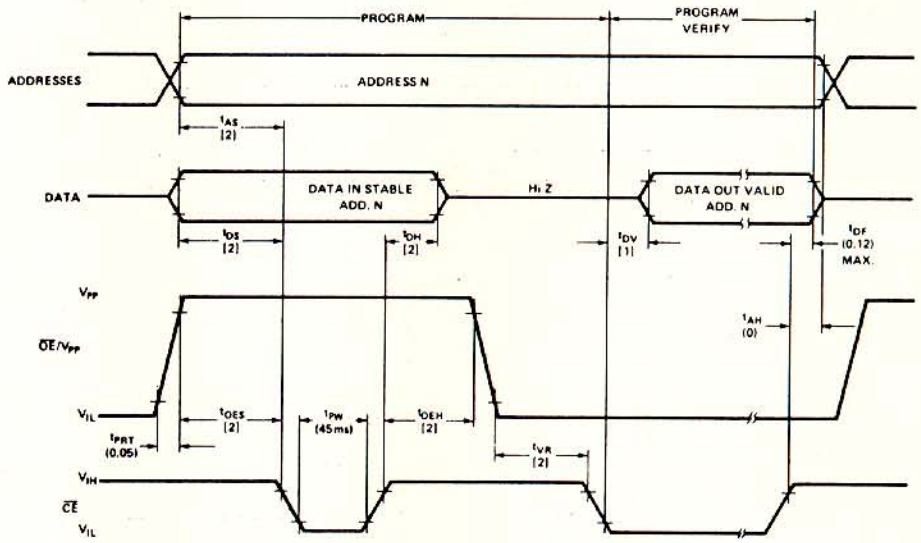
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_{LI}	Input Current (All Inputs)			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{OL}	Output Low Voltage During Verify			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4			V	$I_{OH} = -400$ μA
I_{CC}	V_{CC} Supply Current		85	150	mA	
V_{IL}	Input Low Level (All Inputs)	−0.1		0.8	V	
V_{IH}	Input High Level (All Inputs Except OE/V_{PP})	2.0		$V_{CC}+1$	V	
I_{PP}	V_{PP} Supply Current			50	mA	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$

A.C. PROGRAMMING CHARACTERISTICS: $T_A = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{OEH}	OE Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Chip Enable to Output Float Delay	0		120	ns	
t_{DV}	Data Valid from $\overline{CE}$			1	μs	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$
t_{PW}	$\overline{CE}$ Pulse Width During Programming	45	50	55	ms	
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming	50			ns	
t_{VR}	V_{PP} Recovery Time	2			μs	

Note: 1. When programming the 2732, a 0.1 μF capacitor is required across OE/V_{PP} and ground to suppress spurious voltage transients which may damage the device.

PROGRAMMING WAVEFORMS

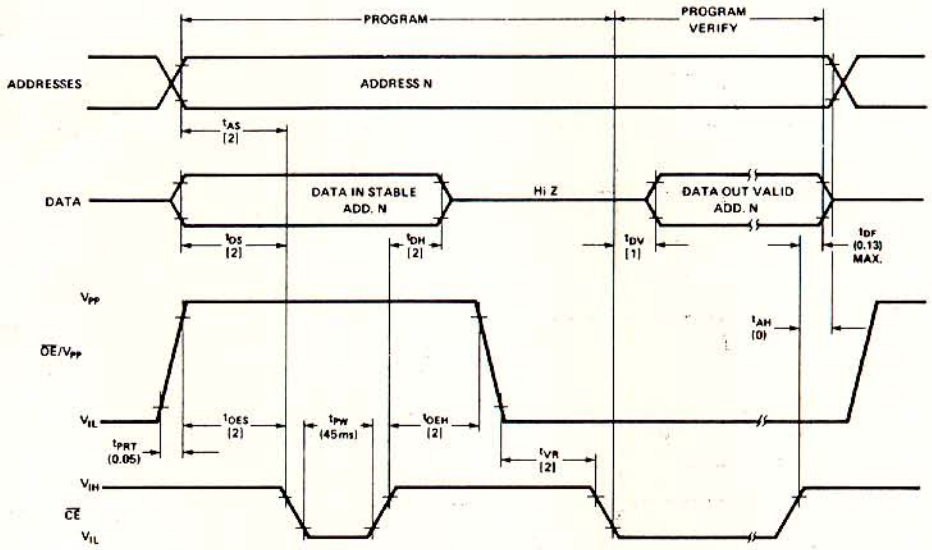


1. ALL TIMES SHOWN IN [ ] ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS 1V FOR A V_{IL} AND 2V FOR A V_{IH}.

D. 2732A Programming

The 2732A is programmed exactly as the 2732 except that $V_{PP} = 21V \pm 0.5V$.

PROGRAMMING WAVEFORMS



1. ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS 1V FOR A V_{IL} AND 2V FOR A V_{IH}.

E. 2764 Programming

Programming is the same as Intel's 2732A except that $\overline{OE}/V_{PP}$ is not multiplexed. They have separate pins. Like the 2732A, ***exceeding 21.5V will damage the 2764.***

Initially, and after each erasure, all bits of the 2764 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2764 is in the programming mode when V_{PP} input is at 21V and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 21V. When the address and data are stable, a 50 msec, active low, TTL program pulse is applied to $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec.

Programming of multiple 2764s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2764s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled 2764s.

PROGRAMMING

D.C. PROGRAMMING CHARACTERISTICS: T_A = 25 ±5°C, V_{CC} = 5V ±5%, V_{PP} = 21V ±0.5V (see Note 1)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Unit	
I_{LI}	Input Current (All Inputs)			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{OL}	Output Low Voltage During Verify			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	2.4			V	I_{OH} = − 400 μA
I_{CC2}	V_{CC} Supply Current (Active)			150	mA	
V_{IL}	Input Low Level (All Inputs)	−0.1		0.8	V	
V_{IH}	Input High Level	2.0		V_{CC}+1	V	
I_{PP}	V_{PP} Supply Current			30	mA	$\overline{CE} = V_{IL} = \overline{PGM}$

A.C. PROGRAMMING CHARACTERISTICS: T_A = 25 ±5°C, V_{CC} = 5V ±5%, V_{PP} = 21V ±0.5V (see Note 1)

Symbol	Parameter	Limits				Test Conditions*
		Min.	Typ.	Max.	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Chip Enable to Output Float Delay	0		130	ns	
t_{VS}	V_{PP} Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Pulse Width During Programming	45	50	55	ms	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

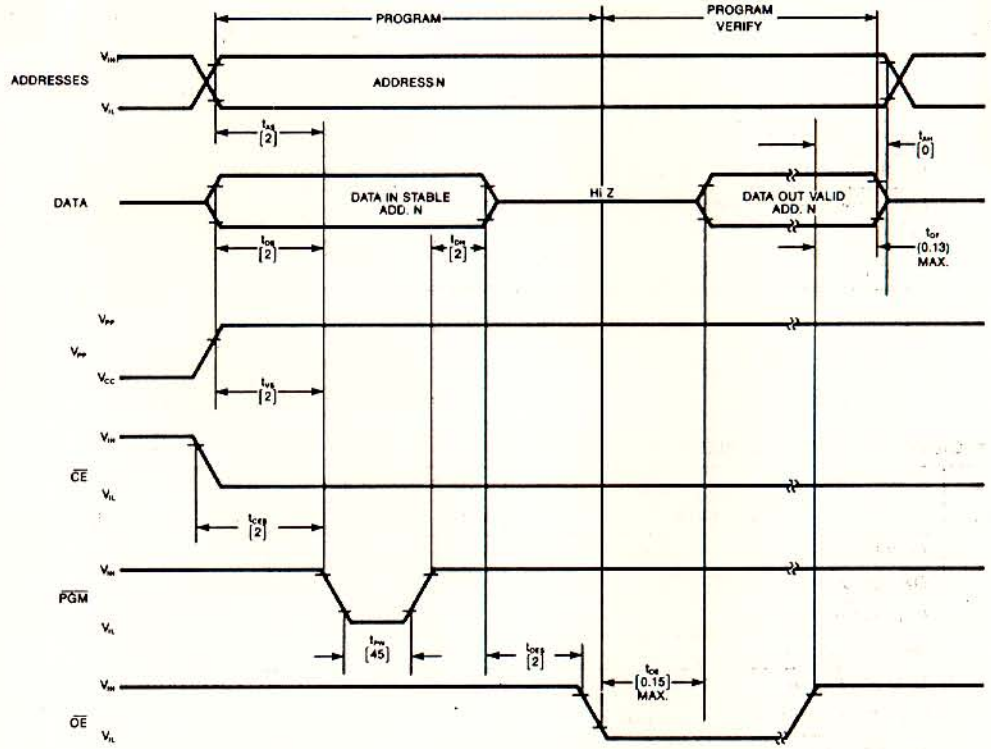
*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels . . . . . 0.8V to 2.2V
Input Timing Reference Level . . . . . 1V and 2V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTE: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AFN-01647A

PROGRAMMING WAVEFORMS



1. ALL TIMES SHOWN IN [ ] ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS 1V FOR A V_{IL} AND 2V FOR A V_{IH}.

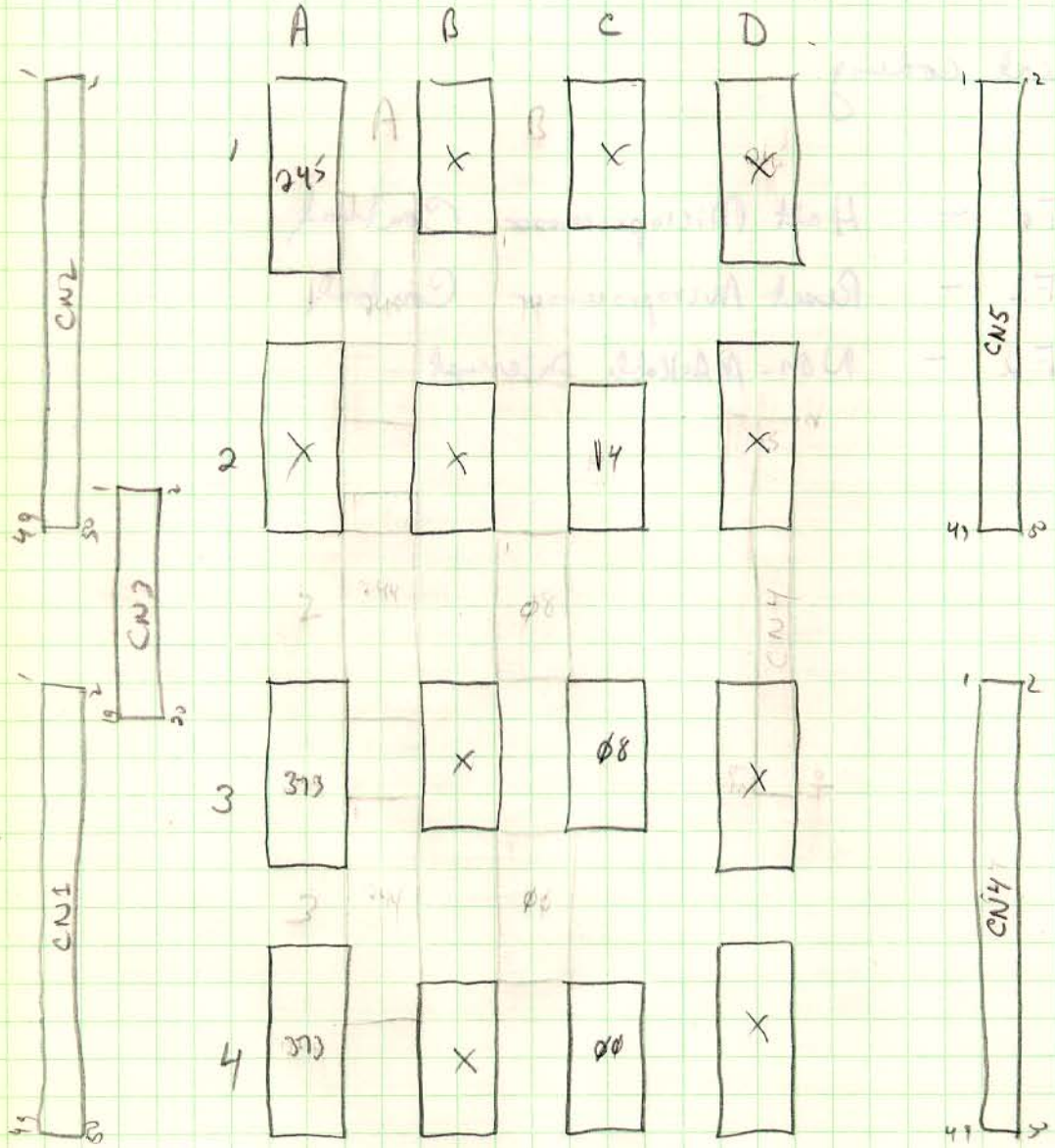
H-BUS Diagnostic Connector Adapter to Expanded PRAM Card

Special coding

F0 – Halt Microprocessor Control
F1 – Reset Microprocessor Control
F2 – Non-Maskable Interrupt

25 July 88

Board Layout

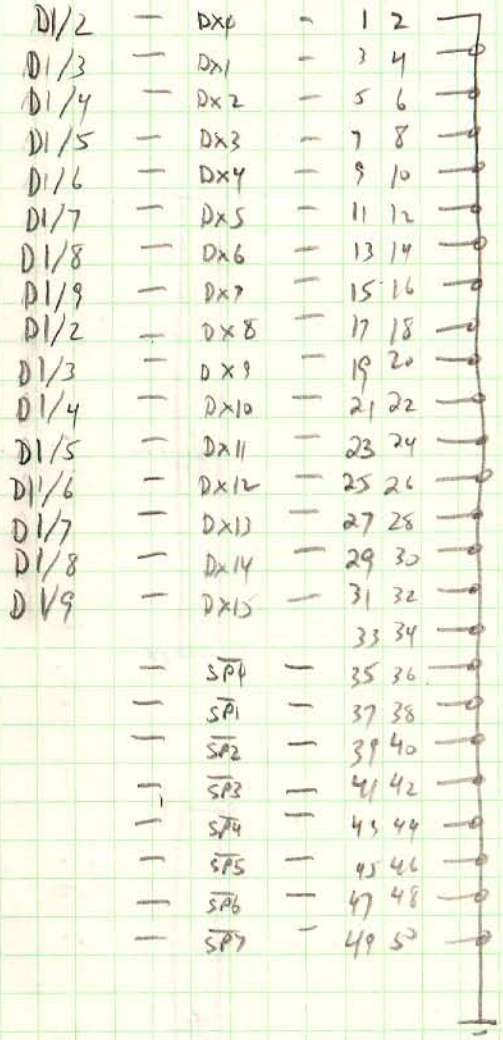


PRAM I/O Connectors

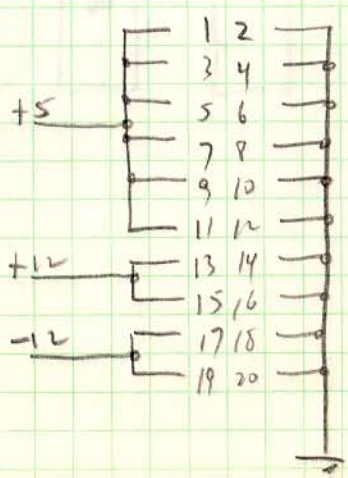
CN1

D1 == A1

CN2



CN3



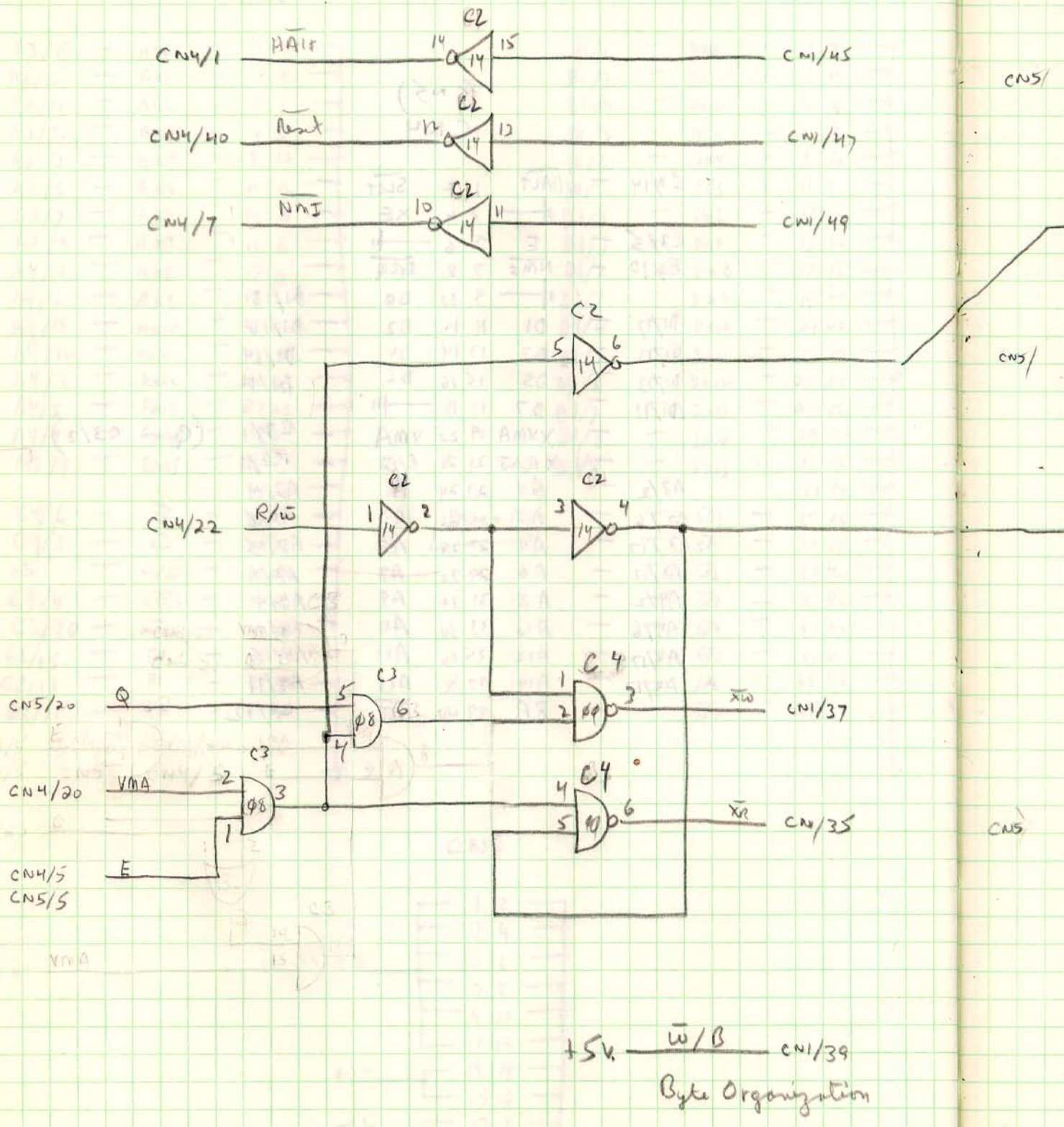
H-BUS Diagnostic Connector

(CN5)
CN4

C2/14	—	$\overline{HALT}$	1	2	$\overline{SLCT}$	—	
		⏚	3	4	XE	—	
C3/5	—	E	5	6			
C2/10	—	$\overline{NMI}$	7	8	$\overline{IRQ}$	—	
		⏚	9	10	D0	—	D1/18
D1/17	—	D1	11	12	D2	—	D1/16
D1/15	—	D3	13	14	D4	—	D1/14
D1/13	—	D5	15	16	D6	—	D1/12
D1/11	—	D7	17	18			
	—	XVMA	19	20	VMA	—	C3/1 (Q — C3/2)
	—	XR/$\overline{W}$	21	22	R/$\overline{W}$	—	E2/1
A3/2	—	A0	23	24	A1	—	A3/4
A3/6	—	A2	25	26	A3	—	A3/8
A3/17	—	A4	27	28	A5	—	A3/15
A3/13	—	A6	29	30	A7	—	A3/11
A4/2	—	A8	31	32	A9	—	A4/4
A4/6	—	A10	33	34	A11	—	A4/8
A4/17	—	A12	35	36	A13	—	A4/15
A4/13	—	A14	37	38	A15	—	A4/11
	—	BA	39	40	$\overline{RST}$	—	C2/12

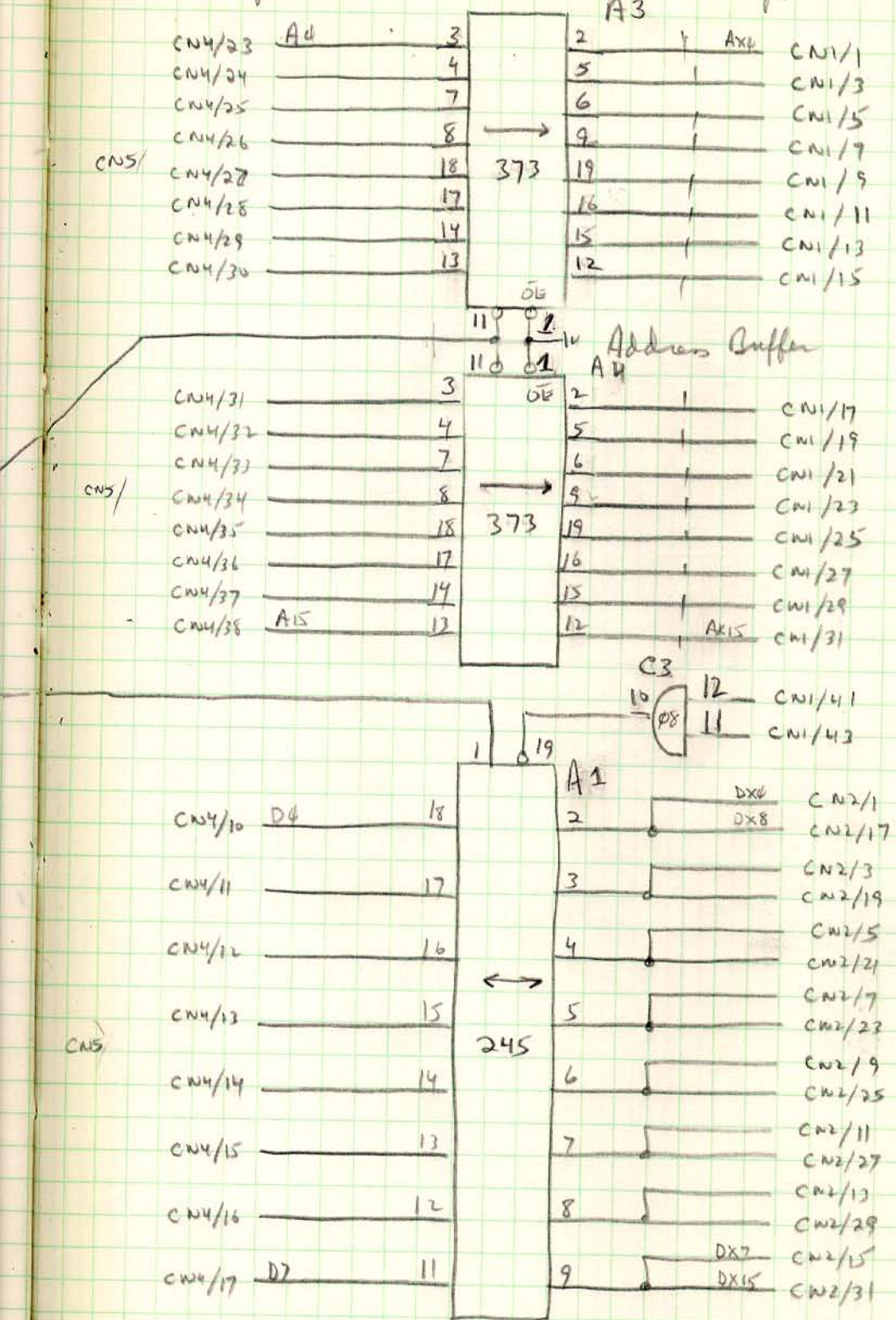
25 July 83
ARB

Control Logic (KBUS connector) (6809 control)



To Diagnostic

Address/Data Buffers To PRAM



25 July 83
ABO

Signetics Generic PROM Programmer

This card will program the following Signetics types

32×8	82S23	O.C.
	82S123	T.S.
256×4	82S126	O.C.
	82S129	T.S.
512×4	82S130	O.C.
	82S131	T.S.
1024×4	82S137	T.S.
512×8	82S141	T.S.
	82S147	T.S.
1024×8	82S180	O.C
	82S181	T.S.
	82LS181	T.S.
	82S183	T.S
	82S2708	T.S
2048×4	82S185	T.S.
2048×8	82S191	T.S

ID = 24_8 @ 177111

22 Jan 1984
ARP

Board Layout

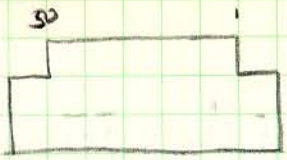
First chips programmed ~ 27 Jan 84

82S181's worked first time!!!

22 Jan 84
ASD

100 pin Connector

TOP Side CT



1	+25A	–	26	MA12	–
2	+25A	–	27	MA13	–
3	+25B	–	28	MA14	–
4	+25B	–	29	MA15	–
5	+12	–	30	GND	–
6	+12	–	31	MD0	–
7	GND	–	32	MD1	–
8	GND	–	33	MD2	–
9	GND	–	34	MD3	–
10	GND	–	35	GND	–
11	MA0	–	36	MD4	–
12	MA1	–	37	MD5	–
13	MA2	–	38	MD6	–
14	MA3	–	39	MD7	–
15	GND	–	40	GND	–
16	MA4	–	41	MD8	–
17	MA5	–	42	MD9	–
18	MA6	–	43	MD10	–
19	MA7	–	44	MD11	–
20	GND	–	45	GND	–
21	MA8	–	46	MD12	–
22	MA9	–	47	MD13	–
23	MA10	–	48	MD14	–
24	MA11	–	49	MD15	–
25	GND	–	50	GND	–

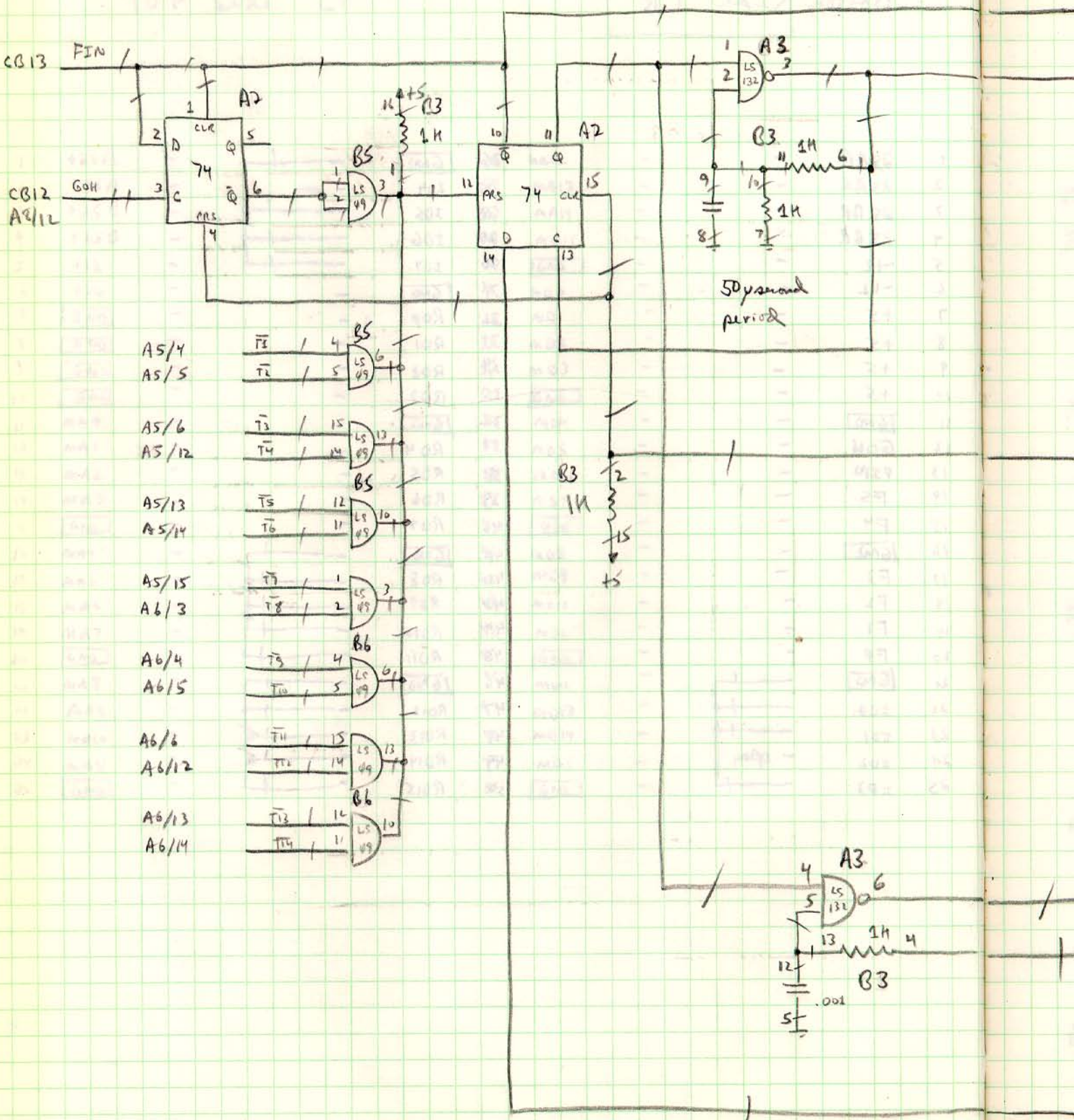
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25

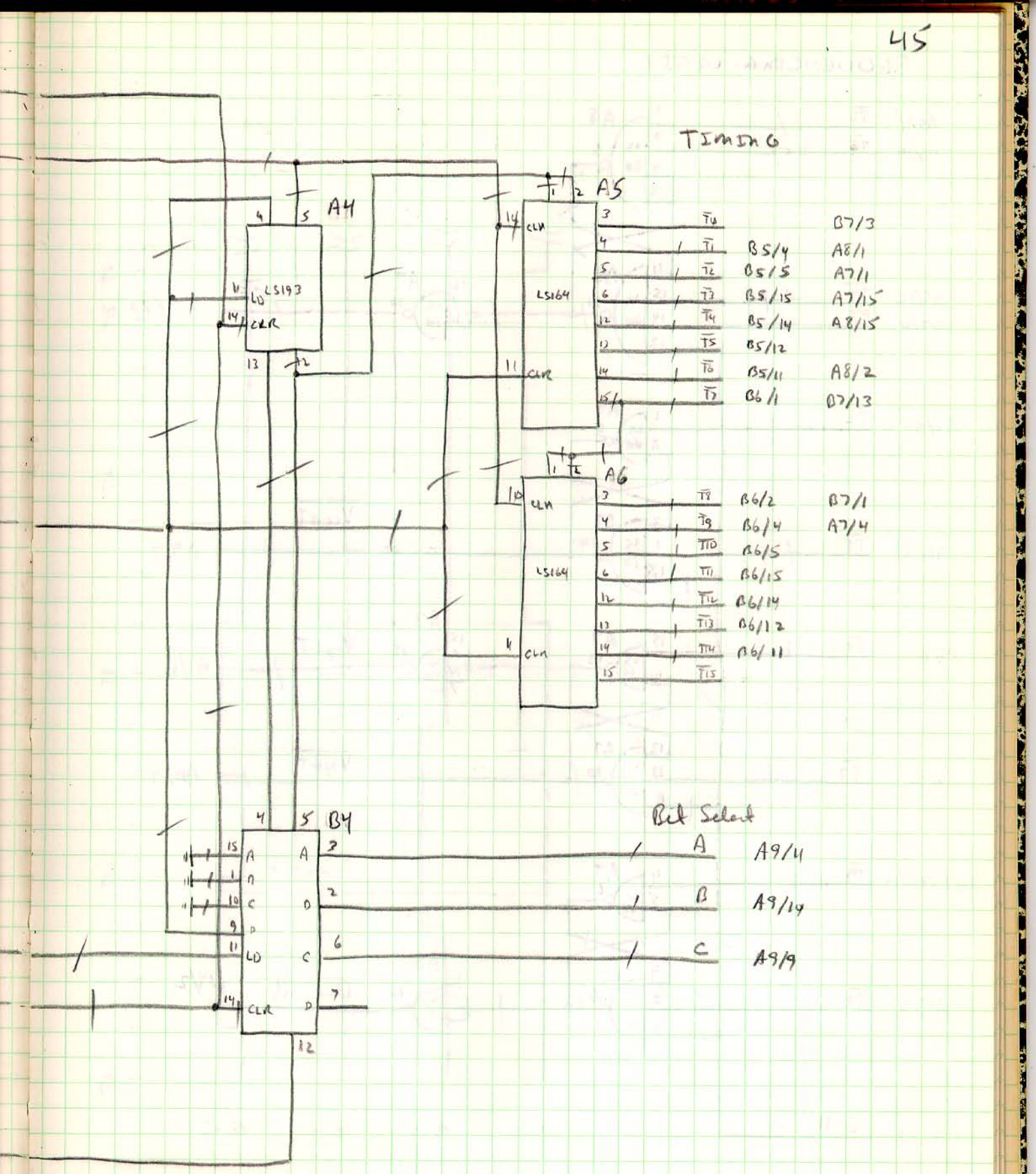
Bottom Side CB

1	25AR	–
2	25AR	–
3	25BR	–
4	25BR	–
5	-12	–
6	-12	–
7	+5	–
8	+5	–
9	+5	–
10	+5	–
11	GND	–
12	GOH	–
13	FIN	–
14	F5	–
15	F4	–
16	GND	–
17	F3	–
18	F2	–
19	F1	–
20	F0	–
21	GND	
22	IO0	
23	IO1	
24	IO2	– open
25	IO3	
26	GND	
27	IO4	– open
28	IO5	
29	IO6	
30	IO7	
31	GND	–
32	RO0	–
33	RO1	–
34	RO2	–
35	RO3	–
36	GND	–
37	RO4	–
38	RO5	–
39	RO6	–
40	RO7	–
41	GND	
42	RO8	
43	RO9	
44	RO10	
45	RO11	
46	GND	
47	RO12	
48	RO13	
49	RO14	
50	RO15	

22 Jan 84
ARO

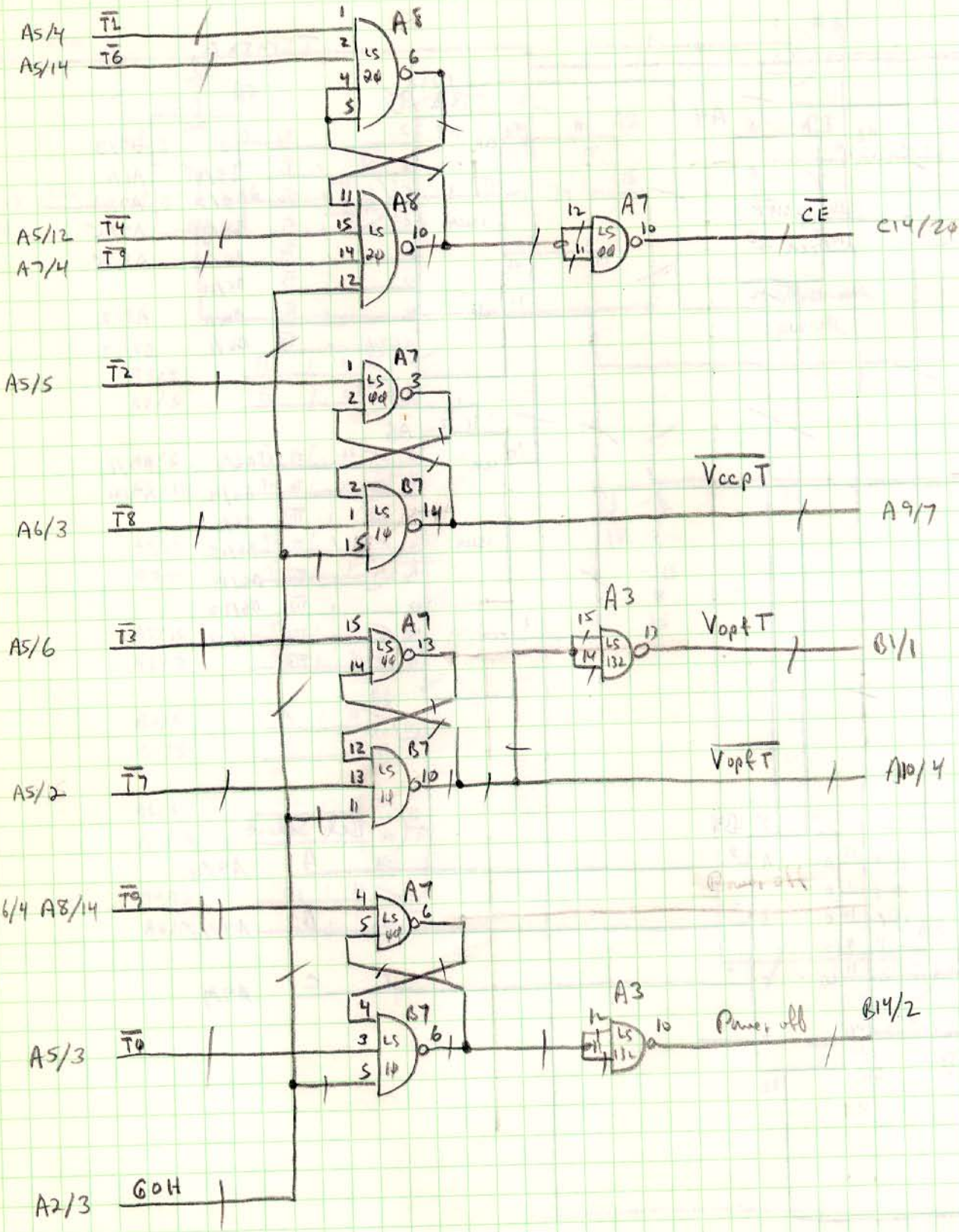
Scan Timer

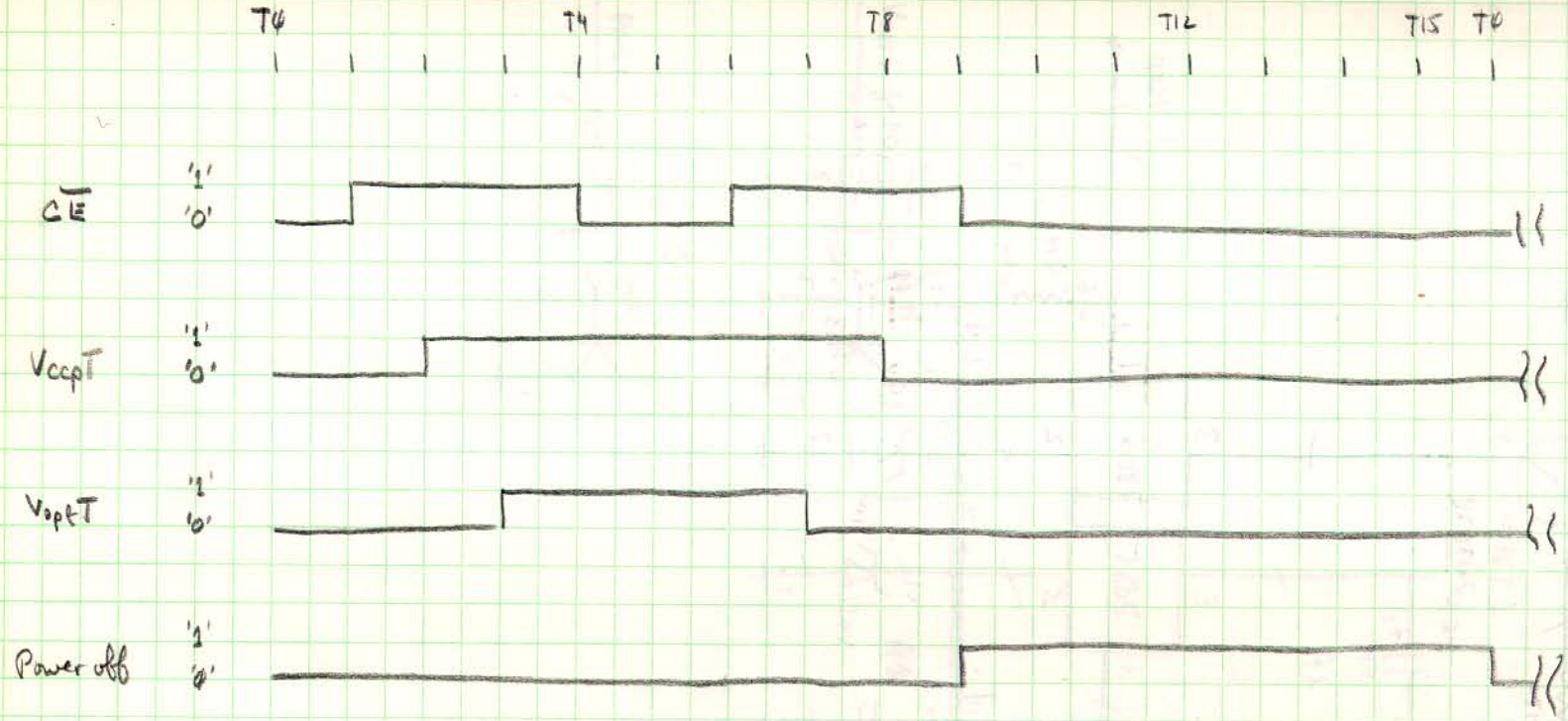

CB13 FIN
A7
74
CLR
D
C
PRS
Q
CB12 A8/12 60H
B5
LS 49
B3 1K
A2
74
PRE
CLR
A3
LS 132
B3 1K
1K
50μsecond period
A5/4
A5/5
A5/6
A5/12
A5/13
A5/14
A5/15
A6/3
A6/4
A6/5
A6/6
A6/12
A6/13
A6/14
B6
B3 1K
+5
A3
LS 132
1K
B3
.001


TIMING
A4
LS193
A5
LS164
A6
LS164
B4
Bit Select
A
B
C
$\overline{T0}$ B7/3
$\overline{T1}$ B5/4 A8/1
$\overline{T2}$ B5/5 A7/1
$\overline{T3}$ B5/15 A7/15
$\overline{T4}$ B5/14 A8/15
$\overline{T5}$ B5/12
$\overline{T6}$ B5/11 A8/2
$\overline{T7}$ B6/1 B7/13
$\overline{T8}$ B6/2 B7/1
$\overline{T9}$ B6/4 A7/4
$\overline{T10}$ B6/5
$\overline{T11}$ B6/15
$\overline{T12}$ B6/14
$\overline{T13}$ B6/12
$\overline{T14}$ B6/11
$\overline{T15}$
A9/4
A9/14
A9/9

22 Jan 84
ARD

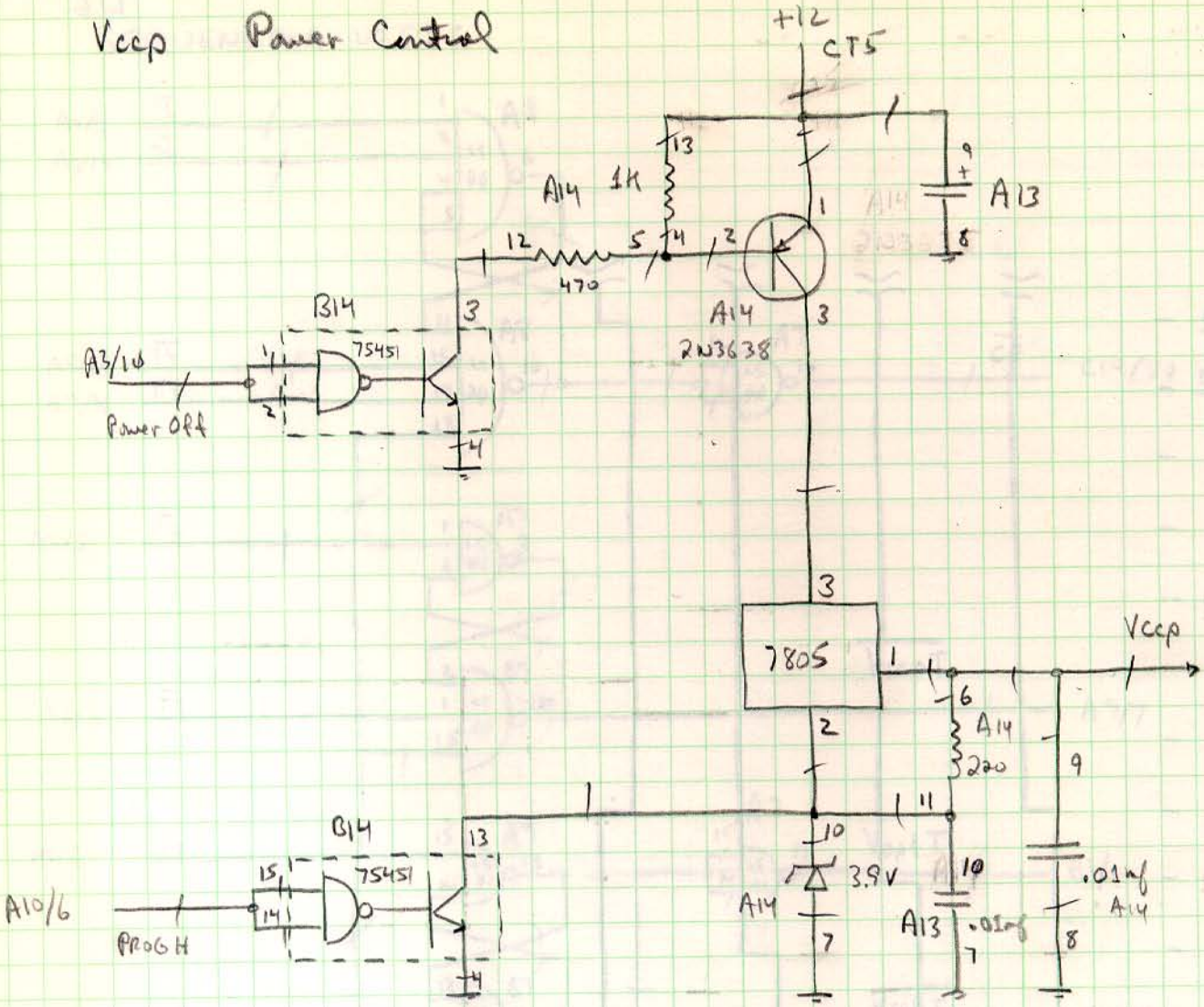
SEQUENCING LOGIC



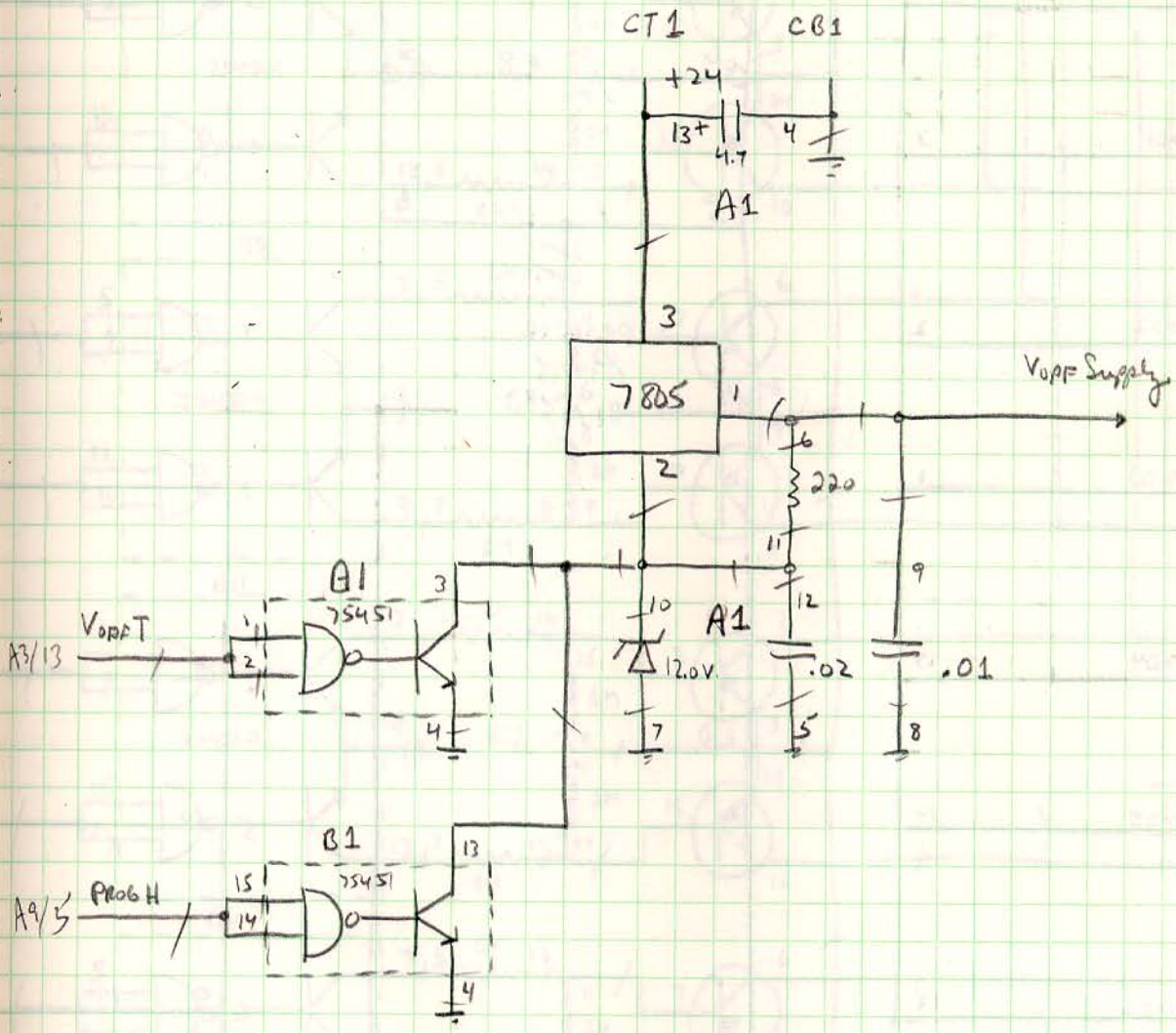


23 Jan 84

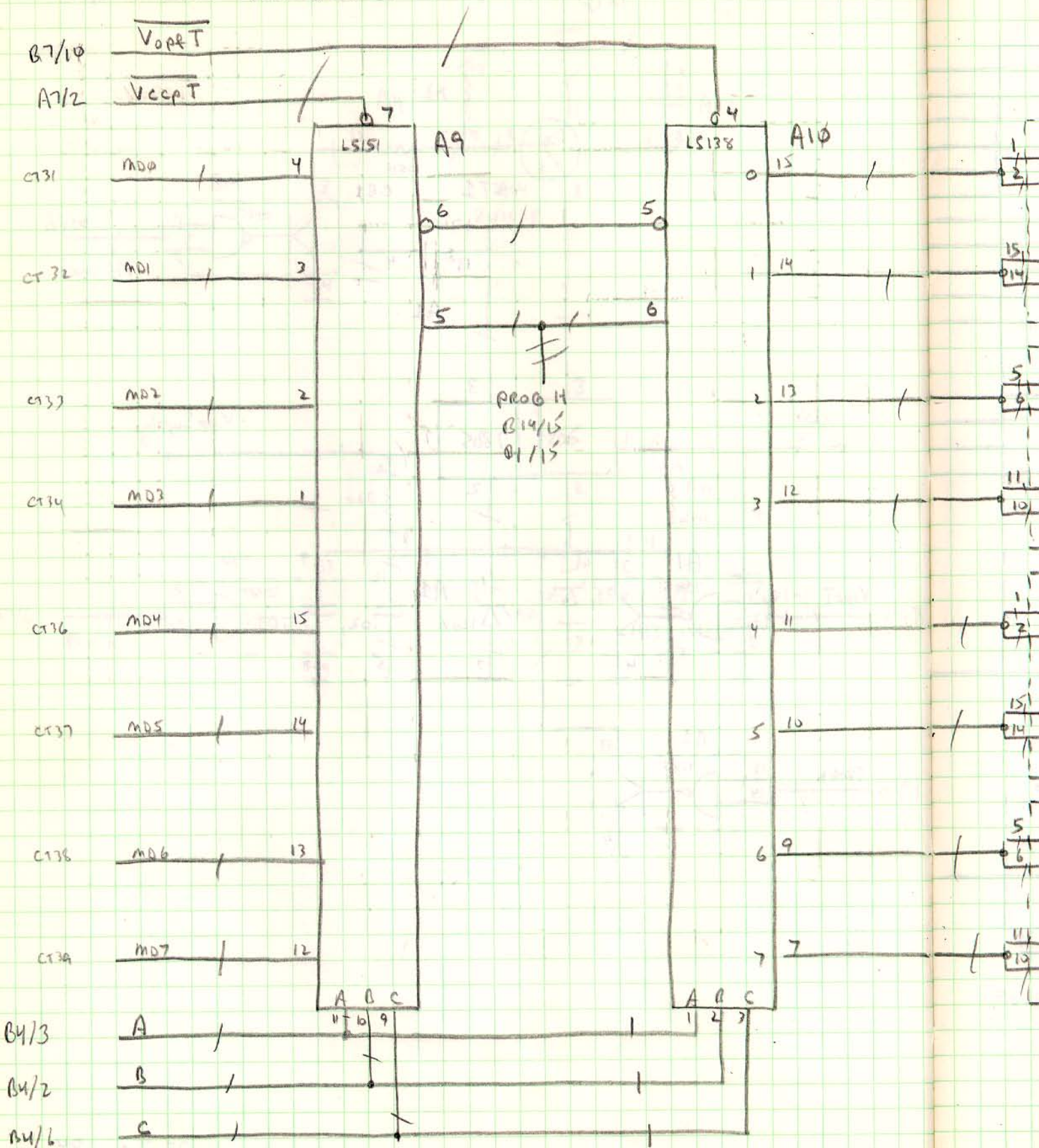
Vccp Power Control

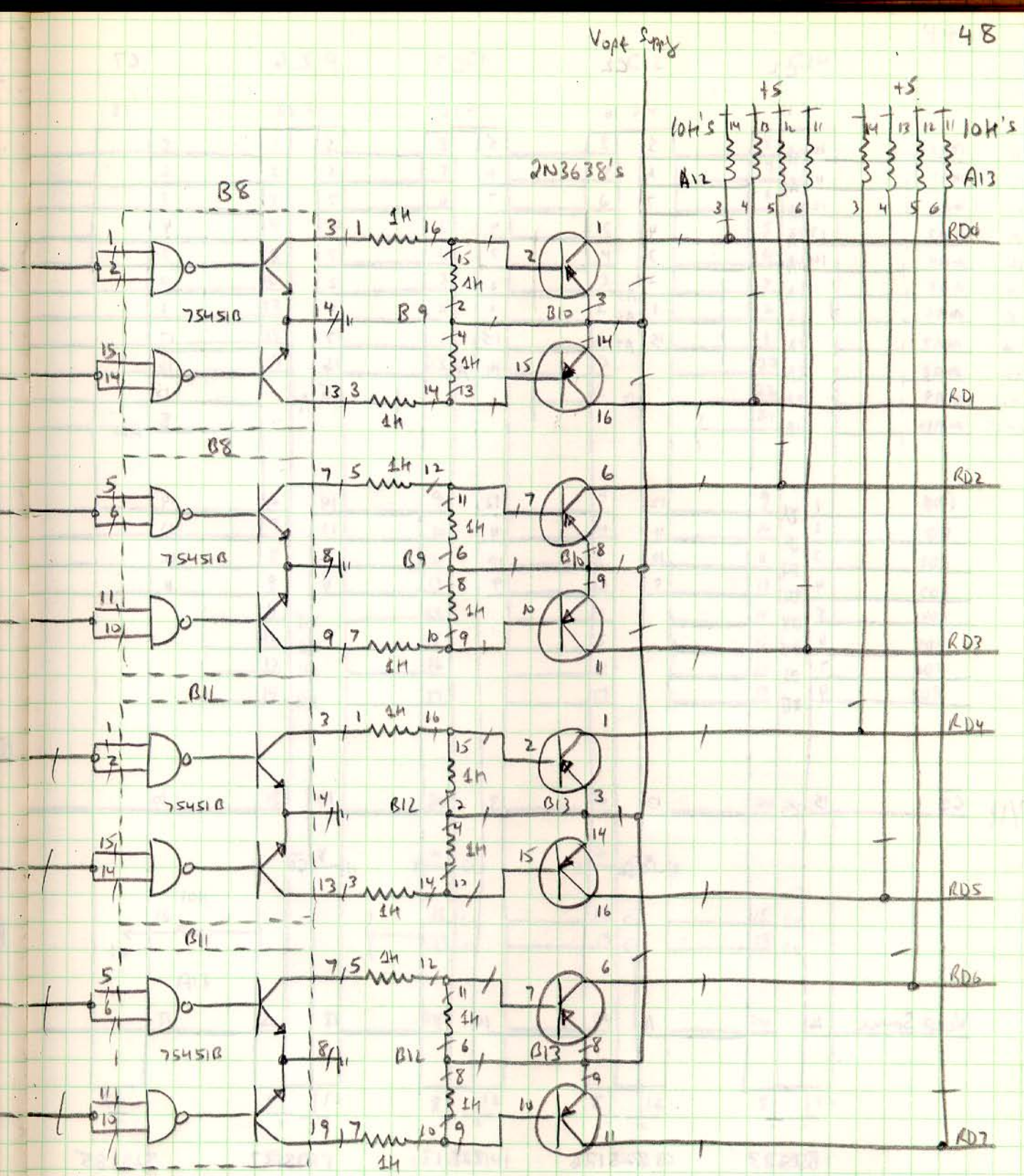


OUTPUT PIN Drain Supply Control

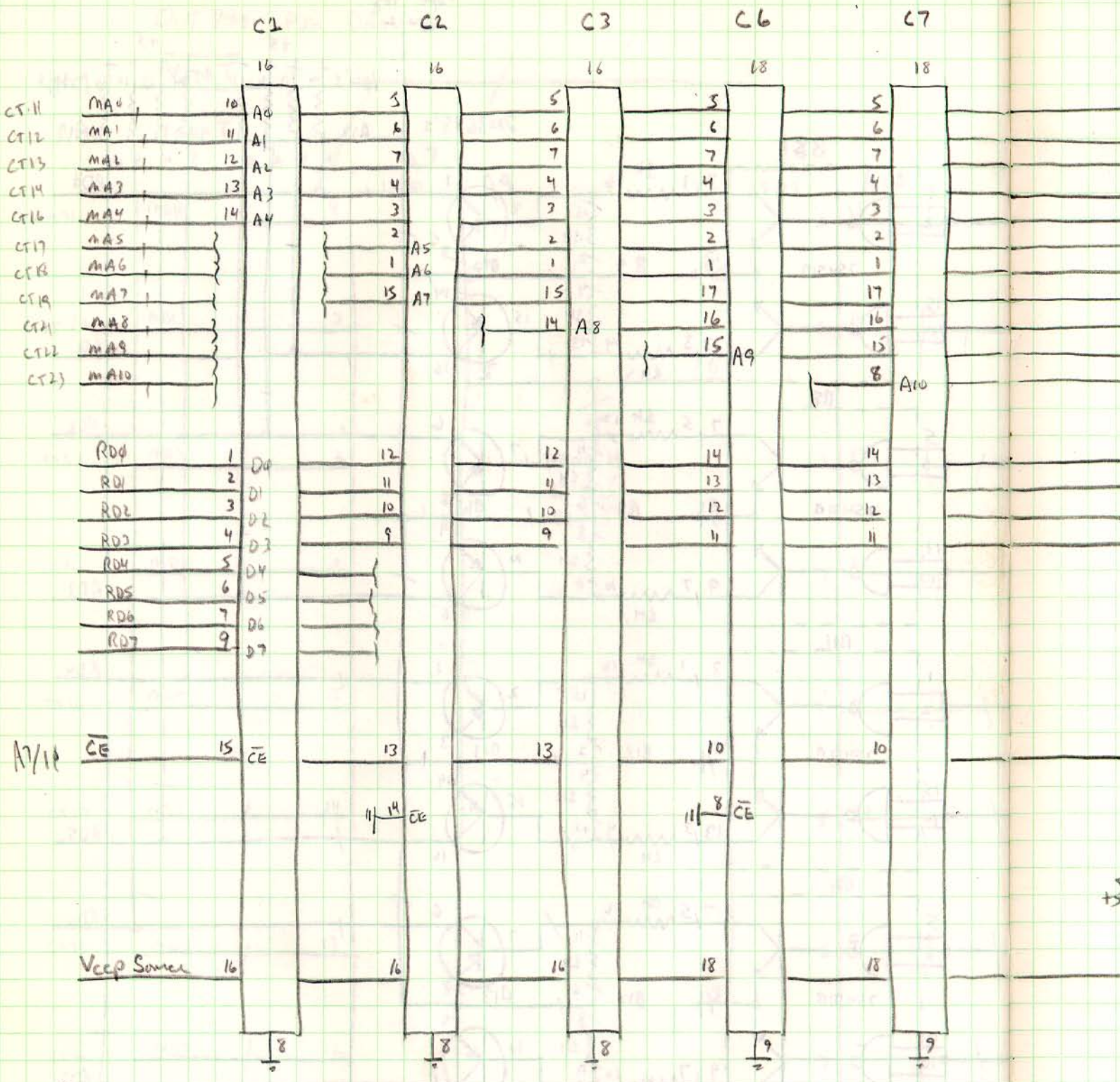


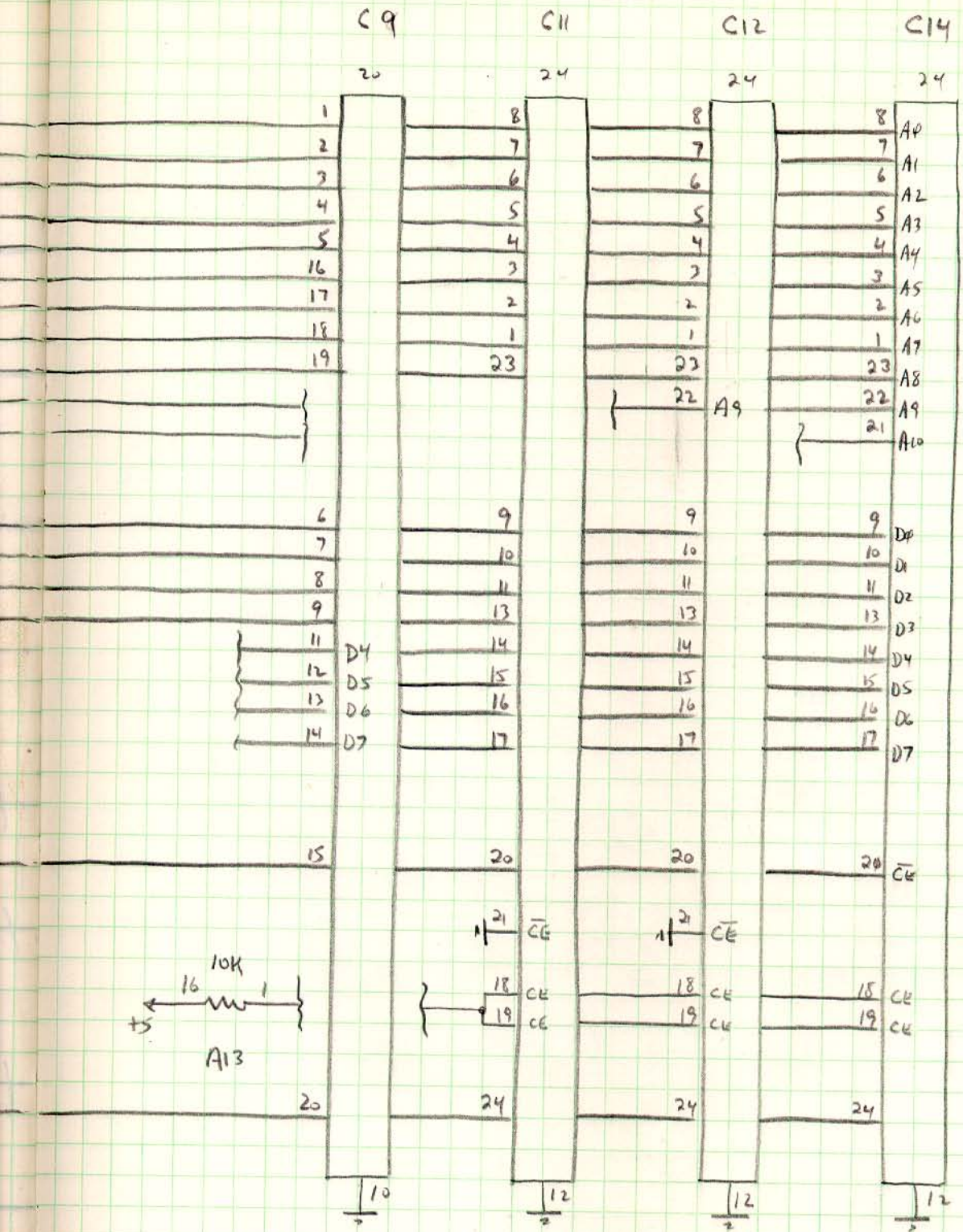
23 Jan 84
APB


OUTPUT PIN DRIVERS
B7/10
VOPRT
A7/2
VCCPT
LS151
A9
LS138
A10
CT31
MD0
CT32
MD1
CT33
MD2
CT34
MD3
CT36
MD4
CT37
MD5
CT38
MD6
CT39
MD7
PROG H
B14/15
A1/15
B4/3
A
B4/2
B
B4/6
C


Vopt Supply
+5
+5
10H's
10H's
2N3638's
A12
A13
B8
B9
B10
B11
B12
B13
7545IB
1H
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7

23 Jan 84
ARD


C1
C2
C3
C6
C7
16
16
16
18
18
CT-11
CT12
CT13
CT14
CT16
CT17
CT18
CT19
CT21
CT22
CT23
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA10
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
D0
D1
D2
D3
D4
D5
D6
D7
A7/11
CE
Vcc & Sense
8
8
8
9
9
82S23
82S123
82S126
82S129
82S130
82S131
82S137
82S185


C9
C11
C12
C14
20
24
24
24
A9
A13
10K
+5
D4
D5
D6
D7
CE
10
12
12
12
82S147
82S141
82S180
82S181
82LS181
82S183
82S2708
82S191

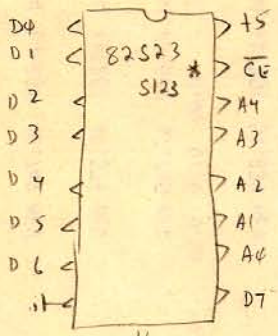
24 Jan 84
ARB

IC location INDEX

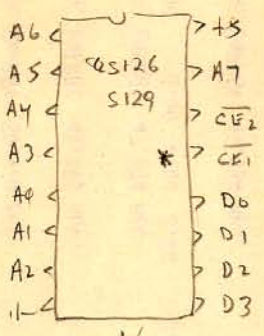
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14

B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
B13
B14

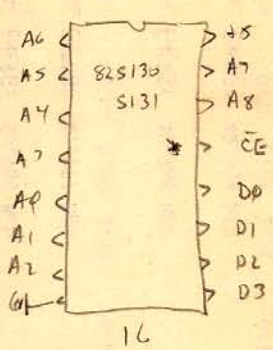
32x8



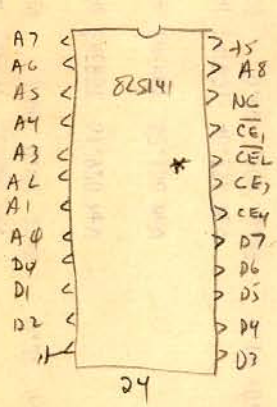
256x4



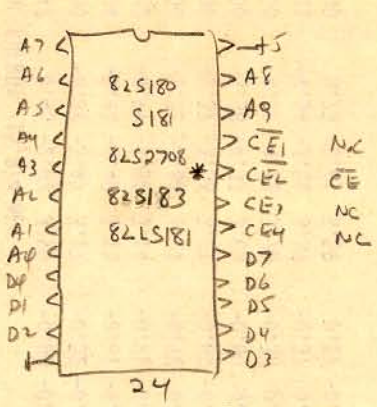
512x4



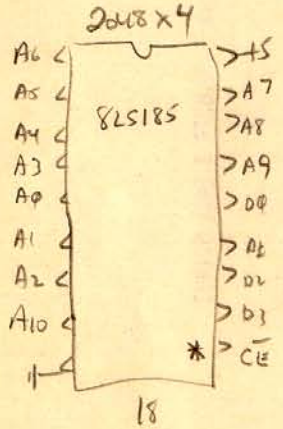
512x8



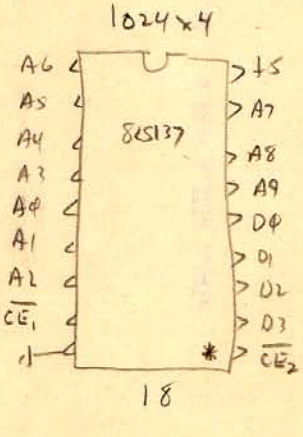
1024x8



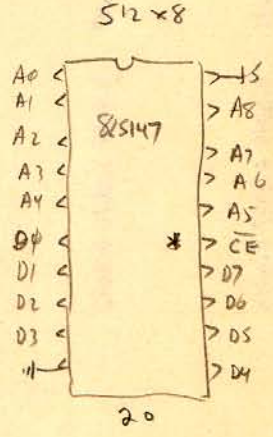
2048x4



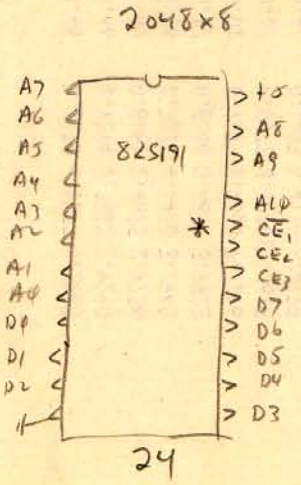
1024x4



512x8



2048x8



74S188/288
TBP18SA030/SO30

74S387/287 *
TBP14SA10/S10

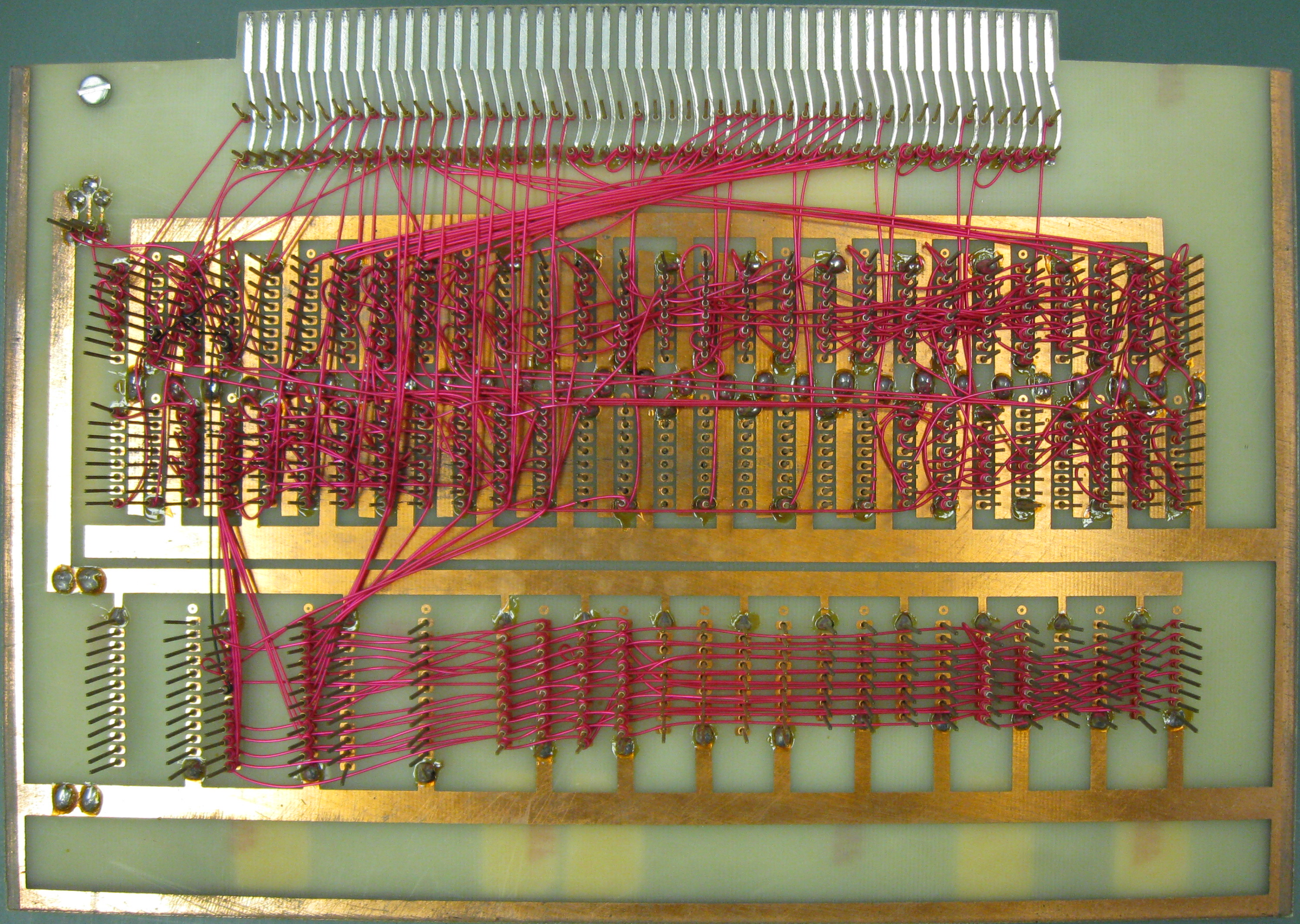
74S470/471
TBP18SA22/S22

74S472/473
TBP18S42/SA42

74S474/475
TBP18S46/SA46

Texas Instruments
Generic Prom Programmer Board

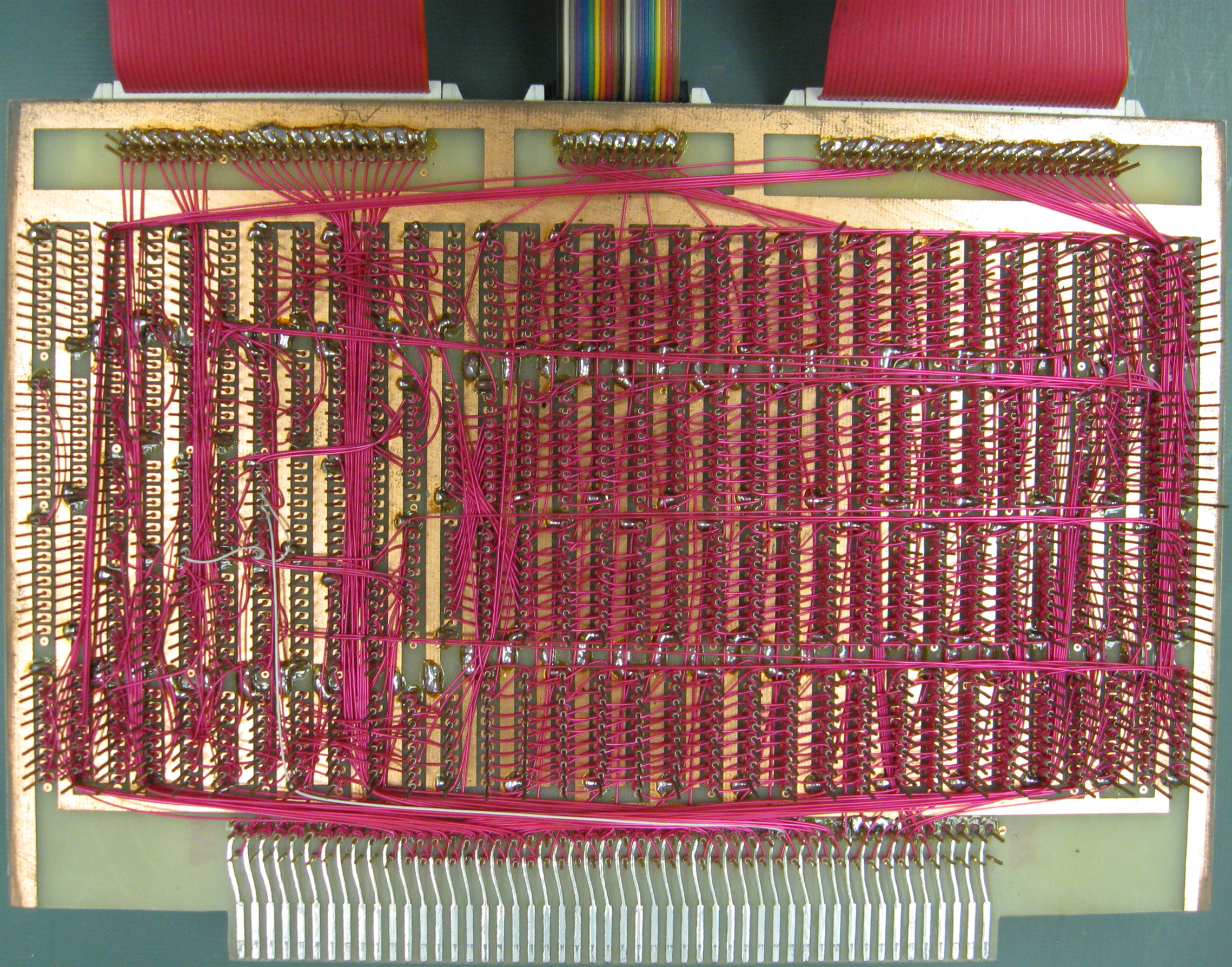
* - Switch #8
OPEN - 18 Series
Closed - 14 Series

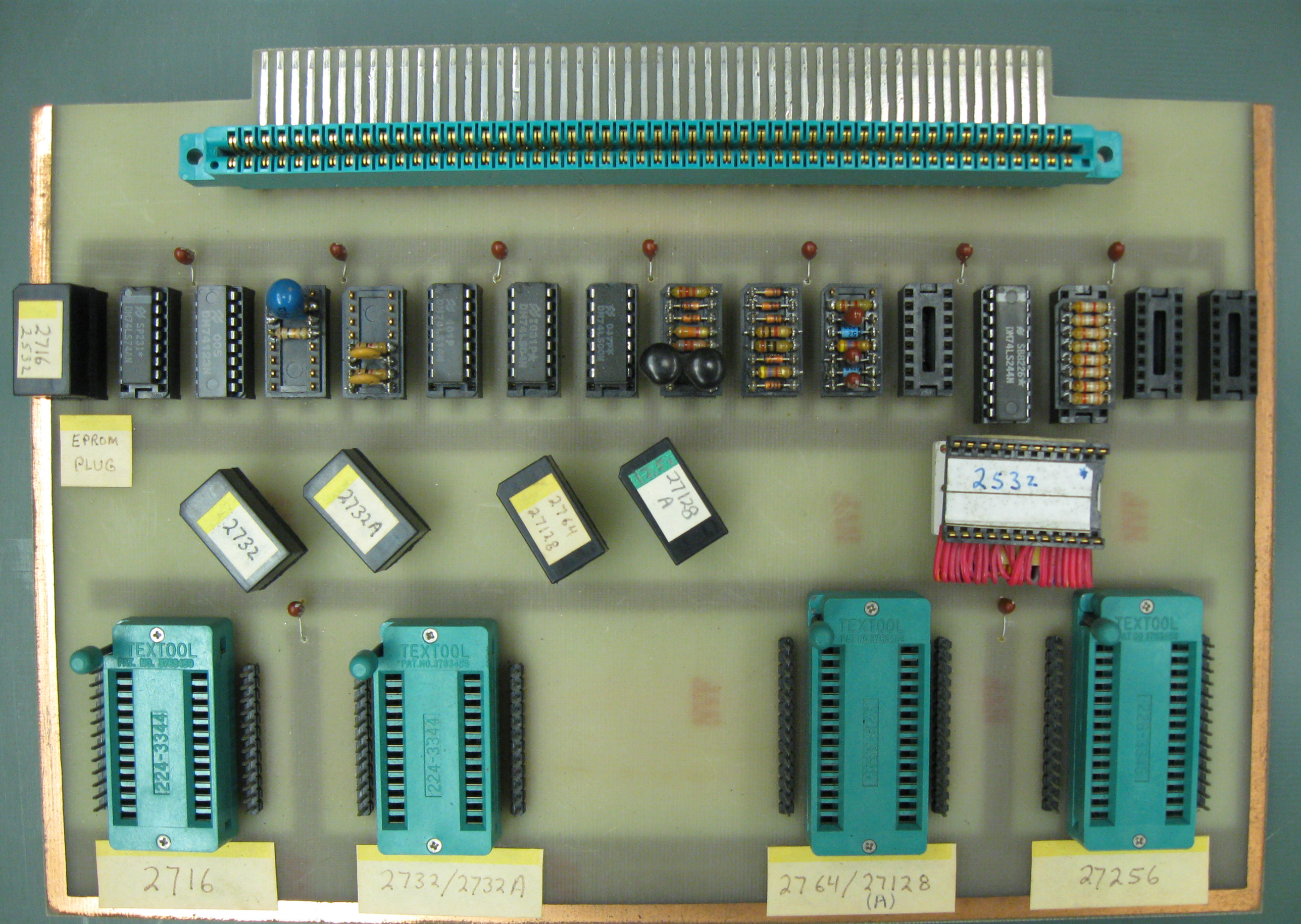


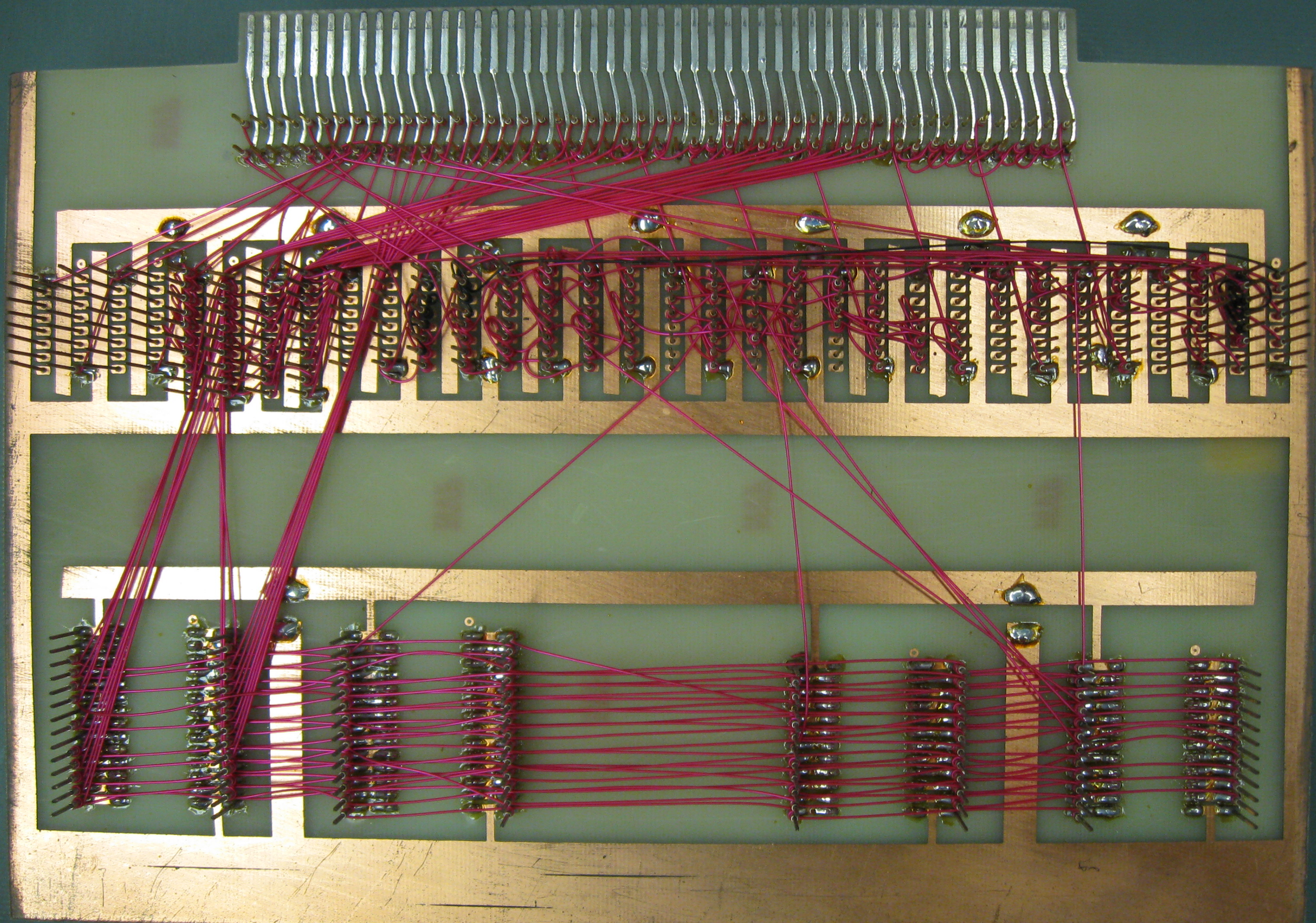
ADDRESS

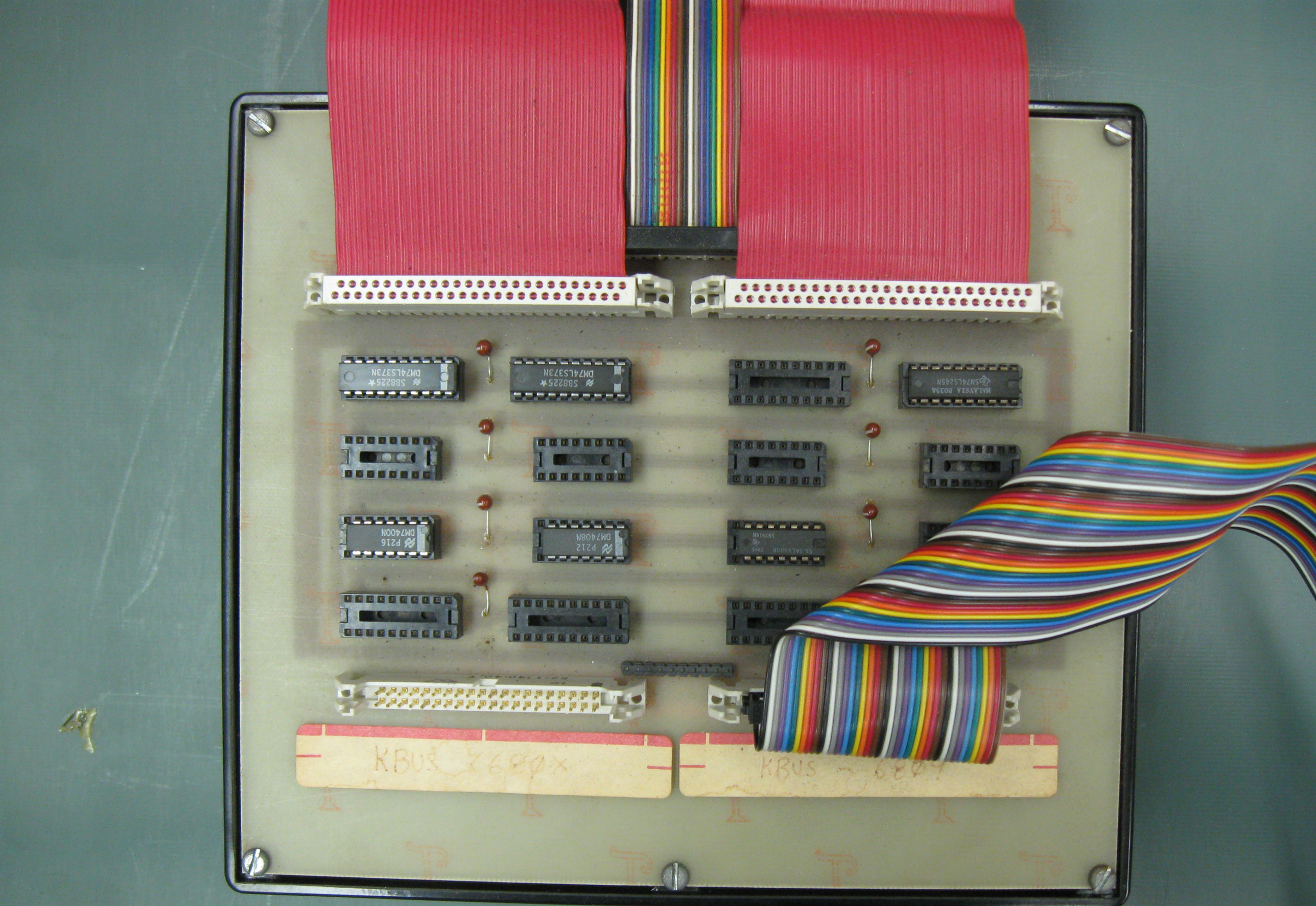
POWER

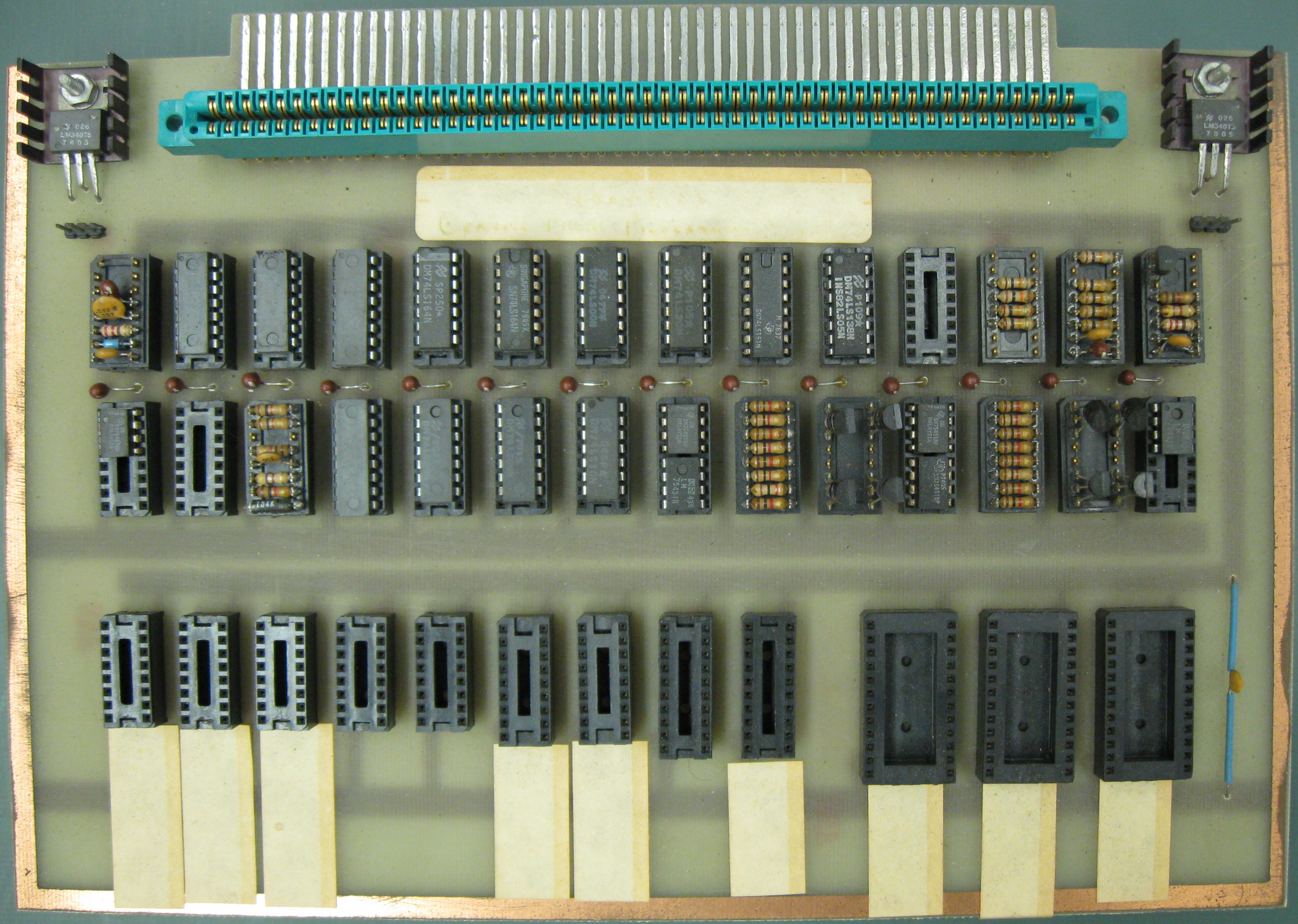
DATA




2716
2532
SP231*
DM74LS74AN
005
DM74123N
4011
DM74LS00N
8031*
DM74LS20N
DM74LS00N
SB8226*
DM74LS244N
EPROM
PLUG
2732
2732A
2764
27128
27128
A
2532
TEXTOOL
224-3344
TEXTOOL
224-3344
TEXTOOL
TEXTOOL
2716
2732/2732A
2764/27128
(A)
27256




KBUS 6800
KBUS 6809


LM340T5
7805
SP250A
DM74LS164N
SINGAPORE 7915X
SN74LS164N
DM74LS00N
SN74LS151N
DM74LS138N
INS82LS05N
SN74LS10N
SN74LS10P
LM
75451N