

#1  
PROM PROGRAMMER

5 DEC 77 - 10 Sept 1980



NATIONAL

53-110

Made in U.S.A.



PROM PROGRAMMER MANUAL

1

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16 Dec 1980  
Aro

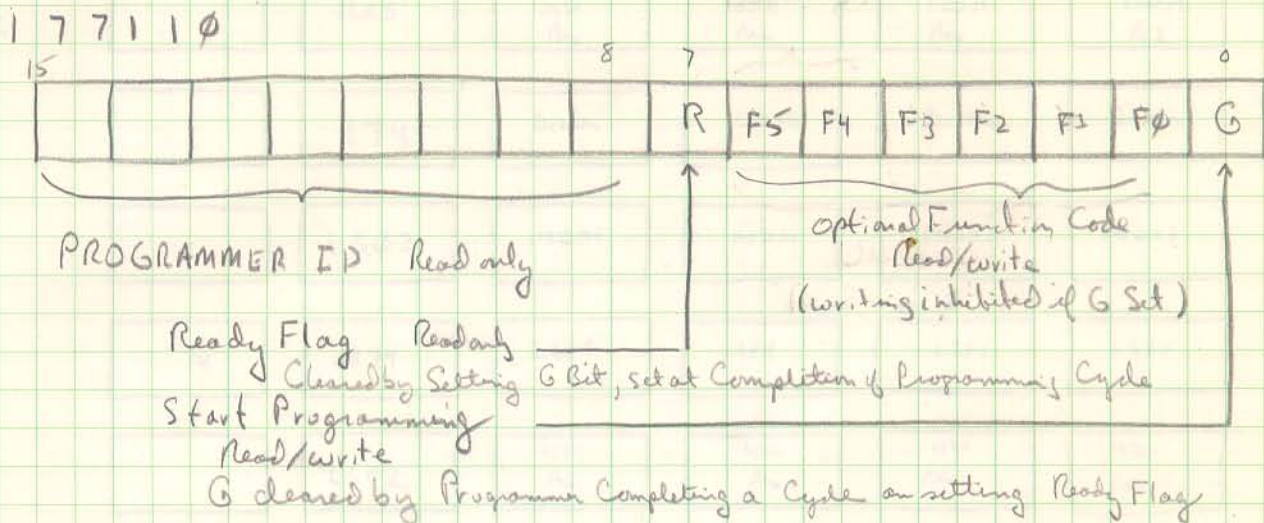


# PROM / EPROM PROGRAMMER INTERFACE

3

MODULE FOR PDP-11 CPU's

Control & STATUS WORD



177112 - Memory Address Register Read/write  
writing inhibited if G bit of Control word Set

177114 - Memory Data Register Read/write  
writing inhibited if G bit of Control word Set

177116 - Verify Data Register Read only

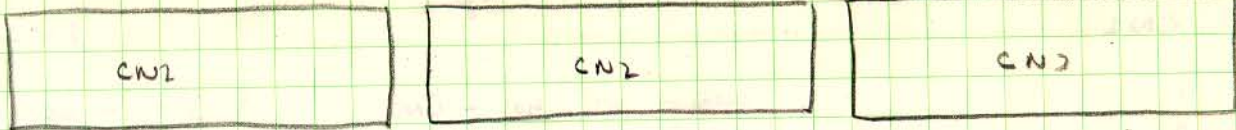


# Interface Board layout

⊗  
+5V

GND  
⊗

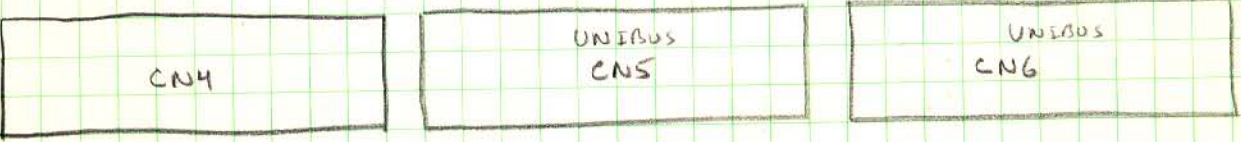




(X)  
+5V.

	A	B	C	D	E	F	
							1
		Res	100K Res	100K Res	100K Res	100K Res	2
		174	Diodes	Diodes	Diodes	Diodes	3
		LS42	14001	14001	14001	14001	4
	74	LS74	LS44	LS44	LS44	LS44	5
		LS42	470 Res	470 Res	470 Res	470 Res	6
	Res	LS139	175	175	175	175	7
	38	LS32	470 Res	470 Res	470 Res	470 Res	8
	LS34	LS44	175	175	175	175	9
	LS44	LS34	LS153	LS153	LS153	LS153	10
	8837	8837	LS153	LS153	LS153	LS153	11
	8837	8837	8838	8838	8838	8838	12

GND  
(X)



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APD



# Interface - Proprietary Connector Wiring

## CN1

1		40	- GND	1
2		39		2
3		38		3
4		37		4
5	- GND	36		5
6		35	- GND	6
7		34		7
8		33		8
9		32		9
10	- GND	31		10
11		30	- GND	11
12		29		12
13		28		13
14		27		14
15	- GND	26		15
16		25	- GND	16
17		24		17
18		23		18
19		22		19
20	- GND	21		20

## CN2

1	MA0 +	C8/1	40	- GND	
2	MA1 +	C8/2	39	GOH +	B6/14
3	MA2 +	C8/3	38	FEN +	A5/13
4	MA3 +	C8/4	37	F5 +	B2/6
5	- GND		36	P4 +	B2/5
6	MA4 +	D8/1	35	- GND	
7	MA5 +	D8/2	34	F3 +	B2/4
8	MA6 +	D8/3	33	F2 +	B2/3
9	MA7 +	D8/4	32	F1 +	B2/2
10	- GND		31	F0 +	B2/1
11	MA8 +	E8/1	30	- GND	
12	MA9 +	E8/2	29	ID0 +	E10/6
13	MA10 +	E8/3	28	ID1 +	E10/10
14	MA11 +	E8/4	27	ID2 +	E11/6
15	- GND		26	ID3 +	E11/10
16	MA12 +	F8/1	25	- GND	
17	MA13 +	F8/2	24	ID4 +	F14/6
18	MA14 +	F8/3	23	ID5 +	F10/10
19	MA15 +	F8/4	22	ID6 +	F11/6
20	- GND		21	ID7 +	F11/10



## CN3

1	MD0	+	C6/1	40	- GND		
2	MD1	+	C6/2	39	RD0	+	C2/14
3	MD2	+	C6/3	38	RD1	+	C2/13
4	MD3	+	C6/4	37	RD2	+	C2/12
5	- GND			36	RD3	+	C2/11
6	MD4	+	D6/1	35	- GND		
7	MD5	+	D6/2	34	RD4	+	D2/14
8	MD6	+	D6/3	33	RD5	+	D2/13
9	MD7	+	D6/4	32	RD6	+	D2/12
10	- GND			31	RD7	+	D2/11
11	MD8	+	E6/1	30	- GND		
12	MD9	+	E6/2	29	RD8	+	E2/14
13	MD10	+	E6/3	28	RD9	+	E2/13
14	MD11	+	E6/4	27	RD10	+	E2/12
15	- GND			26	RD11	+	E2/11
16	MD12	+	F6/1	25	- GND		
17	MD13	+	F6/2	24	RD12	+	F2/14
18	MD14	+	F6/3	23	RD13	+	F2/13
19	MD15	+	F6/4	22	RD14	+	F2/12
20	- GND			21	RD15	+	F2/11

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ABB



# 100 pin Programm Connections

- 1 +25A -
- 2 +25A -
- 3 +25B -
- 4 +25B -
- 5 +12V -
- 6 +12V -
- 7 -GND -
- 8 -GND -
- 9 -GND -
- 10 -GND -
- 11 MA0 -
- 12 MA1 -
- 13 MA2 -
- 14 MA3 -
- 15 -GND
- 16 MA4 -
- 17 MA5 -
- 18 MA6 -
- 19 MA7 -
- 20 -GND
- 21 MA8 -
- 22 MA9 -
- 23 MA10 -
- 24 MA11 -
- 25 -GND

- 26 MA12
- 27 MA13
- 28 MA14
- 29 MA15
- 30 -GND
- 31 MD0 -
- 32 MD2 -
- 33 MD2 -
- 34 MD3 -
- 35 -GND
- 36 MD4 -
- 37 MD5 -
- 38 MD6 -
- 39 MD7 -
- 40 -GND
- 41 MD8 -
- 42 MD9 -
- 43 MD10 -
- 44 MD11 -
- 45 -GND
- 46 MD12 -
- 47 MD13 -
- 48 MD14 -
- 49 MD15 -
- 50 -GND

- A
- B
- C
- D
- E
- F
- H
- J
- H
- L
- M
- N
- P
- R
- S
- T
- U
- V
- W
- X
- Y
- Z
- a
- b
- c



A	+25AR-	d	- GND
B	+25AK-	e	ID4-
C	+25AL-	f	ID5-
D	+25AR-	h	ID6-
E	-12V-	j	ID7-
F	-12V-	K	-GND
H	+5V-	l	RD4-
J	+5V-	m	RD1-
K	+5V-	n	RD2-
L	+5V-	p	RD3-
M	-GND	r	-GND
N	60H-	s	RD4-
P	FIN-	t	RD5-
R	F5-	u	RD6-
S	F4-	v	RD7-
T	-GND	w	-GND
U	F3-	x	RD8-
V	F2-	y	RD9-
W	F1-	z	RD10-
X	F0-	AA	RD11-
Y	-GND	BB	-GND
Z	ID6-	CC	RD12-
a	ID5-	DD	RD13-
b	ID2-	EE	RD14-
c	ID3-	FF	-RD15-

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AGD



# Interface - Unibus Connectors

CN4

1		40	-GND
2		39	
3		38	
4		37	
5	-GND	36	
6		35	-GND
7		34	
8		33	
9		32	
10	-GND	31	
11		30	-GND
12		29	
13		28	
14		27	
15	-GND	26	
16		25	-GND
17		24	
18		23	
19		22	
20	-GND	21	

CN

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20

CN5

1	D00L	+	C12/15	40	-GND
2	D01L	+	C12/12	39	INTEL + B11/1
3	D02L	+	C12/1	38	INTRL -
4	D03L	+	C12/4	37	+5 volts Bus in -
5	-GND			36	+5 volts Bus out -
6	D04L	+	D12/15	35	-GND
7	D05L	+	D12/12	34	PAL -
8	D06L	+	D12/1	33	PAL -
9	D07L	+	D12/4	32	+5 volts Bus out -
10	-GND			31	BASYL -
11	D08L	+	E12/15	30	-GND
12	D09L	+	E12/12	29	SACKL -
13	D10L	+	E12/1	28	+5 volts Bus out -
14	D11L	+	E12/4	27	NPRL -
15	-GND			26	NPGH -
16	D12L	+	F12/15	25	-GND
17	D13L	+	F12/12	24	BR7L -
18	D14L	+	F12/1	23	BR6L -
19	D15L	+	F12/4	22	BR7H -
20	-GND			21	+5 volts Bus out -



## CNG

1	A00L	+	A11/5	40	-GND	
2	A01L	+	A11/3	39	B66H	-
3	A02L	+	A11/1	38	B65H	-
4	A03L	+	A11/11	37	+5 volts IN	-
5	-GND			36	BRS L	-
6	A04L	+	A11/13	35	-GND	
7	A05L	+	A11/15	34	BR4L	-
8	A06L	+	A12/5	33	B64H	-
9	A07L	+	A12/3	32	ACLO L	-
10	-GND			31	DCLO L	-
11	A08L	+	A12/11	30	-GND	
12	A09L	+	A12/11	29	A16L	+ B12/13
13	A10L	+	A12/13	28	A17L	+ B12/15
14	A11L	+	A12/15	27	C1L	+ B11/11
15	-GND			26	C0L	+ B11/13
16	A12L	+	B12/5	25	-GND	
17	A13L	+	B12/3	24	BSSYNL	+ A8/6
18	A14L	+	B12/1	23	+5 volts out	-
19	A15L	T	B12/11	22	+5 volts out	-
20	-GND			21	DASYNL	+ B11/15

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ARD



# UNIBUS Connector

## A Block Side 1

A1	INITL
B1	INTRL
C1	D04 L
D1	D02 L
E1	D04 L
F1	D06 L
H1	D08 L
J1	D10 L
K1	D12 L
L1	D14 L
M1	PA L
N1	GND
P1	GND
R1	GND
S1	GND
T1	GND
U1	NPGH
V1	B67 H

## A Block Side 2

A2	+5
B2	GND
C2	GND
D2	D05 L
E2	D03 L
F2	D05 L
H2	D07 L
J2	D09 L
K2	D11 L
L2	D13 L
M2	D15 L
N2	P0 L
P2	BBSYL
R2	SACK L
S2	NAR L
T2	BR7 L
U2	BR6 L
V2	GND

## B Block Side 1

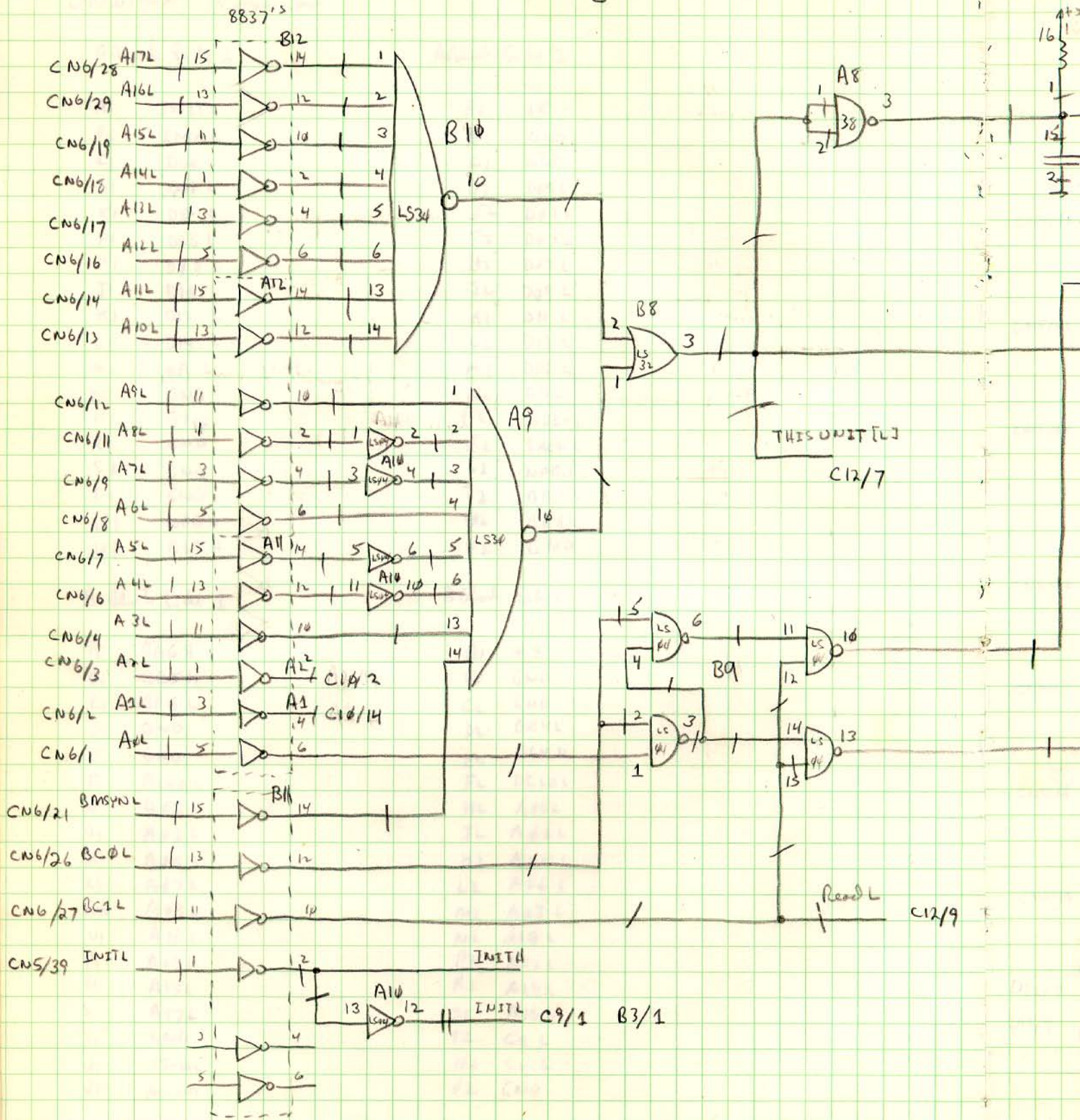
A1	B66 H
B1	B65 H
C1	BR5 L
D1	GND
E1	GND
F1	ACLO L
H1	A01 L
J1	A03 L
K1	A05 L
L1	A07 L
M1	A09 L
N1	A11 L
P1	A13 L
R1	A15 L
S1	A17 L
T1	GND
U1	SSYNL
V1	MSYNL

## B Block Side 2

A2	+5
B2	GND
C2	GND
D2	BR4 L
E2	B64 H
F2	DCLO L
H2	A04 L
J2	A02 L
K2	A04 L
L2	A06 L
M2	A08 L
N2	A10 L
P2	A12 L
R2	A14 L
S2	A16 L
T2	C1 L
U2	C0 L
V2	GND

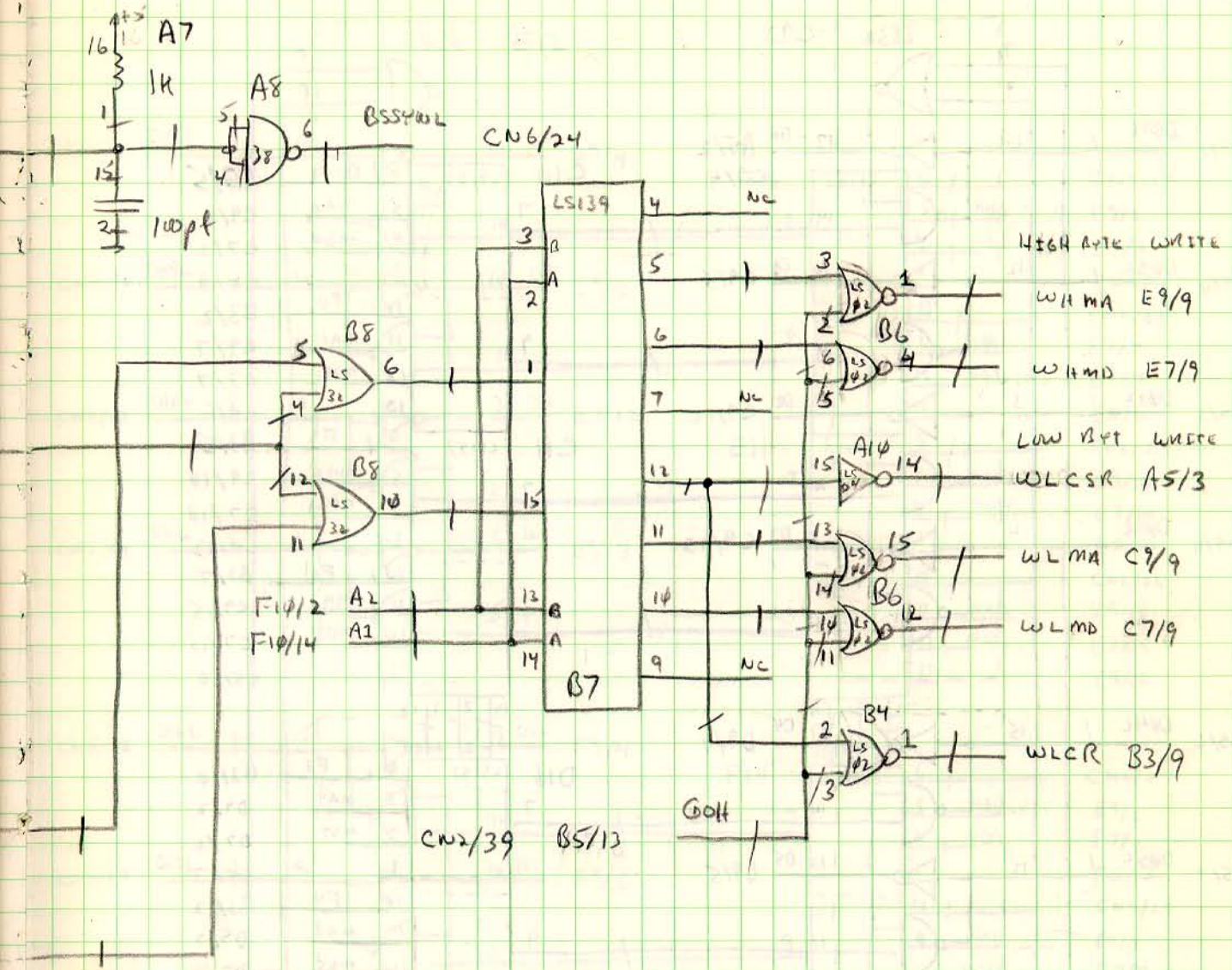


# Inter Base Address Receiver & Decoding



8837's Enabled by grounding pins 7 & 9

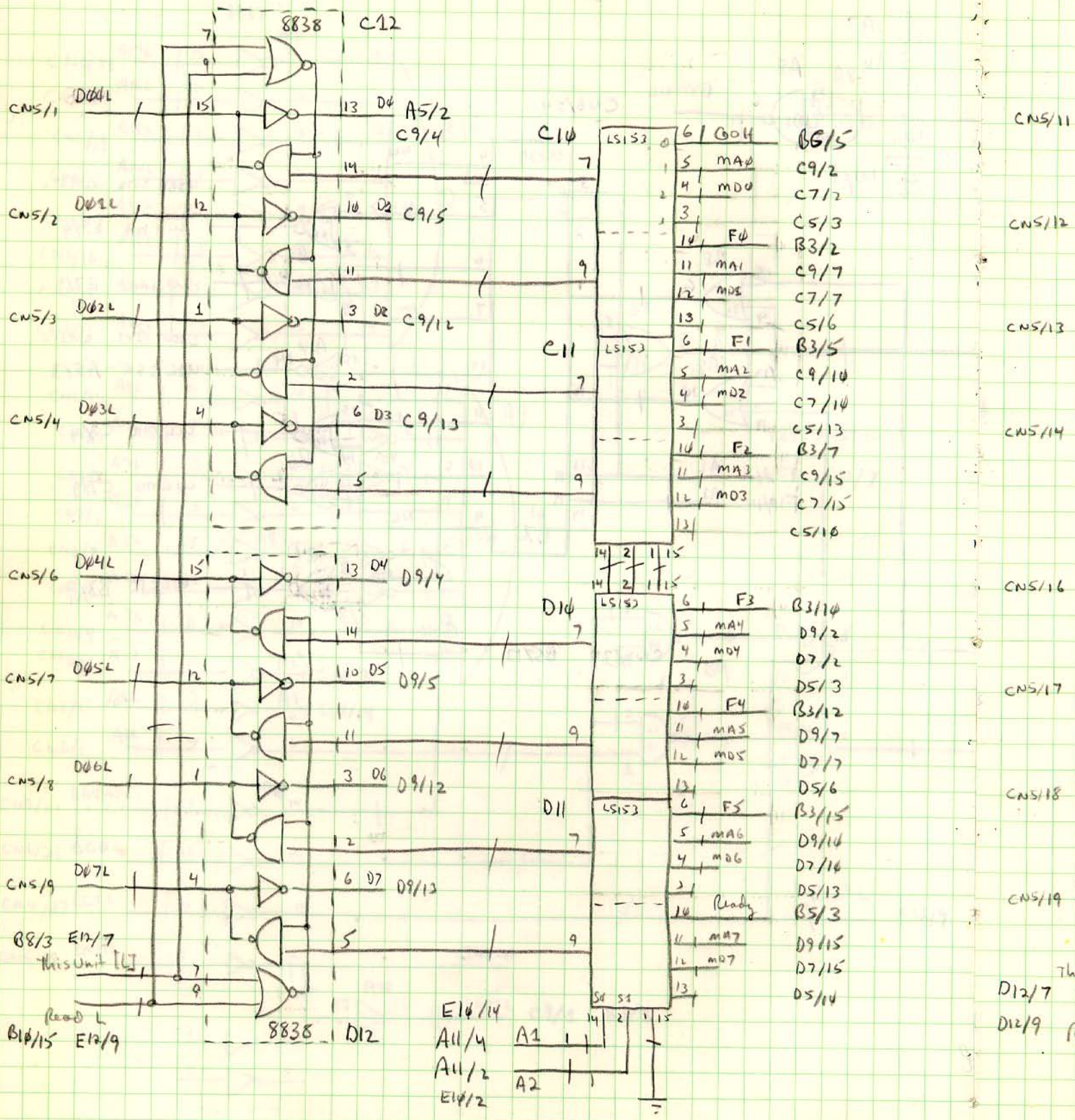




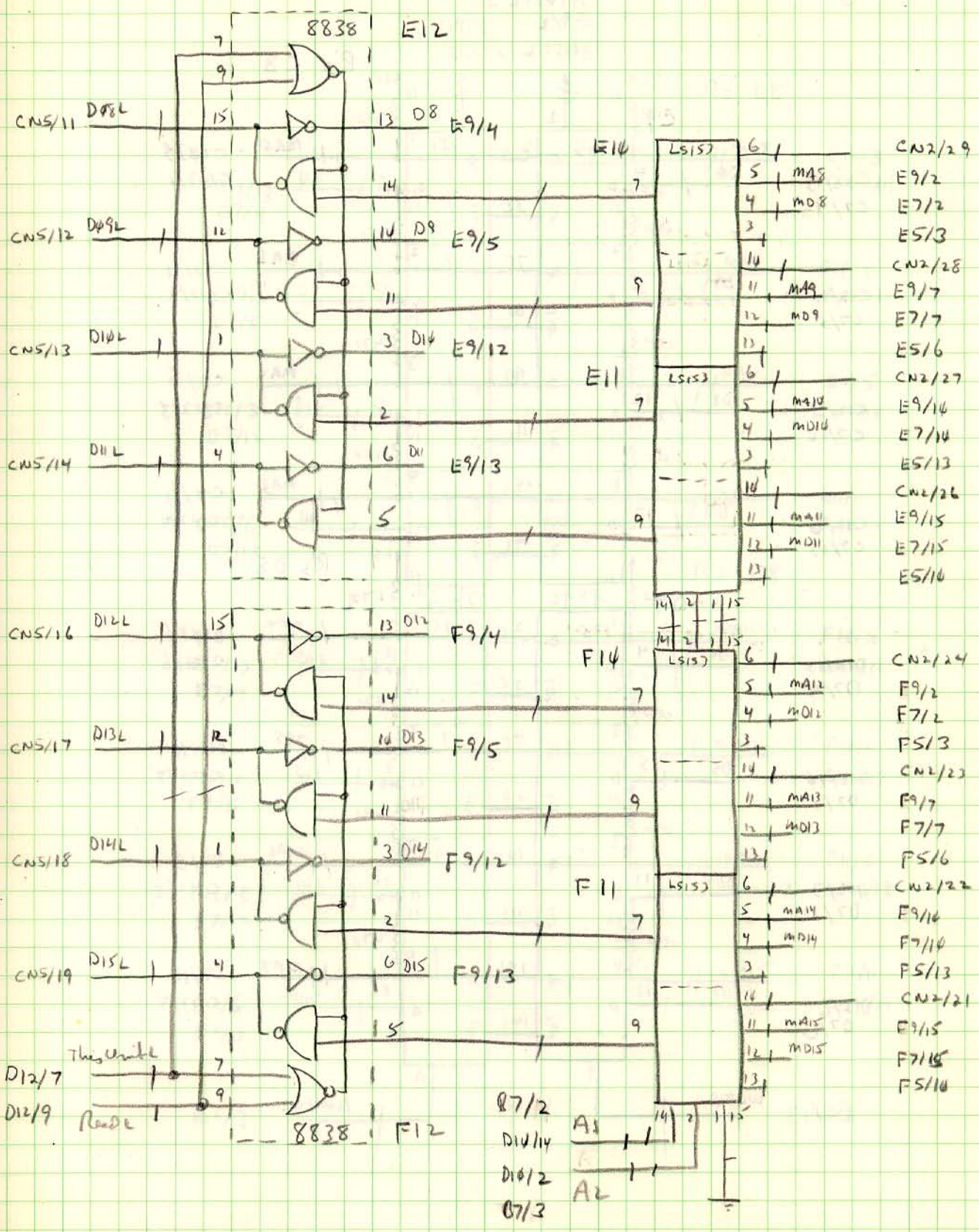
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ADD



# Data Bus Interface & Multiplexer







S. P. 77  
A. P.

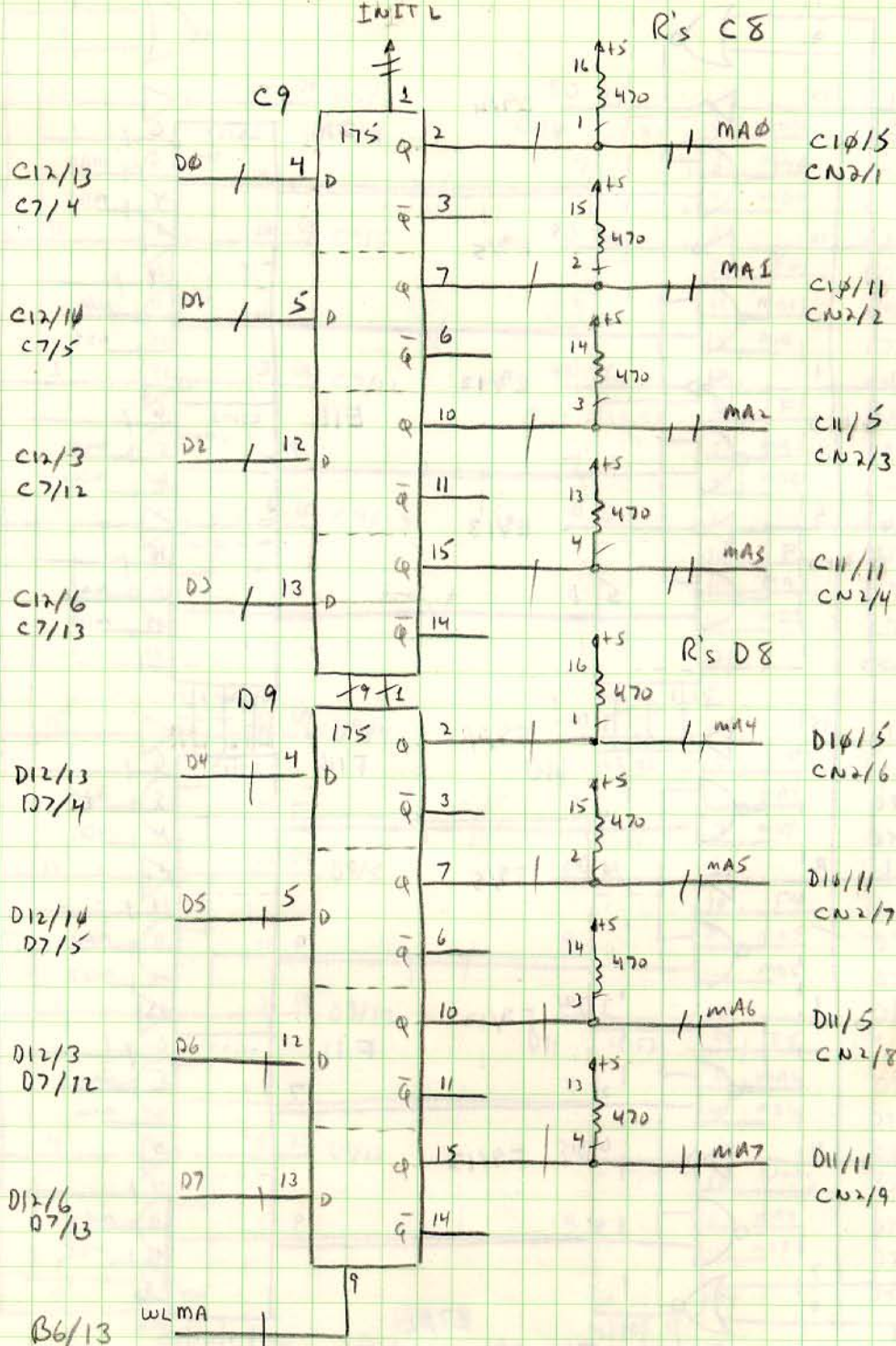


# Memory Address Register

A14/12

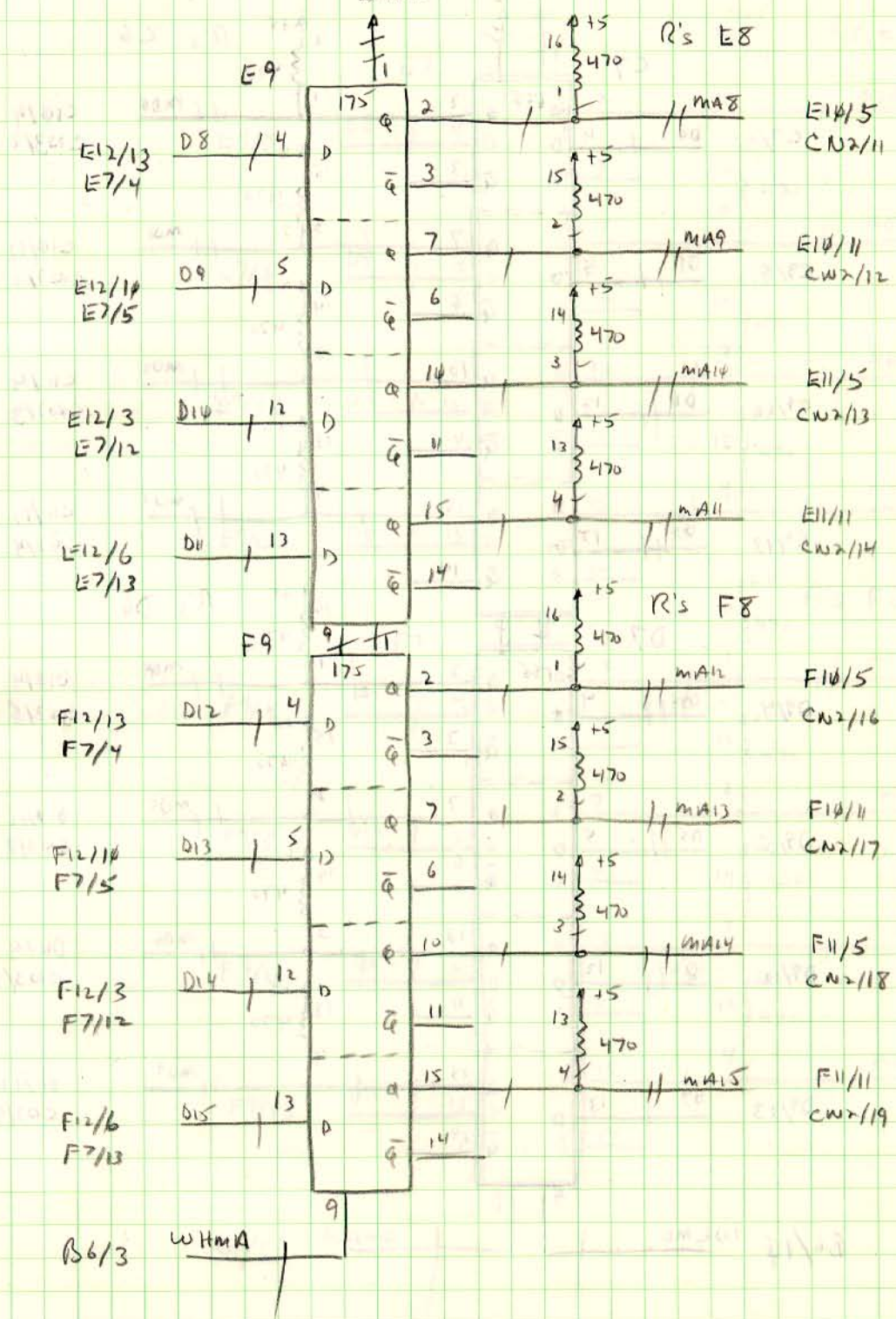
E9/2

INIT L





F7/I  
D9/I  
INSTR

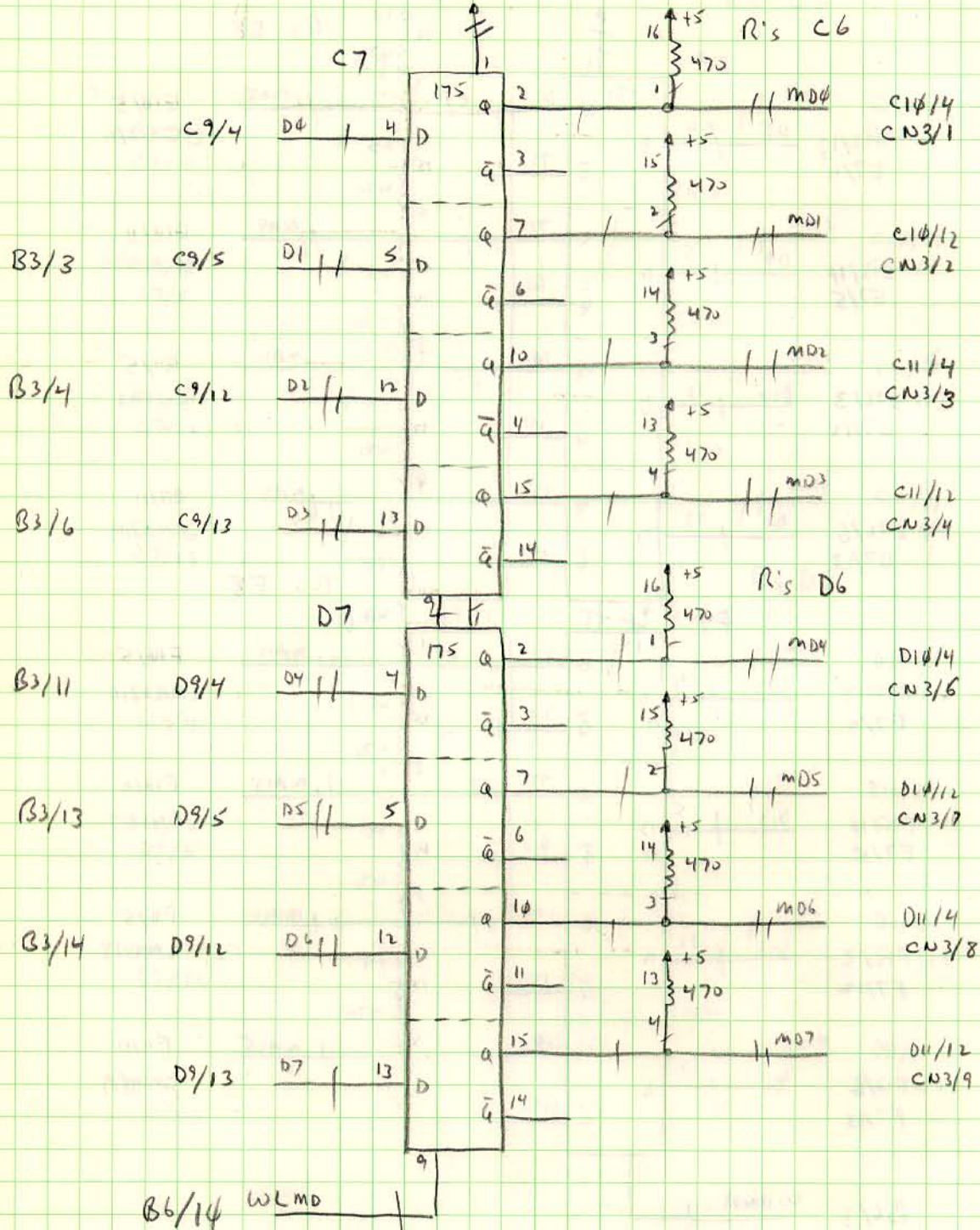


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ARD



# Memory Data Register

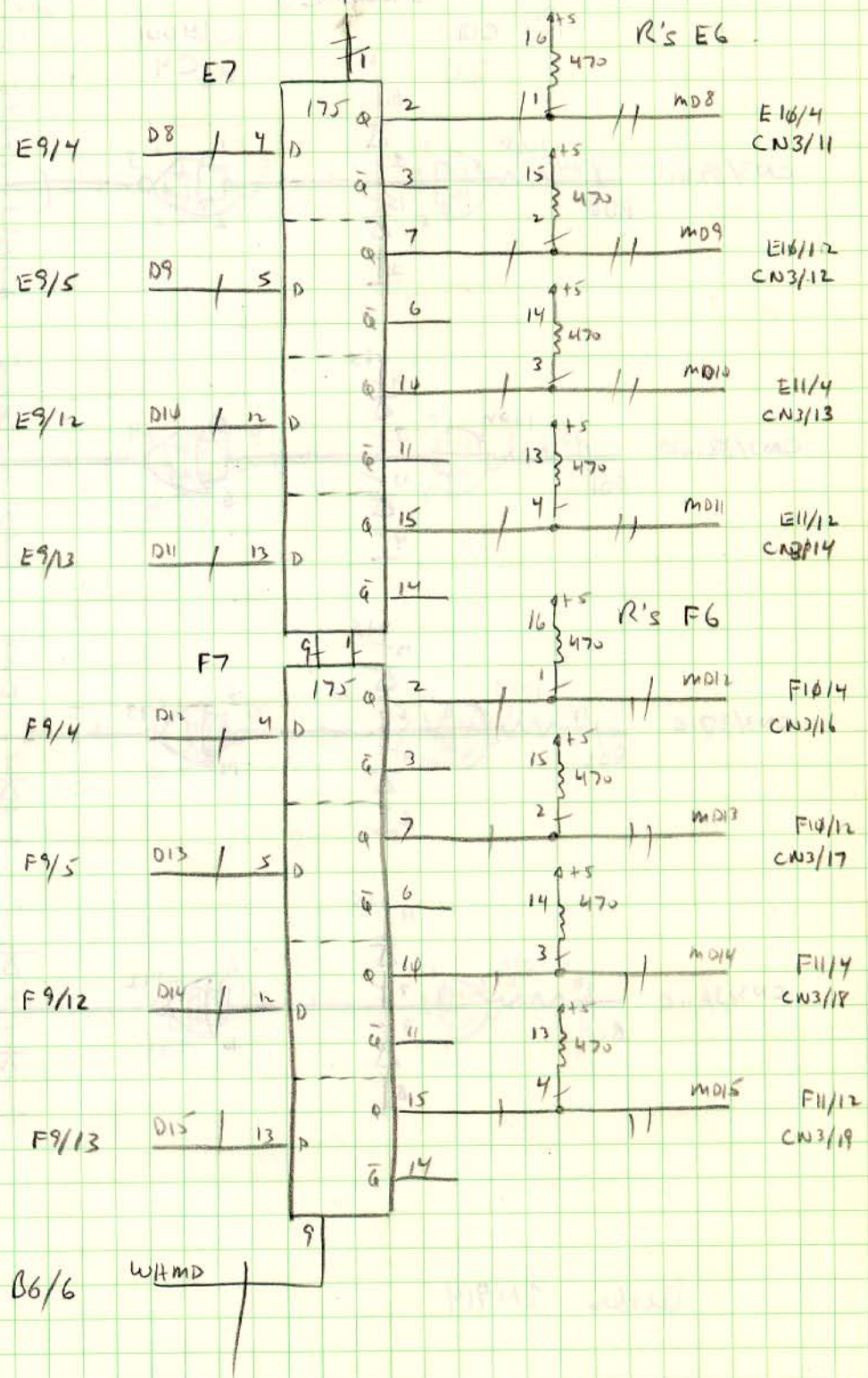
B5/4  
E7/1  
INITL





F9/1  
D7/1

INITL



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AAB

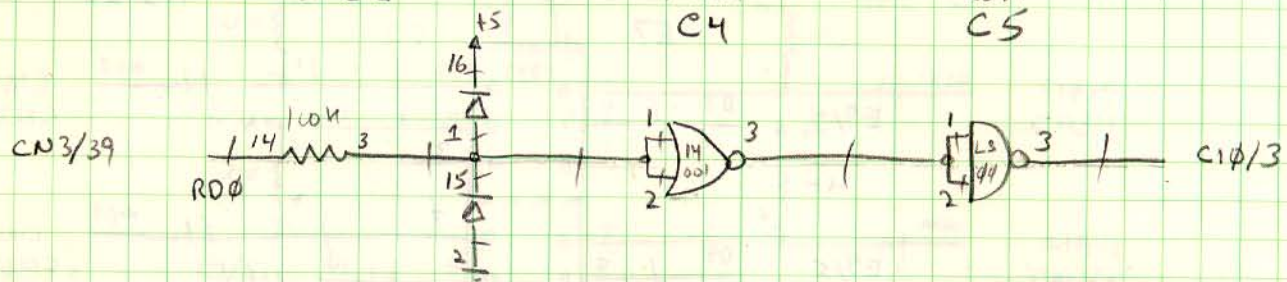


# Verify Read Logic

Diodes C3  
R's C2

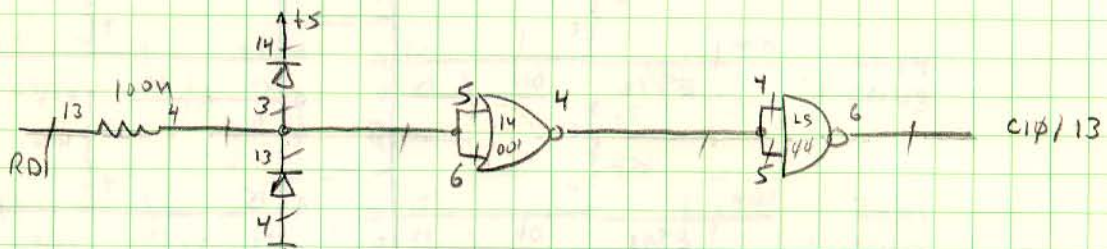
14001  
C4

LS44  
C5



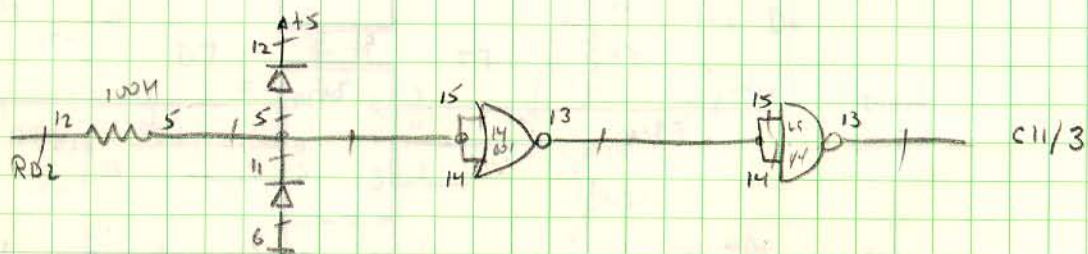
CN3/39

CN3/38



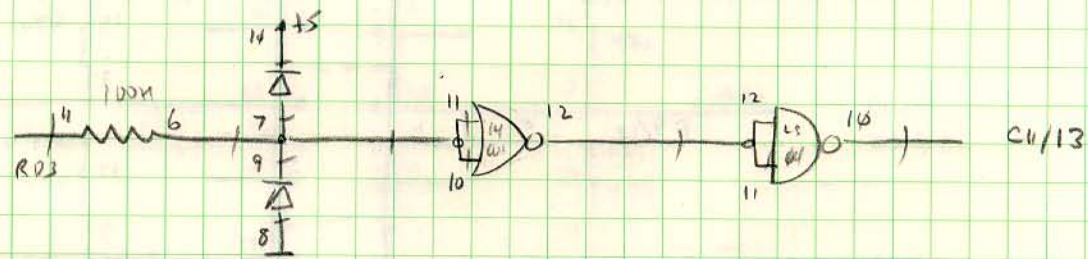
CN3/38

CN3/37



CN3/37

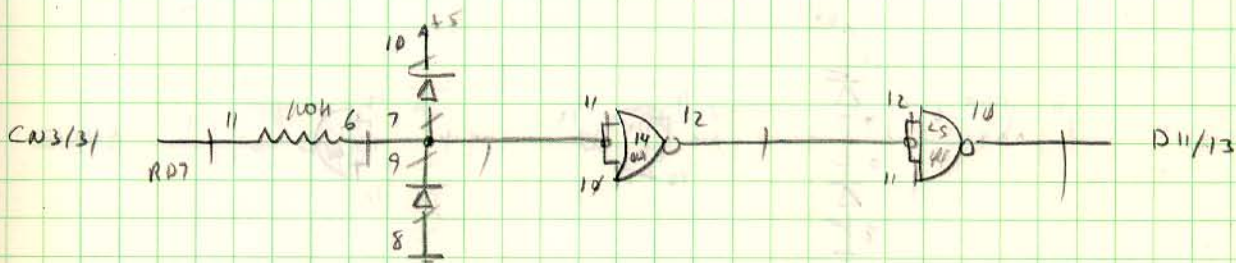
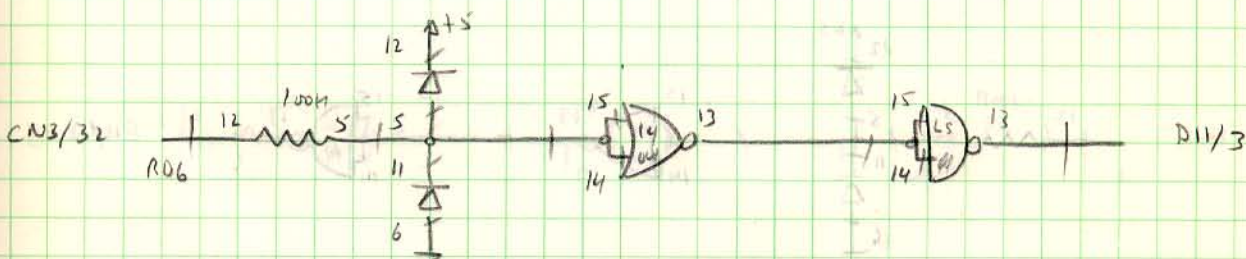
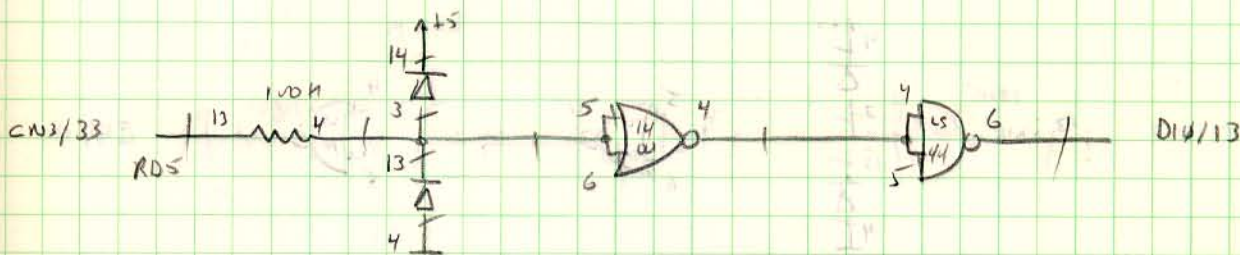
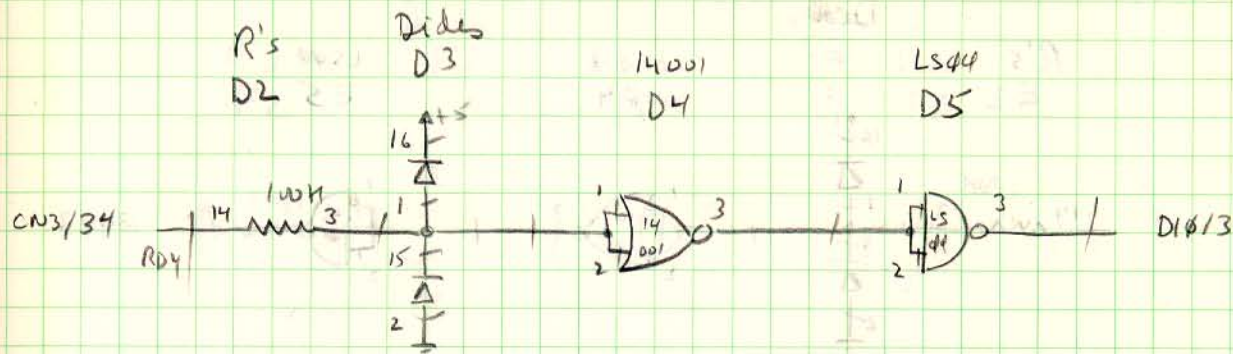
CN3/36



CN3/36

Diodes 1N914

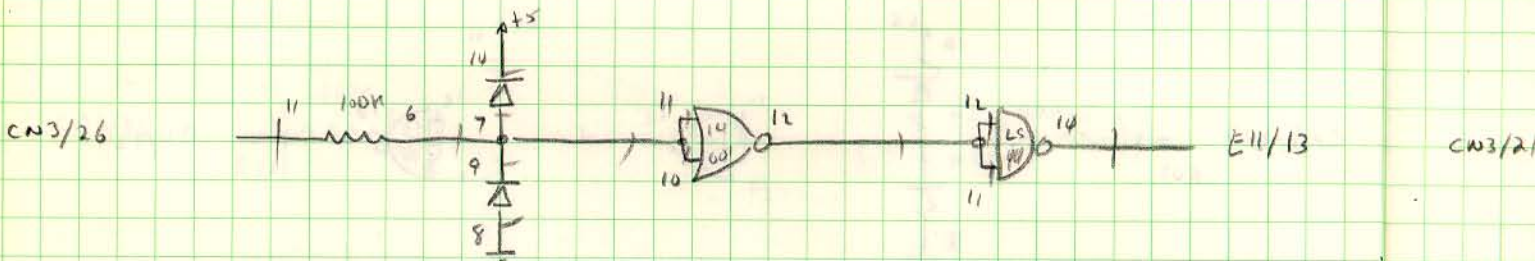
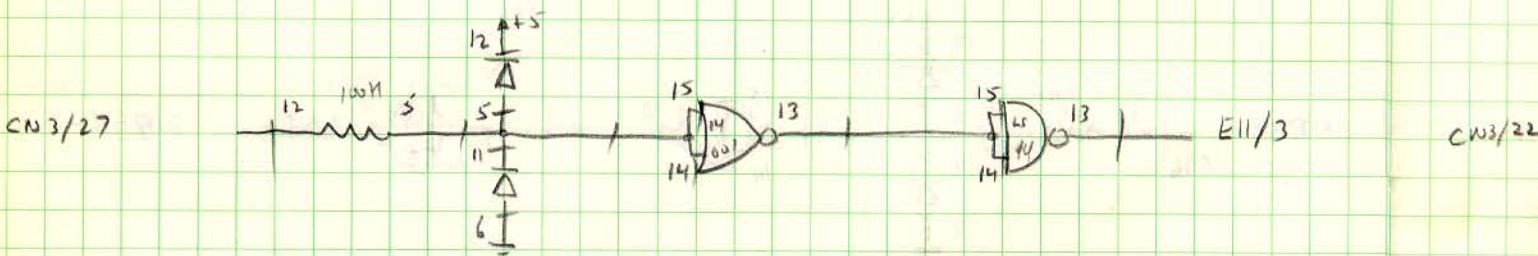
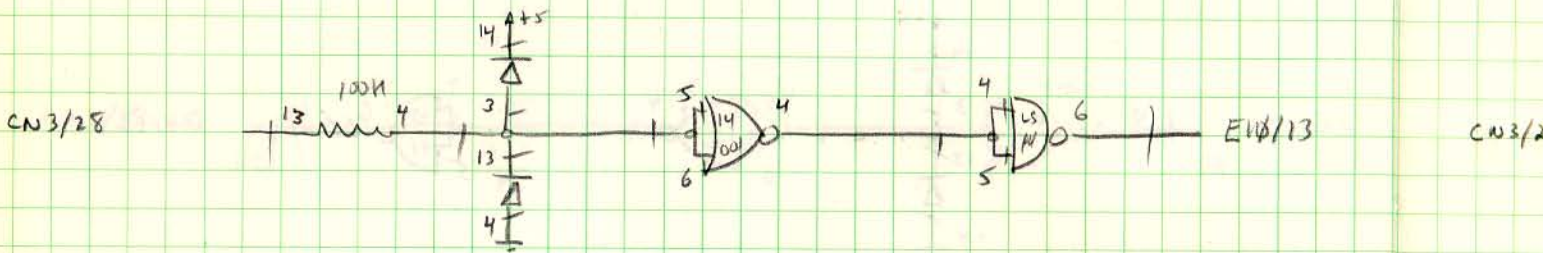
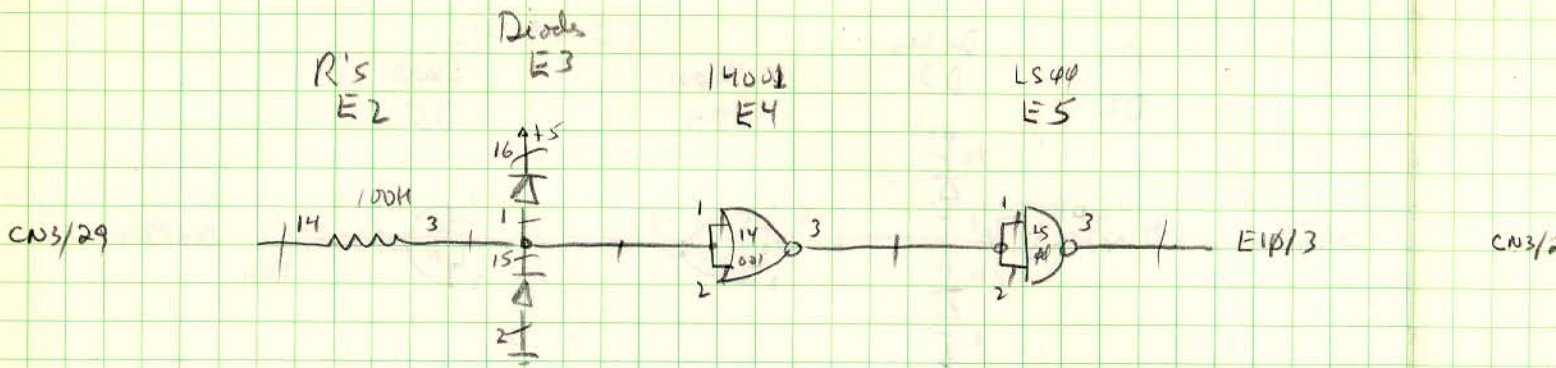




5 Apr 77  
AD

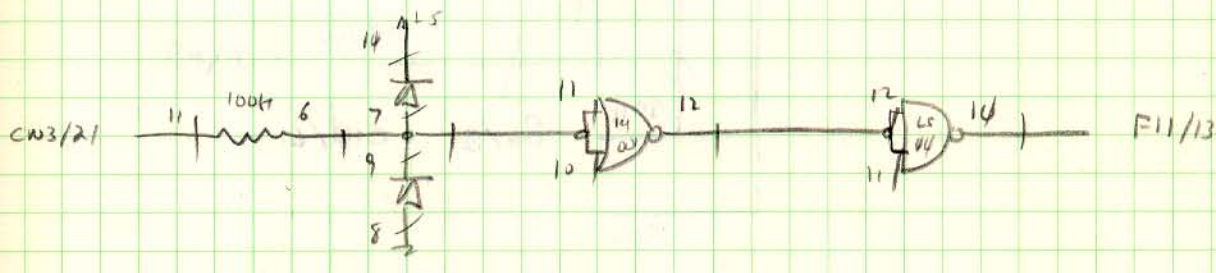
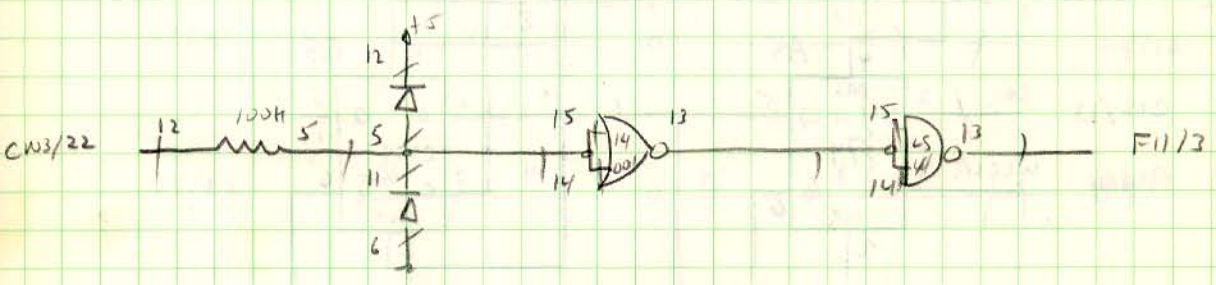
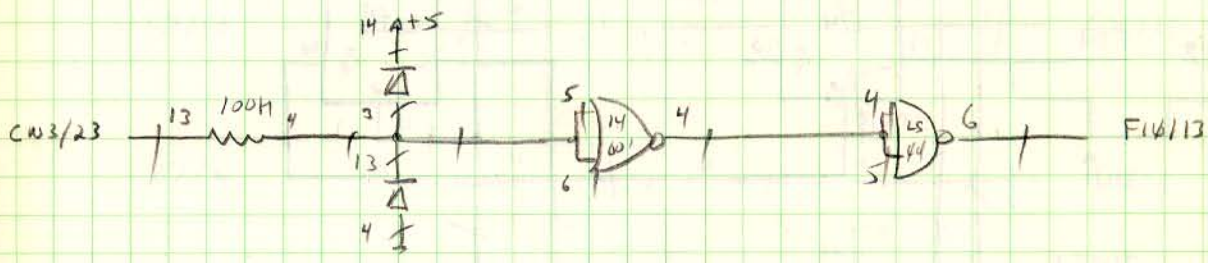
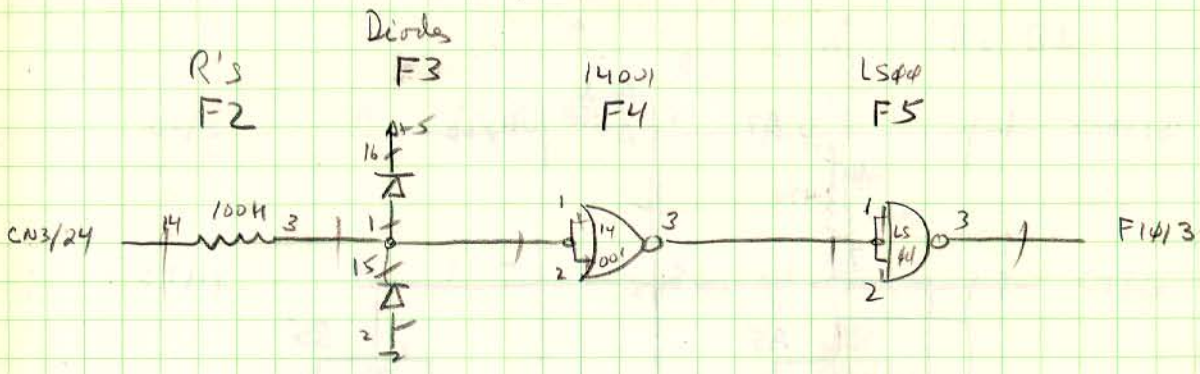


# Ven's Read Logic



Diode 1N914

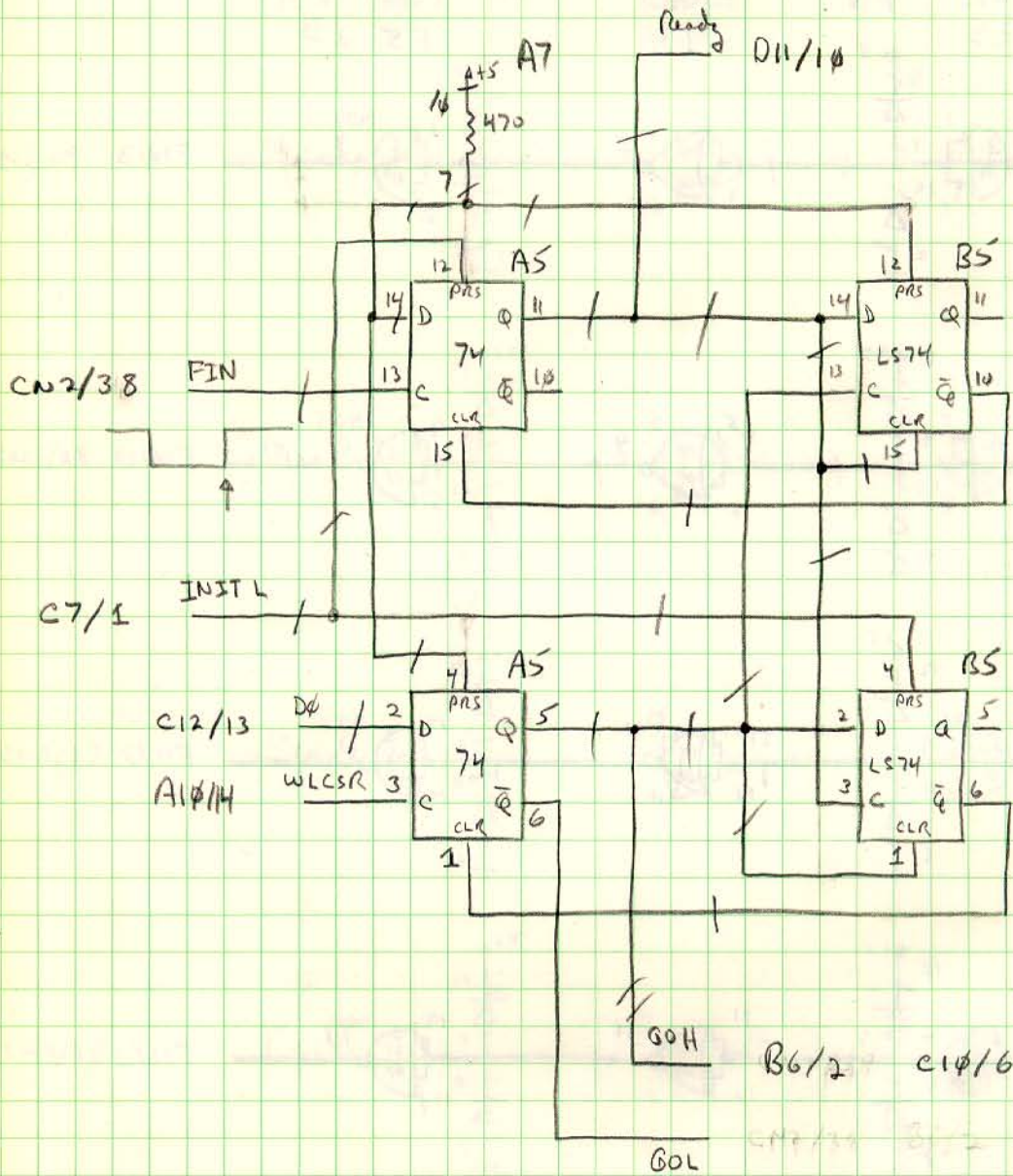




SPe 77  
ARs

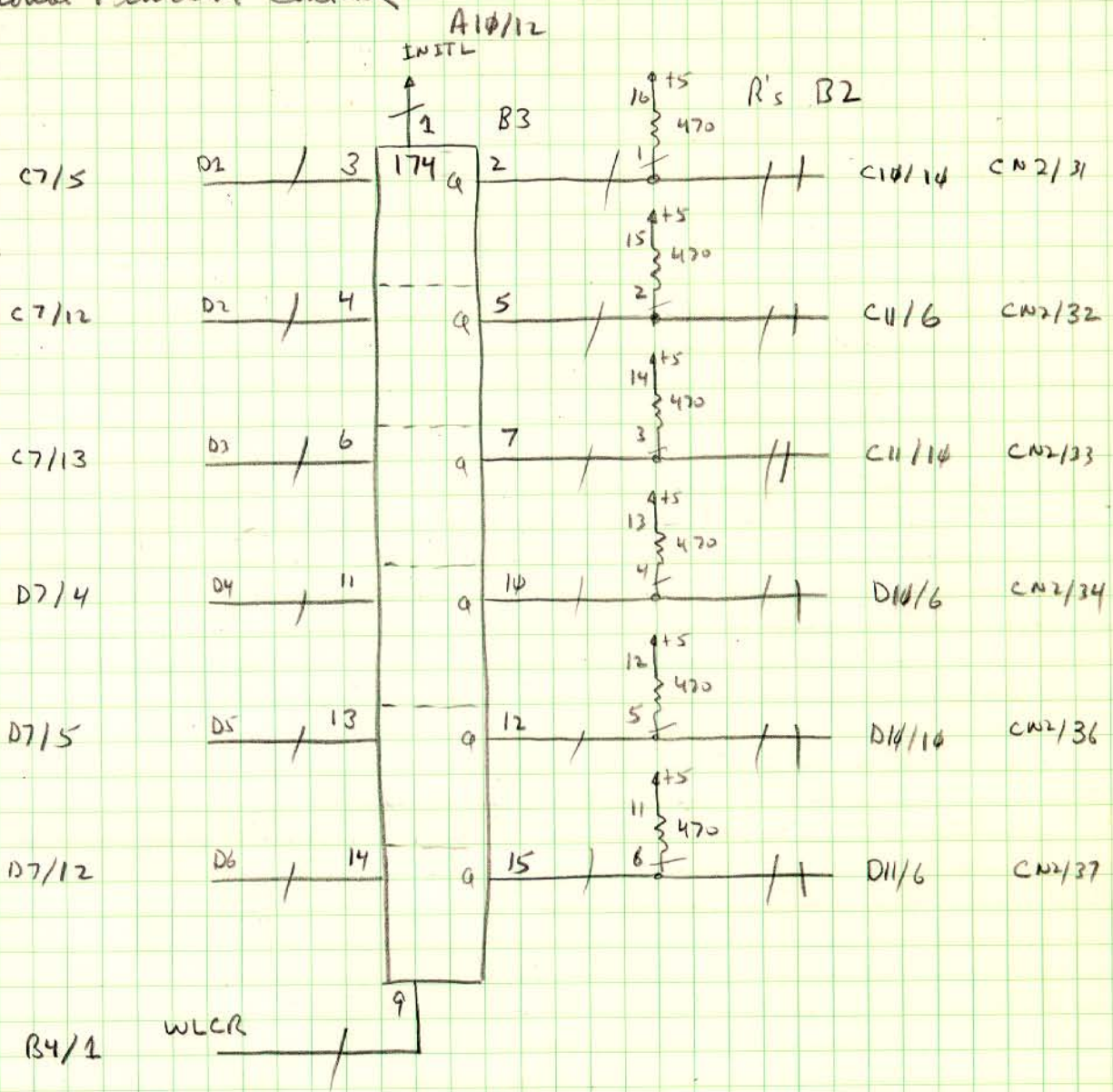


# Interface Control Logic





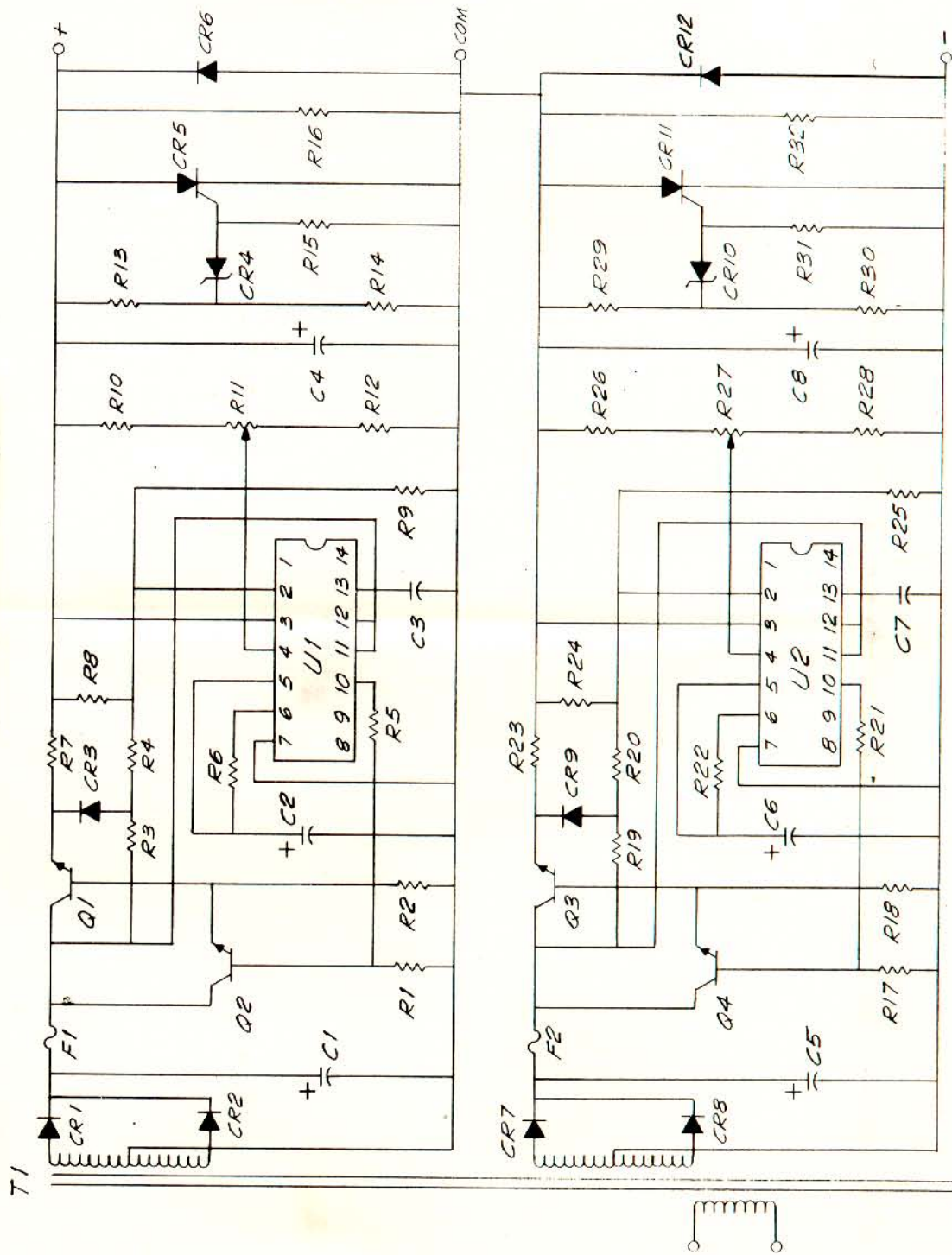
# Optional Function Control



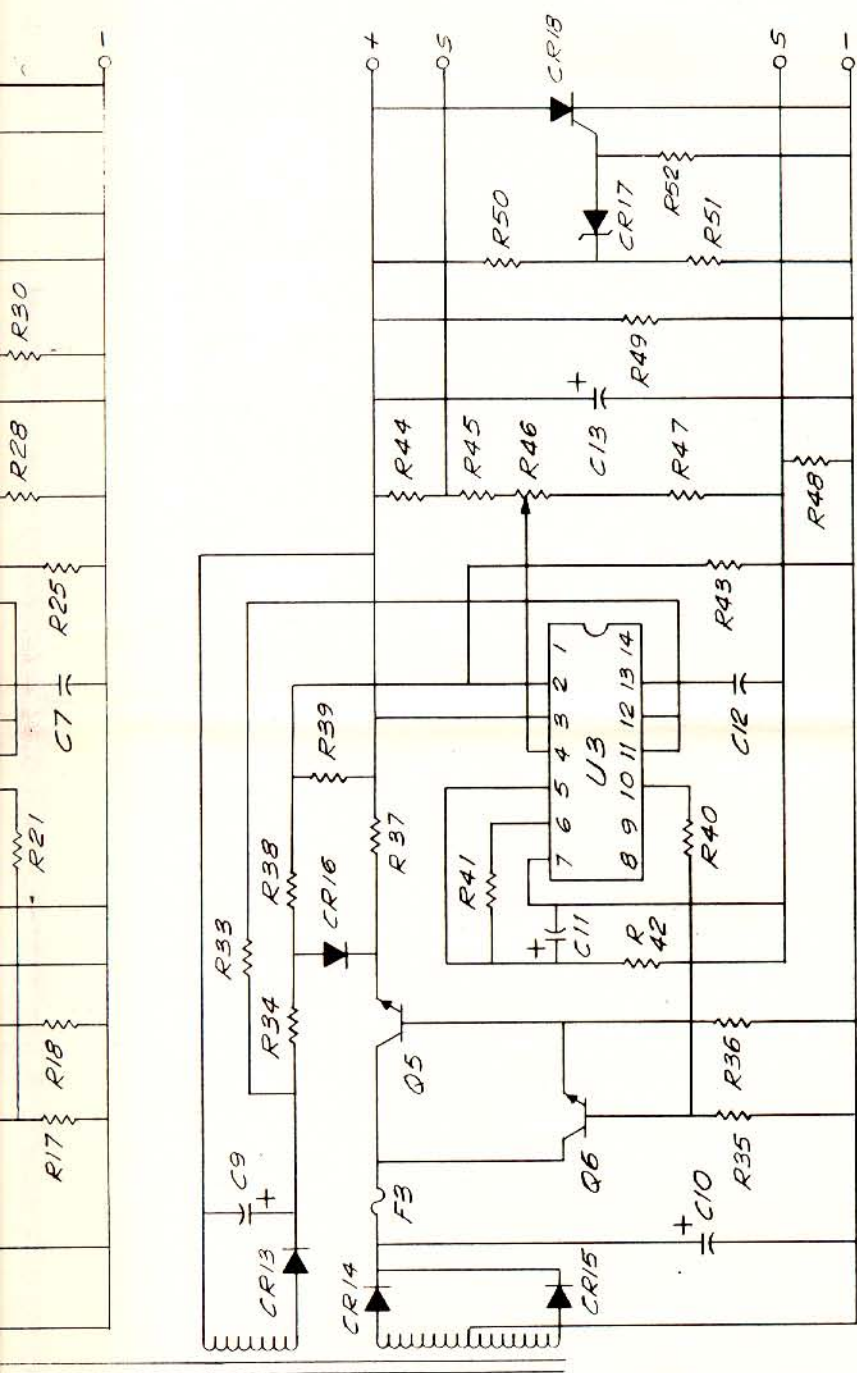
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APD



Internal 5, +12, -12 volt power supplies







**Electrostatics, Inc.**  
 7718 Clairemont Mesa Blvd. San Diego, CA 92111-1114 (714) 279-1414

**DC POWER SUPPLY**  
**MODEL 301**

**Electrostatics, Inc.** 7718 CLAIREMONT MESA BLVD. ■ SAN DIEGO, CALIFORNIA 92111 ■ TELEPHONE: (714) 279-1414

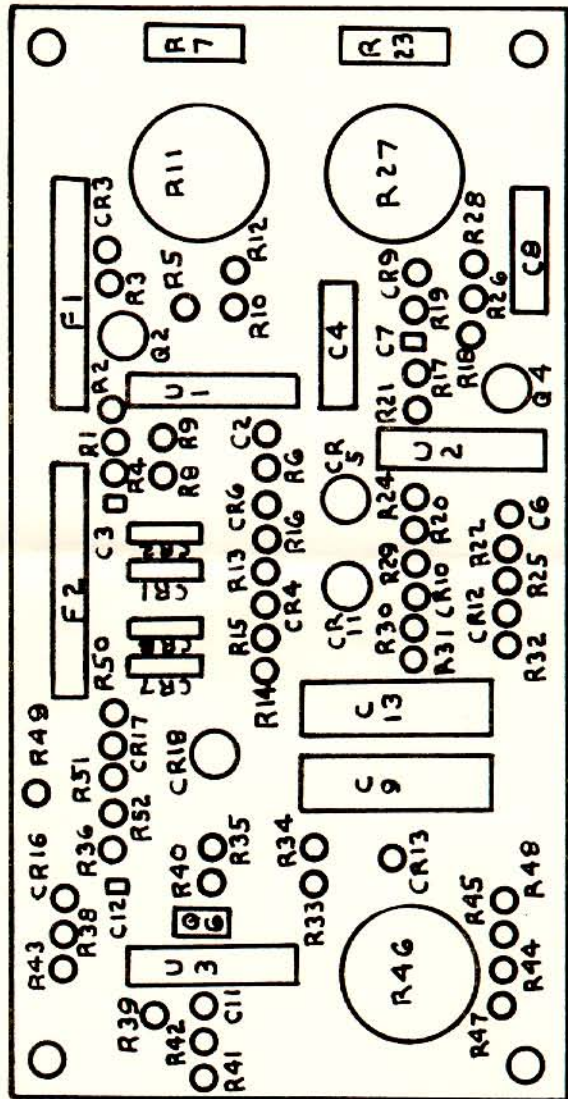
6 Dec 77  
 ARS



ELECTROSTATICS

DC Power Supply Model 301-12

PARTS LIST



RESISTORS

Part Number	Value	Quantity	Notes
R1, 17, 35	10K		
R2, 18	1.2K		
R3, 19	750		
R4, 20, 33, 38	100		
R5, 21	120		
R6, 22	910		
R7, 23	0.51		
R8, 15, 24, 31, 34, 36, 39, 51, 52	1K		
R9	0.4K		
R10	0.51		
R11, 27, 46	500		
R12, 28	820		
R13, 29	100		
R14, 30	680		
R16, 32, 41, 45	910		
R17, 19	0.05		3.75w WW
R20	510		
R21, 27, 46	500		
R22, 28	820		
R23	100		
R24	680		
R25	910		
R26	0.05		3.75w WW
R27	510		
R28	510		
R29	1.6K		
R30	10		
R31	10		
R32	10		
R33	10		
R34	10		
R35	10		
R36	10		
R37	10		
R38	10		
R39	10		
R40	10		
R41	10		
R42	10		
R43	10		
R44	10		
R45	10		
R46	10		
R47	10		



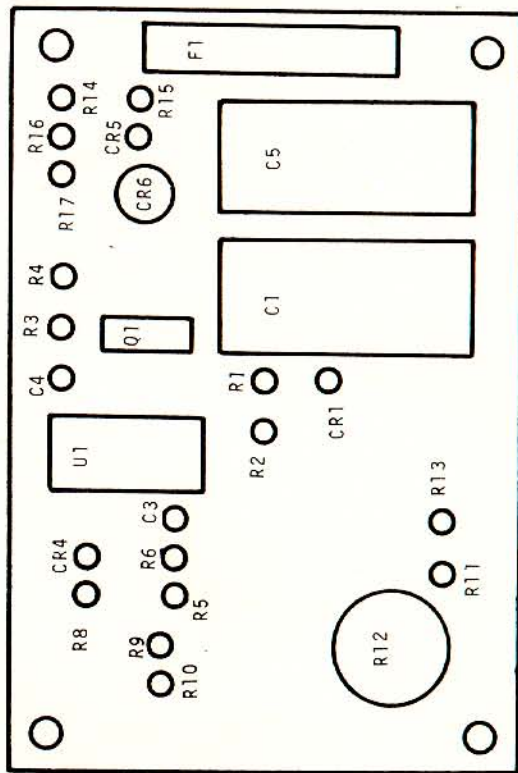
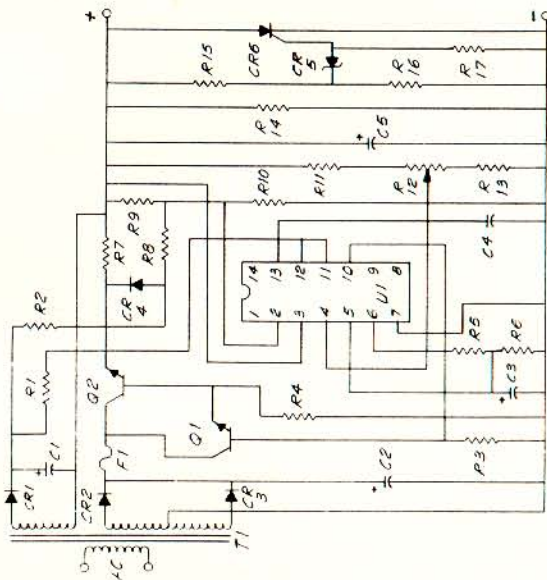




intermed 25A and 250 supply

DC POWER SUPPLY

MODEL 55-26



RESISTORS

- R1, 14 120
- R2, 9, 13, 17 1K
- R3 10K
- R4
- RL20
- RL20
- RL20
- RL20
- RL20

- R6 Omitted
- R7 .2
- R8, 15 100
- RL20



R1,14 120 RL20  
 R2,9,13,17 1K RL20  
 R3 10K RL20  
 R4 3.6K RL20  
 R5 910 RL20

R6 Omitted  
 R7 .2 WM  
 R8,15 100 RL20  
 R10 4.3K RL20  
 R11,16 3.3K RL20  
 R12 500 POT  
 R14 3.6K RL20

## CAPACITORS

C1 500 MFD 15V  
 C2 1600 MFD 50V  
 C3 4.7 MFD 50V  
 C4 1000 mmfd  
 C5 150 MFD 50V

## SEMICONDUCTORS

U1 Regulator 723C  
 Q1 2N5296  
 Q2 2N3055  
 CR1,4 1N4002  
 CR2,3 VTA200/T (VARO)  
 CR5 1N4750A (27V)  
 CR6 40654 (RCA)

F1 Fuse AGC4  
 T1 Transformer 55T26

NOTE: F1,R15,R16,R17,CR5, and CR6 are on units with overvoltage option only.

**Electrostatics, Inc.**

7718 CLAIREMONT MESA BLVD. ■ SAN DIEGO, CALIFORNIA 92111 ■ TELEPHONE: (714) 278-1414



## MODEL 301

### Electrical Specifications:

**INPUT:** 105-125 VAC. 47-420 Hz  
(230V OPTIONAL)

**REGULATION:** LINE: 0.005% or 2 MV MIN (10 VOLT CHANGE)  
LOAD: 0.05% OR 10 MV MIN  
(FULL LOAD CHANGE)

**RIPPLE:** LESS THAN 500 MICROVOLTS

**IMPEDANCE:** 100 Hz - 0.001 OHMS  
1 KHz - 0.005 OHMS  
10 KHz - 0.01 OHMS  
100 KHz - 0.1 OHMS

**RECOVERY TIME:** 25 MICROSECONDS

**OVERSHOOT:** NONE ON TURN ON OR OFF

**TEMPERATURE:** OPERATING -20 TO +71°C  
STORAGE -65 TO +85°C  
COEFFICIENT 0.01%/°C MAX

**CURRENT LIMITING:** FIXED - FOLDBACK TYPE -  
AUTOMATIC RECOVERY

**OUTPUT:** FLOATING

**SEMICONDUCTORS:** SILICON

**CAPACITORS:** COMPUTER GRADE - 10 YEAR LIFE

**OVERVOLTAGE PROTECTION:** OPTIONAL

## MODEL 55

### Electrical Specifications:

**INPUT:** 105-125 VAC. 50—420 Hz

**REGULATION:** LINE —0.005% OR 2 MV MIN (10 VOLT CHANGE)  
LOAD: 0.05% OR 10 MV MIN (FULL LOAD CHANGE)

**RIPPLE:** LESS THAN 250 MICROVOLTS

**IMPEDANCE:** 100 Hz — 0.001 OHMS  
1 KHz — 0.005 OHMS  
10 KHz — 0.01 OHMS  
100 KHz — 0.1 OHMS

**RECOVERY TIME:** 25 MICROSECONDS

**OVERSHOOT:** NONE ON TURN ON OR OFF

**TEMPERATURE:** OPERATING -40 TO +71°C  
STORAGE -65 TO +85°C  
COEFFICIENT 0.01%/°C MAX

**CURRENT LIMITING:** FIXED - FOLDBACK TYPE -  
AUTOMATIC RECOVERY

**OUTPUT:** FLOATING.

**SEMICONDUCTORS:** SILICON

**CAPACITORS:** COMPUTER GRADE — 10 YEAR LIFE

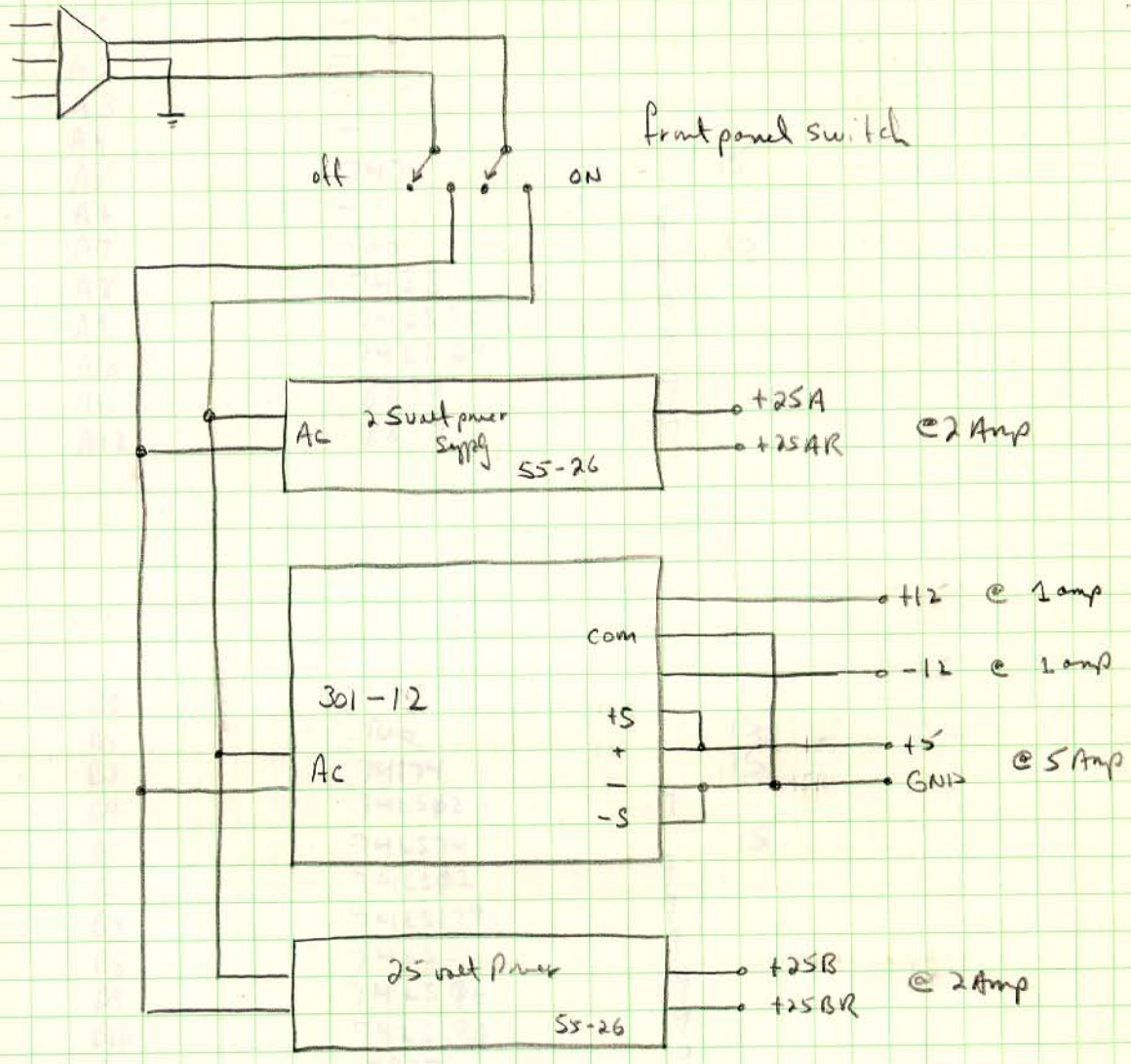
**OVERVOLTAGE PROTECTION:** FIXED CROWBAR - OPTIONAL

**WEIGHT:** 4.25 LBS



# AC Power Wiring

3 wire 120VAC 60Hz



6 Dec 77  
ASD



# Parts Location Lists

A1	---		
A2	---		
A3	---		
A4	---		
A5	7474		15
A6	---		
A7	Res.	9	15
A8	7438	9	
A9	74LS30	9	
A10	74LS04	9	
A11	8837	9	
A12	8837	9	

B1	---		
B2	Res		15
B3	74174		15
B4	74LS02	9	
B5	74LS74		15
B6	74LS02	9	
B7	74LS139	9	
B8	74LS32	9	
B9	74LS00	9	
B10	74LS30	9	
B11	8837	9	
B12	8837	9	

6 Dec 77  
AAS



C1	---	
C2	Res	13
C3	Diodes	13
C4	MC14001	13
C5	74LS00	13
C6	Res	12
C7	74175	12
C8	Res	11
C9	74175	11
C10	74LS153	10
C11	74LS153	10
C12	8838	10

D1	---	
D2	Res	13
D3	Diodes	13
D4	MC14001	13
D5	74LS00	13
D6	Res	12
D7	74175	12
D8	Res	11
D9	74175	11
D10	74LS153	10
D11	74LS153	10
D12	8838	10



E1	- - -	
E2	Res	14
E3	Diodes	14
E4	MC1400	14
E5	74LS44	14
E6	Res	12
E7	74175	12
E8	Res	11
E9	74175	11
E10	74LS153	10
E11	74LS153	10
E12	8838	10

F1	- - -	
F2	Res	14
F3	Diodes	14
F4	MC1400	14
F5	74LS44	14
F6	Res	12
F7	74175	12
F8	Res	11
F9	74175	11
F10	74LS153	10
F11	74LS153	10
F12	8838	10

6 Dec 77  
AM



Designed to program

- a) Intel (45V) 2716 (2Kx8 EPROMs) MOS
- b) 6834 (512x8 EPROMs) MOS
- c) 74S387 (256x4 PROMs) Bipolar

The Programmer ID will read as (Byte 177111<sub>8</sub>)

- a)  $\phi\phi 1_8$  for 2716 ,
- b)  $\phi\phi 2_8$  for 6834 ; or
- c)  $\phi\phi 4_8$  for 3387

When the strapping plug is inserted properly - otherwise  
it will read  $\phi\phi\phi_8$

When the ID =  $\phi\phi 4_8$  bit FS controls the S387  
programmer pulse time

FS = '0' normal 1ms program pulse

FS = '1' extended 70ms program pulse







# 100 Pin Connector

## Topside

1	+25A	+	A14/13	26	MA12	-		1
2	+25A			27	MA13	-		2
3	+25B	+	A14/11	28	MA14	-		3
4	+25B			29	MA15	-		4
5	+12	+	D14/8	30	GND			5
6	+12			31	MD0	+	A11/10	6
7	GND	+	A13/8	32	MD1	+	A11/12	7
8	GND	+	A12/8	33	MD2	+	A11/6	8
9	GND	+	A11/8	34	MD3	+	A11/4	9
10	GND	+	A10/8	35	GND			10
11	MA0	+	D12/24	36	MD4	+	A10/10	11
12	MA1	+	D12/23	37	MD5	+	A10/12	12
13	MA2	+	D12/22	38	MD6	+	A10/6	13
14	MA3	+	D12/21	39	MD7	+	A10/4	14
15	GND			40	GND			15
16	MA4	+	D12/20	41	MD8	-		16
17	MA5	+	D12/19	42	MD9	-		17
18	MA6	+	D12/18	43	MD10	-		18
19	MA7	+	D12/17	44	MD11	-		19
20	GND			45	GND			20
21	MA8	+	D12/17	46	MD12	-		21
22	MA9	+	D3/22	47	MD13	-		22
23	MA10	+	D3/19	48	MD14	-		23
24	MA11	-		49	MD15	-		24
25	GND			50	GND			25



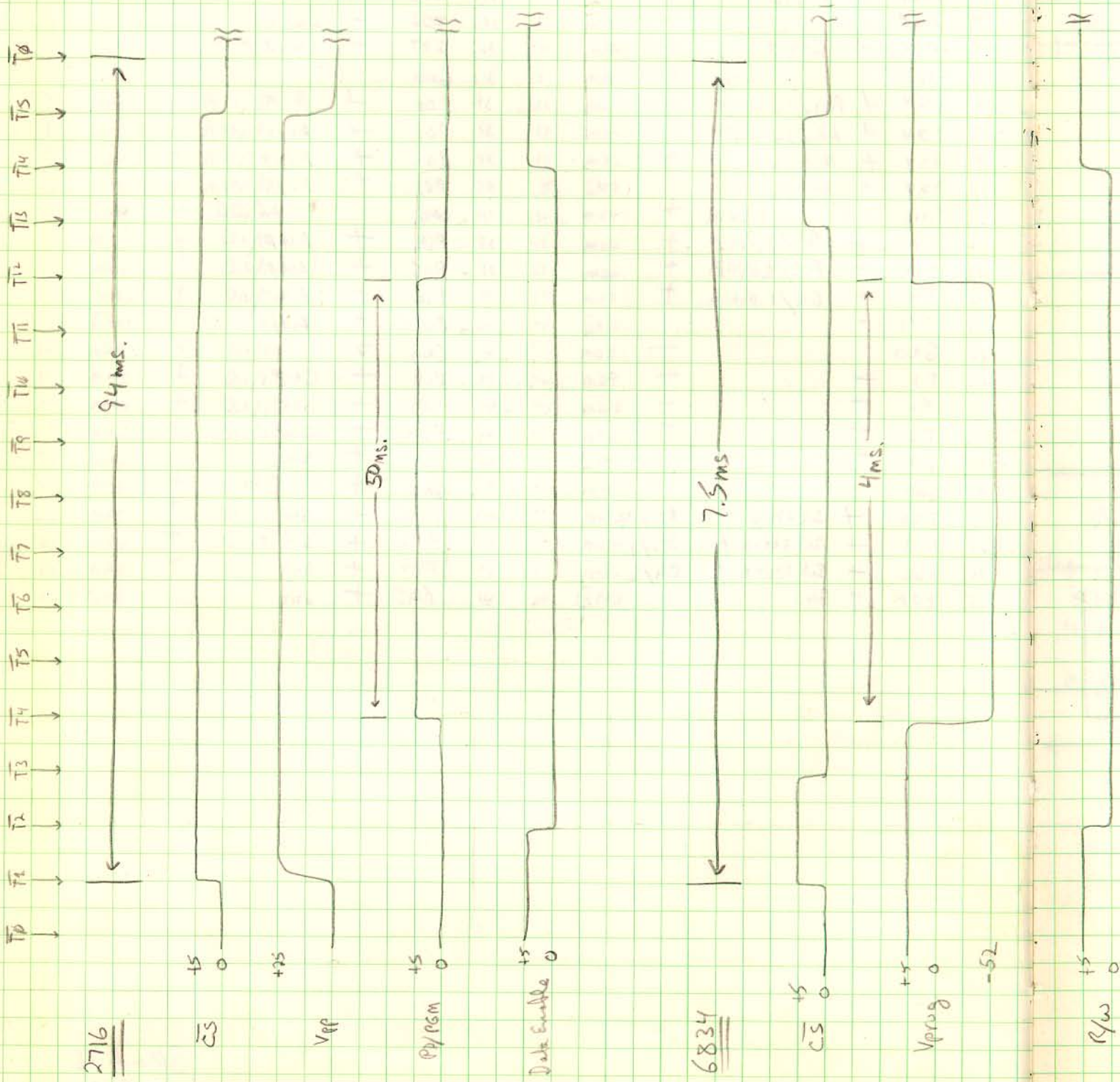
## Bottom Side

1	25AR	+ A14/12		
2	25AR			
3	25BR	+ A14/14		
4	25BR			
5	-12V	+ C14/8		
6	-12V			
7	+5V	+ A12/16		
8	+5V	+ A11/16		
9	+5V	+ A10/16		
10	+5V	+ A9/16		
11	GND			
12	G0H	+ A1/3		
13	F1W	+ A1/1		
14	F5	+ B11/1		
15	F4	-		
16	GND			
17	F3	-		
18	F2	-		
19	F1	-		
20	F0	-		
21	GND			
22	ID6	+ Sel 27164 +	B13/4	
23	ID1	+ Sel 68344 +	B13/2	
24	ID2	+ Sel 53574 +	B11/2	
25	ID3	+ GND		
26	GND			↓
27	ID4			+ GND
28	ID5			+ GND
29	ID6			+ GND
30	ID7			+ GND
31	GND			
32	RD0			↓ A11/9
33	RD1			→ A4/4
34	RD2			+ A11/7
35	RD3			+ A4/5
36	GND			
37	RD4			+ A10/9
38	RD5			+ A10/11
39	RD6			+ A10/7
40	RD7			+ A10/5
41	GND			↓
42	RD8			+ GND
43	RD9			+ GND
44	RD10			+ GND
45	RD11			+ GND
46	GND			↓
47	RD12			+ GND
48	RD13			+ GND
49	RD14			+ GND
50	RD15			+ GND

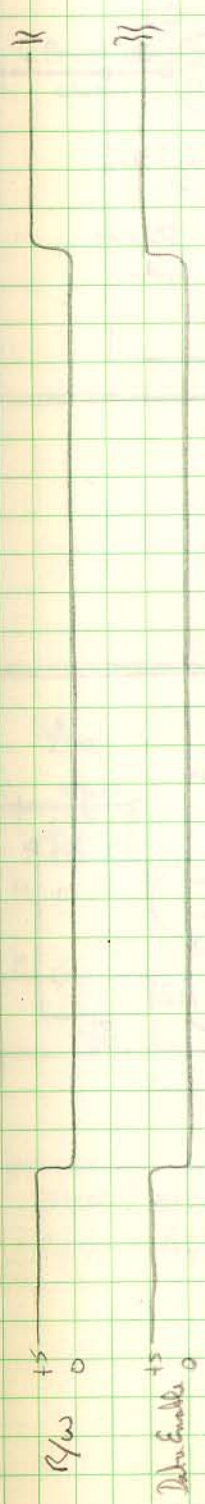
3 March 78  
A.R.



Programming Cycle - 2716, 6834, 74S387



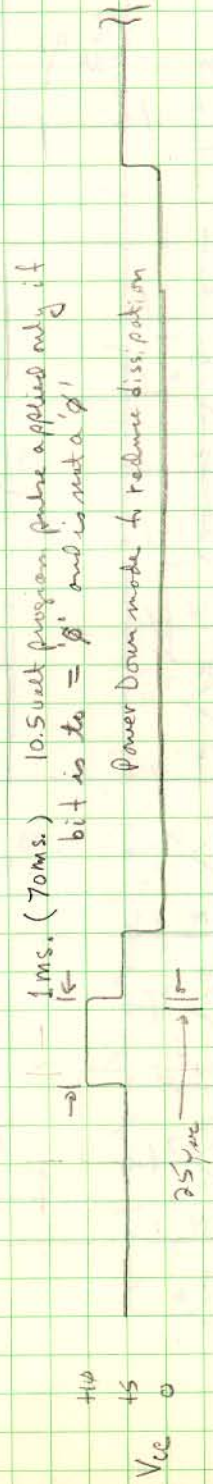




74S387 15ms. (1.05 seconds)  
(Repeated 4 times for single address)



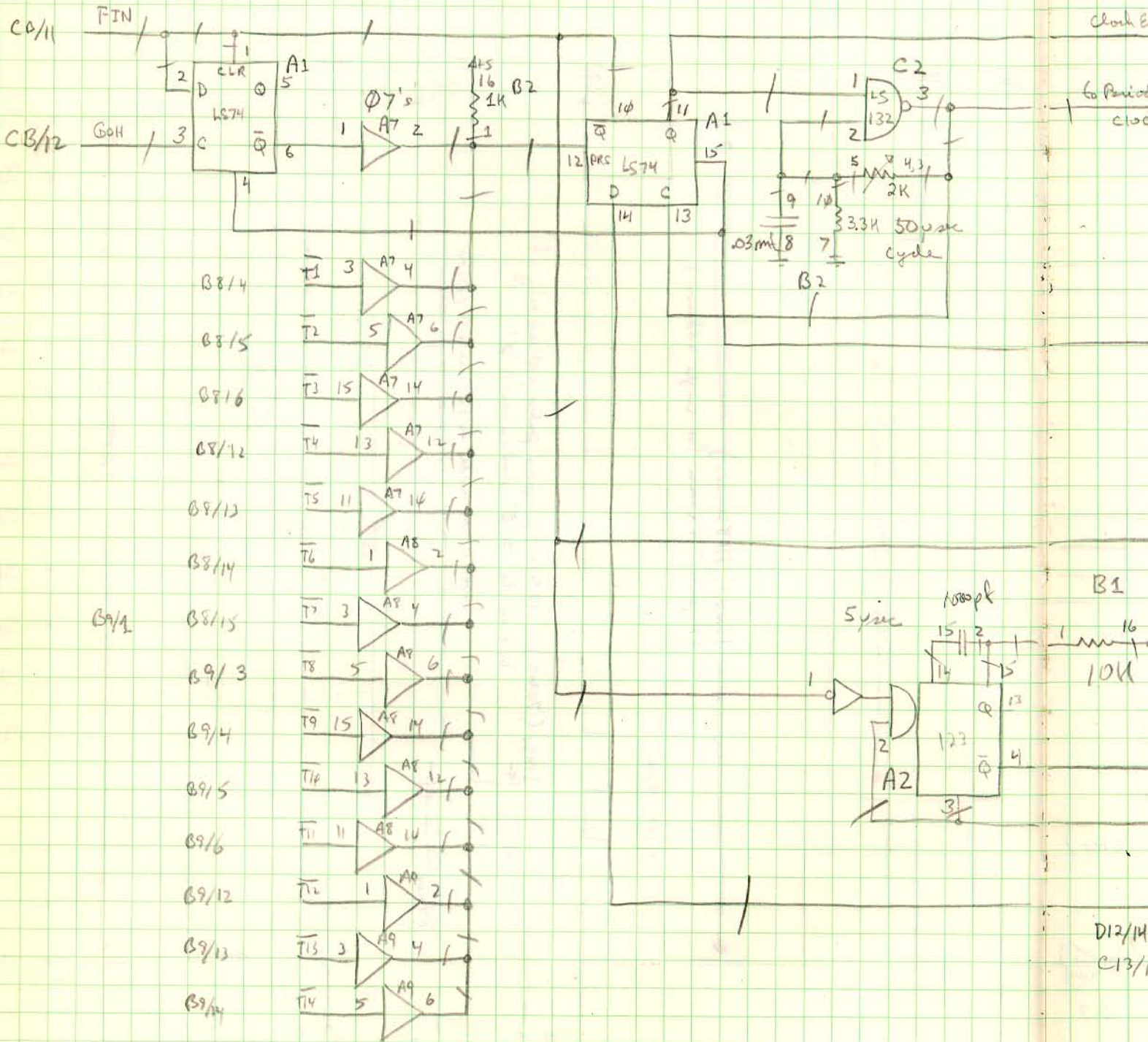
1ms. (70ms.) 10.5 volt program pulse applied only if bit is 0 and is not a '0'  
Power Down mode to reduce dissipation



3 March 78  
ARB



# Scan Timer

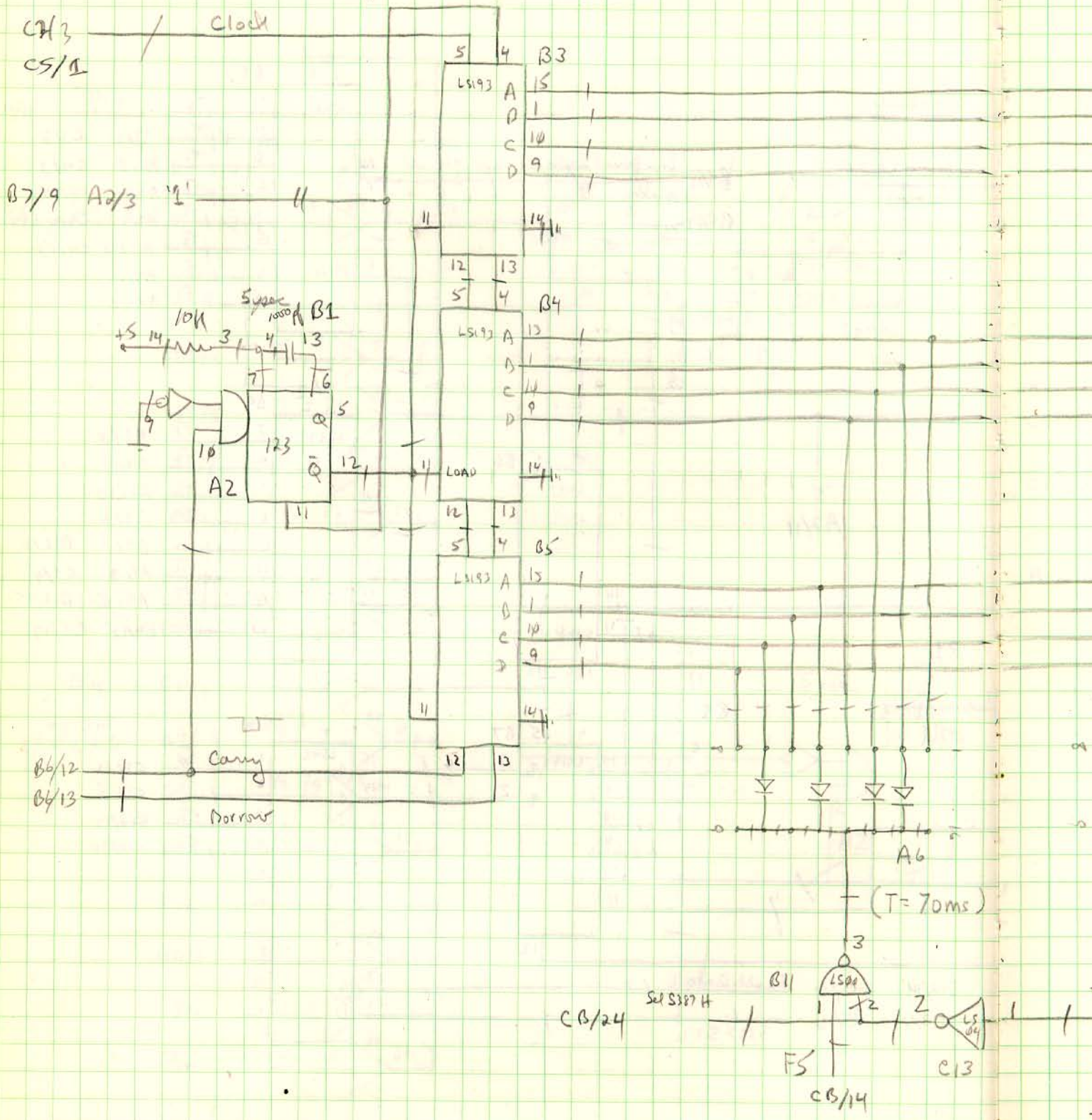






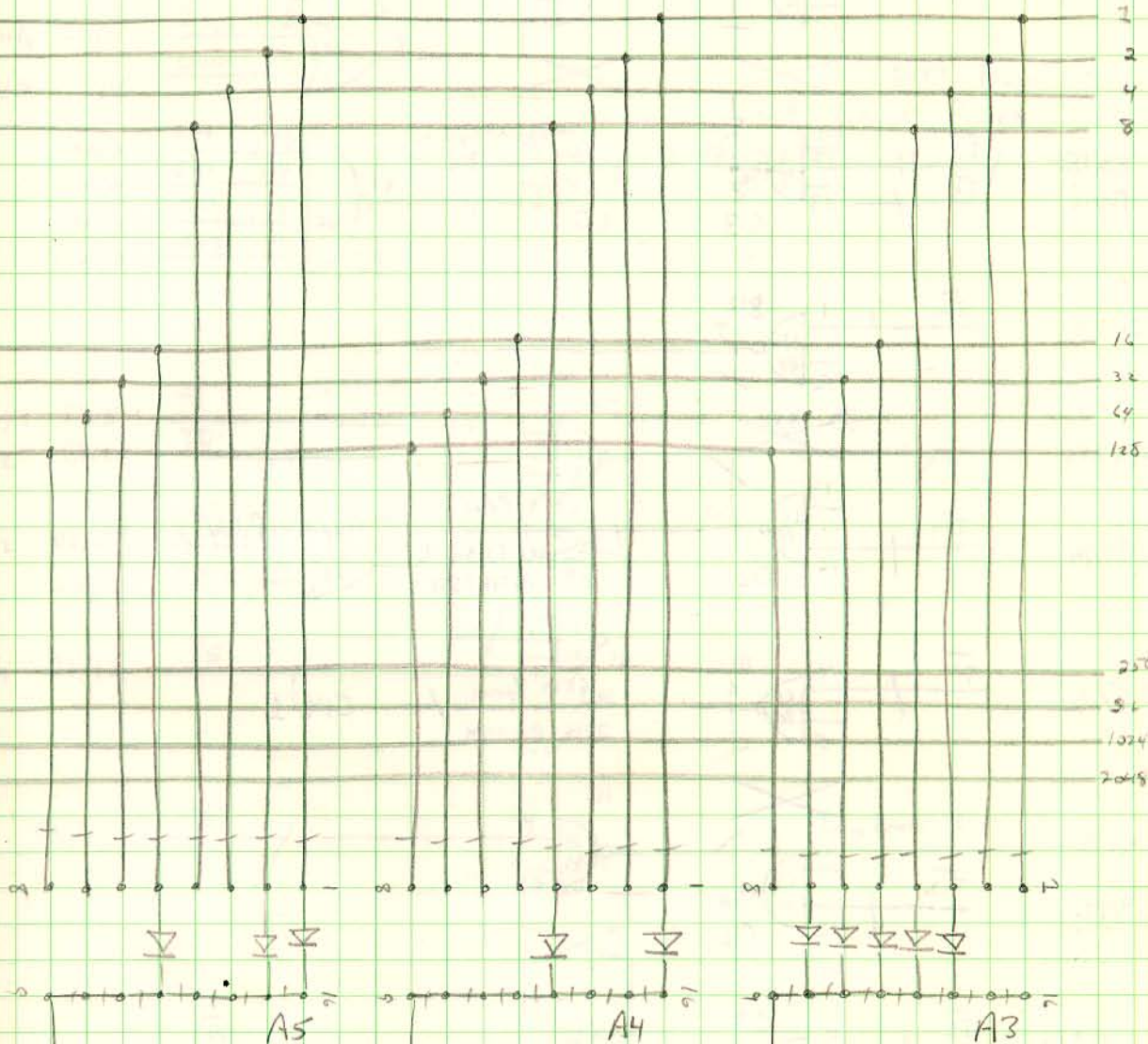


# Scan Period Selector





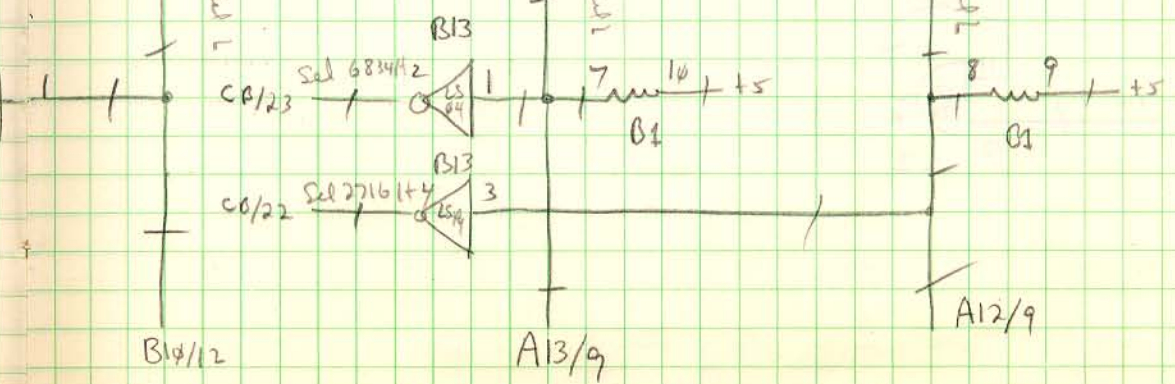
Periods selected by inserting diodes for  $\phi$  bits  
of 2's complement of clock pulses per  $T$  interval



5387 CA1  
 $T = 1 \text{ms}$

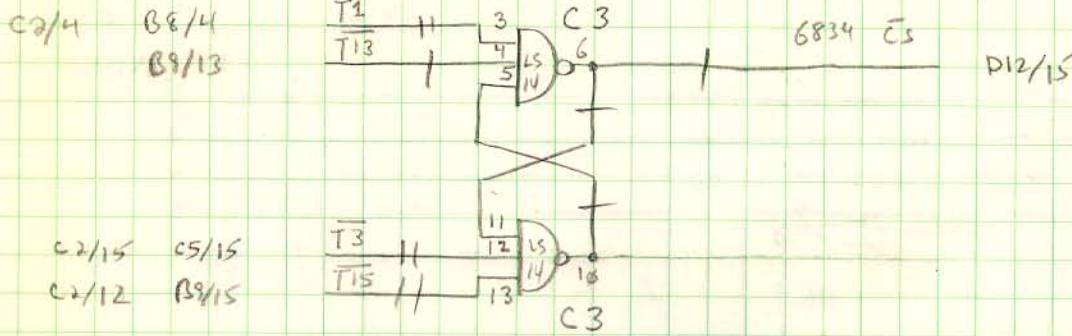
6814 CA1  
 $T = .5 \text{ms}$

916 SA1  
 $T = 6.25 \text{ms}$



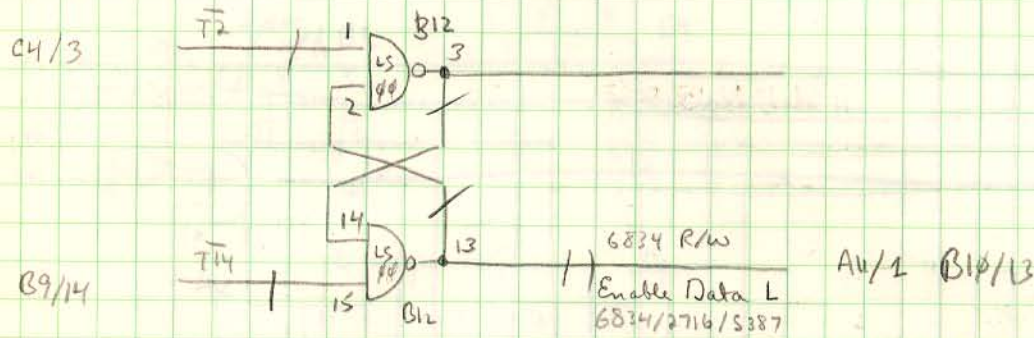
3 March 78  
 ARD



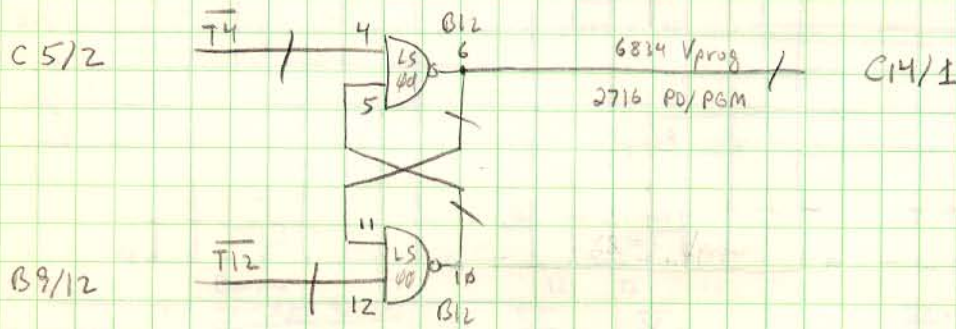


B11/4  
B3/5

C2/15    C5/15  
C2/12    B9/15

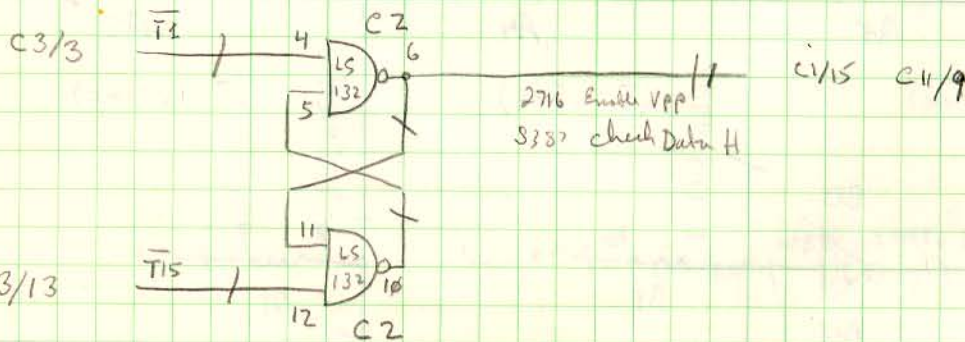


B12/1  
C5/2  
C3/12



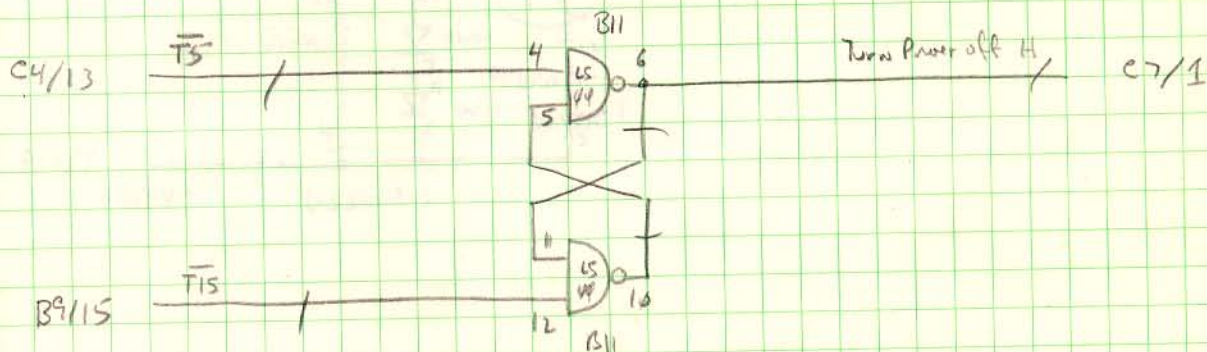
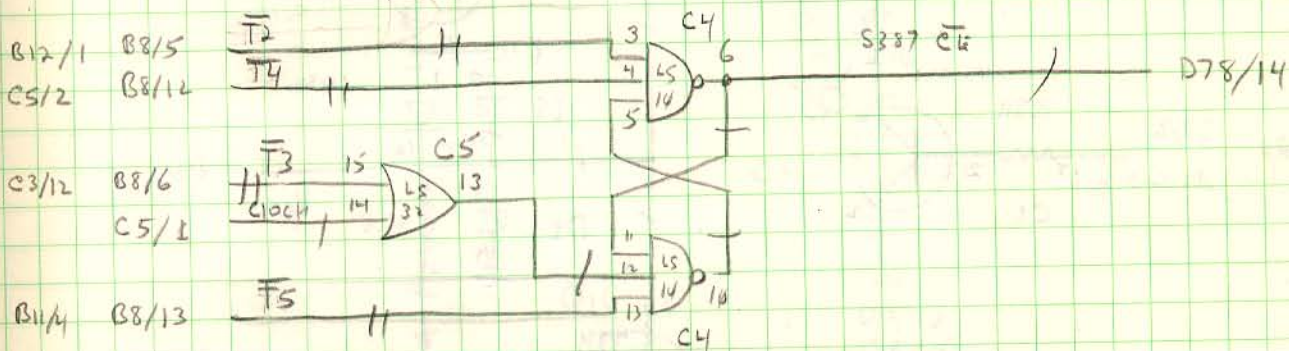
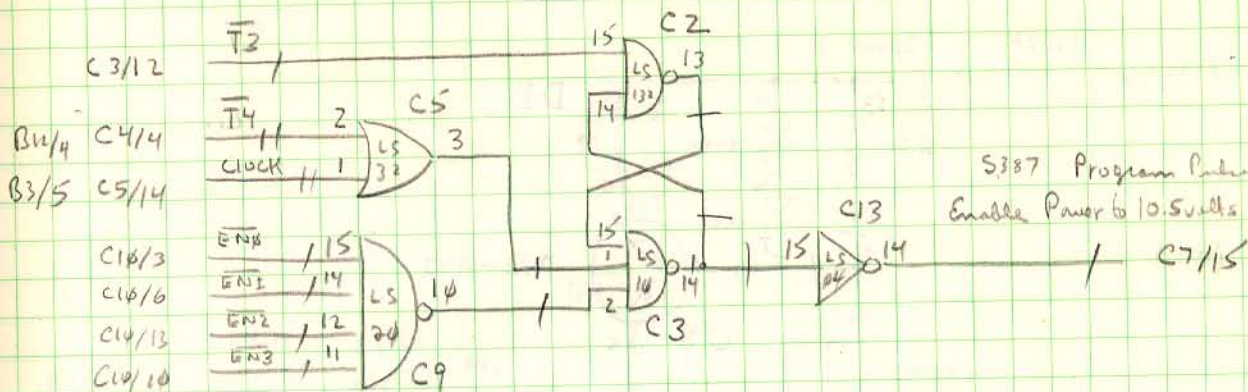
B11/4

B9/12

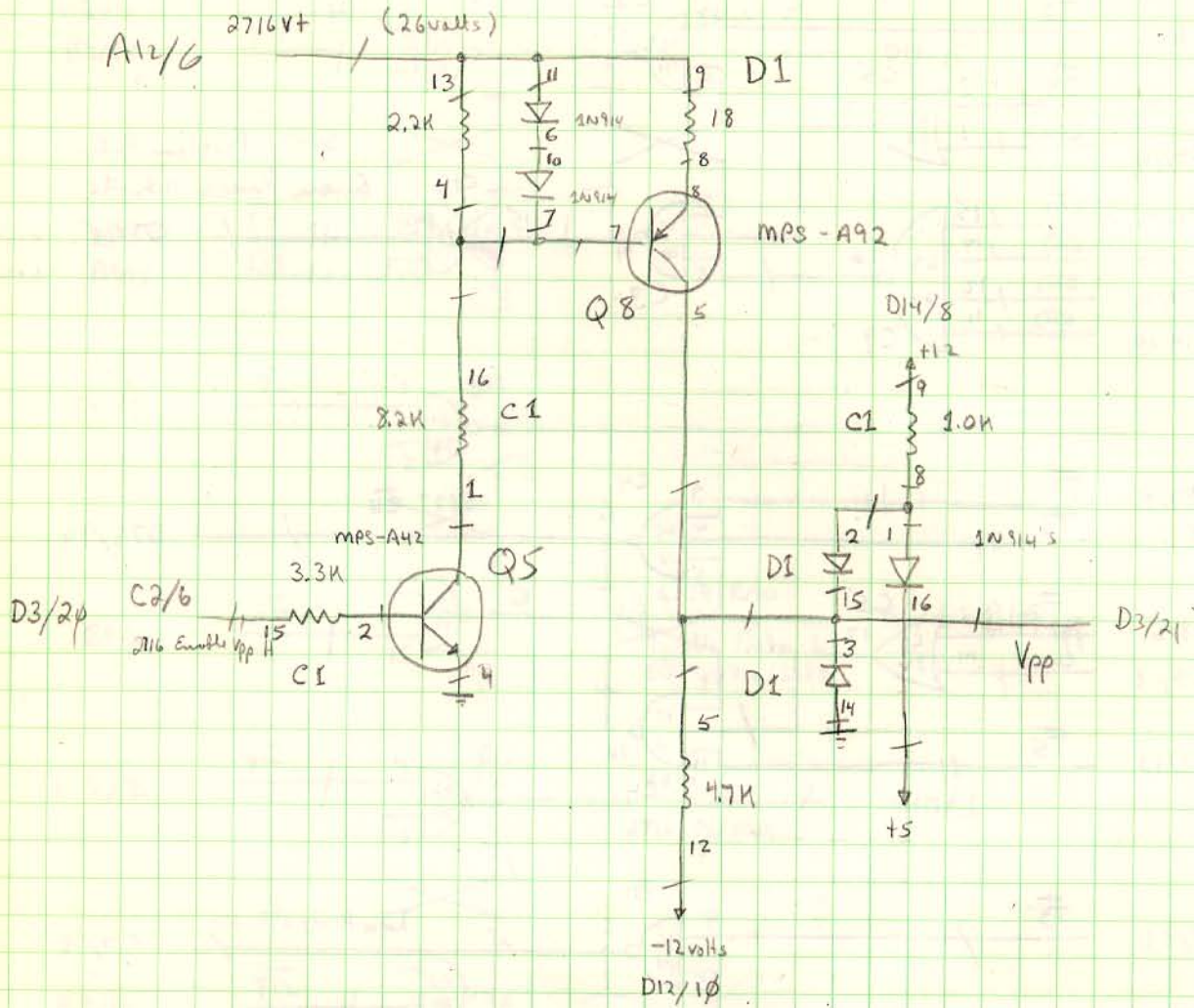


C3/13

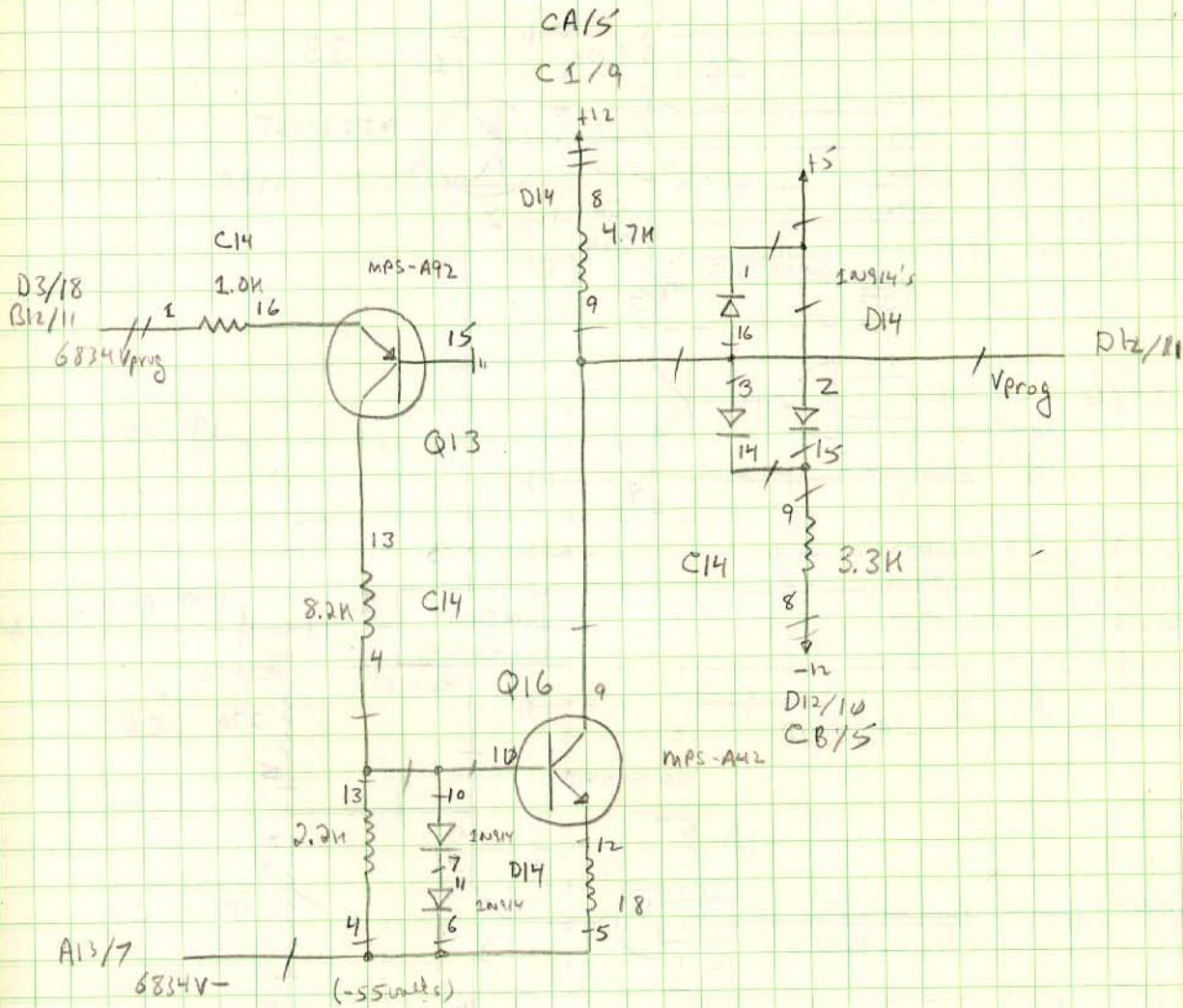








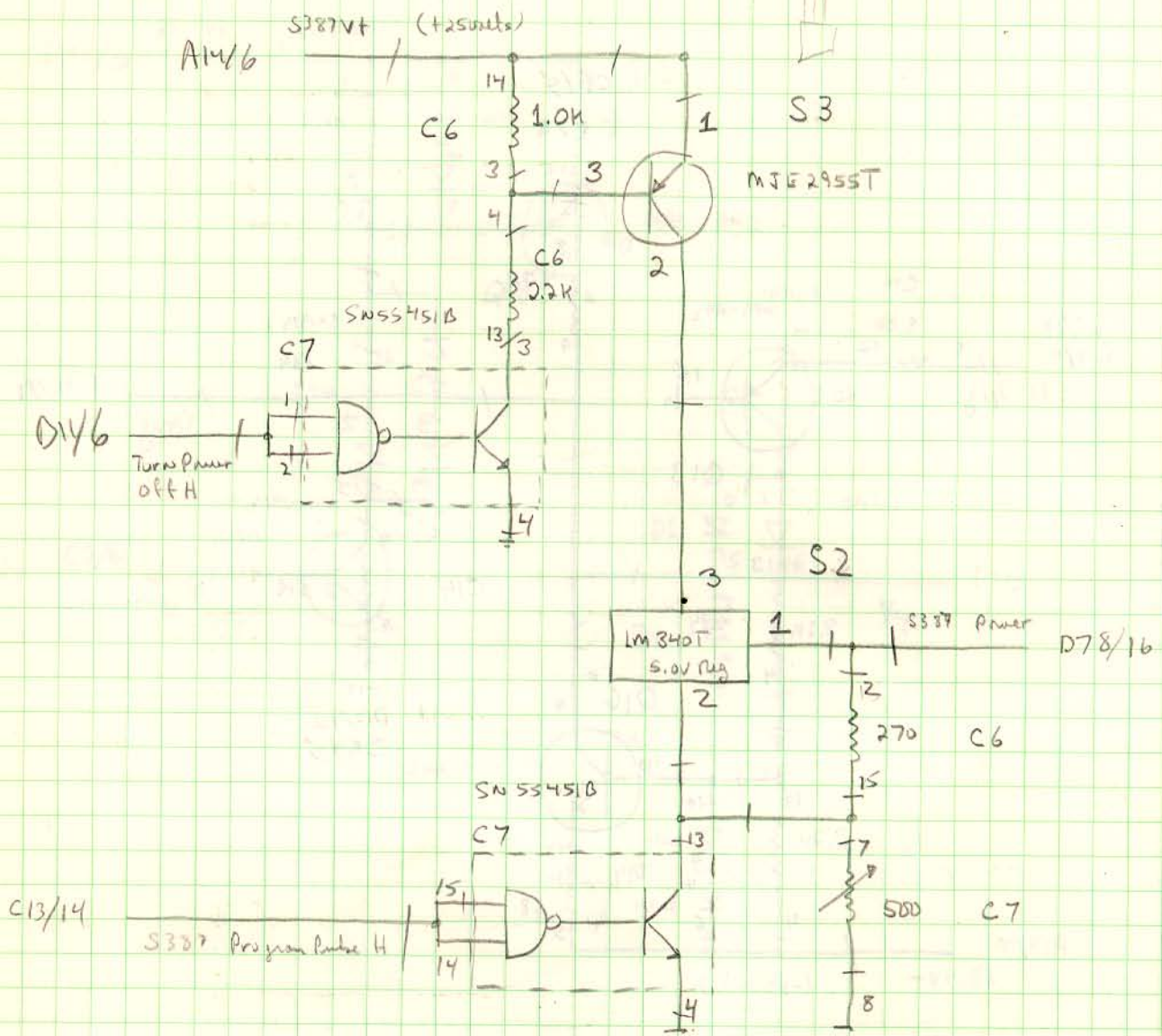
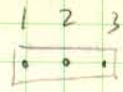




6 March 78  
AR0

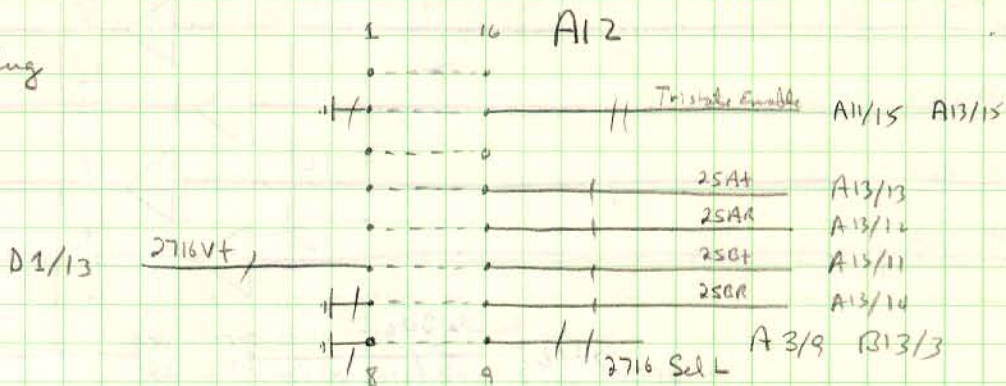


# S387 Pulse generation

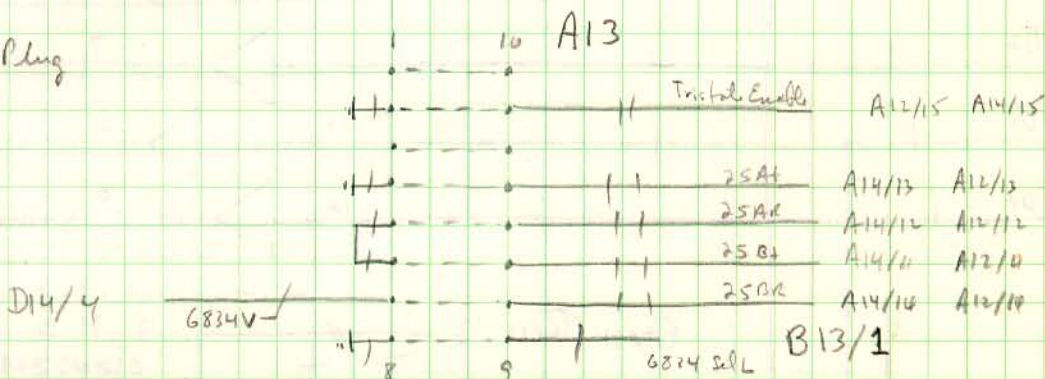




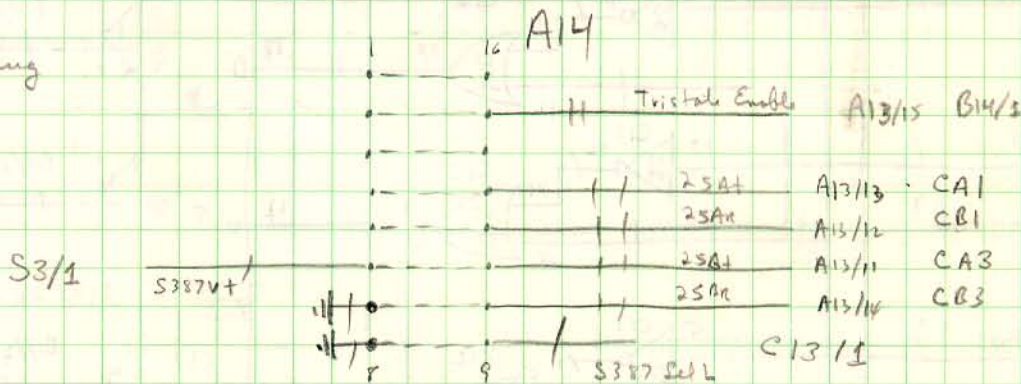
2716 Plug



6834 Plug



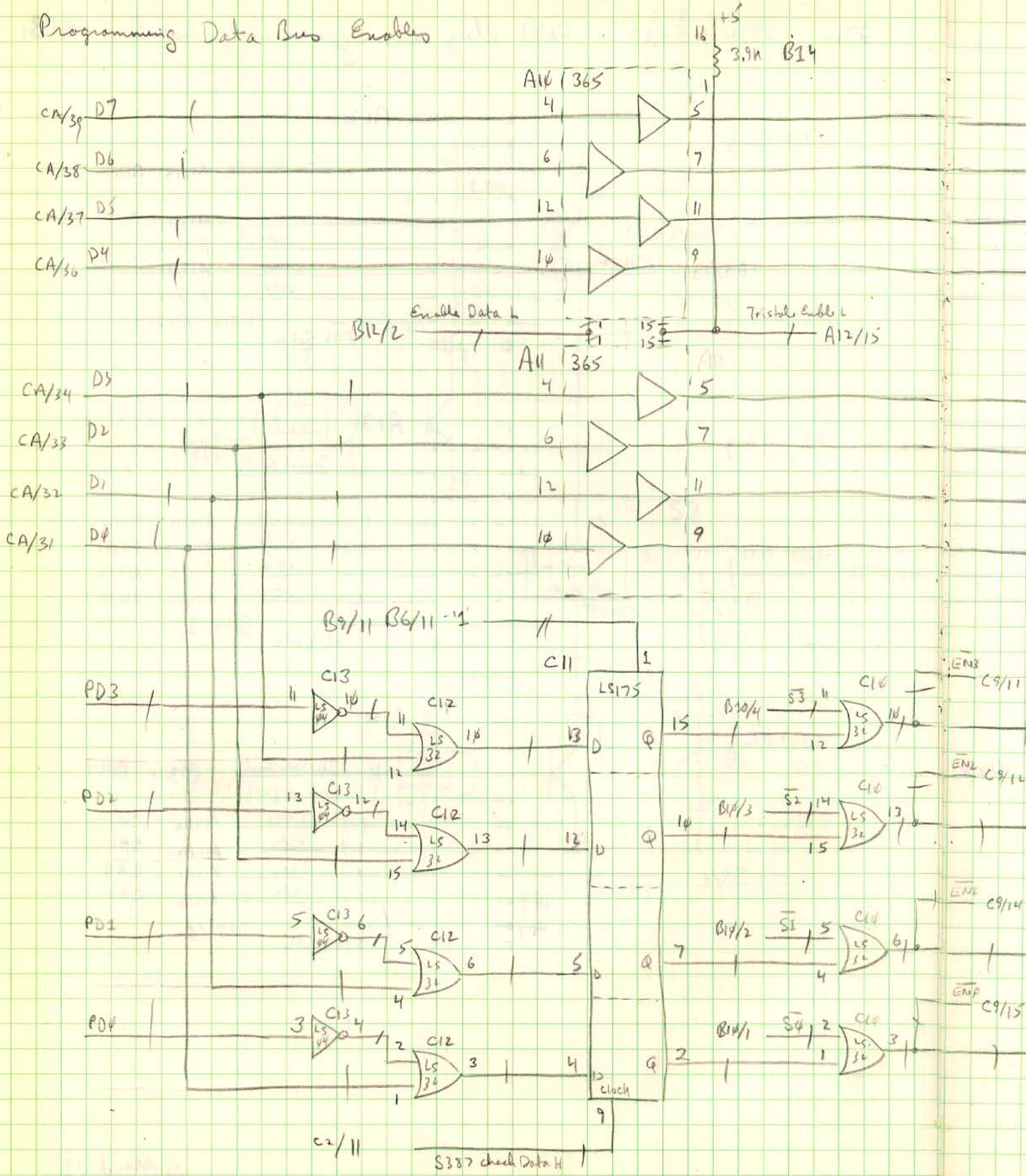
S387 Plug



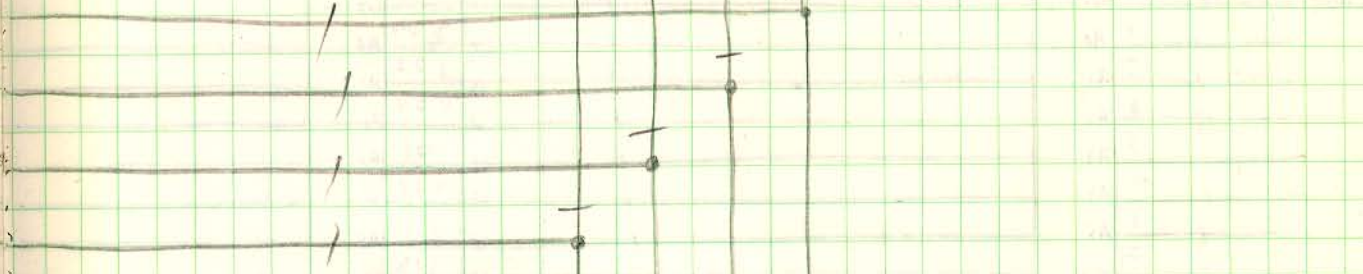
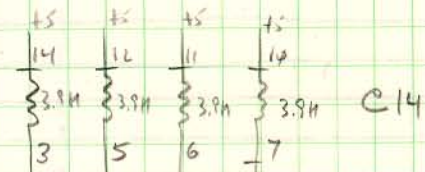
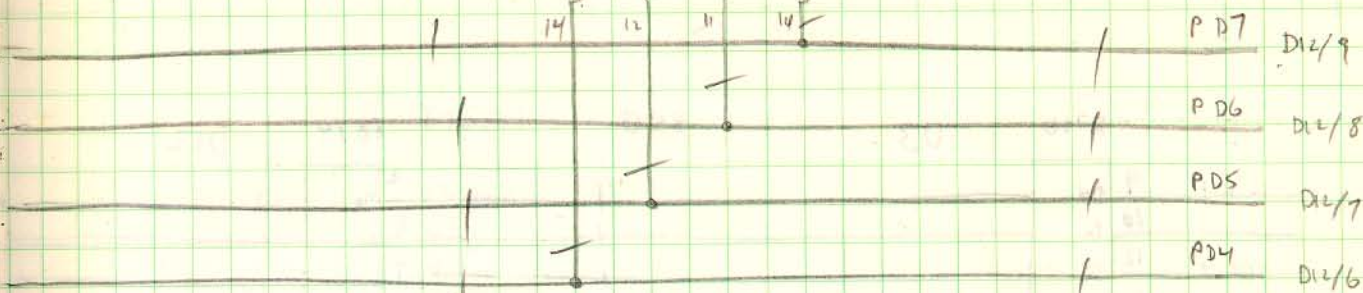
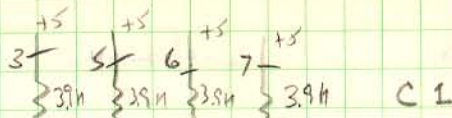
6 March 78  
ASD



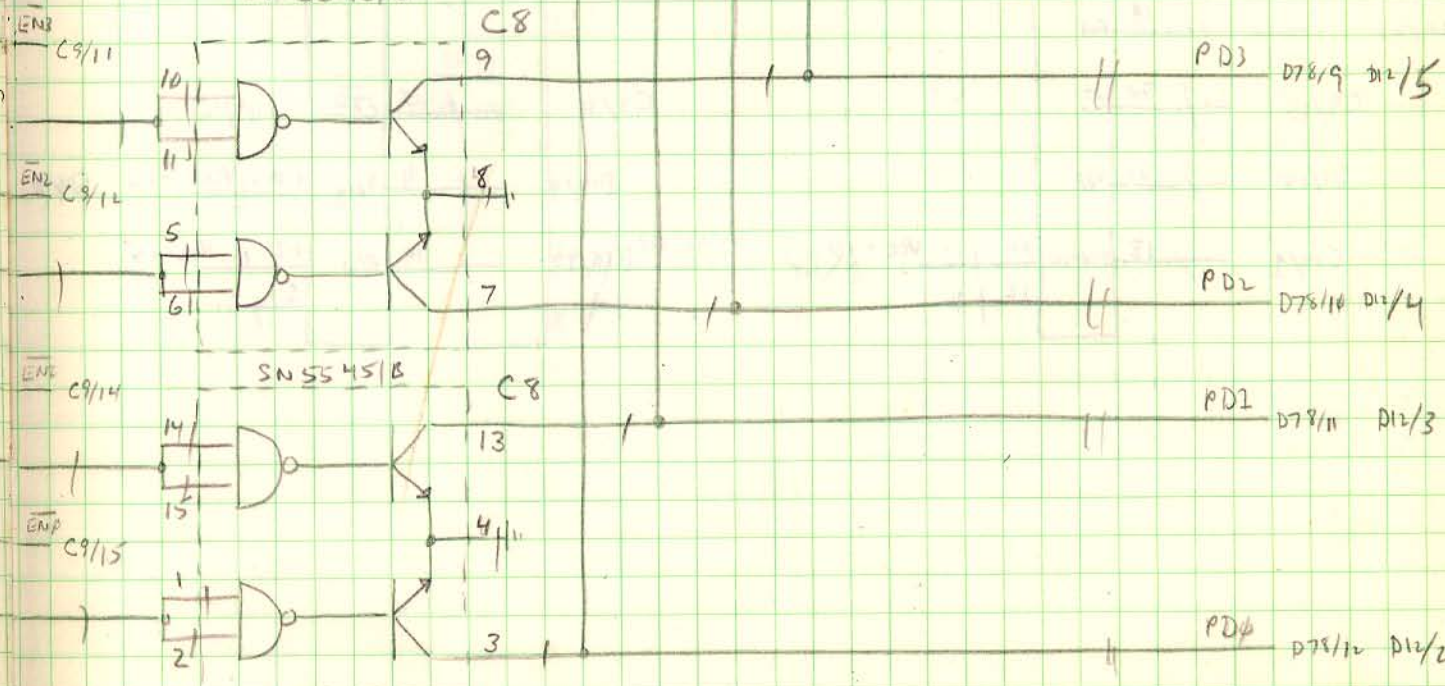
# Programming Data Bus Enable







Power @ 16, 12  
GND @ 4, 8  
SN55451B



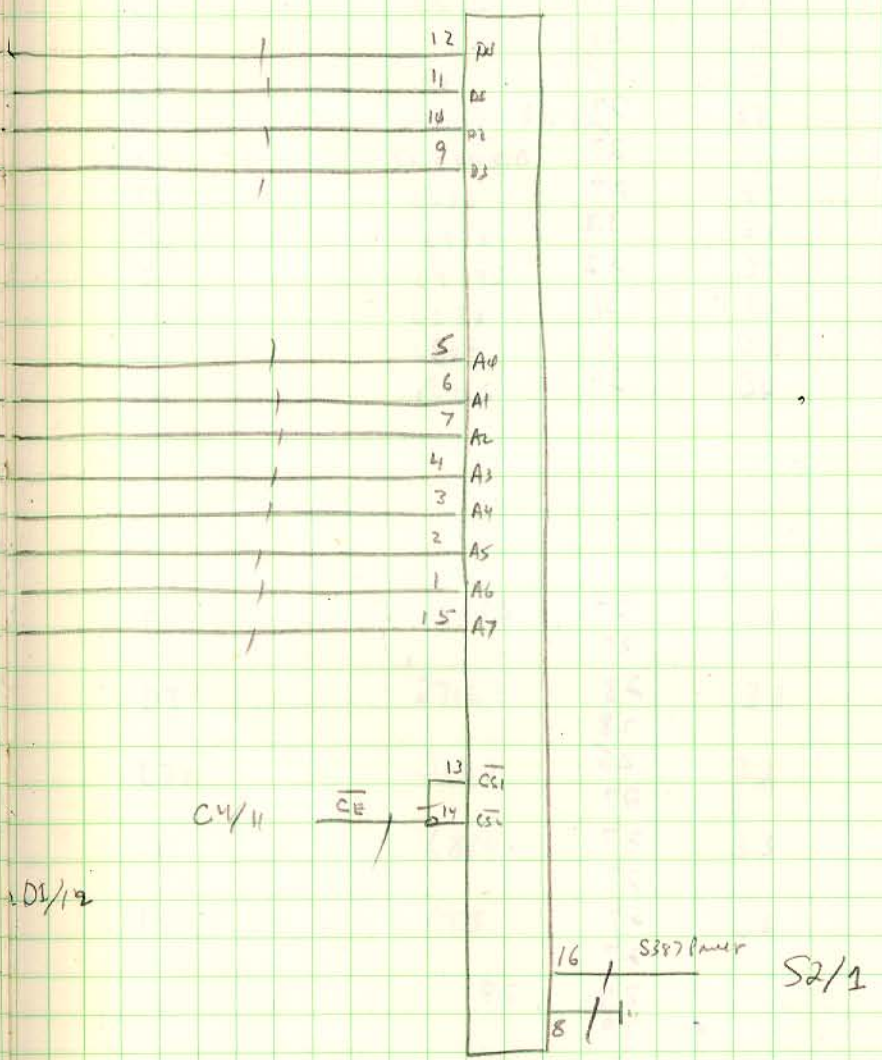
6 March 78  
A00







74S387 D78



6 March 78  
ARD



# IC Locations

A1	LS74	27
A2	123	27 , 28
A3	Diodes	28
A4	Diodes	28
A5	Diodes	28
A6	Diodes	28
A7	Ø7	27
A8	Ø7	27
A9	Ø7	27
A10	365	32
A11	365	32
A12	2716 JUMPER	31
A13	6834 JUMPER	31
A14	5387 JUMPER	31

B1	RES	27 , 28 , 32
B2	RES	27
B3	LS193	28
B4	LS193	28
B5	LS193	28
B6	LS193	27
B7	LS193	27
B8	LS164	27
B9	LS164	27
B10	LS42	27
B11	LSØØ	28 , 29
B12	LSØØ	29
B13	LSØØ	28
B14	RES	32



C1	RES	30	32
C2	LS132	27	29
C3	LS10	29	
C4	LS10	29	
C5	LS32	29	
C6	RES	31	
C7	SN55451B / R <sub>60</sub>	31	31
C8	SN55451B	31	
C9	LS20	29	
C10	LS32	32	
C11	LS175	32	
C12	LS32	32	
C13	LS04	28	32
C14	RES	30	32

D1	RES	30
D3	2716	33
D78	S387	33
D12	6834	33
D14	RES	30

S1		
S2	LM340T-5.0	31
S3	MJE 2955T	31
S4		



Q1

Q2

Q3

Q4

Q5

MPS-A42

34

Q6

Q7

Q8

MPS-A92

34

Q9

Q10

Q11

Q12

Q13

MPS-A92

34

Q14

Q15

Q16

MPS-A42

34

Construction Completed 8 March 78  
APB



# PROM / EPROM Card # 1

36

Designed to Program

±5V. +12V.	}	1) TI's	2716	(2Kx8 EPROMs)	MOS
		2) INTEL	2708	(4Kx8 EPROMs)	MOS
		3) Intel	2704	(512x8 EPROMs)	MOS
		4)	74188	(32x8 PROM)	Bipolar

The Programmer ID (Byte 177111<sub>8</sub>) will read as

- a)  $\phi 11_8$  for 2716
  - b)  $\phi 12_8$  for 2708
  - c)  $\phi 13_8$  for 2704
  - d)  $\phi 14_8$  for 74188
- if stropping plug is not installed the ID will read 000<sub>8</sub>

When the ID is  $\phi 14_8$  bit FS controls  
the 74188 program pulse time

- FS = ' $\phi$ ' normal 1ms program pulse
- FS = '1' extended 15ms program pulse

18 May 78  
AMS



Connector

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
<b>S1</b>	LS74	123	2716 Timing	2704/ 2708 Timing	74188 Timing	Logic 74188 Timing	LS 49	LS 49	LS 32	LS 32	2716 Timing	2708 Timing	2704 Timing	74188 Timing
<b>A</b>	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12	Q13	Q14
<b>B</b>	Res	LS132	LS193	LS193	LS193	LS193	LS193	LS164	LS164	LS74	LS151	LS32	10	Res
<b>C</b>		Res	LS104	LS104	7549 Res.	2714 Res	7549 7549	7549 7549	LS30	LS138	LS151	LS11	LS104	Res
<b>D</b>									<b>S3</b>					Res

- 2708/2704

74188

2716



# 100 pin Connector

top Side

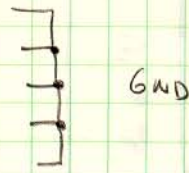
1	+25A	-	A11/13	26	MA12	-	1	
2	+25A	-		27	MA13	-	2	
3	+25B	-	A11/11	28	MA14	-	3	
4	+25B	-		29	MA15	-	4	
5	+12	-		30	GND		5	
6	+12	-		31	MD0	-	A10/12	6
7	GND	-		32	MD1	-	A10/4	7
8	GND	-		33	MD2	-	A10/15	8
9	GND	-		34	MD3	-	A10/12	9
10	GND	-		35	GND			10
11	MA0	-		36	MD4	-	A9/1	11
12	MA1	-		37	MD5	-	A9/4	12
13	MA2	-		38	MD6	-	A9/15	13
14	MA3	-		39	MD7	-	A9/12	14
15	GND	-		40	GND			15
16	MA4	-		41	MD8	-	NC	16
17	MA5	-		42	MD9	-	NC	17
18	MA6	-		43	MD10	-	NC	18
19	MA7	-		44	MD11	-	NC	19
20	GND	-		45	GND			20
21	MA8	-		46	MD12	-	NC	21
22	MA9	-	A11/1	47	MD13	-	NC	22
23	MA10	-		48	MD14	-	NC	23
24	MA11	-		49	MD15	-	NC	24
25	GND	-		50	GND			25



Boctan Side

1	25AR	-	A11/12
2	25AR	-	
3	25BR	-	A11/10
4	25BR	-	
5	-12V	-	
6	-12V	-	
7	+5V	-	
8	+5V	-	
9	+5V	-	
10	+5V	-	
11	GND	-	
12	GOH	-	A1/3
13	FIN	-	B7/14
14	FS	-	C3/12
15	F4	-	
16	GND	-	
17	F3	-	
18	F2	-	
19	F1	-	
20	F0	-	
21	GND	-	
22	ID0	-	C3/12
23	ID1	-	C13/6
24	ID2	-	C13/4
25	ID3	-	A1/4 (+5)

26	GND	-	
27	ID4	-	
28	ID5	-	
29	ID6	-	
30	ID7	-	
31	GND	-	
32	RD4	-	C6/1
33	RD5	-	C6/2
34	RD2	-	C6/3
35	RD3	-	C6/4
36	GND	-	
37	RD4	-	C6/5
38	RD5	-	C6/6
39	RD6	-	C6/7
40	RD7	-	C6/8
41	GND	-	
42	RD8	-	
43	RD9	-	
44	RD10	-	
45	RD11	-	
46	GND	-	
47	RD12	-	
48	RD13	-	
49	RD14	-	
50	RD15	-	



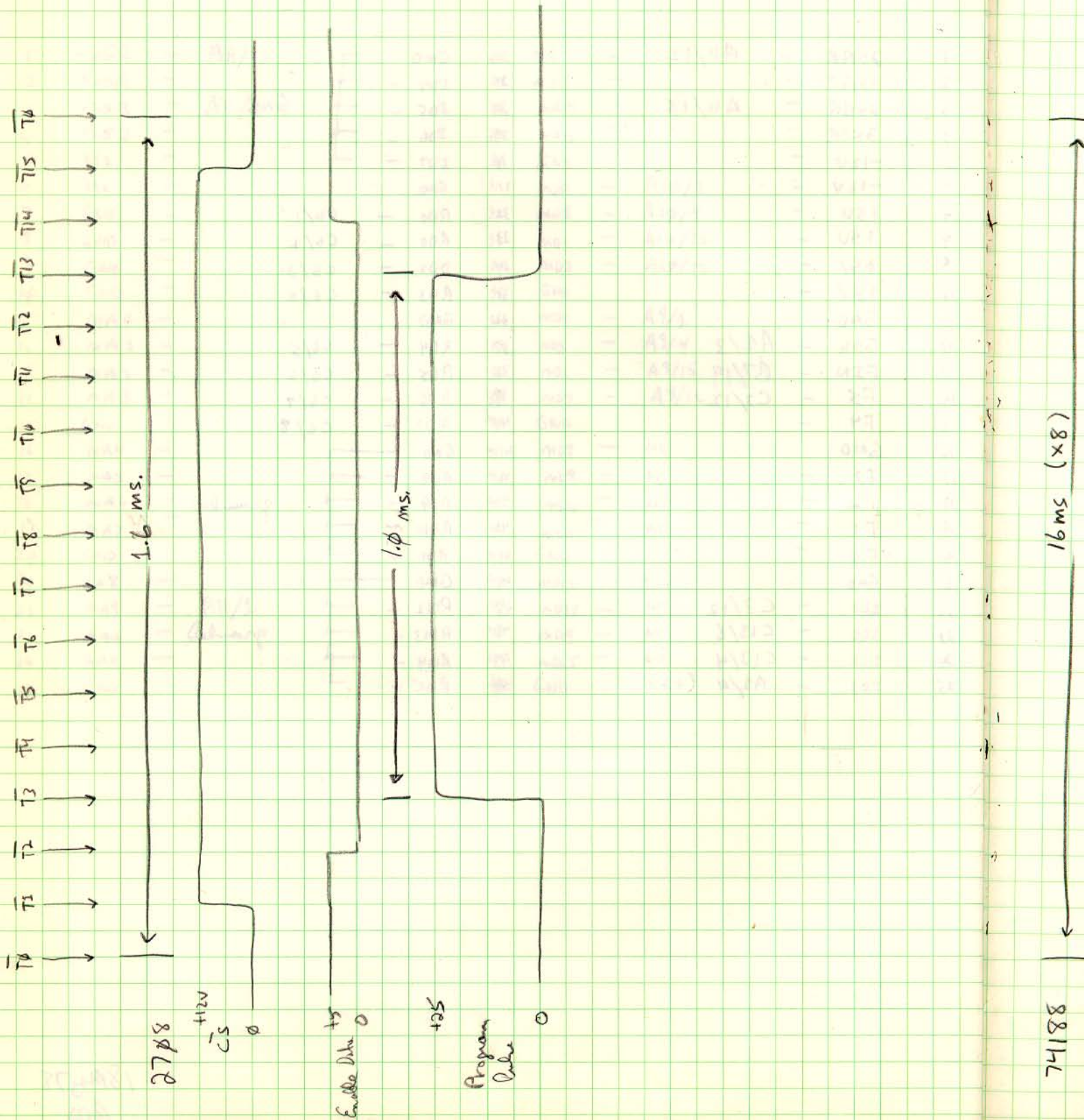
grounded

grounded

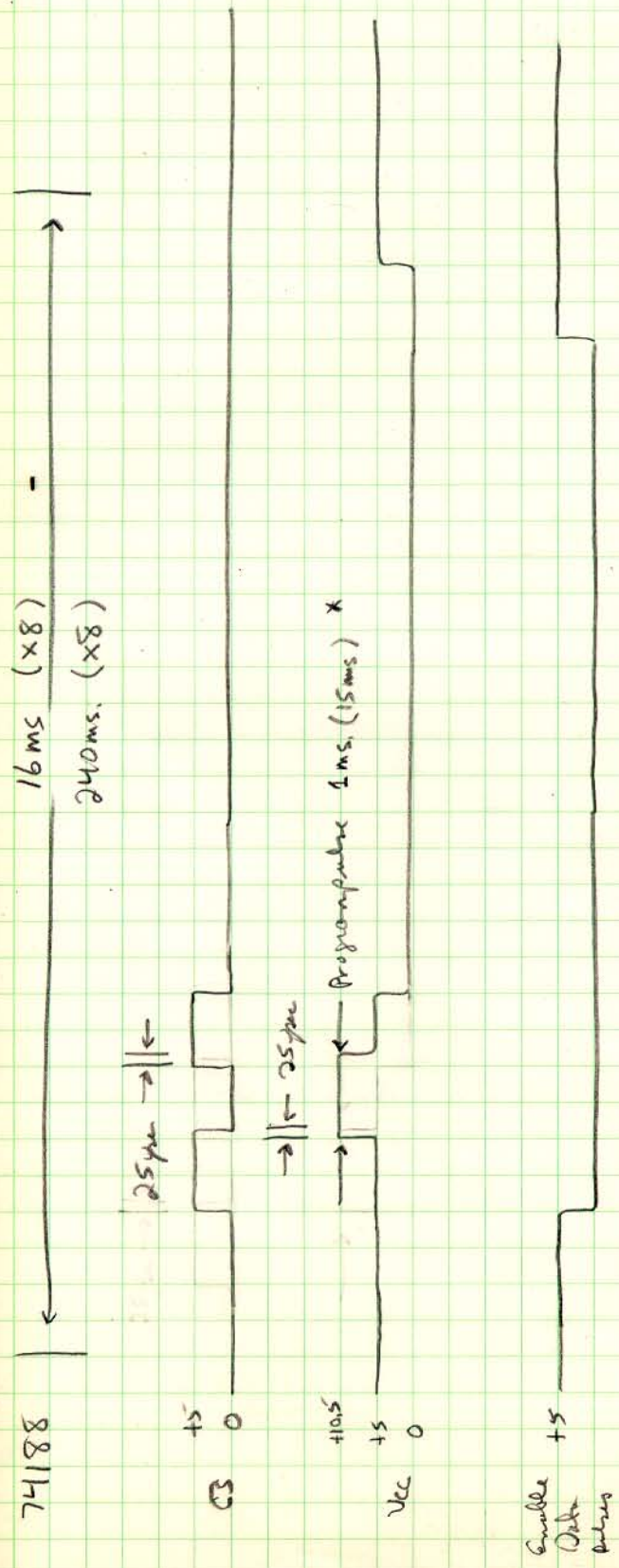
18 May 78  
Am



# Programming cycle



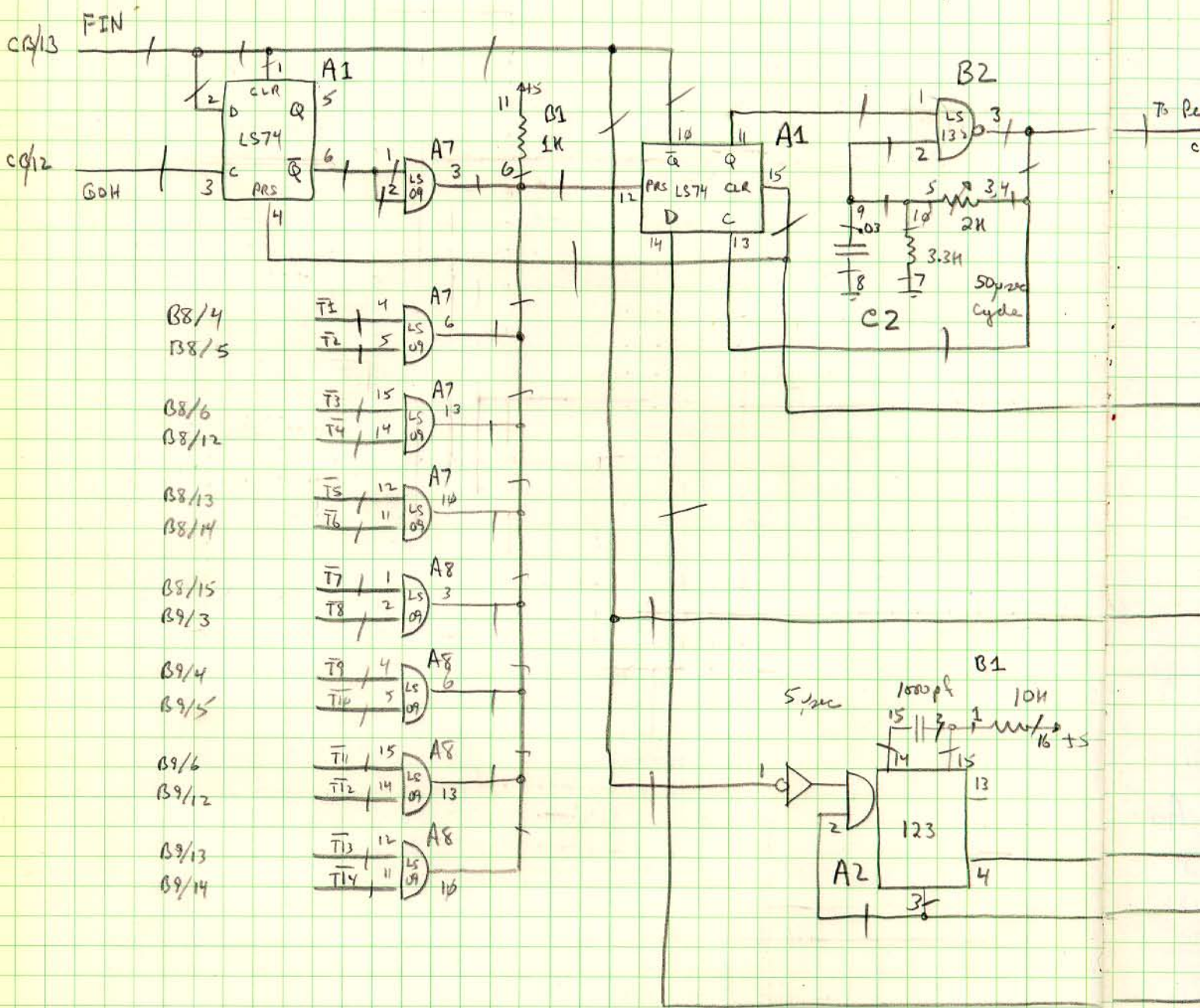




\* Program pulse applied only if bit is take programmed to a '1' and is currently a '0'



# Scan Timer



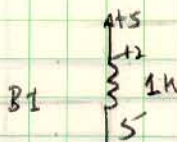


To Period Selector B5/3  
clock

05/12

B5/13

Carry  
From Period Selector  
Circuit



T1  
CB/25

4 5  
B6

LS193

14 Clear  
11 Load

13

4 5  
B7

15 A QA

1 A QB

10 C QC

9 LS193

14 Clear

11 Load

12

74188 Set L C10/5

1 2 B8

10

clock

LS164

12

13

14

15

clear

10

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

3	T0		
4	T1	A7/4	C12/5
5	T2	A7/5	C4/15
6	T3	A7/15	
12	T4	A7/14	
13	T5	A7/12	
14	T6	A7/11	
15	T7	A8/11	

1 2 B9

14

clock

LS164

12

13

14

15

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

clear

11

3	T8	A8/2	
4	T9	A8/4	
5	T10	A8/5	
6	T11	A8/15	
12	T12	A8/14	
13	T13	A8/12	C3/5
14	T14	A8/11	C4/11
15	T15		C12/5

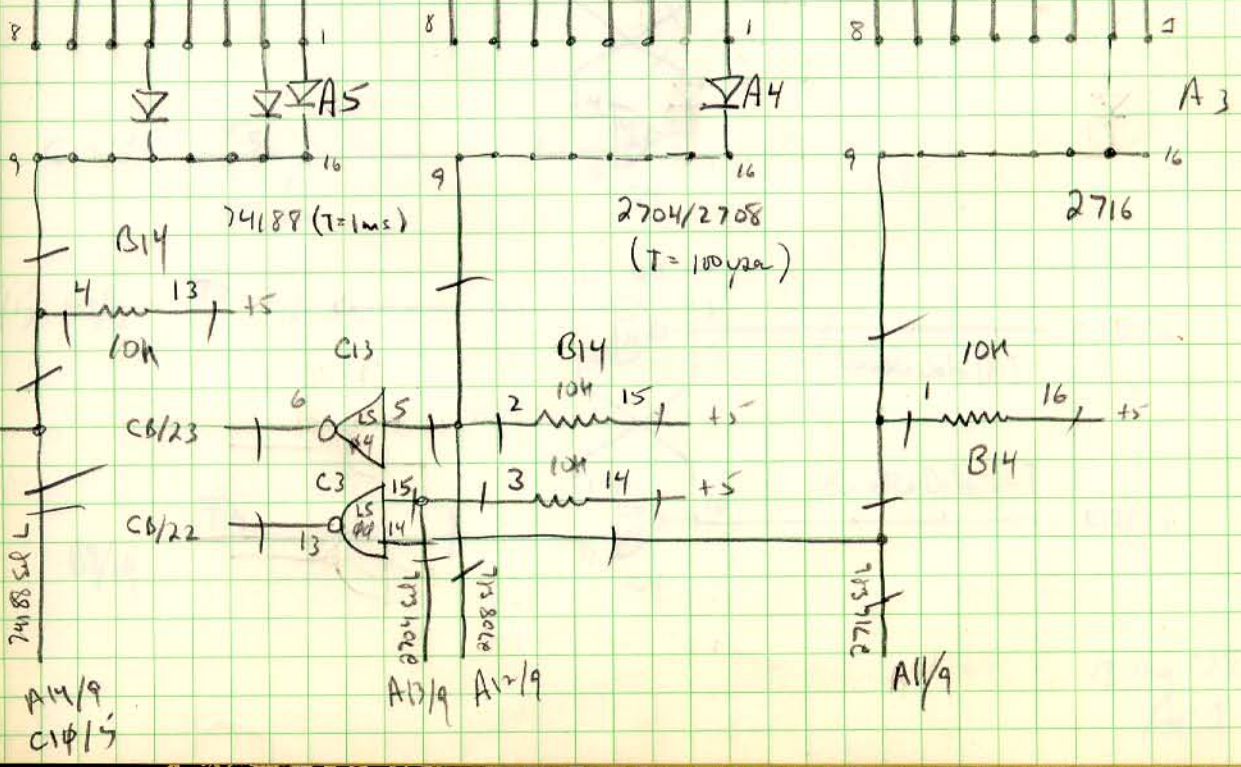
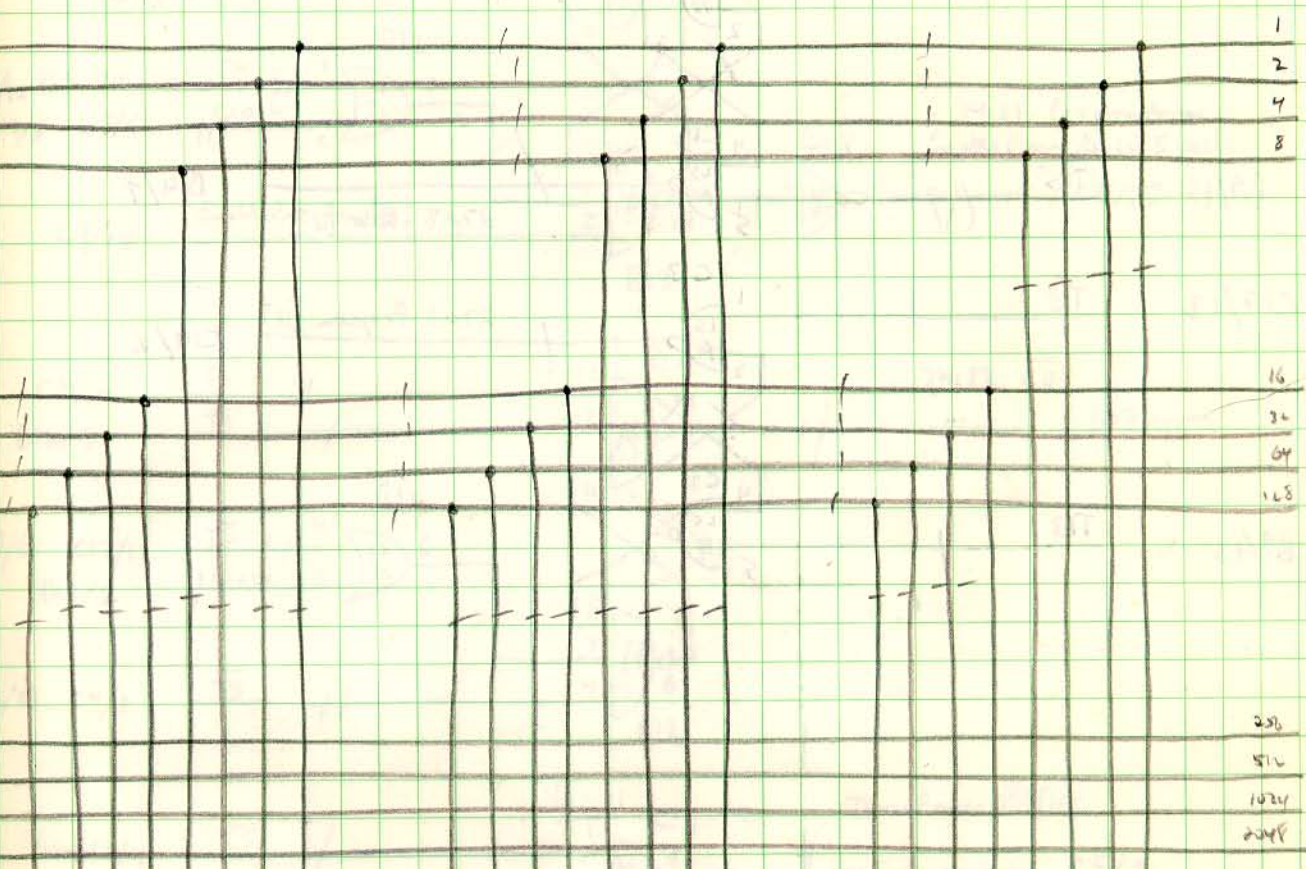
B14/11  
B11/10  
B11/9





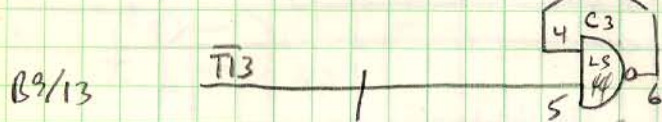
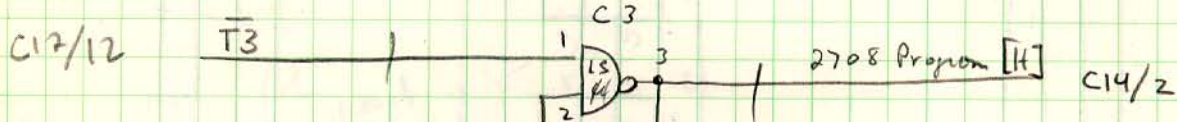
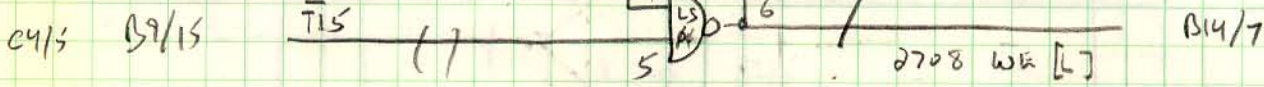
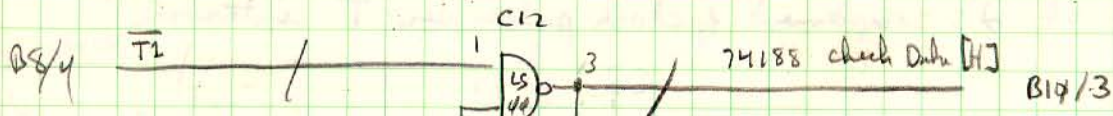


Period selected by inserting diodes for  $\phi$  bits  
of 2's complement of clock pulses per T interval





2708 Timing



C3/2

B13/10  
B12/5

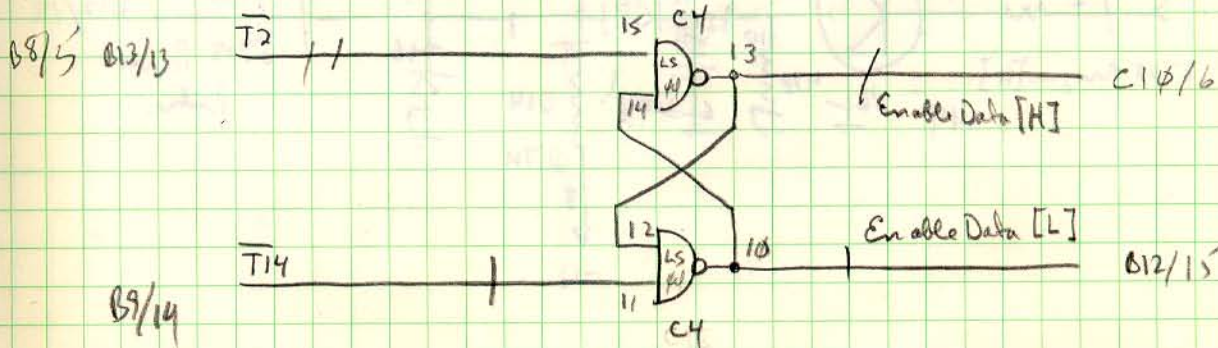
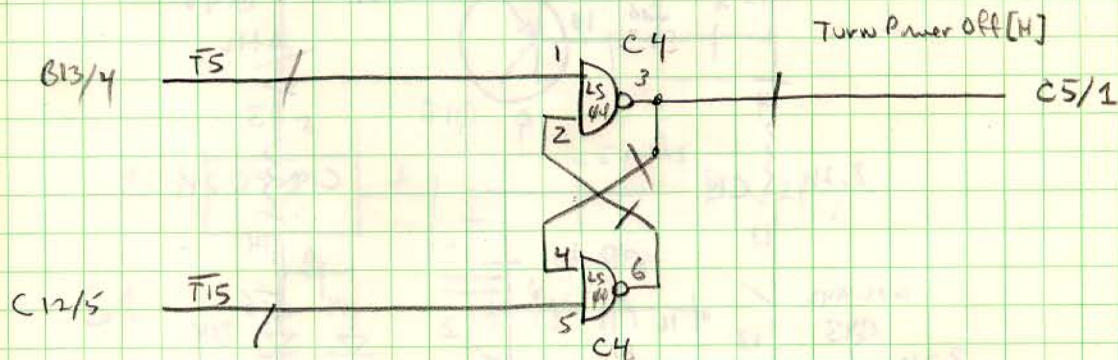
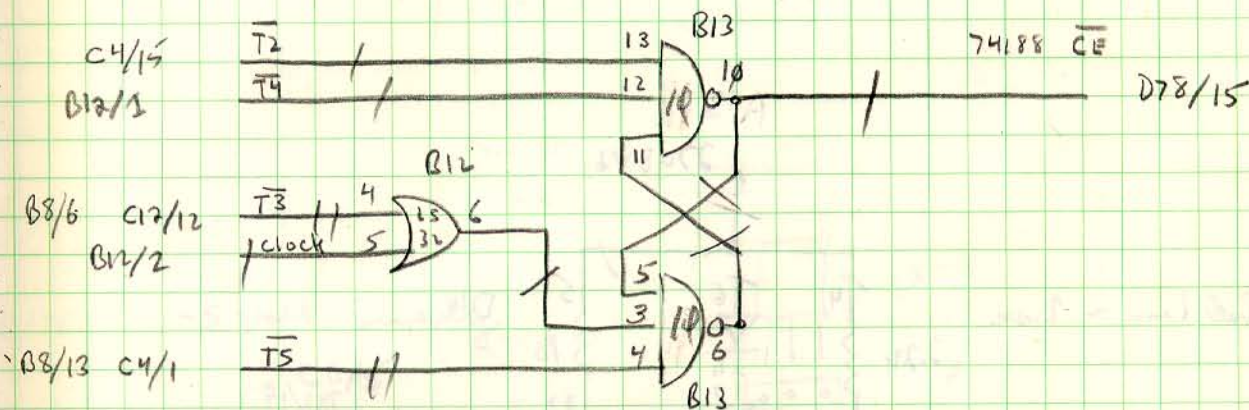
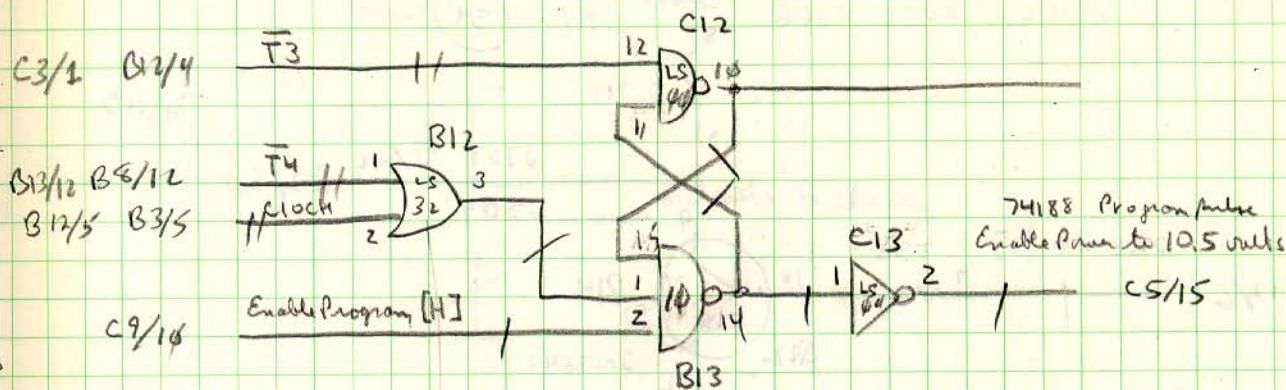
B8/6

B8/13

B8/5



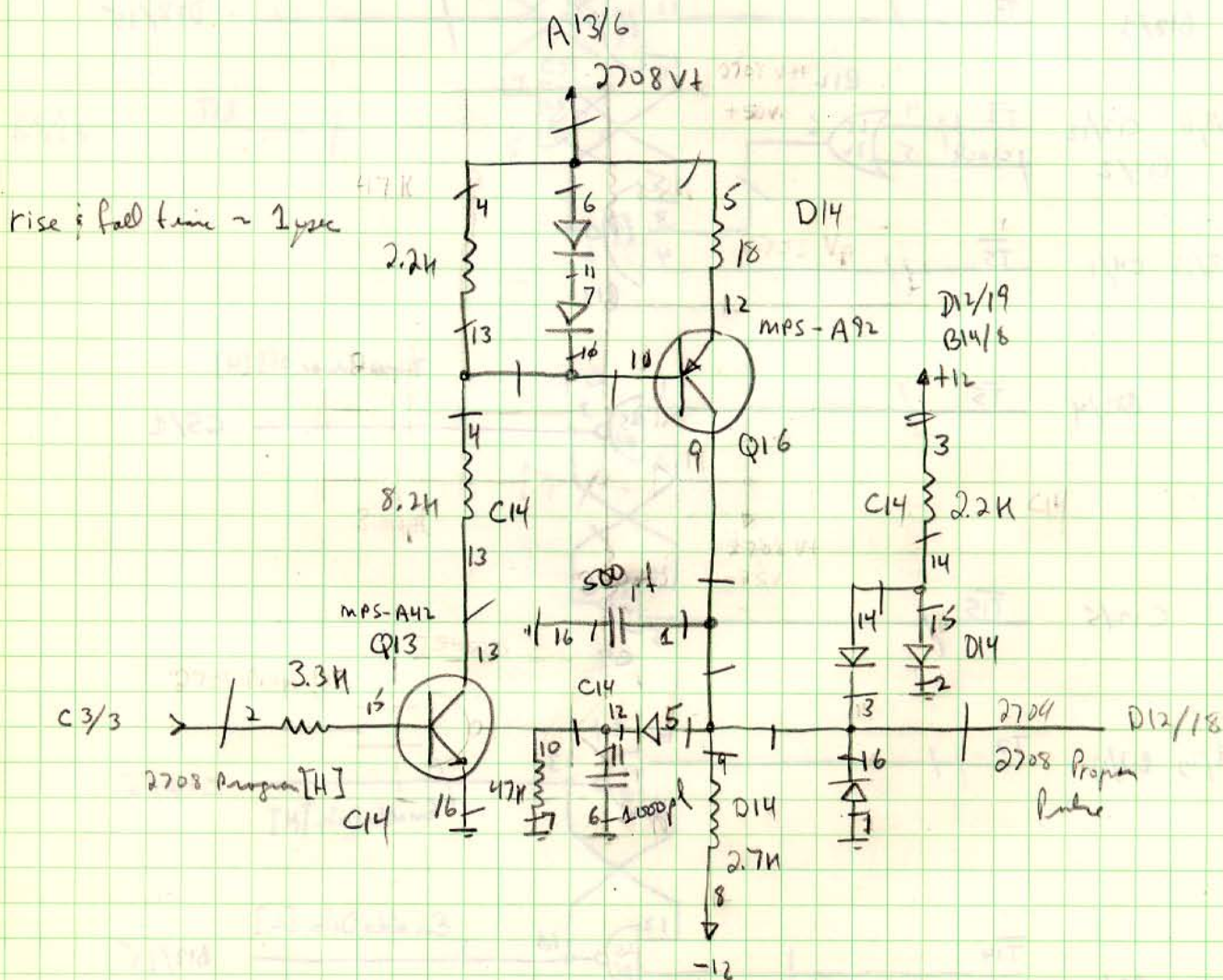
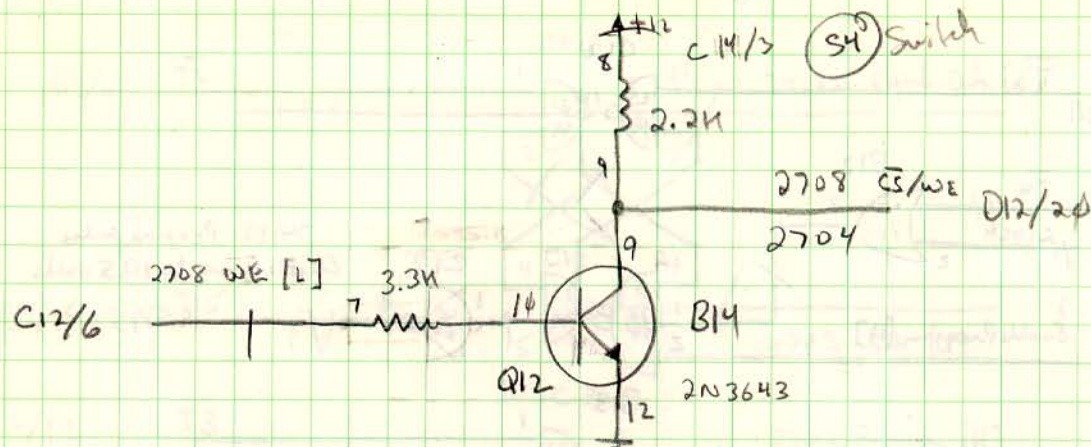
# 74188 Pulse Timing



18 May 78  
HRS

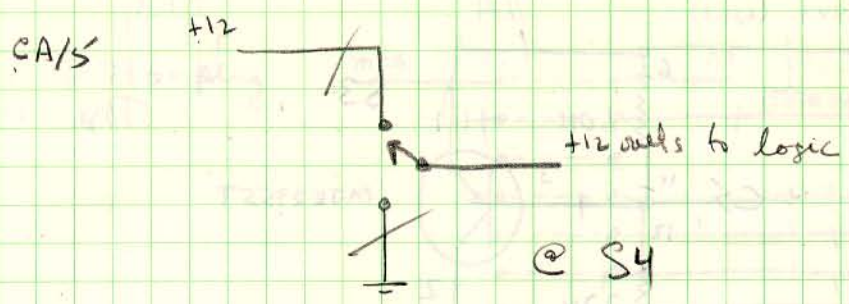


# 2708 Programming Pulse Generation

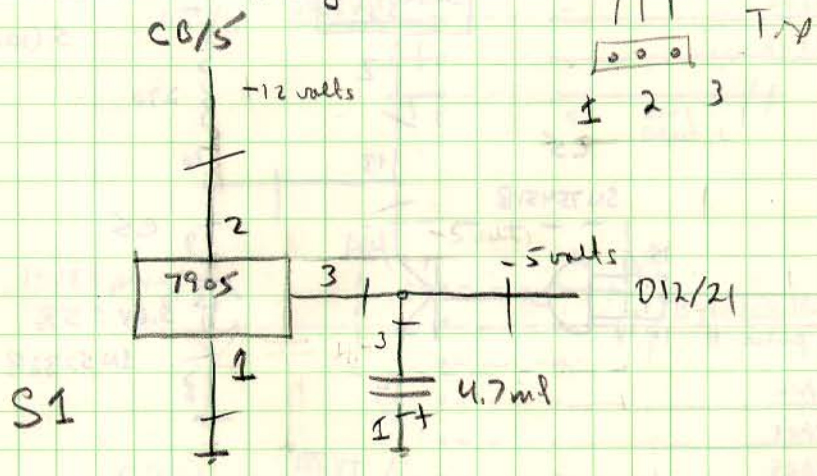




Power Switch (to turn off +12 volts while installing 2704, 2708, & 2716's)



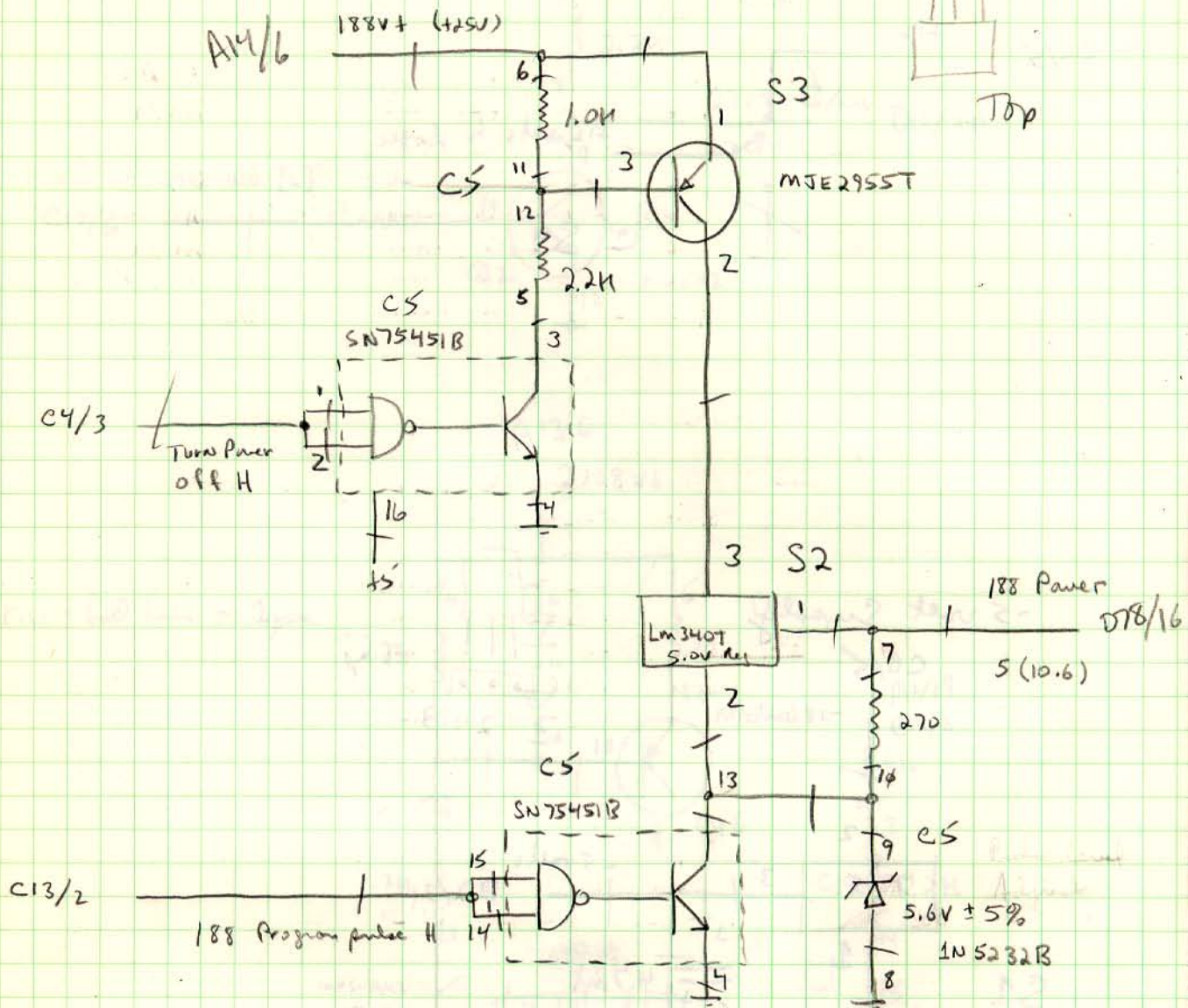
-5 volt Supply



18 May 78  
ARC



# 74188 Program Pulse generation



CA/22  
A12/

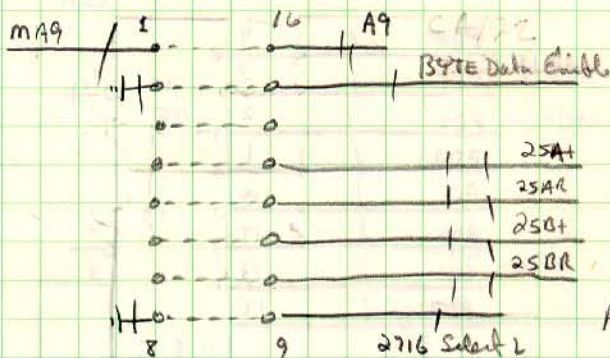
30 units  
202



# 2716, 2708, 74188 Patch Plug Wiring

## A11

CA/22 2716 plug  
A12/1



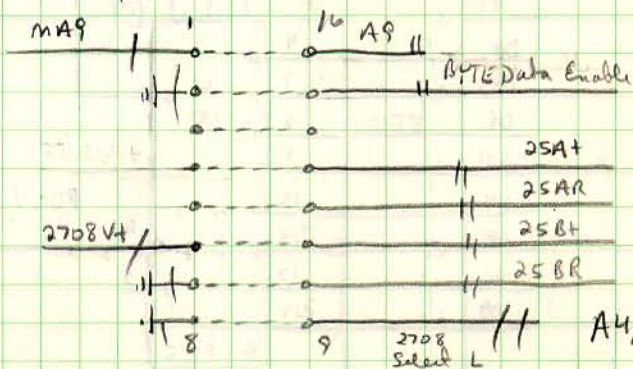
A12/16  
A12/15

A12/13 CA/1  
A12/12 CB/1  
A12/11 CA/3  
A12/10 CB/3

A3/9

## A12

2708 plug



A11/16 A13/16  
A11/15 A13/15

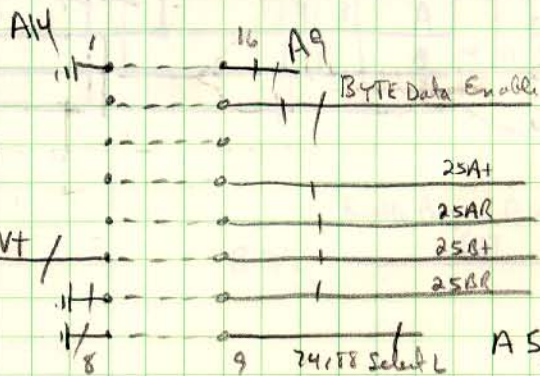
A11/13 A13/13  
A11/12 A13/12  
A11/11 A13/11  
A11/10 A13/10

A4/16 A13/14

A13/6

2708 V4

74188 plug



A13/16 D12/22  
A13/15 B14/6

A13/13  
A13/12  
A13/11  
A13/10

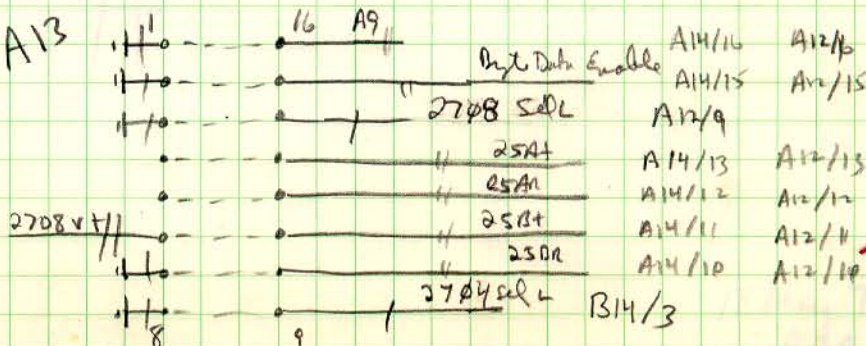
A5/16

C5/6

188 V4

## A13

2704 plug



A14/16 A12/6  
A14/15 A12/15

A12/9  
A14/13 A12/13  
A14/12 A12/12  
A14/11 A12/11  
A14/10 A12/10

B14/3

D14/4 A12/6

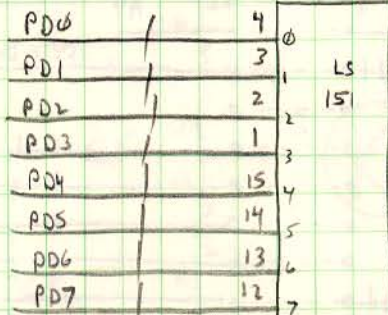
2708 V4



74188

data strobing

D12/19  
 D12/10  
 D12/11  
 D12/13  
 D12/14  
 D12/15  
 D12/16  
 D12/17



C11

A10/1  
 A10/4  
 A10/15  
 A10/12  
 A9/1  
 A9/4  
 A9/15  
 A9/12

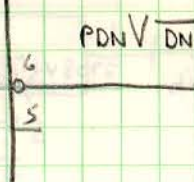
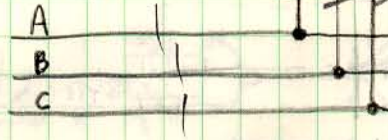


B11

PDN  $\overline{DN}$

74188 check Data  
 C12/3

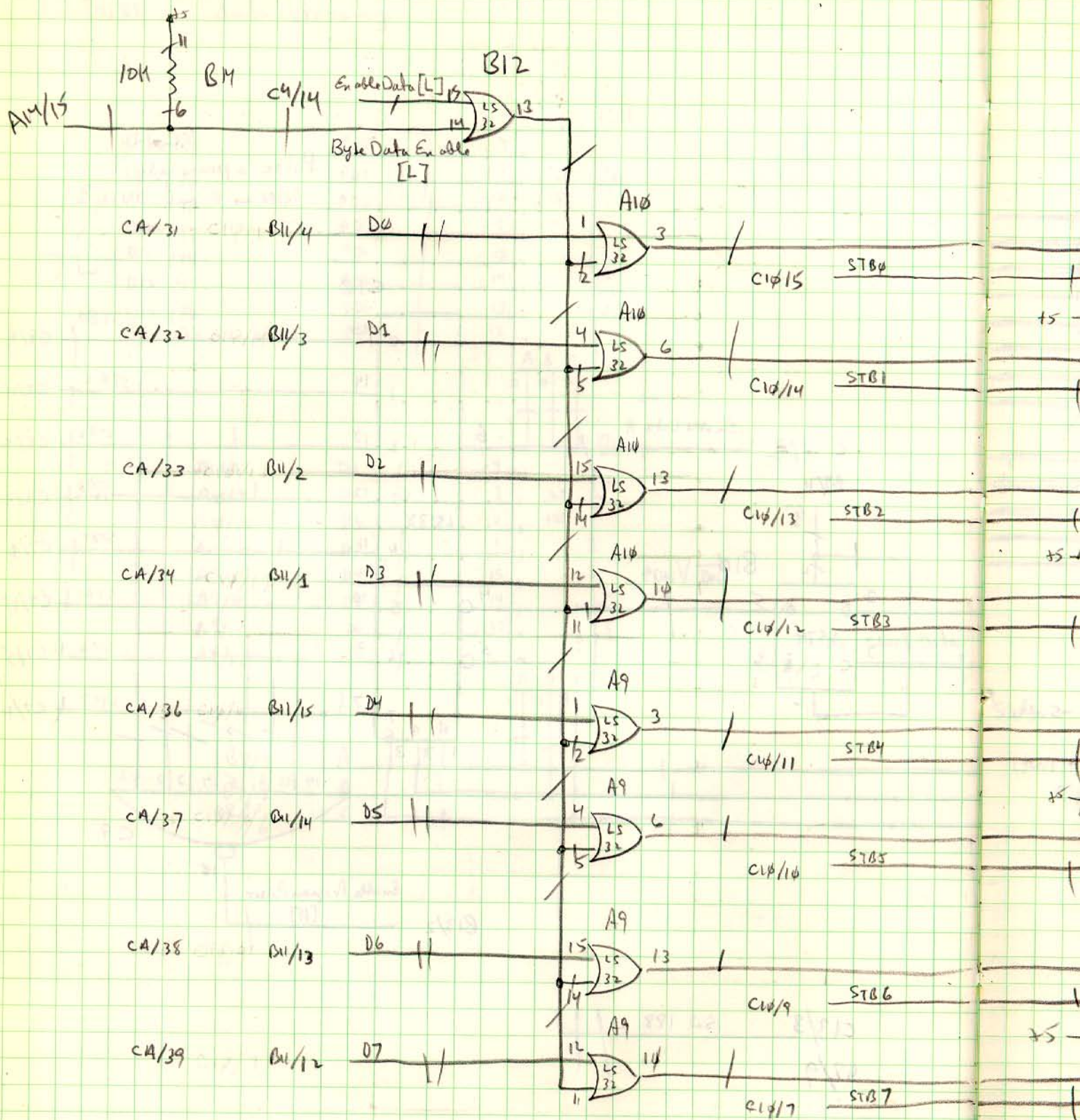
B7/3  
 B7/2  
 B7/6



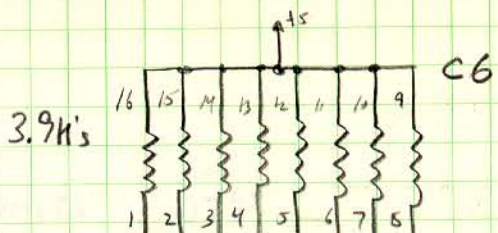




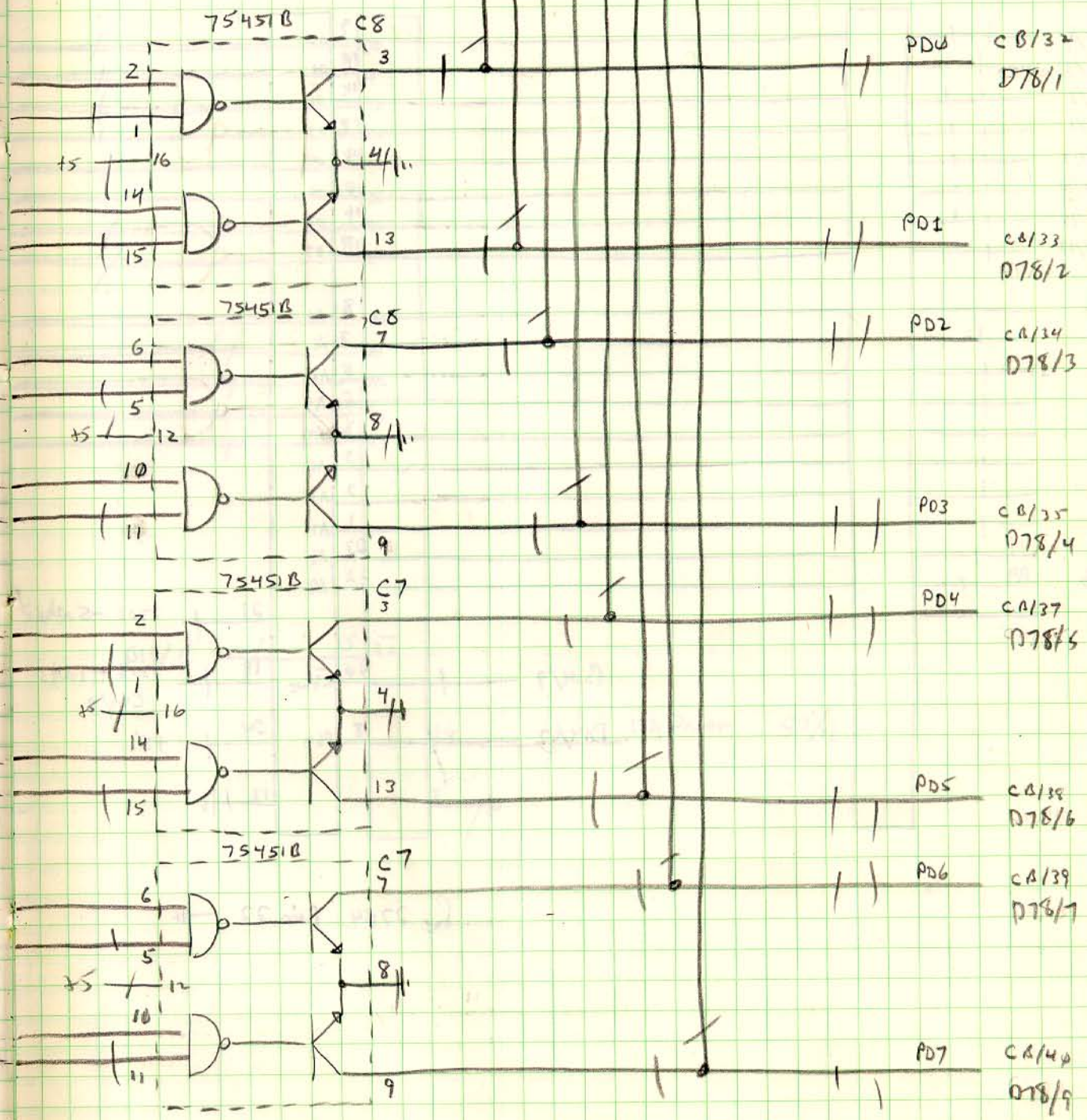








Data to Memory

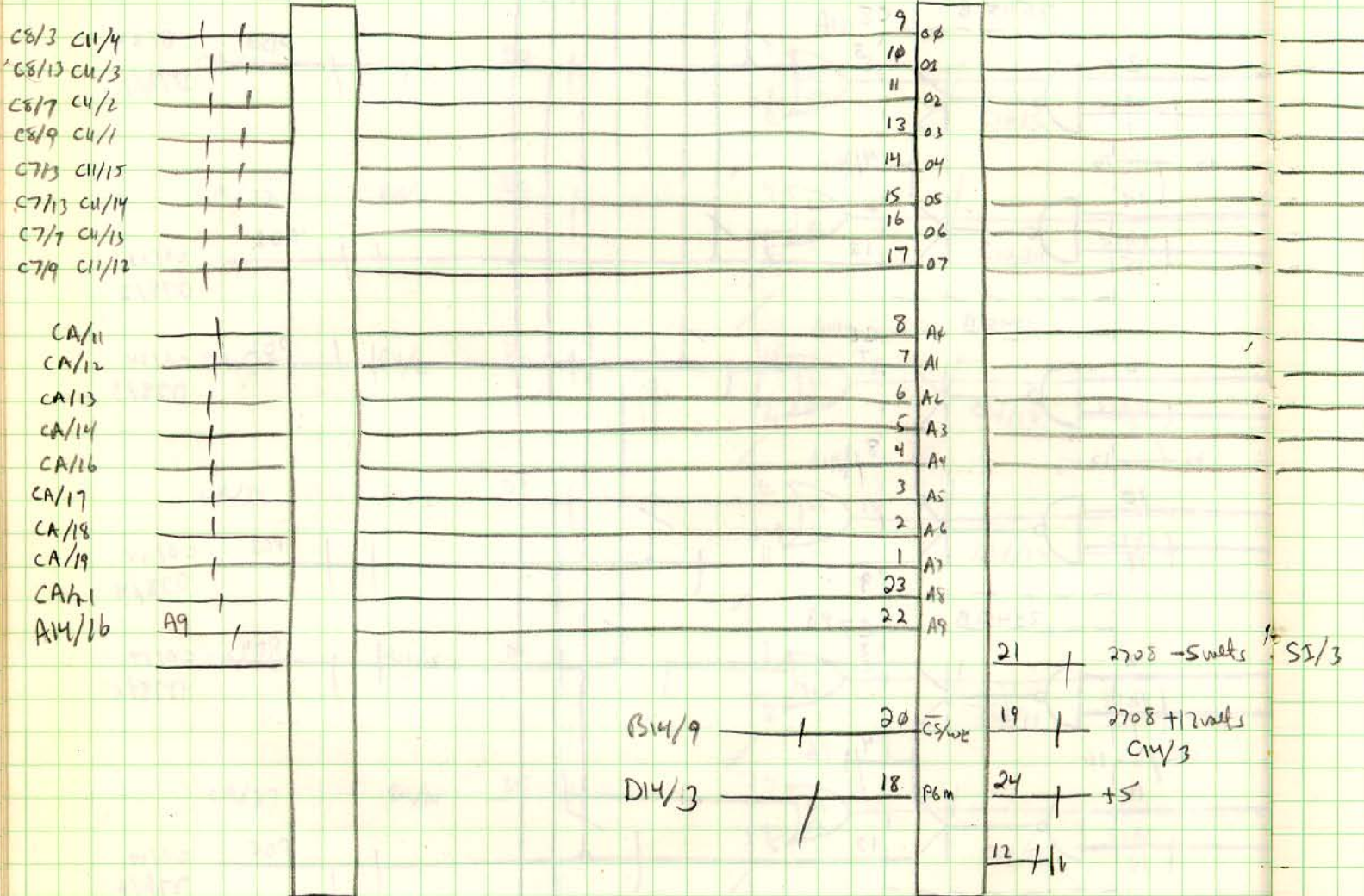


18 May 78  
ARS



D34  
(TMS) 2716

D12  
2708/2704

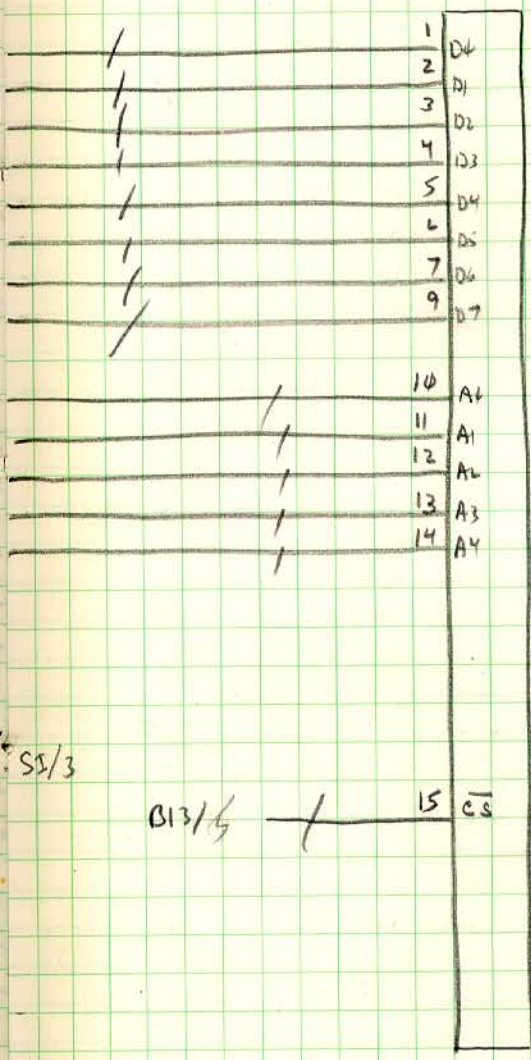


For 2704 Pin 22 - 11



74188

078



SS/3

B13/4

188 Power 92/1



# Circuit Locations

A1	LS74	41
A2	123	41, 42
A3	diodes	42
A4	diodes	42
A5	diodes	42
A6	diodes	42
A7	LS49	41
A8	LS49	41
A9	LS32	47
A10	LS32	47
A11	plug	45
A12	plug	45
A13	plug	45
A14	plug	45
B1	Res	41, 42
B2	LS132	41
B3	LS193	42
B4	LS193	42
B5	LS193	42
B6	LS193	41
B7	LS193	41
B8	LS164	41
B9	LS164	41
B10	LS74	46
B11	LS151	46
B12	LS32	43, 47
B13	1φ	43
B14	RES	42, 44, 47



C1	--	
C2	RES	41
C3	LS00	42, 43
C4	LS00	43
C5	75451/R60	45
C6	R60	47
C7	75451/75451	47
C8	75451/75451	47
C9	LS30	46
C10	LS138	46
C11	LS151	46
C12	LS44	43
C13	LS04	43
C14	RES	42, 44

D34	2716 EProm Socket	48
D78	74188 Prom Socket	48
D12	2704/2708 EProm Socket	48

D1	--	
D14	RES	44

31 May 78  
ARD



S1	LM 7905	44
S2	LM 7805	45
S3	MJE 2955T	45
S4	Switch	44

Q1	—	
Q2	—	
Q3	—	
Q4	—	
Q5	—	
Q6	—	
Q7	—	
Q8	—	
Q9	—	
Q10	—	
Q11	—	
Q12	2N3643	44
Q13	MPSA42	44
Q14	—	
Q15	—	
Q16	MPS-A92	44

Construction Complete 31 May 78  
(except for 2716 wiring)

31 May 78  
AD



# PRAM Card

52

Designed as a Pprom chip substitute during program debugging.

The board may be used to emulate the following chip types and (# of chips)

				nodes
6834	512 x 8	EPROM	8 chips	$\pm 5 - 12$
2704	512 x 8	EPROM	8 chips	$\pm 5 - 12$
2708	1024 x 8	EPROM	4 chips	$\pm 5 - 12$
TMS 2716	2048 x 8	EPROM	2 chips	$\pm 5 - 12$
2716/TMS 2516	2048 x 8	EPROM	2 chips	$\pm 5$
2732	4096 x 8	EPROM	1 chip	$\pm 5$

A 4K x 8 250 ns RAM System is decoded in the above organizations

BOARD ID# is 2008 (Byte 1771118)

19 June 1979  
ARD



Comment

PRAM CARD

LOAD  RUN

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	7474	74123	RES	RES	7415 132	8795	8795	<del>7415</del> 139	7415 139	X	8795	8795	8795	8795	8795	202
B	2102 L2N															
C																2102 L2N
D	1702		6834	2704 2708 2758 2716 TMS 2532	TMS 2716	TMS 2716	TMS 2716			8797 ADD	8797 ADD	8797 DATA	8797 DATA	X	74118	CS BLOCK

1

3

4

6

7

9

10

11

12

13

14

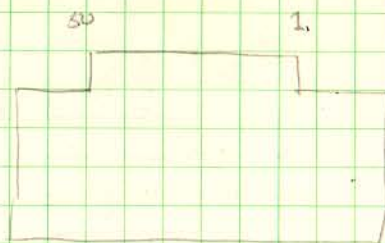
15

16



# 100 pin Connector

top Side CT (Right to left)



1	+25A	-		26	MA12	-	
2	+25A	-		27	MA13	-	
3	+25B	-		28	MA14	-	
4	+25B	-		29	MA15	-	
5	+12	-		30	GND	-	
6	+12	-		31	MD0	+	B1/11
7	GND	-		32	MD1	+	B2/11
8	GND	-		33	MD2	+	B3/11
9	GND	-		34	MD3	+	B4/11
10	GND	-		35	GND	-	
11	MA0	+	A6/4	36	MD4	+	B5/11
12	MA1	+	A6/4	37	MD5	+	B6/11
13	MA2	+	A6/6	38	MD6	+	B7/11
14	MA3	+	A6/10	39	MD7	+	B8/11
15	GND	-		40	GND	-	
16	MA4	+	A6/12	41	MD8	-	
17	MA5	+	A6/14	42	MD9	-	
18	MA6	+	A7/2	43	MD10	-	
19	MA7	+	A7/4	44	MD11	-	
20	GND	-		45	GND	-	
21	MA8	+	A7/6	46	MD12	-	
22	MA9	+	A7/10	47	MD13	-	
23	MA10	+	A7/12	48	MD14	-	
24	MA11	+	A7/14	49	MD15	-	
25	GND	-		50	GND	-	

1	2
2	2
3	2
4	2
5	-
6	-
7	+
8	+
9	+
10	+
11	G
12	G
13	F
14	F
15	F
16	G
17	F
18	F
19	F
20	F
21	G
22	F
23	F
24	F
25	F



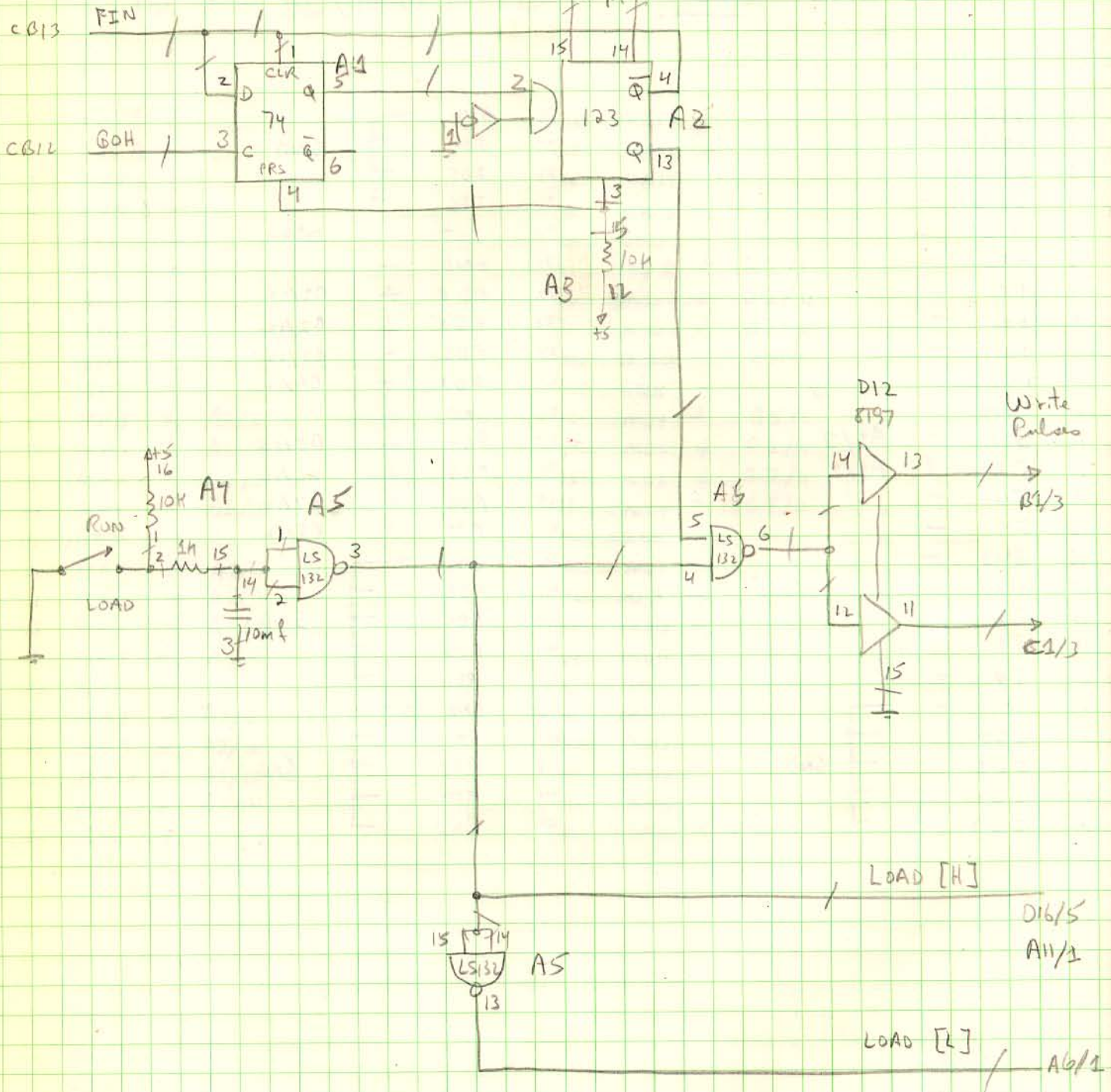
Bottom Side CB

1	25AR	-		26	GND		
2	25AR	-		27	ID4		GND
3	25OR	-		28	IDS		
4	25OR	-		29	ID6		
5	-12	-		30	ID7		open
6	-12	-		31	GND	-	
7	+5	-		32	RD0	+	B1/12
8	+5	-		33	RD1	+	B2/12
9	+5	-		34	RD2	+	B3/12
10	+5	-		35	RD3	+	B4/12
11	GND	-		36	GND	-	
12	GOH	+	A1/3	37	RD4	+	B5/12
13	FIN	+	A1/1	38	RD5	+	B6/12
14	FS	-		39	RD6	+	B7/12
15	F4	-		40	RD7	+	B8/12
16	GND	-		41	GND		
17	F3	-		42	RD8		GND
18	F2	-		43	RD9		
19	F1	-		44	RD10		
20	F0	-		45	RD11		
21	GND	-		46	GND		
22	ID0		GND	47	RD12		GND
23	ID1						
24	ID2						
25	ID3						
				48	RD13		
				49	RD14		
				50	RD15		

19 June 1979  
ARD



# Write Control





# Memory Socket Wiring

2704

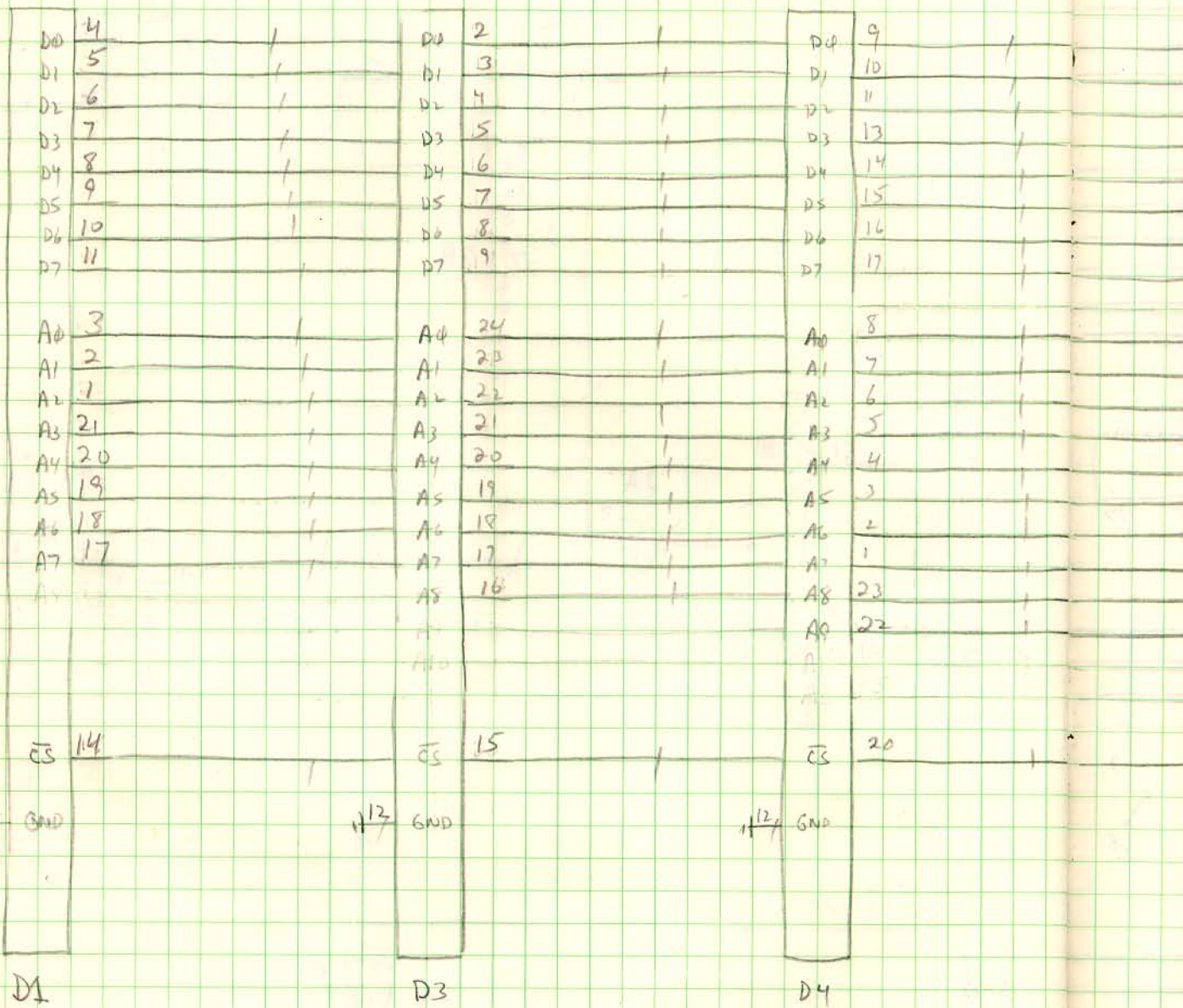
2708

2758

1702

6834

7108





Tms 2716

DATE 27/6

2532  
secretary

56

9	D0	9		9	D0	/	D12/3
10	D1	10		14	D1	/	D12/5
11	D2	11		11	D2	/	D12/7
13	D3	13		13	D3	/	D12/9
14	D4	14		14	D4	/	D13/3
15	D5	15		15	D5	/	D13/5
16	D6	16		16	D6	/	D13/7
17	D7	17		17	D7	/	D13/9
8	A0	8	A0	8	A0	/ CA0	D10/2
7	A1	7	A1	7	A1	/ CA1	D10/4
6	A2	6	A2	6	A2	/ CA2	D10/6
5	A3	5	A3	5	A3	/ CA3	D10/10
4	A4	4	A4	4	A4	/ CA4	D10/12
3	A5	3	A5	3	A5	/ CA5	D10/14
2	A6	2	A6	2	A6	/ CA6	D11/2
1	A7	1	A7	1	A7	/ CA7	D11/4
23	A8	23	A8	23	A8	/ CA8	D11/2
22	A9	22	A9	22	A9	/ CA9	D11/4
20	A10	19	A10	19	A10	/ CA10	D11/6
19	A11	18	A11	18	A11	/ CA11	D11/10
18	CS	18		20		/ CS0	D16/9
12	CS						

D6

D7

D9

Wines

23 Aug 79

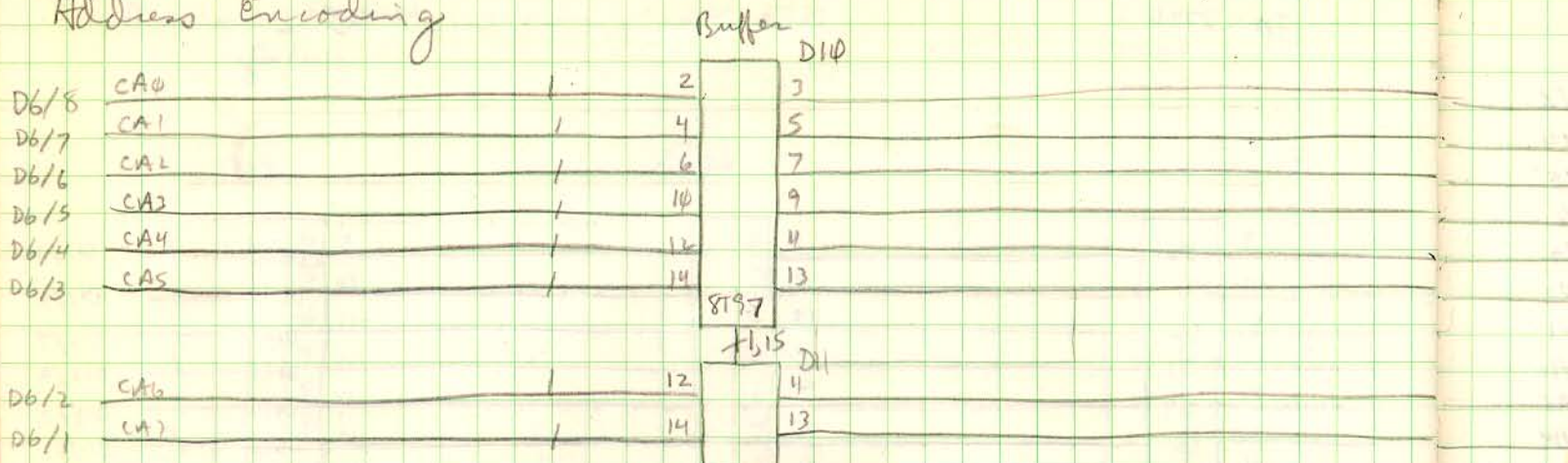
AS

19 June 79

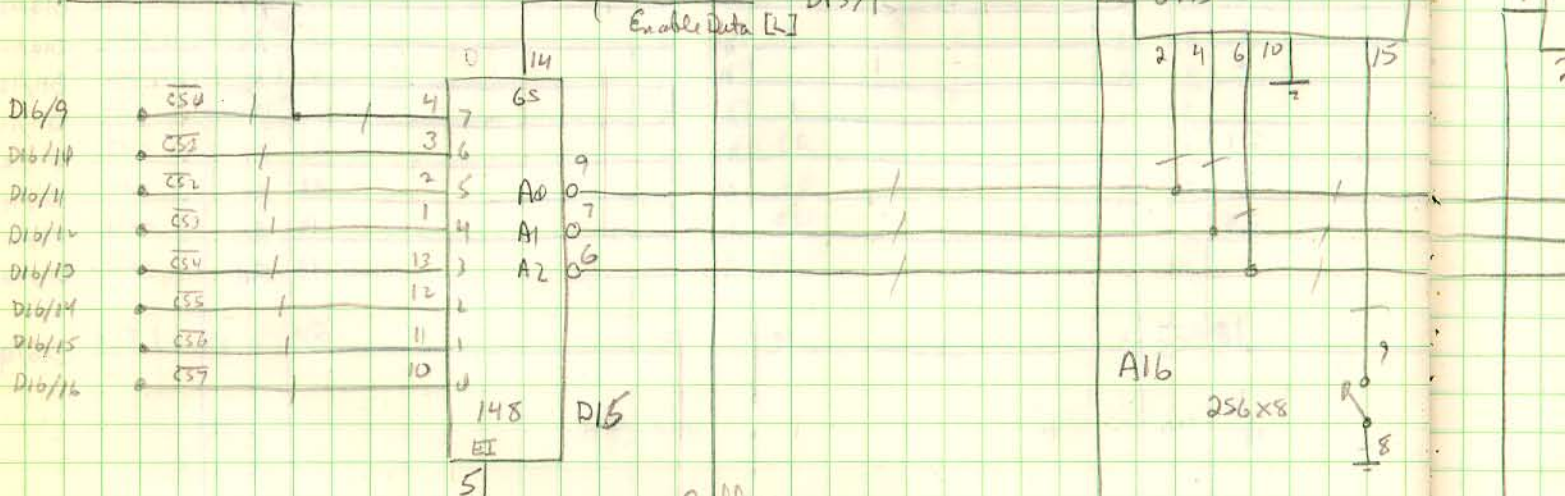
ASD



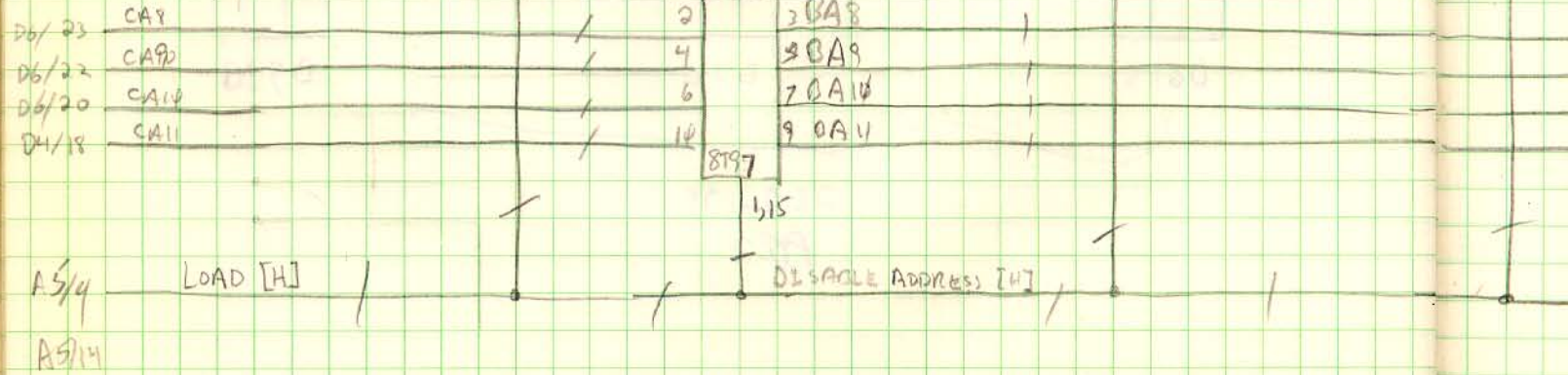
# Address Encoding



DB/18 CS0



AB/4

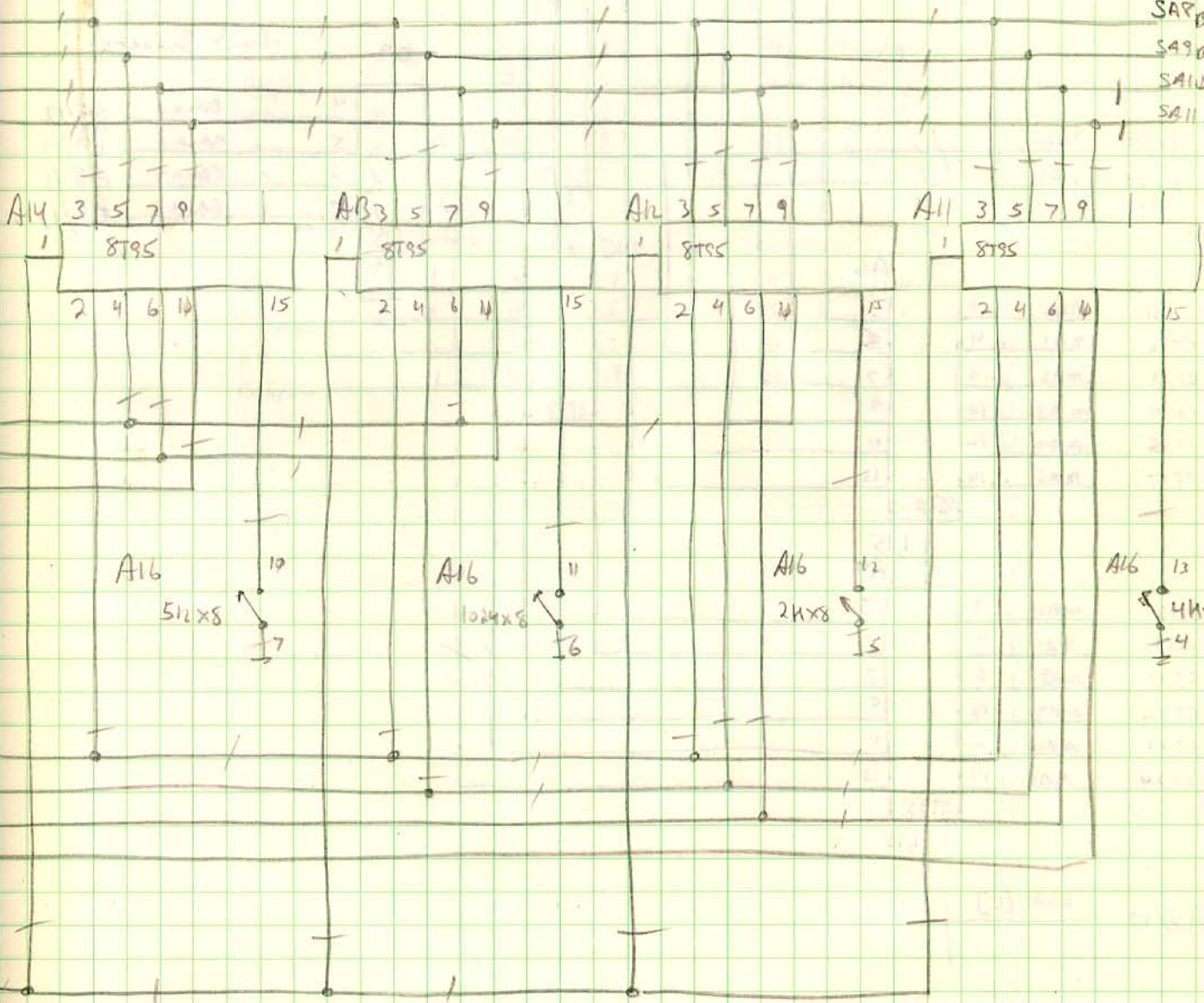




- SA0 C10/8
- SA1 C10/4
- SA2 C10/5
- SA3 C10/6
- SA4 C10/7
- SA5 C10/2

- SA6 C10/1
- SA7 C10/16

- SA8 A15/15
- SA9 A11/14
- SA10 A9/12
- SA11 A9/3

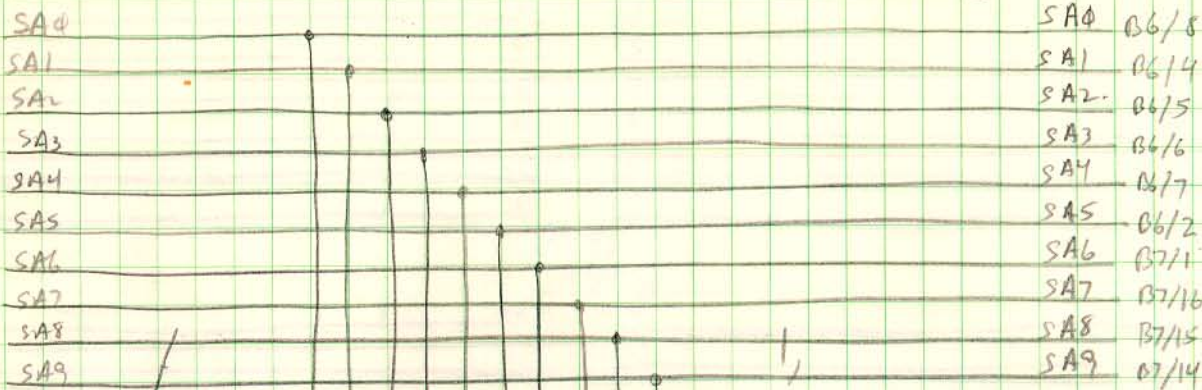


19 June 79  
ARR



# Address Multiplexed

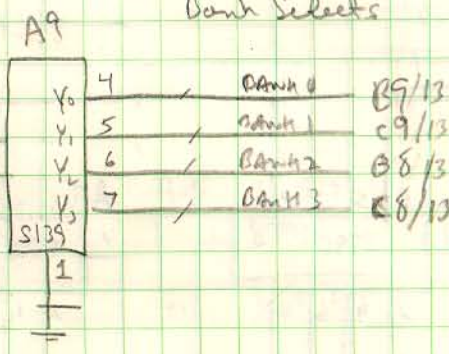
# Address Drive Lines



A11/7  
A11/9

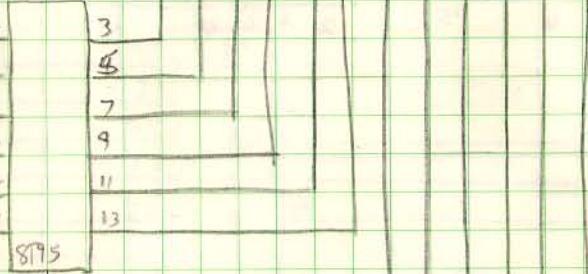
SA10  
SA11

## Bank Selects



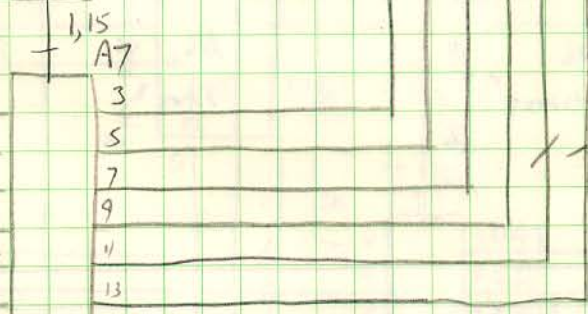
CT11	MA0	2
CT12	MA1	4
CT13	MA2	6
CT14	MA3	10
CT16	MA4	12
CT17	MA5	14

A6



CT18	MA6	2
CT19	MA7	4
CT21	MA8	6
CT22	MA9	10
CT23	MA10	12
CT24	MA11	14

A7



A5/13

LOAD[L]

S139





# Data Buffers

## Data from Memory

## Data to External System

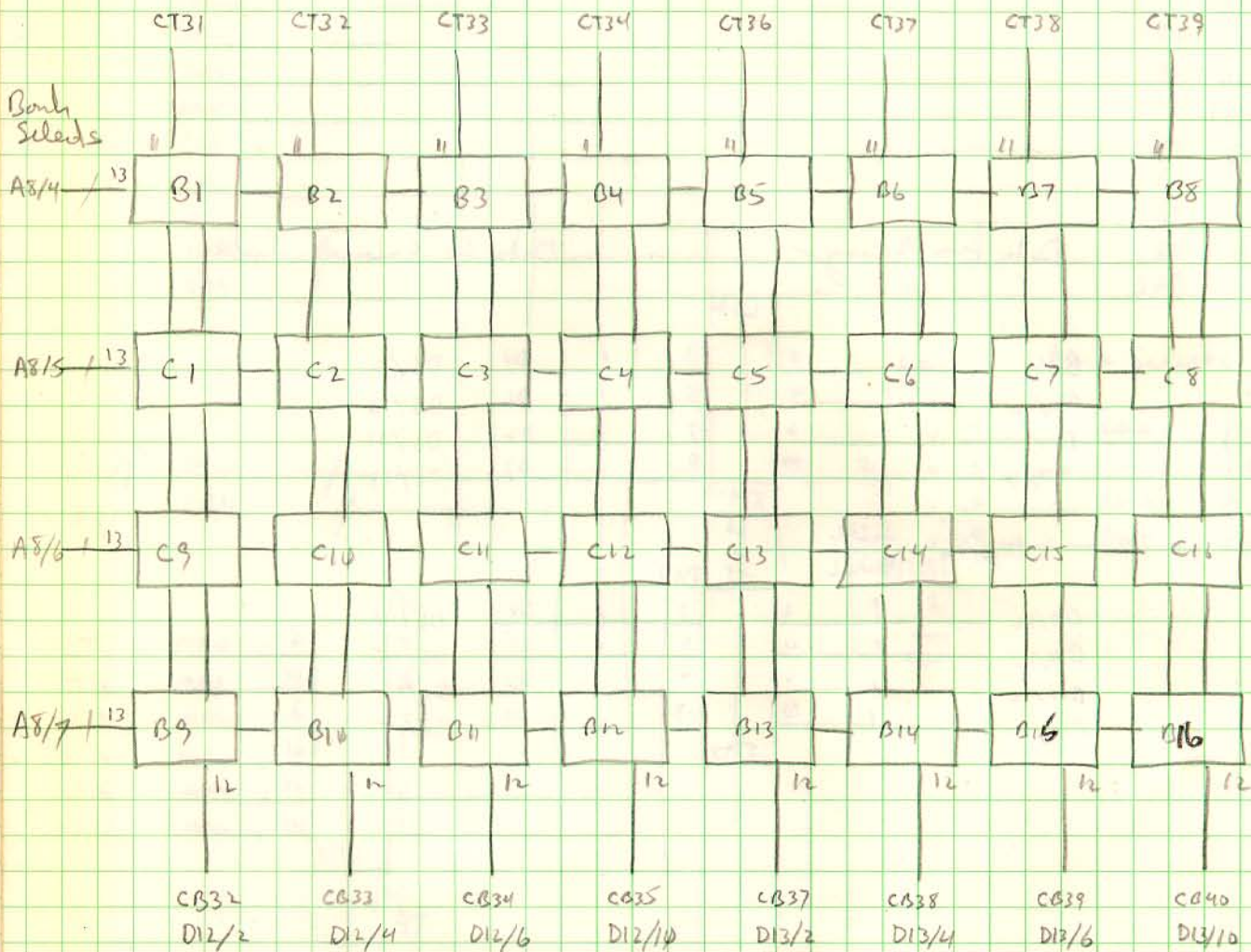
		D12					
B9/12	1	2	3	1	D4	D6/9	
B10/12	1	4	5	1	D1	D6/10	
B11/12	1	6	7	1	D2	D6/11	
B12/12	1	10	9	1	D3	D6/13	
			8197				
			1				
D15/14	Enable	1	1				
	Data L	1	1				
		D13					
D13/12	1	2	3	1	D4	D6/14	
B14/12	1	4	5	1	D5	D6/15	
B15/12	1	6	7	1	D6	D6/16	
B16/12	1	10	9	1	D7	D6/17	
			8197				

19 Jun 79  
AOD



# Memory Organization (all 250 ns 2102 1Kx1 RAMs)

DATA IN



Data out line



# Circuit Locations

A1	7474	55
A2	74123	55
A3	RES	55
A4	RES	55
A5	7413132	55
A6	8T95	58
A7	8T95	58
A8		
A9	745139	58
A10		
A11	8T95	57
A12	8T95	57
A13	8T95	57
A14	8T95	57
A15	8T95	57
A16	Switches	57

B1 - B16 e, C1 - C16      2102A2LN      59

D1	[1702]	56
D3	[6838]	56
D4	[2704, 2708, 2758, 2716, Tms 2532]	56
D6	[Tms 2516]	56
D7	—	56
D9	—	56

D10	8T97	57	
D11	8T97	57	
D12	8T97	55	58
D13	8T97		58
D14	x		
D15	74148		57
D16	CS Clock inputs		57



Finished on 20 June 1979 - checked on AR011 -

20 June 79  
AR0



# National Generic PROM Program

this card will program all National Semiconductor  
PROM's in the following series of devices

32 x 8	DM 74S188 / S288	16 pin
256 x 4	DM 74S287 / S387	16 pin
512 x 4	DM 74S570 / S571	16 pin
1024 x 4	DM 74S572 / S573	18 pin
512 x 8	DM 74S472 / S473	20 pin
512 x 8	DM 74S474 / S475	24 pin

ID = 208

@177111



Connector

Pin  
1 1 1 1

1	LS74	RES
2	LS09	LS132
3	LS09	LS193
4	LS 164	LS193
5	LS 164	LS193
6	10	X
7	LS00	X
8	LS151	07
9	LS138	RES
10	X	TRANS
11	X	RES
12	X	TRANS
13	X	RES
14	RES	07

A

B

16		32x8
16	X	256x4
16	X	512x4
16	X	1024x4
20		512x8
20	X	512x8
24		512x8
24	X	512x8

C

S188/S288

S287/S387

S570/S571

S572/S573

S472/S473

S474/S475







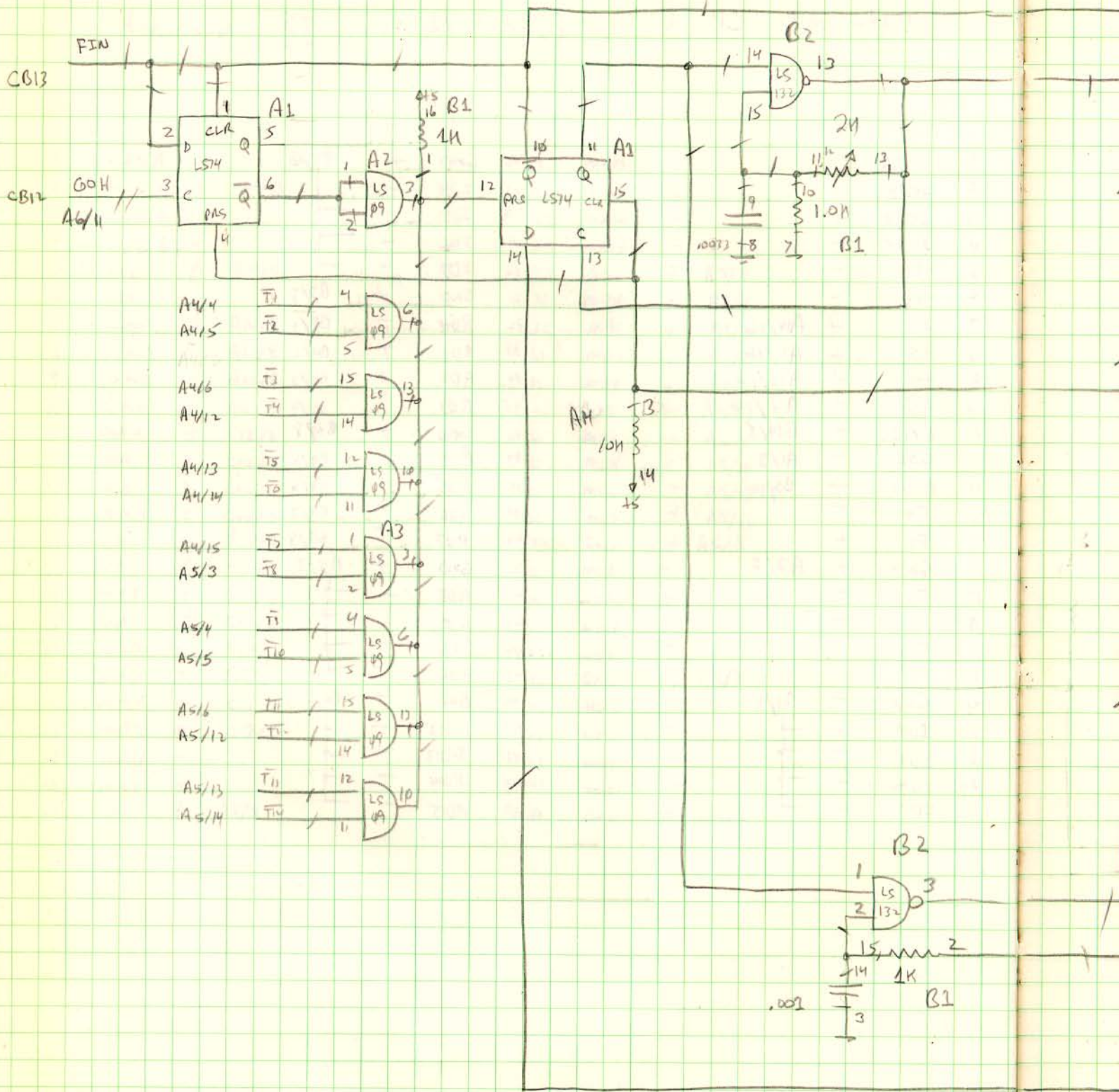
## Bottom side CB

1	25AR	-			
2	25AR	-			
3	25BR	-			
4	25BR	-			
5	-12	-			
6	-12	-			
7	+5	+	A14/16		
8	+5	+	A13/16		
9	+5	+	A12/16		
10	+5	+	A11/16		
11	GND	+	B14/8		
12	GND	-	A1/3		
13	FIN	+	B5/14		
14	F5	-			
15	F4	-			
16	GND	+	A2/8		
17	F3	-			
18	F2	-			
19	F1	-			
20	F0	-			
21	GND	+	A1/8		
22	ID0	-			
23	ID1	-			
24	ID2	-			
25	ID3	-			
26	GND	+		B8/8	
27	ID4	-			open
28	ID5	-			
29	ID6	-			
30	ID7	-			
31	GND	+		B7/8	
32	RD4	-		B11/1	
33	RD1	-		B11/2	
34	RD2	+		B11/3	
35	RD3	+		B11/4	
36	GND	+		B6/8	
37	RD4	-		B11/5	
38	RD5	-		B11/6	
39	RD6	+		B11/7	
40	RD7	-		B11/8	
41	GND	+		B5/8	
42	RD8	-			
43	RD9	-			
44	RD10	-			
45	RD4	-			
46	GND	+		B4/8	
47	RD12	-			
48	RD13	-			
49	RD14	-			
50	RD15	-			

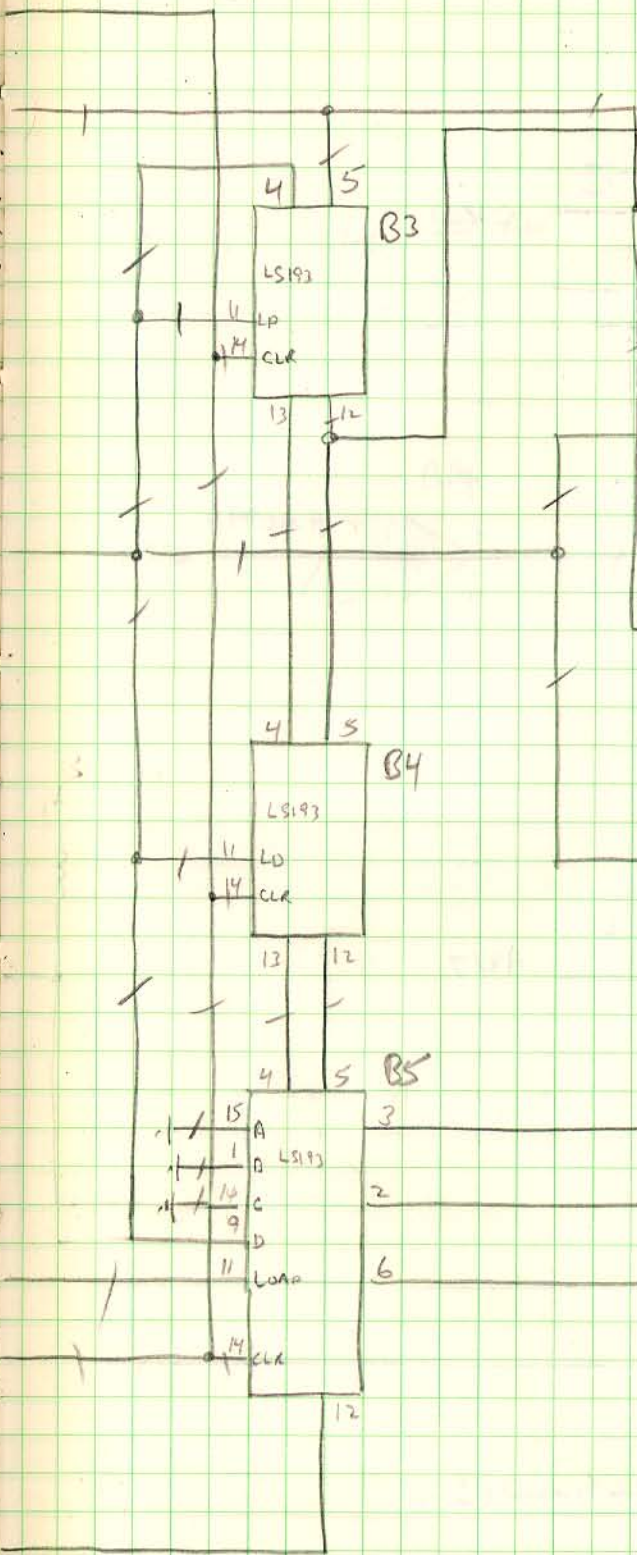
2 May 80  
A00



# Scan Timer







Timing

Pin	Label	Timing	Address	Address
10	CH		A2/4	A6/3
11	CLR		A2/15	A6/2
12			A2/15	A7/1
13			A2/14	A6/4
14			A2/14	A6/12
15			A3/1	A7/2

Pin	Label	Timing	Address
10	CH		A3/2
11	CLR		A3/4
12			A3/5
13			A3/15
14			A3/14
15			A3/12

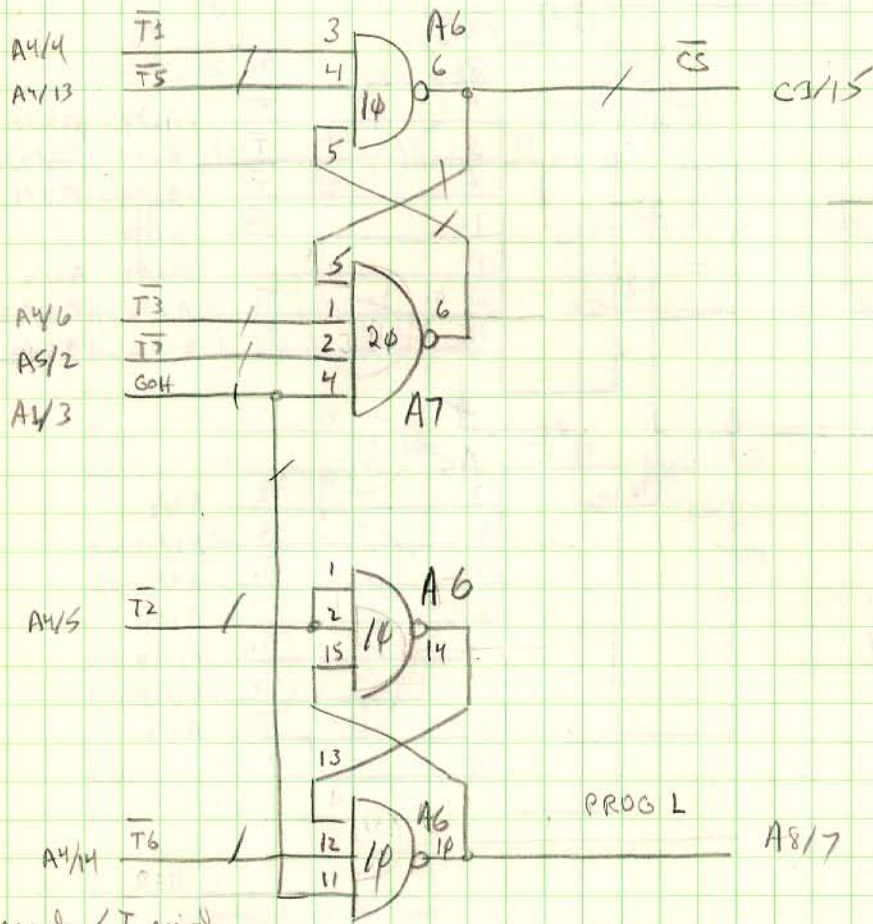
Bit select

Pin	Label	Address
3	A	A8/11
2	B	A8/14
6	C	A8/9

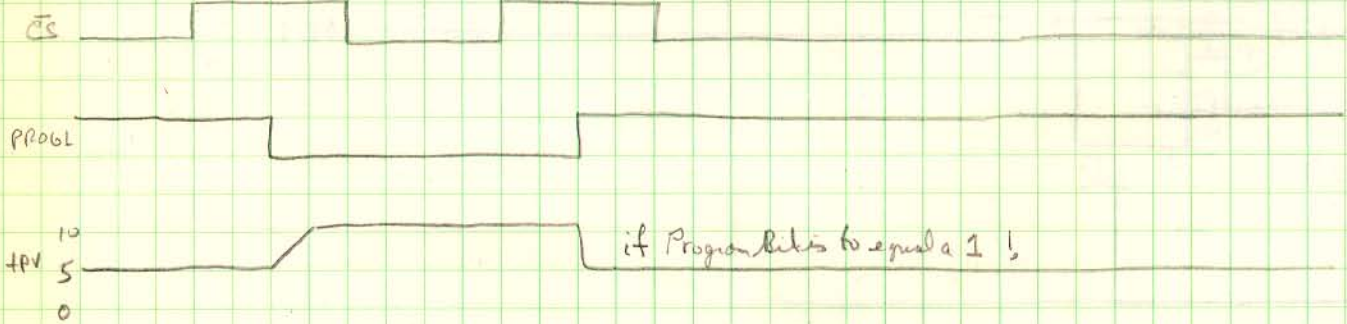
2 May 80  
ARD



# Pulse Timing Generators



5 microseconds / T period

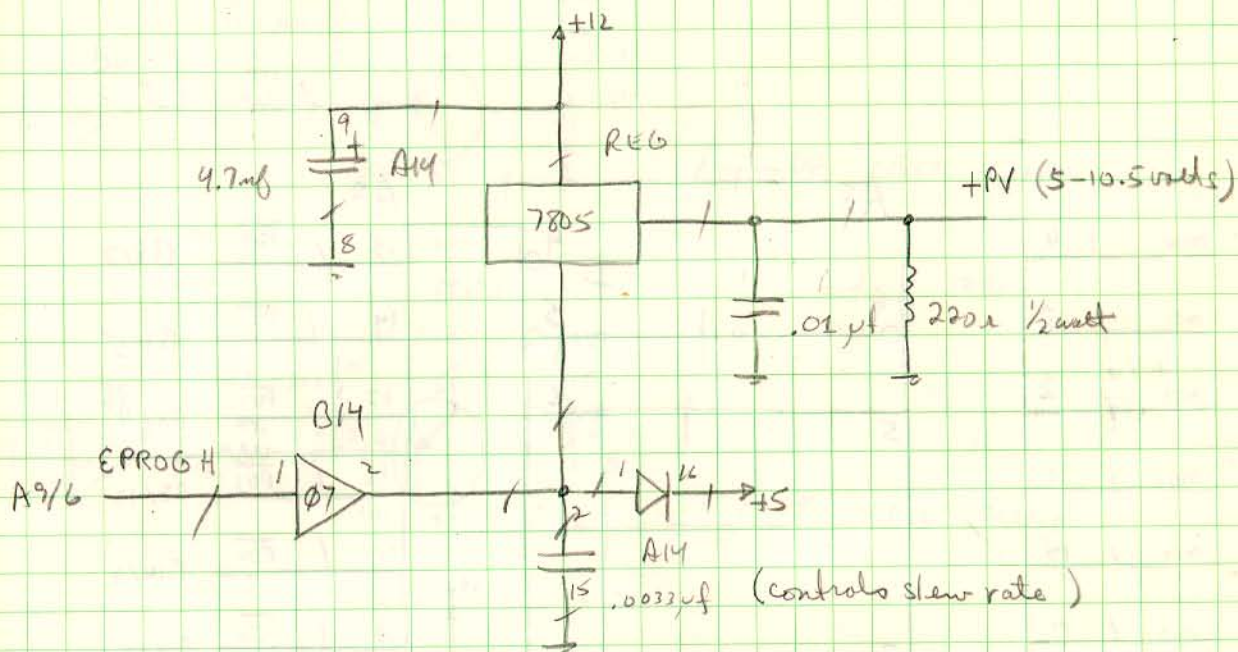


repeats cycle 16. times on each Bit position



# Programming Voltage Generator

65



2 May 80  
ARD

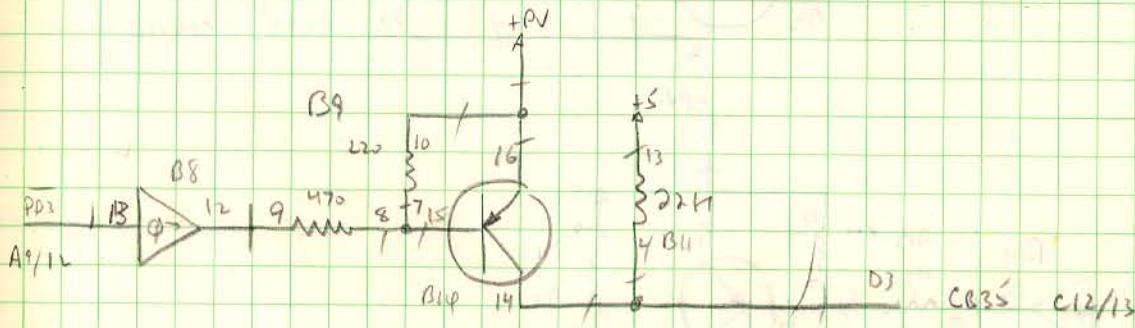
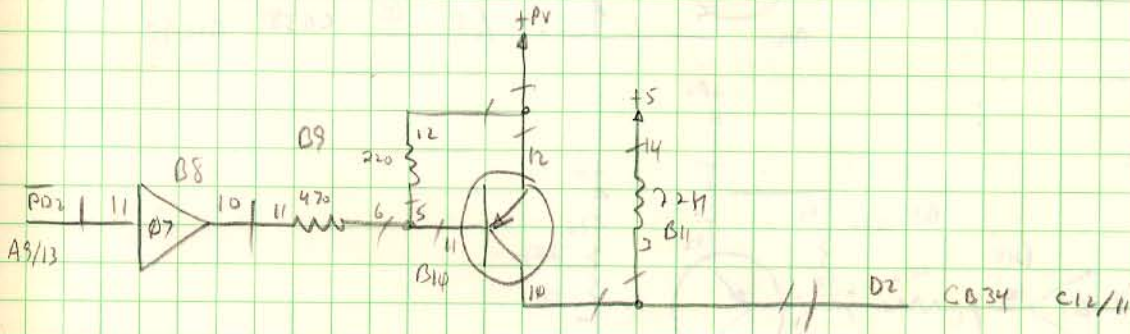
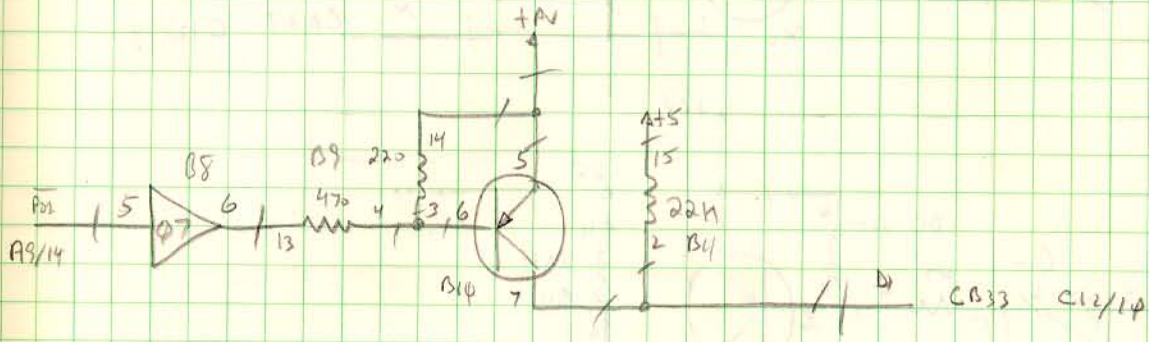
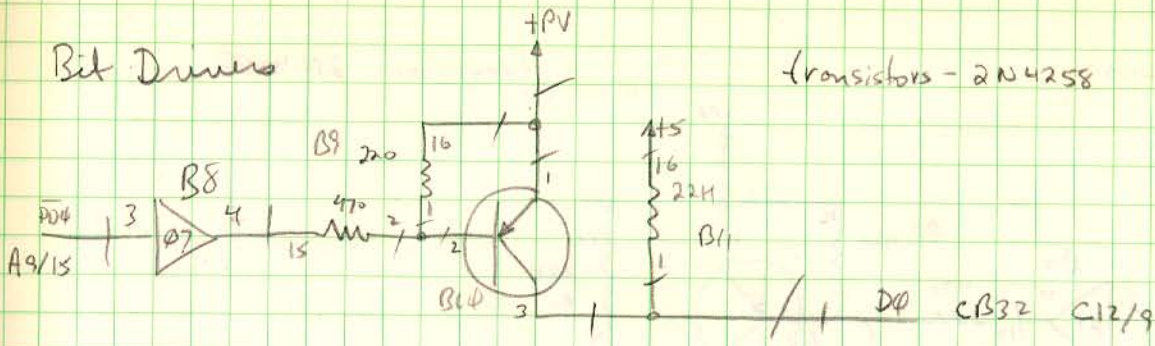






# Bit Drivers

Transistors - 2N4258

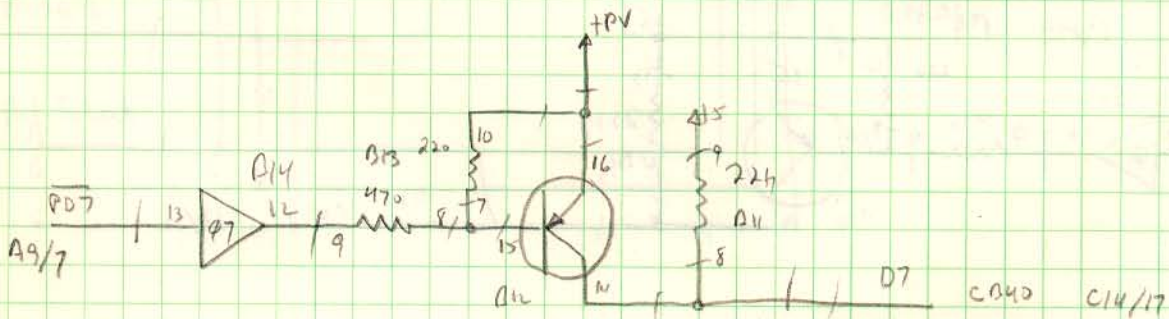
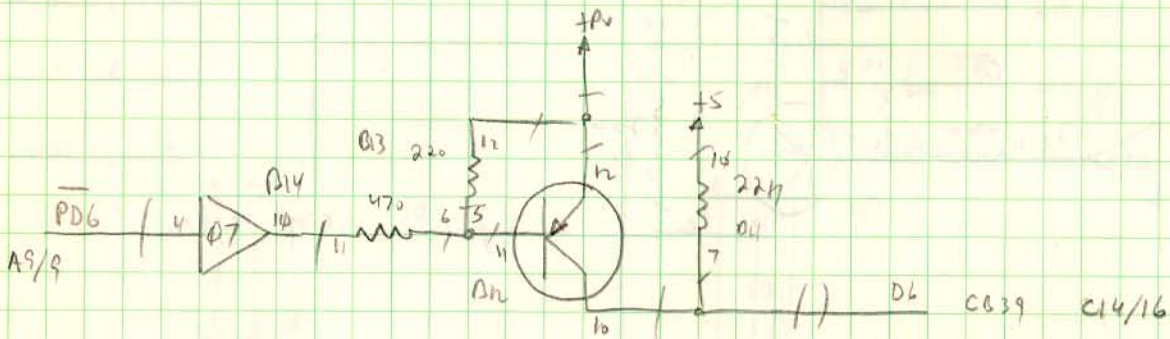
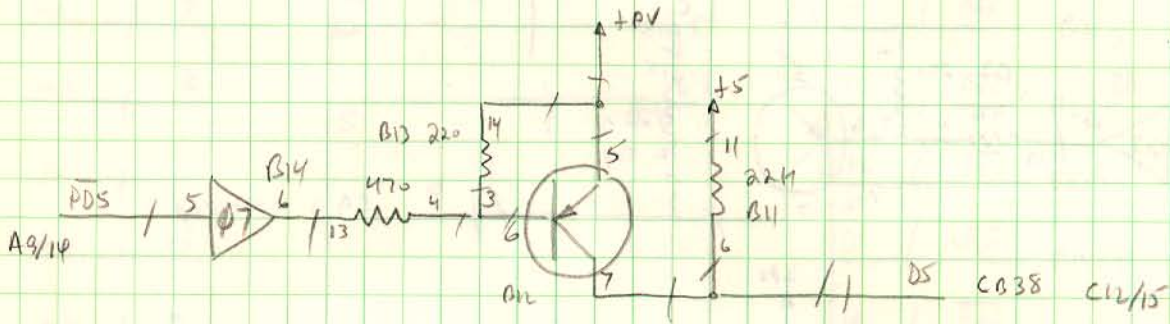
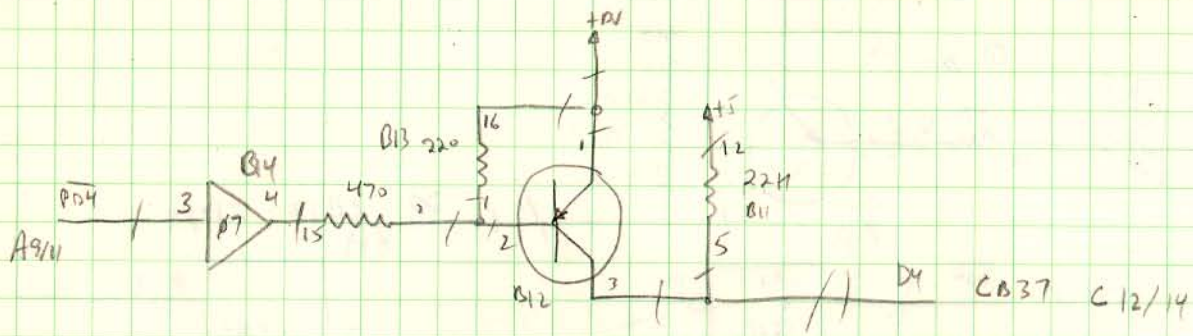


2 May 80  
ARA



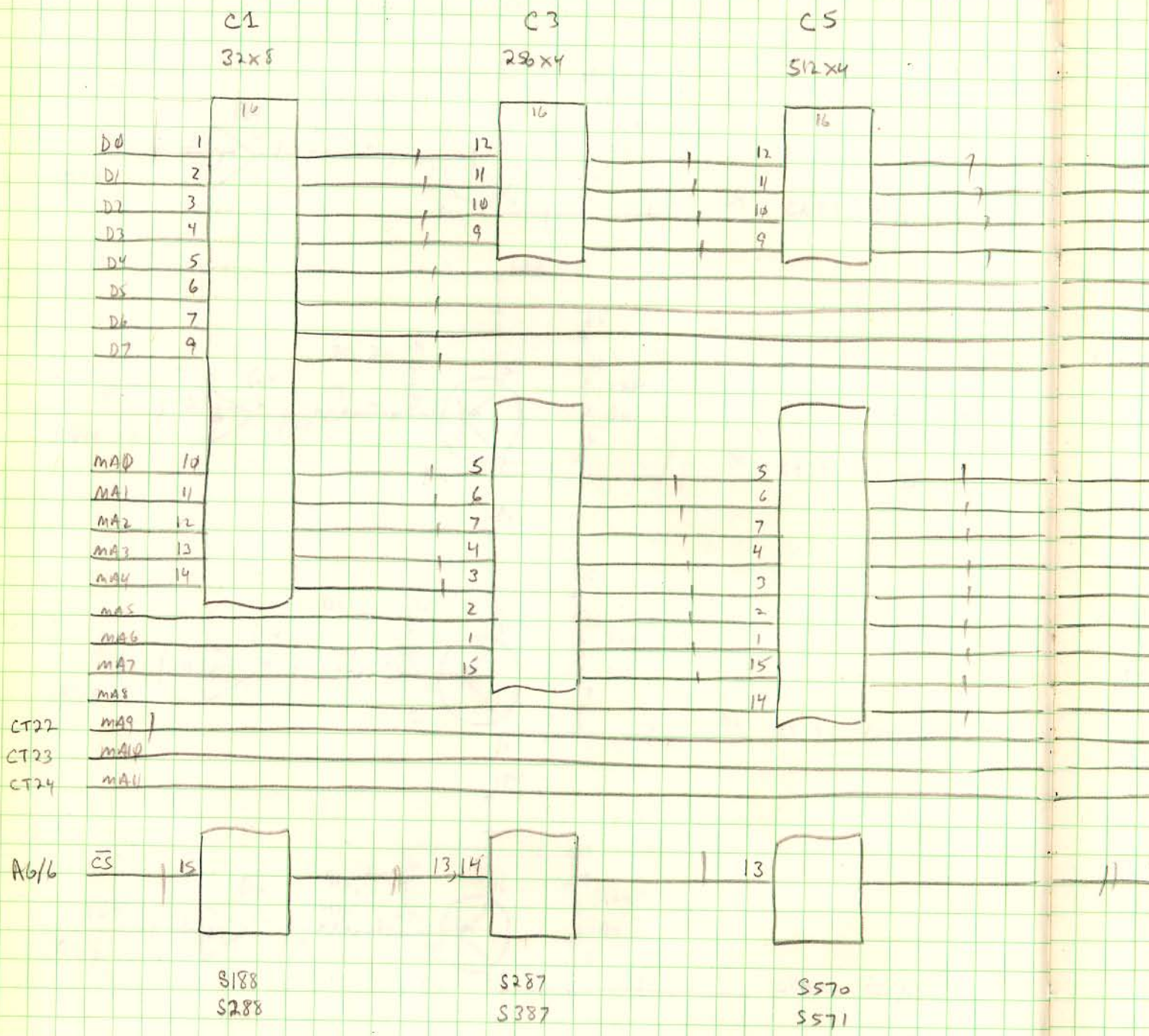
# Bit Drivers

transistors 2N4258





# PROM Socket Wiring



*Handwritten notes:*  
 C1 MA0  
 C1 MA1  
 C1 MA2  
 C1 MA3  
 C1 MA4  
 C1 MA5  
 C1 MA6  
 C1 MA7  
 C1 MA8  
 C1 MA9  
 C1 MA10



C7

1024x4



C9

512x8

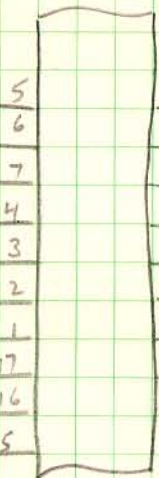


C12

512x8



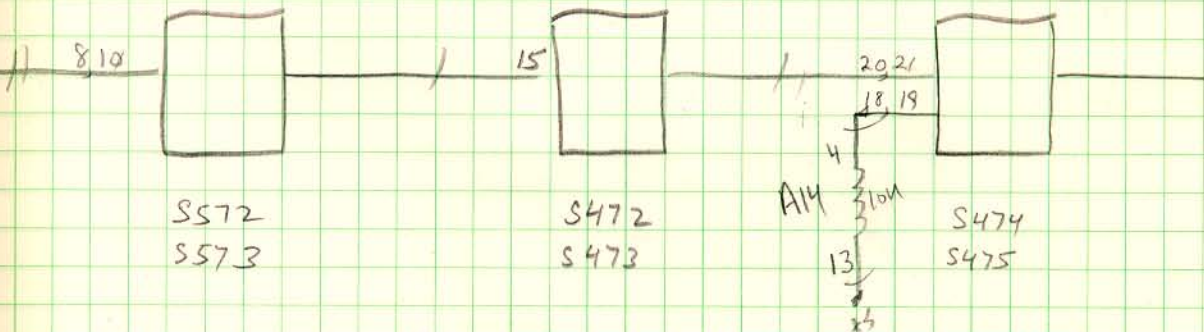
- / B10/3
- / B10/7
- / B10/10
- / B10/14
- / B12/3
- / B12/7
- / B12/10
- / B22/14



- / 1
- / 2
- / 3
- / 4
- / 5
- / 16
- / 17
- / 18
- / 19

- / 8
- / 7
- / 6
- / 5
- / 4
- / 3
- / 2
- / 1
- / 23

- / CT11
- / CT12
- / CT13
- / CT14
- / CT16
- / CT17
- / CT18
- / CT19
- / CT21



2 May 80  
ABD



# IC Localities

A1	LS74	-	64
A2	LS09	-	64
A3	LS09	-	64
A4	LS164	-	64
A5	LS164	-	64
A6	10	-	65
A7	20	-	65
A8	LS151	-	66
A9	LS138	-	66
A10	X		
A11	X		
A12	X		
A13	X		
A14	RES	-	64, 65

B1	RES	-	64
B2	LS132	-	64
B3	LS193	-	64
B4	LS193	-	64
B5	LS193	-	64
B6	X		
B7	X		
B8	07	-	66
B9	RES	-	66
B10	TRANS	-	66
B11	RES	-	66, 67
B12	TRANS	-	67
B13	RES	-	67
B14	07	-	65, 67



C1 68

C2 68

C3 68

C4 68

C5 68

C6 68

C7 68

C8 68

C9 68

C11 68

C12 68

C14 68

2 Mg 80  
A/D



Completed 6 May 80

Tested in ARS 6:7 May 80

CR 1110  
CR 1110



DEC LA-120 Diagnostic / 6800 BUS DIAGNOSTIC  
CARD

For DEC LA-120

F5	-	HALTS Processor
F4	-	---
F3	-	---
F2	-	'0' Selects LA-120
F1	}	Selects R/w IR/IW
F0		

For 6800 H-BUS

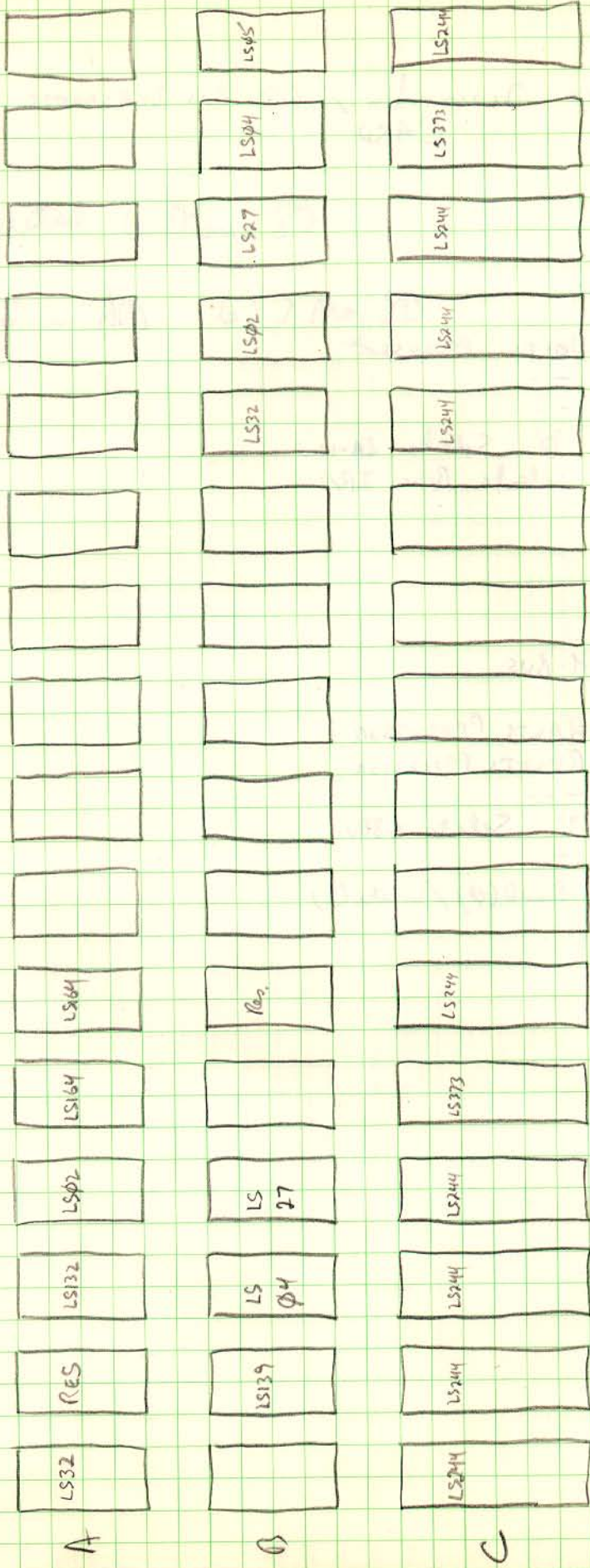
F5	-	HALTS Processor
F4	-	RESETS Processor
F3	-	---
F2	-	'1' Selects 6800
F1	-	---
F0	-	Read(0)/write(1)

16 May 80  
ARJ



Connector CT/CS

16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1



A

B

C

6800 H-BUS

DEC. CAB.



## 100 pin Connector

TOP SIDE CT (right to left from top)

1	+25A	-		26	MA12	-	C3/8	1
2	+25A	-		27	MA13	-	C3/6	2
3	+25B	-		28	MA14	-	C3/4	3
4	+25B	-		29	MA15	-	C3/2	4
5	+12	-		30	GND	+	A9/8	5
6	+12	-		31	MD0	-	C4/11	6
7	GND	+	A16/8	32	MD1	-	C4/13	7
8	GND	+	A15/8	33	MD2	-	C4/15	8
9	GND	+	A14/8	34	MD3	-	C4/17	9
10	GND	+	A13/8	35	GND	+	A8/8	10
11	MD0	-	C2/11	36	MD4	-	C4/8	11
12	MA1	-	C2/13	37	MD5	-	C4/6	12
13	MA2	-	C2/15	38	MD6	-	C4/4	13
14	MA3	-	C2/17	39	MD7	-	C4/2	14
15	GND	+	A12/8	40	GND	+	A7/8	15
16	MA4	-	C2/8	41	MD8	-		16
17	MA5	-	C2/6	42	MD9	-		17
18	MA6	-	C2/4	43	MD10	-		18
19	MA7	-	C2/2	44	MD11	-		19
20	GND	+	A11/8	45	GND	+	A6/8	20
21	MA8	-	C3/11	46	MD12	-		21
22	MA9	-	C3/13	47	MD13	-		22
23	MA10	-	C3/15	48	MD14	-		23
24	MA11	-	C3/17	49	MD15	-		24
25	GND	+	A10/8	50	GND	+	A5/8	25



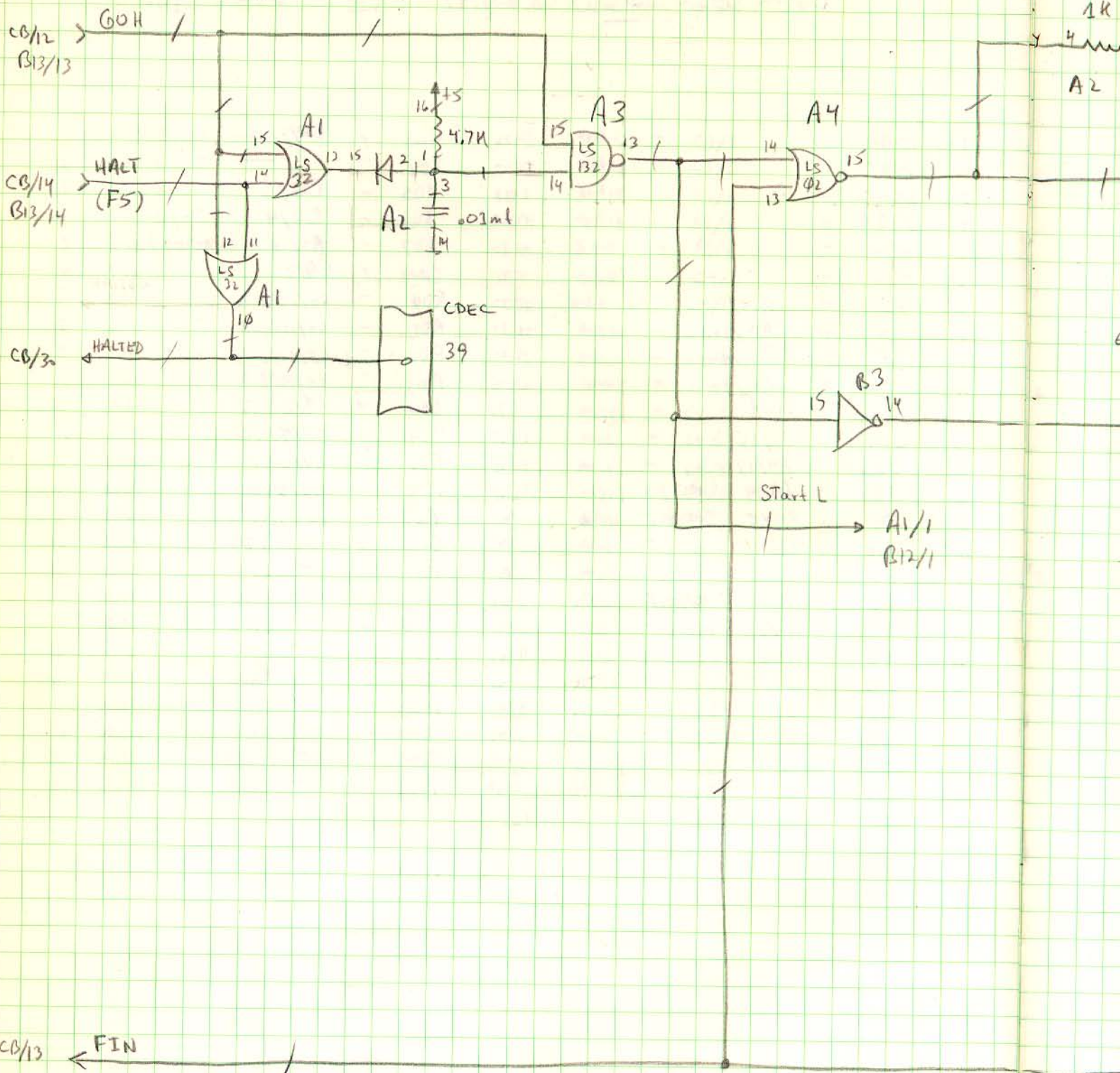
Bottom Side CB

1	25AR	-		26	GND	+	B10/8
2	25AR	-		27	ID4	-	
3	25BR	-		28	ID5	-	B15/6
4	25BR	-		29	ID6	-	B15/4
5	-12	-		30	ID7	-	A1/10 (HALTED)
6	-12	-		31	GND	+	B9/8
7	+5	-	A14/16	32	RD4	-	C5/12
8	+5	+	A13/16	33	RD1	-	C5/15
9	+5	+	A12/16	34	RD2	-	C5/16
10	+5	+	A11/16	35	RD3	-	C5/19
11	GND	+	B13/8	36	GND	+	B8/8
12	GM4	-	A1/15	37	RD4	-	C5/9
13	FIN	-	A4/13	38	RD5	-	C5/6
14	FS	-	A3/14 (HALT)	39	RD6	-	C5/5
15	F4	-	B16/5 (RESET)	40	RD7	-	C5/2
16	GND	+	B12/8	41	GND	+	E7/8
17	F3	-		42	RD8	-	
18	F2	-	A1/2 (8000/6000)	43	RD9	-	
19	F1	-	B2/3 { mode	44	RD10	-	
20	FD	-	B2/2	45	RD11	-	
21	GND	-	B11/8	46	GND	+	B6/8
22	ID0	-		47	RD12	-	
23	ID1	-		48	RD13	-	
24	ID2	-		49	RD14	-	
25	ID3	-		50	RD15	-	

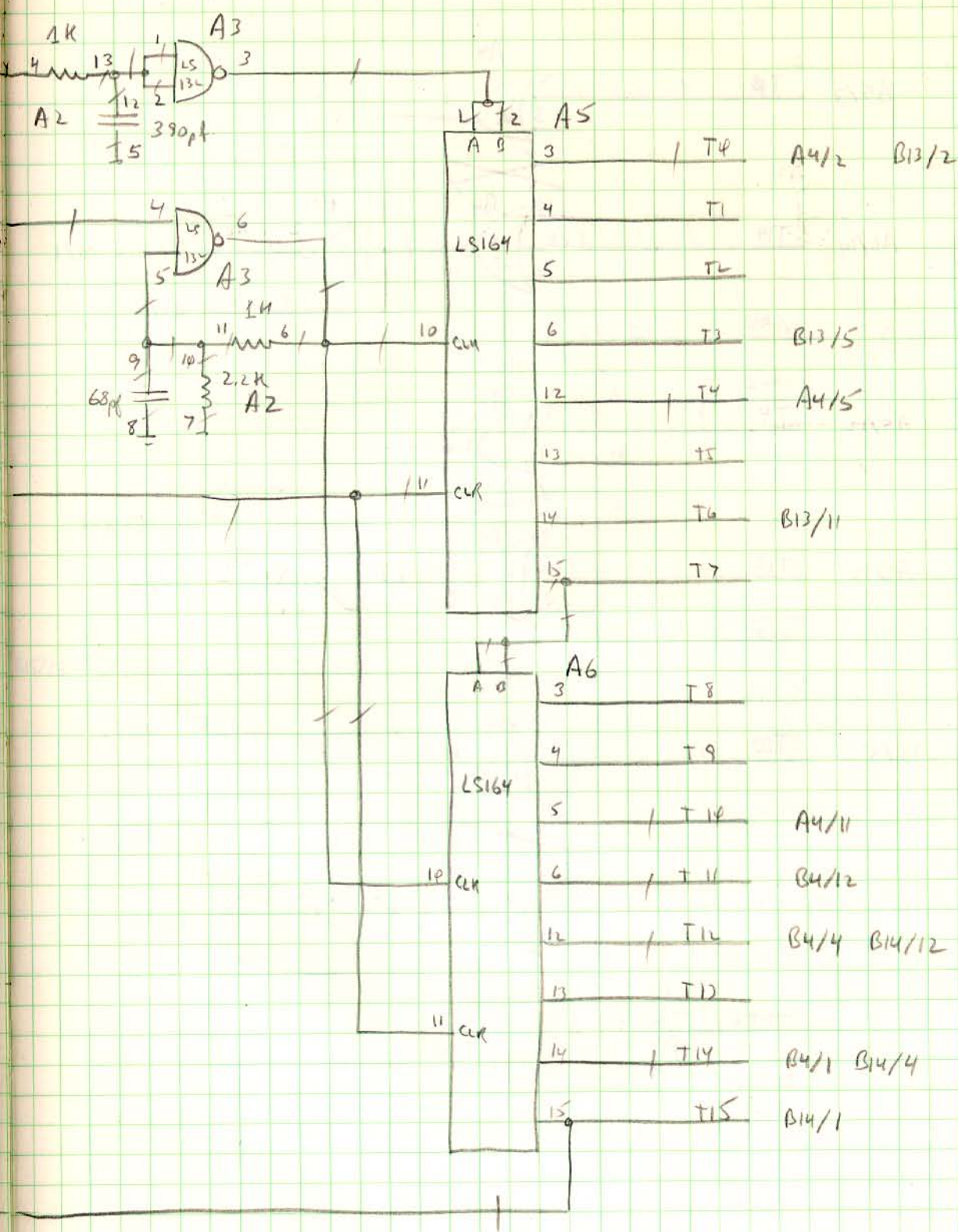
16 May 80  
ARR



# Clock Timing



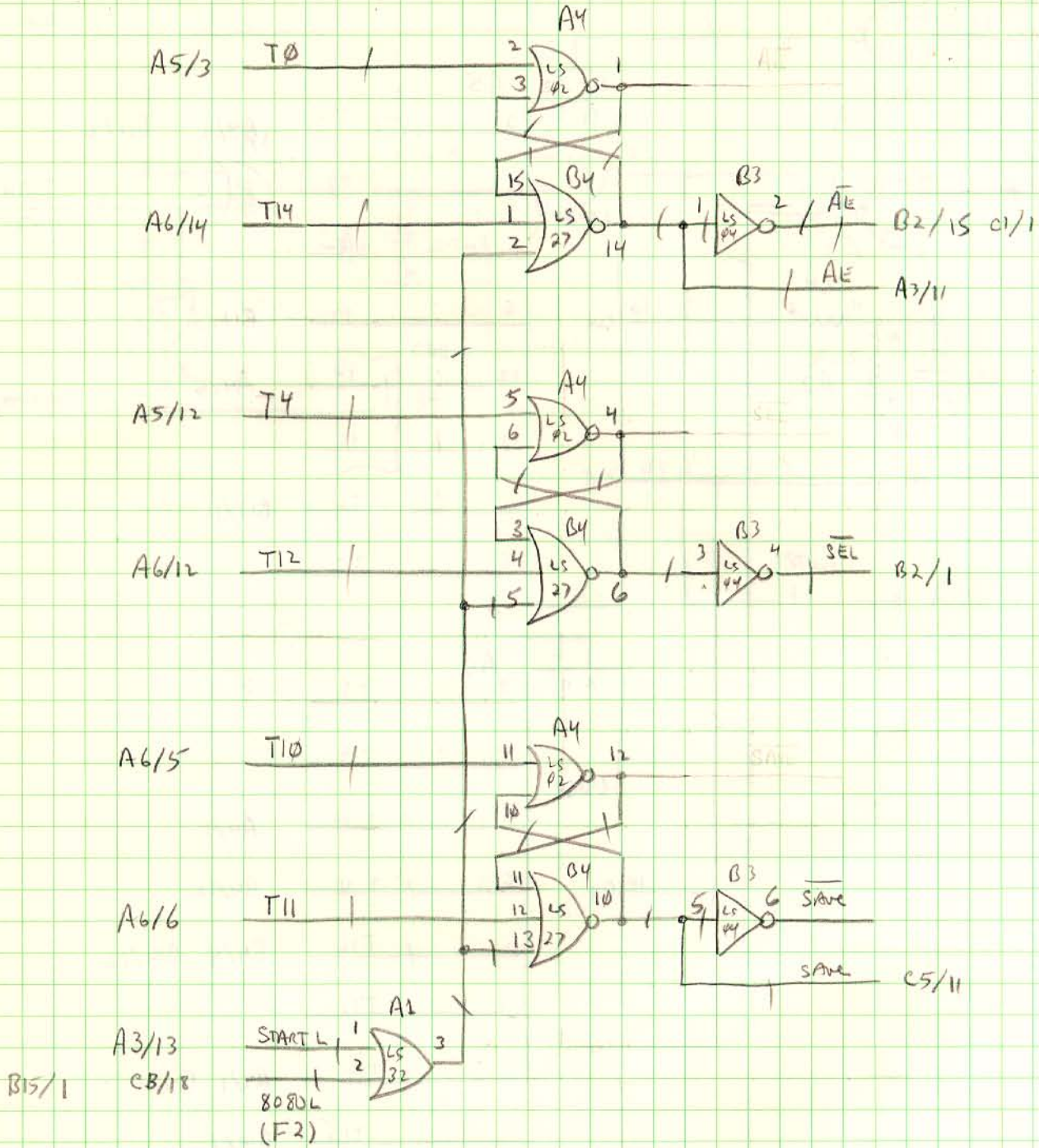




16 May 80  
 ACO

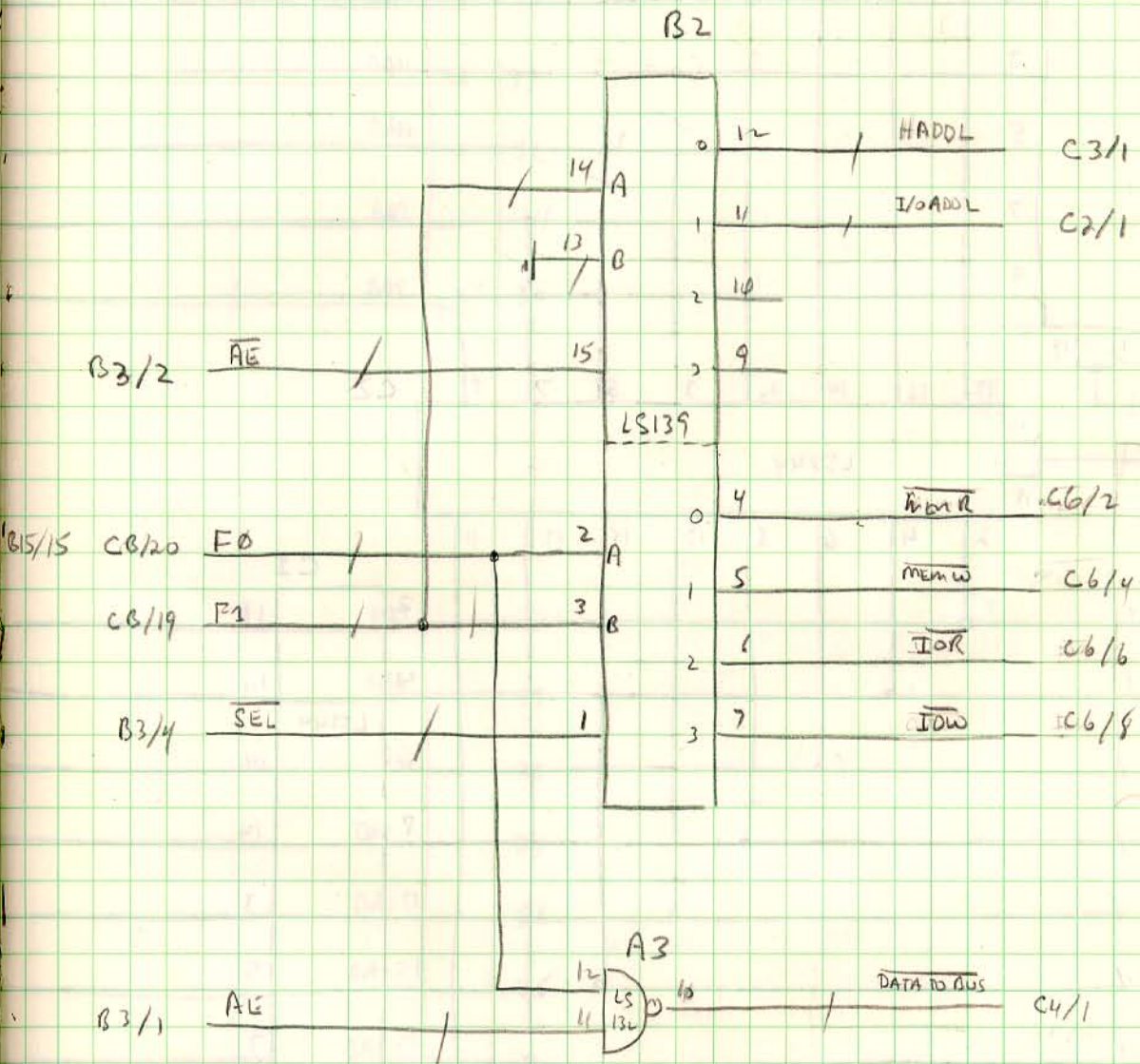


# DEC LA120 8080 Timing





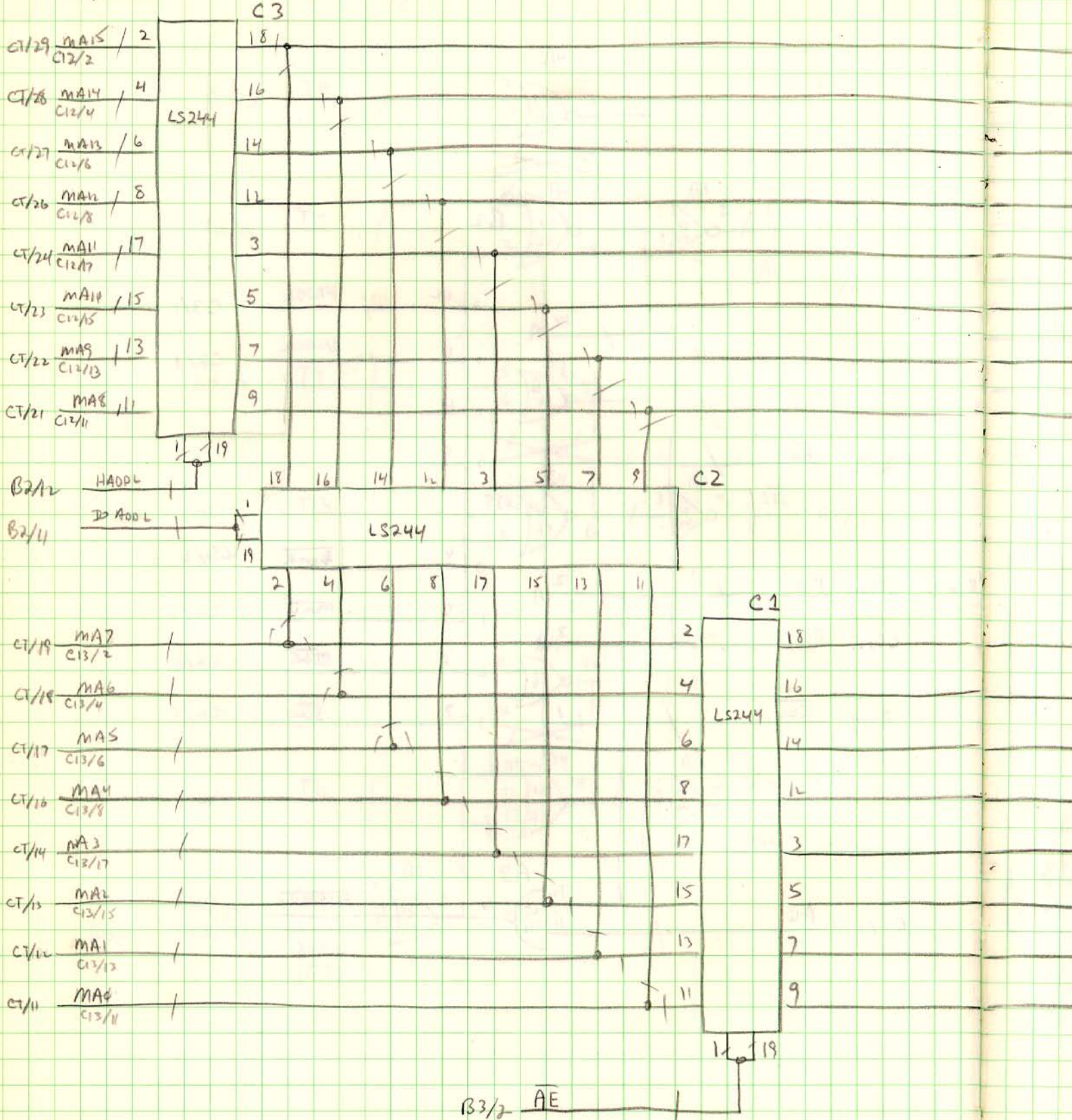
# Read/Write : Bus Control Logic



16 May 80  
ABD



# ADDRESS Buffers





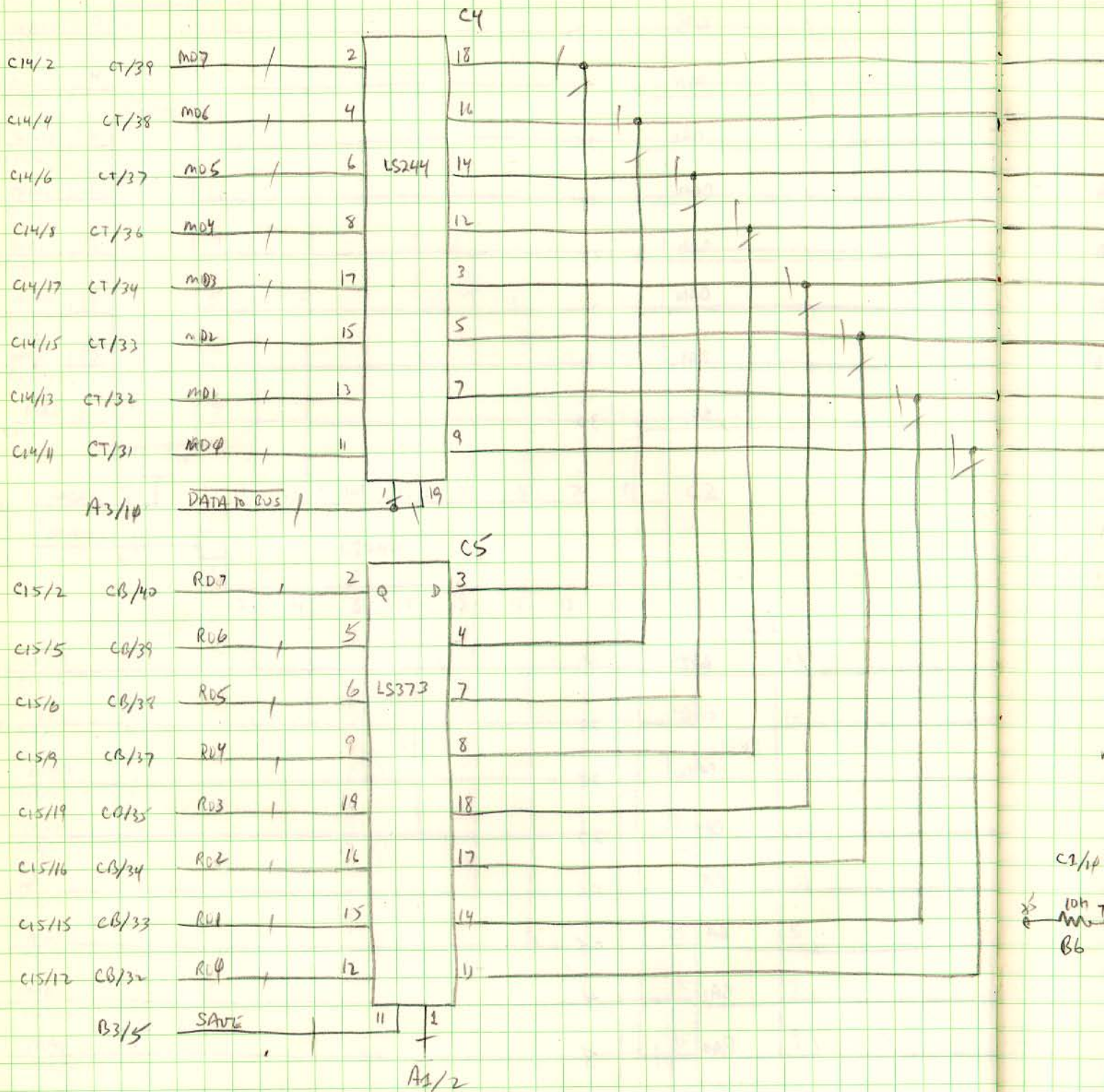
CDEC

/	BA6	37
/	BA5	36
/	BA4	35
/	BA3	34
/	BA2	33
/	BA1	32
/	BA0	31
/	BA7	30
/	BA7	6
/	BA6	29
/	BA5	28
/	BA4	27
/	BA3	26
/	BA2	25
/	BA1	7
/	BA0	8

16 May 80  
APP

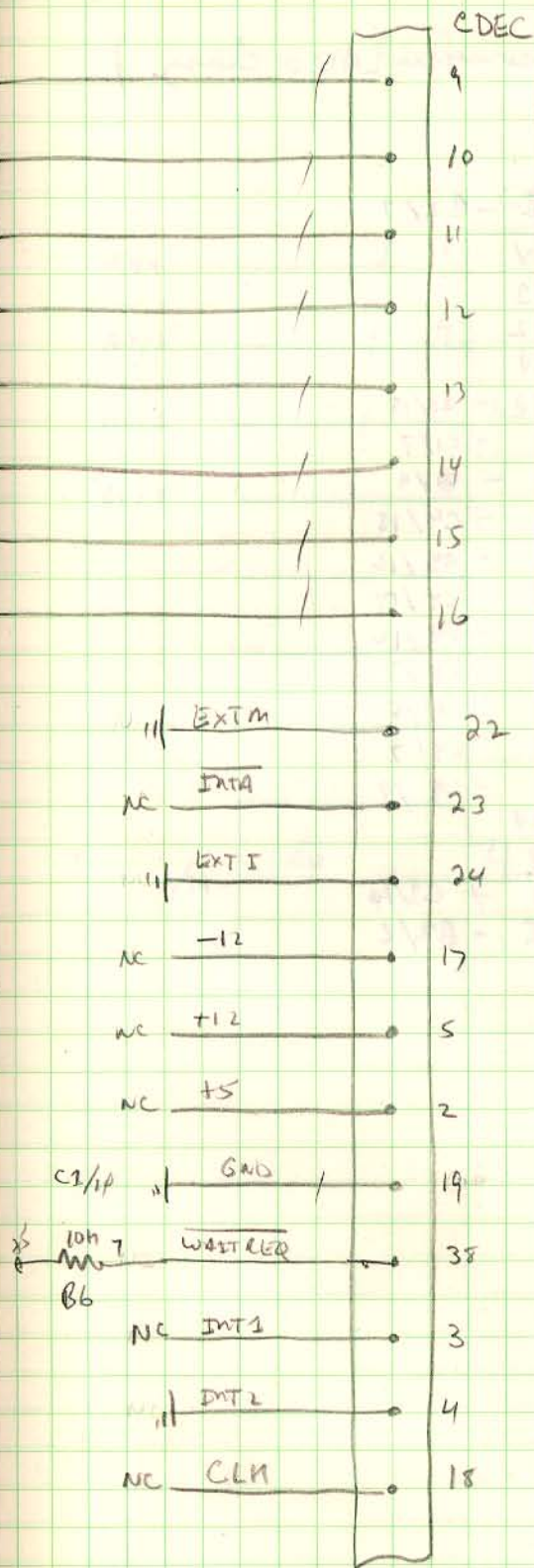


# DATA BUFFER / LATCH



C3/14  
10h  
B6





19 May 80  
AGD

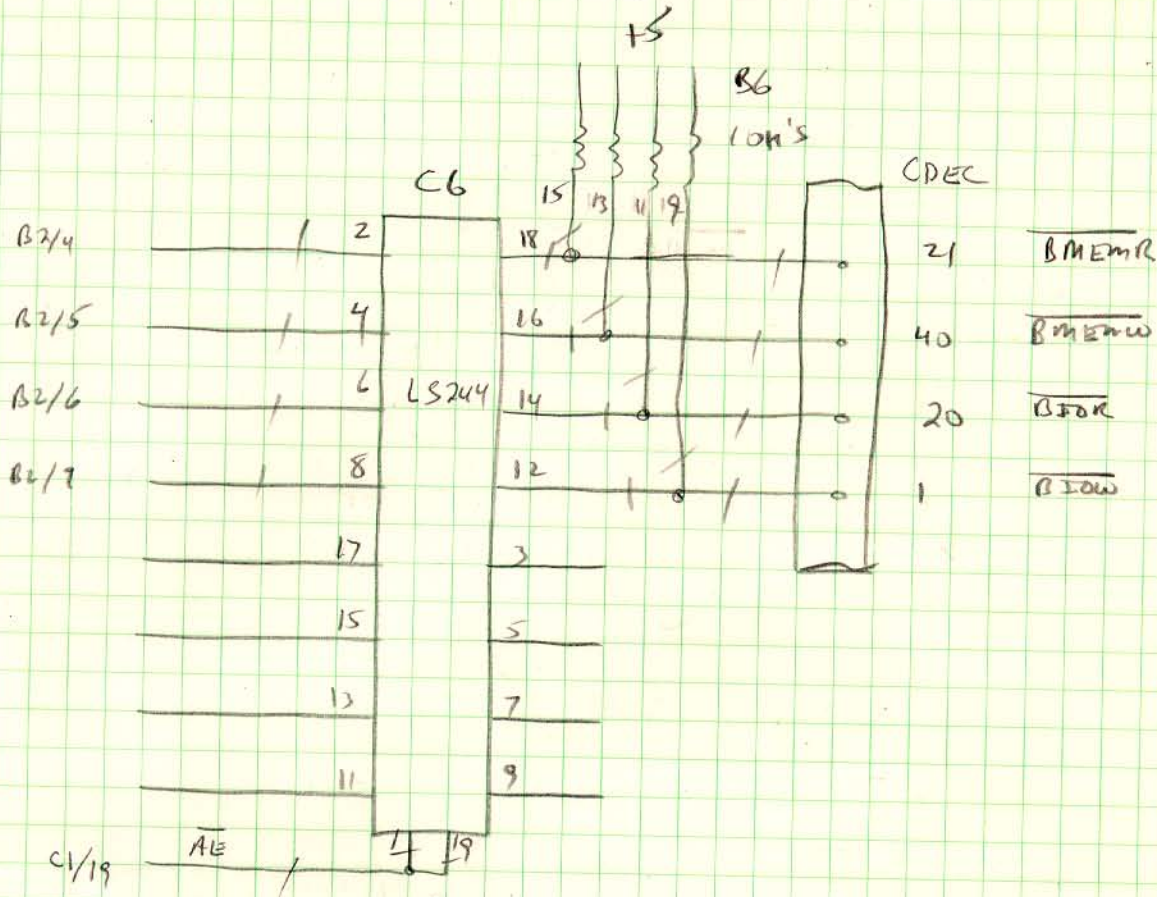


# Dec Counter Configuration

Top view (as observed in LA120 chassy)

B2/5 - MEMW	40	•	•	1	IO $\overline{W}$ - B2/7
A1/14 - HLD REQ	35	•	•	2	+5V
WAIT REQ	33	•	•	3	INT1
C3/18 - A15	37	•	•	4	INT2
C3/16 - A14	36	•	•	5	+12V
C3/14 - A13	35	•	•	6	A7 - C1/18
C3/12 - A12	34	•	•	7	A1 - C1/7
C3/3 - A11	33	•	•	8	A $\phi$ - C1/9
C3/5 - A10	32	•	•	9	D7 - C4/18
C3/7 - A9	31	•	•	10	D6 - C4/16
C3/9 - A8	30	•	•	11	D5 - C4/14
C1/16 - A6	29	•	•	12	D4 - C4/12
C1/14 - A5	28	•	•	13	D3 - C4/3
C1/12 - A4	27	•	•	14	D2 - C4/5
C1/3 - A3	26	•	•	15	D1 - C4/7
C1/5 - A2	25	•	•	16	D0 - C4/9
EXTI	24	•	•	17	-12V
INTA	23	•	•	18	CLK
EXTM	22	•	•	19	GND + C1/14
B2/4 - MEMR	21	•	•	20	IO $\overline{R}$ - B2/6

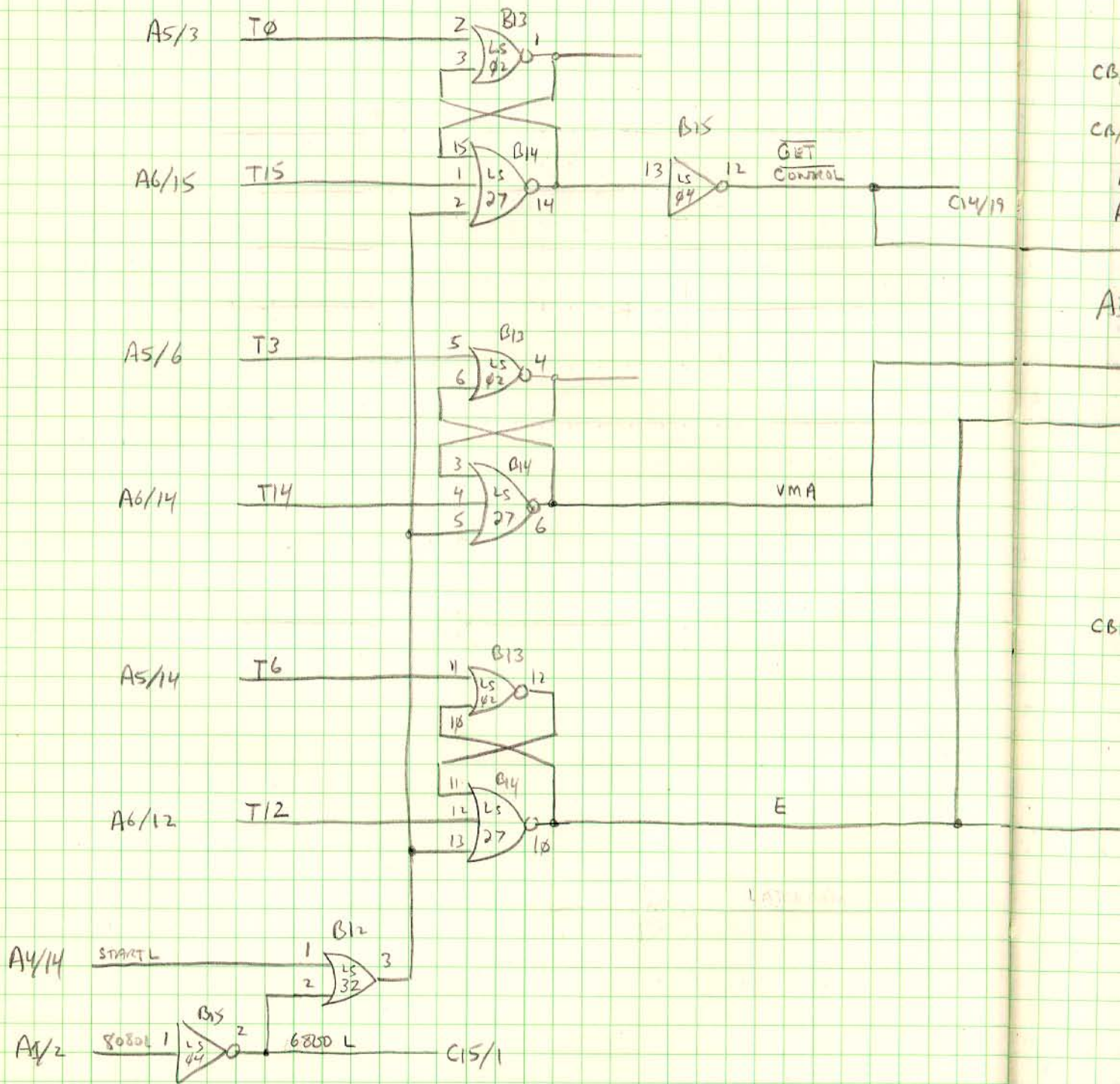




19 May 80  
APB



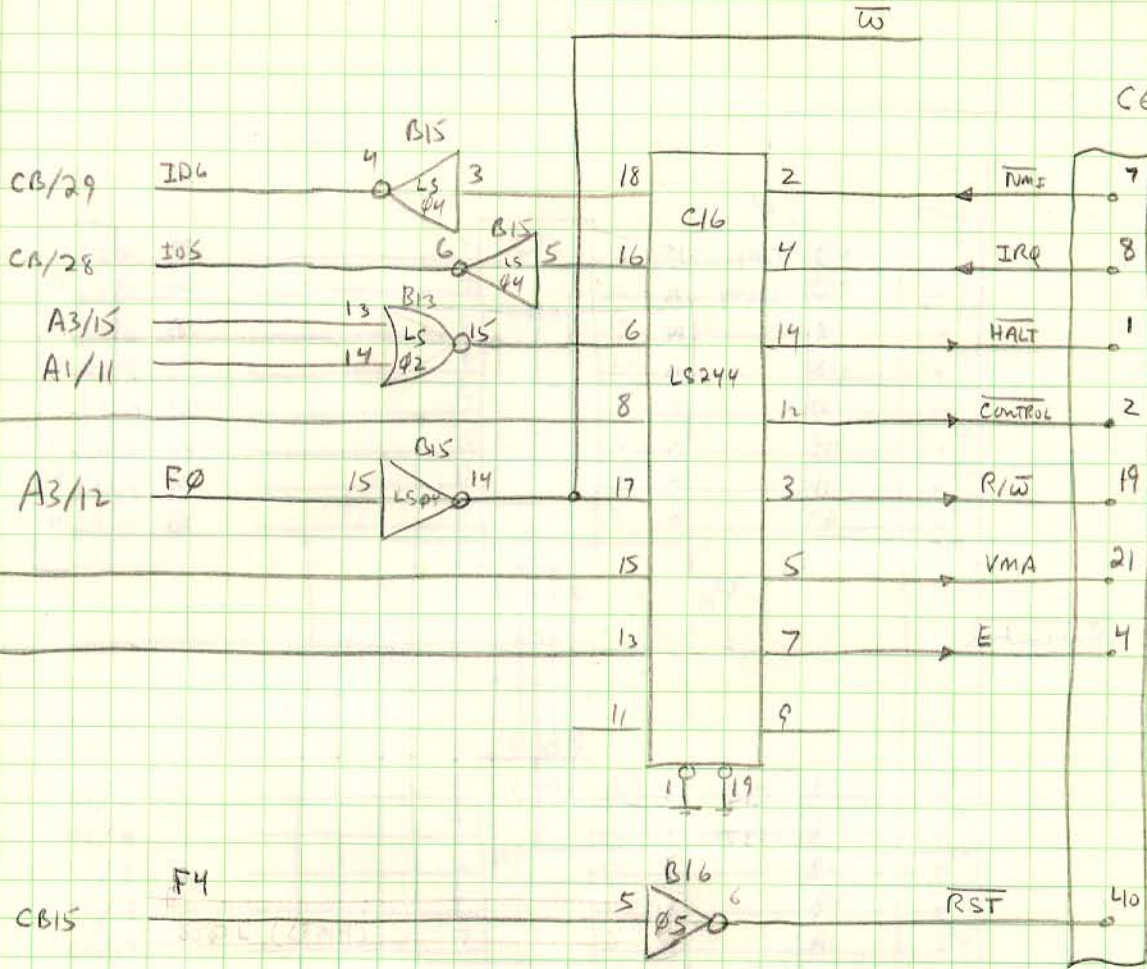
# 6800 K-BUS Diagnostic Wiring





CONTROL LOGIC

AT&T 80



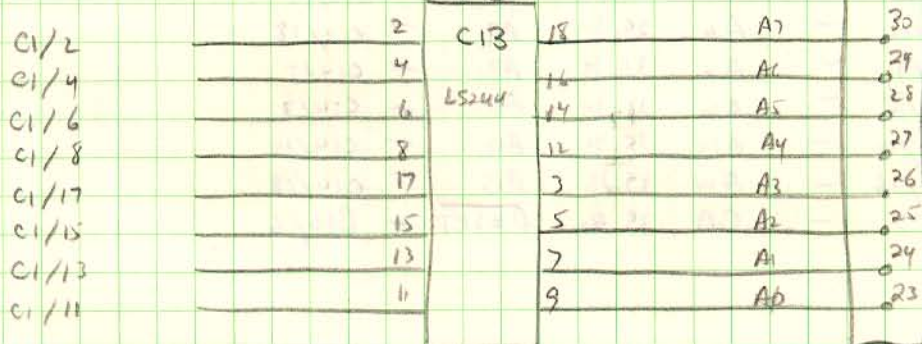
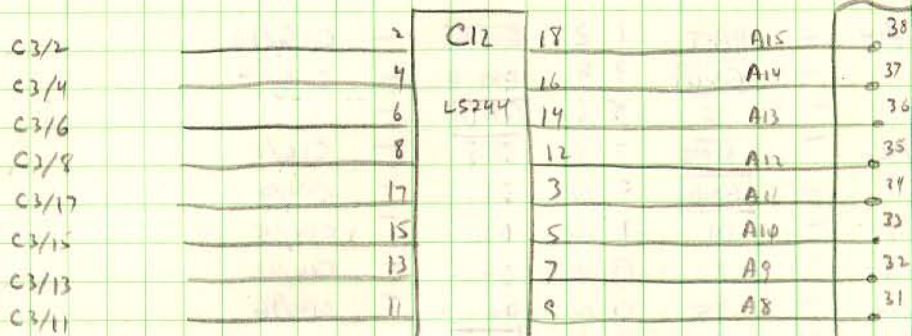
C15/11

5 Aug 80  
ARD



# ADDRESS Connections

CN6800



5 Aug 80  
ARD



H-BUS

# DIAGNOSTIC Connector Configuration

C16/14	-	HACT	1	2	EXT BUS	-	C16/12
-	-	GND	3	4	EXT E	-	C16/7
-	-	E	5	6	GND	-	-
C16/2	-	NMI	7	8	IRQ	-	C16/4
-	-	GND	9	10	D0	-	C14/9
C14/7	-	D1	11	12	D2	-	C14/5
C14/3	-	D3	13	14	D4	-	C14/12
C14/14	-	D5	15	16	D6	-	C14/16
C14/18	-	D7	17	18	GND	-	-
C16/5	-	EXT VMA	19	20	VMA	-	-
C16/3	-	EXT R/W	21	22	R/W	-	-
C13/9	-	A0	23	24	A1	-	C13/7
C13/5	-	A2	25	26	A3	-	C13/3
C13/12	-	A4	27	28	A5	-	C13/14
C13/16	-	A6	29	30	A7	-	C13/18
C14/9	-	A8	31	32	A9	-	C14/7
C14/5	-	A10	33	34	A11	-	C14/3
C14/12	-	A12	35	36	A13	-	C14/14
C14/16	-	A14	37	38	A15	-	C14/18
-	-	BA	39	40	RESET	-	B16/6



# Advanced Micro Devices Generic PROM Programmer

84

This Card will program all AMD Devices of the following types:

32x8	Am27S18 / Am27S19	(74S188 / 74S288)
256x4	Am27S20 / Am27S21	(74S287 / 74S387)
512x4	Am27S12 / Am27S13	
1024x4	Am27S32 / Am27S33	
512x8	Am27S28 / Am27S29	(74S472 / 74S473)
2048x4	Am27S184 / Am27S185	
512x8	Am27S30 / Am27S31	
1024x8	Am27S180 / Am27S181	

ID = 21

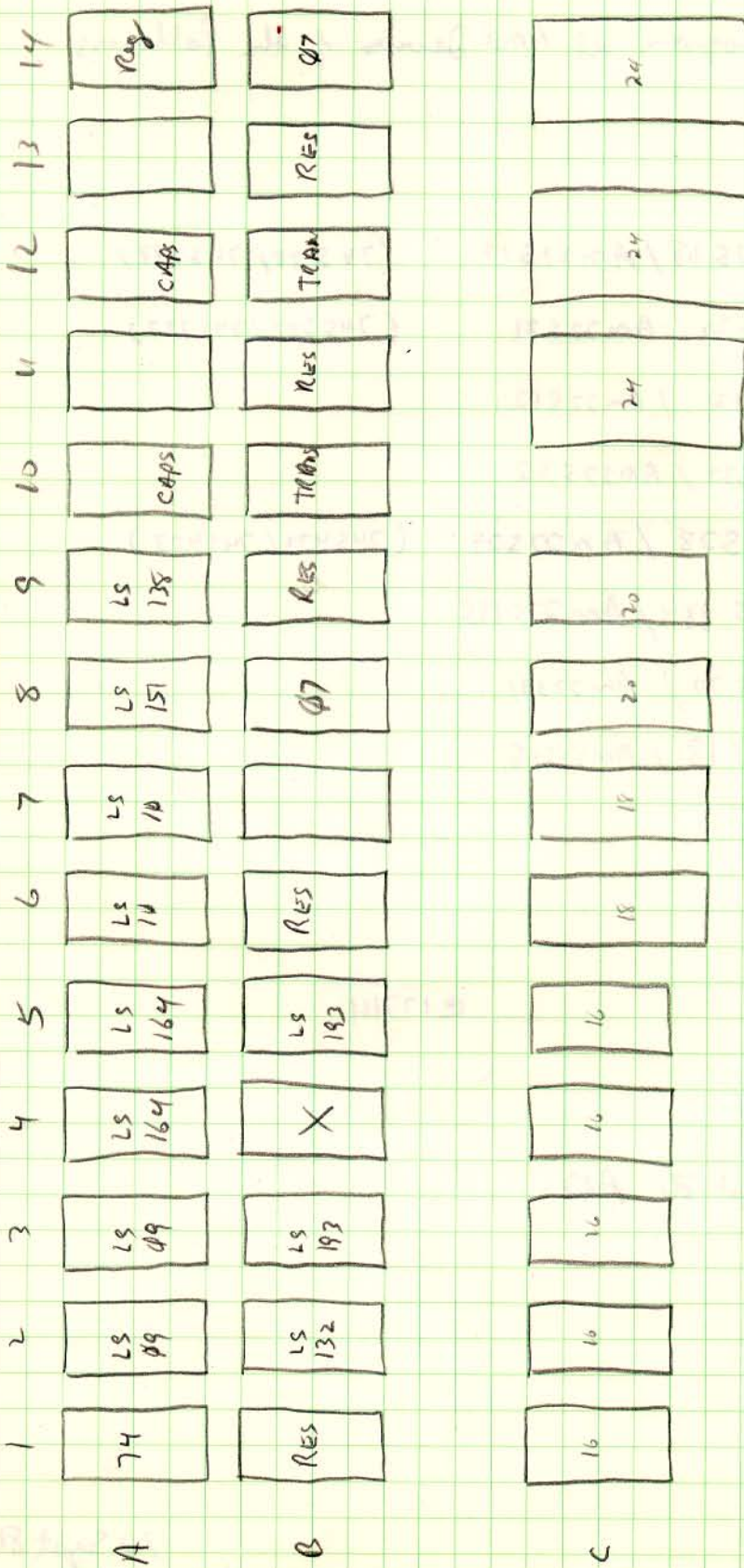
@177111

final checkout 15 Sept 80 AOD

10 Sept 80  
AOD



# Layout





100 Pin Connector  
Top Side CT



1	+25A	+	A14/2
2	+25A	-	
3	+25B	-	
4	+25B	-	
5	+12	-	
6	+12	-	
7	GND	+	A14/8
8	GND	+	A13/8
9	GND	+	A12/8
10	GND	+	A11/8
11	MA4	+	C14/8
12	MA1	+	C14/7
13	MA2	+	C14/6
14	MA3	+	C14/5
15	GND	+	A10/8
16	MA4	+	C14/4
17	MA5	+	C14/3
18	MA6	+	C14/2
19	MA7	+	C14/1
20	GND	+	A9/8
21	MA8	+	C14/23
22	MA9	+	C14/22
23	MA10	+	C6/8
24	MA11	-	
26	GND	+	A8/8

28	MA12	-	
27	MA13	-	
25	MA14	-	
29	MA15	-	
30	GND	+	A7/8
31	MD8	+	A8/4
32	MD1	+	A8/3
33	MD2	+	A8/2
34	MD3	+	A8/1
35	GND	+	A6/8
36	MD4	+	A8/15
37	MD5	+	A8/14
38	MD6	+	A8/13
39	MD7	+	A8/12
40	GND	+	A5/8
41	MD8	-	
42	MD9	-	
43	MD10	-	
44	MD11	-	
45	GND	+	A4/8
46	MD12	-	
47	MD13	-	
48	MD14	-	
49	MD15	-	
50	GND	+	A3/8

1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	G
12	G
13	F
14	F
15	F
16	G
17	F
18	F
19	F
20	F
21	G
22	F
23	F
24	F
25	F



## Bottom Side CB

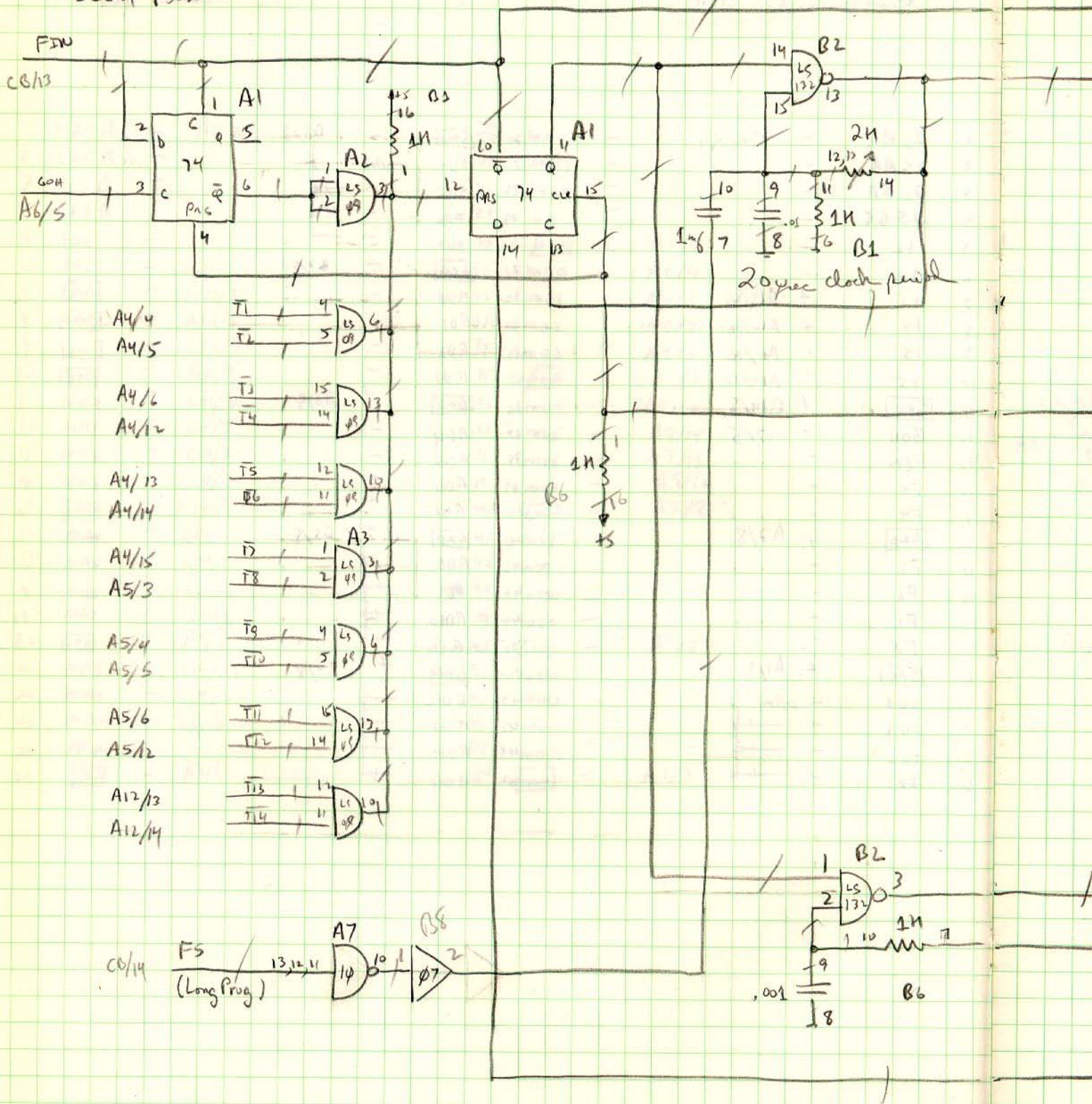
1	25AR	7	C14/12
2	25AR	-	
3	25BR	-	
4	25BR	-	
5	-12	-	
6	-12	-	
7	+5	+	A13/16
8	+5	+	A12/16
9	+5	+	A11/16
10	+5	+	A10/16
11	GND	+	B14/8
12	G0H	-	A7/5
13	F10	-	
14	F5	-	
15	F4	-	
16	GND	+	A2/8
17	F3	-	
18	F2	-	
19	F1	-	
20	F0	-	
21	GND	+	A1/8
22	ID9	-	open
23	ID1	-	+
24	ID2	-	+
25	ID3	-	+

26	GND	-	B8/8
27	ID4	-open	+
28	ID5	-	+
29	ID6	-	+
30	ID7	-	+
31	GND	+	B7/8
32	RD4	-	
33	RD1	-	
34	RD2	-	
35	RD3	-	
36	GND	+	B6/8
37	RD4	-	
38	RD5	-	
39	RD6	-	
40	RD7	-	
41	GND	+	B5/8
42	RD8	+	+
43	RD9	+	+
44	RD10	+	+
45	RD11	+	+
46	GND	+	B4/8
47	RD12	+	+
48	RD13	+	+
49	RD14	+	+
50	RD15	+	+

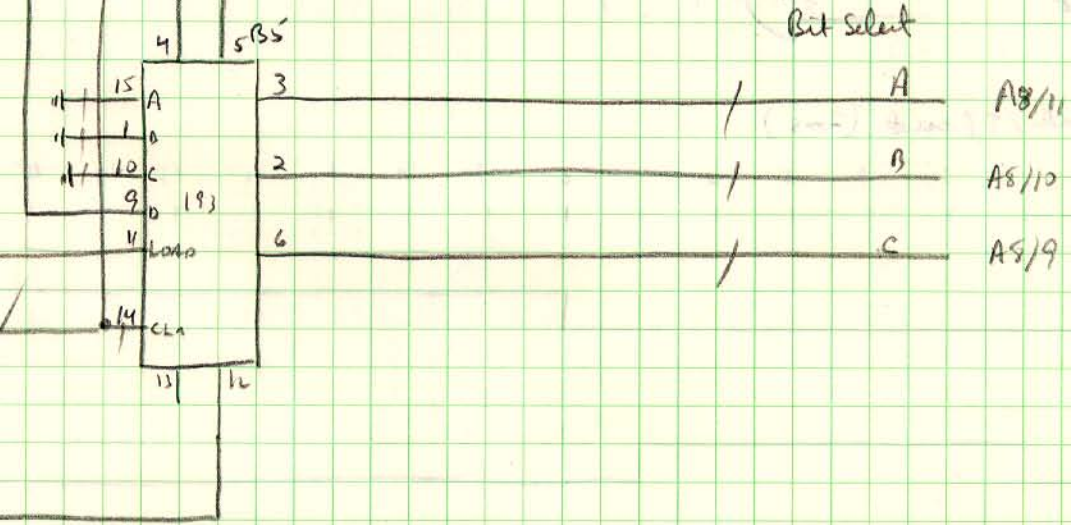
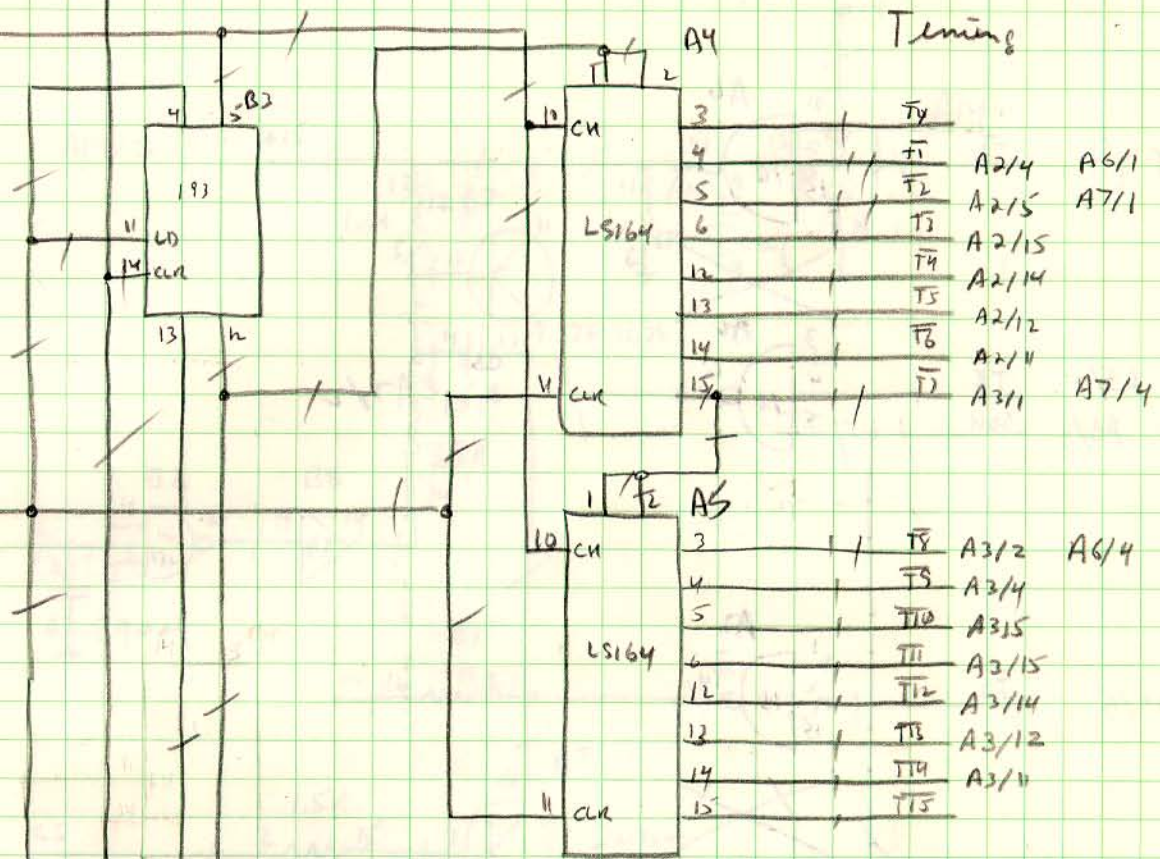
10 Sept 80  
ARD



# Scan Timer



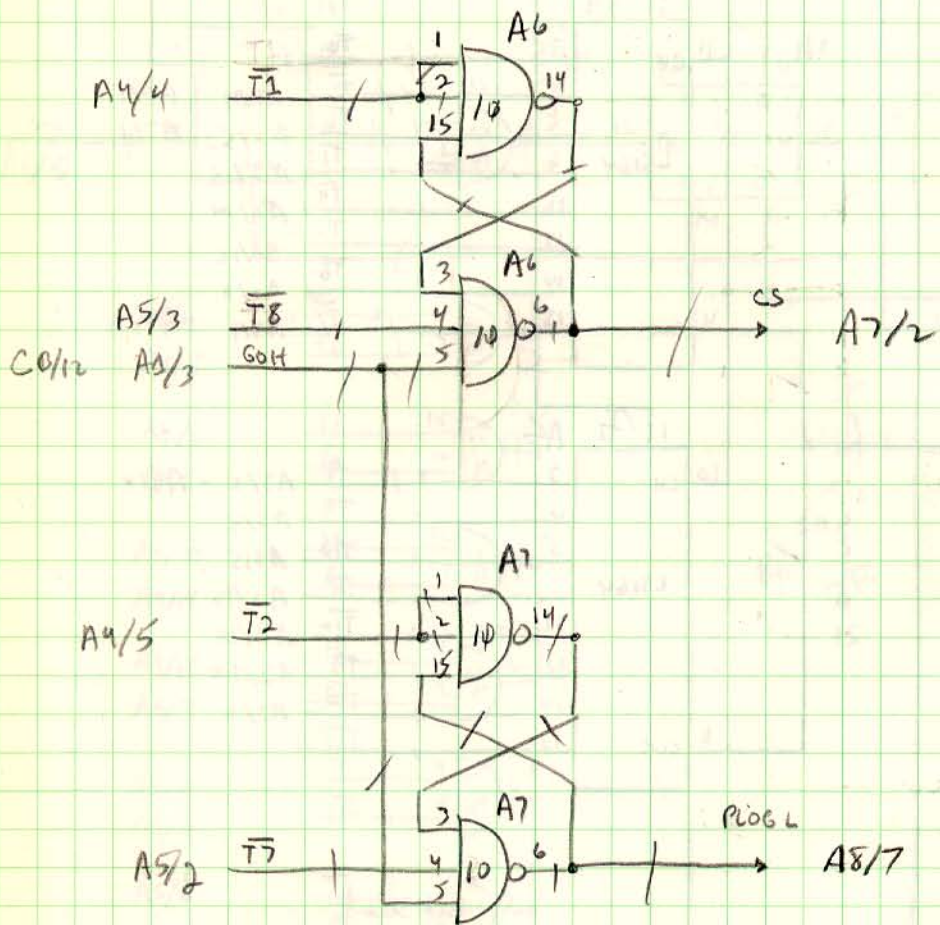




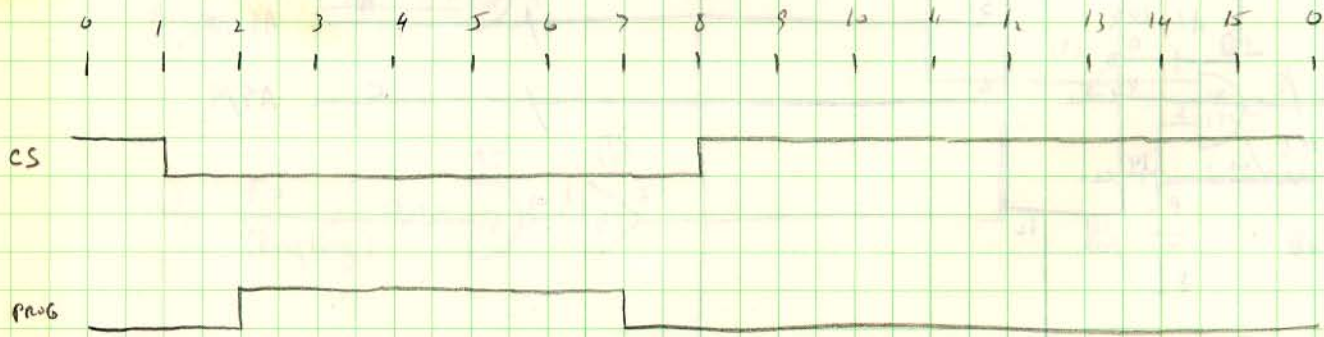
10 Sept 80  
ARO



# Pulse Timing Generators



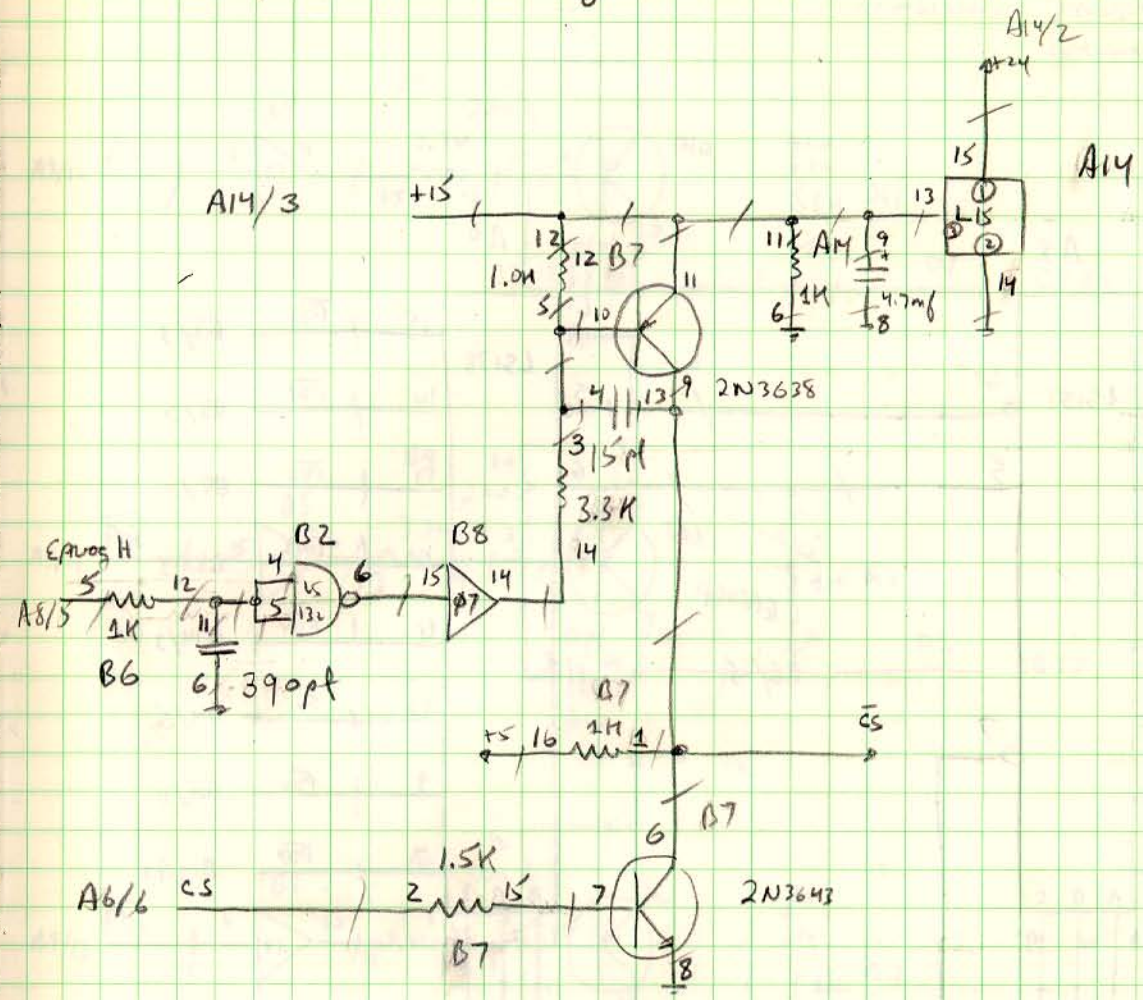
20  $\mu$ sec/div / T period (2ms)



Repeated for each Bit!



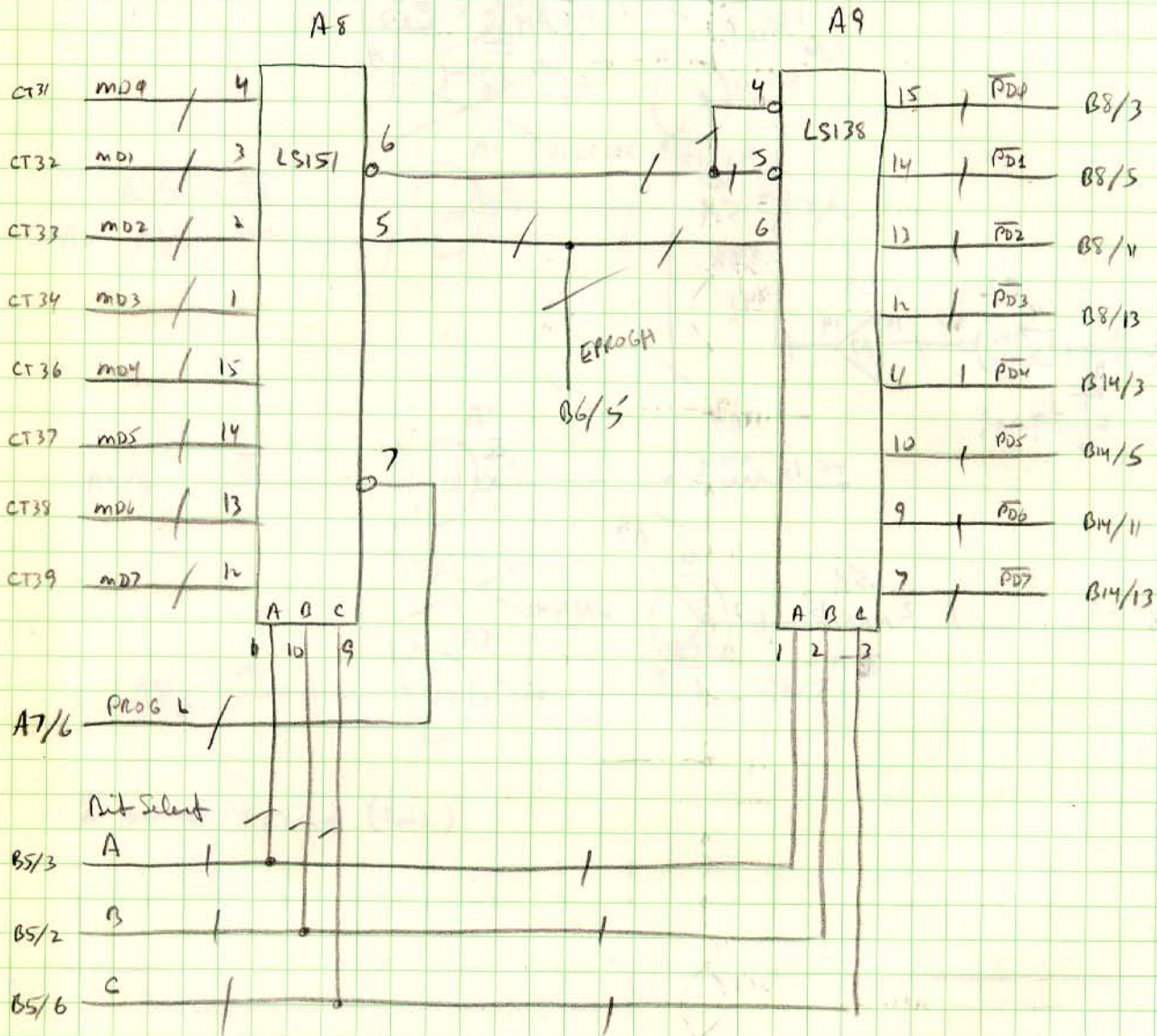
# Chip Select Timing



10 Sept 80  
ARD



# BIT DATA Selector



A9/15 PD

A9/14 PD

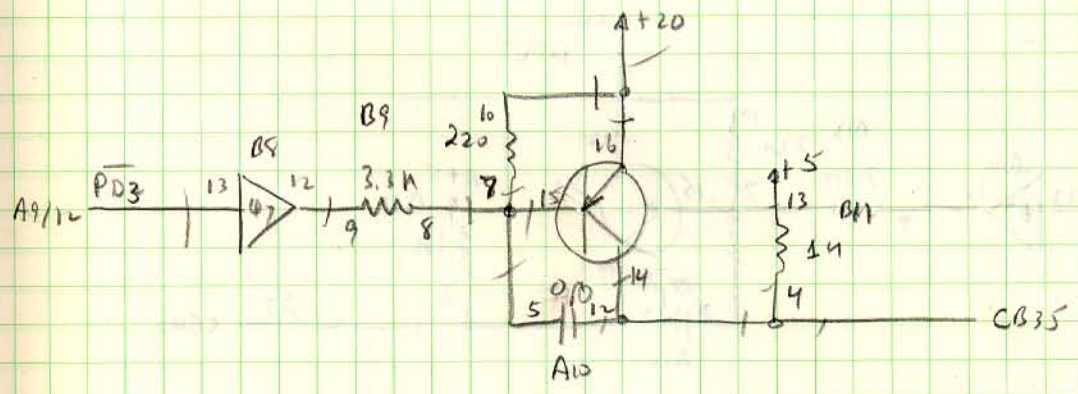
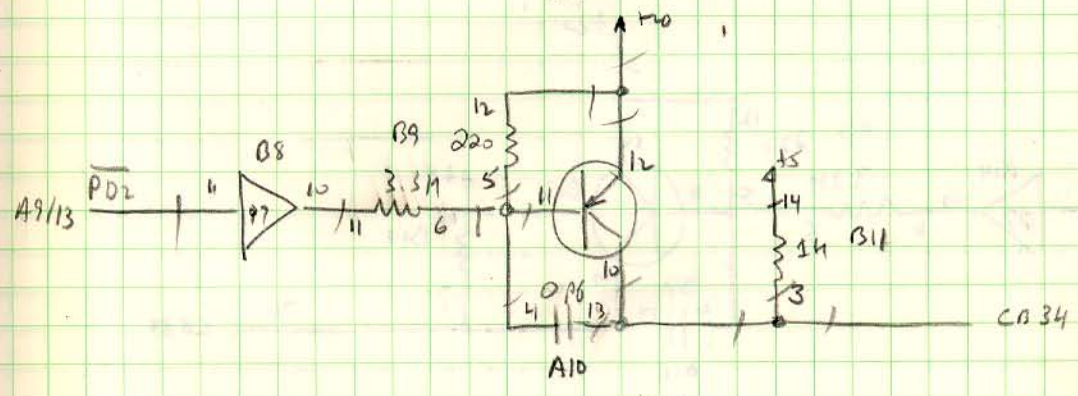
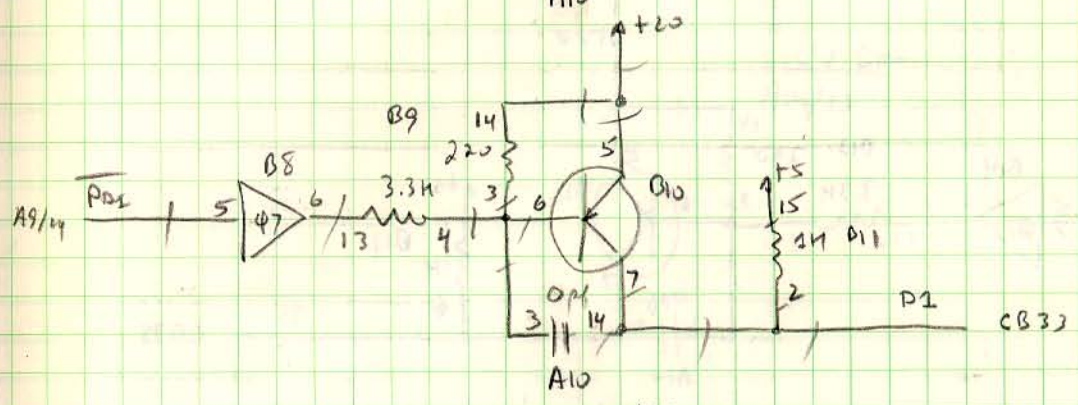
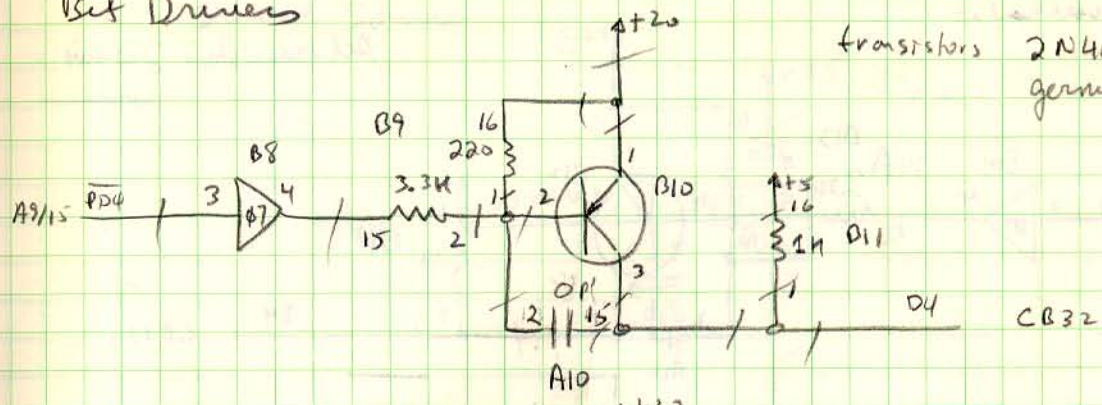
A9/13 PD

A9/12 PD



# Bit Drivers

transistors 2N404  
germanium

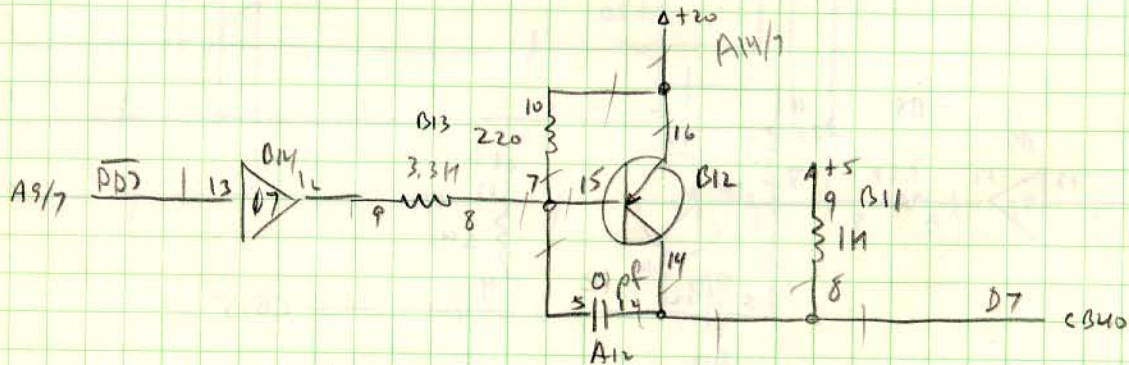
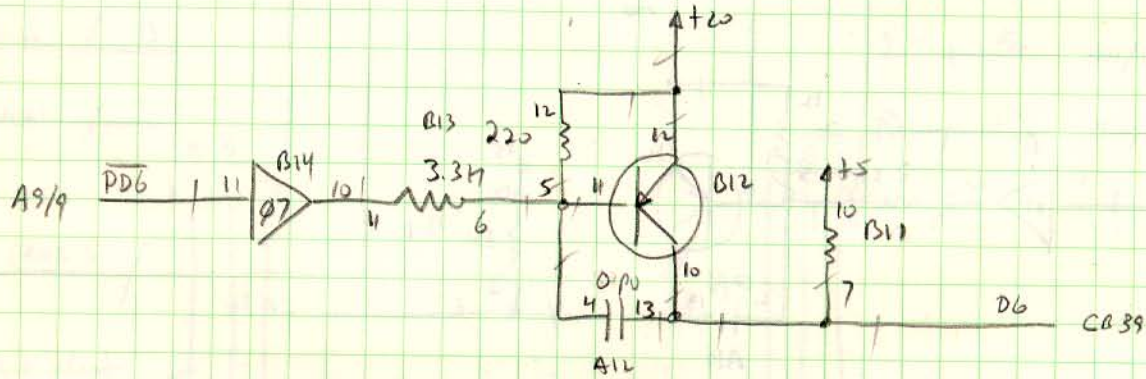
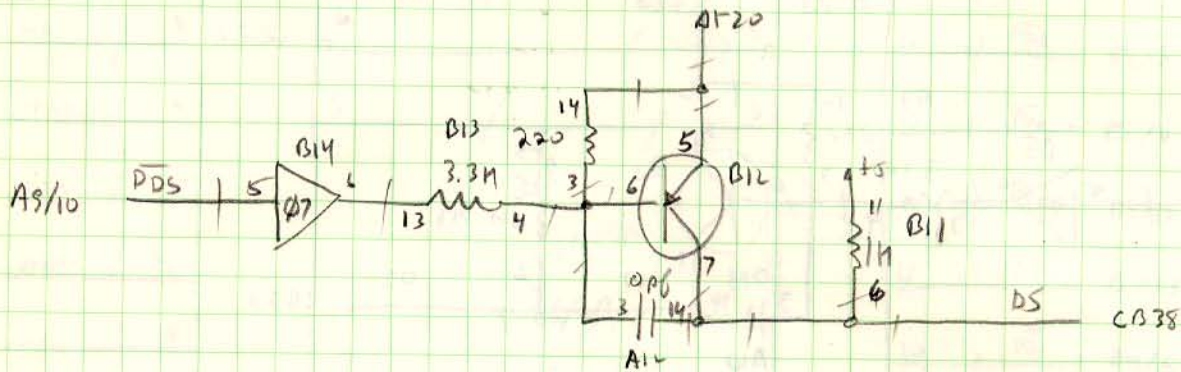
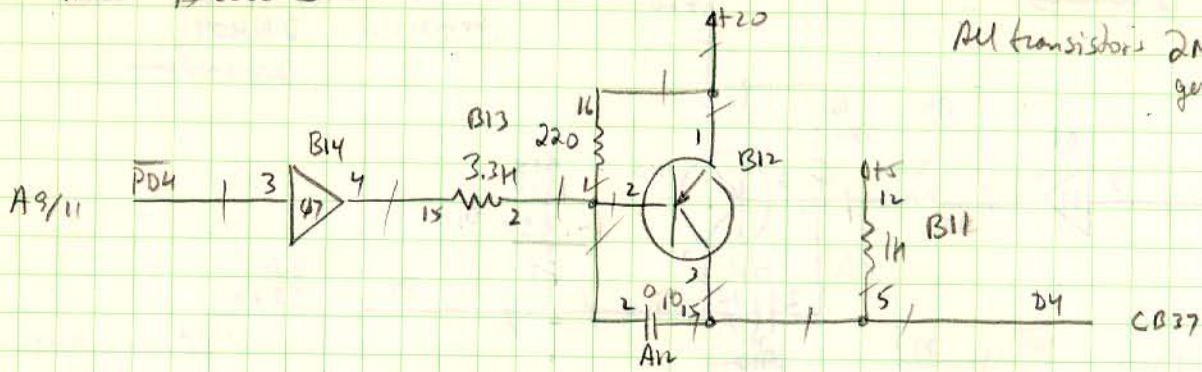


10 Sept 80  
APP



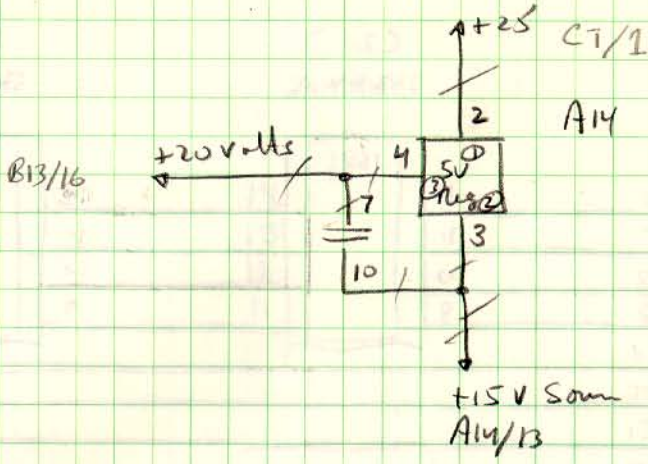
# Bit Drivers

All transistors 2N404 germanium





20 volt Source



10 Sept 80  
A80

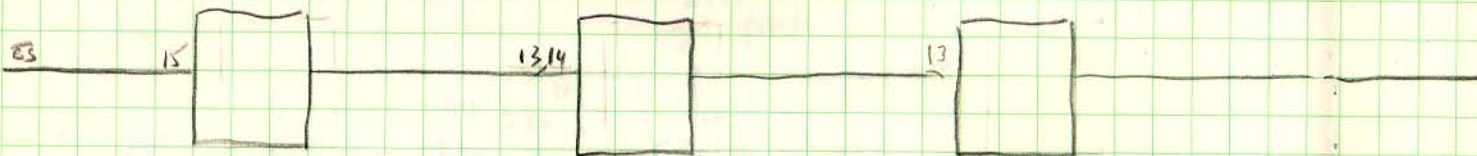
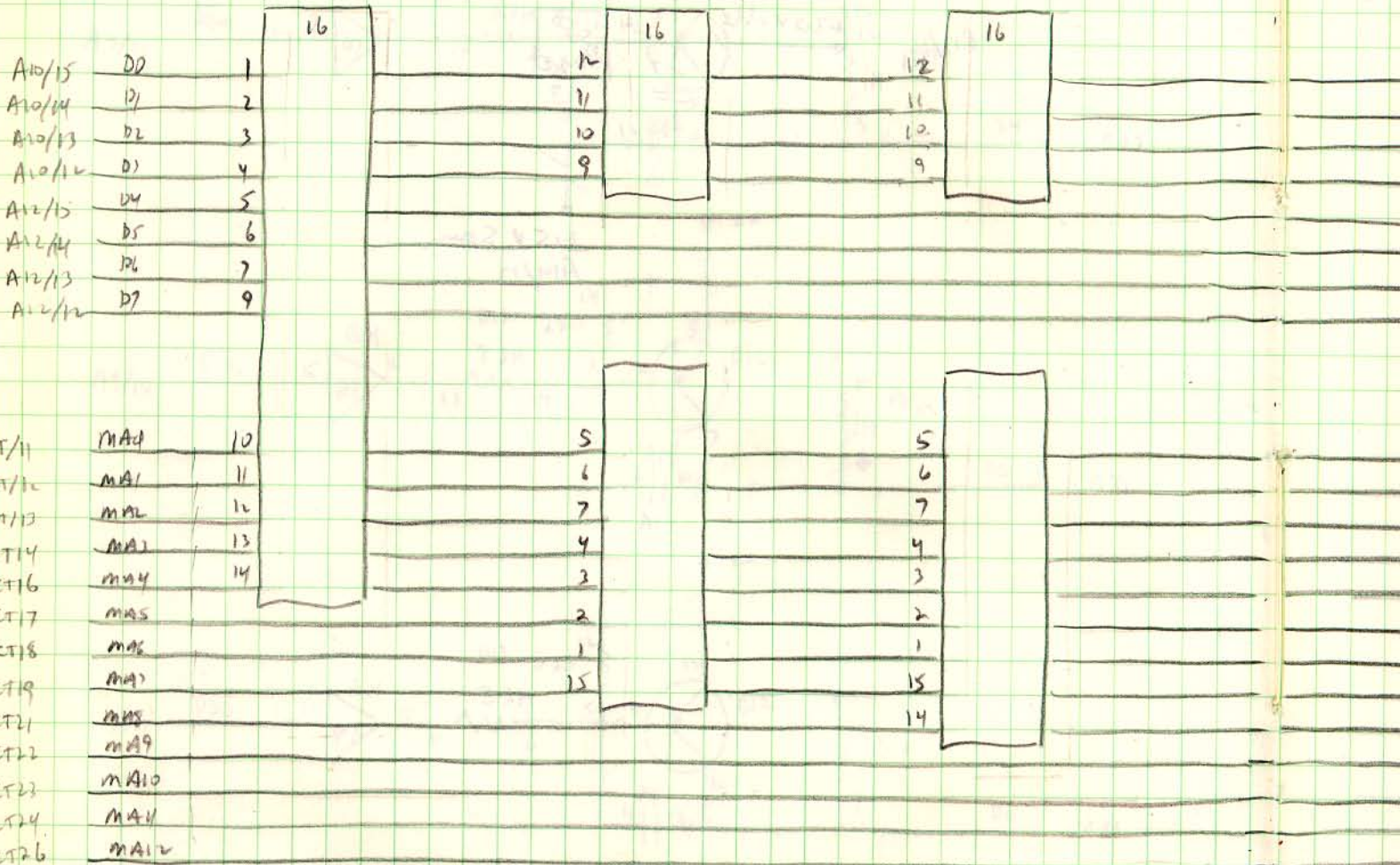


# Prom Socket Wiring

C1  
32x8

C3  
256x4

C5  
512x4



Am 27S18  
Am 27S19

Am 27S08  
Am 27S09

Am 27S20  
Am 27S21

Am 27S10  
Am 27S11

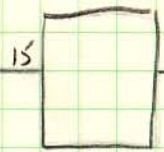
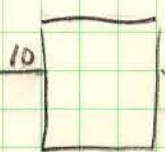
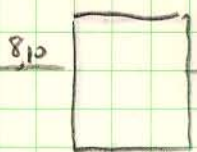
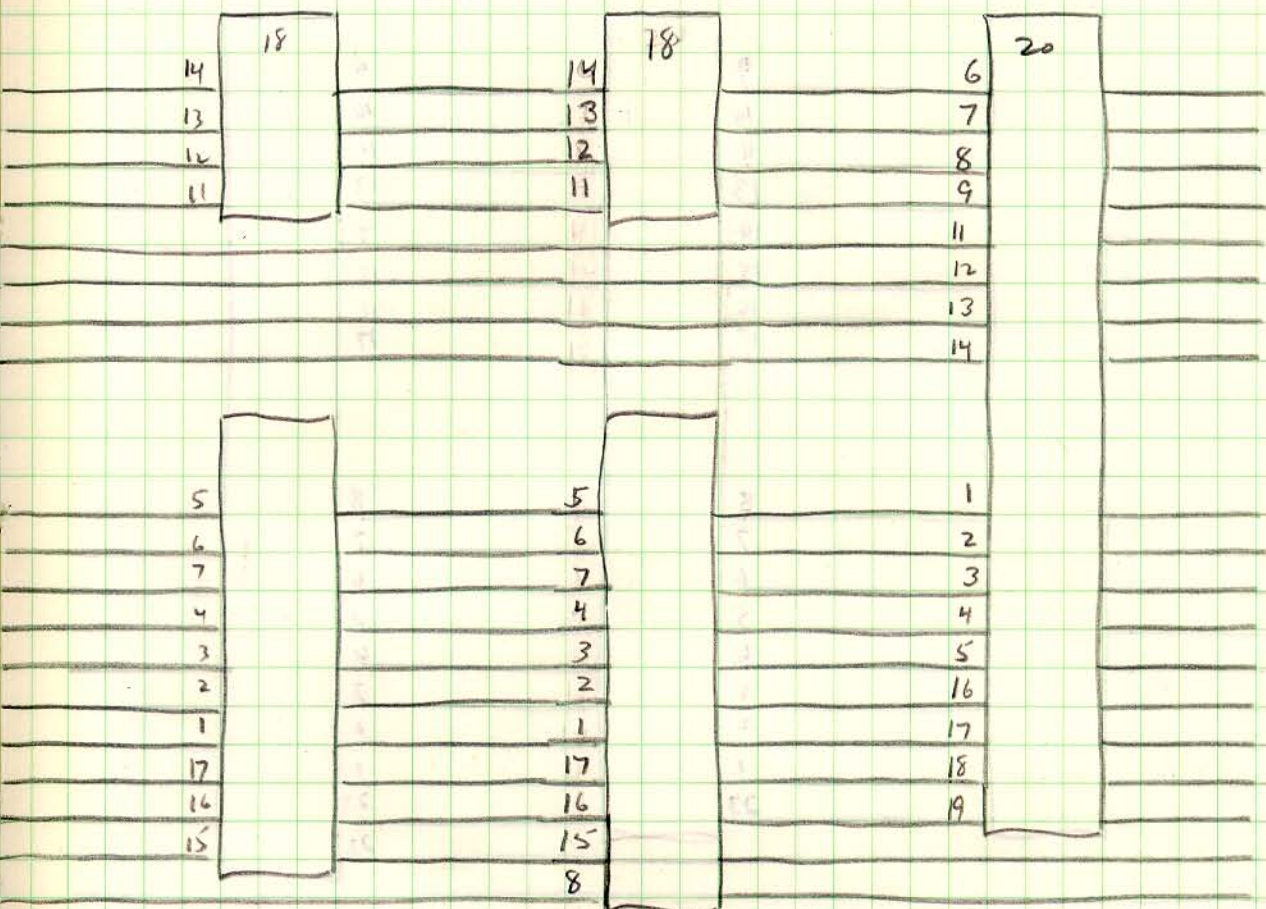
Am 27S12  
Am 27S13



C7  
1024x4

C6  
2048x4

C9  
512x8



Am27532  
Am27533

Am275184  
Am275185

Am27528  
Am27529

11 Sept 8  
ABD

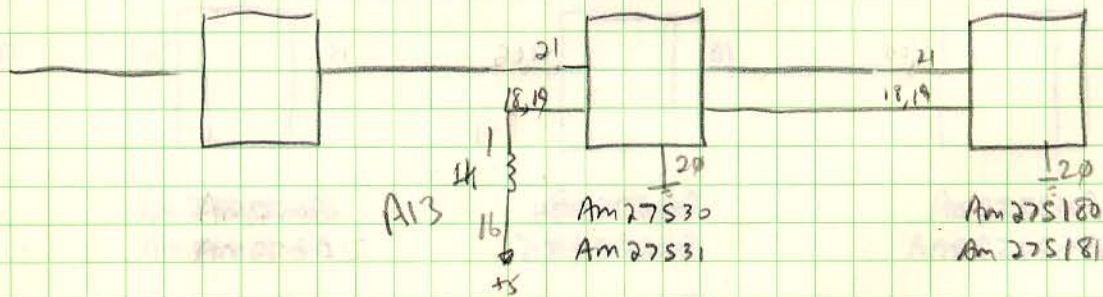
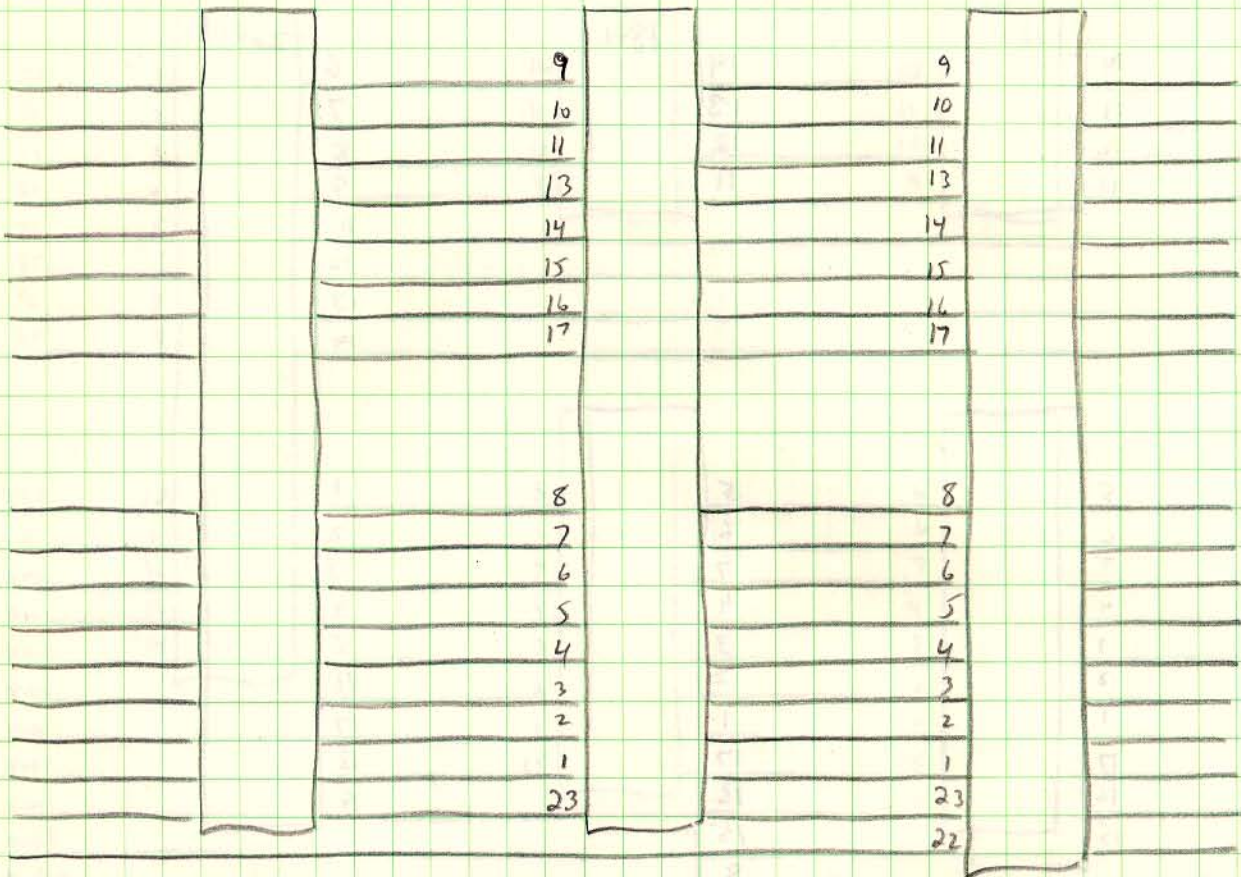


# Atom Socket Wiring

C11  
512x8

C12  
512x8

C14  
1024x8







PROM PROGRAMMER

POWER

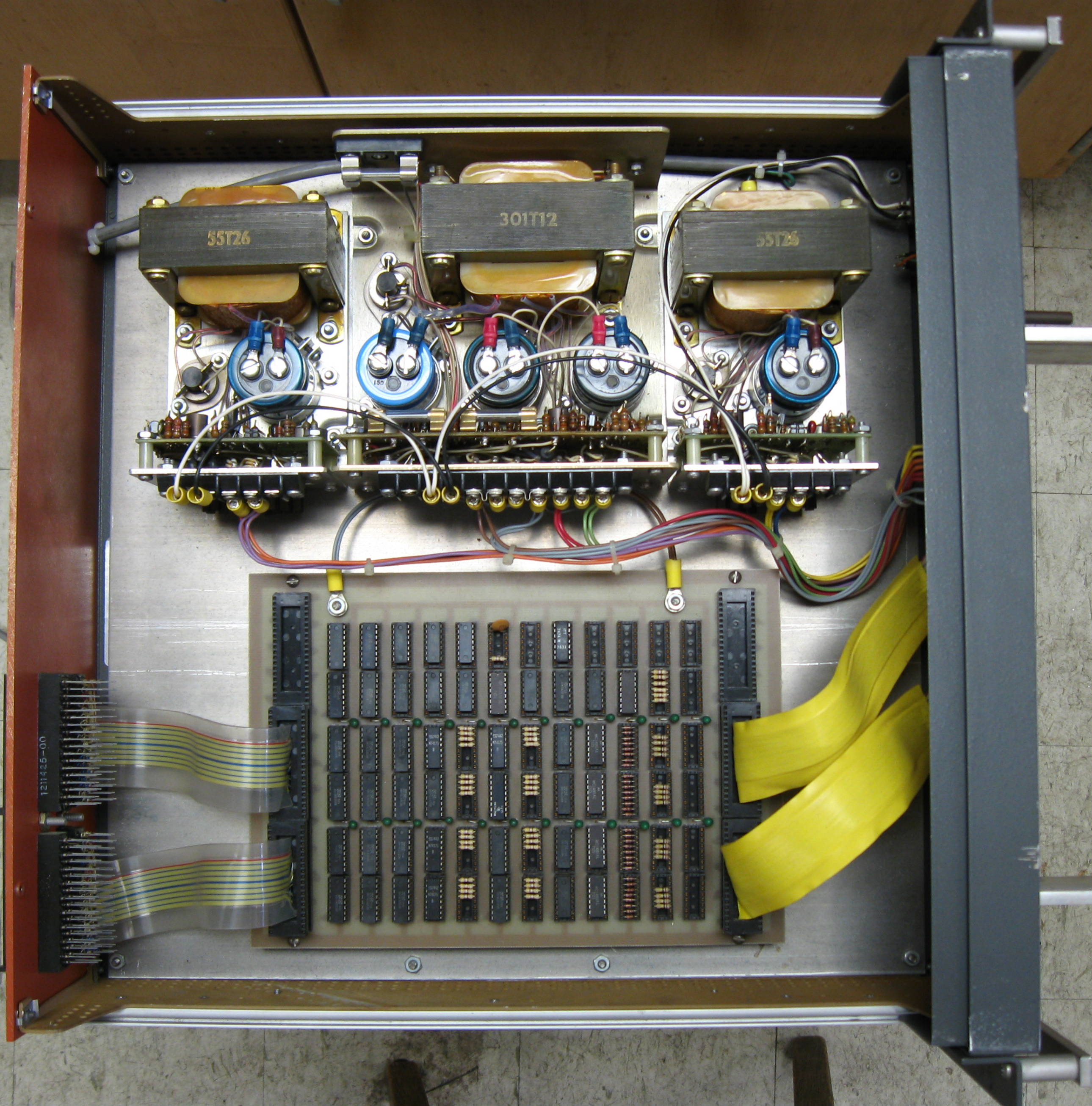
ON





TO:  
ALL SIZE  
BOXES





55T26

301T12

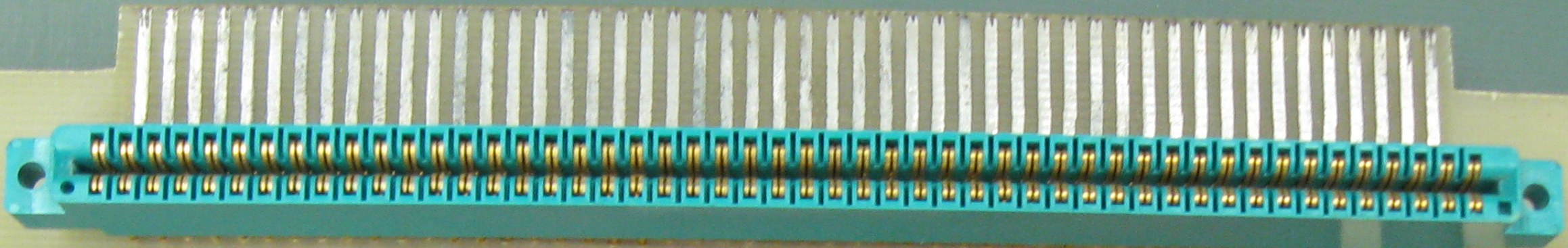
55T26

1211455-00







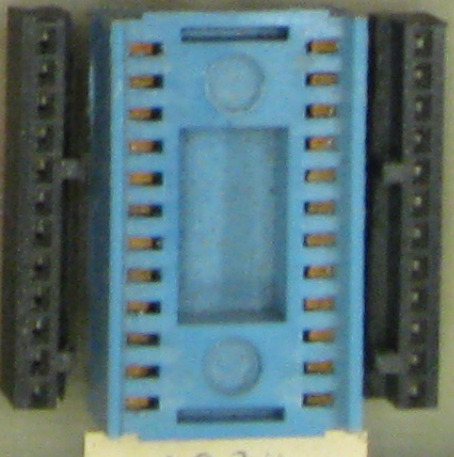
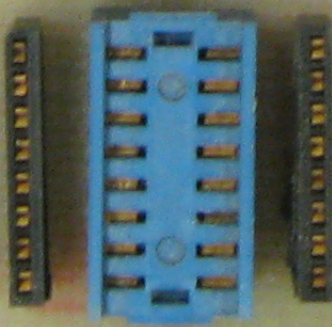
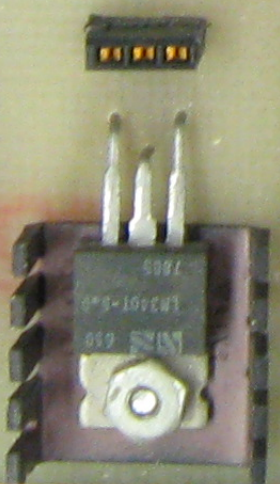
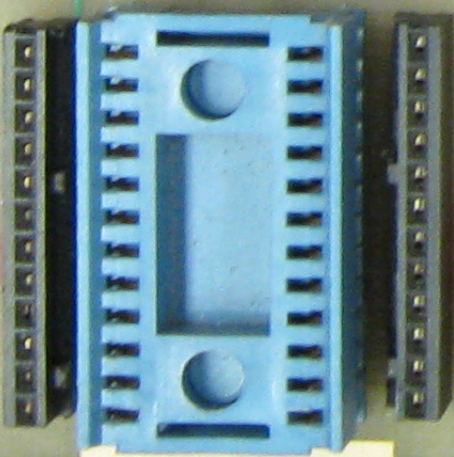
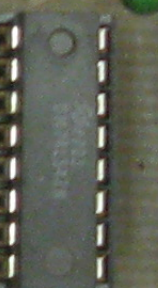
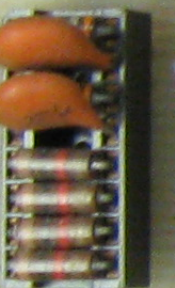
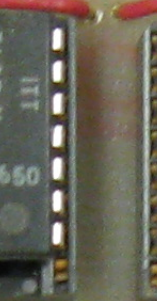
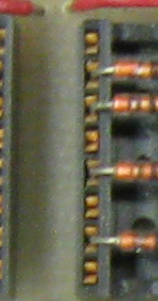
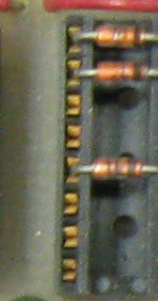
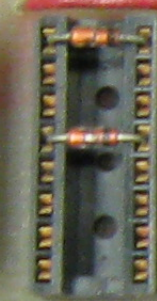


CARD # 0

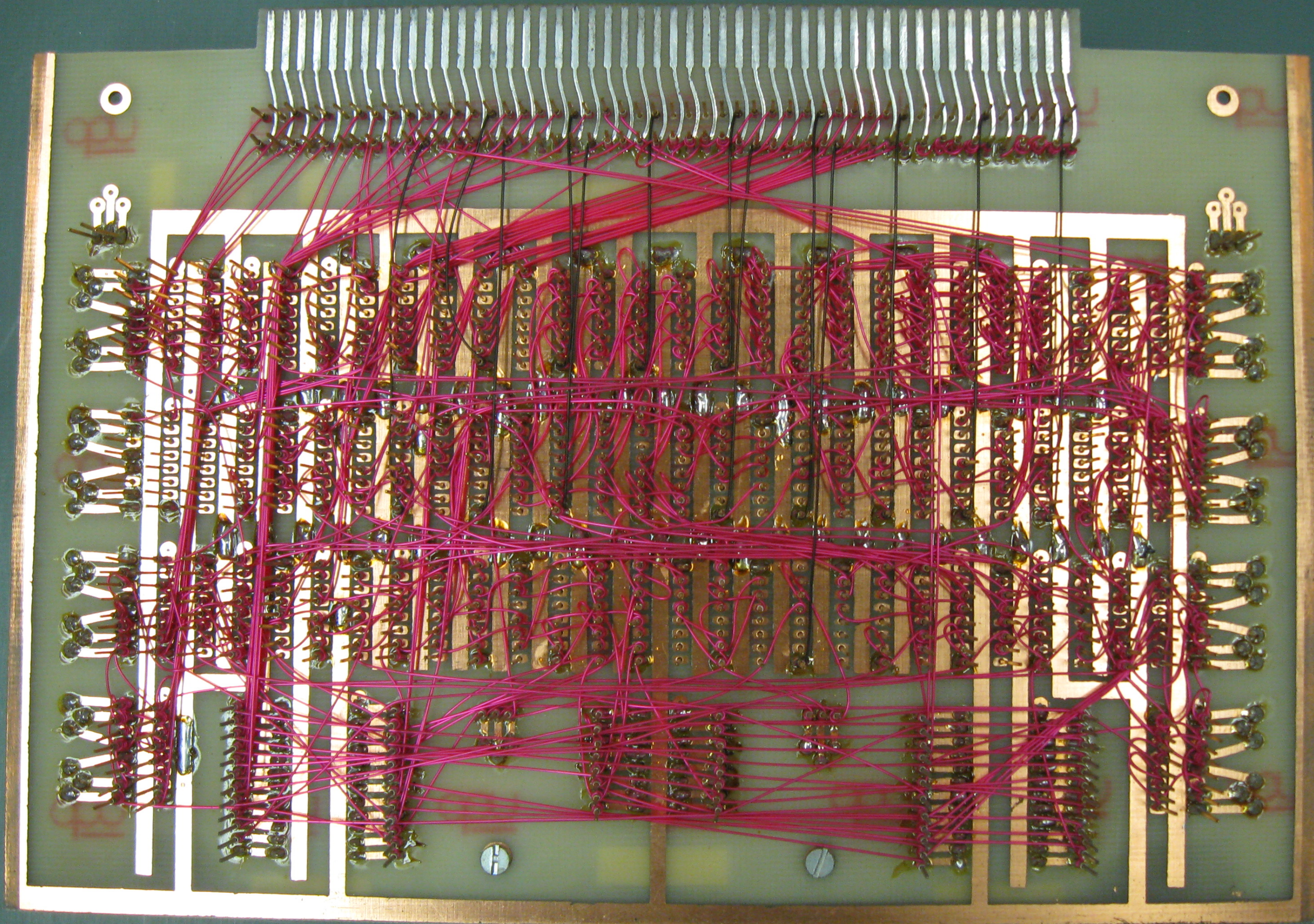
5V 2716

6834

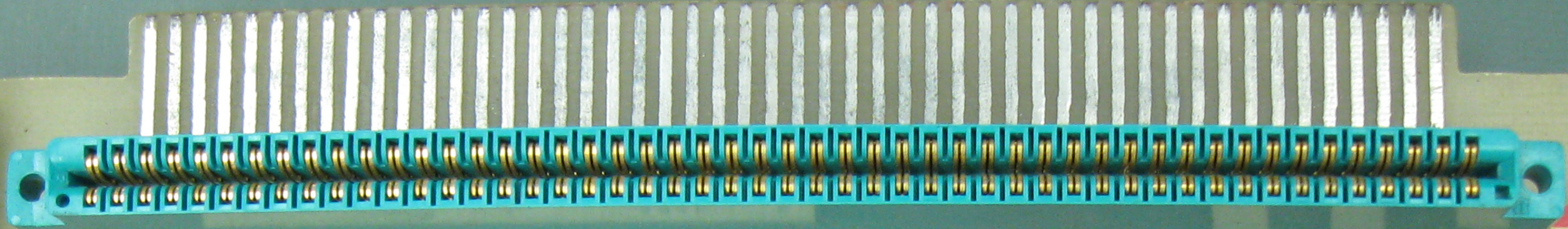
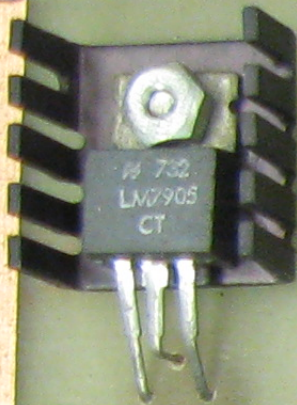
74S387











ON 12V OFF

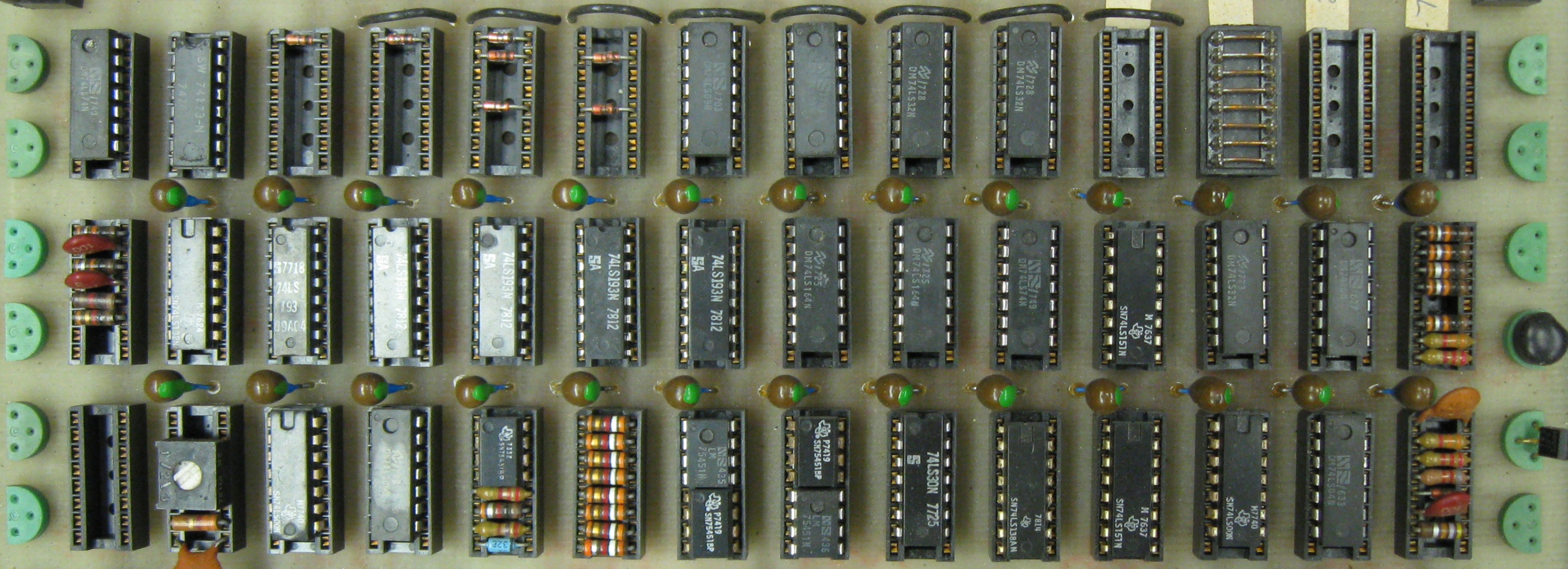
Card #1 IS, +12 2704, 2708  
TTL 2716 74188

2716

8072

4072

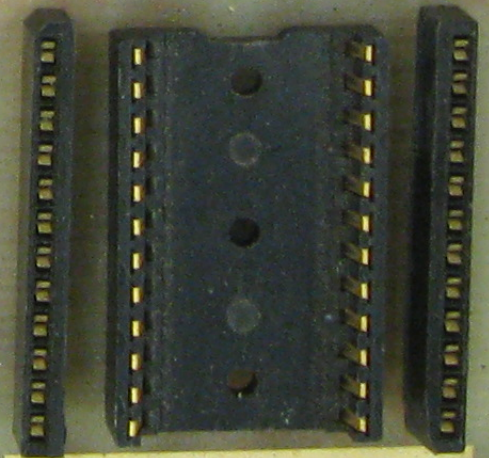
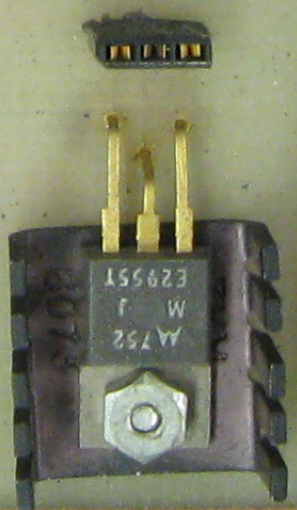
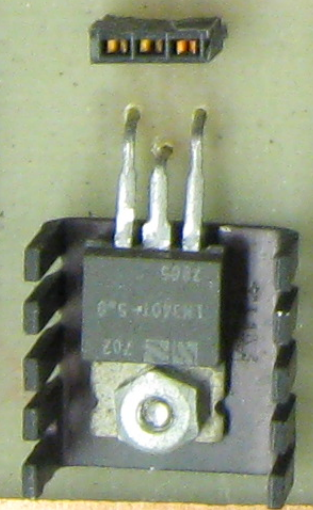
74188



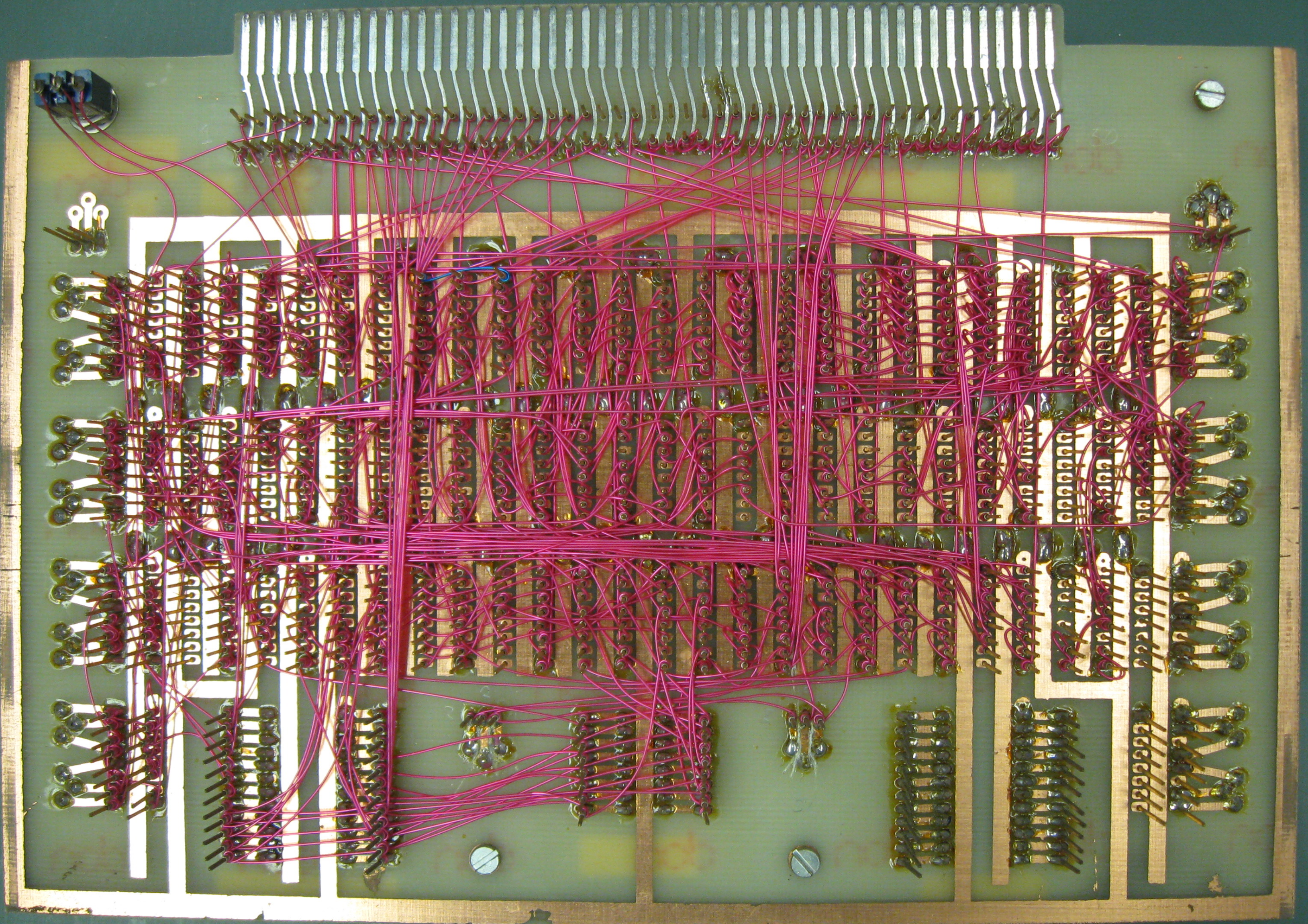
25  
+12 2716

74188

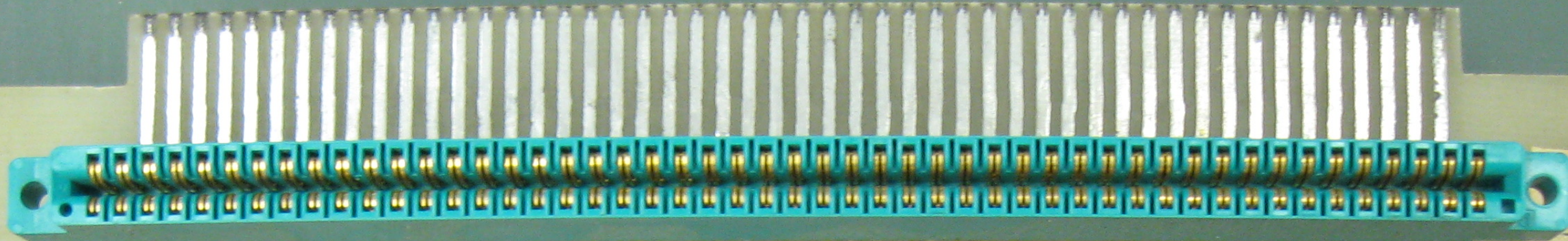
2704/4072









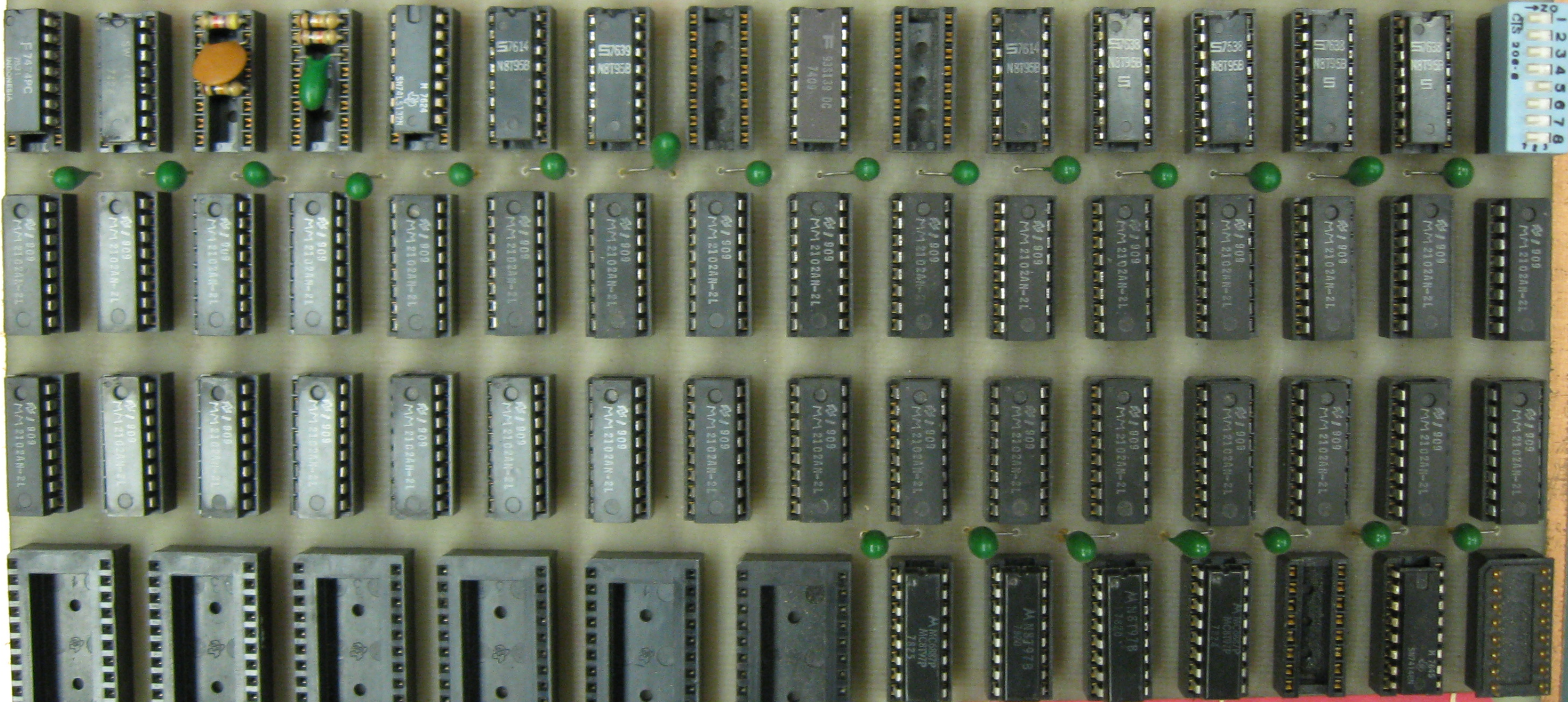


RUN



LOAD

4Kx8 RAM

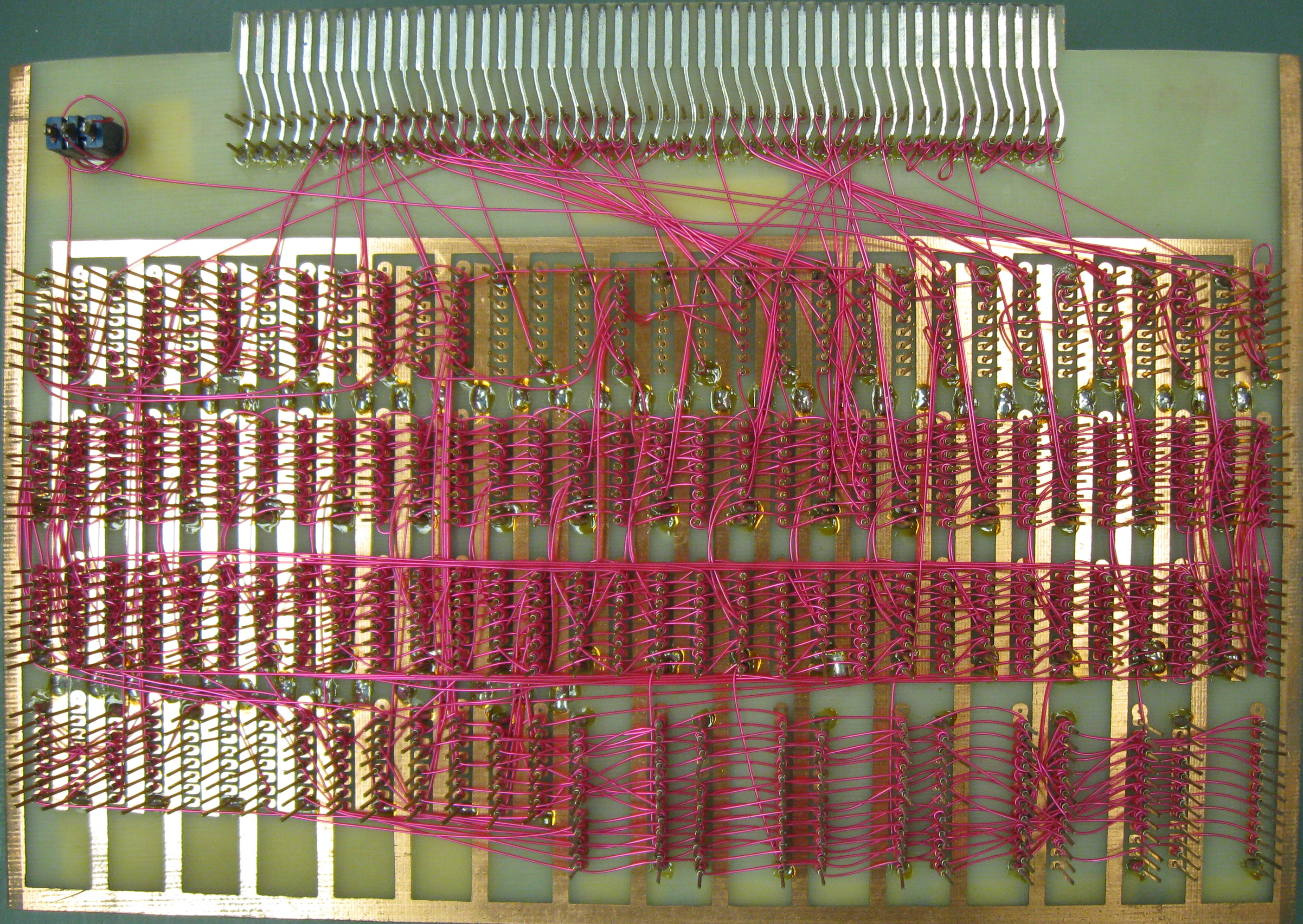


1 2 3 4 5 6 7 8  
↑ ↓  
D5 200-8

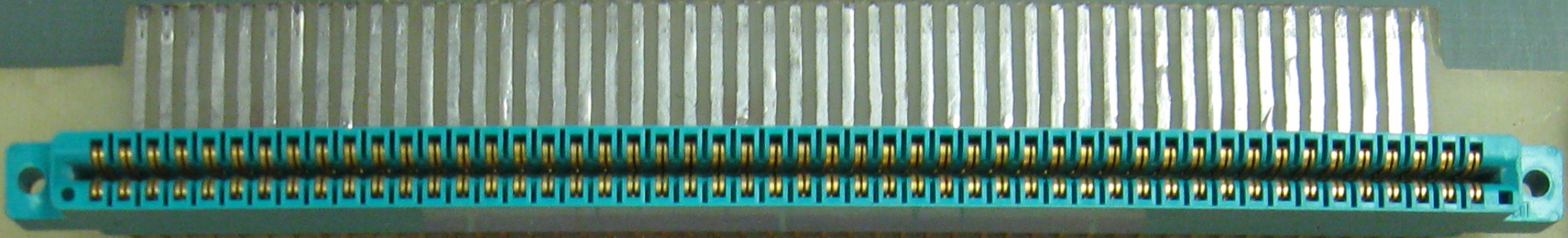
256x8  
512x8  
1Kx8  
2Kx8  
2Kx8  
4Kx8

256 - 8      1K - 6      4K - 4  
512 - 7      2K - 5      SWITCHES

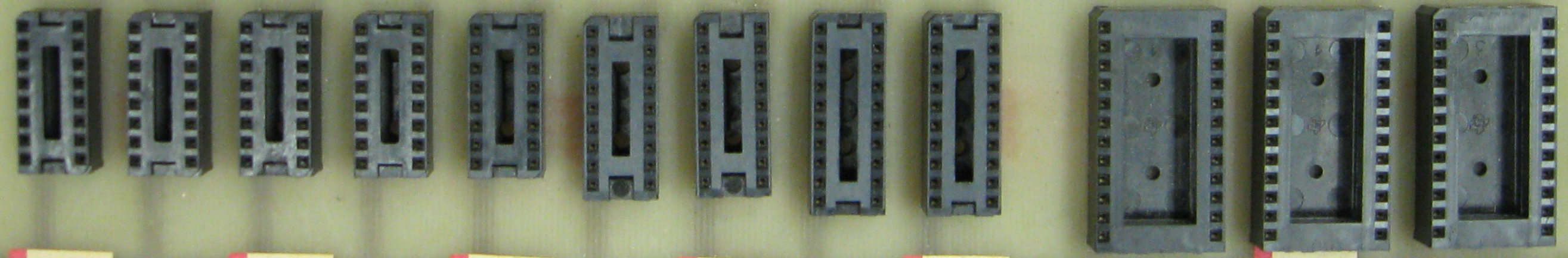
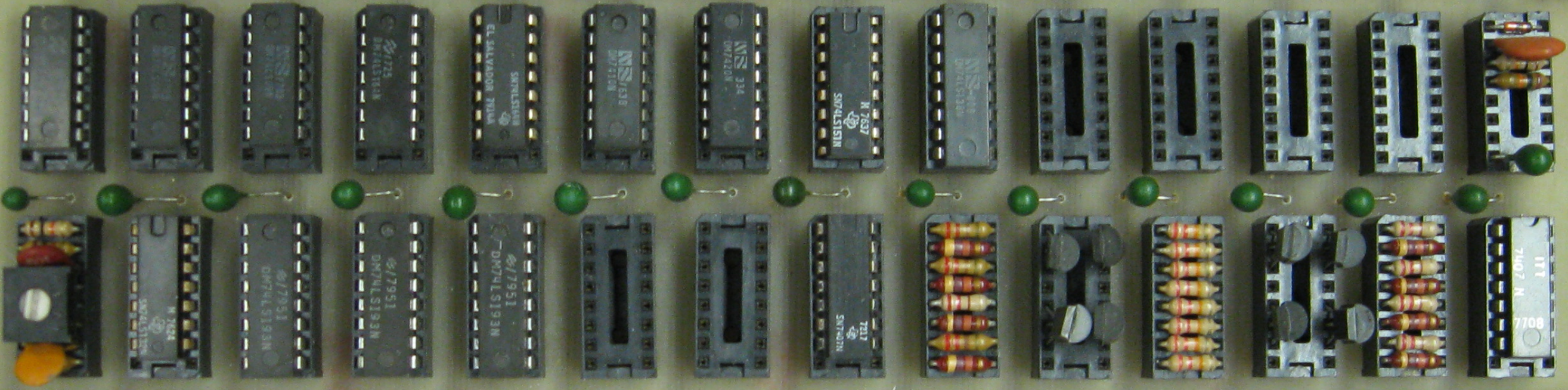
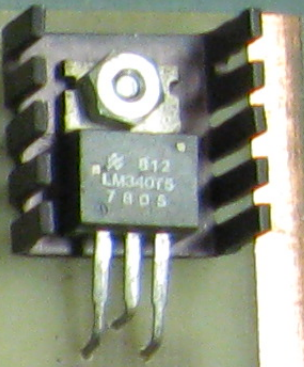








National Semiconductor  
Bipolar PROM Programmer



S188/S288

S287/S387

S570/S571

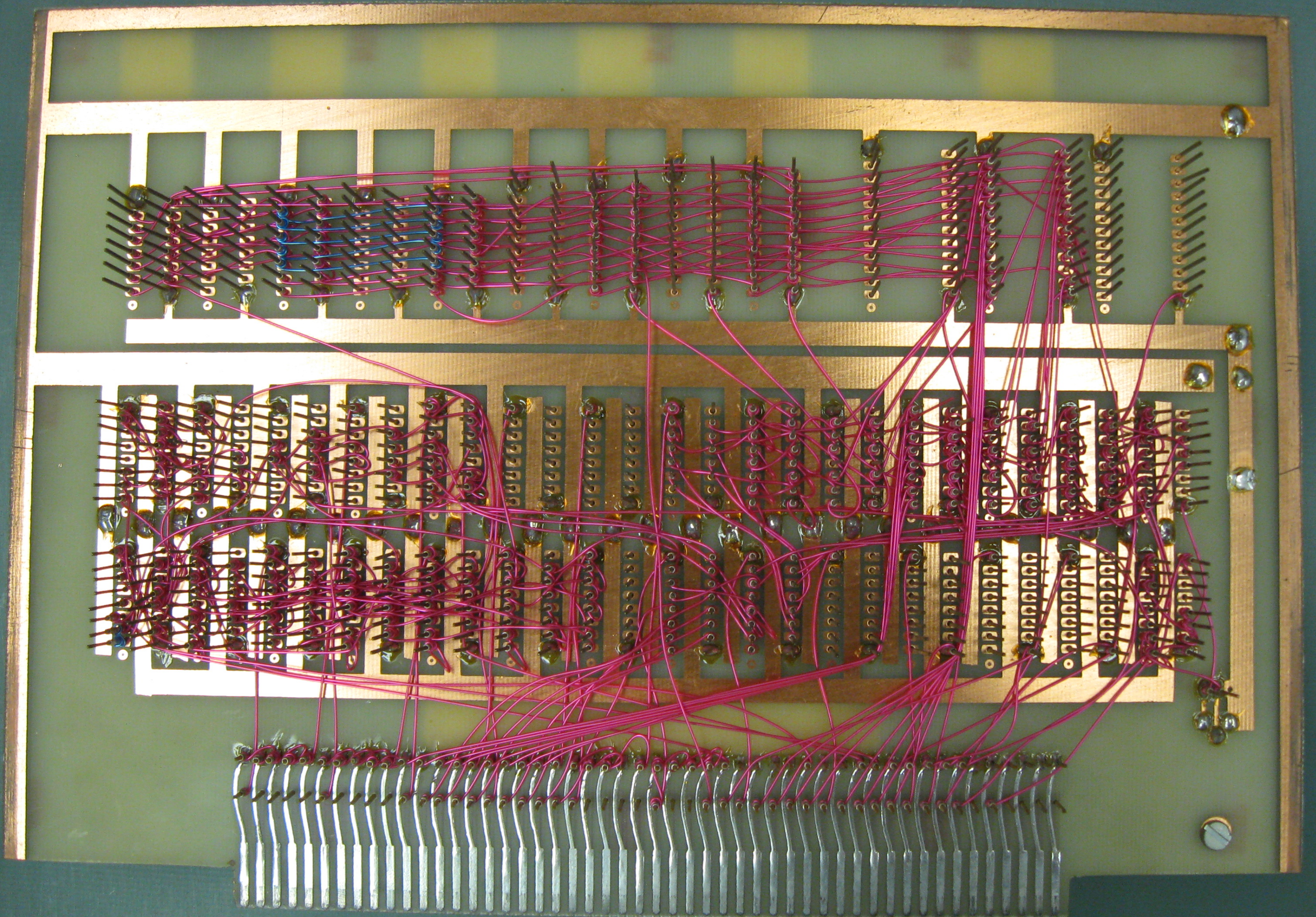
S572/S573

S472/S473

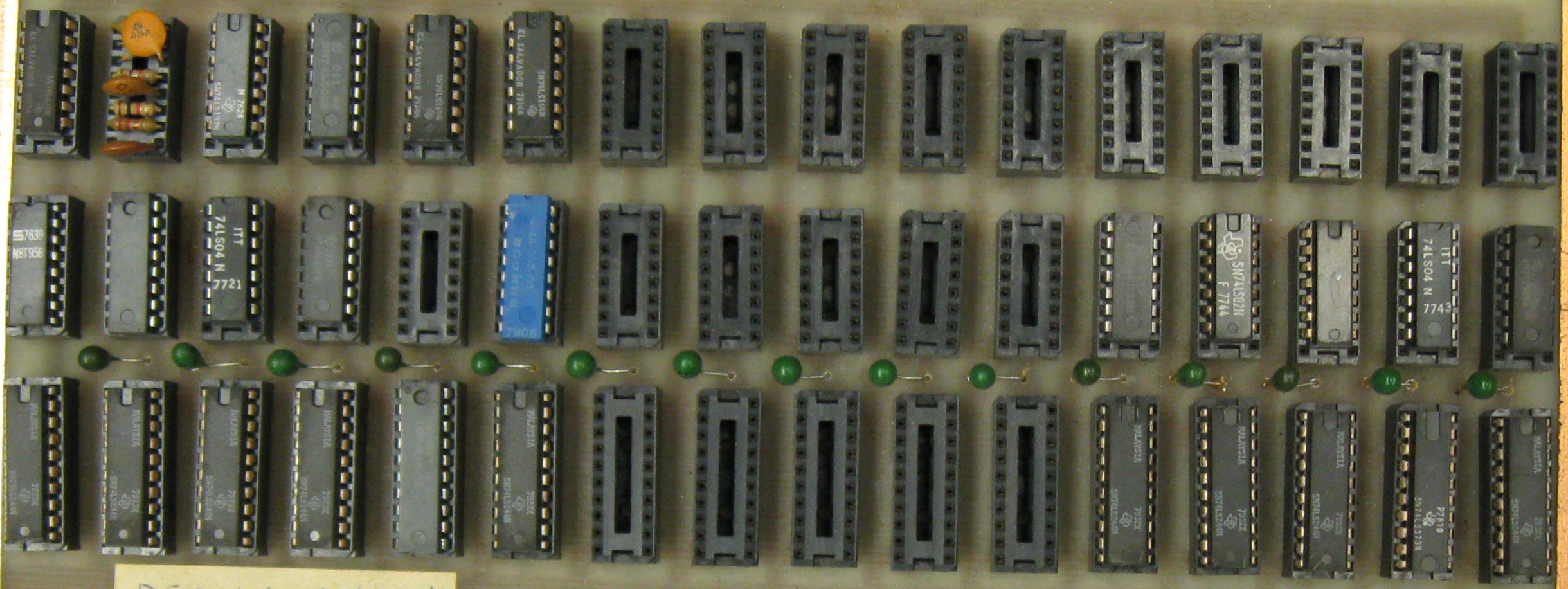
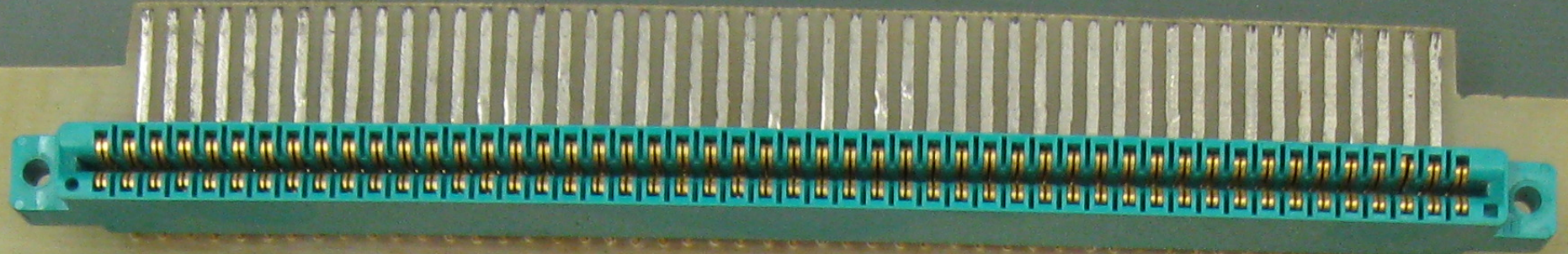
S474/S475



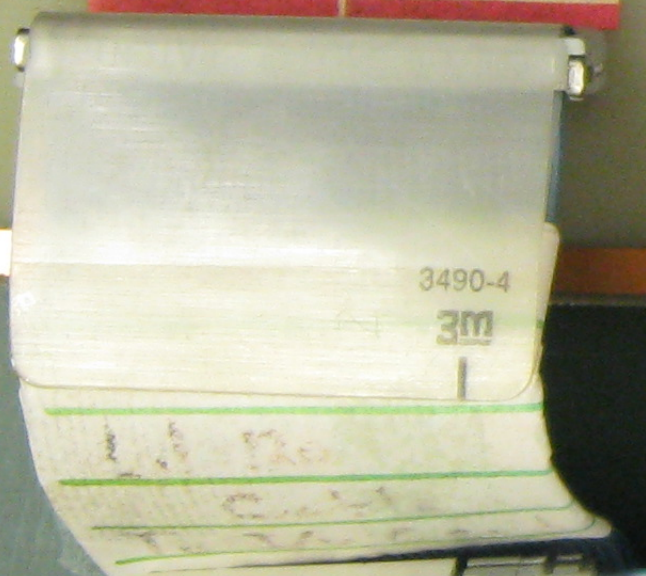




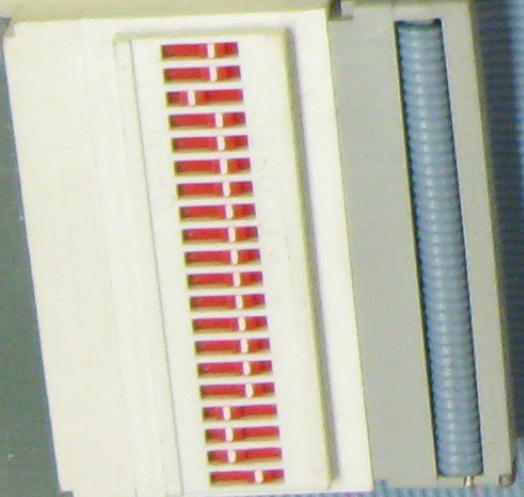




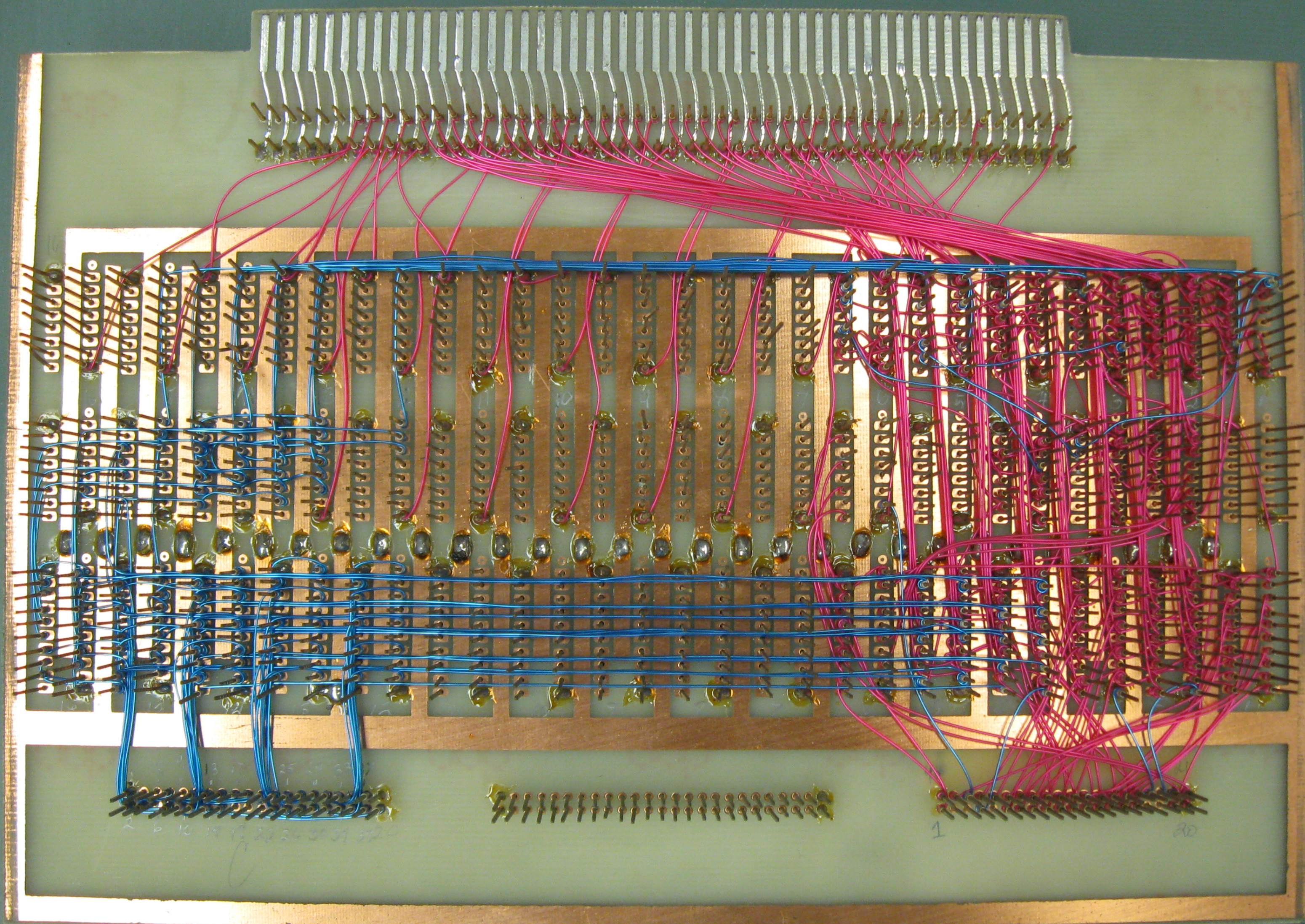
DEC LA-120 ↓



LA-120  
Cable  
To LA-120





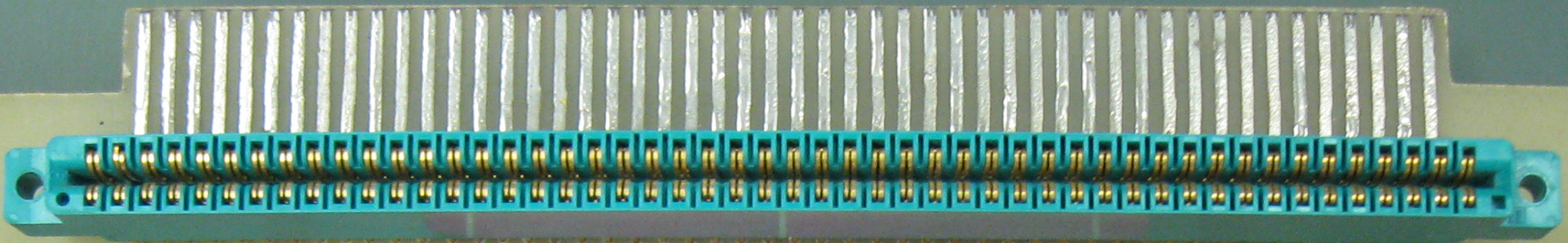


2 6 10 14 18 22 26 30 34 38

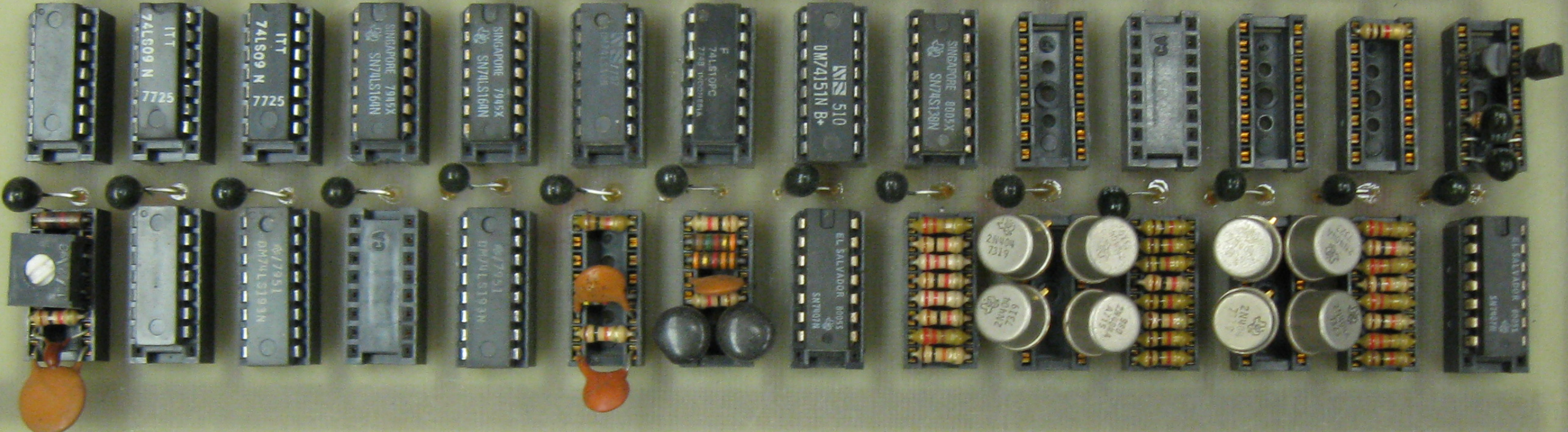
1

20





ADVANCED MICRO DEVICES  
Generic PROM Programming Board



Am 27S18/19  
32 x 8

Am 27S20/21  
256 x 4

Am 27S12/13  
512 x 4

Am 27S15/16  
2048 x 4

Am 27S32/33  
1024 x 4

Am 27S28/29  
512 x 8

Am 27S30/31  
512 x 8

Am 27S180/181  
1024 x 8



