Dual Cassett Tape Syster

Jan 1979

NATIONAL

53-110

Made in U.S.A.

Dual Cassette Controller

An emulation of The DEC TA11 Cassette System

Recording Medium	.150" wide 1 mil modified Dorado cassette (reflective leader)
Recording Type	Ratio mode / Blocked
Capacity	~ 50 K bytes (200 ft tape)
transfer rate	800 bytes/sec average
format	Variable block length 1–N bytes
recording density	225 BPI
Drive	direct (clutch controlled)
Read/write Speed	30 ips
Rewind	30 ips
Latency (Transfer Request)	1.2 milliseconds

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Controller Command Descriptions

Write File Gap

WFG writes a length of blank tape that is used to seperate files. Normally, 375 ms. of blank tape is written, at BOT 689 ms of tape is written for Load point gap.

Normal WFG
1. program issues WFG and GO
2. ready cleared
3. tape written, ready set

Abnormal WFG
a. WFG on write protected
1. program issues; WFG and GO
2. ready cleared
3. Ready set ; Error set

b. WFG at EOT
1 program issues WFG and GO
2 ready cleared, motion initiated
3. 10 ms later, Ready set, Error set

c. WFG enters EOT
1. program issues WFG and GO
2. ready cleared, motion initiated
3. aborts to EOT, ready set, Error set

Write

records data as bytes of data on tape. # of bytes is program controlled.

Normal Write
1. program issues Write and GO
2. clears ready, initials tape motion, sets Transfer Request
3. programs responds to TR by loading data into TADO, TR cleared
4. data is transferred to the cassette TR set again
5. steps 3 & 4 repeated N times for an N byte Block

6. stand if transfer ILBS is set by program
7. TR deased, CRC written, tape stopped, Ready set

Abnormal Write Sequences

a. Write at BOT
   1. program issues Write and GO
   2. if clear leader, a WFG is executed
   3. normal Write now performed

b. Write on protected cassette
   1. program issues write and GO
   2. clears ready
   3. ready set with Error

c. Write from EOT:
   1. program issues write and GO
   2. clears ready
   3. WFG executed
   4. upon error - set ready & Error

d. Write enters EOT
   1. assume Write in progress
   2. tape enters EOT
   3. ready set with Error

e. Write with timing error
   1. Assume Write in progress
   2. NO response to TR within 500 μsec
   3. CRC & Block gap written
   4. ready set, Error & Timing Error

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READ

the read function is used to recover a block of data that was previously written on the tape. To assure proper cyclical redundancy checking, the program must know the number of bytes written in the block. Block Check Error will normally result if the program issues ILBS at the wrong time.

Normal Read

1. program issues Read & GO
2. clears ready, start tape
3. TR set when byte of data available
4. program reads byte, clearing TR
5. steps 3 & 4 repeat N times for an N byte block
6. after the Nth byte is read, at next TR set ILBS
7. controller clears TR and check CRC. when finished ready is set, if BlockCHECH then ERROR is set

Abnormal Read

a. Read enters EOT

1. Normal Read in progress
2. Tape enters EOT
3. Read, set, motion stopped, ERROR set

b. Read Blank tape or Beginning of a file gap

1. Program issues Read & GO
2. removes ready
3. No data within 150ms, ready set, File Gap, ERROR

c. Read from BOT

1. program issues Read & GO
2. removes ready, initiates tape motion
3. tape moved off BOT - proceeds to search for Data
4. continues with normal read

d. Read with Timing Error

1. Normal read in progress
2. No response to TR within 500 μsec
3. tape stops in gap, ready set, Error and Timing Error

Space Reverse File (SRF)

SRF is used to move the tape in reverse into the preceding file gap. previously written data must be encountered before the transport begins to look for the blank tape of a file gap.

Normal SRF

1. Program issues SRF & GO
2. ready removed, tape motion
3. when positioned, ready set with File gap

Abnormal Sequence – SRF enters BOT or at clear leader

1. program issues SRF & GO
2. when clear leader detected sets Ready, Error

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SPACE Reverse BLOCK (SRB)

SRB is used to move the tape in reverse into the preceding block gap. Previously written data must be encountered before search for blank tape in gap is initiated.

Normal SRB

1. Program issues SRB & GO
2. clear ready, tape motion
3. when positioned at previous block gap, Ready sets

Abnormal SRB - ends in BOT or at BOT

1. program issues SRB & GO
2. when clear leader detected, Ready & Error set

Space Forward File (SFF)

SFF is used to advance the tape to the next file gap. In contrast to SRF, SFF does not look for data prior to looking for the blank tape of the file gap (except for BOT); therefore SFF and SRF are not symmetrical functions. In addition, this implies that if SFF is issued at the beginning of a file gap, a FILE GAP indication will result in the same gap.

Normal SFF

1. Program issues SFF and GO
2. clears ready, tape motion
3. when file gap detected, Ready and FILE GAP set

Abnormal SFF

a. SFF from BOT
   1. Program issues SFF and Go
   2. clears ready, tape motion
   3. moved off BOT, read until data found
   4. when gap detected, Ready & FILE GAP set

b. SFF from EOT; SFF enters EOT
   1. program issues SFF and Go
   2. clears ready, tape motion
   3. when clear leader detected, Ready Error set

SPACE FORWARD BLOCK (SFB)

SFB is used to advance the tape to the next block gap. In contrast to SRB, SFB does not look for data prior to looking for the block gap (except at BOT); therefore, if SFB is initiated at the beginning of a FILE GAP, a FILE GAP indication will occur in the same gap. SFB is a READ will go Transfer Requests.

Normal SFB

1. Program issues SFB & GO
2. clears ready, tape motion
3. when gap detected, Ready & BLOCK Check set

Abnormal SFB

a. SFB from BOT
   1. program issues SFB & GO
   2. clears ready, tape motion
   3. reads past load point gap & to data
   4. at gap sets Ready, BLock CHECK

b. SFB fm EOT, or enters EOT
   1. program issues SFB & GO
   2. clears ready,
   3. clear leader detected, sets Ready, Error

c. SFB enters File Gap
   1. program issues SFB & GO
   2. clears ready, tape motion
   3. when file gap detected, Ready, Error, File GAP

FUNC

0 –

1 –

2 –

REWIND

Rewind is used to position tape at BOT.

3 –

Normal REWIND

4 –

1. Program issues REWIND & GO
2. clear ready, tape motion
3. clear leader, Ready set

5 –

6 –

OFFLINE

7 –

Status if no cassette in drive

NORMAL VS. ERROR STATUS Conditions

FUNCTION	POSSIBLE NORMAL INDICATOR, ERROR = Ø	POSSIBL ERROR INDICATORS ERROR = 1
Ø - WFG	NONE	Write Lock Clear Leader OFF-Line
1 - Write	NONE	Write Lock clear leader Timing error off-line
2 - Read	NONE	clear leader File gap Timing error Block check off line
3 - SRF	File Gap	Clear Leader off line
4 - SRB	None	clear leader off line
5 - SFF	File Gap	Clear leader off line
6 - SFB	Block Check	File Gap Clear leader off-line
7 - Rewind	Clear Lieader	off line

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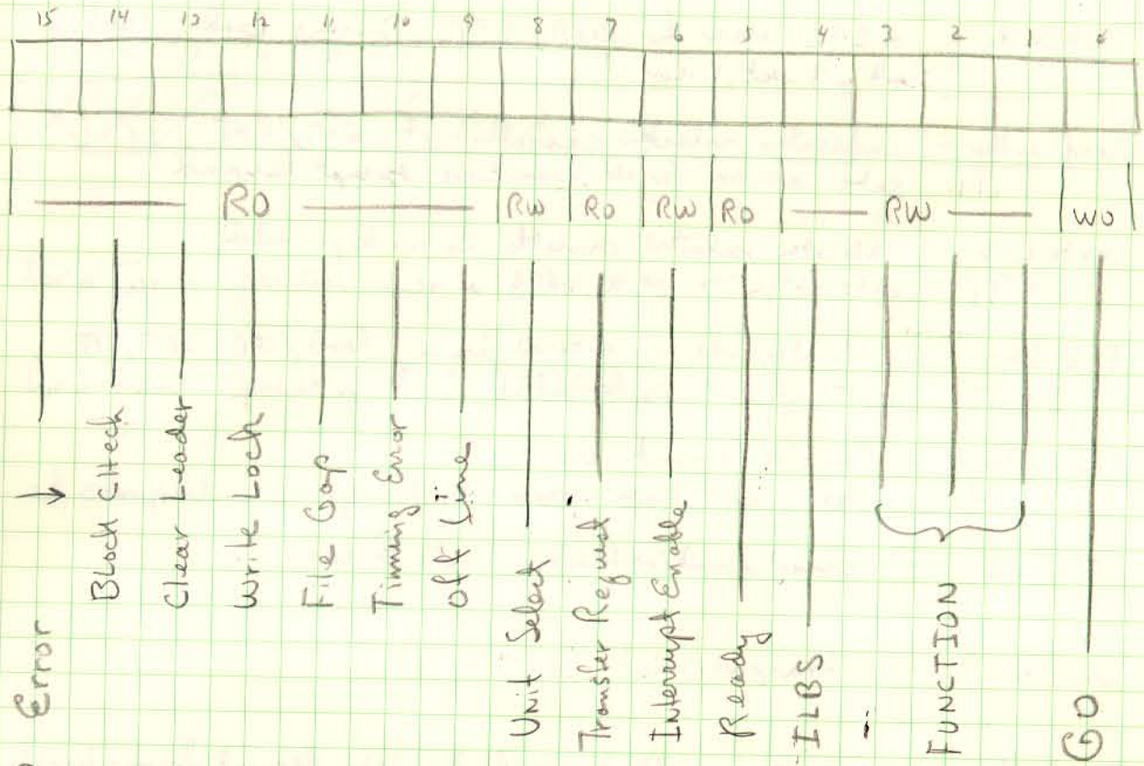
Register / Vector Addresses

CSR – Control & Status Register — 777500_8

DBR – Data Buffer Register — 777502_8

Vector Address – 260_8

Command and Status Register 777500_8



Functions

0	Write file Gap
1	Write
2	Read
3	Space Rev file
4	Space Rev Block
5	Space forward file
6	Space forward Block
7	Rewind

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Bit

15 ERROR - an error condition from (14:08) and current function (03:01)
Error valid only when Ready set

14 Block Check - a CRC error for Read / SFB, During Read, Block check will set Error

13 Clear Leader - indicates selected cassette at EOT / BOT
sets error for all functions except Rewind

12 Write Lock - indicates selected cassette is write protected
sets Error on Write, WFG

11 File Gap - indicates file gap entered during Read / SFB / SRF / SFF
sets Error on Read / SFA

10 Timing Error - Transfer Request error
sets error in Read / Write

9 OFF-Line - cassette not installed sets Error

8 Unit select - transport select 0, 1

7 Transfer Request - data available during Read, data Request during Write
cleared by init and addressing TADA, held clear by ILBS

6 interrupt enable - enables Ready or Transfer request to interrupt
cleared by init

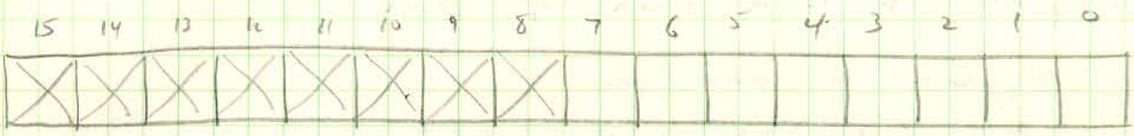
5 Ready - Controller ready / operation complete

4 ILBS - initiate Last Byte sequence - transport reads CRC on Read, writes CRC on write

3-1 Function

0 GO - initiate selected operation

Cassette Data Buffer Register 777502_8



for a write operation Write data into Buffer upon TR = 1

for a read operation Read data from Buffer upon TR = 1

at completion of operation - Error code may be present

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Turning NOTES:

WFG - File gap is 375 ms

File gap detected if 110 ms blank tape found

Block gap is 1.2 ms blank tape

SRB - Block gap detected 1.2 ms after lost data found

Logic Drawings

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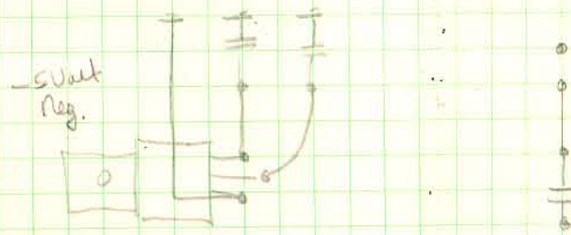
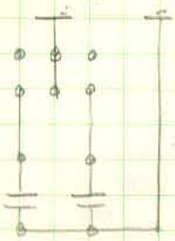
Ports Layout



	1	2	3	4	5	6	7	8	9	10	11	12	13
A	RES	3140 / 3140	LS132	LS191	LS191								
B	LS74	LS74 X	RES	LS74	LS74								
C	LS51	LS08	RES 10M	LS153	LS00	LS193	LS00	LS193	LS74	LS193	X	LS193	X
D	68B21	68B21	68B21	68B00	7433	RES	LS132	LS74	Res	RES			LS138
E					27A08		27A08	27A08		68B10			LS374
F	CN1									CN3		SW	LS244
	CN2									CN4			



20	21	22	23	24	
LS74	LS193	LS193	LS193	SW	A
LS74	LS193	LS193	RES	SW	B

13	14	15	16	17	18	19					
X	X	LS00	LS11	LS08	LS173	LS173	LS04	LS02	LS02	LS139	LS00	C
LS138	LS138	LS175	LS74	LS74	LS158	RES	74S74	74S74	LS08	8136	RES	D
LS374	LS374	8838	8838	8838	8838	7438	7438	8837	8837	8136	SW	E
LS244	LS244	CN5				CN6				8136	SW	F

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Transport Control Connectors

CN1 Transport 0 Control (J10)

1	Rewind [L]	– C3/1	16			
2	Write Enabled [H]	– D1/16	15			
3	Cassette in Place [H]	– D1/15	14			
4	Switch Common	–	13			
5	Allow Write	– D1/12	12			
6	Forward [L]	– D1/10	11	Read Phase	– C4/10	
7	Write Data	– CN2/7 C13/5	10	Reverse [L]	– C2/3	
8	Clear Leader [L]	– D1/17	9	Read Data	– C4/6	

CN2 Transport 1 Control (J10)

1	Rewind [L]	– C3/4	16			
2	Write Enable [H]	– D3/16	15			
3	Cassette in Place	– D3/15	14			
4	Switch Common	–	13			
5	Allow Write	– D3/12	12			
6	Forward [L]	– D3/10	11	Read Phase	– C4/11	
7	Write Data	– CN1/7	10	Reverse [L]	– C2/6	
8	Clear Leader [L]	– D3/17	9	Read Data	– C4/5	

CN3 Panel Switch Connector

	T0				T1		
1	LED +5	–	+5	16	LED +5	–	+5
2	SW/LED	–		15	SW/LED	–	
3	SW	–	GND	14	SW	–	GND
4				13			
5				12			
6				11			
7				10			
8				9			

CN4

1		
2		15
3		14
4		13
5		12
6		11
7		10
8		9

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UNIBUS INTERConnect CABLE

CN5

1	DØØ L	+	E15/1	40	GND	1
2	DØ1 L	+	E15/4			2
3	DØ2 L	+	E15/12	39	INIT L +	3
4	DØ3 L	+	E15/15	38	INTR L +	4
				37	+5 BUS IN −	
5	GND			36	+5 Bus out + E15/16	5
6	DØ4 L	+	E16/1	35	GND	6
7	DØ5 L	+	E16/4			7
8	DØ6 L	+	E16/12	34	PAL −	8
9	DØ7 L	+	E16/15	33	PBL −	9
				32	+5 Bus out + E16/16	
10	GND			31	BOSY L −	10
11	DØ8 L	+	E17/1	30	GND	11
12	DØ9 L	+	E17/4			12
13	DI1 L	+	E17/12	29	SACK L −	13
14	DI1 L	+	E17/15	28	+5 Bus out + E17/16	14
				27	NPR L	
15	GND			26	NPG H	15
16	DI2 L	+	E18/1	25	GND	16
17	DI3 L	+	E18/4			17
18	DI4 L	+	E18/12	24	BR7 L	18
19	DI5 L	+	E18/15	23	BR6 L	19
				22	BG7 H	
20	GND			21	+5 Bus out + E18/16	20

CN 6

1	AØØ L	+	E22/1
2	AØ1 L	+	E22/5
3	AØ2 L	+	F23/13
4	AØ3 L	+	F23/15
5	GND		
6	AØ4 L	+	F23/5
7	AØ5 L	+	F23/3
8	AØ6 L	+	F23/1
9	AØ7 L	+	E23/11
10	GND		
11	AØ8 L	+	E23/13
12	AØ9 L	+	E23/15
13	A1Ø L	+	E23/5
14	A11 L	+	E23/3
15	GND		
16	A12 L	+	E23/1
17	A13 L	+	D23/11
18	A14 L	+	D23/13
19	A15 L	+	D23/15
20	GND		

40	GND		
39	BG6 H	–	
38	BG5 H	+	
37	BUSG out	+	E2Ø/16
36	BR5 L	+	
35	GND		
34	BR4 L	–	
33	BG4 H	–	
32	ACLO L	–	
31	DCLO L	–	
30	GND		
29	A16 L	+	D23/5
28	A17 L	+	D23/3
27	C1 L	+	E22/15
26	CØ L	+	E22/13
25	GND		
24	BSSYN L	–	
23	+5 BUS out	+	E22/16
22	+5 BUS out	+	E21/16
21	BMSYN L	+	D23/1

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UNIBUS Connector

A Block Side 1

A1	INIT L
B1	INTR L
C1	DØ0 L
D1	DØ2 L
E1	DØ4 L
F1	DØ6 L
H1	DØ8 L
J1	D10 L
K1	D12 L
L1	D14 L
M1	PA L
N1	GND
P1	GND
R1	GND
S1	GND
T1	GND
U1	NPGH
V1	BG7H

A Block Side 2

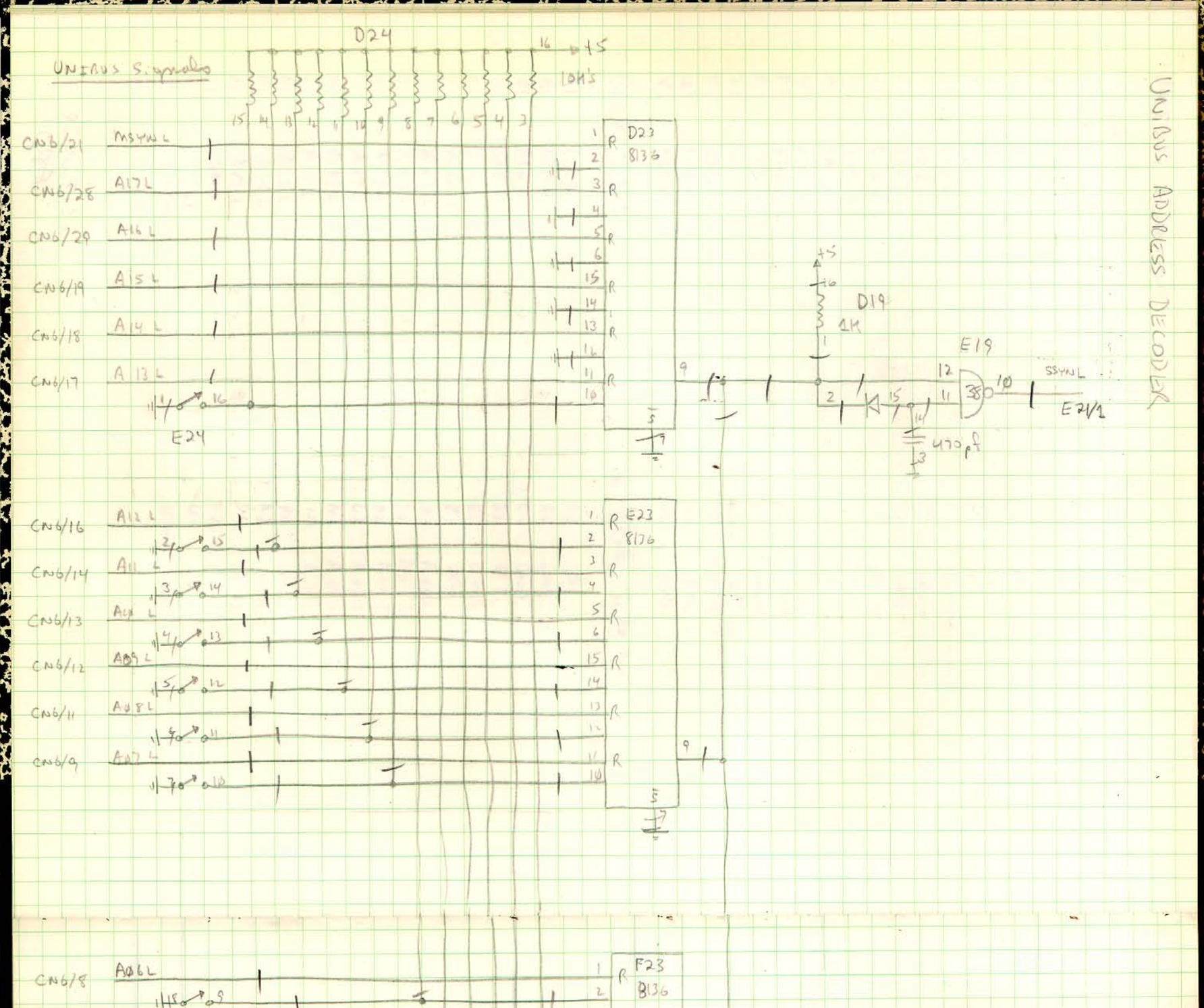
A2	+5
B2	GND
C2	GND
D2	DØ1 L
E2	DØ3 L
F2	DØ5 L
H2	DØ7 L
J2	DØ9 L
K2	D11 L
L2	D13 L
M2	D15 L
N2	PBL
P2	BØSY L
R2	SACK L
S2	NPR L
T2	BR7 L
U2	BR6 L
V2	GND

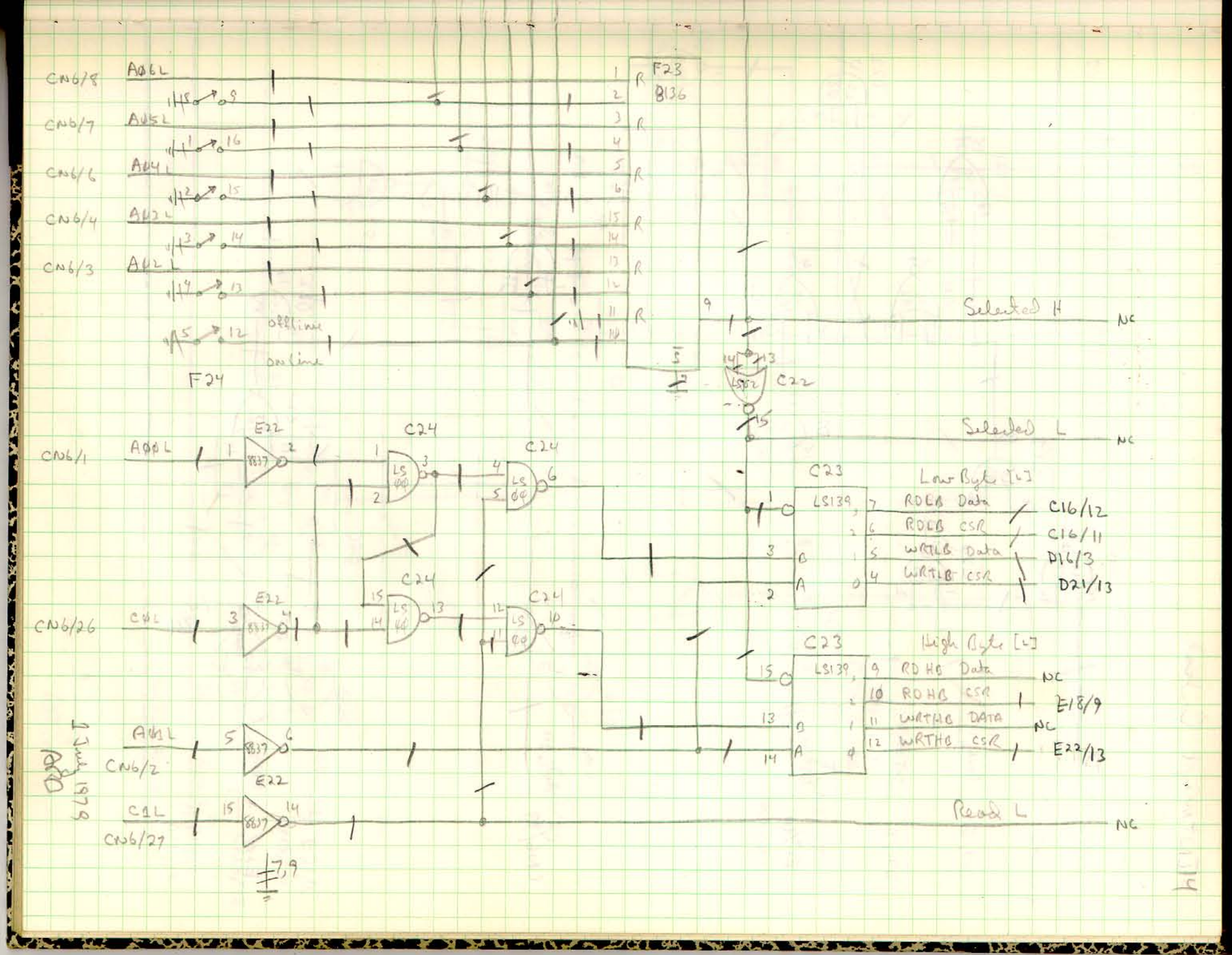
B Block Side 1

A1	BG6H
B1	BG5H
C1	BR5 L
D1	GND
E1	GND
F1	ACLO L
H1	AØ1 L
J1	AØ3 L
K1	AØ5 L
L1	AØ7 L
M1	AØ9 L
N1	A11 L
P1	A13 L
R1	A15 L
S1	A17 L
T1	GND
U1	SSYNL
V1	MSYNL

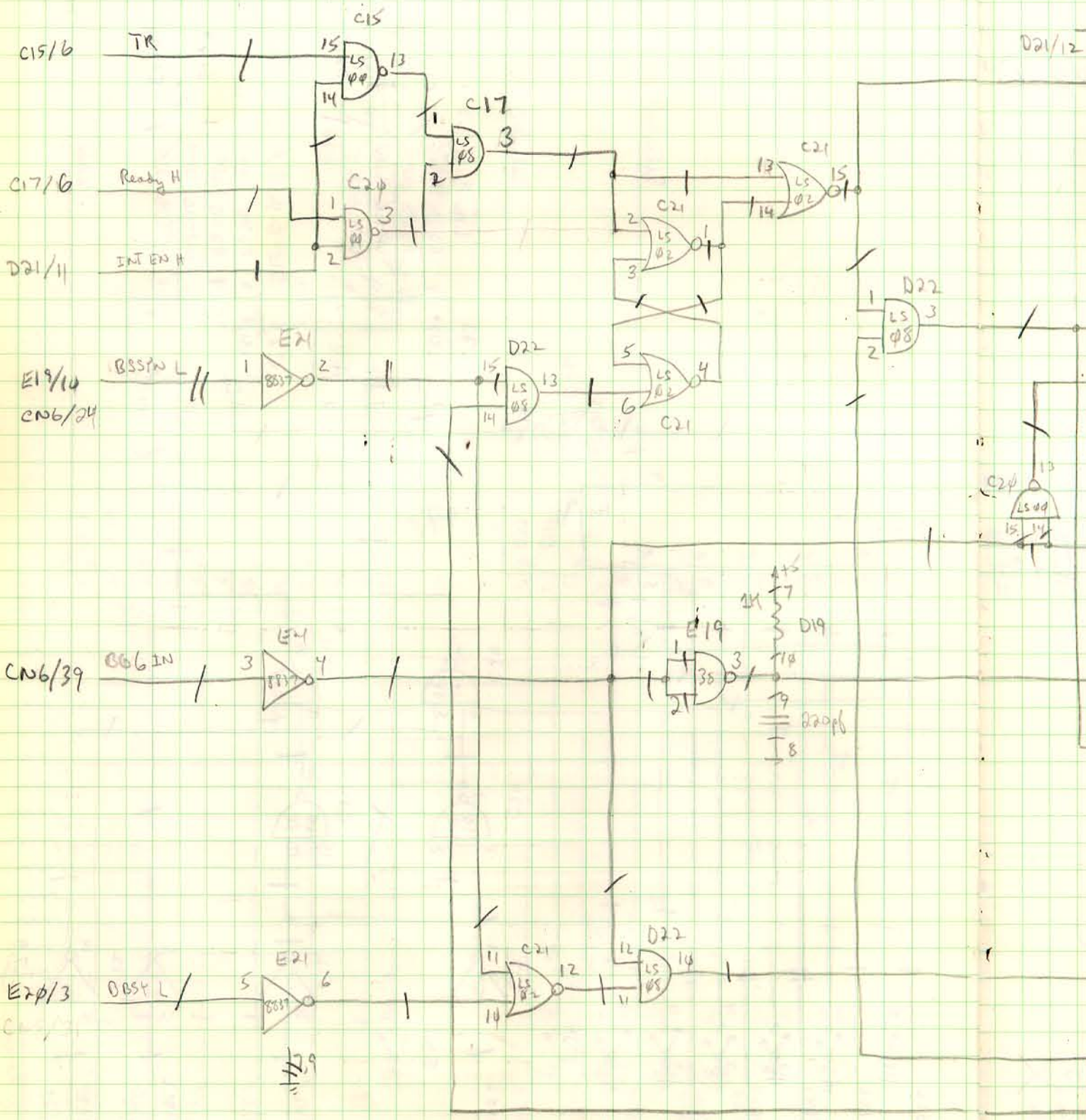
B Block Side 2

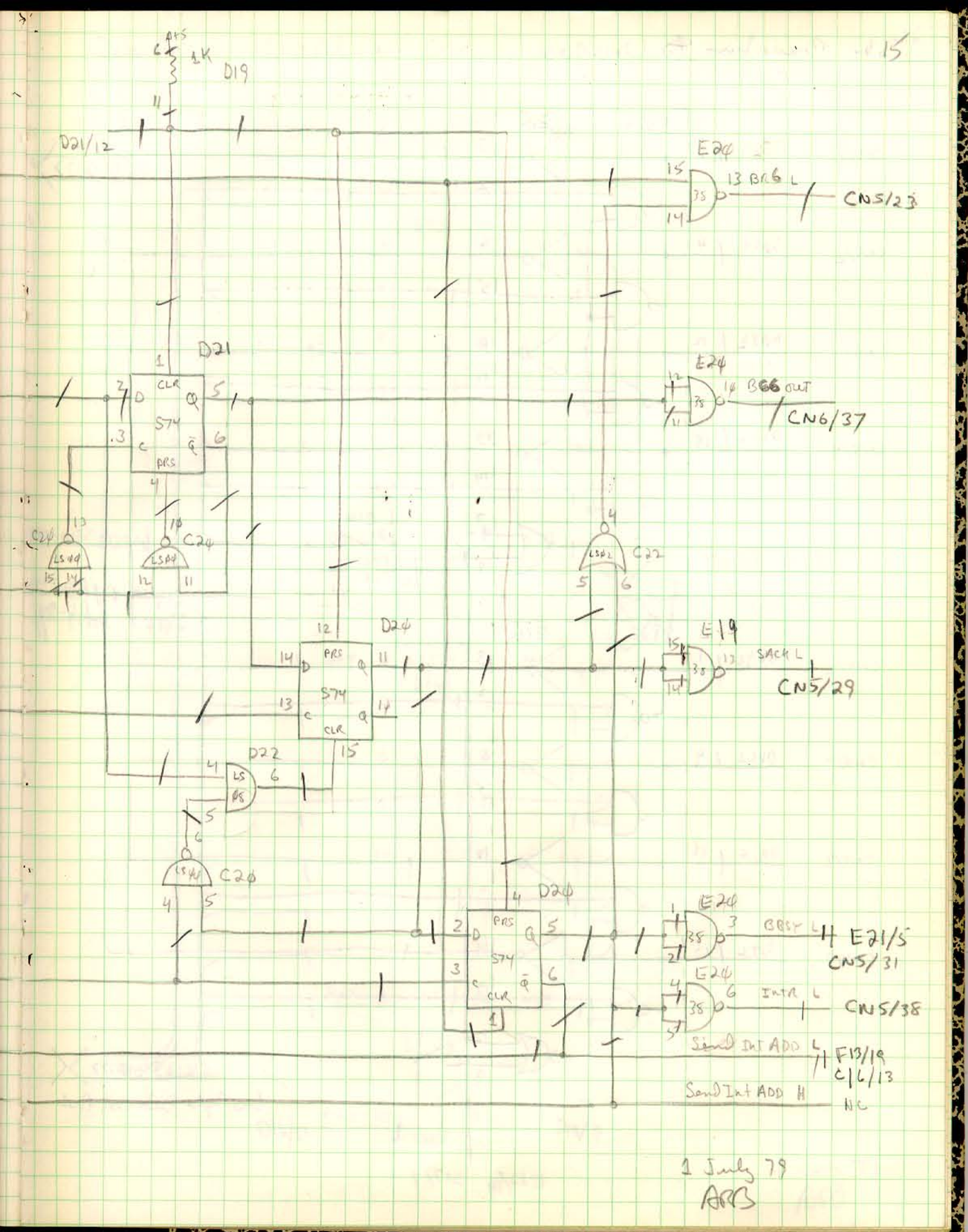
A2	+5
B2	GND
C2	GND
D2	BR4L
E2	BG4H
F2	DCLO L
H2	AØØL
J2	AØ2 L
K2	AØ4 L
L2	AØ6 L
M2	AØ8 L
N2	A10 L
P2	A12 L
R2	A14 L
S2	A16 L
T2	C1 L
U2	CØ L
V2	GND


UNIBUS ADDRESS DECODER
UNIBUS Signals
D24
10K's
+5
CN6/21 MSYN L
CN6/28 A17 L
CN6/20 A16 L
CN6/19 A15 L
CN6/18 A14 L
CN6/17 A13 L
E24
D23
8136
CN6/16 A12 L
CN6/14 A11 L
CN6/13 A10 L
CN6/12 A09 L
CN6/11 A08 L
CN6/9 A07 L
E23
8136
D19
1K
E19
SSYN L
E21/2
470 pf
CN6/8 A06 L
F23
8136


CN6/8
A00L
CN6/7
A01L
CN6/6
A04L
CN6/4
A03L
CN6/3
A02L
offline
online
F24
F23
8136
Selected H
NC
C22
LS02
Selected L
NC
C23
LS139
Low Byte [L]
RDLB Data
RDLB CSR
WRTLB Data
WRTLB CSR
C16/12
C16/11
D16/3
D21/13
High Byte [L]
RDHB Data
RDHB CSR
WRTHB DATA
WRTHB CSR
NC
E18/9
NC
E22/13
Read L
NC
E22
C24
LS00
CN6/1
A00L
CN6/26
C1L
A01L
CN6/2
C1L
CN6/27
7,9

INterrupt Control




APS
1K
D19
D21/12
E24
13 BRG L
CN5/23
D21
CLR
D
Q
S74
C
PRS
E24
B66 OUT
CN6/37
C24
LS04
C24
LS04
C22
LS02
D20
PRS
S74
CLR
E19
38
SACK L
CN5/29
D22
LS
PRS
C24
LS04
D20
PRS
S74
CLR
E20
38
BUSY L
E21/5
CN5/31
E20
38
INTR L
CN5/38
Send Int ADD L
F13/19
C16/13
Send Int ADD H
NC

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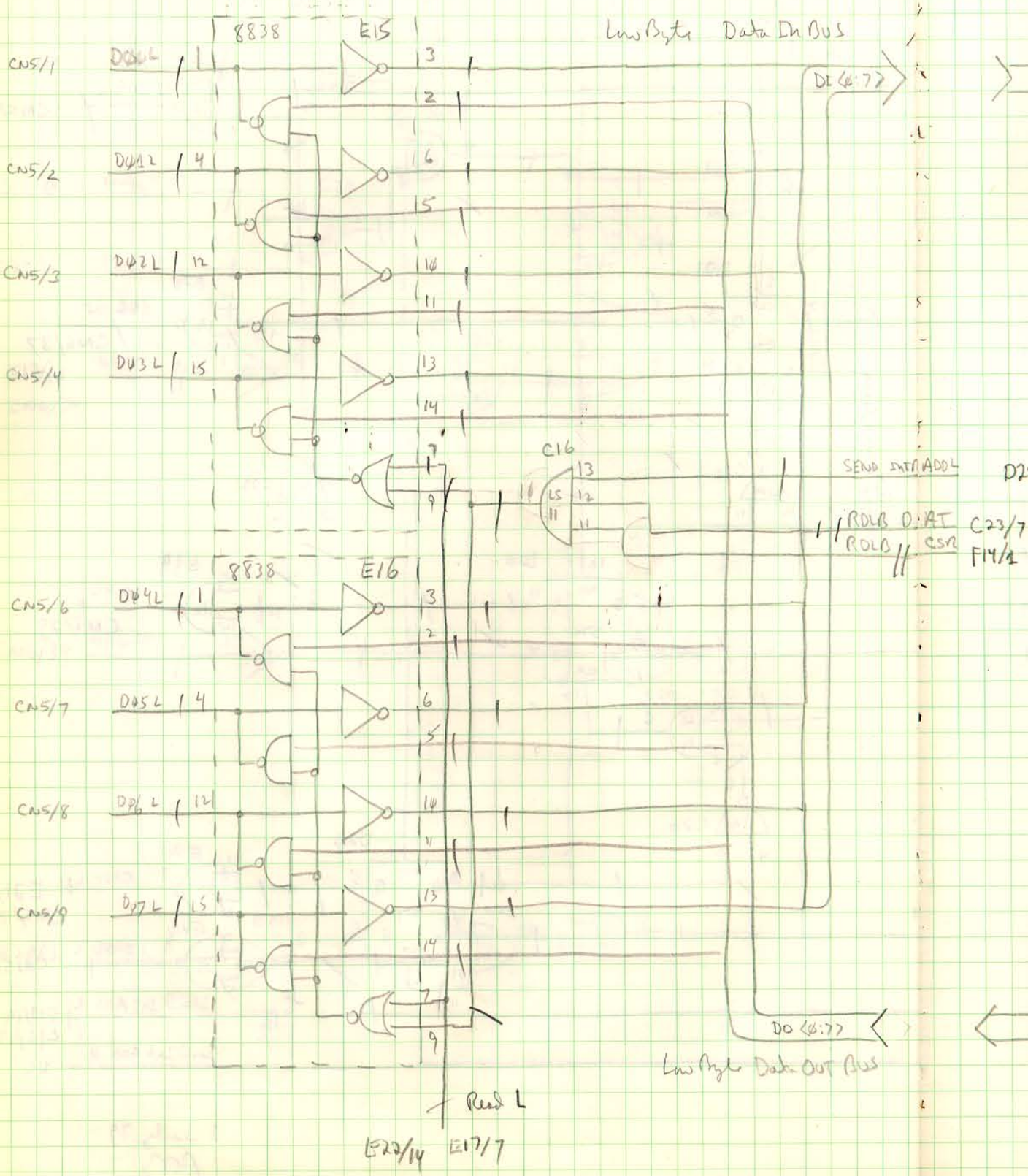
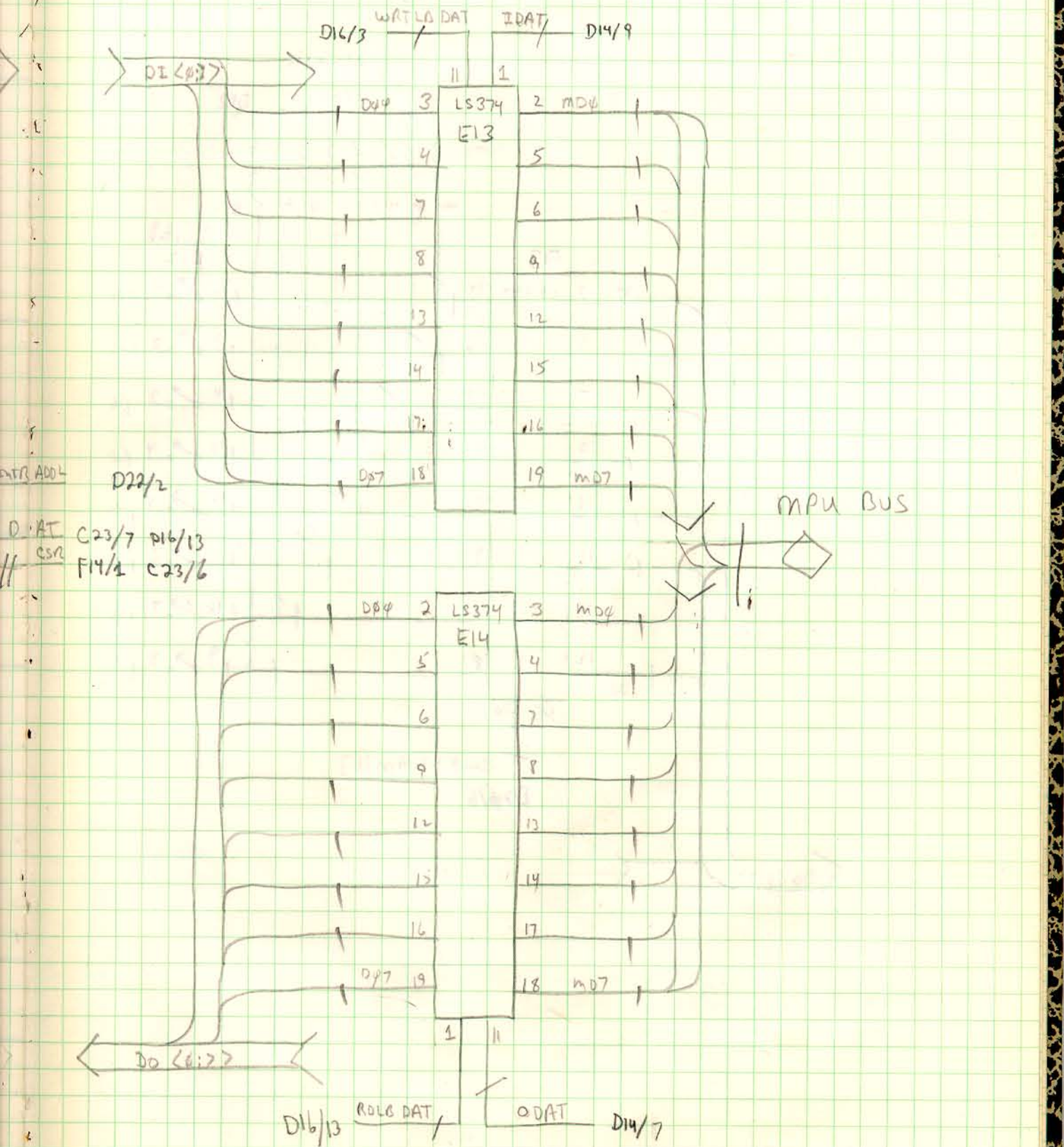
Data Connections to UNIBUS
LOW BYTE



Data Registers & MPU



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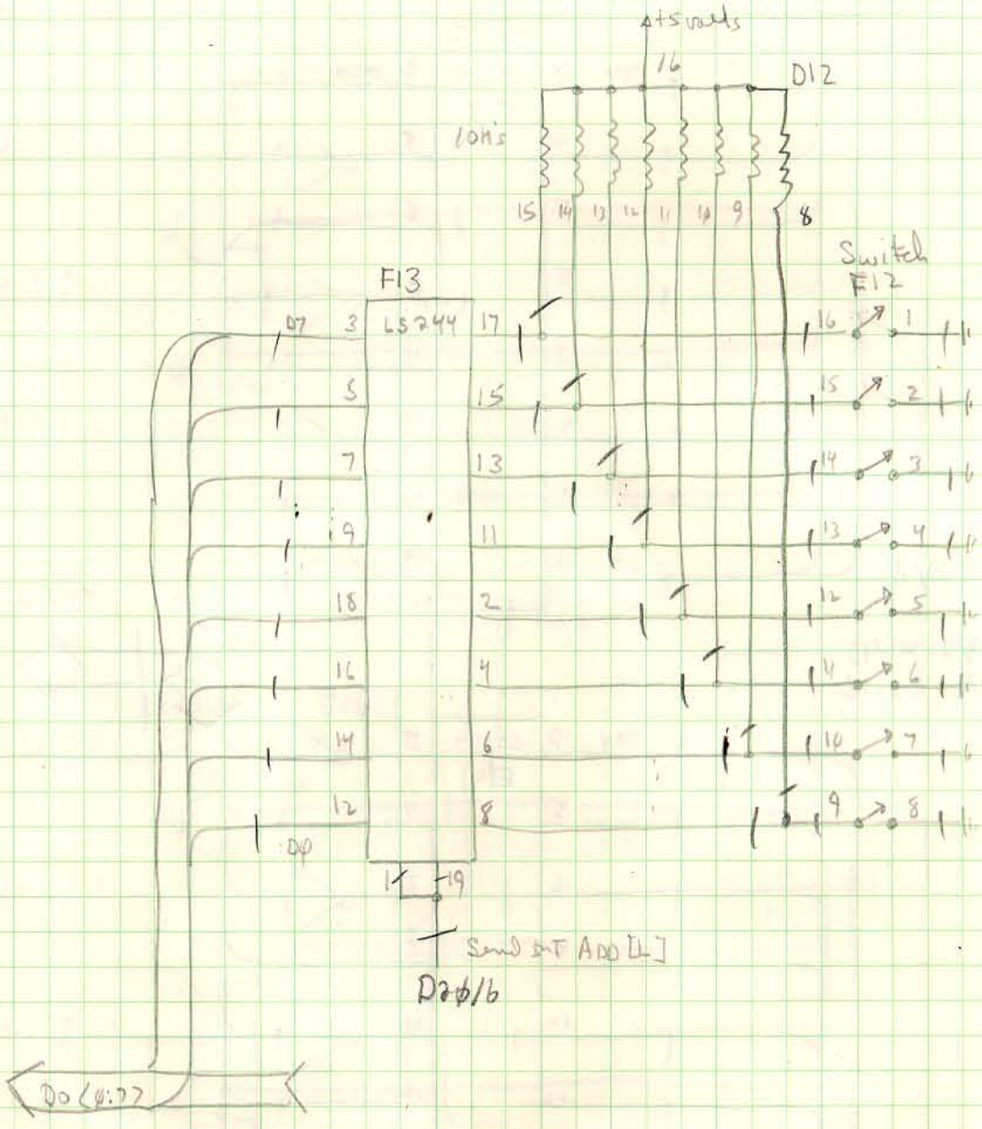
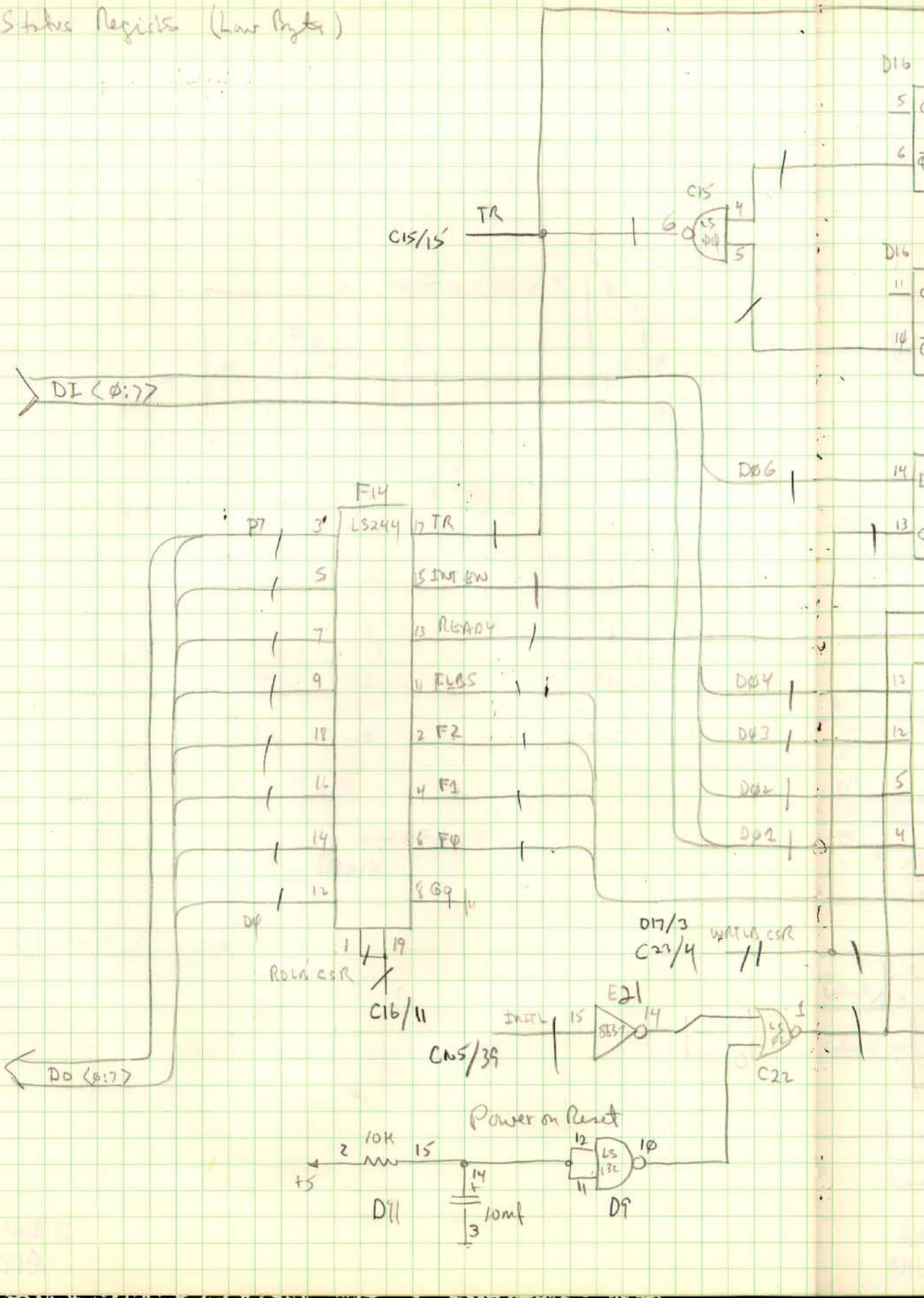
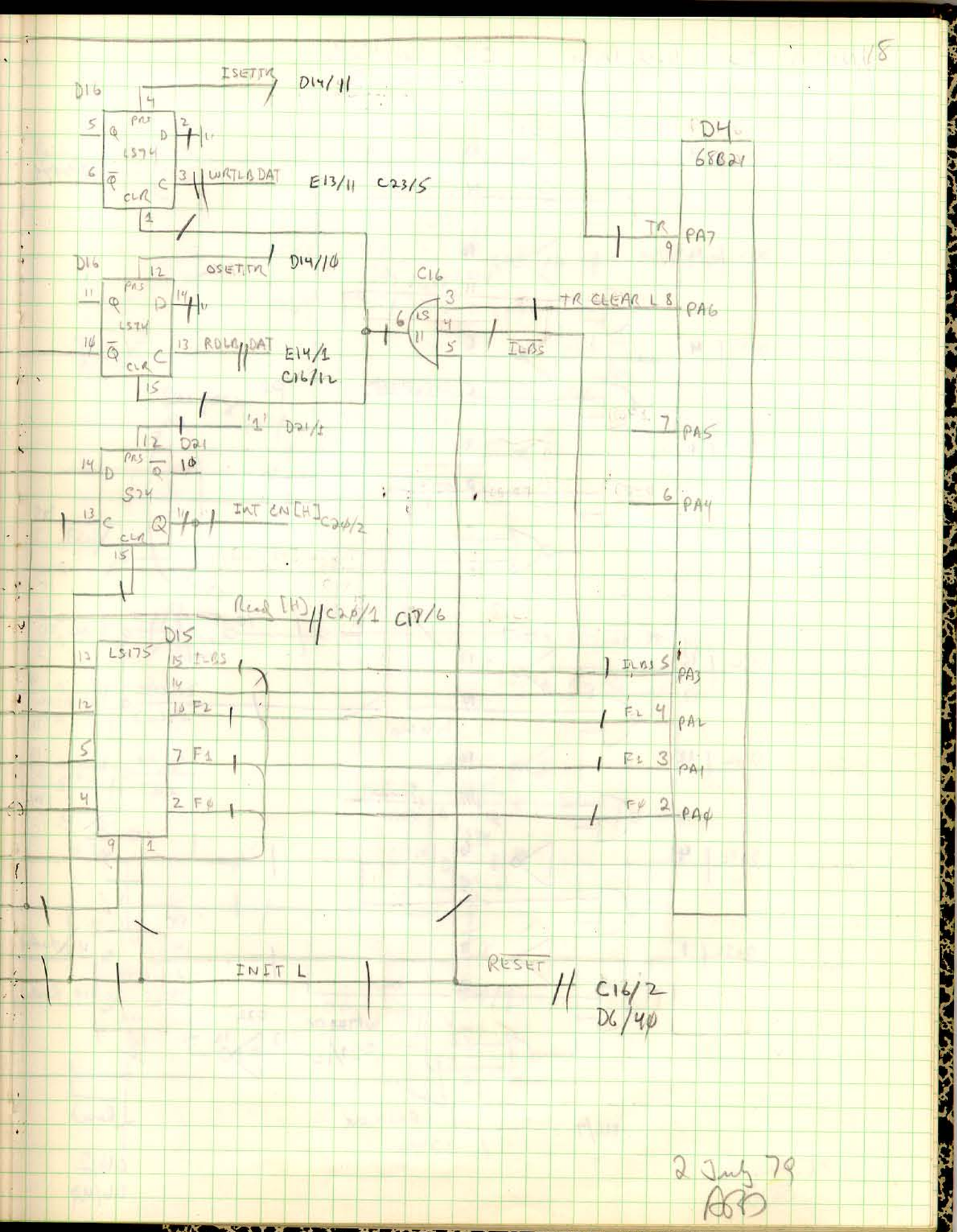
Interrupt Vector



Control & Status Registers (Low Byte)




D16
ISETTR
D14/11
LS74
PRE
CLR
WRTLAB DAT
E13/11 C23/5
OSETTR
D14/10
RDLB DAT
E14/1
C16/12
'1'
D21/1
D21
S74
INT EN [H] C20/2
Read [H] C20/1 C17/6
D15
LS175
ILBS
F2
F1
F0
INIT L
RESET
C16/2
D6/40
C16
LS11
TR CLEAR L 8
ILBS
D4
68B21
TR
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0

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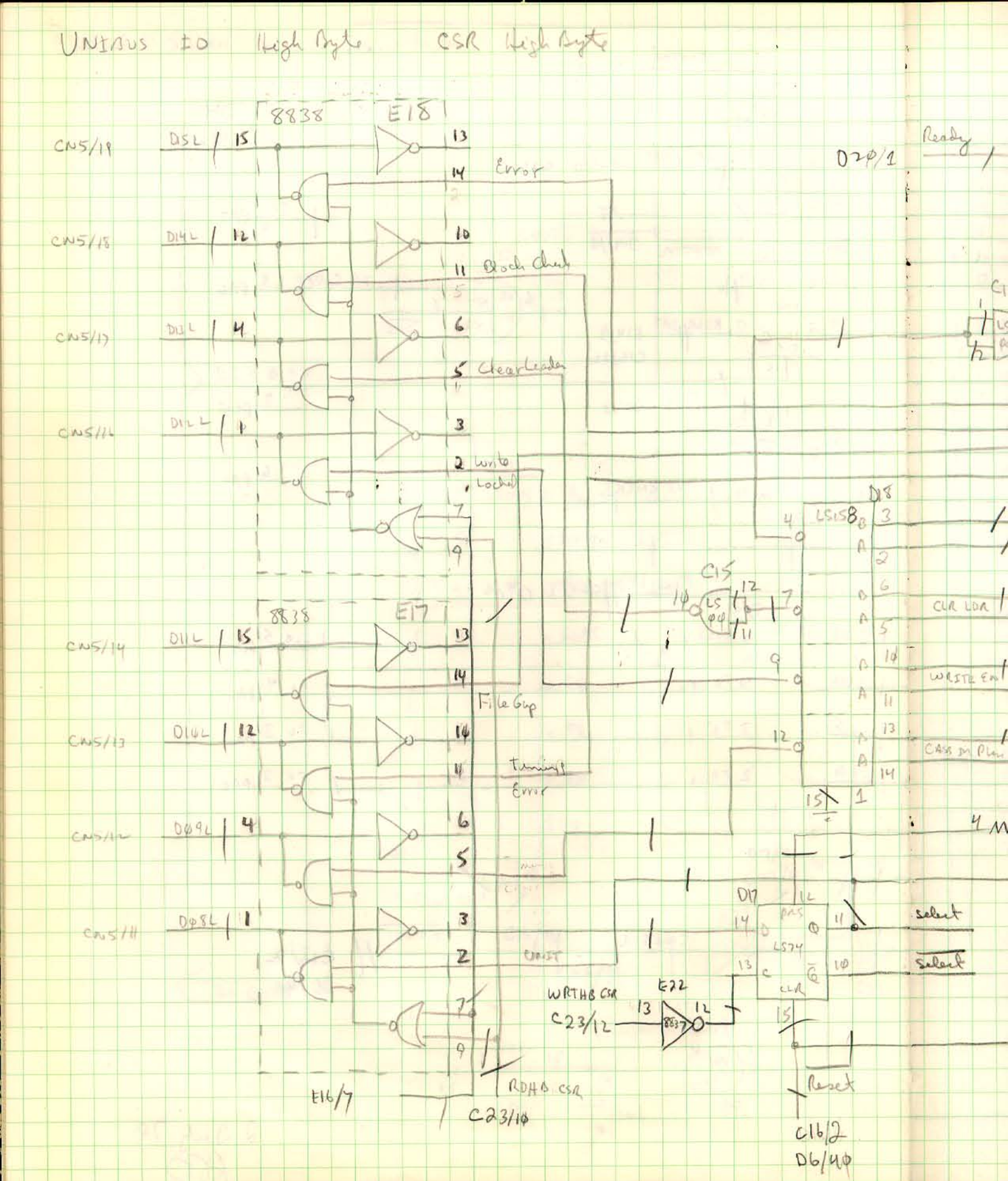
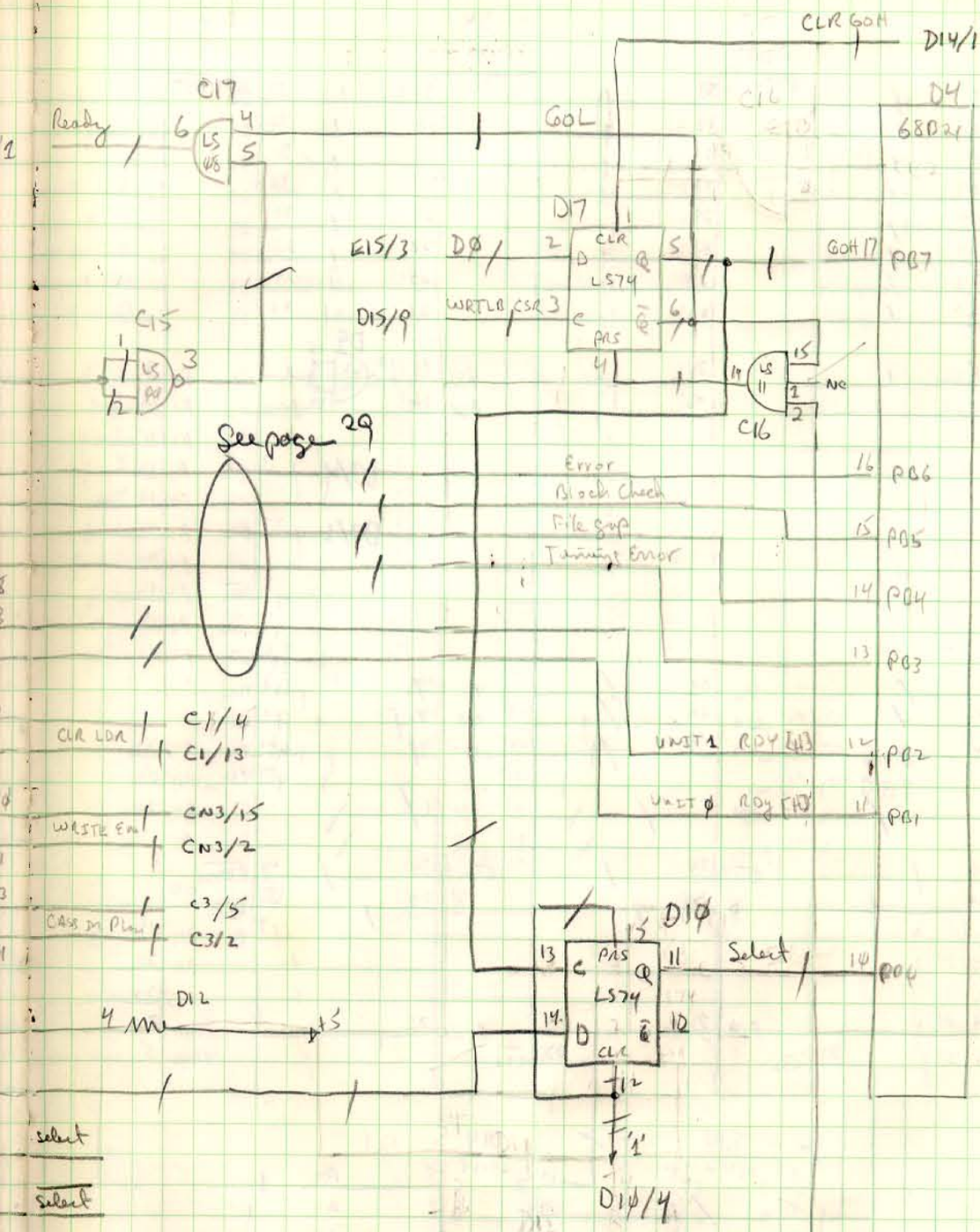
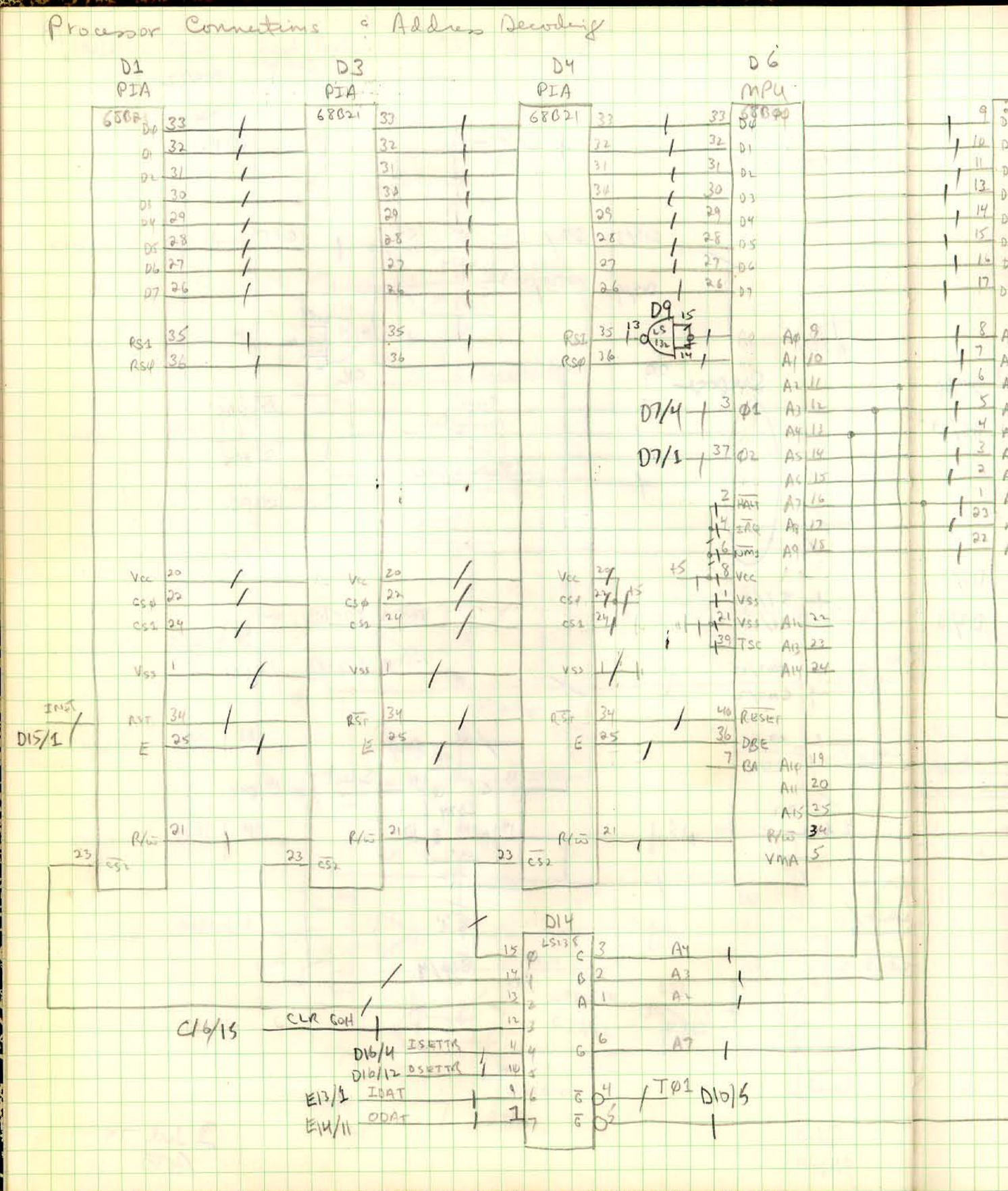
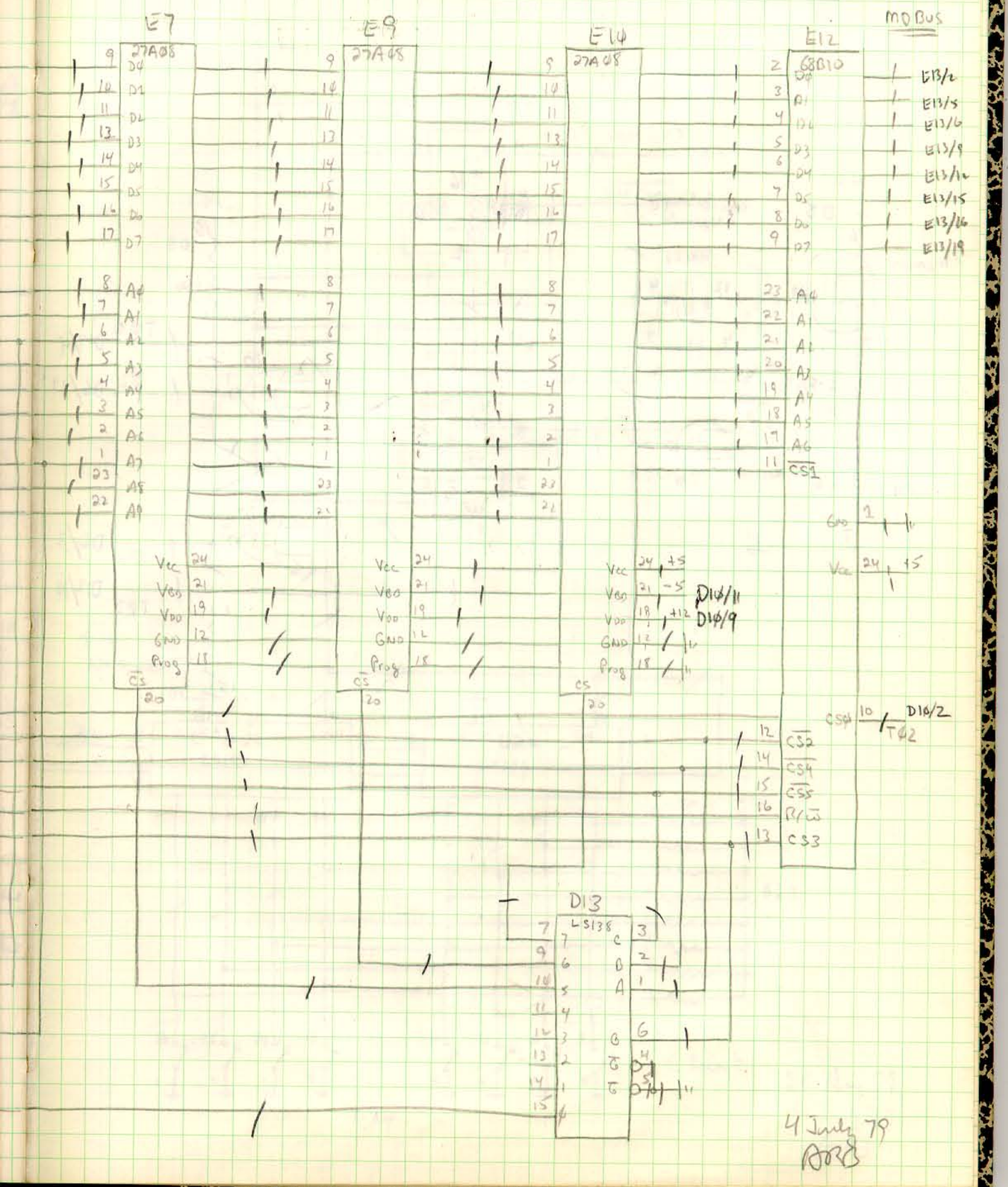

UNIBUS I/O High Byte
CSR High Byte
8838
E18
CN5/19
D5L
15
13
14
Error
CN5/18
D14L
12
10
11
Block check
CN5/17
D13L
4
6
5
Clear Leader
CN5/16
D12L
1
3
2
Write Lockout
7
9
8838
E17
CN5/14
D11L
15
13
14
File Gap
CN5/13
D10L
12
14
11
Timing Error
CN5/12
D09L
4
6
5
CN5/11
D08L
1
3
2
ERROR
7
9
E16/7
RDH8 CSR
C23/10
WRTH8 CSR
C23/12
E22
8837
C15
LS
12
10
7
11
9
12
D18
LS158
4
B
A
3
2
6
5
10
11
13
14
15
1
CLR LDR
WRITE EN
CASS IN PLA
4 M
D17
LS74
PRS
D
Q
14
11
C
CLR
13
10
select
select
15
Reset
C16/2
D6/40
Ready
D29/1
C1
LS
A
h


CLR GOH
D14/12
C17
Ready
GOL
D4
68D24
D7
E15/3
D0
CLR
LS74
GOH 17
PB7
D15/9
WRTLB CSR 3
PRS
C15
C16
See page 29
Error
Block Check
File Sup
Timing Error
PB6
PB5
PB4
PB3
PB2
PB1
PB0
CLR LDR
C1/4
C1/13
WRITE Enb
CN3/15
CN3/2
CAS in Plan
C3/5
C3/2
D12
D10
Select
D10/4
select
select

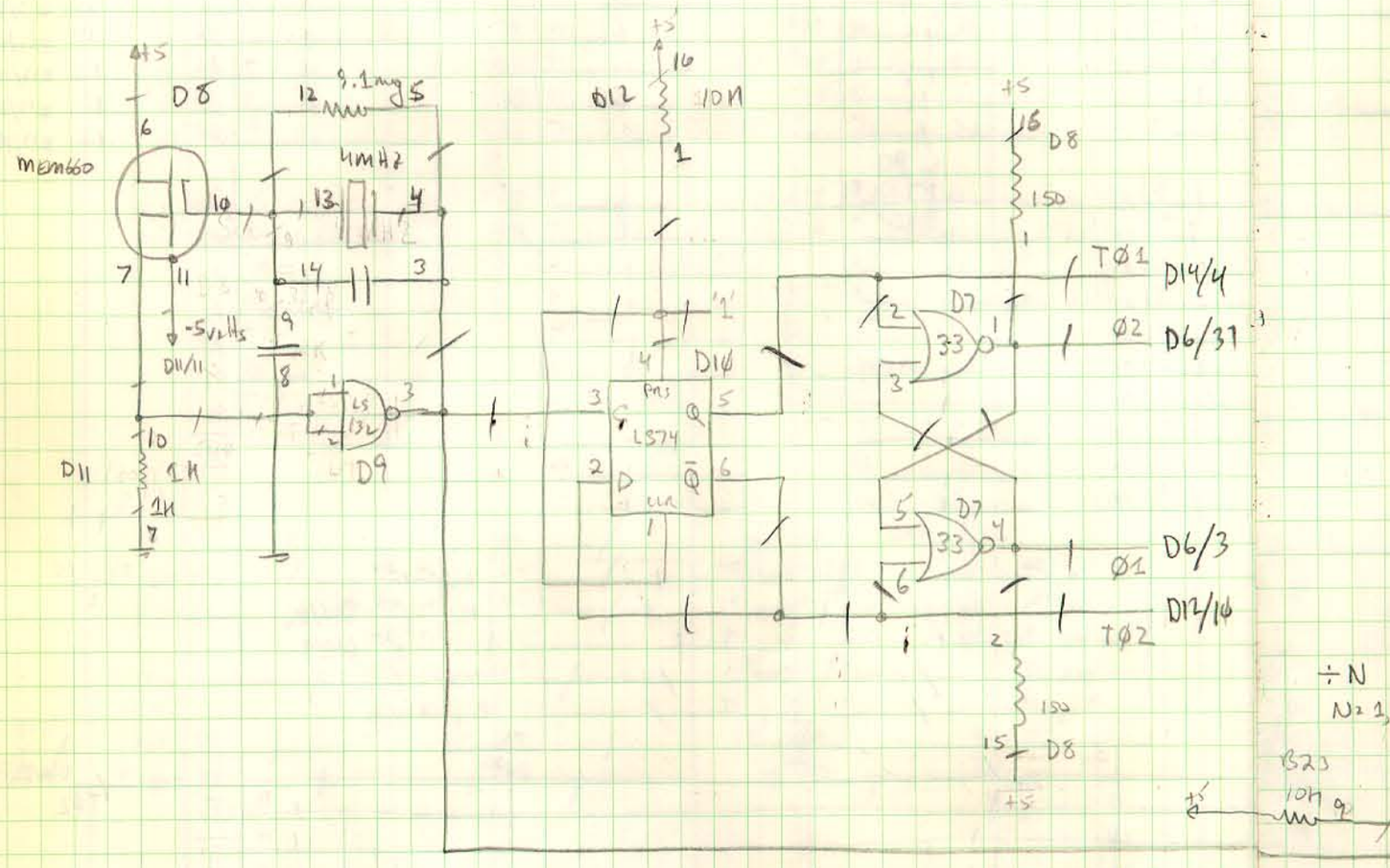
2 July 78
BRS

Processor Connections & Address Decoding

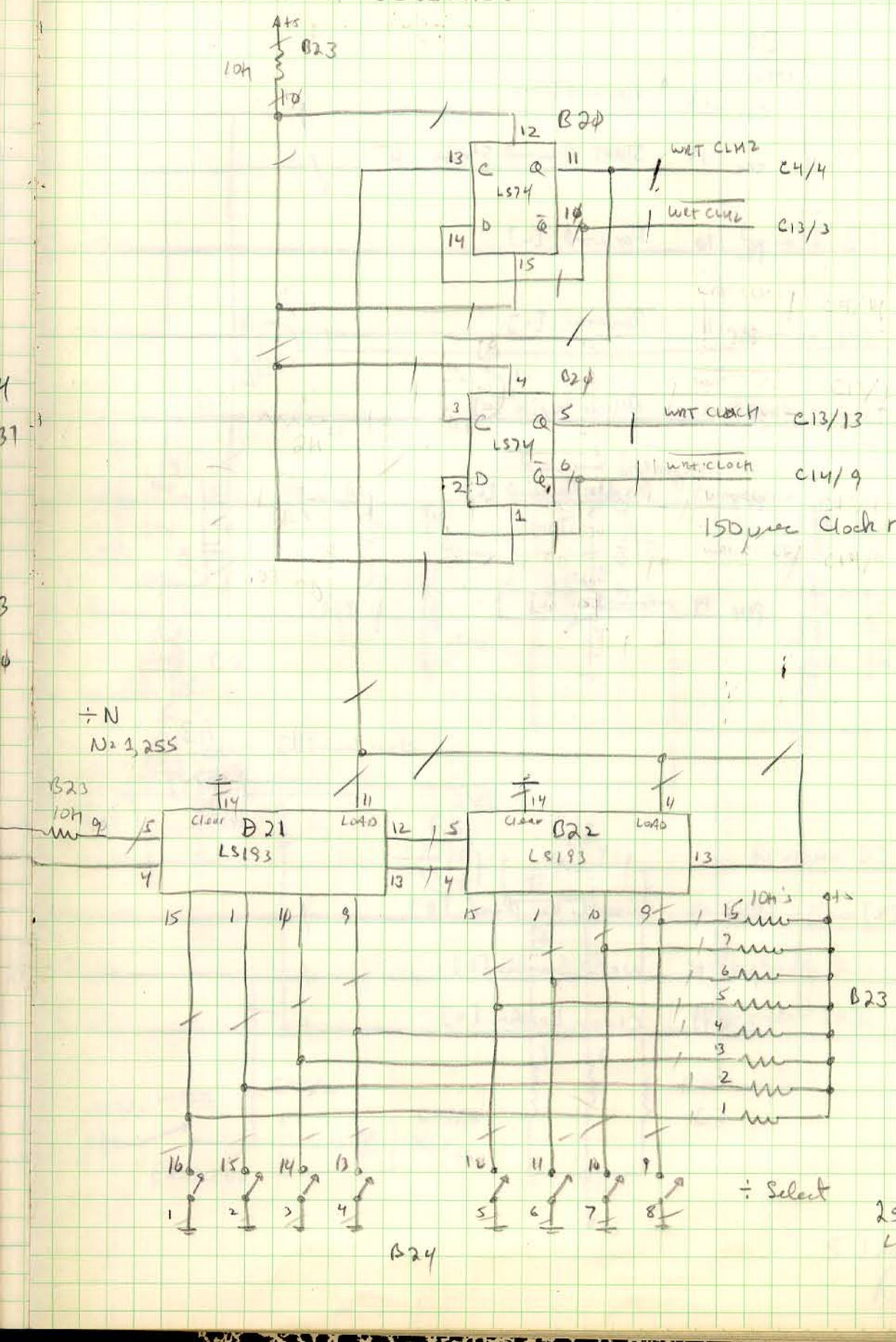



E7
E9
E14
E12
MOBUS
27A08
68B10
D13
LS138
Vcc
VBB
VDD
GND
Prog
CS
R/W
+5
-5
+12
D14/11
D14/9
D16/2
Φ2
4 July 79

MPU CLOCK GENERATOR



WRITE CLOCK GENERATOR



÷N

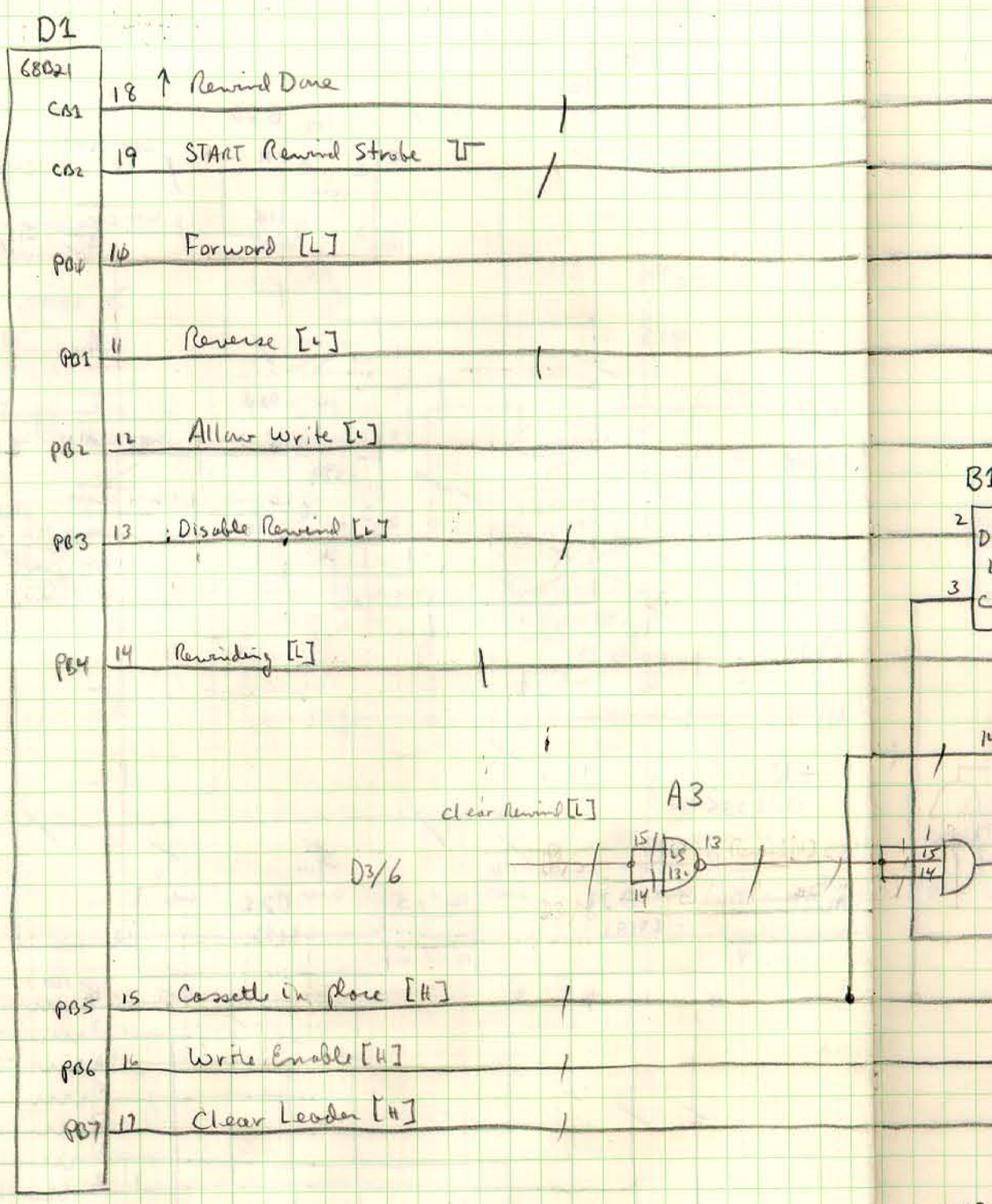
N = 1,255

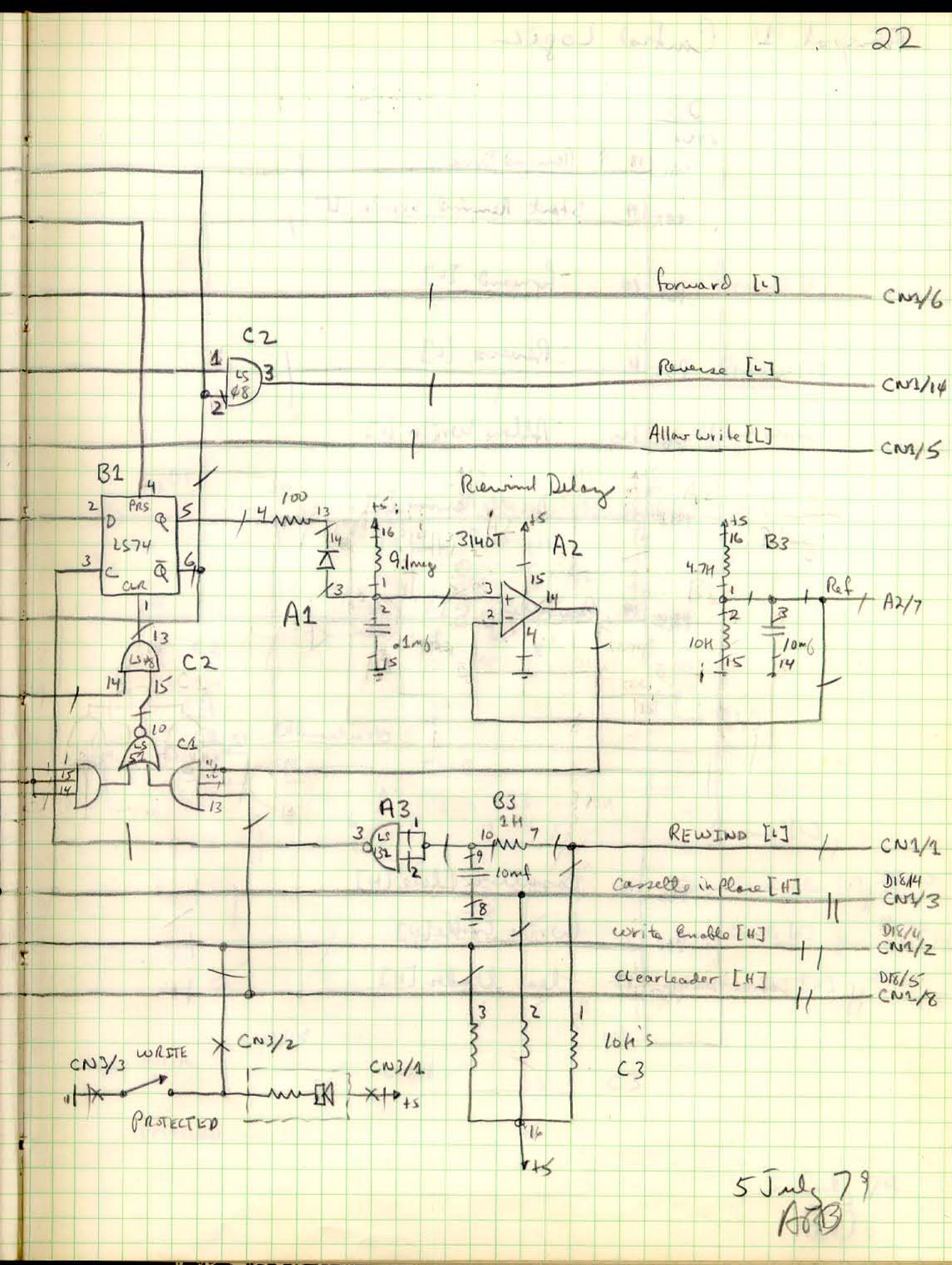
25 Aug 79

4 July 79

BRD

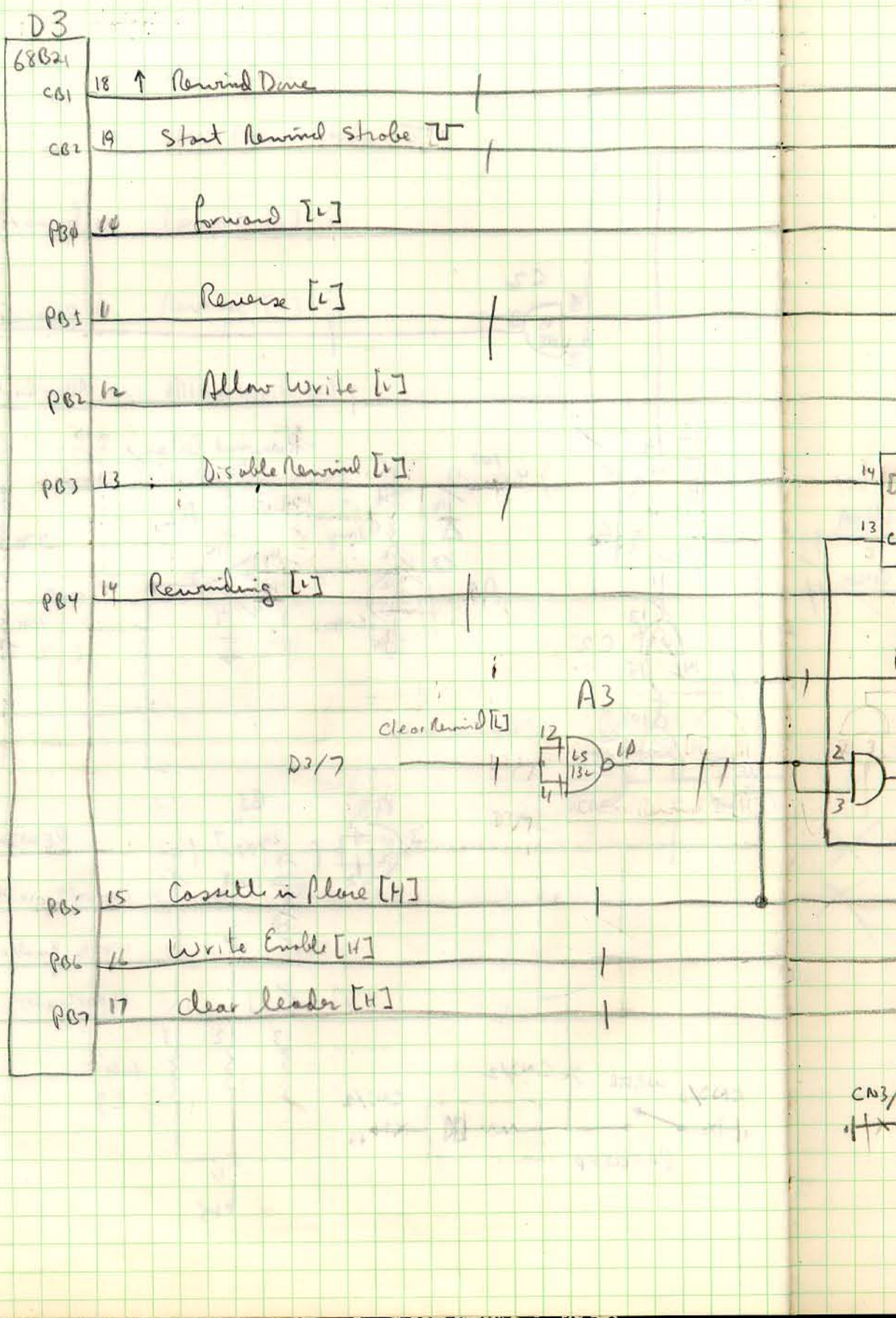
Transport ∅ Control Logic

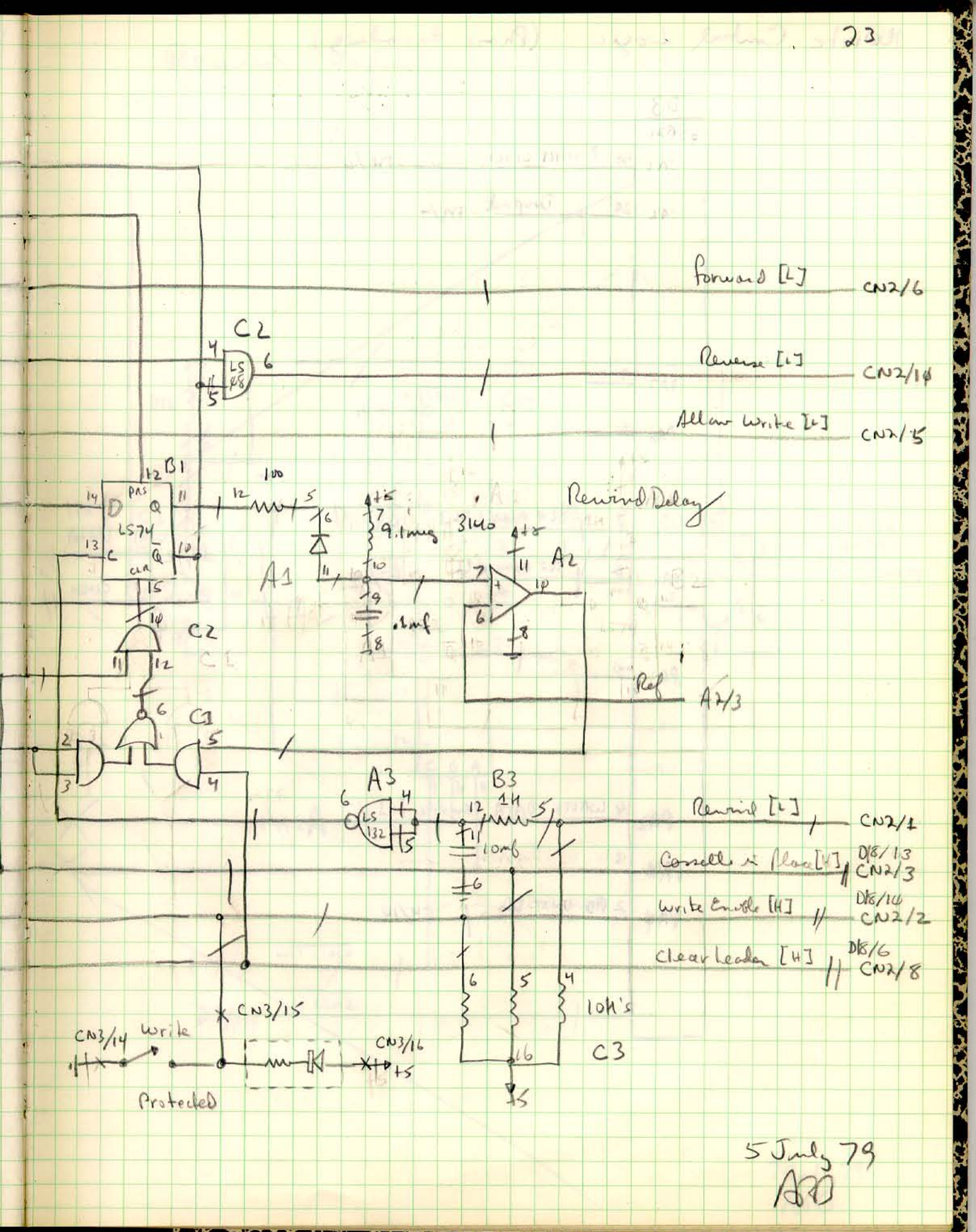



forward [L]
CN1/6
C2
LS 08
Reverse [L]
CN1/14
Allow Write [L]
CN1/5
B1
LS74
PRS
CLR
100
Rewind Delay
+5
9.1meg
A1
3140T
A2
B3
4.7M
10K
Ref
A2/7
10mf
C2
LS 08
C1
LS 32
A3
1M
REWIND [L]
CN1/1
10mf
Cassette in place [H]
DI6/4
CN1/3
Write Enable [H]
DI6/4
CN1/2
Clearleader [H]
DI6/5
CN1/8
10K's
C3
CN3/3
WRITE
CN3/2
CN3/1
PROTECTED

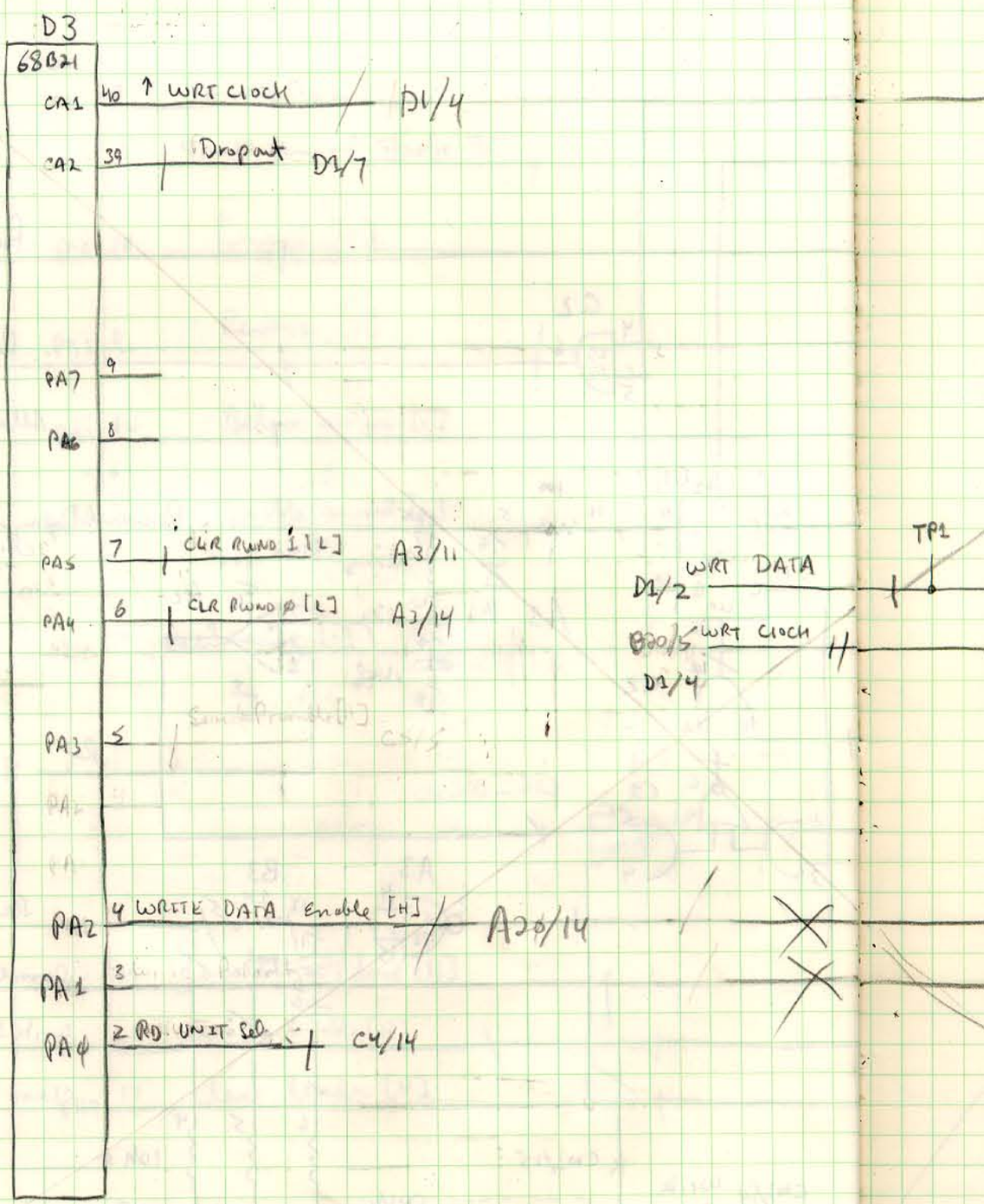
5 July 79
AOB

Transport 1 Control Logic



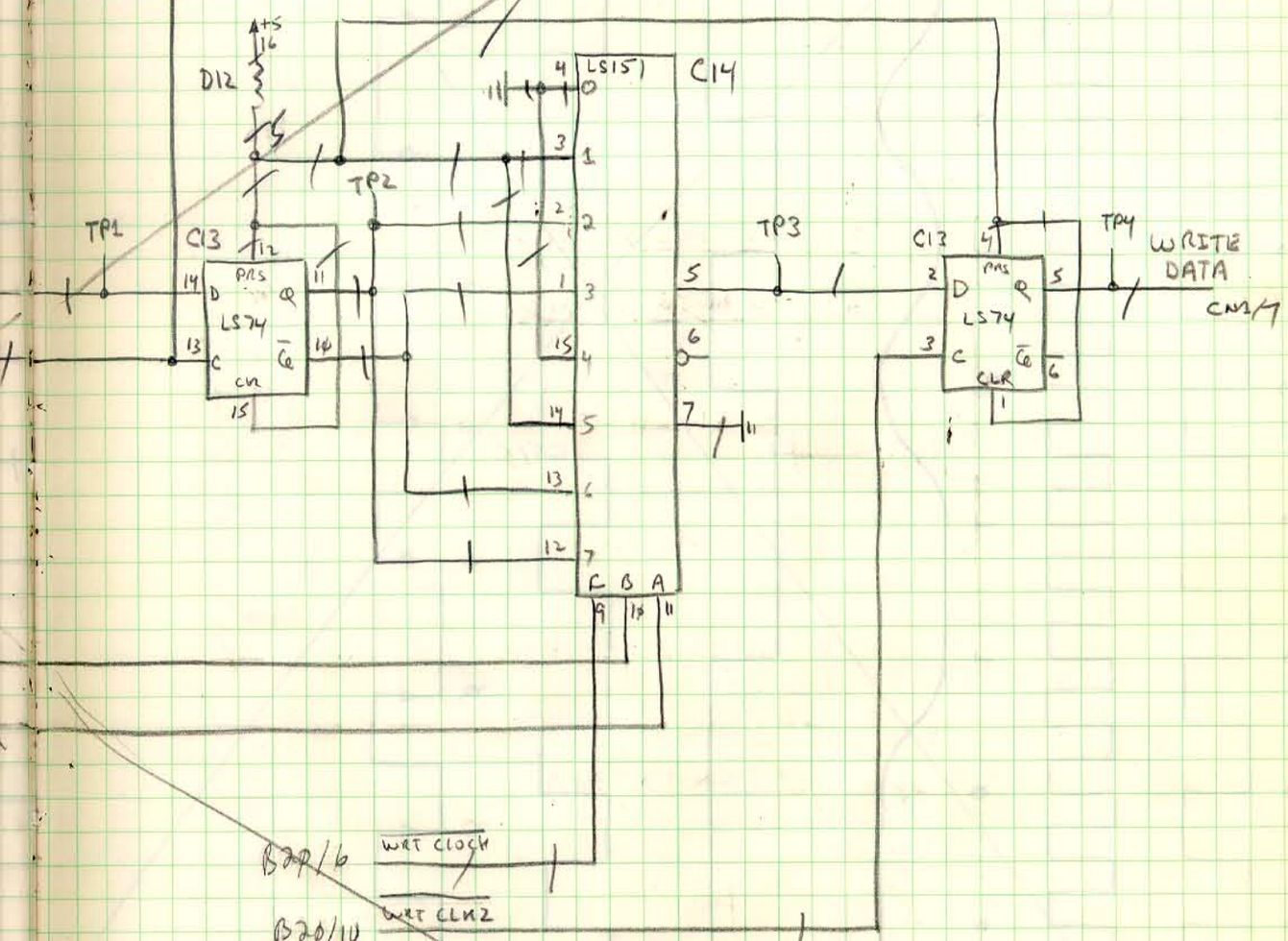

forward [L]
CN2/6
C2
LS 08
Reverse [L]
CN2/10
Allow Write [L]
CN2/5
B1
LS74
100
Rewind Delay
9.1meg
3140
A2
A1
.1mf
Ref
A2/3
C2
C1
A3
LS 132
B3
1M
Rewind [L]
CN2/1
10mf
Console Play [L]
D18/13
CN2/3
Write Enable [H]
D18/10
CN2/2
Clear Leader [H]
D18/6
CN2/8
CN3/15
CN3/14
Write
Protected
CN3/16
+5
10M's
C3
5 July 79
AB

Write Control Logic (Phase Encoding)



Rewired 10 DEC 79

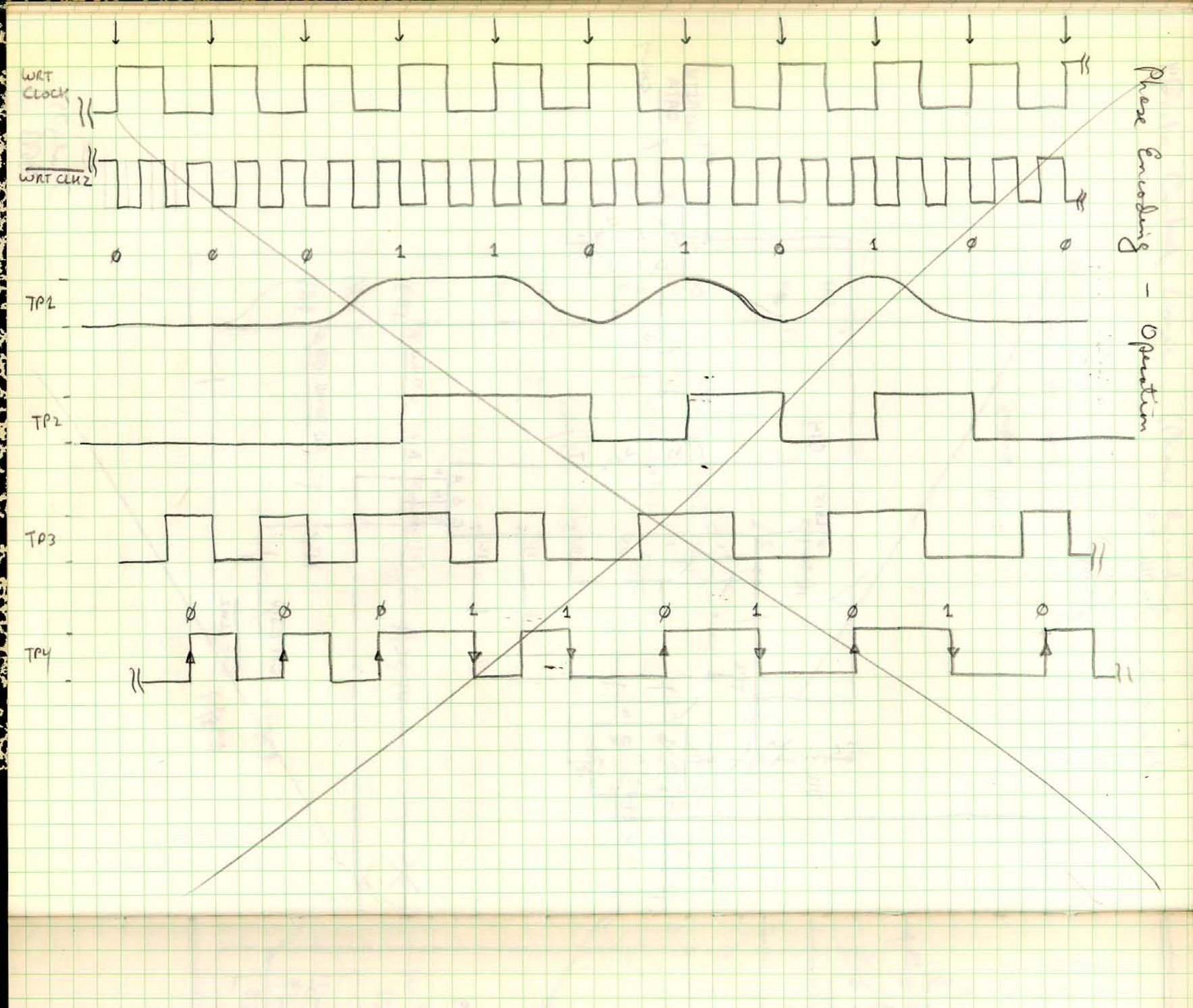
ARP



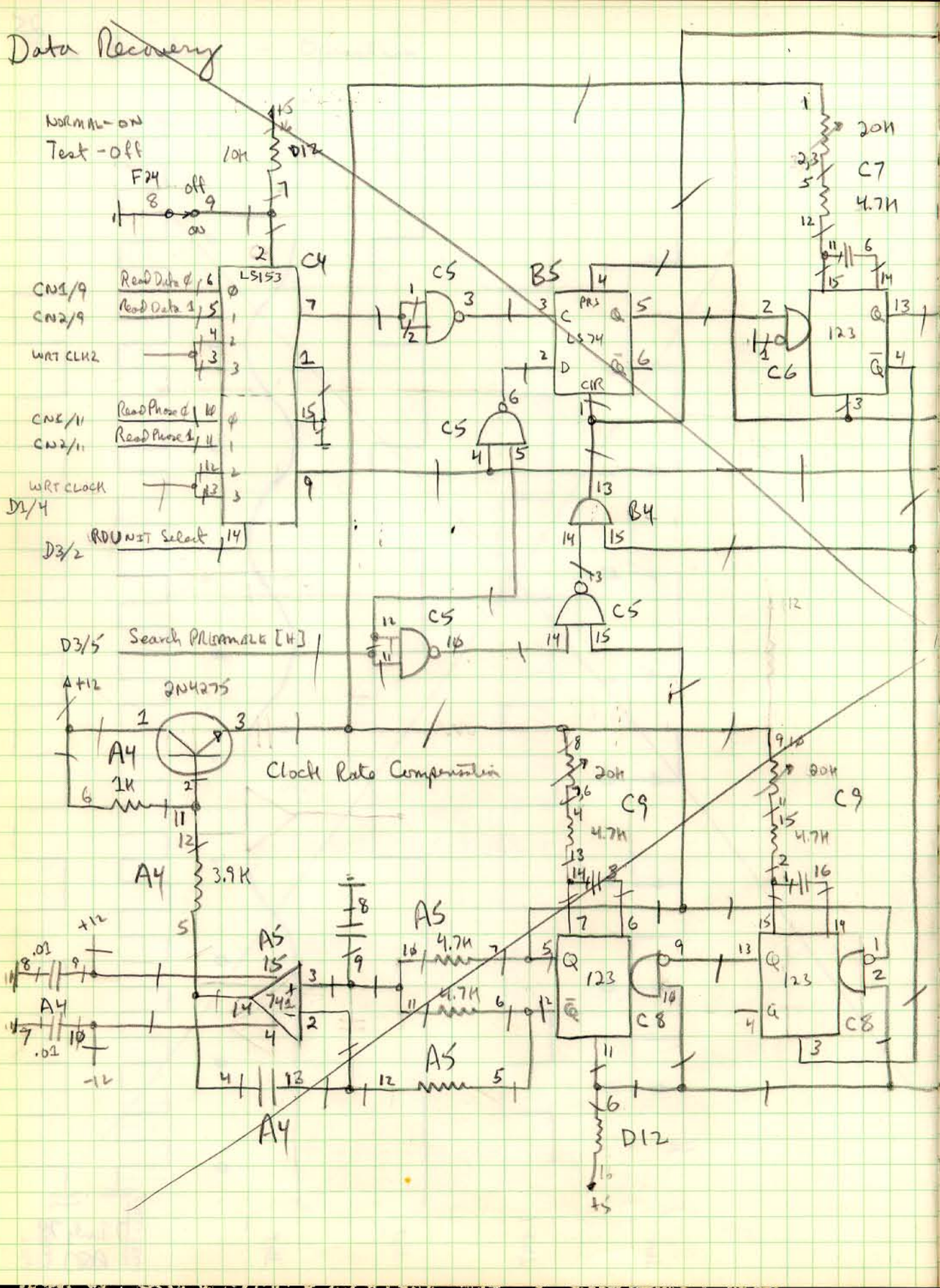
B2P/6 WRT CLOCK

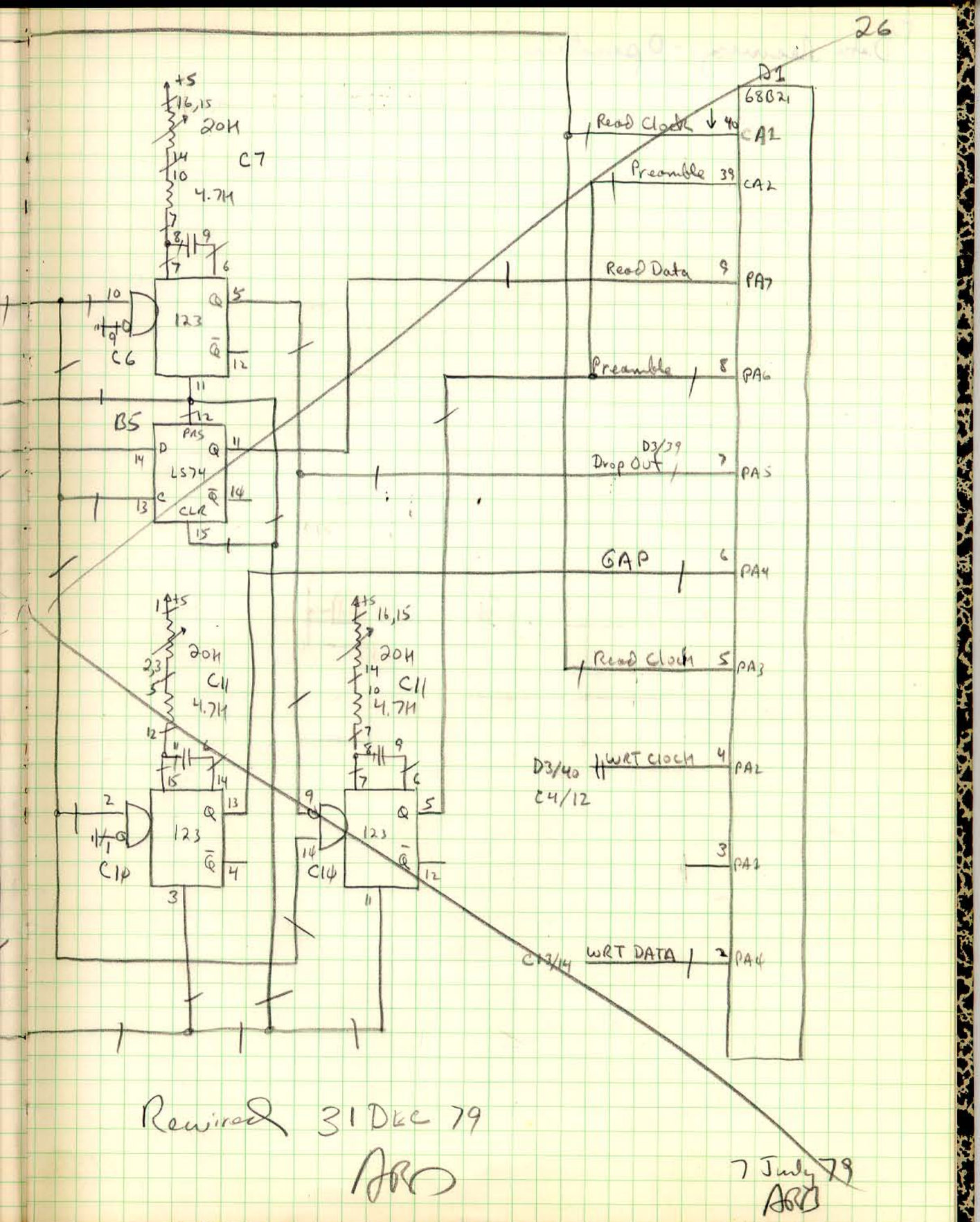
B2P/14 WRT CLK2

7 July 79
ARP

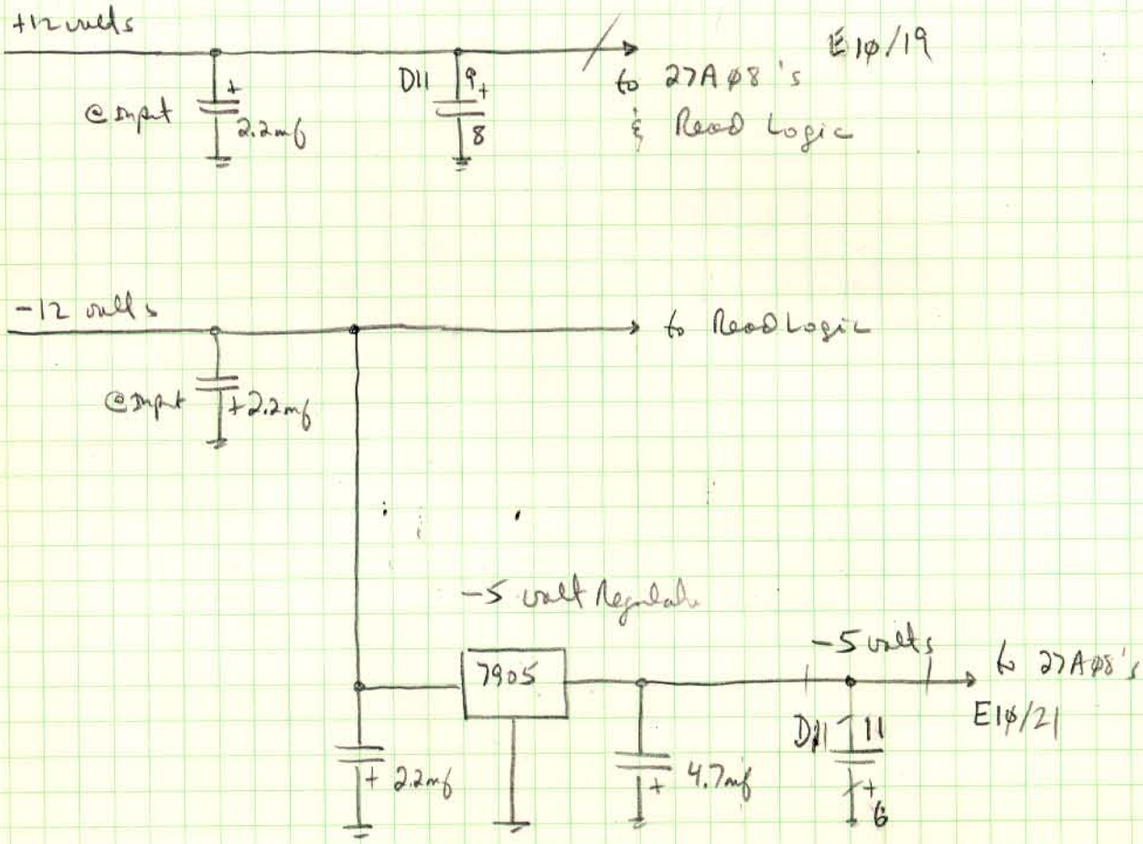

WRT CLOCK
WRT CLK2
0 0 0 1 1 0 1 0 1 0 0
TP2
TP3
0 0 0 1 1 0 1 0 1 0
TP4
Phase Encoding - Operation

Data Recovery

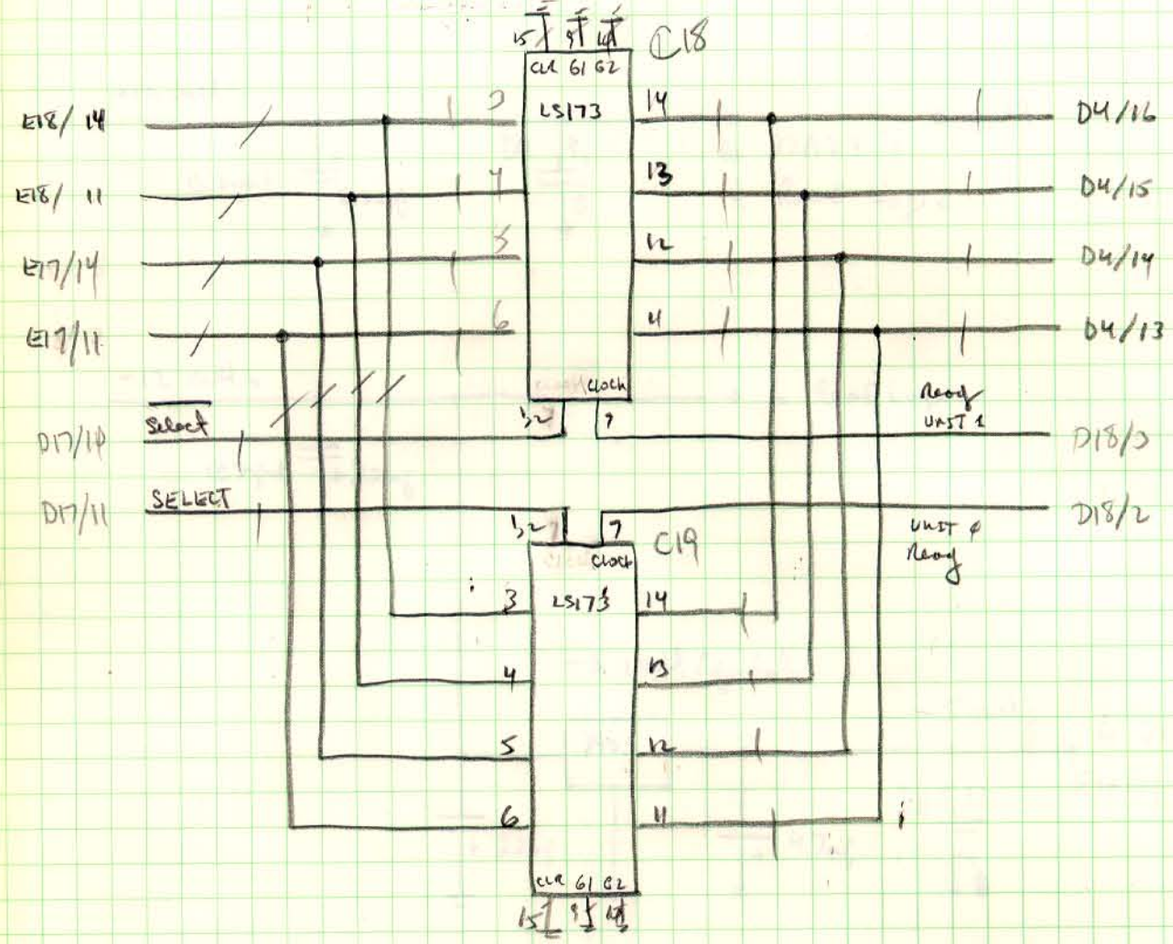



+5
16,15
20H
C7
14
10
4.7H
7
8
9
7
6
10
Q
5
123
9
C6
Q
12
11
B5
12
PA5
D
Q
11
14
LS74
C
CLR
14
13
15
+5
20H
C11
4.7H
C14
C13/14
D1
6821
Read Clock
40
CA1
Preamble
39
CA2
Read Data
9
PA7
Preamble
8
PA6
D3/39
Drop Out
7
PA5
GAP
6
PA4
Read Clock
5
PA3
D3/40
WRT Clock
4
PA2
C4/12
3
PA1
WRT DATA
2
PA0
Rewired 31 DEC 79
ARO
7 July 79
ARO

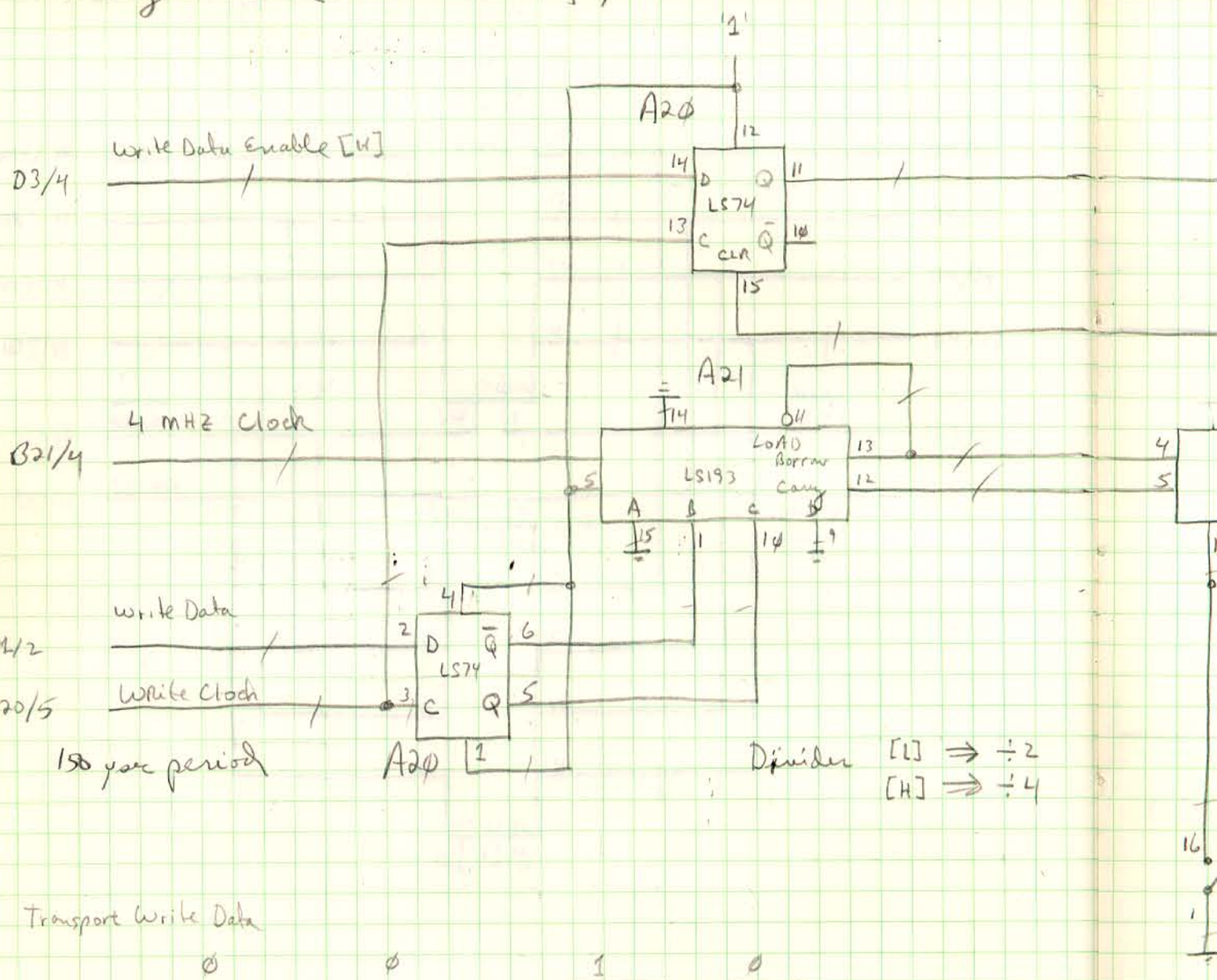
± 12 volt Power Distribution



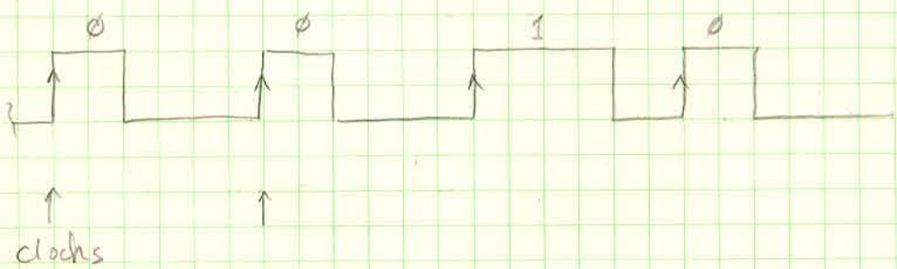
Error code Buffer

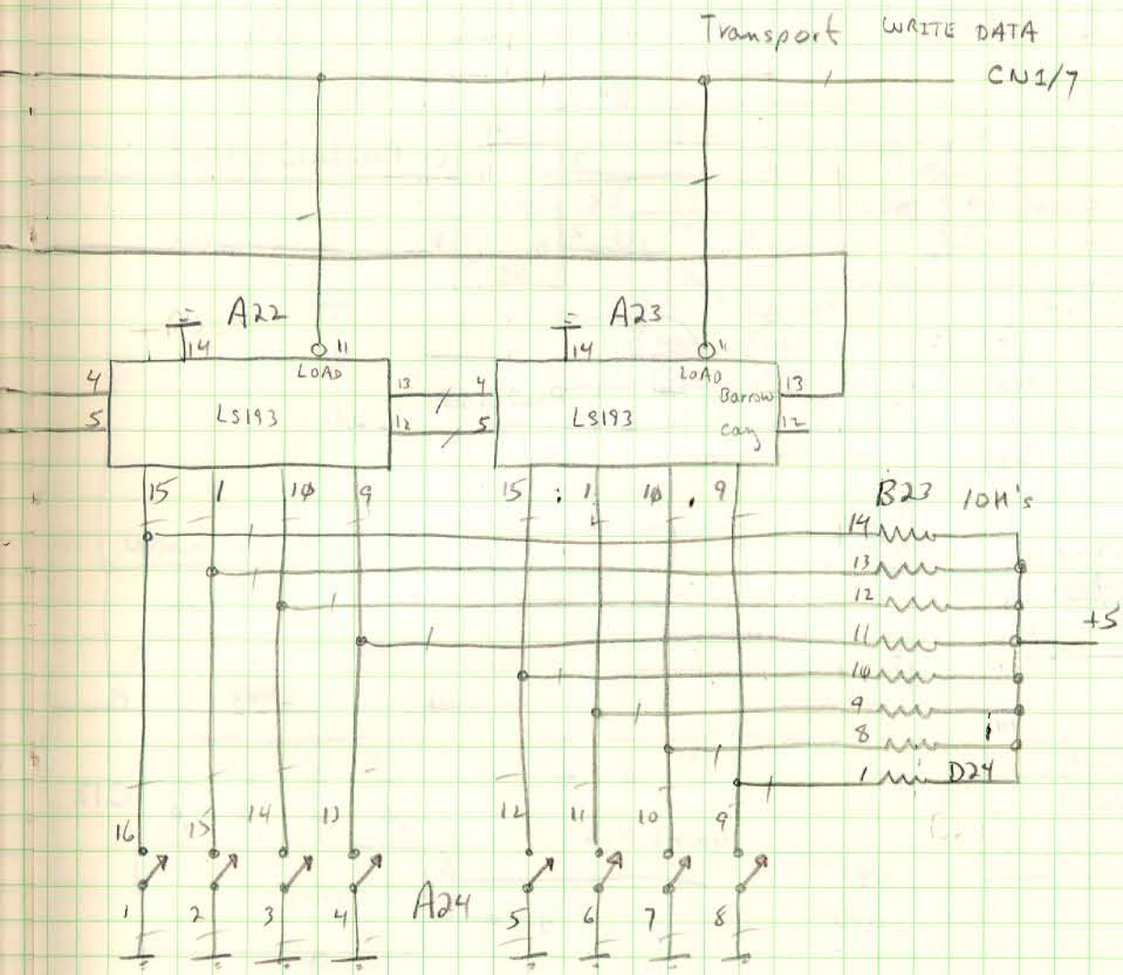


Write Logic (Rotor Method)



Transport Write Data

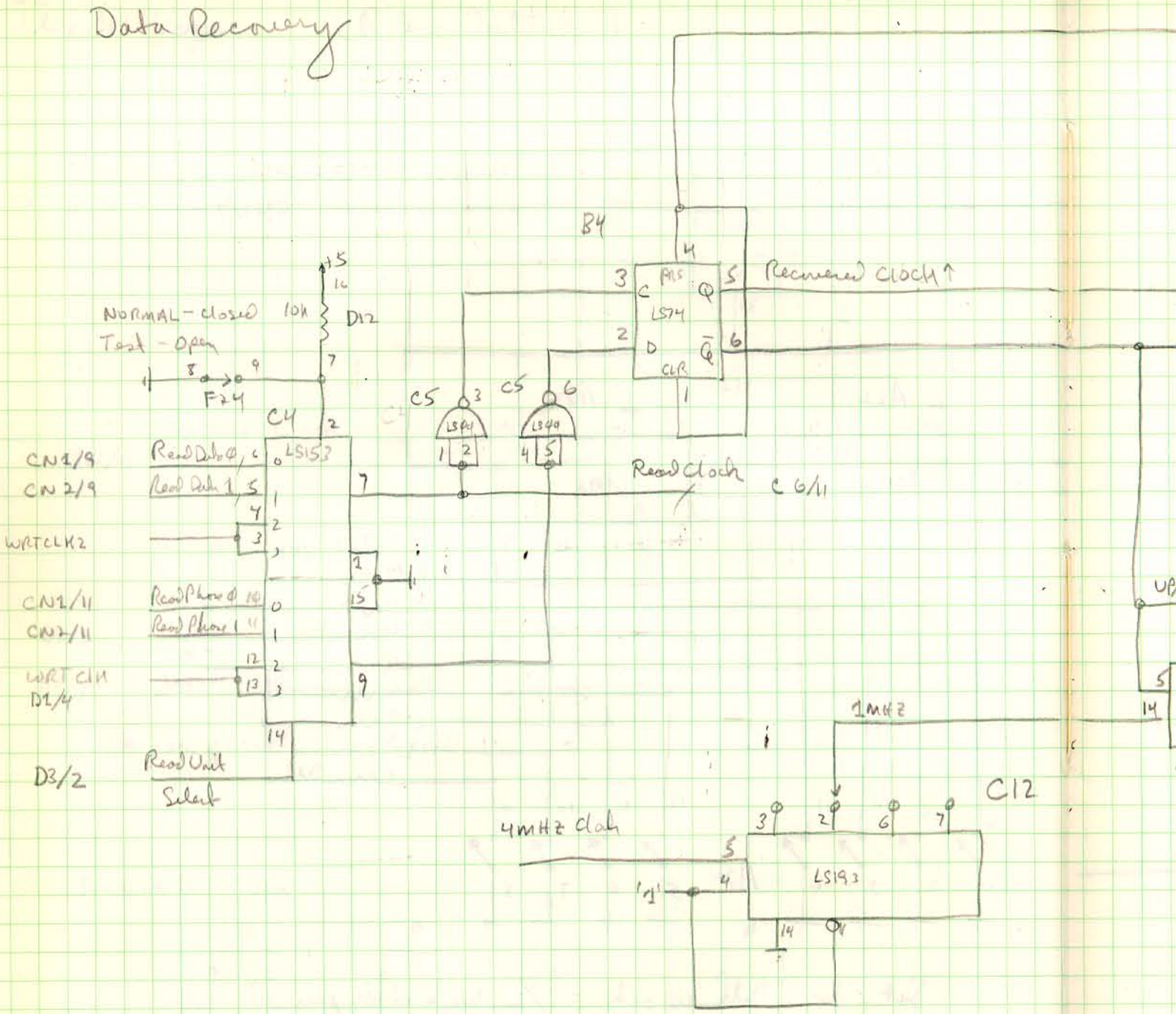




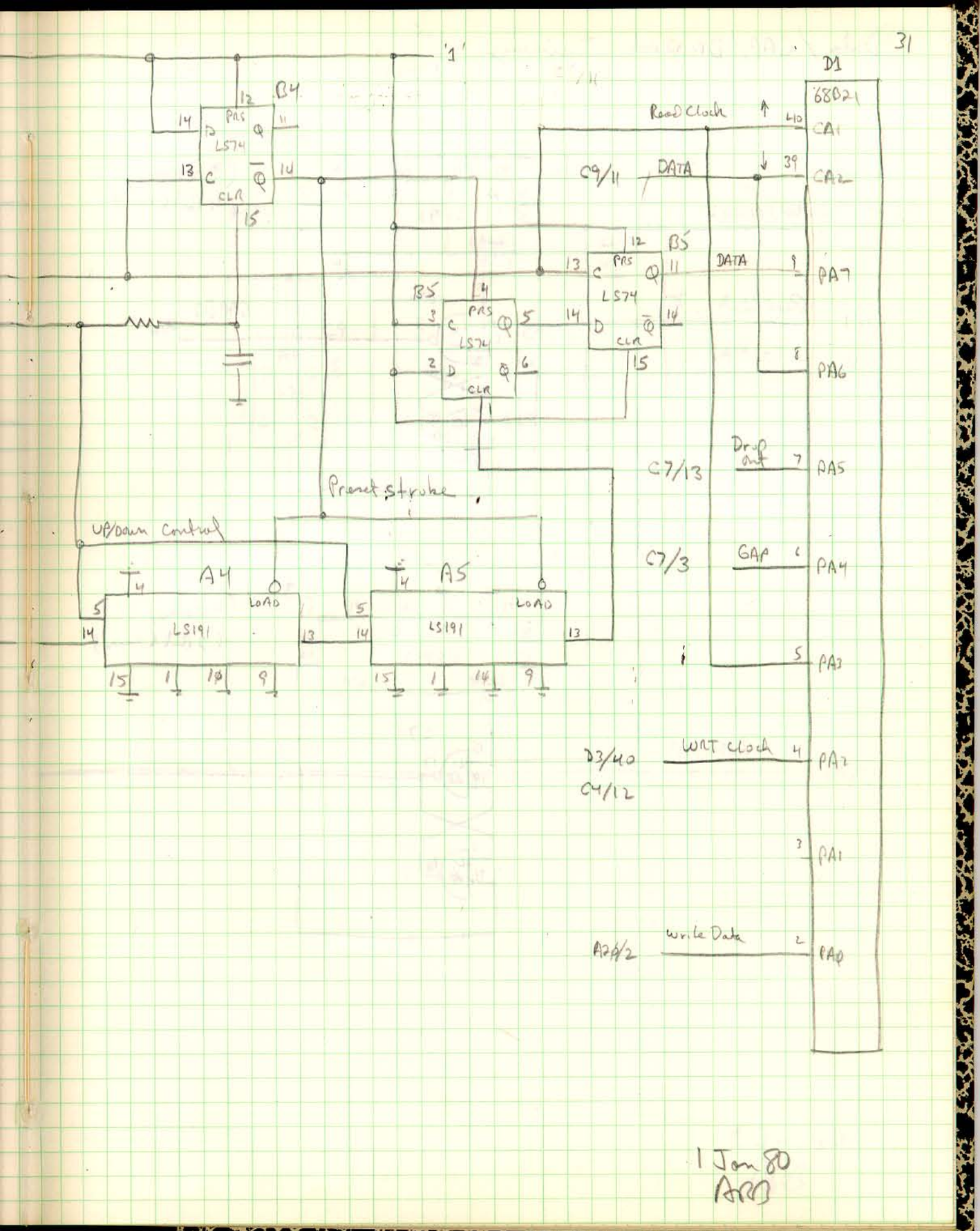
Set for Data width = 1/3 write clock period
with Write Data = [1]

1 Jan 80
ARB

Data Recovery

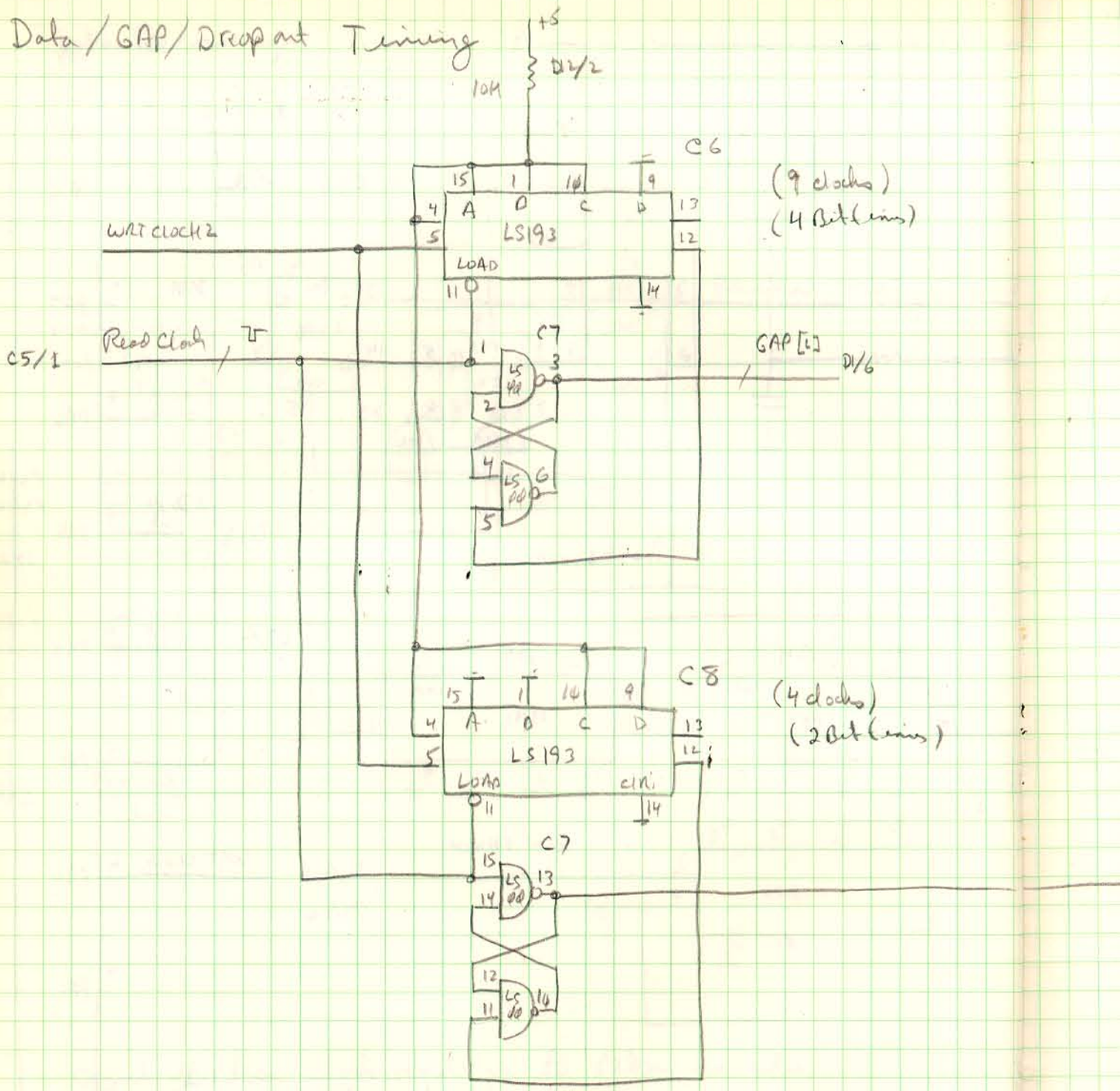


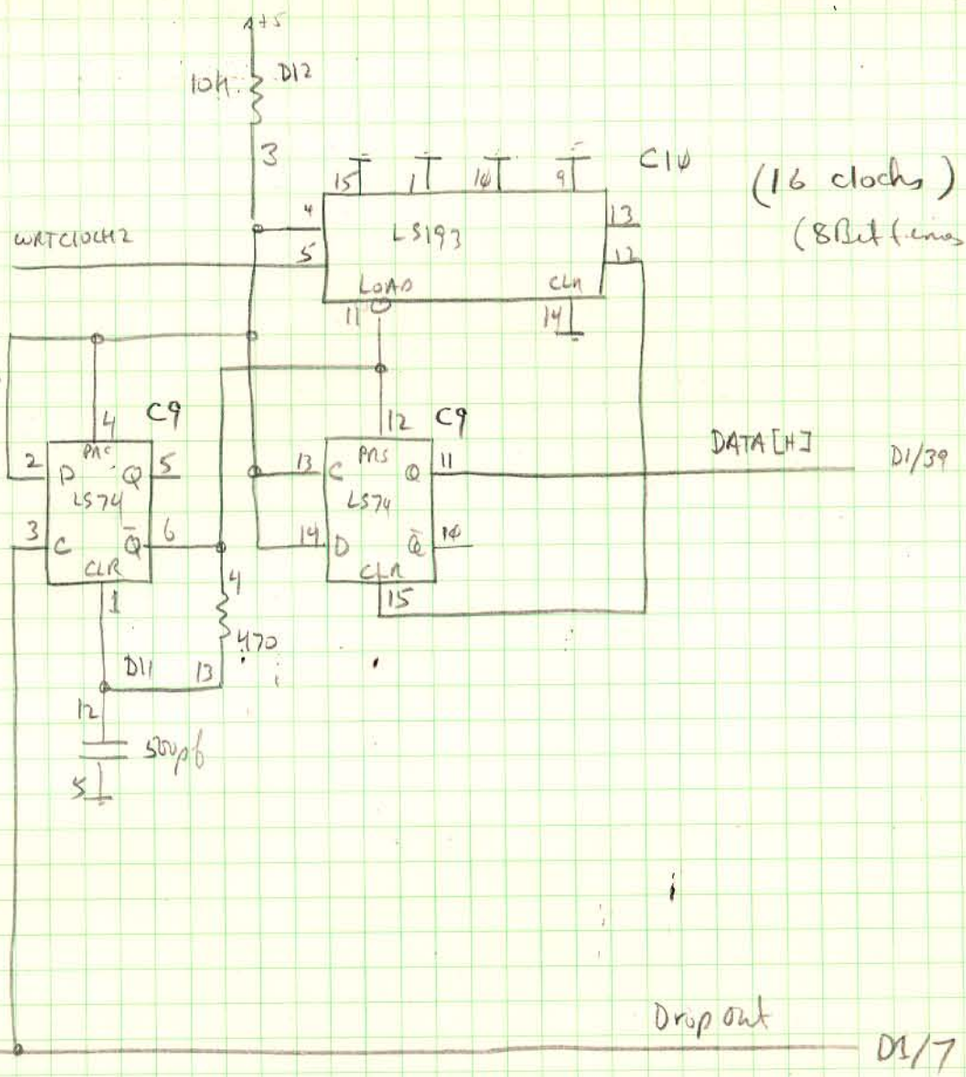
count up from clock transition to return transition
count down until next clock transition


'1'
B4
B5
B5
LS74
PRS
CLR
A4
A5
LS191
LOAD
Preset strobe
Up/down Control
D1
6802
Read Clock
DATA
C9/11
C7/13
C7/3
C3/10
C4/12
A2/2
Drop out
GAP
WRT clock
Write Data
CA1
CA2
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0

1 Jan 80
ARM

Data / GAP / Dropout Timing




+5
10K
D12
3
C10
15
1
10
9
(16 clocks)
(8 Bit (ones)
WRTCLOCK2
4
5
LS193
13
12
LOAD
CLR
11
14
4
C9
12
C9
2
PRE
P
Q
5
LS74
3
C
Q̄
6
CLR
1
13
C
PRE
Q
11
LS74
14
D
Q̄
10
CLR
15
DATA [H]
D1/39
4
470
D11
13
12
500pf
5
Drop out
D1/7

1 Jan 80
ABB

Position index

A1	RES	22, 23
A2	CA3140/CA3140	22, 23
A3	LS132	22, 23
A4	LS191	31
A5	LS191	31

A20	LS74	30
A21	LS193	30
A22	LS193	30
A23	LS193	30
A24	Switches	30

B1	LS74	22, 23
B2	---	
B3	Resistors	22, 23
B4	LS74	31
B5	LS74	31

B20	LS74	21
B21	LS193	21
B22	LS193	21
B23	Resistors	21, 30
B24	Switches	21

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ARD

C1	LS51	22, 23
C2	LSØ8	22, 23
C3	Resistors	22, 23
C4	LS153	31
C5	LSØØ	31
C6	LS193	32
C7	LSØØ	32
C8	LS193	32
C9	LS74	32
C10	LS193	32
C11	---	
C12	LS193	31
C13	---	
C14	---	
C15	LSØØ	15, 18, 19
C16	LS11	16, 18, 19
C17	LSØ8	15, 19
C18	LS173	19, 29
C19	LS173	19, 29
C20	LSØØ	15
C21	LSØ2	15
C22	LSØ2	14, 15, 18
C23	LS139	14
C24	LSØØ	14

D1	68B21	20, 22, 31
D3	68B21	20, 23, 24
D4	68B21	18, 20
D6	68B00	20
D7	7433	21
D8	Resistors	21
D9	LS132	18, 20, 21
D10	LS74	19, 21
D11	Resistors	18, 21, 28
D12	Resistors	17, 21, 31, 32
D13	LS138	20
D14	LS138	20
D15	LS175	18
D16	LS74	18
D17	LS74	19
D18	LS158	19
D19	Resistors	14, 15
D20	74S74	15
D21	74S74	15, 18
D22	LS08	15
D23	8136	14
D24	Resistors	14

2-Jan-80
BMD

E7	27Aø8 (Not used)	20
E9	27Aø8	20
E10	27Aø8	20
E12	68B10	20
E13	LS374	16
E14	LS374	16
E15	8838	16
E16	8838	16
E17	8838	19
E18	8838	19
E19	7438	14, 15
E20	7438	15
E21	8837	15, 18, 19
E22	8837	14
E23	8136	14
E24	Switch	14

F12	Switch	17
F13	LS244	17
F14	LS244	18
F		

F23	8136	14
F24	Switch	14

2 Jan 80
ARB

```
.IIF    NDF,.M68        .NLIST  ;CROSS-ASSEMBLER NOT LISTED
        ;DURING CHECKOUT DEFINE .M68 TO ENABLE LISTING
.IIF    DF,.M68         .LIST   SRC,SEQ,COM,MD,MC
        ;
        ;
        .TITLE  M6800 CROSS-ASSEMBLER
        ;
.IIF    DF,.M68 .SBTTL  CROSS-ASSEMBLER INTRODUCTION
        ;
.ENABLE ABS
        ;
        ;*************************************************************
        ;*                                                           *
        ;*      MACRO PACKAGE FOR THE MOTOROLA 6800 MICROPROCESSOR   *
        ;*              TO RUN UNDER MACRO 11.                       *
        ;*                                                           *
        ;*      BY ALAN R. BALDWIN                                   *
        ;*                                                           *
        ;*              V03 - OCTOBER 1980                           *
        ;*                                                           *
        ;*************************************************************
        ;
        ;
        ;THE FOLLOWING DIFFERENCES EXIST BETWEEN THIS CROSS-ASSEMBLER
        ;AND MOTOROLA'S M6800 ASSEMBLER
        ;       LABELS MUST TERMINATE WITH A :
        ;       COMMENTS START WITH A ;
        ;       IMMEDIATE MODE IS DENOTED BY A SEPERATE ARGUMENT - #
        ;
        ;
        ;DEFINITION OF ASSEMBLER DIRECTIVES WITH DIFFERENCES
        ;       END - USE       .END    END OF PROGRAM
        ;       EQU - USE  =            EQUATE SYMBOL
        ;       FCB                     FORM SINGLE-BYTE CONSTANT
        ;                               NO MORE THAN 10 ARGUMENTS
        ;       FCC   <ASCII CHRS>      FORM CONSTANT CHARACTERS
        ;       FDB                     FORM DOUBLE-BYTE CONSTANT
        ;                               NO MORE THAN 10 ARGUMENTS
        ;       MON - NOT IMPLEMENTED   RETURN TO MONITOR CONSOLE
        ;       NAM - USE       .SBTTL  PROGRAM NAME
        ;       OPT - NOT IMPLEMENTED   OPTION
        ;       ORG                     ORIGIN
        ;       PAGE - USE      .PAGE   ADVANCE LISTING TO TOP OF PAGE
        ;       RMB                     RESERVE MEMORY BYTES
        ;       SPC - NOT IMPLEMENTED   SPACE N LINES
        ;
        ;
        ;PROCESSOR CONDITION CODE REVIEW
        ;       0 - CARRY BIT (C)
        ;       1 - OVERFLOW BIT (V)
        ;       2 - ZERO BIT (Z)
        ;       3 - NEGATIVE BIT (N)
        ;       4 - INTERRUPT MASK BIT (I)
        ;       5 - HALF CARRY BIT (H)
        ;       6 - ALWAYS 1
        ;       7 - ALWAYS 1
        ;
.IIF    DF,.M68 .PAGE
.IIF    DF,.M68 .SBTTL  SINGLE BYTE 'INHERENT' INSTRUCTIONS
        ;
.MACRO  AINST   H,I
 .MACRO H
 .NLIST SRC
 .BYTE  I
 .LIST  SRC
 .ENDM
.ENDM   AINST
        ;
        ;
    ;MNEMONIC  OPCODE   ;OPERATION
AINST   NOP,    1       ;DO NOTHING
AINST   TAP,    6       ;A TO CC'S
AINST   TPA,    7       ;CC'S TO A
AINST   INX,    10      ;INCREMENT INDEX REGISTER
AINST   DEX,    11      ;DECREMENT INDEX REGISTER
AINST   CLV,    12      ;CLEAR V BIT
```

```
AINST   SEV,    13      ;SET C BIT
AINST   CLC,    14      ;CLEAR C BIT
AINST   SEC,    15      ;SET C BIT
AINST   CLI,    16      ;CLEAR I BIT
AINST   SEI,    17      ;SET I BIT
AINST   SBA,    20      ;ACCA=ACCA-ACCB
AINST   CBA,    21      ;COMPARE ACCA & ACCB
AINST   TAB,    26      ;ACCB=ACCA
AINST   TBA,    27      ;ACCA=ACCB
AINST   DAA,    31      ;DECIMAL ADJUST
AINST   ABA,    33      ;ACCA=ACCA+ACCB
AINST   TSX,    60      ;X=SP+1
AINST   INS,    61      ;SP=SP+1
AINST   PULA,   62      ;PULL A FROM STACK
AINST   PULB,   63      ;PULL B FROM STACK
AINST   DES,    64      ;SP=SP-1
AINST   TXS,    65      ;SP=X-1
AINST   PSHA,   66      ;PUSH A ONTO STACK
AINST   PSHB,   67      ;PUSH B ONTO STACK
AINST   RTS,    71      ;RETURN FROM SUBROUTINE
AINST   RTI,    73      ;RETURN FROM INTERRUPT
AINST   WAI,    76      ;WAIT FOR INTERRUPT
AINST   SWI,    77      ;SOFTWARE INTERRUPT
AINST   NEGA,   100     ;NEGATE A
AINST   COMA,   103     ;COMPLEMENT A
AINST   LSRA,   104     ;LOGICAL SHIFT RIGHT A
AINST   RORA,   106     ;ROTATE RIGHT A
AINST   ASRA,   107     ;ARITHMETIC SHIFT RIGHT A
AINST   ASLA,   110     ;ARITHMETIC SHIFT LEFT A
AINST   ROLA,   111     ;ROTATE LEFT A
AINST   DECA,   112     ;DECREMENT A
AINST   INCA,   114     ;INCREMENT A
AINST   TSTA,   115     ;TEST A
AINST   CLRA,   117     ;CLEAR A
AINST   NEGB,   120     ;NEGATE B
AINST   COMB,   123     ;COMPLEMENT B
AINST   LSRB,   124     ;LOGICAL SHIFT RIGHT B
AINST   RORB,   126     ;ROTATE RIGHT B
AINST   ASRB,   127     ;ARITHMETIC SHIFT RIGHT B
AINST   ASLB,   130     ;ARITHMETIC SHIFT LEFT B
AINST   ROLB,   131     ;ROTATE LEFT B
AINST   DECB,   132     ;DECREMENT B
AINST   INCB,   134     ;INCREMENT B
AINST   TSTB,   135     ;TEST B
AINST   CLRB,   137     ;CLEAR B
        ;
.IIF    DF,.M68 .PAGE
.IIF    DF,.M68 .SBTTL  PUSH AND PULL OPCODES
        ;
.MACRO  PKRNL   I,J
 .IIF   IDN     <J>,A   ...A=0  ;PSH/PUL A
 .IIF   IDN     <J>,B   ...A=1  ;PSH/PUL B
 .BYTE  I+...A          ;INVALID ARGUMENT
.ENDM
        ;
.MACRO  PINST   H,I
 .MACRO H       J
 .NLIST SRC
 PKRNL  I,J
 .LIST  SRC
 .ENDM
.ENDM   PINST
        ;
    ;MNEMONIC  OPCODE   ;OPERATION
PINST   PUL,    62      ;PUL BYTE FROM STACK S=S+1
PINST   PSH,    66      ;PUSH BYTE ONTO STACK S=S-1
        ;
.IIF    DF,.M68 .PAGE
.IIF    DF,.M68 .SBTTL  RELATIVE BRANCH INSTRUCTIONS
        ;
.MACRO  BKRNL   I,J
 ...A=J-.-2
 .IIF   LT,...A+200     .ERROR  ;BRANCH OUT OF RANGE
 .IIF   GE,...A-200     .ERROR  ;BRANCH OUT OF RANGE
 .BYTE  I,...A
.ENDM
```

```
        ;
.MACRO  BINST   H,I
 .MACRO H       J
 .NLIST SRC
 BKRNL  I,J
 .LIST  SRC
 .ENDM
.ENDM   BINST
        ;
        ;
    ;MNEMONIC  OPCODE   ;OPFERATION
BINST   BRA,    40      ;BRANCH ALWAYS
BINST   BHI,    42      ;BRANCH IF (C=0) AND (Z=0)
BINST   BLS,    43      ;BRANCH IF (C=1) OR (Z=1)
BINST   BCC,    44      ;BRANCH IF (C=0)
BINST   BCS,    45      ;BRANCH IF (C=1)
BINST   BNE,    46      ;BRANCH IF (Z=0)
BINST   BEQ,    47      ;BRANCH IF (Z=1)
BINST   BVC,    50      ;BRANCH IF (V=0)
BINST   BVS,    51      ;BRANCH IF (V=1)
BINST   BPL,    52      ;BRANCH IF (N=0)
BINST   BMI,    53      ;BRANCH IF (N=1)
BINST   BGE,    54      ;BRANCH IF (<N XOR V>=0)
BINST   BLT,    55      ;BRANCH IF (<N XOR V>=1)
BINST   BGT,    56      ;BRANCH IF (Z=0) AND (<N XOR V>=0)
BINST   BLE,    57      ;BRANCH IF (Z=1) OR (<N XOR V>=1)
BINST   BSR,    215     ;BRANCH TO SUBROUTINE
        ;
        ;
.IIF    DF,.M68 .PAGE
.IIF    DF,.M68 .SBTTL  INSTRUCTIONS HAVING ONLY ACCX,INDEXED,AND EXTENDED MODES
        ;
        ;
.MACRO  CKRNL   I,J,K
 .IF    NB,<K>          ;TWO ARGUMENTS - THEN INDEXED
  .IIF  DIF     <K>,X   .ERROR  ;INDEX BAD
  .IIF  LT,J    .ERROR  ;NEGATIVE OFFSET
  .BYTE I+40,J          ;OFFSET OUT OF RANGE
  .MEXIT
 .ENDC
 .IF    NB,<J>          ;ONE ARGUMENT - A, B, OR EXTENDED MODE
  ...A=60
  .IIF  IDN     <J>,A   ,...A=0         ;ACCA MODE
  .IIF  IDN     <J>,B   ,...A=20        ;ACCB MODE
  .IIF  NE,...A-60      .BYTE   I+...A
  .IIF  EQ,...A-60      .BYTE   I+...A,J&177400/400,J&377
  .MEXIT
 .ENDC
 .ERROR ;BAD INSTRUCTION
.ENDM
        ;
.MACRO  CINST   H,I
 .MACRO H       J,K
 .NLIST SRC
 CKRNL  I,J,K
 .LIST  SRC
 .ENDM
.ENDM   CINST
        ;
        ;

    ;MNEMONIC  OPCODE   ;OPERATION
        ;
CINST   NEG,    100     ;NEGATE
CINST   COM,    103     ;COMPLEMENT
CINST   LSR,    104     ;LOGICAL SHIFT RIGHT
CINST   ROR,    106     ;ROTATE RIGHT
CINST   ASR,    107     ;ARITHMETIC SHIFT RIGHT
CINST   ASL,    110     ;ARITHMETIC SHIFT LEFT
CINST   ROL,    111     ;ROTATE LEFT
CINST   DEC,    112     ;DECREMENT
CINST   INC,    114     ;INCREMENT
CINST   TST,    115     ;TEST
CINST   CLR,    117     ;CLEAR
        ;
        ;
```

```
        ;
.IIF    DF,.M68 .PAGE
.IIF    DF,.M68 .SBTTL  JUMP AND JSR INSTRUCTIONS
        ;
.MACRO  DKRNL   I,J,K
 .IF    NB,<K>          ;TWO ARGUMENTS - INDEXED MODE
  .IIF  DIF     <K>,X   .ERROR  ;BAD INDEX
  .IIF  LT,J            .ERROR  ;NEGATIVE OFFSET
  .BYTE I+40,J          ;OFFSET TOO LARGE
  .MEXIT
 .ENDC
 .IF    NB,<J>          ;ONE ARGUMENT - EXTENDED MODE
  .BYTE I+60,J&177400/400,J&377
  .MEXIT
 .ENDC
 .ERROR ;BAD INSTRUCTION
.ENDM
        ;
.MACRO  DINST   H,I
 .MACRO H       J,K
 .NLIST SRC
 DKRNL  I,J,K
 .LIST  SRC
 .ENDM
.ENDM   DINST
        ;
        ;
     ;MNEMONIC  OPCODE  ;OPERATION
DINST   JMP,    116     ;JUMP
DINST   JSR,    215     ;JUMP TO SUBROUTINE
        ;
        ;
.IIF    DF,.M68 .PAGE
.IIF    DF,.M68 .SBTTL  ALL ACCX INSTRUCTIONS
        ;
.MACRO  EKRNL   I,J,K,L
 ...A=-1
 .IIF   IDN     <J>,A   ,...A=0         ;ACCA MODE
 .IIF   IDN     <J>,B   ,...A=100       ;ACCB MODE
  .IF   GE,...A                 ;ACCX MODES
   .IF  NB,<L>                  ;THREE ARGS - IMMEDIATE/INDEXED
    .IF IDN     <K>,#   ;CHECK IMMEDIATE
     .IIF       EQ      <I>-207 ,.ERROR ;STA #
     .BYTE      I+...A,L
     .MEXIT
    .ENDC
    .IF IDN     <L>,X   ;CHECK INDEXED
     .IIF       LT,K    .ERROR  ;NEGATIVE OFFSET
     .BYTE      I+...A+40,K     ;OFFSET TOO LARGE
     .MEXIT
    .ENDC
    .ERROR      ;BAD INSTRUCTION
    .MEXIT
   .ENDC
   .IF  NB,<K>                  ;TWO ARGS - DIRECT/EXTENDED
    .IIF        EQ,K&177400     .BYTE   I+...A+20,K
    .IIF        NE,K&177400     .BYTE   I+...A+60,K&177400/400,K&377
    .MEXIT
   .ENDC
  .ENDC
 .ERROR ;BAD INSTRUCTION
.ENDM
        ;
.MACRO  EINST   H,I
 .MACRO H       J,K,L
 .NLIST SRC
 EKRNL  I,J,K,L
 .LIST  SRC
 .ENDM
.ENDM   EINST
        ;
        ;
     ;MNEMONIC  OPCODE  ;OPERATION
EINST   SUB,    200     ;SUBTRACT
EINST   CMP,    201     ;COMPARE
EINST   SBC,    202     ;SUBTRACT WITH CARRY
```

```
EINST   AND,    204     ;LOGICAL AND
EINST   BIT,    205     ;BIT TEST
EINST   LDA,    206     ;LOAD ACCUMULATOR
EINST   STA,    207     ;STORE ACCUMULATOR
EINST   EOR,    210     ;EXCLUSIVE OR
EINST   ADC,    211     ;ADD WITH CARRY
EINST   ORA,    212     ;LOGICAL OR
EINST   ADD,    213     ;ADD
        ;
        ;
.IIF    DF,.M68 .PAGE
.IIF    DF,.M68 .SBTTL  ALL SHORT FORM ACCX INSTRUCTIONS
        ;
.MACRO  SKRNL   I,J,K
 .IF    NB,<K>          ;TWO ARGS - IMMEDIATE/INDEXED
  .IF   IDN     <J>,#   ;CHECK IMMEDIATE
   .IIF EQ      <I>-207 ,.ERROR ;STAA #
   .IIF EQ      <I>-307 ,.ERROR ;STAB #
   .BYTE        I,K
   .MEXIT
  .ENDC
  .IF   IDN     <K>,X   ;CHECK INDEXED
   .IIF LT,J    .ERROR  ;NEGATIVE OFFSET
   .BYTE        I+40,J          ;OFFSET TOO LARGE
   .MEXIT
  .ENDC
  .ERROR        ;BAD INSTRUCTION
  .MEXIT
 .ENDC
 .IF    NB,<J>          ;ONE ARG - DIRECT/EXTENDED
  .IIF  EQ,J&177400     .BYTE   I+20,J
  .IIF  NE,J&177400     .BYTE   I+60,J&177400/400,J&377
  .MEXIT
 .ENDC
 .ERROR ;BAD INSTRUCTION
.ENDM
        ;
.MACRO  SINST   H,I
 .MACRO H       J,K
 .NLIST SRC
 SKRNL  I,J,K
 .LIST  SRC
 .ENDM
.ENDM   SINST
        ;
        ;
    ;MNEMONIC  OPCODE   ;OPERATION
        ;
SINST   SUBA,   200     ;SUBTRACT
SINST   SUBB,   300
SINST   CMPA,   201     ;COMPARE
SINST   CPMB,   301
SINST   SBCA,   202     ;SUBTRACT WITH CARRY
SINST   SBCB,   302
SINST   ANDA,   204     ;LOGICAL AND
SINST   ANDB,   304
SINST   BITA,   205     ;BIT TEST
SINST   BITB,   305
SINST   LDAA,   206     ;LOAD ACCUMULATOR
SINST   LDAB,   306
SINST   STAA,   207     ;STORE ACCUMULATOR
SINST   STAB,   307
SINST   EORA,   210     ;EXCLUSIVE OR
SINST   EORB,   310
SINST   ADCA,   211     ;ADD WITH CARRY
SINST   ADCB,   311
SINST   ORAA,   212     ;LOGICAL OR
SINST   ORAB,   312
SINST   ADDA,   213     ;ADD
SINST   ADDB,   313
        ;
        ;
.IIF    DF,.M68 .PAGE
.IIF    DF,.M68 .SBTTL  STACK AND INDEX REGISTER INSTRUCTIONS
        ;
.MACRO  FKRNL   I,J,K,L
```

```
 .IF    B,<K>           ;ONE ARG - DIRECT/EXTENDED MODE
  .IF   NB,<J>
   .IIF NE,J&177400     .BYTE   I+60,J&177400/400,J&377
   .IIF EQ,J&177400     .BYTE   I+20,J
   .MEXIT
  .ENDC
  .ERROR        ;BAD INSTRUCTION
  .MEXIT
 .ENDC
 .IF    IDN     <J>,#   ;IMMEDIATE MODE
  .IIF  EQ      <I>-217 ,.ERROR ;STS #
  .IIF  EQ      <I>-317 ,.ERROR ;STX #
  .IIF  NB,<L>  .BYTE   I,K,L
  .IIF  B,<L>   .BYTE   I,K&177400/400,K&377
  .MEXIT
 .ENDC
 .IF    B,<L>
  .IF   NB,<K>
   .IF  IDN     <K>,X           ;INDEXED
    .IIF        LT,J    .ERROR  ;NEGATIVE OFFSET
    .BYTE       I+40,J
    .MEXIT
   .ENDC
  .ENDC
 .ENDC
 .ERROR ;BAD INSTRUCTION
.ENDM
        ;
.MACRO  FINST   H,I
 .MACRO H       J,K,L
 .NLIST SRC
 FKRNL  I,J,K,L
 .LIST  SRC
 .ENDM
.ENDM   FINST
        ;
        ;
    ;MNEMONIC  OPCODE   ;OPERATION
        ;
FINST   CPX,    214     ;COMPARE TO INDEX
FINST   LDS,    216     ;LOAD STACK REGISTER
FINST   LDX,    316     ;LOAD INDEX REGISTER
FINST   STS,    217     ;STORE STACK REGISTER
FINST   STX,    317     ;STORE INDEX REGISTER
        ;
        ;
        ;
.IIF    DF,.M68 .PAGE
.IIF    DF,.M68 .SBTTL  ASSEMBLER DIRECTIVES
        ;
.MACRO  FCB     A,B,C,D,E,F,G,H,I,J
.NLIST  SRC
 .IIF   NB,<A>  .BYTE   A
 .IIF   NB,<B>  .BYTE   B
 .IIF   NB,<C>  .BYTE   C
 .IIF   NB,<D>  .BYTE   D
 .IIF   NB,<E>  .BYTE   E
 .IIF   NB,<F>  .BYTE   F
 .IIF   NB,<G>  .BYTE   G
 .IIF   NB,<H>  .BYTE   H
 .IIF   NB,<I>  .BYTE   I
 .IIF   NB,<J>  .BYTE   J
.LIST   SRC
.ENDM   FCB
        ;
.MACRO  FCC     H
.NLIST  SRC
.ASCII  /H/
.LIST   SRC
.ENDM   FCC
        ;
.MACRO  FDB     A,B,C,D,E,F,G,H,I,J
.NLIST  SRC
 .IIF   NB,<A>  .BYTE   A&177400/400,A&377
 .IIF   NB,<B>  .BYTE   B&177400/400,B&377
 .IIF   NB,<C>  .BYTE   C&177400/400,C&377
```

```
 .IIF   NB,<D>  .BYTE   D&177400/400,D&377
 .IIF   NB,<E>  .BYTE   E&177400/400,E&377
 .IIF   NB,<F>  .BYTE   F&177400/400,F&377
 .IIF   NB,<G>  .BYTE   G&177400/400,G&377
 .IIF   NB,<H>  .BYTE   H&177400/400,H&377
 .IIF   NB,<I>  .BYTE   I&177400/400,I&377
 .IIF   NB,<J>  .BYTE   J&177400/400,J&377
.LIST   SRC
.ENDM   FDB
        ;
.MACRO  ORG     H
.NLIST  SRC
.=<H>
.LIST   SRC
.ENDM   ORG
        ;
.MACRO  RMB     H
.NLIST  SRC
.BLKB   H
.LIST   SRC
.ENDM   RMB
        ;
        ;
        ;
.NLIST  TTM     ;PRINTING MODE
.LIST   MD,MEB  ;ENABLE PRINTING OF MACRO EXPANSIONS
.LIST           ;LIST PROGRAM PROPER
        .PAGE
```

```
        .TITLE  DUAL CASSETTE DRIVE SOFTWARE
        ;
        ;*********************************************************
        ;*                                                       *
        ;*                                                       *
        ;*        THIS SOFTWARE IS FOR A DUAL CASSETTE           *
        ;*      DRIVE SYSTEM UTILIZING A MOTOROLA M68B00         *
        ;*      MICROPROCESSOR.                                  *
        ;*                                                       *
        ;*                                                       *
        ;*              WRITTEN BY    ALAN R. BALDWIN            *
        ;*                              JULY  1979               *
        ;*              COMPLETED       JANUARY  1980            *
        ;*                                                       *
        ;*********************************************************
        ;
        ;
        ;
        .PAGE
        .SBTTL  SPECIAL MACRO'S
        ;
        .MACRO  SETBIT  I,J
        LDA A   I
        ORA A   #,J
        STA A   I
        .ENDM   SETBIT
        ;
        ;
        .MACRO  CLRBIT  I,J
        LDA A   I
        AND A   #,377-J
        STA A   I
        .ENDM   CLRBIT
        ;
        ;
        .MACRO  BITTST  I,J
        LDA A   I
        BIT A   #,J
        .ENDM   BITTST
        ;
        ;
        .MACRO  STRBL   I,J
        LDA A   I
        AND A   #,377-J
        STA A   I
        ORA A   #,J
        STA A   I
        .ENDM   STRBL
        ;
        ;
        .MACRO  STRBH   I,J
        LDA A   I
        ORA A   #,J
        STA A   I
        AND A   #,377-J
        STA A   I
        .ENDM   STRBH
        ;
        ;
        .PAGE
        .MACRO SETBTX   I,J
        LDA A   I,X
        ORA A   #,J
        STA A   I,X
        .ENDM   SETBTX
        ;
        ;
        .MACRO  CLRBTX  I,J
        LDA A   I,X
        AND A   #,377-J
        STA A   I,X
        .ENDM   CLRBTX
        ;
        ;
        .MACRO  BTTSTX  I,J
        LDA A   I,X
        BIT A   #,J
```

```
        .ENDM   BTTSTX
        ;
        ;
        .MACRO  STRBLX  I,J
        LDA A   I,X
        AND A   #,377-J
        STA A   I,X
        ORA A   #,J
        STA A   I,X
        .ENDM   STRBLX
        ;
        ;
        .MACRO  STRBHX  I,J
        LDA A   I,X
        ORA A   #,J
        STA A   I,X
        AND A   #,377-J
        STA A   I,X
        .ENDM   STRBHX
        ;
        ;
        .MACRO  STORX   I,J
        LDA A   #,J
        STA A   I,X
        .ENDM   STORX
        ;
        .PAGE
        .SBTTL  VARIABLE DEFINITIONS
        ;
        STACK   =       77              ;SET STACK POSITION
        ;
        ORG     100             ;VARIABLES AREA
        ;
VA.1:   .BYTE   0       ;RDYFLG(DEV.1)
VB.1:   .BYTE   0       ;RWSTAT(DEV.1)
VC.1:   .BYTE   0       ;DVSTAT(DEV.1)
VD.1:   .BYTE   0
VA.0:   .BYTE   0       ;RDYFLG(DEV.0)
VB.0:   .BYTE   0       ;RWSTAT(DEV.0)
VC.0:   .BYTE   0       ;DVSTAT(DEV.0)
VD.0:   .BYTE   0
EXSTAT: .BYTE   0       ;SAVED STATUS FROM PDP-11
EXCMD:  .BYTE   0       ;SAVED COMMAND FROM PDP-11
DEV.X:  .BYTE   0,0     ;SELECTED DEVICE INDEX
T.WAIT: .BYTE   0,0     ;WAIT LOOP COUNTER
CRC:    .BYTE   0,0     ;CRC VALUE
SVCRC:  .BYTE   0,0     ;SAVED CRC VALUE
RWDATA: .BYTE   0       ;READ / WRITE  DATA
LPCNTR: .BYTE   0       ;LOOP COUNTER
        ;
        .PAGE
        .SBTTL  INTERRUPT LINKAGE
        ;
        ORG     177770  ;VECTOR AREA
IRQ:    FDB     PWRUP   ;SET ALL FOR POWER UP RESTART
SWI:    FDB     PWRUP
NMI:    FDB     PWRUP
RES:    FDB     PWRUP
        ;
        ;
        ORG     174000          ;ORIGIN THIS SEGMENT
        ;
PWRUP:  LDS     #,STACK         ;SET UP STACK
        CLR     ODAT            ;INITIALIZE REGISTER
        LDA A   #,100           ;POWER UP ERROR
        STA A   VC.0
        STA A   VC.1
        LDA A   #,210           ;INIT TO READY AND PROGRAMMED
        STA A   VB.0            ;PROGRAMMED, AND READY
        STA A   VB.1
        LDA A   #,2             ;SET UP READY FLAGS
        STA A   VA.0
        ASL A
        STA A   VA.1
        ;
        .PAGE
```

```
        .SBTTL  INITIALIZATION OF COMMAND REGISTER 68B21 PIA D4
        ;
        ;       THE COMMAND REGISTER IS A TWO BYTE
        ;       STATUS AND CONTROL REGISTER WHICH INTERFACES WITH THE
        ;       PDP-11 UNIBUS.
        ;
                TSTAT   =       200
        ;       TSTAT IS THE ERROR/READY STATUS REGISTER
        ;
        ;       7-      GO BIT (H-COMMAND ISSUED)       (IN)
        ;       6-      ERROR                           (OUT)
        ;       5-      BLOCK CHECK ERROR               (OUT)
        ;       4-      FILE GAP                        (OUT)
        ;       3-      TIMING ERROR                    (OUT)
        ;       2-      UNIT 1 READY(H)                 (OUT)
        ;       1-      UNIT 0 READY(H)                 (OUT)
        ;       0-      UNIT SELECTED                   (IN)
        ;
                TCMD    =       201
        ;       TCMD IS THE COMMAND/TRANSFER REGISTER
        ;
        ;       7-      TR SERVICED (H)                 (IN)
        ;       6-      CLEAR TR (L)                    (OUT)
        ;       5-      ---
        ;       4-      ---
        ;       3-      ILBS FLAG                       (IN)
        ;       2-      FUNCTION BIT 2                  (IN)
        ;       1-      FUNCTION BIT 1                  (IN)
        ;       0-      FUNCTION BIT 0                  (IN)
        ;
                PD4BC   =       202
                PD4AC   =       203
        ;
        ;       PD4(A/B)C ARE THE PIA CONTROL REGISTERS
        ;       PD4BC IS PAIRED WITH TSTAT
        ;       PD4AC IS PAIRED WITH TCMD
        ;
        LDX     #,0,0           ;ACCESS DIRECTION REGISTERS
        STX     PD4BC           ;LOAD BOTH B & A
        LDX     #,176,100       ;SET INPUTS & OUTPUTS
        STX     TSTAT           ;IN BOTH TSTAT & TCMD
        LDX     #,4,4           ;ACCESS DATA REGISTERS
        STX     PD4BC
        LDX     #,0,0           ;SET BOTH UNITS NOT READY
        STX     TSTAT
        CLR     CLRGOH          ;ENABLE READY
        ;
        .PAGE
        .SBTTL  INITIALIZE TRANSPORT 0 68B21 PIA
        ;
        ;         THE 68B21 PIA D1 CONTAINS TWO 8 BIT
        ;       CONTROL REGISTERS:
        ;
                TMC0    =       210
        ;       1. TRANSPORT 0 MOTION CONTROL
        ;
        ;       7-      CLEAR LEADER (H)                (IN)
        ;       6-      WRITE ENABLE (H)                (IN)
        ;       5-      CASSETTE IN PLACE (H)           (IN)
        ;       4-      REWIND DONE (H)                 (IN)
        ;       3-      DISABLE REWIND (L)              (OUT)
        ;       2-      ALLOW WRITE (L)                 (OUT)
        ;       1-      REVERSE (L)                     (OUT)
        ;       0-      FORWORD (L)                     (OUT)
        ;
                RWCSR0  =       211
        ;       2. TRANSPORT R/W STATUS REGISTER 0
        ;
        ;       7-      READ DATA                       (IN)
        ;       6-      DATA                            (IN)
        ;       5-      DROP OUT                        (IN)
        ;       4-      GAP                             (IN)
        ;       3-      READ CLOCK                      (IN)
        ;       2-      WRITE CLOCK                     (IN)
        ;       1-      ---
        ;       0-      WRITE DATA                      (OUT)
```

```
;
        PD1BC   =       212
        PD1AC   =       213
;       PD1(A/B)C ARE PIA CONTROL REGISTERS
;       PD1BC IS PAIRED WITH TMC0
;       PD1AC IS PAIRED WITH RWCSR0
;
LDX     #,4,4           ;SET FOR DATA REGISTERS
STX     PD1BC
LDX     #,17,0          ;SET FOR NO MOTION/WRITING
STX     TMC0
LDX     #,0,0           ;ACCESS DIRECTION REGISTERS
STX     PD1BC
LDX     #,17,1          ;SET INPUTS AND OUTPUTS
STX     TMC0
LDX     #,76,6          ;CB1(REWIND DONE +) / CB2(OUT)
                        ;CA1(READ CLOCK +) / CA2(DATA -), DATA
STX     PD1BC
;
.PAGE
.SBTTL  INITIALIZE TRANSPORT 1 68B21 PIA
;
;         THE 68B21 PIA D3 CONTAINS TWO 8 BIT
;       CONTROL REGISTERS:
;
        TMC1    =       204
;       1. TRANSPORT 1 MOTION CONTROL
;
;       7-      CLEAR LEADER (H)                (IN)
;       6-      WRITE ENABLE (H)                (IN)
;       5-      CASSETTE IN PLACE (H)           (IN)
;       4-      REWIND DONE (H)                 (IN)
;       3-      DISABLE REWIND (L)              (OUT)
;       2-      ALLOW WRITE (L)                 (OUT)
;       1-      REVERSE (L)                     (OUT)
;       0-      FORWORD (L)                     (OUT)
;
        RWCSR1  =       205
;       2. TRANSPORT R/W STATUS REGISTER 1
;
;       7-      ---
;       6-      ---
;       5-      CLEAR REWIND 1 (L)              (OUT)
;       4-      CLEAR REWIND 0 (L)              (OUT)
;       3-      ---
;       2-      WRITE DATA ENABLE (H)           (OUT)
;       1-      ---
;       0-      READ UNIT SELECT                (OUT)
;
        PD3BC   =       206
        PD3AC   =       207
;       PD3(A/B)C ARE PIA CONTROL REGISTERS
;       PD3BC IS PAIRED WITH TMC1
;       PD3AC IS PAIRED WITH RWCSR1
;
LDX     #,4,4           ;SET FOR DATA REGISTERS
STX     PD3BC
LDX     #,17,60         ;SET FOR NO MOTION
STX     TMC1
LDX     #,0,0           ;ACCESS DIRECTION REGISTERS
STX     PD3BC
LDX     #,17,377        ;SET INPUTS AND OUTPUTS
STX     TMC1
LDX     #,76,26         ;CB1(REWIND DONE +) / CB2(OUT)
                        ;CA1(WRT CLK +) / CA2(DROP OUT +), DATA
STX     PD3BC
;
.PAGE
.SBTTL  REGISTER DEFINITIONS
;
;       8-BIT INPUT DATA REGISTER FROM PDP-11 UNIBUS
        IDAT    =       230
;
;       8-BIT OUTPUT DATA REGISTER TO PDP-11 UNIBUS
        ODAT    =       234
;
```

```
        ;       INPUT SET TR FLAG REGISTER
                ISETTR  =       220
        ;
        ;       OUTPUT SET TR FLAG REGISTER
                OSETTR  =       224
        ;
        ;       CLEAR GOH / ENABLE READY FLAGS TO PDP-11
                CLRGOH  =       214
        ;
        ;
        ;       INDEXED MODE DEVICE REGISTERS AND
        ;       STATUS REGISTER DEFINITIONS
        ;
                DEV.0   =       10
                DEV.1   =       4
        ;
                TMC     =       200
                TRWND   =       202
        ;
                RDYFLG  =       74      ;=2 (DEV.0), =4 (DEV.1)
        ;
                RWSTAT  =       75
        ;       7-      OPERATION DONE  (1)
        ;       4-      REWIND DONE     (1)
        ;       3-      PROGRAMMED      (1)
        ;       0-      EOT (0) / BOT (1)
        ;
                DVSTAT  =       76      ;ERROR FLAGS (SEE TSTAT)
        ;       7-      ILBS / LAST BYTE CRC
        ;       6-      ERROR                   (1)
        ;       5-      BLOCK CHECK ERROR       (1)
        ;       4-      FILE GAP                (1)
        ;       3-      TIMING ERROR            (1)
        ;       0-      ILBS / FIRST BYTE CRC
        ;
        ;
        ;       THESE DEFINITIONS ARE USED BY ALL FUNCTION
        ;       ROUTINES TO ALLOW UNIT INDEPENDENT HANDLERS
        ;       TO BE WRITTEN.
        ;
        .PAGE
        .SBTTL  CHECK FOR COMMAND SCANNER
        ;
        ;       TRANSPORT STATUS SCANNER
        ;
        LDA A   #,1             ;INIT FOR TSTC.A
TSTC.A: DEC A                   ;NEED TO CHECK TRANSPORT STATUS ?
        BNE     TSTCMD          ;IF NOT - SKIP
        LDX     #,DEV.0         ;SET UP FOR DEVICE 0
        STX     DEV.X           ;SAVE POINTER
        SETBTX  TMC,10          ;ENABLE REWINDING
        JSR     SCANTR
        LDX     #,DEV.1         ;SET UP FOR DEVICE 1
        STX     DEV.X           ;SAVE POINTER
        SETBTX  TMC,10          ;ENABLE REWINDING
        JSR     SCANTR
        CLR A                   ;RESET COUNTER
        BRA     TSTCMD
        ;
        ;       COMMAND TERMINATION
        ;
LDRCHK: LDA A   TMC,X           ;CHECK FOR CLEAR LEADER
        BPL     DONE            ;ON OXIDE - SKIP
ERDONE: SETBTX  DVSTAT,100      ;ERROR
DONE:   CLRBIT  TCMD,100        ;CLEAR TR
        LDA A   TSTAT           ;GET STATUS WORD
        AND A   #,6             ;SAVE ONLY READY'S
        ORA A   DVSTAT,X        ;ADD IN NEW STATUS
        STA A   TSTAT           ;GET FLAGS OUT
        ORA A   RDYFLG,X        ;SET READY FLAG
        STA A   TSTAT           ;SEND TO PDP-11
        SETBTX  TMC,10          ;ALLOW REWIND
        CLR A                   ;RESET COUNTER
        ;
        ;       COMMAND SCANNER
        ;
```

```
TSTCMD: LDX     TSTAT           ;GET STATUS
        BPL     TSTC.A          ;NO COMMAND - BRANCH
        STX     EXSTAT          ;SAVE THE COMMAND
        LDA A   EXSTAT          ;GET THE SELECT
        AND A   #,1             ;FIND WHICH UNIT SELECTED
        BNE     TSTC.B          ;IF UNIT 1 - SKIP
        LDX     #,DEV.0         ;DEVICE 0 SELECTED
        CLRBIT  RWCSR1,1        ;SET READ SELECT UNIT 0
        BRA     TSTC.C
TSTC.B: LDX     #,DEV.1         ;DEVICE 1 SELECTED
        SETBIT  RWCSR1,1        ;SET READ SELECT UNIT 1
TSTC.C: STX     DEV.X           ;SAVE SELECTED DEVICE POINTER
        ;
        ;
        LDA A   RDYFLG,X        ;GET READY FLAG
        COM A                   ;MAKE MASK
        AND A   TSTAT           ;MASK OUT SELECTED READY
        STA A   TSTAT           ;SET READY FLAGS
        STA A   CLRGOH          ;LET PDP-11 SEE READY'S
        CLR     DVSTAT,X        ;NEW COMMAND
        LDA B   TMC,X           ;GET DEVICE STATUS
        AND B   #,367           ;DISABLE REWIND
        STA B   TMC,X           ;SEND TO DEVICE
        BMI     TSTC.D          ;ON CLEAR LEADER - SKIP
        CLRBTX  RWSTAT,1        ;CLEAR BOT FLAG
TSTC.D: AND B   #,60            ;CHECK IN PLACE AND REWIND DONE
        CMP B   #,60
        BNE     ERDONE          ;IF NOT - ERROR
        ;
        .PAGE
        .SBTTL  COMMAND DISPATCH ROUTINE
        ;
        LDA B   EXCMD           ;GET COMMAND
        AND B   #,7             ;MASK OUT OTHER
        TBA                     ;SAVE IN A
        ABA
        ABA                     ;3*COMMAND
        CLR B
        ADD A   #,JMPTBL&377    ;LOW ORDER TABLE ADDRESS
        ADC B   #,JMPTBL&177400/400
        PSH A                   ;PLACE ADDRESS ON STACK
        PSH B
        RTS                     ;GO TO JUMP TABLE
        ;
JMPTBL: JMP     WFG             ;WRITE FILE GAP
        JMP     WRITE           ;WRITE DATA
        JMP     READ            ;READ DATA
        JMP     SRF             ;SPACE REVERSE FILE
        JMP     SRB             ;SPACE REVERSE BLOCK
        JMP     SFF             ;SPACE FORWARD FILE
        JMP     SFB             ;SPACE FORWARD BLOCK
        JMP     REWIND          ;REWIND
        ;
        .PAGE
        .SBTTL  TRANSPORT SCANNING ROUTINE
        ;
        ; 1.    CHECK FOR REWINDING
        ;       IF REWINDING THEN:
        ;               CLEAR OPERATION DONE FLAG
        ;               CLEAR REWIND DONE FLAG
        ;               CLEAR READY STATUS TO PDP-11
        ;               SET PROGRAMMED FLAG
        ;
SCANTR: LDA A   TMC,X           ;GET TRANSPORT MOTION
        AND A   #,20            ;PHYSICALLY REWINDING ?
        BNE     SCAN.A          ;IF NOT - SKIP
        ORA A   #,157           ;MASK OUT OPERATION DONE
        AND A   RWSTAT,X        ;MASK IN OTHER FLAGS
        ORA A   #,10            ;SET PROGRAMMED
        STA A   RWSTAT,X        ;SAVE NEW STATUS
        LDA A   RDYFLG,X        ;GET READY FLAG
        COM A                   ;MAKE A MASK
        AND A   TSTAT           ;MASK IN CURRENT STATUS
        STA A   TSTAT           ;SEND NEW STATUS TO PDP-11
        ;
        ; 2.    CHECK REWINDING STATUS
```

```
        ;       IF REWINDING THEN SCAN FOR COMPLETION
        ;       UPON COMPLETION:
        ;               SET REWIND DONE FLAG
        ;               SET OPERATION COMPLETE FLAG
        ;               SET BOT FLAG
        ;
SCAN.A: LDA A   RWSTAT,X        ;GET STATUS
        BIT A   #,20            ;ARE WE REWINDING ?
        BNE     SCAN.C          ;IF NOT - SKIP
        LDA A   TMC,X           ;IF SO - THEN GET MOTION STATUS
        AND A   #,20            ;FINISHED YET ?
        BEQ     SCAN.C          ;IF NOT - SKIP
        ORA A   RWSTAT,X        ;ELSE MASK IN STATUS
        ORA A   #,201           ;SET BOT AND OPERATION COMPLETE FLAGS
        STA A   RWSTAT,X        ;SAVE STATUS
        JSR     STOP            ;STOP MOTION AND WAIT
        ;
        ; 3.    CHECK OPERATION DONE FLAG
        ;       IF SET THEN
        ;               CHECK CASSETTE IN PLACE: IF NOT
        ;                       CLEAR BOT FLAG
        ;
SCAN.C: LDA A   RWSTAT,X        ;GET STATUS
        BPL     SCAN.F          ;IF NOT DONE - SKIP
        LDA B   TMC,X           ;GET TRANSPORT CONTROL
        BIT B   #,40            ;CASSETTE IN PLACE ?
        BNE     SCAN.D          ;IF SO - SKIP
        AND A   #,376           ;ELSE CLEAR BOT FLAG
        STA A   RWSTAT,X        ;AND SAVE NEW STATUS
        ;
        ; 4.    CHECK PROGRAMMED FLAG: IF SET THEN
        ;               CLEAR PROGRAMMED FLAG
        ;               SET ERROR BIT IF
        ;                       NOT CLEAR LEADER OR NOT IN PLACE
        ;               SET READY FLAG TO PDP-11
        ;
SCAN.D: BIT A   #,10            ;PROGRAMMED ?
        BEQ     SCAN.F          ;IF NOT - SKIP
        AND A   #,367           ;CLEAR PROGRAMMED FLAG
        STA A   RWSTAT,X        ;SAVE STATUS
        LDA A   TSTAT           ;GET STATUS
        AND A   #,6             ;SAVE ONLY READY'S
        AND B   #,240           ;CHECK IN PLACE AND CLEAR LEADER
        CMP B   #,240           ;BOTH SET ?
        BEQ     SCAN.E          ;IF SO - SKIP
        ORA A   #,100           ;ELSE SET ERROR BIT
SCAN.E: STA A   TSTAT           ;GET FLAGS OUT
        ORA A   RDYFLG,X        ;SET READY FLAG
        STA A   TSTAT           ;SEND STATUS TO PDP-11
SCAN.F: RTS                     ;FINISHED
        ;
        .PAGE
        .SBTTL  WRITE FILE GAP COMMAND - WFG
        ;
WFG:    LDA B   TMC,X           ;GET STATUS
        BIT B   #,100           ;WRITE ENABLED ?
        BEQ     WFG.E           ;IF NOT - ERROR
        TST B                   ;A CLEAR LEADER ?
        BPL     WFG.A           ;IF NOT - GO
        BTTSTX  RWSTAT,1        ;AT BOT ?
        BEQ     WFG.E           ;IF NOT - ERROR
WFG.A:  CLRBIT  RWCSR1,4        ;WRITE DATA DISABLED
        CLRBTX  TMC,5           ;FORWARD / ALLOW WRITE
        TST B                   ;STARTING IN CLEAR LEADER ?
        BPL     WFG.C           ;IF NOT - SKIP
        ;
        ;       WFG FROM BOT CLEAR LEADER
        ;
WFG.B:  LDA A   TMC,X           ;KEEP CHECKING CLEAR LEADER
        BMI     WFG.B           ;LOOP
        JSR     WC.4            ;EXTENDED GAP
        ;
        ;       WFG ON OXIDE
        ;
WFG.C:  JSR     WC.4            ;NORMAL GAP
WFG.D:  JSR     STOP            ;STOP TRANSPORT
```

```
        SETBTX  TMC,4           ;DISABLE WRITE
        BMI     WFG.E           ;IF CLEAR LEADER - ERROR
        JMP     DONE            ;FINISHED
WFG.E:  JMP     ERDONE          ;FINISH UP COMMAND
        ;
        .PAGE
        .SBTTL  WRITE COMMAND - WRITE
        ;
WRITE:  LDA B   TMC,X           ;CHECK DEVICE
        BIT B   #,100           ;WRITE ENABLED ?
        BEQ     WRIT.C          ;IF NOT - ERROR
        TST B                   ;CLEAR LEADER ?
        BPL     WRIT.A          ;IF NOT - SKIP
        BTTSTX  RWSTAT,1        ;AT BOT ?
        BEQ     WRIT.C          ;IF NOT - AT EOT
WRIT.A: CLRBIT  RWCSR1,4        ;WRITE DATA DISABLED
        CLRBTX  TMC,5           ;FORWARD / ALLOW WRITE
        LDX     #,6250.         ;WAIT 25 MS. TO REACH SPEED
        DEX
        BNE     .-1             ;LOOP UNTIL TIME UP
        LDX     DEV.X           ;GET POINTER
        TST B                   ;CLEAR LEADER ?
        BPL     WRIT.D          ;IF NOT - SKIP
WRIT.B: LDA A   TMC,X           ;READ STATUS
        BMI     WRIT.B          ;LOOP UNTIL OFF CLEAR LEADER
        JSR     WC.4            ;EXTENDED GAP AT BOT
        JSR     WC.4
        BCC     WRIT.E
WRIT.C: JMP     WRIT.Q          ;ERROR RETURN
WRIT.D: JSR     WC.1            ;NORMAL GAP
        BCS     WRIT.C          ;ERROR - CLEAR LEADER
WRIT.E: SETBIT  TCMD,100        ;ENABLE TR'S
        STA A   ISETTR          ;SET TR TO PDP-11
        LDA A   RWCSR1          ;CLEAR CLOCK FLAG
WRIT.F: LDA A   PD3AC           ;WAIT FOR CLOCK
        BPL     WRIT.F          ;LOOP
        SETBIT  RWCSR1,4        ;ENABLE WRITE DATA / CLEAR CLOCK FLAG
        CLRBIT  RWCSR0,1        ;PREAMBLE 0'S
        LDX     #,0             ;CLEAR CRC
        STX     CRC
        LDX     DEV.X           ;GET DEVICE POINTER
        LDA B   #,31.           ;31. MORE ZERO'S
WRIT.G: LDA A   PD3AC           ;CHECK CLOCK FLAG
        BPL     WRIT.G          ;LOOP
        LDA A   RWCSR1          ;CLEAR CLOCK FLAG
        DEC B                   ;0'S DONE ?
        BNE     WRIT.G          ;LOOP UNTIL FINISHED
WRIT.H: LDA A   PD3AC           ;CHECK FLAG
        BPL     WRIT.H          ;LOOP
        LDA A   RWCSR1          ;CLEAR CLOCK FLAG
        SETBIT  RWCSR0,1        ;SET FRAME BIT
WRIT.I: BITTST  TCMD,10         ;ILBS SET ?
        BNE     WRIT.J          ;IF SO - SKIP
        BIT A   #,200           ;TR SERVICED ?
        BEQ     WRIT.K          ;IF SO - SKIP
        SETBTX  DVSTAT,110      ;SET ERROR / TIMING
WRIT.J: SETBTX  DVSTAT,1        ;ILBS / FIRST BYTE CRC
        LDA A   CRC+1           ;SAVE THE CRC
        LDA B   CRC
        STA A   SVCRC+1
        STA B   SVCRC
        BRA     WRIT.L
WRIT.K: LDA A   IDAT            ;GET DATA FROM PDP-11
        STA A   ISETTR          ;SET TR TO PDP-11
WRIT.L: STA A   ODAT            ;LOAD OUTPUT REGISTER
        STA A   RWDATA          ;SAVE DATA
        LDA A   #,10            ;8. BITS PER BYTE
        STA A   T.WAIT+1        ;SAVE COUNT
WRIT.M: JSR     WTCRC           ;WRITE DATA / COMPUTE CRC
        LDA A   TMC,X           ;CHECK FOR CLEAR LEADER
        BMI     WRIT.P          ;IF SO - BRANCH
        DEC     T.WAIT+1        ;DONE ?
        BNE     WRIT.M          ;IF NOT - LOOP
        LDA B   DVSTAT,X        ;GET STATUS
        BMI     WRIT.N          ;CHECK FOR END OF ILBS
        BIT B   #,1             ;ILBS / FIRST BYTE CRC ?
```

```
        BEQ     WRIT.I          ;IF NOT - LOOP
        ORA B   #,200           ;ILBS SET
        STA B   DVSTAT,X
        LDA A   SVCRC           ;GET LAST BYTE OF CRC
        BRA     WRIT.L
WRIT.N: LDA A   PD3AC           ;WAIT FOR CLOCK
        BPL     WRIT.N
        LDA A   RWCSR1          ;CLEAR CLOCK FLAG
        CLR     RWCSR0          ;SET FINAL BIT = 0
        LDA B   #,2             ;SET UP FOR 2 ZERO BITS
WRIT.O: LDA A   PD3AC           ;WAIT FOR CLOCK
        BPL     WRIT.O
        LDA A   RWCSR1          ;CLEAR CLOCK FLAG
        DEC B                   ;ZERO'S DONE ?
        BNE     WRIT.O          ;IF NOT - LOOP
WRIT.P: CLRBIT  RWCSR1,4        ;TERMINATE DATA WRITING
        JSR     WC.3            ;WAIT A WHILE
        JSR     STOP            ;STOP MOTION
WRIT.Q: SETBTX  TMC,4           ;DISABLE WRITE
        JMP     LDRCHK          ;CHECK CLEAR LEADER
        ;
        .PAGE
        .SBTTL  READ COMMAND - READ
        ;
READ:   JSR     FORWRD          ;START MOTION, FIND PREAMBLE
        BEQ     READ.A          ;IF NO ERROR - SKIP
        JMP     ERDONE          ;ELSE TERMINATE IN ERROR
READ.A: BITTST  RWCSR0,160      ;GAP ?
        BEQ     READ.F          ;ERROR - USE BLOCK CHECK
        TST A                   ;FRAME BIT FOUND ?
        BPL     READ.A          ;IF NOT - LOOP
        SETBIT  TCMD,100        ;ENABLE TR (TRANSFER REQUESTS)
        LDX     #,0             ;INIT CRC
        STX     CRC
        LDX     DEV.X           ;POINT TO DEVICE
        LDA A   RWCSR0          ;CLEAR CLOCK FLAG
READ.B: JSR     RDCRC           ;GET BIT 0
        JSR     RDCRC           ;GET BIT 1
        JSR     RDCRC           ;GET BIT 2
        JSR     RDCRC           ;GET BIT 3
        JSR     RDCRC           ;GET BIT 4
        JSR     RDCRC           ;GET BIT 5
        LDA A   TMC,X           ;CHECK CLEAR LEADER
        BMI     READ.G          ;ERROR - BRANCH
        JSR     RDCRC           ;GET BIT 6
        BITTST  RWCSR0,100      ;CHECK DATA FLAG
                                ;=1 ON DROPOUT
        BEQ     READ.C          ;NO ERROR - SKIP
        SETBTX  DVSTAT,140      ;ERROR - DROP OUT (USE BLOCK CHECK)
READ.C: JSR     RDCRC           ;GET BIT 7
        BITTST  RWCSR0,160      ;IN A GAP ?
        BEQ     READ.F          ;ERROR - USE BLOCK CHECK
        LDA B   TCMD            ;WAS TR SERVICED ?
        BPL     READ.D          ;IF SO SKIP
        SETBTX  DVSTAT,110      ;ERROR / TIMING ERROR
READ.D: LDA A   RWDATA          ;GET READ DATA
        STA A   ODAT            ;SEND TO INTERFACE
        STA A   OSETTR          ;SET TR FLAG TO PDP-11
        BIT B   #,10            ;TR SERVICED BY AN ILBS ?
        BEQ     READ.B          ;IF NOT - GET NEXT BYTE
READ.E: LDX     CRC             ;CHECK CRC
        BEQ     READ.G          ;IF GOOD - SKIP
        LDX     DEV.X           ;GET POINTER
READ.F: SETBTX  DVSTAT,140      ;ERROR / BLOCK CHECK
READ.G: JSR     GAP             ;WAIT FOR GAP
        JSR     WC.2            ;WAIT A WHILE
        JSR     STOP            ;STOP MOTION
        JMP     LDRCHK          ;CHECK FOR CLEAR LEADER
        ;
        .PAGE
        .SBTTL  SPACE REVERSE FILE COMMAND - SRF
        ;
SRF:    JSR     REVERS          ;START MOTION, GET DATA
        BNE     SRF.B           ;ERROR
SRF.A:  JSR     GAP             ;WAIT FOR GAP
        LDX     #,-15588.       ;GAP TIME OF 250 MS.
```

```
        JSR     DATA            ;TRY TO READ DATA
        BEQ     SRF.A           ;IF DATA FOUND - NO GAP
        BMI     SRF.B           ;CLEAR LEADER - SKIP
        SETBTX  DVSTAT,20       ;ELSE GAP FOUND
SRF.B:  JSR     STOP            ;STOP MOTION
        JMP     LDRCHK          ;CHECK FOR CLEAR LEADER
        ;
        .PAGE
        .SBTTL  SPACE REVERSE BLOCK COMMAND - SRB
        ;
SRB:    JSR     REVERS          ;START MOTION, GET DATA
        BNE     SRB.A           ;ERROR - BRANCH
        JSR     GAP             ;GET PAST DATA
        JSR     WC.1            ;WAIT A WHILE
        JSR     STOP            ;STOP MOTION
SRB.A:  JMP     LDRCHK          ;CHECK CLEAR LEADER
        ;
        .PAGE
        .SBTTL  SPACE FORWARD FILE COMMAND - SFF
        ;
SFF:    LDA A   TMC,X           ;CHECK IF ON LEADER
        BPL     SFF.A           ;IF NOT - SKIP
        BTTSTX  RWSTAT,1        ;AT BOT ?
        BNE     SFF.A           ;IF SO - SKIP
        JMP     ERDONE          ;ELSE ERROR
SFF.A:  JSR     FORWRD          ;START MOTION, FIND PREAMBLE
        BNE     SFF.C           ;ERROR - BRANCH
SFF.B:  JSR     GAP             ;WAIT FOR GAP
        BRA     SFF.A           ;KEEP GOING
SFF.C:  LDA A   DVSTAT,X        ;GET STATUS
        CMP A   #,120           ;ERROR / GAP ?
        BNE     SFF.D           ;IF NOT - TRUE ERROR
        AND A   #,277           ;ELSE JUST GAP
        STA A   DVSTAT,X        ;NOT AN ERROR IN SFF
SFF.D:  JMP     LDRCHK          ;GO FINISH UP
        ;
        .PAGE
        .SBTTL  SPACE FORWARD BLOCK COMMAND - SFB
        ;
SFB:    LDA A   TMC,X           ;ON CLEAR LEADER ?
        BPL     SFB.A           ;IF NOT - SKIP
        BTTSTX  RWSTAT,1        ;AT BOT ?
        BNE     SFB.A           ;IF SO - SKIP
        JMP     ERDONE          ;ELSE ERROR
SFB.A:  JSR     FORWRD          ;START MOTION
        BNE     SFB.B           ;ERROR - BRANCH
        JSR     GAP             ;CHECK FOR GAP
        JSR     WC.2            ;WAIT A WHILE
        JSR     STOP            ;STOP PAST BLOCK
SFB.B:  JMP     LDRCHK          ;CHECK CLEAR LEADER
        ;
        .PAGE
        .SBTTL  REWIND COMMAND - REWIND
        ;
REWIND: STRBLX  TRWND,10        ;STROBE REWIND
        STORX   RWSTAT,10       ;SET REWINDING AND PROGRAMMED
        JMP     TSTCMD          ;GO CHECK FOR ANOTHER COMMAND
        ;
        .PAGE
        .SBTTL  GENERAL WAIT ROUTINE  WC
        ;
        ;       RETURNS AFTER SPECIFIED TIME WITH 'C' CLEAR
        ;       RETURNS ON CLEAR LEADER WITH 'C' SET
        ;       TIME = 20+21*X+10*INT(1+X/256) CLOCK CYCLES
        ;
WC.1:   LDX     #,-2375.        ;25 MS. ENTRY POINT     (3)
        BRA     WC.A            ;                       (4)
WC.2:   LDX     #,-8554.        ;90 MS. ENTRY POINT     (3)
        BRA     WC.A            ;                       (4)
WC.3:   LDX     #,-9505.        ;100 MS. ENTRY POINT    (3)
        BRA     WC.A            ;                       (4)
WC.4:   LDX     #,-59412.       ;625 MS. ENTRY POINT    (3)
        BRA     WC.A            ;                       (4)
        ;
WC.A:   STX     T.WAIT          ;SAVE WAIT COUNT        (5)
        LDX     DEV.X           ;GET DEVICE POINTER     (3)
```

```
        ;
WC.B:   LDA A   #,177           ;PRESET VALUE           (2)
        SUB A   TMC,X           ;CLEAR LEADER ?         (5)
        BCS     WC.C            ;IF SO - LEAVE          (4)
        INC     T.WAIT+1        ;UPDATE COUNT           (6)
        BNE     WC.B            ;                       (4)
        INC     T.WAIT          ;                       (6)
        BNE     WC.B            ;                       (4)
WC.C:   RTS                     ;FINISHED               (5)
        ;
        .PAGE
        .SBTTL  GENERAL UTILLITIES
        ;
STOP:   LDX     DEV.X           ;GET POINTER TO DEVICE
        SETBTX  TMC,3           ;STOP MOTION IN TRANSPORT
        LDX     #,12500.        ;50 MS. WAIT FOR STOP
STOP.A: DEX                     ;                       (4)
        BNE     STOP.A          ;LOOP UNTIL TIME UP     (4)
        LDX     DEV.X           ;GET DEVICE POINTER
        RTS                     ;FINISHED
        ;
        ;
GAP:    LDA B   #,8.            ;1 BYTE TIME
GAP.A:  LDA A   PD3AC           ;WAIT FOR WRITE CLOCK
        BPL     GAP.A
        LDA A   RWCSR1          ;CLEAR CLOCK FLAG
        BITTST  RWCSR0,160      ;A GAP ?
        BNE     GAP             ;IF NOT - SCAN AGAIN
        DEC B                   ;DECREMENT WAIT COUNTER
        BNE     GAP.A           ;WAIT A FULL BYTE TIME
        RTS                     ;FINISHED
        ;
        .PAGE
        .SBTTL  READ CRC GENERATION
        ;
        ;       COMPLETION TIME = 63 + (14/20) CLOCK CYCLES
        ;
RDCRC:  LDA B   #,4             ;SET UP WAIT FOR ONLY 4 BIT TIMES       (2)
RDC.LC: LDA A   RWCSR1          ;CLEAR WRITE CLOCK FLAG                 (3)
RDC.LP: LDA A   PD1AC           ;CHECK READ CLOCK                       (3)
        BMI     RDC.GO          ;IF CLOCKED - GET DATA                  (4)
        LDA A   PD3AC           ;CHECK WRITE CLOCK FOR TIME             (3)
        BPL     RDC.LP          ;IF NOT SET - LOOP                      (4)
        DEC B                   ;TIMED OUT ?                            (2)
        BNE     RDC.LC          ;IF NOT - LOOP                          (4)
RDC.GO: LDA A   CRC+1           ;LOAD CURRENT CRC                       (3)
        LDA B   CRC             ;                                       (3)
        LSR B                   ;INITIAL SHIFT                          (2)
        ROR A                   ;WAS BIT 0 SET ?                        (2)
        BCC     RDCR.A          ;IF NOT - SKIP                          (4)
        EOR B   #,240           ;ELSE XOR BITS 16, 14, AND 1            (2)
        EOR A   #,1             ;                                       (2)
RDCR.A: ROL     RWCSR0          ;C= NEW BIT / CLEAR CLOCK FLAG          (6)
        BCC     RDCR.B          ;IF NOT SET - SKIP                      (4)
        EOR B   #,240           ;ELSE XOR BITS 16, 14, AND 1            (2)
        EOR A   #,1             ;                                       (2)
RDCR.B: ROR     RWDATA          ;SHIFT CARRY INTO DATA WORD             (6)
        STA A   CRC+1           ;SAVE NEW CRC RESULT                    (4)
        STA B   CRC             ;                                       (4)
        RTS                     ;FINISHED                               (5)
        ;
        .PAGE
        .SBTTL  WRITE CRC GENERATION
        ;
WTCRC:  LDA A   PD3AC           ;WAIT FOR WRITE CLOCK
        BPL     WTCRC
        LDA A   RWCSR1          ;CLEARS CLOCK FLAG
        LDA A   CRC+1           ;GET CURRENT CRC
        LDA B   CRC
        LSR B                   ;SHIFT CRC
        ROR A
        BCC     WTCR.A          ;IF CARRY CLEAR - SKIP
        EOR B   #,240           ;ELSE XOR BITS 16, 14, AND 1
        EOR A   #,1
WTCR.A: ROR     RWDATA          ;GET NEXT BIT
        BCC     WTCR.B          ;IF CARRY CLEAR - SKIP
```

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        EOR B   #,240           ;ELSE XOR BITS 16, 14, AND 1
        EOR A   #,1
WTCR.B: ROL     RWCSR0          ;SET NEXT BIT TO WRITE
        STA A   CRC+1           ;SAVE NEW CRC
        STA B   CRC
        RTS                     ;FINISHED
        ;
        .PAGE
        .SBTTL  FORWARD ROUTINE
        ;
FORWRD: LDA A   TMC,X           ;CHECK LEADER
        BPL     FORW.D          ;ON OXIDE - BRANCH
        BTTSTX  RWSTAT,1        ;AT BOT ?
        BEQ     FORW.F          ;IF NOT  ERROR
FORW.A: CLRBTX  TMC,1           ;START FORWARD MOTION
        BMI     FORW.A          ;WAIT UNTIL PAST CLEAR LEADER
FORW.B: LDX     #,0             ;SEARCH UNTIL DATA FOUND
        JSR     RDPREA          ;TRY TO FIND PREAMBLE
        BEQ     FORW.G          ;IF FOUND - BRANCH
        BGT     FORW.B          ;IF TIMED OUT - SEARCH SOME MORE
FORW.C: CLRBTX  RWSTAT,1        ;ELSE CLEAR LEADER - EOT
        BRA     FORW.E
FORW.D: CLRBTX  TMC,1           ;START FORWARD MOTION
        LDX     #,6250.         ;WAIT 25. MS TO REACH SPEED
        DEX
        BNE     .-1             ;LOOP UNTIL TIME UP
        LDX     #,-32443.       ;520 MS. SEARCH
        JSR     RDPREA          ;TRY TO FIND DATA
        BEQ     FORW.G          ;IF FOUND DATA - BRANCH
        BMI     FORW.C          ;IF CLEAR LEADER - BRANCH
        SETBTX  DVSTAT,20       ;GAP FOUND
FORW.E: JSR     STOP            ;STOP MOTION ON ERRORS
FORW.F: SETBTX  DVSTAT,100      ;ERROR
FORW.G: BTTSTX  DVSTAT,100      ;ANY ERRORS ?
        RTS                     ;FINISHED
        ;
        .PAGE
        .SBTTL  REVERSE ROUTINE
        ;
REVERS: BTTSTX  RWSTAT,1        ;AT BOT ?
        BNE     REVE.D          ;IF SO - ERROR
        CLRBTX  TMC,2           ;START MOTION
        LDX     #,6250.         ;WAIT 25 MS. TO REACH SPEED
        DEX
        BNE     .-1
        STX     T.WAIT          ;WAIT COUNTER SETUP
        LDX     DEV.X           ;GET POINTER
REVE.A: LDA A   TMC,X           ;CHECK STATUS
        BPL     REVE.B          ;OFF CLEAR LEADER - BRANCH
        INC     T.WAIT+1
        BNE     REVE.A
        INC     T.WAIT
        BNE     REVE.A
        BRA     REVE.C          ;ERROR IF GETS THIS FAR
REVE.B: LDX     #,0             ;SET TO SEARCH FOR DATA
        JSR     DATA            ;TRY TO FIND DATA
        BEQ     REVE.E          ;FIND DATA - BRANCH
        BGT     REVE.B          ;TIME-OUT  - TRY AGAIN
REVE.C: SETBTX  RWSTAT,1        ;CLEAR LEADER - BOT
        JSR     STOP            ;ON ERRORS STOP MOTION
REVE.D: SETBTX  DVSTAT,100      ;INDICATE ERROR
REVE.E: BTTSTX  DVSTAT,100      ;ANY ERRORS ?
        RTS                     ;FINISHED
        ;
        .PAGE
        .SBTTL  FIND PREAMBLE ROUTINE
        ;
        ;       PREAMBLE IS FOUND IF 8 CONSECUTIVE 0'S ARE DETECTED
        ;
RDPR.A: LDX     T.WAIT          ;LOAD TO FINISH SEARCH
RDPREA: JSR     DATA            ;SCAN FOR DATA
        BNE     RDPR.C          ;ON ERROR - FINISHED
        CLR     RWDATA          ;PRESET READ DATA
        LDA A   #,8.            ;READ 8 BITS OF DATA
        STA A   LPCNTR
RDPR.B: JSR     RDCRC           ;GET DATA BIT
```

```
        LDA A   RWCSR0          ;CHECK FOR CONTINUOUS DATA
        AND A   #,160
        CMP A   #,60
        BNE     RDPR.A          ;IF NOT - FINISH SEARCH
        LDA A   RWDATA          ;CHECK IF DATA IS 0
        BNE     RDPR.A          ;IF NOT - FINISH SEARCH
        DEC     LPCNTR          ;8 BITS YET ?
        BNE     RDPR.B          ;LOOP UNTIL ALL 8
RDPR.C: RTS                     ;FINISHED
        ;
        .PAGE
        .SBTTL  FIND DATA ROUTINE
        ;
        ;       UPON RETURN  N=0, Z=1 IF DATA
        ;                    N=1, Z=0 IF CLEAR LEADER
        ;                    N=0, Z=0 IF TIME-OUT
        ;
        ;               TIME-OUT = 16+32*X+10*INT(1+X/256)  CLOCK CYCLES
        ;                                + 4 BIT TIMES
        ;
DATA:   STX     T.WAIT          ;TIMEOUT COUNTER                    (5)
        LDX     DEV.X           ;GET DEVICE POINTER                 (4)
DATA.A: LDA B   #,4             ;4 BIT TIMES CHECK                  (2)
DATA.B: LDA A   TMC,X           ;CLEAR LEADER ?                     (5)
        BMI     DATA.E          ;IF SO - ERROR FORM (N=1, Z=0)      (4)
        LDA A   RWCSR0          ;GET STATUS                         (3)
        AND A   #,160           ;DATA FOUND IF                      (2)
        CMP A   #,60            ;DATA(0), GAP(1), AND DROP OUT(1)   (2)
        BNE     DATA.D          ;NOT DATA - SKIP                    (4)
        LDA A   RWCSR1          ;CLEAR CLOCK FLAG                   (3)
DATA.C: LDA A   PD3AC           ;CHECK WRITE CLOCK                  (3)
        BPL     DATA.C          ;LOOP UNTIL TIME                    (4)
        DEC B                   ;BIT TIMES ELAPSED ?                (2)
        BNE     DATA.B          ;IF NOT - LOOP                      (4)
        RTS                     ;FINISHED (N=0, Z=1)                (5)
DATA.D: INC     T.WAIT+1        ;TIMEOUT COUNTER                    (6)
        BNE     DATA.A          ;                                   (4)
        INC     T.WAIT          ;                                   (6)
        BNE     DATA.A          ;                                   (4)
        LDA B   #,1             ;ERROR FORM (N=0, Z=0)              (2)
DATA.E: RTS                     ;FINISHED                           (5)
        ;
        .END
```

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```
 1                                .TITLE  DUAL CASSETTE DRIVE SOFTWARE
 2                                ;
 3                                ;*********************************************************
 4                                ;*                                                       *
 5                                ;*                                                       *
 6                                ;*        THIS SOFTWARE IS FOR A DUAL CASSETTE           *
 7                                ;*      DRIVE SYSTEM UTILIZING A MOTOROLA M68B00         *
 8                                ;*      MICROPROCESSOR.                                  *
 9                                ;*                                                       *
10                                ;*                                                       *
11                                ;*              WRITTEN BY    ALAN R. BALDWIN            *
12                                ;*                                JULY  1979             *
13                                ;*              COMPLETED       JANUARY  1980            *
14                                ;*                                                       *
15                                ;*********************************************************
16                                ;
17                                ;
```

SPECIAL MACRO'S

```
                                        .SBTTL  SPECIAL MACRO'S
                                        ;
                                        .MACRO  SETBIT  I,J
                                        LDA A   I
                                        ORA A   #,J
                                        STA A   I
                                        .ENDM   SETBIT
                                        ;
                                        ;
                                        .MACRO  CLRBIT  I,J
                                        LDA A   I
                                        AND A   #,377-J
                                        STA A   I
                                        .ENDM   CLRBIT
                                        ;
                                        ;
                                        .MACRO  BITTST  I,J
                                        LDA A   I
                                        BIT A   #,J
                                        .ENDM   BITTST
                                        ;
                                        ;
                                        .MACRO  STRBL   I,J
                                        LDA A   I
                                        AND A   #,377-J
                                        STA A   I
                                        ORA A   #,J
                                        STA A   I
                                        .ENDM   STRBL
                                        ;
                                        ;
                                        .MACRO  STRBH   I,J
                                        LDA A   I
                                        ORA A   #,J
                                        STA A   I
```

```
    37                                  STA A   I
    38                                  .ENDM   STRBH
    39                                  ;
    40                                  ;
```

SPECIAL MACRO'S

```
 1                                      .MACRO SETBTX   I,J
 2                                      LDA A   I,X
 3                                      ORA A   #,J
 4                                      STA A   I,X
 5                                      .ENDM   SETBTX
 6                                      ;
 7                                      ;
 8                                      .MACRO  CLRBTX  I,J
 9                                      LDA A   I,X
10                                      AND A   #,377-J
11                                      STA A   I,X
12                                      .ENDM   CLRBTX
13                                      ;
14                                      ;
15                                      .MACRO  BTTSTX  I,J
16                                      LDA A   I,X
17                                      BIT A   #,J
18                                      .ENDM   BTTSTX
19                                      ;
20                                      ;
21                                      .MACRO  STRBLX  I,J
22                                      LDA A   I,X
23                                      AND A   #,377-J
24                                      STA A   I,X
25                                      ORA A   #,J
26                                      STA A   I,X
27                                      .ENDM   STRBLX
28                                      ;
29                                      ;
30                                      .MACRO  STRBHX  I,J
31                                      LDA A   I,X
32                                      ORA A   #,J
33                                      STA A   I,X
34                                      AND A   #,377-J
35                                      STA A   I,X
```

```
    37                                  ;
    38                                  ;
    39                                  .MACRO  STORX   I,J
    40                                  LDA A   #,J
    41                                  STA A   I,X
    42                                  .ENDM   STORX
    43                                  ;
```

VARIABLE DEFINITIONS

```
                                        .SBTTL  VARIABLE DEFINITIONS
                                        ;
         000077                         STACK   =       77              ;SET STACK POSITION
                                        ;
 000000                                 ORG     100             ;VARIABLES AREA
                                        ;
 000100     000                 VA.1:   .BYTE   0       ;RDYFLG(DEV.1)
 000101     000                 VB.1:   .BYTE   0       ;RWSTAT(DEV.1)
 000102     000                 VC.1:   .BYTE   0       ;DVSTAT(DEV.1)
 000103     000                 VD.1:   .BYTE   0
 000104     000                 VA.0:   .BYTE   0       ;RDYFLG(DEV.0)
 000105     000                 VB.0:   .BYTE   0       ;RWSTAT(DEV.0)
 000106     000                 VC.0:   .BYTE   0       ;DVSTAT(DEV.0)
 000107     000                 VD.0:   .BYTE   0
 000110     000                 EXSTAT: .BYTE   0       ;SAVED STATUS FROM PDP-11
 000111     000                 EXCMD:  .BYTE   0       ;SAVED COMMAND FROM PDP-11
 000112     000     000         DEV.X:  .BYTE   0,0     ;SELECTED DEVICE INDEX
 000114     000     000         T.WAIT: .BYTE   0,0     ;WAIT LOOP COUNTER
 000116     000     000         CRC:    .BYTE   0,0     ;CRC VALUE
 000120     000     000         SVCRC:  .BYTE   0,0     ;SAVED CRC VALUE
 000122     000                 RWDATA: .BYTE   0       ;READ / WRITE  DATA
 000123     000                 LPCNTR: .BYTE   0       ;LOOP COUNTER
                                        ;
```

INTERRUPT LINKAGE

```
                                        .SBTTL  INTERRUPT LINKAGE
                                        ;
000124                                  ORG     177770  ;VECTOR AREA
177770                          IRQ:    FDB     PWRUP   ;SET ALL FOR POWER UP RESTART
  177770     370     000
177772                          SWI:    FDB     PWRUP
  177772     370     000
177774                          NMI:    FDB     PWRUP
  177774     370     000
177776                          RES:    FDB     PWRUP
  177776     370     000
                                        ;
                                        ;
000000                                  ORG     174000          ;ORIGIN THIS SEGMENT
                                        ;
174000                          PWRUP:  LDS     #,STACK         ;SET UP STACK
  174000     216     000     077
174003                                  CLR     ODAT            ;INITIALIZE REGISTER
  174003     177     000     234
174006                                  LDA A   #,100           ;POWER UP ERROR
  174006     206     100
174010                                  STA A   VC.0
  174010     227     106
174012                                  STA A   VC.1
  174012     227     102
174014                                  LDA A   #,210           ;INIT TO READY AND PROGRAMMED
  174014     206     210
174016                                  STA A   VB.0            ;PROGRAMMED, AND READY
  174016     227     105
174020                                  STA A   VB.1
  174020     227     101
174022                                  LDA A   #,2             ;SET UP READY FLAGS
  174022     206     002
174024                                  STA A   VA.0
  174024     227     104
```

```
   174026     110
23 174027                                STA A   VA.1
   174027     227     100
24                                       ;
```

INITIALIZATION OF COMMAND REGISTER 68B21 PIA D4

```
                                .SBTTL  INITIALIZATION OF COMMAND REGISTER 68B21 PIA D4
                                ;
                                ;       THE COMMAND REGISTER IS A TWO BYTE
                                ;       STATUS AND CONTROL REGISTER WHICH INTERFACES WITH
 THE
                                ;       PDP-11 UNIBUS.
                                ;
 000200                                 TSTAT   =       200
                                ;       TSTAT IS THE ERROR/READY STATUS REGISTER
                                ;
                                ;       7-      GO BIT (H-COMMAND ISSUED)       (IN)
                                ;       6-      ERROR                           (OUT)
                                ;       5-      BLOCK CHECK ERROR               (OUT)
                                ;       4-      FILE GAP                        (OUT)
                                ;       3-      TIMING ERROR                    (OUT)
                                ;       2-      UNIT 1 READY(H)                 (OUT)
                                ;       1-      UNIT 0 READY(H)                 (OUT)
                                ;       0-      UNIT SELECTED                   (IN)
                                ;
 000201                                 TCMD    =       201
                                ;       TCMD IS THE COMMAND/TRANSFER REGISTER
                                ;
                                ;       7-      TR SERVICED (H)                 (IN)
                                ;       6-      CLEAR TR (L)                    (OUT)
                                ;       5-      ---
                                ;       4-      ---
                                ;       3-      ILBS FLAG                       (IN)
                                ;       2-      FUNCTION BIT 2                  (IN)
                                ;       1-      FUNCTION BIT 1                  (IN)
                                ;       0-      FUNCTION BIT 0                  (IN)
                                ;
 000202                                 PD4BC   =       202
 000203                                 PD4AC   =       203
                                ;
                                ;       PD4(A/B)C ARE THE PIA CONTROL REGISTERS
                                ;       PD4BC IS PAIRED WITH TSTAT
```

```
    36                                  ;       PD4AC IS PAIRED WITH TCMD
    37                                  ;
    38 174031                           LDX     #,0,0           ;ACCESS DIRECTION REGISTERS
       174031   316     000     000
    39 174034                           STX     PD4BC           ;LOAD BOTH B & A
       174034   337     202
    40 174036                           LDX     #,176,100       ;SET INPUTS & OUTPUTS
       174036   316     176     100
    41 174041                           STX     TSTAT           ;IN BOTH TSTAT & TCMD
       174041   337     200
    42 174043                           LDX     #,4,4           ;ACCESS DATA REGISTERS
       174043   316     004     004
    43 174046                           STX     PD4BC
       174046   337     202
    44 174050                           LDX     #,0,0           ;SET BOTH UNITS NOT READY
       174050   316     000     000
    45 174053                           STX     TSTAT
       174053   337     200
    46 174055                           CLR     CLRGOH          ;ENABLE READY
       174055   177     000     214
    47                                  ;
```

INITIALIZE TRANSPORT 0 68B21 PIA

```
                                .SBTTL  INITIALIZE TRANSPORT 0 68B21 PIA
                                ;
                                ;         THE 68B21 PIA D1 CONTAINS TWO 8 BIT
                                ;       CONTROL REGISTERS:
                                ;
000210                                  TMC0    =       210
                                ;       1. TRANSPORT 0 MOTION CONTROL
                                ;
                                ;       7-      CLEAR LEADER (H)                (IN)
                                ;       6-      WRITE ENABLE (H)                (IN)
                                ;       5-      CASSETTE IN PLACE (H)           (IN)
                                ;       4-      REWIND DONE (H)                 (IN)
                                ;       3-      DISABLE REWIND (L)              (OUT)
                                ;       2-      ALLOW WRITE (L)                 (OUT)
                                ;       1-      REVERSE (L)                     (OUT)
                                ;       0-      FORWORD (L)                     (OUT)
                                ;
000211                                  RWCSR0  =       211
                                ;       2. TRANSPORT R/W STATUS REGISTER 0
                                ;
                                ;       7-      READ DATA                       (IN)
                                ;       6-      DATA                            (IN)
                                ;       5-      DROP OUT                        (IN)
                                ;       4-      GAP                             (IN)
                                ;       3-      READ CLOCK                      (IN)
                                ;       2-      WRITE CLOCK                     (IN)
                                ;       1-      ---
                                ;       0-      WRITE DATA                      (OUT)
                                ;
000212                                  PD1BC   =       212
000213                                  PD1AC   =       213
                                ;       PD1(A/B)C ARE PIA CONTROL REGISTERS
                                ;       PD1BC IS PAIRED WITH TMC0
                                ;       PD1AC IS PAIRED WITH RWCSR0
                                ;
```

```
       174060     316     004     004
    37 174063                              STX     PD1BC
       174063     337     212
    38 174065                              LDX     #,17,0          ;SET FOR NO MOTION/WRITING
       174065     316     017     000
    39 174070                              STX     TMC0
       174070     337     210
    40 174072                              LDX     #,0,0           ;ACCESS DIRECTION REGISTERS
       174072     316     000     000
    41 174075                              STX     PD1BC
       174075     337     212
    42 174077                              LDX     #,17,1          ;SET INPUTS AND OUTPUTS
       174077     316     017     001
    43 174102                              STX     TMC0
       174102     337     210
    44 174104                              LDX     #,76,6          ;CB1(REWIND DONE +) / CB2(OUT)
       174104     316     076     006
    45                                                             ;CA1(READ CLOCK +) / CA2(DATA -),
DATA
    46 174107                              STX     PD1BC
       174107     337     212
    47                                     ;
```

INITIALIZE TRANSPORT 1 68B21 PIA

```
                                .SBTTL  INITIALIZE TRANSPORT 1 68B21 PIA
                                ;
                                ;         THE 68B21 PIA D3 CONTAINS TWO 8 BIT
                                ;       CONTROL REGISTERS:
                                ;
000204                                  TMC1    =       204
                                ;       1. TRANSPORT 1 MOTION CONTROL
                                ;
                                ;       7-      CLEAR LEADER (H)                (IN)
                                ;       6-      WRITE ENABLE (H)                (IN)
                                ;       5-      CASSETTE IN PLACE (H)           (IN)
                                ;       4-      REWIND DONE (H)                 (IN)
                                ;       3-      DISABLE REWIND (L)              (OUT)
                                ;       2-      ALLOW WRITE (L)                 (OUT)
                                ;       1-      REVERSE (L)                     (OUT)
                                ;       0-      FORWORD (L)                     (OUT)
                                ;
000205                                  RWCSR1  =       205
                                ;       2. TRANSPORT R/W STATUS REGISTER 1
                                ;
                                ;       7-      ---
                                ;       6-      ---
                                ;       5-      CLEAR REWIND 1 (L)              (OUT)
                                ;       4-      CLEAR REWIND 0 (L)              (OUT)
                                ;       3-      ---
                                ;       2-      WRITE DATA ENABLE (H)           (OUT)
                                ;       1-      ---
                                ;       0-      READ UNIT SELECT                (OUT)
                                ;
000206                                  PD3BC   =       206
000207                                  PD3AC   =       207
                                ;       PD3(A/B)C ARE PIA CONTROL REGISTERS
                                ;       PD3BC IS PAIRED WITH TMC1
                                ;       PD3AC IS PAIRED WITH RWCSR1
                                ;
```

```
        174111     316     004     004
     37 174114                             STX     PD3BC
        174114     337     206
     38 174116                             LDX     #,17,60         ;SET FOR NO MOTION
        174116     316     017     060
     39 174121                             STX     TMC1
        174121     337     204
     40 174123                             LDX     #,0,0           ;ACCESS DIRECTION REGISTERS
        174123     316     000     000
     41 174126                             STX     PD3BC
        174126     337     206
     42 174130                             LDX     #,17,377        ;SET INPUTS AND OUTPUTS
        174130     316     017     377
     43 174133                             STX     TMC1
        174133     337     204
     44 174135                             LDX     #,76,26         ;CB1(REWIND DONE +) / CB2(OUT)
        174135     316     076     026
     45                                                             ;CA1(WRT CLK +) / CA2(DROP OUT +)
, DATA
     46 174140                             STX     PD3BC
        174140     337     206
     47                                    ;
```

REGISTER DEFINITIONS

```
                                .SBTTL  REGISTER DEFINITIONS
                                ;
                                ;       8-BIT INPUT DATA REGISTER FROM PDP-11 UNIBUS
000230                                  IDAT    =       230
                                ;
                                ;       8-BIT OUTPUT DATA REGISTER TO PDP-11 UNIBUS
000234                                  ODAT    =       234
                                ;
                                ;       INPUT SET TR FLAG REGISTER
000220                                  ISETTR  =       220
                                ;
                                ;       OUTPUT SET TR FLAG REGISTER
000224                                  OSETTR  =       224
                                ;
                                ;       CLEAR GOH / ENABLE READY FLAGS TO PDP-11
000214                                  CLRGOH  =       214
                                ;
                                ;
                                ;       INDEXED MODE DEVICE REGISTERS AND
                                ;       STATUS REGISTER DEFINITIONS
                                ;
000010                                  DEV.0   =       10
000004                                  DEV.1   =       4
                                ;
000200                                  TMC     =       200
000202                                  TRWND   =       202
                                ;
000074                                  RDYFLG  =       74      ;=2 (DEV.0), =4 (DEV.1)
                                ;
000075                                  RWSTAT  =       75
                                ;       7-      OPERATION DONE  (1)
                                ;       4-      REWIND DONE     (1)
                                ;       3-      PROGRAMMED      (1)
                                ;       0-      EOT (0) / BOT (1)
                                ;
```

```
                                ;       7-      ILBS / LAST BYTE CRC
                                ;       6-      ERROR                   (1)
                                ;       5-      BLOCK CHECK ERROR       (1)
                                ;       4-      FILE GAP                (1)
                                ;       3-      TIMING ERROR            (1)
                                ;       0-      ILBS / FIRST BYTE CRC
                                ;
                                ;
                                ;       THESE DEFINITIONS ARE USED BY ALL FUNCTION
                                ;       ROUTINES TO ALLOW UNIT INDEPENDENT HANDLERS
                                ;       TO BE WRITTEN.
                                ;
```

CHECK FOR COMMAND SCANNER

```
      1                                     .SBTTL  CHECK FOR COMMAND SCANNER
      2                                     ;
      3                                     ;       TRANSPORT STATUS SCANNER
      4                                     ;
      5 174142                              LDA A   #,1             ;INIT FOR TSTC.A
        174142     206     001
      6 174144                      TSTC.A: DEC A                   ;NEED TO CHECK TRANSPORT STATUS ?
        174144     112
      7 174145                              BNE     TSTCMD          ;IF NOT - SKIP
        174145     046     102
      8 174147                              LDX     #,DEV.0         ;SET UP FOR DEVICE 0
        174147     316     000     010
      9 174152                              STX     DEV.X           ;SAVE POINTER
        174152     337     112
     10 174154                              SETBTX  TMC,10          ;ENABLE REWINDING
        174154     246     200
        174156     212     010
        174160     247     200
     11 174162                              JSR     SCANTR
        174162     275     371     021
     12 174165                              LDX     #,DEV.1         ;SET UP FOR DEVICE 1
        174165     316     000     004
     13 174170                              STX     DEV.X           ;SAVE POINTER
        174170     337     112
     14 174172                              SETBTX  TMC,10          ;ENABLE REWINDING
        174172     246     200
        174174     212     010
        174176     247     200
     15 174200                              JSR     SCANTR
        174200     275     371     021
     16 174203                              CLR A                   ;RESET COUNTER
        174203     117
     17 174204                              BRA     TSTCMD
        174204     040     043
     18                                     ;
```

```
20                                      ;
21 174206                       LDRCHK: LDA A   TMC,X           ;CHECK FOR CLEAR LEADER
   174206     246     200
22 174210                               BPL     DONE            ;ON OXIDE - SKIP
   174210     052     006
23 174212                       ERDONE: SETBTX  DVSTAT,100      ;ERROR
   174212     246     076
   174214     212     100
   174216     247     076
24 174220                       DONE:   CLRBIT  TCMD,100        ;CLEAR TR
   174220     226     201
   174222     204     277
   174224     227     201
25 174226                               LDA A   TSTAT           ;GET STATUS WORD
   174226     226     200
26 174230                               AND A   #,6             ;SAVE ONLY READY'S
   174230     204     006
27 174232                               ORA A   DVSTAT,X        ;ADD IN NEW STATUS
   174232     252     076
28 174234                               STA A   TSTAT           ;GET FLAGS OUT
   174234     227     200
```

CHECK FOR COMMAND SCANNER

```
     29 174236                                ORA A   RDYFLG,X        ;SET READY FLAG
        174236     252     074
     30 174240                                STA A   TSTAT           ;SEND TO PDP-11
        174240     227     200
     31 174242                                SETBTX  TMC,10          ;ALLOW REWIND
        174242     246     200
        174244     212     010
        174246     247     200
     32 174250                                CLR A                   ;RESET COUNTER
        174250     117
     33                                       ;
     34                                       ;       COMMAND SCANNER
     35                                       ;
     36 174251                          TSTCMD: LDX     TSTAT           ;GET STATUS
        174251     336     200
     37 174253                                BPL     TSTC.A          ;NO COMMAND - BRANCH
        174253     052     267
     38 174255                                STX     EXSTAT          ;SAVE THE COMMAND
        174255     337     110
     39 174257                                LDA A   EXSTAT          ;GET THE SELECT
        174257     226     110
     40 174261                                AND A   #,1             ;FIND WHICH UNIT SELECTED
        174261     204     001
     41 174263                                BNE     TSTC.B          ;IF UNIT 1 - SKIP
        174263     046     013
     42 174265                                LDX     #,DEV.0         ;DEVICE 0 SELECTED
        174265     316     000     010
     43 174270                                CLRBIT  RWCSR1,1        ;SET READ SELECT UNIT 0
        174270     226     205
        174272     204     376
        174274     227     205
     44 174276                                BRA     TSTC.C
        174276     040     011
     45 174300                          TSTC.B: LDX     #,DEV.1         ;DEVICE 1 SELECTED
        174300     316     000     004
```

```
   174303     226     205
   174305     212     001
   174307     227     205
47 174311                      TSTC.C: STX     DEV.X           ;SAVE SELECTED DEVICE POINTER
   174311     337     112
48                                    ;
49                                    ;
50 174313                              LDA A   RDYFLG,X        ;GET READY FLAG
   174313     246     074
51 174315                              COM A                   ;MAKE MASK
   174315     103
52 174316                              AND A   TSTAT           ;MASK OUT SELECTED READY
   174316     224     200
53 174320                              STA A   TSTAT           ;SET READY FLAGS
   174320     227     200
54 174322                              STA A   CLRGOH          ;LET PDP-11 SEE READY'S
   174322     227     214
55 174324                              CLR     DVSTAT,X        ;NEW COMMAND
   174324     157     076
56 174326                              LDA B   TMC,X           ;GET DEVICE STATUS
   174326     346     200
```

CHECK FOR COMMAND SCANNER

```
    57 174330                              AND B   #,367           ;DISABLE REWIND
       174330     304     367
    58 174332                              STA B   TMC,X           ;SEND TO DEVICE
       174332     347     200
    59 174334                              BMI     TSTC.D          ;ON CLEAR LEADER - SKIP
       174334     053     006
    60 174336                              CLRBTX  RWSTAT,1        ;CLEAR BOT FLAG
       174336     246     075
       174340     204     376
       174342     247     075
    61 174344                      TSTC.D: AND B   #,60            ;CHECK IN PLACE AND REWIND DONE
       174344     304     060
    62 174346                              CMP B   #,60
       174346     301     060
    63 174350                              BNE     ERDONE          ;IF NOT - ERROR
       174350     046     240
    64                                     ;
```

COMMAND DISPATCH ROUTINE

```
      1                                     .SBTTL  COMMAND DISPATCH ROUTINE
      2                                     ;
      3 174352                              LDA B   EXCMD           ;GET COMMAND
        174352     326     111
      4 174354                              AND B   #,7             ;MASK OUT OTHER
        174354     304     007
      5 174356                              TBA                     ;SAVE IN A
        174356     027
      6 174357                              ABA
        174357     033
      7 174360                              ABA                     ;3*COMMAND
        174360     033
      8 174361                              CLR B
        174361     137
      9 174362                              ADD A   #,JMPTBL&377    ;LOW ORDER TABLE ADDRESS
        174362     213     371
     10 174364                              ADC B   #,JMPTBL&177400/400
        174364     311     370
     11 174366                              PSH A                   ;PLACE ADDRESS ON STACK
        174366     066
     12 174367                              PSH B
        174367     067
     13 174370                              RTS                     ;GO TO JUMP TABLE
        174370     071
     14                                     ;
     15 174371                   JMPTBL: JMP     WFG             ;WRITE FILE GAP
        174371     176     371     144
     16 174374                              JMP     WRITE           ;WRITE DATA
        174374     176     371     235
     17 174377                              JMP     READ            ;READ DATA
        174377     176     372     200
     18 174402                              JMP     SRF             ;SPACE REVERSE FILE
        174402     176     372     372
     19 174405                              JMP     SRB             ;SPACE REVERSE BLOCK
        174405     176     373     030
```

```
   174410     176     373     051
21 174413                             JMP     SFB             ;SPACE FORWARD BLOCK
   174413     176     373     115
22 174416                             JMP     REWIND          ;REWIND
   174416     176     373     153
23                                    ;
```

TRANSPORT SCANNING ROUTINE

```
                                        .SBTTL  TRANSPORT SCANNING ROUTINE
                                        ;
                                        ; 1.    CHECK FOR REWINDING
                                        ;       IF REWINDING THEN:
                                        ;               CLEAR OPERATION DONE FLAG
                                        ;               CLEAR REWIND DONE FLAG
                                        ;               CLEAR READY STATUS TO PDP-11
                                        ;               SET PROGRAMMED FLAG
                                        ;
174421                          SCANTR: LDA A   TMC,X           ;GET TRANSPORT MOTION
  174421     246     200
174423                                  AND A   #,20            ;PHYSICALLY REWINDING ?
  174423     204     020
174425                                  BNE     SCAN.A          ;IF NOT - SKIP
  174425     046     017
174427                                  ORA A   #,157           ;MASK OUT OPERATION DONE
  174427     212     157
174431                                  AND A   RWSTAT,X        ;MASK IN OTHER FLAGS
  174431     244     075
174433                                  ORA A   #,10            ;SET PROGRAMMED
  174433     212     010
174435                                  STA A   RWSTAT,X        ;SAVE NEW STATUS
  174435     247     075
174437                                  LDA A   RDYFLG,X        ;GET READY FLAG
  174437     246     074
174441                                  COM A                   ;MAKE A MASK
  174441     103
174442                                  AND A   TSTAT           ;MASK IN CURRENT STATUS
  174442     224     200
174444                                  STA A   TSTAT           ;SEND NEW STATUS TO PDP-11
  174444     227     200
                                        ;
                                        ; 2.    CHECK REWINDING STATUS
                                        ;       IF REWINDING THEN SCAN FOR COMPLETION
                                        ;       UPON COMPLETION:
```

```
     26                                     ;              SET OPERATION COMPLETE FLAG
     27                                     ;              SET BOT FLAG
     28                                     ;
     29 174446                        SCAN.A: LDA A   RWSTAT,X        ;GET STATUS
        174446     246     075
     30 174450                                BIT A   #,20            ;ARE WE REWINDING ?
        174450     205     020
     31 174452                                BNE     SCAN.C          ;IF NOT - SKIP
        174452     046     017
     32 174454                                LDA A   TMC,X           ;IF SO - THEN GET MOTION STATUS
        174454     246     200
     33 174456                                AND A   #,20            ;FINISHED YET ?
        174456     204     020
     34 174460                                BEQ     SCAN.C          ;IF NOT - SKIP
        174460     047     011
     35 174462                                ORA A   RWSTAT,X        ;ELSE MASK IN STATUS
        174462     252     075
     36 174464                                ORA A   #,201           ;SET BOT AND OPERATION COMPLETE F
LAGS
        174464     212     201
     37 174466                                STA A   RWSTAT,X        ;SAVE STATUS
        174466     247     075
```

TRANSPORT SCANNING ROUTINE

```
     38 174470                                JSR     STOP            ;STOP MOTION AND WAIT
        174470     275     373     245
     39                                       ;
     40                                       ; 3.    CHECK OPERATION DONE FLAG
     41                                       ;       IF SET THEN
     42                                       ;               CHECK CASSETTE IN PLACE: IF NOT
     43                                       ;                       CLEAR BOT FLAG
     44                                       ;
     45 174473                        SCAN.C: LDA A   RWSTAT,X        ;GET STATUS
        174473     246     075
     46 174475                                BPL     SCAN.F          ;IF NOT DONE - SKIP
        174475     052     044
     47 174477                                LDA B   TMC,X           ;GET TRANSPORT CONTROL
        174477     346     200
     48 174501                                BIT B   #,40            ;CASSETTE IN PLACE ?
        174501     305     040
     49 174503                                BNE     SCAN.D          ;IF SO - SKIP
        174503     046     004
     50 174505                                AND A   #,376           ;ELSE CLEAR BOT FLAG
        174505     204     376
     51 174507                                STA A   RWSTAT,X        ;AND SAVE NEW STATUS
        174507     247     075
     52                                       ;
     53                                       ; 4.    CHECK PROGRAMMED FLAG: IF SET THEN
     54                                       ;               CLEAR PROGRAMMED FLAG
     55                                       ;               SET ERROR BIT IF
     56                                       ;                       NOT CLEAR LEADER OR NOT IN PLACE
     57                                       ;               SET READY FLAG TO PDP-11
     58                                       ;
     59 174511                        SCAN.D: BIT A   #,10            ;PROGRAMMED ?
        174511     205     010
     60 174513                                BEQ     SCAN.F          ;IF NOT - SKIP
        174513     047     026
     61 174515                                AND A   #,367           ;CLEAR PROGRAMMED FLAG
        174515     204     367
```

```
   174517     247     075
63 174521                          LDA A   TSTAT           ;GET STATUS
   174521     226     200
64 174523                          AND A   #,6             ;SAVE ONLY READY'S
   174523     204     006
65 174525                          AND B   #,240           ;CHECK IN PLACE AND CLEAR LEADER
   174525     304     240
66 174527                          CMP B   #,240           ;BOTH SET ?
   174527     301     240
67 174531                          BEQ     SCAN.E          ;IF SO - SKIP
   174531     047     002
68 174533                          ORA A   #,100           ;ELSE SET ERROR BIT
   174533     212     100
69 174535                  SCAN.E: STA A   TSTAT           ;GET FLAGS OUT
   174535     227     200
70 174537                          ORA A   RDYFLG,X        ;SET READY FLAG
   174537     252     074
71 174541                          STA A   TSTAT           ;SEND STATUS TO PDP-11
   174541     227     200
72 174543                  SCAN.F: RTS                     ;FINISHED
   174543     071
```

TRANSPORT SCANNING ROUTINE

```
     73                                      ;
```

WRITE FILE GAP COMMAND - WFG

```
                                        .SBTTL  WRITE FILE GAP COMMAND - WFG
                                        ;
174544                          WFG:    LDA B   TMC,X           ;GET STATUS
  174544     346     200
174546                                  BIT B   #,100           ;WRITE ENABLED ?
  174546     305     100
174550                                  BEQ     WFG.E           ;IF NOT - ERROR
  174550     047     060
174552                                  TST B                   ;A CLEAR LEADER ?
  174552     135
174553                                  BPL     WFG.A           ;IF NOT - GO
  174553     052     006
174555                                  BTTSTX  RWSTAT,1        ;AT BOT ?
  174555     246     075
  174557     205     001
174561                                  BEQ     WFG.E           ;IF NOT - ERROR
  174561     047     047
174563                          WFG.A:  CLRBIT  RWCSR1,4        ;WRITE DATA DISABLED
  174563     226     205
  174565     204     373
  174567     227     205
174571                                  CLRBTX  TMC,5           ;FORWARD / ALLOW WRITE
  174571     246     200
  174573     204     372
  174575     247     200
174577                                  TST B                   ;STARTING IN CLEAR LEADER ?
  174577     135
174600                                  BPL     WFG.C           ;IF NOT - SKIP
  174600     052     007
                                        ;
                                        ;       WFG FROM BOT CLEAR LEADER
                                        ;
174602                          WFG.B:  LDA A   TMC,X           ;KEEP CHECKING CLEAR LEADER
  174602     246     200
174604                                  BMI     WFG.B           ;LOOP
```

```
 19 174606                              JSR     WC.4            ;EXTENDED GAP
    174606     275     373     213
 20                                     ;
 21                                     ;       WFG ON OXIDE
 22                                     ;
 23 174611                      WFG.C:  JSR     WC.4            ;NORMAL GAP
    174611     275     373     213
 24 174614                      WFG.D:  JSR     STOP            ;STOP TRANSPORT
    174614     275     373     245
 25 174617                              SETBTX  TMC,4           ;DISABLE WRITE
    174617     246     200
    174621     212     004
    174623     247     200
 26 174625                              BMI     WFG.E           ;IF CLEAR LEADER - ERROR
    174625     053     003
 27 174627                              JMP     DONE            ;FINISHED
    174627     176     370     220
 28 174632                      WFG.E:  JMP     ERDONE          ;FINISH UP COMMAND
    174632     176     370     212
 29                                     ;
```

WRITE COMMAND - WRITE

```
                                        .SBTTL  WRITE COMMAND - WRITE
                                        ;
174635                          WRITE:  LDA B   TMC,X           ;CHECK DEVICE
  174635     346     200
174637                                  BIT B   #,100           ;WRITE ENABLED ?
  174637     305     100
174641                                  BEQ     WRIT.C          ;IF NOT - ERROR
  174641     047     054
174643                                  TST B                   ;CLEAR LEADER ?
  174643     135
174644                                  BPL     WRIT.A          ;IF NOT - SKIP
  174644     052     006
174646                                  BTTSTX  RWSTAT,1        ;AT BOT ?
  174646     246     075
  174650     205     001
174652                                  BEQ     WRIT.C          ;IF NOT - AT EOT
  174652     047     043
174654                          WRIT.A: CLRBIT  RWCSR1,4        ;WRITE DATA DISABLED
  174654     226     205
  174656     204     373
  174660     227     205
174662                                  CLRBTX  TMC,5           ;FORWARD / ALLOW WRITE
  174662     246     200
  174664     204     372
  174666     247     200
174670                                  LDX     #,6250.         ;WAIT 25 MS. TO REACH SPEED
  174670     316     030     152
174673                                  DEX
  174673     011
174674                                  BNE     .-1             ;LOOP UNTIL TIME UP
  174674     046     375
174676                                  LDX     DEV.X           ;GET POINTER
  174676     336     112
174700                                  TST B                   ;CLEAR LEADER ?
  174700     135
```

```
   174701     052     017
18 174703                          WRIT.B: LDA A   TMC,X           ;READ STATUS
   174703     246     200
19 174705                                  BMI     WRIT.B          ;LOOP UNTIL OFF CLEAR LEADER
   174705     053     374
20 174707                                  JSR     WC.4            ;EXTENDED GAP AT BOT
   174707     275     373     213
21 174712                                  JSR     WC.4
   174712     275     373     213
22 174715                                  BCC     WRIT.E
   174715     044     010
23 174717                          WRIT.C: JMP     WRIT.Q          ;ERROR RETURN
   174717     176     372     167
24 174722                          WRIT.D: JSR     WC.1            ;NORMAL GAP
   174722     275     373     174
25 174725                                  BCS     WRIT.C          ;ERROR - CLEAR LEADER
   174725     045     370
26 174727                          WRIT.E: SETBIT  TCMD,100        ;ENABLE TR'S
   174727     226     201
   174731     212     100
   174733     227     201
```

WRITE COMMAND - WRITE

```
     27 174735                              STA A   ISETTR          ;SET TR TO PDP-11
        174735     227     220
     28 174737                              LDA A   RWCSR1          ;CLEAR CLOCK FLAG
        174737     226     205
     29 174741                         WRIT.F: LDA A   PD3AC         ;WAIT FOR CLOCK
        174741     226     207
     30 174743                              BPL     WRIT.F          ;LOOP
        174743     052     374
     31 174745                              SETBIT  RWCSR1,4        ;ENABLE WRITE DATA / CLEAR CLOCK
FLAG
        174745     226     205
        174747     212     004
        174751     227     205
     32 174753                              CLRBIT  RWCSR0,1        ;PREAMBLE 0'S
        174753     226     211
        174755     204     376
        174757     227     211
     33 174761                              LDX     #,0             ;CLEAR CRC
        174761     316     000     000
     34 174764                              STX     CRC
        174764     337     116
     35 174766                              LDX     DEV.X           ;GET DEVICE POINTER
        174766     336     112
     36 174770                              LDA B   #,31.           ;31. MORE ZERO'S
        174770     306     037
     37 174772                         WRIT.G: LDA A   PD3AC         ;CHECK CLOCK FLAG
        174772     226     207
     38 174774                              BPL     WRIT.G          ;LOOP
        174774     052     374
     39 174776                              LDA A   RWCSR1          ;CLEAR CLOCK FLAG
        174776     226     205
     40 175000                              DEC B                   ;0'S DONE ?
        175000     132
     41 175001                              BNE     WRIT.G          ;LOOP UNTIL FINISHED
        175001     046     367
     42 175003                         WRIT.H: LDA A   PD3AC         ;CHECK FLAG
```

```
        175003     226     207
     43 175005                              BPL     WRIT.H          ;LOOP
        175005     052     374
     44 175007                              LDA A   RWCSR1          ;CLEAR CLOCK FLAG
        175007     226     205
     45 175011                              SETBIT  RWCSR0,1        ;SET FRAME BIT
        175011     226     211
        175013     212     001
        175015     227     211
     46 175017                      WRIT.I: BITTST  TCMD,10         ;ILBS SET ?
        175017     226     201
        175021     205     010
     47 175023                              BNE     WRIT.J          ;IF SO - SKIP
        175023     046     012
     48 175025                              BIT A   #,200           ;TR SERVICED ?
        175025     205     200
     49 175027                              BEQ     WRIT.K          ;IF SO - SKIP
        175027     047     026
     50 175031                              SETBTX  DVSTAT,110      ;SET ERROR / TIMING
        175031     246     076
        175033     212     110
        175035     247     076
```

WRITE COMMAND - WRITE

```
     51 175037                          WRIT.J: SETBTX  DVSTAT,1        ;ILBS / FIRST BYTE CRC
        175037     246     076
        175041     212     001
        175043     247     076
     52 175045                                  LDA A   CRC+1           ;SAVE THE CRC
        175045     226     117
     53 175047                                  LDA B   CRC
        175047     326     116
     54 175051                                  STA A   SVCRC+1
        175051     227     121
     55 175053                                  STA B   SVCRC
        175053     327     120
     56 175055                                  BRA     WRIT.L
        175055     040     004
     57 175057                          WRIT.K: LDA A   IDAT            ;GET DATA FROM PDP-11
        175057     226     230
     58 175061                                  STA A   ISETTR          ;SET TR TO PDP-11
        175061     227     220
     59 175063                          WRIT.L: STA A   ODAT            ;LOAD OUTPUT REGISTER
        175063     227     234
     60 175065                                  STA A   RWDATA          ;SAVE DATA
        175065     227     122
     61 175067                                  LDA A   #,10            ;8. BITS PER BYTE
        175067     206     010
     62 175071                                  STA A   T.WAIT+1        ;SAVE COUNT
        175071     227     115
     63 175073                          WRIT.M: JSR     WTCRC           ;WRITE DATA / COMPUTE CRC
        175073     275     373     364
     64 175076                                  LDA A   TMC,X           ;CHECK FOR CLEAR LEADER
        175076     246     200
     65 175100                                  BMI     WRIT.P          ;IF SO - BRANCH
        175100     053     051
     66 175102                                  DEC     T.WAIT+1        ;DONE ?
        175102     172     000     115
     67 175105                                  BNE     WRIT.M          ;IF NOT - LOOP
```

```
 68 175107                              LDA B   DVSTAT,X        ;GET STATUS
    175107     346     076
 69 175111                              BMI     WRIT.N          ;CHECK FOR END OF ILBS
    175111     053     014
 70 175113                              BIT B   #,1             ;ILBS / FIRST BYTE CRC ?
    175113     305     001
 71 175115                              BEQ     WRIT.I          ;IF NOT - LOOP
    175115     047     300
 72 175117                              ORA B   #,200           ;ILBS SET
    175117     312     200
 73 175121                              STA B   DVSTAT,X
    175121     347     076
 74 175123                              LDA A   SVCRC           ;GET LAST BYTE OF CRC
    175123     226     120
 75 175125                              BRA     WRIT.L
    175125     040     334
 76 175127                      WRIT.N: LDA A   PD3AC           ;WAIT FOR CLOCK
    175127     226     207
 77 175131                              BPL     WRIT.N
    175131     052     374
 78 175133                              LDA A   RWCSR1          ;CLEAR CLOCK FLAG
```

WRITE COMMAND - WRITE

```
        175133     226     205
     79 175135                              CLR     RWCSR0          ;SET FINAL BIT = 0
        175135     177     000     211
     80 175140                              LDA B   #,2             ;SET UP FOR 2 ZERO BITS
        175140     306     002
     81 175142                         WRIT.O: LDA A   PD3AC          ;WAIT FOR CLOCK
        175142     226     207
     82 175144                              BPL     WRIT.O
        175144     052     374
     83 175146                              LDA A   RWCSR1          ;CLEAR CLOCK FLAG
        175146     226     205
     84 175150                              DEC B                   ;ZERO'S DONE ?
        175150     132
     85 175151                              BNE     WRIT.O          ;IF NOT - LOOP
        175151     046     367
     86 175153                         WRIT.P: CLRBIT  RWCSR1,4        ;TERMINATE DATA WRITING
        175153     226     205
        175155     204     373
        175157     227     205
     87 175161                              JSR     WC.3            ;WAIT A WHILE
        175161     275     373     206
     88 175164                              JSR     STOP            ;STOP MOTION
        175164     275     373     245
     89 175167                         WRIT.Q: SETBTX  TMC,4           ;DISABLE WRITE
        175167     246     200
        175171     212     004
        175173     247     200
     90 175175                              JMP     LDRCHK          ;CHECK CLEAR LEADER
        175175     176     370     206
     91                                     ;
```

READ COMMAND - READ

```
                                        .SBTTL  READ COMMAND - READ
                                        ;
175200                          READ:   JSR     FORWRD          ;START MOTION, FIND PREAMBLE
  175200    275     374     027
175203                                  BEQ     READ.A          ;IF NO ERROR - SKIP
  175203    047     003
175205                                  JMP     ERDONE          ;ELSE TERMINATE IN ERROR
  175205    176     370     212
175210                          READ.A: BITTST  RWCSR0,160      ;GAP ?
  175210    226     211
  175212    205     160
175214                                  BEQ     READ.F          ;ERROR - USE BLOCK CHECK
  175214    047     132
175216                                  TST A                   ;FRAME BIT FOUND ?
  175216    115
175217                                  BPL     READ.A          ;IF NOT - LOOP
  175217    052     367
175221                                  SETBIT  TCMD,100        ;ENABLE TR (TRANSFER REQUESTS)
  175221    226     201
  175223    212     100
  175225    227     201
175227                                  LDX     #,0             ;INIT CRC
  175227    316     000     000
175232                                  STX     CRC
  175232    337     116
175234                                  LDX     DEV.X           ;POINT TO DEVICE
  175234    336     112
175236                                  LDA A   RWCSR0          ;CLEAR CLOCK FLAG
  175236    226     211
175240                          READ.B: JSR     RDCRC           ;GET BIT 0
  175240    275     373     310
175243                                  JSR     RDCRC           ;GET BIT 1
  175243    275     373     310
175246                                  JSR     RDCRC           ;GET BIT 2
  175246    275     373     310
```

```
        175251     275     373     310
     19 175254                              JSR     RDCRC           ;GET BIT 4
        175254     275     373     310
     20 175257                              JSR     RDCRC           ;GET BIT 5
        175257     275     373     310
     21 175262                              LDA A   TMC,X           ;CHECK CLEAR LEADER
        175262     246     200
     22 175264                              BMI     READ.G          ;ERROR - BRANCH
        175264     053     070
     23 175266                              JSR     RDCRC           ;GET BIT 6
        175266     275     373     310
     24 175271                              BITTST  RWCSR0,100      ;CHECK DATA FLAG
        175271     226     211
        175273     205     100
     25                                                             ;=1 ON DROPOUT
     26 175275                              BEQ     READ.C          ;NO ERROR - SKIP
        175275     047     006
     27 175277                              SETBTX  DVSTAT,140      ;ERROR - DROP OUT (USE BLOCK CHEC
K)
        175277     246     076
        175301     212     140
        175303     247     076
```

READ COMMAND - READ

```
     28 175305                          READ.C: JSR     RDCRC           ;GET BIT 7
        175305     275     373     310
     29 175310                                  BITTST  RWCSR0,160      ;IN A GAP ?
        175310     226     211
        175312     205     160
     30 175314                                  BEQ     READ.F          ;ERROR - USE BLOCK CHECK
        175314     047     032
     31 175316                                  LDA B   TCMD            ;WAS TR SERVICED ?
        175316     326     201
     32 175320                                  BPL     READ.D          ;IF SO SKIP
        175320     052     006
     33 175322                                  SETBTX  DVSTAT,110      ;ERROR / TIMING ERROR
        175322     246     076
        175324     212     110
        175326     247     076
     34 175330                          READ.D: LDA A   RWDATA          ;GET READ DATA
        175330     226     122
     35 175332                                  STA A   ODAT            ;SEND TO INTERFACE
        175332     227     234
     36 175334                                  STA A   OSETTR          ;SET TR FLAG TO PDP-11
        175334     227     224
     37 175336                                  BIT B   #,10            ;TR SERVICED BY AN ILBS ?
        175336     305     010
     38 175340                                  BEQ     READ.B          ;IF NOT - GET NEXT BYTE
        175340     047     276
     39 175342                          READ.E: LDX     CRC             ;CHECK CRC
        175342     336     116
     40 175344                                  BEQ     READ.G          ;IF GOOD - SKIP
        175344     047     010
     41 175346                                  LDX     DEV.X           ;GET POINTER
        175346     336     112
     42 175350                          READ.F: SETBTX  DVSTAT,140      ;ERROR / BLOCK CHECK
        175350     246     076
        175352     212     140
        175354     247     076
```

```
   175356     275     373     266
44 175361                          JSR     WC.2            ;WAIT A WHILE
   175361     275     373     201
45 175364                          JSR     STOP            ;STOP MOTION
   175364     275     373     245
46 175367                          JMP     LDRCHK          ;CHECK FOR CLEAR LEADER
   175367     176     370     206
47                                 ;
```

SPACE REVERSE FILE COMMAND - SRF

```
                                        .SBTTL  SPACE REVERSE FILE COMMAND - SRF
                                        ;
175372                          SRF:    JSR     REVERS          ;START MOTION, GET DATA
  175372     275     374     145
175375                                  BNE     SRF.B           ;ERROR
  175375     046     023
175377                          SRF.A:  JSR     GAP             ;WAIT FOR GAP
  175377     275     373     266
175402                                  LDX     #,-15588.       ;GAP TIME OF 250 MS.
  175402     316     303     034
175405                                  JSR     DATA            ;TRY TO READ DATA
  175405     275     374     314
175410                                  BEQ     SRF.A           ;IF DATA FOUND - NO GAP
  175410     047     365
175412                                  BMI     SRF.B           ;CLEAR LEADER - SKIP
  175412     053     006
175414                                  SETBTX  DVSTAT,20       ;ELSE GAP FOUND
  175414     246     076
  175416     212     020
  175420     247     076
175422                          SRF.B:  JSR     STOP            ;STOP MOTION
  175422     275     373     245
175425                                  JMP     LDRCHK          ;CHECK FOR CLEAR LEADER
  175425     176     370     206
                                        ;
```

SPACE REVERSE BLOCK COMMAND - SRB

```
      1                                     .SBTTL  SPACE REVERSE BLOCK COMMAND - SRB
      2                                     ;
      3 175430                        SRB:  JSR     REVERS          ;START MOTION, GET DATA
        175430     275     374     145
      4 175433                              BNE     SRB.A           ;ERROR - BRANCH
        175433     046     011
      5 175435                              JSR     GAP             ;GET PAST DATA
        175435     275     373     266
      6 175440                              JSR     WC.1            ;WAIT A WHILE
        175440     275     373     174
      7 175443                              JSR     STOP            ;STOP MOTION
        175443     275     373     245
      8 175446                        SRB.A:JMP     LDRCHK          ;CHECK CLEAR LEADER
        175446     176     370     206
      9                                     ;
```

SPACE FORWARD FILE COMMAND - SFF

```
                                        .SBTTL  SPACE FORWARD FILE COMMAND - SFF
                                        ;
175451                          SFF:    LDA A   TMC,X           ;CHECK IF ON LEADER
  175451    246     200
175453                                  BPL     SFF.A           ;IF NOT - SKIP
  175453    052     011
175455                                  BTTSTX  RWSTAT,1        ;AT BOT ?
  175455    246     075
  175457    205     001
175461                                  BNE     SFF.A           ;IF SO - SKIP
  175461    046     003
175463                                  JMP     ERDONE          ;ELSE ERROR
  175463    176     370     212
175466                          SFF.A:  JSR     FORWRD          ;START MOTION, FIND PREAMBLE
  175466    275     374     027
175471                                  BNE     SFF.C           ;ERROR - BRANCH
  175471    046     005
175473                          SFF.B:  JSR     GAP             ;WAIT FOR GAP
  175473    275     373     266
175476                                  BRA     SFF.A           ;KEEP GOING
  175476    040     366
175500                          SFF.C:  LDA A   DVSTAT,X        ;GET STATUS
  175500    246     076
175502                                  CMP A   #,120           ;ERROR / GAP ?
  175502    201     120
175504                                  BNE     SFF.D           ;IF NOT - TRUE ERROR
  175504    046     004
175506                                  AND A   #,277           ;ELSE JUST GAP
  175506    204     277
175510                                  STA A   DVSTAT,X        ;NOT AN ERROR IN SFF
  175510    247     076
175512                          SFF.D:  JMP     LDRCHK          ;GO FINISH UP
  175512    176     370     206
                                        ;
```

SPACE FORWARD BLOCK COMMAND - SFB

```
                                        .SBTTL  SPACE FORWARD BLOCK COMMAND - SFB
                                        ;
175515                          SFB:    LDA A   TMC,X           ;ON CLEAR LEADER ?
  175515     246     200
175517                                  BPL     SFB.A           ;IF NOT - SKIP
  175517     052     011
175521                                  BTTSTX  RWSTAT,1        ;AT BOT ?
  175521     246     075
  175523     205     001
175525                                  BNE     SFB.A           ;IF SO - SKIP
  175525     046     003
175527                                  JMP     ERDONE          ;ELSE ERROR
  175527     176     370     212
175532                          SFB.A:  JSR     FORWRD          ;START MOTION
  175532     275     374     027
175535                                  BNE     SFB.B           ;ERROR - BRANCH
  175535     046     011
175537                                  JSR     GAP             ;CHECK FOR GAP
  175537     275     373     266
175542                                  JSR     WC.2            ;WAIT A WHILE
  175542     275     373     201
175545                                  JSR     STOP            ;STOP PAST BLOCK
  175545     275     373     245
175550                          SFB.B:  JMP     LDRCHK          ;CHECK CLEAR LEADER
  175550     176     370     206
                                        ;
```

REWIND COMMAND - REWIND

```
      1                                     .SBTTL  REWIND COMMAND - REWIND
      2                                     ;
      3 175553                        REWIND: STRBLX  TRWND,10        ;STROBE REWIND
        175553     246     202
        175555     204     367
        175557     247     202
        175561     212     010
        175563     247     202
      4 175565                              STORX   RWSTAT,10       ;SET REWINDING AND PROGRAMMED
        175565     206     010
        175567     247     075
      5 175571                              JMP     TSTCMD          ;GO CHECK FOR ANOTHER COMMAND
        175571     176     370     251
      6                                     ;
```

```
                                        .SBTTL  GENERAL WAIT ROUTINE  WC
                                        ;
                                        ;       RETURNS AFTER SPECIFIED TIME WITH 'C' CLEAR
                                        ;       RETURNS ON CLEAR LEADER WITH 'C' SET
                                        ;       TIME = 20+21*X+10*INT(1+X/256) CLOCK CYCLES
                                        ;
175574                          WC.1:   LDX     #,-2375.        ;25 MS. ENTRY POINT     (3)
  175574    316     366     271
175577                                  BRA     WC.A            ;                       (4)
  175577    040     017
175601                          WC.2:   LDX     #,-8554.        ;90 MS. ENTRY POINT     (3)
  175601    316     336     226
175604                                  BRA     WC.A            ;                       (4)
  175604    040     012
175606                          WC.3:   LDX     #,-9505.        ;100 MS. ENTRY POINT    (3)
  175606    316     332     337
175611                                  BRA     WC.A            ;                       (4)
  175611    040     005
175613                          WC.4:   LDX     #,-59412.       ;625 MS. ENTRY POINT    (3)
  175613    316     027     354
175616                                  BRA     WC.A            ;                       (4)
  175616    040     000
                                        ;
175620                          WC.A:   STX     T.WAIT          ;SAVE WAIT COUNT        (5)
  175620    337     114
175622                                  LDX     DEV.X           ;GET DEVICE POINTER     (3)
  175622    336     112
                                        ;
175624                          WC.B:   LDA A   #,177           ;PRESET VALUE           (2)
  175624    206     177
175626                                  SUB A   TMC,X           ;CLEAR LEADER ?         (5)
  175626    240     200
175630                                  BCS     WC.C            ;IF SO - LEAVE          (4)
  175630    045     012
175632                                  INC     T.WAIT+1        ;UPDATE COUNT           (6)
```

```
    23 175635                              BNE     WC.B            ;                       (4)
       175635     046     365
    24 175637                              INC     T.WAIT          ;                       (6)
       175637     174     000     114
    25 175642                              BNE     WC.B            ;                       (4)
       175642     046     360
    26 175644                      WC.C:   RTS                     ;FINISHED               (5)
       175644     071
    27                                     ;
```

GENERAL UTILLITIES

```
                                        .SBTTL  GENERAL UTILLITIES
                                        ;
175645                          STOP:   LDX     DEV.X           ;GET POINTER TO DEVICE
  175645    336     112
175647                                  SETBTX  TMC,3           ;STOP MOTION IN TRANSPORT
  175647    246     200
  175651    212     003
  175653    247     200
175655                                  LDX     #,12500.        ;50 MS. WAIT FOR STOP
  175655    316     060     324
175660                               STOP.A: DEX                ;                       (4)
  175660    011
175661                                  BNE     STOP.A          ;LOOP UNTIL TIME UP     (4)
  175661    046     375
175663                                  LDX     DEV.X           ;GET DEVICE POINTER
  175663    336     112
175665                                  RTS                     ;FINISHED
  175665    071
                                        ;
                                        ;
175666                          GAP:    LDA B   #,8.            ;1 BYTE TIME
  175666    306     010
175670                          GAP.A:  LDA A   PD3AC           ;WAIT FOR WRITE CLOCK
  175670    226     207
175672                                  BPL     GAP.A
  175672    052     374
175674                                  LDA A   RWCSR1          ;CLEAR CLOCK FLAG
  175674    226     205
175676                                  BITTST  RWCSR0,160      ;A GAP ?
  175676    226     211
  175700    205     160
175702                                  BNE     GAP             ;IF NOT - SCAN AGAIN
  175702    046     362
175704                                  DEC B                   ;DECREMENT WAIT COUNTER
  175704    132
```

```
        175705     046     361
     20 175707                              RTS                     ;FINISHED
        175707     071
     21                                     ;
```

READ CRC GENERATION

```
                                        .SBTTL  READ CRC GENERATION
                                        ;
                                        ;       COMPLETION TIME = 63 + (14/20) CLOCK CYCLES
                                        ;
175710                          RDCRC:  LDA B   #,4             ;SET UP WAIT FOR ONLY 4 BIT TIMES
 (2)
  175710    306     004
175712                          RDC.LC: LDA A   RWCSR1          ;CLEAR WRITE CLOCK FLAG
 (3)
  175712    226     205
175714                          RDC.LP: LDA A   PD1AC           ;CHECK READ CLOCK
 (3)
  175714    226     213
175716                                  BMI     RDC.GO          ;IF CLOCKED - GET DATA
 (4)
  175716    053     007
175720                                  LDA A   PD3AC           ;CHECK WRITE CLOCK FOR TIME
 (3)
  175720    226     207
175722                                  BPL     RDC.LP          ;IF NOT SET - LOOP
 (4)
  175722    052     370
175724                                  DEC B                   ;TIMED OUT ?
 (2)
  175724    132
175725                                  BNE     RDC.LC          ;IF NOT - LOOP
 (4)
  175725    046     363
175727                          RDC.GO: LDA A   CRC+1           ;LOAD CURRENT CRC
 (3)
  175727    226     117
175731                                  LDA B   CRC             ;
 (3)
  175731    326     116
175733                                  LSR B                   ;INITIAL SHIFT
 (2)
  175733    124
175734                                  ROR A                   ;WAS BIT 0 SET ?
 (2)
  175734    106
175735                                  BCC     RDCR.A          ;IF NOT - SKIP
 (4)
```

```
   175735     044     004

18 175737                          EOR B   #,240           ;ELSE XOR BITS 16, 14, AND 1
   (2)

   175737     310     240

19 175741                          EOR A   #,1             ;
   (2)

   175741     210     001

20 175743                    RDCR.A: ROL     RWCSR0          ;C= NEW BIT / CLEAR CLOCK FLAG
   (6)

   175743     171     000     211

21 175746                          BCC     RDCR.B          ;IF NOT SET - SKIP
   (4)

   175746     044     004

22 175750                          EOR B   #,240           ;ELSE XOR BITS 16, 14, AND 1
   (2)

   175750     310     240

23 175752                          EOR A   #,1             ;
   (2)

   175752     210     001

24 175754                    RDCR.B: ROR     RWDATA          ;SHIFT CARRY INTO DATA WORD
   (6)

   175754     166     000     122

25 175757                          STA A   CRC+1           ;SAVE NEW CRC RESULT
   (4)

   175757     227     117

26 175761                          STA B   CRC             ;
   (4)

   175761     327     116

27 175763                          RTS                     ;FINISHED
   (5)

   175763     071

28                                 ;
```

WRITE CRC GENERATION

```
                                        .SBTTL  WRITE CRC GENERATION
                                        ;
175764                          WTCRC:  LDA A   PD3AC           ;WAIT FOR WRITE CLOCK
  175764    226     207
175766                                  BPL     WTCRC
  175766    052     374
175770                                  LDA A   RWCSR1          ;CLEARS CLOCK FLAG
  175770    226     205
175772                                  LDA A   CRC+1           ;GET CURRENT CRC
  175772    226     117
175774                                  LDA B   CRC
  175774    326     116
175776                                  LSR B                   ;SHIFT CRC
  175776    124
175777                                  ROR A
  175777    106
176000                                  BCC     WTCR.A          ;IF CARRY CLEAR - SKIP
  176000    044     004
176002                                  EOR B   #,240           ;ELSE XOR BITS 16, 14, AND 1
  176002    310     240
176004                                  EOR A   #,1
  176004    210     001
176006                          WTCR.A: ROR     RWDATA          ;GET NEXT BIT
  176006    166     000     122
176011                                  BCC     WTCR.B          ;IF CARRY CLEAR - SKIP
  176011    044     004
176013                                  EOR B   #,240           ;ELSE XOR BITS 16, 14, AND 1
  176013    310     240
176015                                  EOR A   #,1
  176015    210     001
176017                          WTCR.B: ROL     RWCSR0          ;SET NEXT BIT TO WRITE
  176017    171     000     211
176022                                  STA A   CRC+1           ;SAVE NEW CRC
  176022    227     117
176024                                  STA B   CRC
```

FORWARD ROUTINE

```
                                        .SBTTL  FORWARD ROUTINE
                                        ;
176027                          FORWRD: LDA A   TMC,X           ;CHECK LEADER
  176027     246     200
176031                                  BPL     FORW.D          ;ON OXIDE - BRANCH
  176031     052     040
176033                                  BTTSTX  RWSTAT,1        ;AT BOT ?
  176033     246     075
  176035     205     001
176037                                  BEQ     FORW.F          ;IF NOT  ERROR
  176037     047     071
176041                          FORW.A: CLRBTX  TMC,1           ;START FORWARD MOTION
  176041     246     200
  176043     204     376
  176045     247     200
176047                                  BMI     FORW.A          ;WAIT UNTIL PAST CLEAR LEADER
  176047     053     370
176051                          FORW.B: LDX     #,0             ;SEARCH UNTIL DATA FOUND
  176051     316     000     000
176054                                  JSR     RDPREA          ;TRY TO FIND PREAMBLE
  176054     275     374     253
176057                                  BEQ     FORW.G          ;IF FOUND - BRANCH
  176057     047     057
176061                                  BGT     FORW.B          ;IF TIMED OUT - SEARCH SOME MORE
  176061     056     366
176063                          FORW.C: CLRBTX  RWSTAT,1        ;ELSE CLEAR LEADER - EOT
  176063     246     075
  176065     204     376
  176067     247     075
176071                                  BRA     FORW.E
  176071     040     034
176073                          FORW.D: CLRBTX  TMC,1           ;START FORWARD MOTION
  176073     246     200
  176075     204     376
  176077     247     200
```

FORWARD ROUTINE

```
        176134     212     100
        176136     247     076
     26 176140                          FORW.G: BTTSTX  DVSTAT,100      ;ANY ERRORS ?
        176140     246     076
        176142     205     100
     27 176144                                  RTS                     ;FINISHED
        176144     071
     28                                         ;
```

REVERSE ROUTINE

```
      1                                     .SBTTL  REVERSE ROUTINE
      2                                     ;
      3 176145                      REVERS: BTTSTX  RWSTAT,1        ;AT BOT ?
        176145     246     075
        176147     205     001
      4 176151                              BNE     REVE.D          ;IF SO - ERROR
        176151     046     063
      5 176153                              CLRBTX  TMC,2           ;START MOTION
        176153     246     200
        176155     204     375
        176157     247     200
      6 176161                              LDX     #,6250.         ;WAIT 25 MS. TO REACH SPEED
        176161     316     030     152
      7 176164                              DEX
        176164     011
      8 176165                              BNE     .-1
        176165     046     375
      9 176167                              STX     T.WAIT          ;WAIT COUNTER SETUP
        176167     337     114
     10 176171                              LDX     DEV.X           ;GET POINTER
        176171     336     112
     11 176173                      REVE.A: LDA A   TMC,X           ;CHECK STATUS
        176173     246     200
     12 176175                              BPL     REVE.B          ;OFF CLEAR LEADER - BRANCH
        176175     052     014
     13 176177                              INC     T.WAIT+1
        176177     174     000     115
     14 176202                              BNE     REVE.A
        176202     046     367
     15 176204                              INC     T.WAIT
        176204     174     000     114
     16 176207                              BNE     REVE.A
        176207     046     362
     17 176211                              BRA     REVE.C          ;ERROR IF GETS THIS FAR
        176211     040     012
```

REVERSE ROUTINE

```
        176250     071
     27                                      ;
```

FIND PREAMBLE ROUTINE

```
      1                                     .SBTTL  FIND PREAMBLE ROUTINE
      2                                     ;
      3                                     ;       PREAMBLE IS FOUND IF 8 CONSECUTIVE 0'S ARE DETECT
ED
      4                                     ;
      5 176251                        RDPR.A: LDX     T.WAIT          ;LOAD TO FINISH SEARCH
        176251     336     114
      6 176253                        RDPREA: JSR     DATA            ;SCAN FOR DATA
        176253     275     374     314
      7 176256                                BNE     RDPR.C          ;ON ERROR - FINISHED
        176256     046     033
      8 176260                                CLR     RWDATA          ;PRESET READ DATA
        176260     177     000     122
      9 176263                                LDA A   #,8.            ;READ 8 BITS OF DATA
        176263     206     010
     10 176265                                STA A   LPCNTR
        176265     227     123
     11 176267                        RDPR.B: JSR     RDCRC           ;GET DATA BIT
        176267     275     373     310
     12 176272                                LDA A   RWCSR0          ;CHECK FOR CONTINUOUS DATA
        176272     226     211
     13 176274                                AND A   #,160
        176274     204     160
     14 176276                                CMP A   #,60
        176276     201     060
     15 176300                                BNE     RDPR.A          ;IF NOT - FINISH SEARCH
        176300     046     347
     16 176302                                LDA A   RWDATA          ;CHECK IF DATA IS 0
        176302     226     122
     17 176304                                BNE     RDPR.A          ;IF NOT - FINISH SEARCH
        176304     046     343
     18 176306                                DEC     LPCNTR          ;8 BITS YET ?
        176306     172     000     123
     19 176311                                BNE     RDPR.B          ;LOOP UNTIL ALL 8
        176311     046     354
     20 176313                        RDPR.C: RTS                     ;FINISHED
```

FIND DATA ROUTINE

```
      1                                     .SBTTL  FIND DATA ROUTINE
      2                                     ;
      3                                     ;       UPON RETURN  N=0, Z=1 IF DATA
      4                                     ;                    N=1, Z=0 IF CLEAR LEADER
      5                                     ;                    N=0, Z=0 IF TIME-OUT
      6                                     ;
      7                                     ;               TIME-OUT = 16+32*X+10*INT(1+X/256)  CLOCK
 CYCLES
      8                                     ;                                + 4 BIT TIMES
      9                                     ;
     10 176314                      DATA:   STX     T.WAIT          ;TIMEOUT COUNTER
        (5)
        176314     337     114
     11 176316                              LDX     DEV.X           ;GET DEVICE POINTER
        (4)
        176316     336     112
     12 176320                      DATA.A: LDA B   #,4             ;4 BIT TIMES CHECK
        (2)
        176320     306     004
     13 176322                      DATA.B: LDA A   TMC,X           ;CLEAR LEADER ?
        (5)
        176322     246     200
     14 176324                              BMI     DATA.E          ;IF SO - ERROR FORM (N=1, Z=0)
        (4)
        176324     053     036
     15 176326                              LDA A   RWCSR0          ;GET STATUS
        (3)
        176326     226     211
     16 176330                              AND A   #,160           ;DATA FOUND IF
        (2)
        176330     204     160
     17 176332                              CMP A   #,60            ;DATA(0), GAP(1), AND DROP OUT(1)
        (2)
        176332     201     060
     18 176334                              BNE     DATA.D          ;NOT DATA - SKIP
        (4)
        176334     046     012
     19 176336                              LDA A   RWCSR1          ;CLEAR CLOCK FLAG
        (3)
        176336     226     205
```

Symbol table

```
CLRGOH= 000214          LPCNTR  000123          REVERS  176145          STACK = 000077          WC.3    1
75606

CRC     000116          NMI     177774          REVE.A  176173          STOP    175645          WC.4    1
75613

DATA    176314          ODAT  = 000234          REVE.B  176213          STOP.A  175660          WFG     1
74544

DATA.A  176320          OSETTR= 000224          REVE.C  176225          SVCRC   000120          WFG.A   1
74563

DATA.B  176322          PD1AC = 000213          REVE.D  176236          SWI     177772          WFG.B   1
74602

DATA.C  176340          PD1BC = 000212          REVE.E  176244          TCMD  = 000201          WFG.C   1
74611

DATA.D  176350          PD3AC = 000207          REWIND  175553          TMC   = 000200          WFG.D   1
74614

DATA.E  176364          PD3BC = 000206          RWCSR0= 000211          TMC0  = 000210          WFG.E   1
74632

DEV.X   000112          PD4AC = 000203          RWCSR1= 000205          TMC1  = 000204          WRITE   1
74635

DEV.0 = 000010          PD4BC = 000202          RWDATA  000122          TRWND = 000202          WRIT.A  1
74654

DEV.1 = 000004          PWRUP   174000          RWSTAT= 000075          TSTAT = 000200          WRIT.B  1
74703

DONE    174220          RDCRC   175710          SCANTR  174421          TSTCMD  174251          WRIT.C  1
74717

DVSTAT= 000076          RDCR.A  175743          SCAN.A  174446          TSTC.A  174144          WRIT.D  1
74722

ERDONE  174212          RDCR.B  175754          SCAN.C  174473          TSTC.B  174300          WRIT.E  1
74727

EXCMD   000111          RDC.GO  175727          SCAN.D  174511          TSTC.C  174311          WRIT.F  1
74741

EXSTAT  000110          RDC.LC  175712          SCAN.E  174535          TSTC.D  174344          WRIT.G  1
74772

FORWRD  176027          RDC.LP  175714          SCAN.F  174543          T.WAIT  000114          WRIT.H  1
75003

FORW.A  176041          RDPREA  176253          SFB     175515          VA.0    000104          WRIT.I  1
75017

FORW.B  176051          RDPR.A  176251          SFB.A   175532          VA.1    000100          WRIT.J  1
75037

FORW.C  176063          RDPR.B  176267          SFB.B   175550          VB.0    000105          WRIT.K  1
75057

FORW.D  176073          RDPR.C  176313          SFF     175451          VB.1    000101          WRIT.L  1
75063

FORW.E  176127          RDYFLG= 000074          SFF.A   175466          VC.0    000106          WRIT.M  1
75073

FORW.F  176132          READ    175200          SFF.B   175473          VC.1    000102          WRIT.N  1
75127
```

```
GAP     175666          READ.B  175240          SFF.D   175512          VD.1    000103          WRIT.P  1
75153

GAP.A   175670          READ.C  175305          SRB     175430          WC.A    175620          WRIT.Q  1
75167

IDAT  = 000230          READ.D  175330          SRB.A   175446          WC.B    175624          WTCRC   1
75764

IRQ     177770          READ.E  175342          SRF     175372          WC.C    175644          WTCR.A  1
76006

ISETTR= 000220          READ.F  175350          SRF.A   175377          WC.1    175574          WTCR.B  1
76017

JMPTBL  174371          READ.G  175356          SRF.B   175422          WC.2    175601          ...A  = 0
00100

LDRCHK  174206          RES     177776


. ABS.  177776    000   (RW,I,GBL,ABS,OVR)

        000000    001   (RW,I,LCL,REL,CON)

Errors detected:  0


*** Assembler statistics



Work  file  reads: 0

Work  file writes: 0

Size of work file: 15174 Words  ( 60 Pages)

Size of core pool: 18176 Words  ( 71 Pages)

Operating  system: RT-11


Elapsed time: 00:00:02.07

CAS,CAS=M6800,CAS
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OPERATING AND MAINTENANCE MANUAL FOR MAGNETIC TAPE CASSETTE TRANSPORT MODEL 100

TM # 21K026

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SECTION I. GENERAL INFORMATION

1-1. GENERAL.

1-2. The Magnetic Tape Cassette Transport, Model 100*, is a general purpose, single channel, constant speed, spindle-driven (reel-to-reel) Cassette Transport designed for minimum cost and long life.

1-3. The magnetic Tape Cassette Transport, Model 100, hereafter referred to as the Cassette Transport is a peripheral piece of equipment that may be interfaced with other electronic support systems. For an explanation of various options available refer to paragraph 1-4.

1-4. OPTIONS. There are three versions of the Cassette Transport. They are as follows:

Basic Unit — The basic unit is Model 100. It consists of the basic mechanical transport with a Tape Local Electronic (TLE) printed circuit board and a Read-After-Write (RAW) head. A Read/Write (R/W) head may be specified instead of the RAW head.

Option - 1 — This unit consists of the basic unit (Model 100) plus a Tape Transport Control (TTC) printed circuit board.

Option - 2 — This unit consists of the mechanical transport only. Either a Read-After-Write (RAW) or Read/Write (R/W) head may be specified.

*Approved by Underwriters' Laboratories

1-5. REFERENCE DATA.

1-6. Reference data is general data pertaining to the Cassette Transport. A Glossary of Abbreviations is provided in Appendix A.

1-7. TAPE CASSETTE. The magnetic tape cassette used in the Redactron Cassette Transport is a "Norelco-type" cassette modified as follows:

- o Diameter hub liner is 1.2 inches.
- o Tape per reel is 200 feet.
- o Tape is computer grade 0.7 mil tape (need not be certified perfect with Read-After-Write head).
- o Pressure pad is 0.140 by 0.313 inches.
- o ID of hubs held to $^{+0.003}_{-0.000}$ inches.
- o Rotating corner roller.
- o Replaceable "Write Enable" button.
- o Reflective leader at beginning and End-Of-Tape (EOT).
- o Reliability: 2,000 passes before a non-recoverable read occurs (80% confidence factor).

1-8. START/STOP CHARACTERISTICS. It requires 25 milliseconds for the tape to be up to proper speed for recording, which is approximately 0.25 ± 0.025 inches of tape.

NOTE

All direction reversal commands must be spaced by a "STOP" period of a minimum of 12 milliseconds.

1-9. TAPE SPEED. Depending on the reel diameter the constant spindle speeds cause tape velocity to vary as follows:

- o Average Tape Speed . . . . . 31 IPS
- o Maximum Tape Speed . . . . . 38 IPS
- o Minimum Tape Speed . . . . . 24 IPS

The nominal read/write speed varies from one end of the tape to the other. At a particular point the deviation from the nominal is not greater than ±15%.

1-10. REWIND TIME. Rewinding a full 200 foot reel requires 77 seconds.

1-11. RECORDING. Maximum recording rate is 25 microseconds between flux transitions.

1-12. AVERAGE DENSITY. The average density which occurs at the maximum recording rate is approximately 1290 flux changes per inch (fci). The maximum density is approximately 1666 fci at the beginning of tape and 1050 fci at the End-Of-Tape (EOT).

1-13. ERROR RATE. The average non-recoverable read error rate after 100 passes of a perfect tape is 1 byte in 10^7.

1-14. MEAN TIME BETWEEN FAILURE. The Mean Time Between Failure (MTBF) is 2,000 hours or 10^7 blocks (whichever occurs first) with an 80% confidence factor.

1-15. MEAN TIME TO REPAIR. The Mean Time To Repair (MTTR) the equipment is 20 minutes with an 80% confidence factor.

1-16. HEAD DATA. The following data pertains to the Read-After-Write (RAW) Head and the Read/Write (R/W) Head.

a. RAW HEAD.

Gap.....0.150 ± 0.005 inch separation between Read and Write Heads

Write...0.118 inches wide

Read....0.087 inches wide

b. R/W HEAD.

Erase...full width of tape

Read/Write.....0.087 inches wide

1-17. ENVIRONMENTAL CONDITIONS. The environmental limits are for the mechanism only. Actual limits are defined by the magnetic tape used in the system. Limits are as follows:

a. TEMPERATURE.

Storage.....-40°c to 65°c

Operating.... 0°c to 55°c

b. HUMIDITY.

Storage..... 0% to 95% @ 40°c without condensation

Operating.... 10% to 95% @ 40°c without condensation

c. FINISH.

Equipment is fungus and rust proof as per MIL-SPEC MIL-T-21200F.

1-18. TAPE LOCAL ELECTRONIC. The Tape Local Electronic (TLE) is a printed circuit board. Refer to paragraph 4-27 for a detailed discussion.

1-19. TAPE TRANSPORT CONTROL. The Tape Transport Control (TTC) is a printed circuit board. Refer to paragraph 4-63 for a detailed discussion.

1-20. WARRANTY. Redactron Corporation warrants that every instrument manufactured by us to be free from material defects. Servicing or adjustment of a Redactron Corporation instrument and the replacement of any defective part is effective for ninety (90) days after shipping date from factory to the original purchaser. Our liability under this warranty is limited to manufactured defective parts, supplied by Redactron Corporation, and which, subject to our examination, are found to our satisfaction to be defective. Our liability does not cover faults which have occurred as a result of abnormal operating conditions, or misuse. An estimate of repairs will be submitted, in these cases, before work is begun. Refer to paragraphs 1-21 and 1-22 for the proper procedures in preparation for use or reshipment.

1-21. PREPARATION FOR USE. The instrument should be inspected before use. If damaged in any way a claim should be filed with the carrier. The claim agent should prepare a full report of the damage and forward the report to us. The original purchaser will then be advised of the equipment disposition and arrangements will be made for repair or replacement. Refer to paragraphs 1-20 and 1-22 for warranty and preparation for reshipment procedures.

1-22. PREPARATION FOR RESHIPMENT. When a Redactron Corporation instrument appears to be defective it should be returned to us via Railway Express, transportation charges prepaid, by the original purchaser. The instrument should be covered by a protective plastic covering, surrounded by a few inches of excelsior or equivalent shock-absorbing

material, and carefully packed in a sturdy wooden box. Provide full details of the difficulty, including operating symptoms, model number, type number, serial number and purchase date prior to reshipment.

SECTION II. INSTALLATION

2-1. GENERAL.

2-2. The Cassette Transport is shipped completely assembled and ready for use. Inspect the unit for possible shipping damages. Refer to paragraphs 1-20 through 1-22 for information pertaining to warranty and damage claims resulting from shipment.

2-3. UNPACKING.

2-4. The Cassette Transport is shipped in a reinforced packing case to provide maximum protection during handling and shipping. The packing case should be retained for possible reshipment of the equipment.

2-5. All parts of the equipment are to be checked against the packing invoice to ensure that shipment is complete. A visual check is to be performed immediately after unpacking. If after completion of inspection any damage or an incomplete shipment is noted, refer to paragraphs 1-20 through 1-22 for corrective action to be taken.

2-6. MECHANICAL INSTALLATION.

2-7. PHYSICAL DIMENSIONS. Physical dimensions for Cassette Transport are as follows:

- Height.....to fit in 5-1/4 inch rack mount
- Width.....less than 5-3/4 inches
- Depth.....less than 12 inches
- Weight.....approximately 8.5 pounds

2-8. RACK MOUNTING. The Cassette Transport can be mounted in any rack-type-panel providing it meets the required specifications as indicated in figure 2-1. It is important that the dimensions given be strictly adhered to. After cut-out has been made in customer's panel, mount Cassette Transport as follows:

a. Remove Front Bezel Assembly (figure 6-1, item 12).

b. Loosen screws on Adjustable Brackets (figure 6-1, item 15).

c. Extend Adjustable Brackets (figure 6-1, item 14) to maximum distance.

d. Attach Adjustable Brackets to customers panel using four 8-32 screws.

e. Place Front Bezel flush against customer's panel.

f. Slide Cassette Transport chassis forward until it is flush with Bezel Mount Bracket (figure 6-1, item 3).

g. Open plastic Door Front and attach Front Bezel to Front Plate Assembly (figure 6-1, item 18) by tightening 1/4-turn Captive Fasteners (figure 6-1, item 2).

h. Tighten screws in step b.

2-9. ELECTRICAL INSTALLATION.

2-10. Since the Cassette Transport is used in conjunction with options and/or external electronic systems it is required that reference should be made to Connector/Pin Versus Signal (table 2-1) and Interconnecting Wiring Block Diagram (figure 2-2).

CAUTION

The basic Cassette Transport contains a 115 V ac motor. It is possible for a 230 V ac motor to be installed at customer request.

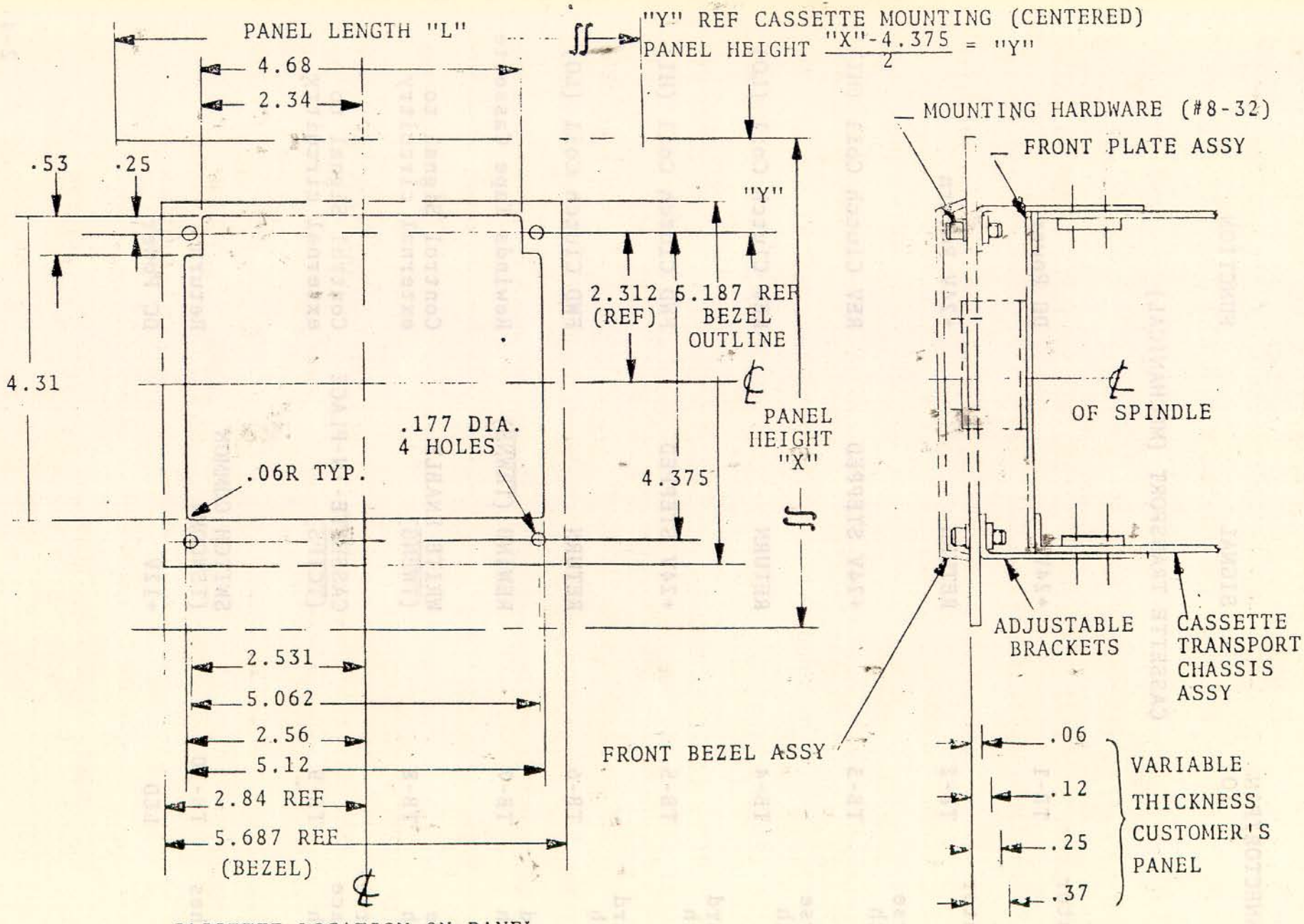


Figure 2-1. Rack Mounting Diagram for Cassette Transport

TABLE 2-1. CONNECTOR/PIN VERSUS SIGNAL

CONNECTOR/PIN FROM	TO	SIGNAL	FUNCTION
		CASSETTE TRANSPORT (MECHANICAL)	
Stop-Actuator Coil	TB-1	+24V	DC Power
Stop-Actuator Coil	TB-2	RETURN	+24V Return
Reverse Clutch Coil	TB-3	+24V STEPPED	REV Clutch Coil (HI)
Reverse Clutch Coil	TB-4	RETURN	REV Clutch Coil (LO)
Forward Clutch Coil	TB-5	+24V STEPPED	FWD Clutch Coil (HI)
Forward Clutch Coil	TB-6	RETURN	FWD Clutch Coil (LO)
Rewind Switch	TB-7	REWIND ($\overline{\text{TRWNS}}$)	Rewinds Tape Cassette
Write Enable Switch	TB-8	WRITE ENABLE ($\overline{\text{TWENS}}$)	Control Signal to external circuitry
Cassette-In-Place Switch	TB-9	CASSETTE-IN-PLACE ($\overline{\text{TCIPS}}$)	Control Signal to external circuitry
Front Panel Assy Switches	TB-10	SWITCH COMMON (TSWCOM)	Return
TB-11	LED	+12V	DC Power

TABLE 2-1. CONNECTOR/PIN VERSUS SIGNAL (Cont)

CONNECTOR/PIN FROM	TO	SIGNAL	FUNCTION
LED	TB-12	RETURN	LED Return
LED (Detector)	TB-13	EOT	Detects End-Of-Tape
Write Head	TB-14	WRITE HEAD	Head Input
Write Head	TB-15	WRITE HEAD	Head Input
TB-16	Chassis	OV (GRD)	Chassis Ground
Read Head	TB-17	READ HEAD (CENTER TAP)	Center Tap to GRD
Read Head	TB-18	READ HEAD	Head Input
Read Head	TB-19	READ HEAD	Head Input
Ext. Source	J11-1	ACH	AC High
Ext. Source	J11-2	ACN	AC Low
Ext. Source	J11-3	AC GRD	AC GRD
		TAPE LOCAL ELECTRONIC (TLE)	
Ext. Source	J9-4, 5	+24V	DC Power
Ext. Source	J9-6, 7	+24V RETURN	DC Return
Ext. Source	J9-8	-12V	DC Power
Ext. Source	J9-9	+12V	DC Power

TABLE 2-1. CONNECTOR/PIN VERSUS SIGNAL (Cont)

CONNECTOR/PIN FROM	TO	SIGNAL	FUNCTION
Ext. Source	J9-10	+5V	DC Power
Ext. Source	J9-11	RETURN	DC Return
J10-1	C-1 (TTC)	REWIND ($\overline{\text{TRWNS}}$)	Local Control
J10-2	C-2 (TTC)	WRITE ENABLE ($\overline{\text{TWENS}}$)	Output Control
J10-3	C-3 (TTC)	CASSETTE-IN-PLACE ($\overline{\text{TCIPS}}$)	Output Control
C-4 (TTC)	J10-4	SWITCH COMMON (TSWCOM)	Switch Common
C-5 (TTC)	J10-5	ALLOW WRITE ($\overline{\text{TWRAL}}$)	Input Command
C-6 (TTC)	J10-6	FORWARD RUN ($\overline{\text{TWDAT}}$)	Input Command
C-7 (TTC)	J10-7	WRITE DATA ($\overline{\text{TWDAT}}$)	Data Input
J10-8	C-8 (TTC)	LEADER DETECTION (TLEDER)	Output Control
J10-9	C-9 (TTC)	READ DATA ($\overline{\text{TRDAT}}$)	Serial Data Output
C-10 (TTC)	J10-10	REVERSE RUN ($\overline{\text{TREV}}$)	Input Command
J10-11	C-11 (TTC)	TAPE PHASE REF ($\overline{\text{TPREF}}$)	Data Output
		TAPE TRANSPORT CONTROL (TTC)	
Ext. Source	TTC	DC RETURN	DC Power
Ext. Source	TTC	+5V	DC Power

TABLE 2-1. CONNECTOR/PIN VERSUS SIGNAL (Cont)

CONNECTOR/PIN FROM	TO	SIGNAL	FUNCTION
Ext. Source	A20-10	-12V	DC Power
A-1	Ext. Source	REWIND (TRWNS)	Output Control
A-2	Ext. Source	WRITE ENABLE (TWENS)	Output Control
A-3	Ext. Source	CASSETTE-IN-PLACE (TCIPS)	Output Control
A-5	Ext.	WRITE OK (COKTWR)	Defines active write area on completion of motion start up time and IRG delays
Ext. Source	A-7	WRITE DATA (CWDATA)	Data bit is presented on this line for recording
Ext. Source	A-11	CLEAR (CCLEAR)	A "power on clear" (clear logic)
A-12	Ext. Source	BUSY (CMTBSY)	Indicates cassette not loaded, or cassette transport performing requested function (e.g. READ, WRITE)
Ext. Source	A-13	INHIBIT SPROCKETS (CINSPK)	Suppression of sprockets special pattern generation
A-14	Ext. Source	MOTION TIME OUT (CMTMO)	Indicates data activity
Ext. Source	B-1	REWIND (CARWN)	Pulse activates rewind function to rewind tape
Ext. Source	B-2	FORWARD (ANYFWD)	Forward Command
Ext. Source	B-3	FWD/REV READ COMMAND (CREAD)	Read Command issued in conjunction with ANYFWD

TABLE 2-1. CONNECTOR/PIN VERSUS SIGNAL (Cont)

CONNECTOR/PIN FROM	TO	SIGNAL	FUNCTION
Ext. Source	B-4	WRITE ACTIVE	Data available for transfer on WRITE DATA line
B-6	Ext. Source	WRITE CLOCK ($\overline{\text{CWRCLK}}$)	Pulse that samples input WRITE DATA
B-7	Ext. Source	READ ACTIVE (CRACTV)	Tape moving through the region of active READ DATA
B-8	Ext. Source	READ CLOCK (CRDCLK)	Pulse defining presence of READ DATA available for sampling
B-9	Ext. Source	READ DATA (CRDATA)	0 and 1 bit serial data available
B-10	Ext.	LEADER DETECTION (TLEDER)	Detects leader on tape
B-12	TP	COUNT DOWN ($\overline{\text{CCDN}}$)	Ratio Detector Counter, counting in the down direction
Ext. Source	B-14	CLOCK PULSE (01X)	Strobe Pulse
Ext. Source	B-16	MAIN CLOCK (02X)	Main system clock signal generated from basic clock

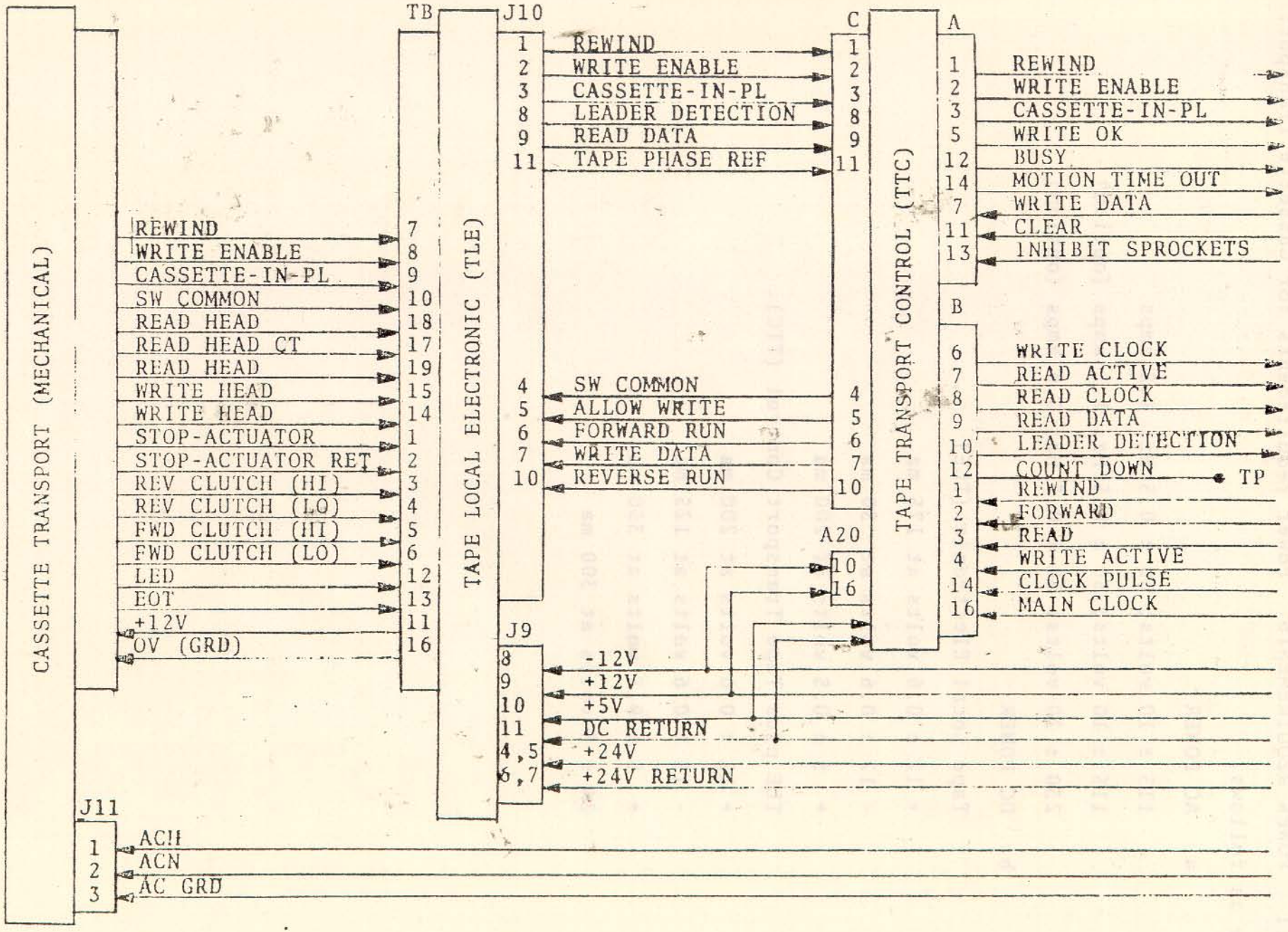


Figure 2-2. Interconnecting Wiring Block Diagram, Cassette Transport

2-11. POWER REQUIREMENTS. Power requirements for Cassette Transport are as follows:

a. AC POWER

115 ± 10 volts; 60 ± 0.5 Hz; 1.2 amps

115 ± 10 volts; 50 ± 0.5 Hz; 1.2 amps (option)

230 ± 20 volts; 50 ± 0.5 Hz; 0.6 amps (option)

b. DC POWER

Tape Local Electronic (TLE)

+ 12 ± 0.6 volts at 175 ma

- 12 ± 0.6 volts at 50 ma

+ 5 ± 0.5 volts at 200 ma

TLE plus Tape Transport Control (TTC).

+ 12 ± 0.6 volts at 200 ma

- 12 ± 0.6 volts at 125 ma

+ 5 ± 0.5 volts at 350 ma

24 ± 3 volts at 300 ma

SECTION III. OPERATION

3-1. GENERAL.

3-2. This section describes the operating controls and operating procedure for the Cassette Transport. It is assumed that the equipment has been properly installed and that the initial installation check has been performed as described in Section II.

3-3. OPERATING CONTROLS.

3-4. The Cassette Transport is designed to be used and controlled by other external equipment. As a result, local operator controls are limited to two local control buttons.

3-5. LOCAL CONTROLS. The Cassette Transport contains the following local controls.

a. REWIND BUTTON. Depressing this button allows the tape cassette to rewind itself. The REWIND button located on the upper left of the Front Bezel must be used with external control equipment.

b. EJECT BUTTON. Whenever the tape cassette is to be removed from the Cassette Transport the EJECT button located on the upper right of the Front Bezel is to be pushed in by the operator.

3-6. REMOTE CONTROLS. Control signals to and from the Cassette Transport that are used in conjunction with external control circuitry are shown in the Interconnecting Wiring Block Diagram, figure 2-2.

3-7. LOADING TAPE CASSETTE. The tape cassette is loaded into the Cassette Transport by opening the plastic door on the Front Bezel and inserting the tape cassette into its holding blocks. To remove tape cassette press EJECT button and remove cassette.

NOTE

Anytime that the tape cassette does not smoothly snap into place and smoothly eject, it is recommended that the Cassette Transport be serviced.

3-8. OPERATOR'S MAINTENANCE. The Magnetic Head is to be cleaned once a week using Isopropyl Alcohol and a cotton swab.

3-9. READ/WRITE TECHNIQUES.

3-10. Various READ/WRITE techniques may be used with the Cassette Transport. Two recommended techniques for READ/WRITE are presented in paragraphs 3-12 and 3-17.

3-11. When Option-1 (paragraph 1-4) is selected, it is recommended that the READ/WRITE technique based on ratios in paragraph 3-12 be used. The reason being that it combines the highest usable density with a very high tolerance to speed variation and permits a transfer rate of 1500 bytes/second. The READ/WRITE technique in paragraph 3-17 is a modified phase recording method which has a lower recording density.

3-12. READ/WRITE SYSTEM BASED ON RATIOS.

3-13. The ratio technique of reading and writing data is considered to be a comparatively new concept in data transfer to and from magnetic tape. It is derived by the use of bit cells containing one data bit. A bit cell is defined by one clock pulse period. In the case of the Cassette Transport, the bit cell rate is 12,000 p.p.s. resulting in a two-microsecond negative going pulse occurring approximately every 83 microseconds.

3-14. When data is to be written on tape, a maximum density of that specified in paragraph 1-12 is achieved. A data "0" is written 27 microseconds after the negative going transition representing the start of a bit cell. A data "1" is written 54 microseconds after the negative going transition representing the start of a bit cell.

3-15. During data recovery (reading) a 32 increment Up/Down Counter is used. The start of the bit cell enables the counter to start incrementing. The next pulse causes the counter to decrement until the start of the next bit cell at which time the process repeats. Since a data "0" bit is written 27 microseconds after the start of the bit cell, the counter will increment for one-third of a bit cell (27 usec./83 usec.) and then decrement for two-thirds of a bit cell ((83 usec.-27 usec.)/83 usec.) when the data "0" is read. Therefore, the counter will decrement more times that it will increment. This is indicated by an "underflow" level. Since a data "1" is written 54 microseconds after the start of a bit cell, the counter will increment for two thirds of a

bit cell (54 usec./83 usec.) and then decrement for one-third of a bit cell ((83 usec. - 54 usec)/83 usec) when the data "1" is read. Therefore, the counter will increment more than it will decrement. In this case the "underflow" level is not produced.

3-16. In conclusion, when the "underflow" level is present, the bit cell contains a data "0". Conversely when the "underflow" level is absent, the bit cell contains a data "1".

3-17. READ/WRITE SYSTEM BASED ON MODIFIED PHASE RECORDING.

3-18. A modified phase recording scheme may also be used with the Cassette Transport. With this method, each transition of a 50% duty cycle clock pulse defines the boundaries of a bit cell. When a data "0" is to be recorded within the bit cell, no change to the clock pulse is effected. When a data "1" is to be recorded, an added transition is effected to the clock pulse. This added transition (data "1") occurs at a time equal to 25% of the bit cell time.

3-19. During data recovery each transition recorded on tape, both bit cell and data "1's", produces a negative-going pulse. When this serial stream of pulses is read, those pulses caused by bit cell transitions are eliminated, leaving only negative going pulses due to data "1's".

SECTION IV. THEORY OF OPERATION

4-1. GENERAL.

4-2. This section provides a functional block diagram discussion and a detailed functional analysis for the Cassette Transport and its options.

4-3. To facilitate the understanding of the theory of operation of the Cassette Transport this section provides timing diagrams and functional block diagrams. In addition, schematic diagrams in Section VII are to be used in conjunction with this section.

4-4. OPTIONS. The Cassette Transport is a general purpose single channel tape recorder. Refer to paragraph 1-4 for various combinations of options that are possible. Also, refer to paragraph 3-12 and 3-13 for a detailed discussion of the two READ/WRITE techniques that Redactron recommends to be used in conjunction with the Cassette Transport.

4-5. BLOCK DIAGRAM DISCUSSION, FUNCTIONAL.

4-6. TAPE DRIVE SYSTEM.

4-7. The tape drive system (figure 4-1) consists of an AC motor with an associated pulley belt system that drives two separate Clutch-Spindle Assemblies. When either the Forward or Reverse Clutch is energized, that respective spindle is mechanically engaged to the motor drive. The energized Clutch-Spindle Assembly, in turn, drives the cassette tape reel, moving the magnetic tape in either the forward or reverse direction.

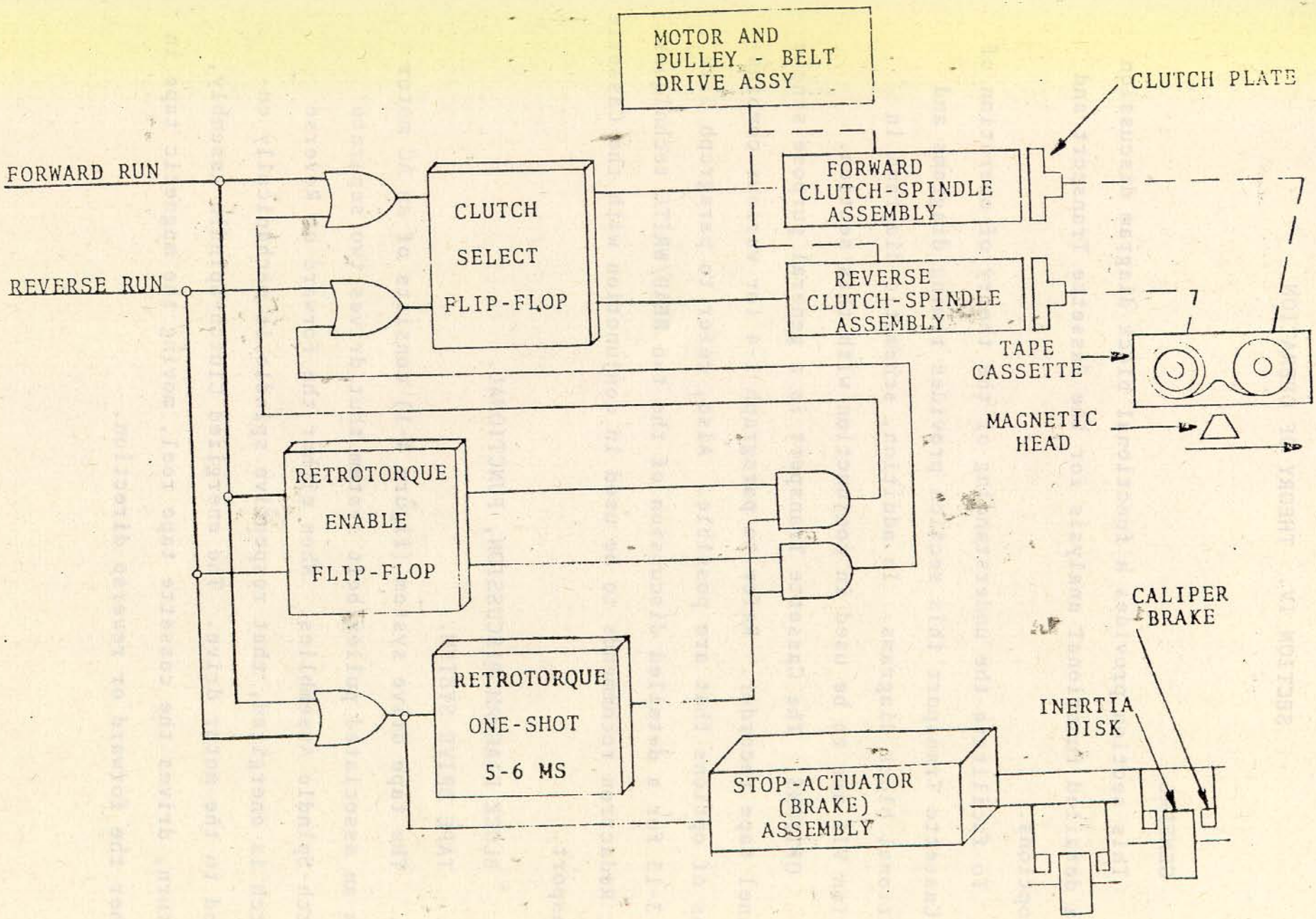


Figure 4-1. Tape Drive Block Diagram, Simplified.

4-8. CLUTCH SELECT FLIP-FLOP. The Clutch Select Flip-Flop selects either the Forward or Reverse Run solenoid coil. When either clutch solenoid coil is energized it mechanically engages the tape cassette spindle drive to the Motor Drive Assembly. If the Forward Clutch-Spindle drive is engaged, the reverse tape spindle drive is free-wheeling. If the Reverse Clutch-Spindle drive is engaged the forward tape spindle drive is free-wheeling.

4-9. RETROTORQUE CLUTCH CIRCUITRY.

4-10. When the tape drive system is driving the tape cassette reel in either the forward or reverse direction, the Retrotorque Clutch Circuitry (upon sensing either a change in direction command, or a stop condition) will apply a momentary signal to the Clutch Select Flip-Flop. This allows the opposite Clutch-Spindle Assembly (i.e., the free-wheeling spindle) to energize. This results in the tape cassette reel to be momentarily driven in the opposite direction. This momentary driving of the tape reel in the opposite direction in conjunction with the Stop-Actuator (Brake) makes it possible for the tape cassette reels to come to a smooth stop. At the same time it ensures that there will not be any spilling or breakage of magnetic tape.

4-11. RETROTORQUE ENABLE FLIP-FLOP. The Retrotorque Enable Flip-Flop memorizes whether the Forward or Reverse Run command is present. It then selects the proper gate that will allow the momentary retrotorque pulse signal, that is generated by the Retrotorque One-Shot, to energize the free-wheeling Clutch-Spindle Assembly. This results in the tape cassette reel to be momentarily driven in the opposite direction.

4-12. RETROTORQUE ONE-SHOT. The Retrotorque One-Shot generates a five to six millisecond pulse which is applied to one of the Clutch-Spindle Assemblies. The retrotorque pulse is always applied to the Clutch-Spindle Assembly that is free-wheeling. The Retrotorque One-Shot pulse is always generated in conjunction with the Stop-Actuator (Brake), except on initial power turn-on of the tape cassette recorder.

4-13. STOP-ACTUATOR.

4-14. The Stop-Actuator (Brake) Circuitry applies caliper-type brakes to each of the interia disks, located on the Forward, and Reverse Clutch-Spindle Assembly. The Stop-Actuator brakes are applied when initial power is turned on and no forward or reverse tape motion is requested; or when the tape cassette is being driven in either the Forward or Reverse Run direction and the opposite run direction is requested; or when in the Forward or Reverse Run a complete stop condition is requested.

4-15. WRITE CHANNEL CIRCUITRY.

4-16. Serial digital data from an external source (figure 4-2) arrives at connector J10-7. This digital data is coupled through Write Enable gates to the Write Head. The Allow Write ($\overline{\text{TWRAL}}$) signal controls the enabling or inhibiting of the Write Enable gates.

4-17. The Write Channel Circuitry also develops a DC limiting and threshold voltage level that is used in the Read Channel Circuitry.

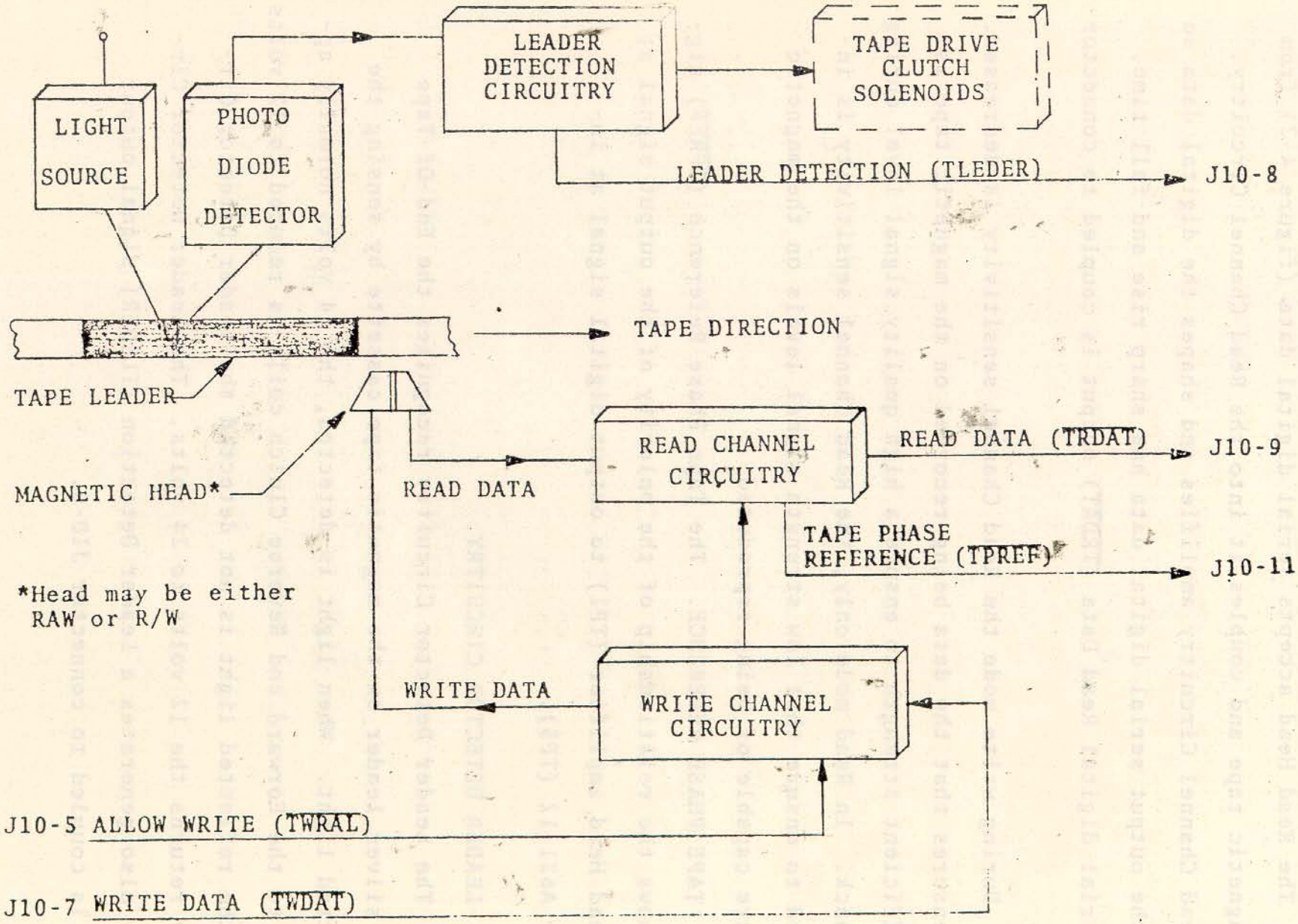


Figure 4-2. Magnetic Tape RAW Block Diagram, Simplified.

4-18. READ CHANNEL CIRCUITRY.

4-19. The Read Head accepts serial digital data (figure 4-2) from the magnetic tape and couples it into the Read Channel Circuitry. The Read Channel Circuitry amplifies and shapes the digital data so that the output serial digital data has sharp rise and fall time. The serial digital Read Data ($\overline{\text{TRDAT}}$) output is coupled to connector J10-9.

4-20. During write mode the Read Channel sensitivity is decreased. This ensures that the data being recorded on the magnetic tape is of sufficient strength to ensure a high quality signal level during read back. In Read mode only, the Read Channel sensitivity is increased to ensure that low strength signal levels on the magnetic tape are capable of being reproduced.

4-21. TAPE PHASE REFERENCE. The Tape Phase Reference ($\overline{\text{TPREF}}$) signal shows the relationship of the polarity of the output signal at the Read Head amplifier (TP1) to output digital signal at inverter A6Z1-12 (TP5).

4-22. LEADER DETECTOR CIRCUITRY.

4-23. The Leader Detector Circuitry recognizes the End-Of-Tape (EOT) silver leader on the magnetic tape cassette by sensing the reflected light. When light is detected, the 24 volts normally applied to the Forward and Reverse Clutch coils is reduced to 12 volts. When the reflected light is not detected the Leader Detector Circuitry returns the 12 volts to 24 volts. The Leader Detector Circuitry also generates a Leader Detection (TLEDER) signal output which is coupled to connector J10-8.

4-24. VOLTAGE REQUIREMENTS.

4-25. All DC voltages required in the Magnetic Tape Cassette Transport are provided by an external voltage source. The AC power requirement may be either 115 VAC, 60 or 50 Hz; or 230 VAC, 50 Hz. Refer to paragraph 2-11 for a more detailed description of input power requirements.

4-26. FUNCTIONAL CIRCUIT ANALYSIS.

4-27. TAPE LOCAL ELECTRONICS. Functional circuit analysis for the Tape Local Electronic (TLE) printed circuit board is divided into six main areas. These areas are as follows: Tape Drive Circuitry, Retrotorque Clutch Circuitry, Write Channel Circuitry, Read Channel Circuitry, Stop-Actuator (Brake) Circuitry, Leader Detector Circuitry.

NOTE

Logic 1 = $+5.0\ ^{+0.0}_{-2.2}$ VDC

Logic 0 = $0.0\ ^{+0.4}_{-0.0}$ VDC

4-28. TAPE DRIVE CIRCUITRY.

4-29. When the Forward Run ($\overline{\text{TFWD}}$) and Reverse Run ($\overline{\text{TREV}}$) input signals are at a Logic 1 (figure 4-3) the Forward and Reverse Clutch are in the de-energized position. When either the $\overline{\text{TFWD}}$ or $\overline{\text{TREV}}$ signal goes to a Logic 0 that respective clutch becomes energized resulting in the tape cassette running in either the forward or reverse direction.

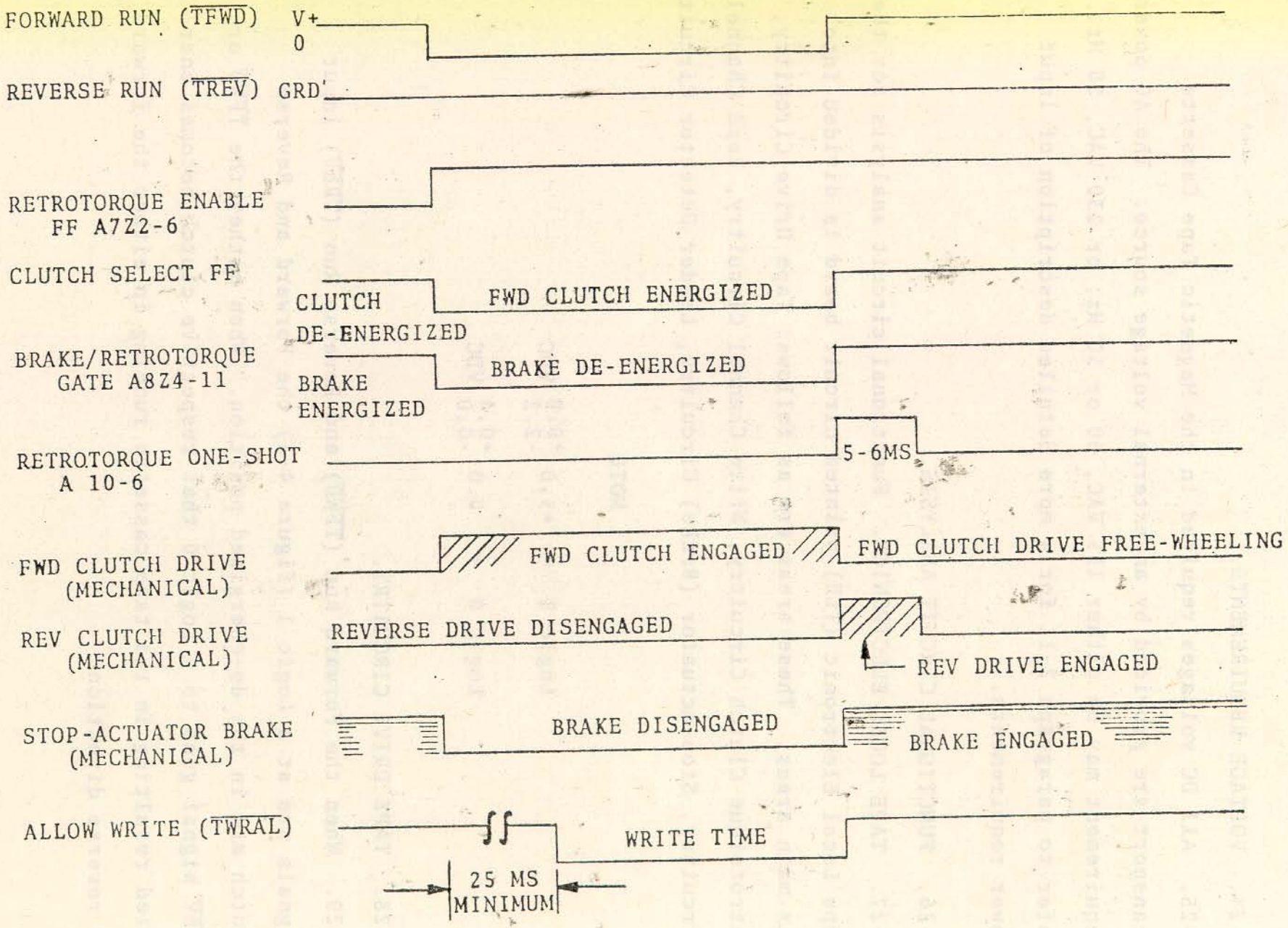


Figure 4-3. Tape Drive Control Timing Diagram, Forward Run.

4-30. FORWARD CLUTCH ENERGIZE. Forward Run ($\overline{TFWD}$) signal from connector J10-6 is coupled to the input of inverter A6-9. When $\overline{TFWD}$ signal goes to a logic 0 the output of A6Z1-8 goes to a Logic 1. This signal is coupled to the input of inverter A6Z2-5 resulting in the output of A6Z2-6 going to a Logic 0. This signal is coupled to three separate places as follows: to Retrotorque Enable Flip-Flop, to nand gate A8Z2-4, and to nand gate A7Z1-1.

4-31. RETROTORQUE ENABLE FLIP-FLOP. The Retrotorque Enable Flip-Flop is a DC set-reset flip-flop consisting of nand gates A7Z2 and A7Z3. When $\overline{TFWD}$ signal at A7Z2-4 goes to a Logic 0 it sets the Retrotorque Enable Flip-Flop output pin 6 to a Logic 1 and output pin 8 to a Logic 0. The output signal from A7Z3-8 inhibits nand gate A8Z1. The output signal from A7Z2-6 enables nand gate A7Z4. At this time pin 4 of nand gate A8Z2 is at a Logic 0 resulting in output pin 6 to be at a Logic 1. This signal is coupled to the Clutch Select Flip-Flop. The output signal from Retrotorque One-Shot A10-6 is at a Logic 0. This signal is coupled to the input of nand gate A7Z4 resulting in output pin 11 going to a Logic 1. Since both inputs to nand gate A9Z1 are at a Logic 1, the output signal at A9Z1-11 is a Logic 0. This signal is coupled to the Clutch Select Flip-Flop.

4-32. CLUTCH SELECT FLIP-FLOP. The Clutch Select Flip-Flop is a DC set-reset flip-flop consisting of nand gates A8Z3 and A9Z2. When the input signal at A9Z2-2 goes to a Logic 0, it sets Clutch Select Flip-Flop output A9Z2-3 to a Logic 1 and output A8Z3-3 to a Logic 0. The output of A8Z3-3 is coupled to input of current driving chip A11-6. This signal is inverted in chip A11 resulting in the current driver transistor to be forward biased. This transistor provides a

ground return for the Forward Clutch solenoid. With the Forward Clutch energized the magnetic tape cassette is driven in the forward direction. At the same time that input signal to A11-6 is at Logic 0, the input signal to A11-1 is at a Logic 1. This results in the current driving transistor in chip A11 to be reverse biased. Since no ground return is provided for the Reverse Clutch solenoid, the Reverse Clutch solenoid is de-energized allowing the Reverse Clutch-Spindle Assembly to free-run.

4-33. REVERSE CLUTCH ENERGIZE. Signal path flow to energize the Reverse Clutch solenoid is the same as the signal path to energize the Forward Clutch solenoid. The difference is that the input Reverse Run ($\overline{\text{TREV}}$) signal is at a Logic 0 and the input Forward Run ($\overline{\text{TFWD}}$) signal is at a Logic 1. With these two signal conditions the Retrotorque Enable Flip-Flop output A7Z3-8 is set to a Logic 1. The Clutch Select Flip-Flop A9Z2-3 is at a Logic 0. When A9Z2-3 is at a Locig 0 the base of current driving transistor in chip A11 is forward biased providing a ground return for the Reverse Clutch solenoid. With the Reverse Clutch solenoid energized, the magnetic tape cassette is driven in the reverse direction. Since no ground return is provided for the Forward Clutch solenoid, the Forward Clutch is de-energized allowing the Forward Clutch-Spindle Assembly to free-run.

4-34. RETROTORQUE CLUTCH CIRCUITRY.

4-35. In the Forward Run condition the input signal to A7Z1-1 is at a Logic 0 resulting in the output signal of nand gate A7Z1-3 to be at a Logic 1. This signal is coupled to the input of nand gate A8Z4-12 resulting in the output signal at A8Z4-11 to be at a Logic 0.

This signal is coupled to the input of Retrotorque One-Shot A10-5 and to the base of transistor Q2.

4-36. RETROTORQUE ONE-SHOT. When the Forward Run ($\overline{\text{TFWD}}$) signal returns to a Logic 1 the output of nand gate A8Z4-11 goes to a Logic 1. This positive going edge results in the output of Retrotorque One-Shot generating a positive pulse with a pulse width of approximately five to six milliseconds. Since the Retrotorque Enable Flip-Flop has enabled nand gate A7Z4 the five millisecond pulse is gated through nand gate A7Z4-13. The inverted signal output signal at A7Z4-11 is coupled to nand gate A9Z1-12. The output of A9Z1-11 sets the Clutch Select Flip-Flop so that the output at A9Z2-3 is at a Logic 0 for a pulse duration of five to six milliseconds. This pulse signal is coupled to the input of A11-1. During this period of time the base of current driving transistor is forward biased resulting in the Reverse Clutch solenoid being energized for a time period of five to six milliseconds. With the Reverse Clutch energized the Reverse Clutch-Spindle Assembly drive is running in the reverse direction for a period of five to six milliseconds.

4-37. STOP-ACTUATOR.

4-38. BRAKE ENERGIZED. When the output of nand gate A8Z4-11 is at a Logic 1, +5 volts is applied to the base of transistor Q2. With transistor Q2 forward biased a ground return is provided for the Stop-Actuator (Brake) solenoid coil. With the solenoid coil energized two caliper-type brake shoes are applied to each of the inertia disks.

4-39. BRAKE DE-ENERGIZED. When the output of nand gate A8Z4-11 is at Logic 0 (ground), the +5 volts at resistor R29 is pulled to ground. This results in transistor Q2 to be reversed biased. Since no ground return is provided, the Stop-Actuator (Brake) solenoid coil is not energized. This results in no brake pressure applied to the two inertia disks.

4-40. WRITE CHANNEL CIRCUITRY.

4-41. WRITE DATA ENABLE. When recording (writing) is not required, the Allow Write ($\overline{\text{TWRAL}}$) signal (figure 4-4) from connector J10-5 is at a Logic 1. When recording is required the $\overline{\text{TWRAL}}$ signal goes to a Logic 0 enabling the Write Channel Circuitry.

4-42. When Allow Write ($\overline{\text{TWRAL}}$) goes to a Logic 0, the output of nand gate A9Z3-6 goes to a Logic 1. This signal enables write gates A9Z4-9 and A12Z4-9 allowing serial digital data to be gated through to the current drivers in chip A13.

4-43. WRITE DATA. Digital data to be recorded arrives on the Write Data ($\overline{\text{TWDAT}}$) line from connector J10-7. This digital data is coupled to write gate A9Z4-10, and to write gate A12Z2-10 through inverter A12Z1. Output signals from the write gates are coupled to current driver transistors in chip A13. Since the input signal at the two write gates are always complimentary to each other only one of the two current drivers in chip A13 can be forward biased. The other current driver is reverse biased.

4-44. The direction of the current flow in the Write Head coil depends on which current drive transistor in chip A13 is forward biased. Current flow in one direction represents a Logic 0 and current flow in the opposite direction represents a Logic 1.

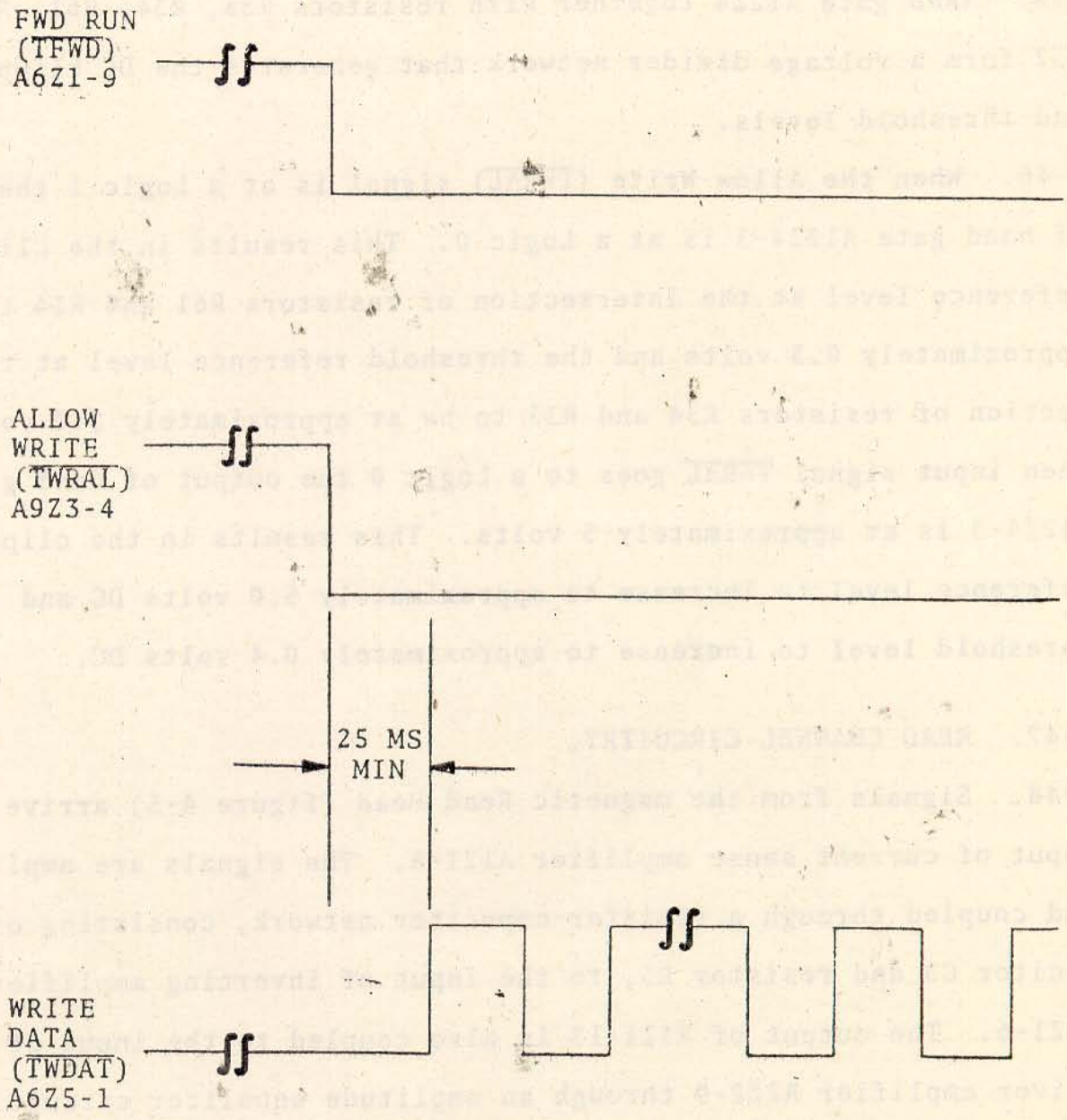


Figure 4-4. Write Channel Timing Diagram.

4-45. CLIPPING AND THRESHOLD LEVELS. The clipping and threshold DC levels generated in the write circuits are only used in the Read Channel Circuitry but are controlled by the Allow Write ($\overline{\text{TWRAL}}$) signal. Nand gate A12Z4 together with resistors R35, R34, R61, R33 and R32 form a voltage divider network that generates the DC clipping and threshold levels.

4-46. When the Allow Write ($\overline{\text{TWRAL}}$) signal is at a Logic 1 the output of nand gate A12Z4-3 is at a Logic 0. This results in the clipping reference level at the intersection of resistors R61 and R34 to be approximately 0.3 volts and the threshold reference level at the intersection of resistors R34 and R35 to be at approximately 0.2 volts. When input signal $\overline{\text{TWRAL}}$ goes to a Logic 0 the output of nand gate A12Z4-3 is at approximately 5 volts. This results in the clipping reference level to increase to approximately 5.0 volts DC and the threshold level to increase to approximately 0.4 volts DC.

4-47. READ CHANNEL CIRCUITRY.

4-48. Signals from the magnetic Read Head (figure 4-5) arrive at the input of current sense amplifier A1Z1-8. The signals are amplified and coupled through a resistor-capacitor network, consisting of capacitor C3 and resistor R5, to the input of inverting amplifier A2Z1-6. The output of A1Z1-13 is also coupled to the input of driver amplifier A2Z2-9 through an amplitude equalizer circuit.

4-49. AMPLITUDE EQUALIZER. Signal inputs from the magnetic Read Head are of various signal strength resulting in the signal outputs from amplifier A1Z1 to vary in amplitude. To equalize these various signal amplitudes the signal is coupled into an amplitude equalizing circuit. This circuit consists of variable resistor R5 and diodes

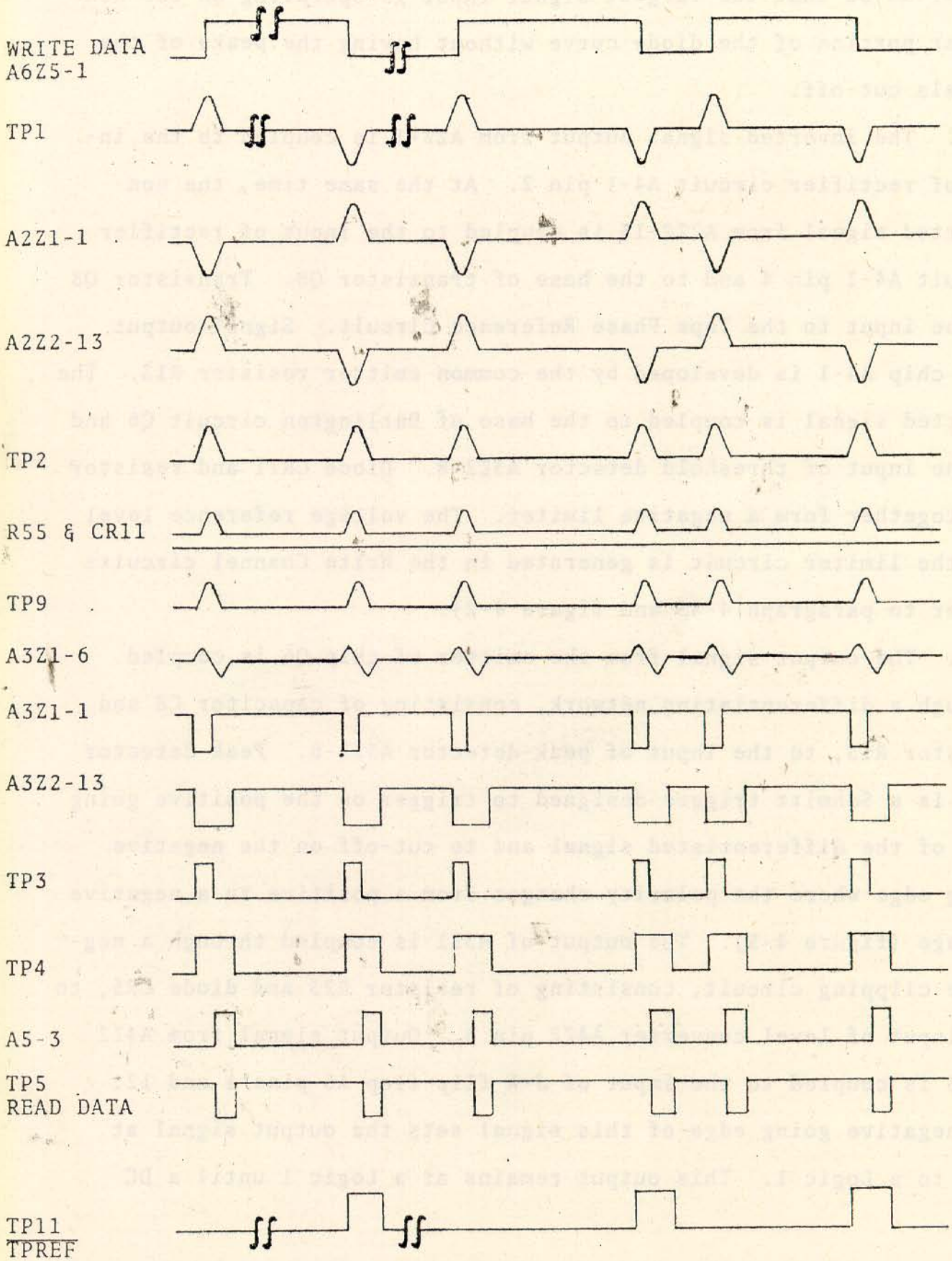


Figure 4-5. Read Channel Timing Diagram.

CR1 and CR2. The signals are equalized by adjusting variable resistor R5 so that the largest signal input is operating on the non-linear portion of the diode curve without having the peaks of the signals cut-off.

4-50. The inverted signal output from A2Z-1 is coupled to the input of rectifier circuit A4-1 pin 2. At the same time, the non-inverted signal from A2Z2-13 is coupled to the input of rectifier circuit A4-1 pin 4 and to the base of transistor Q8. Transistor Q8 is the input to the Tape Phase Reference Circuit. Signal output from chip A4-1 is developed by the common emitter resistor R13. The detected signal is coupled to the base of Darlington circuit Q6 and to the input of threshold detector A3Z2-8. Diode CR11 and resistor R55 together form a negative limiter. The voltage reference level for the limiter circuit is generated in the Write Channel circuits (refer to paragraph 4-45 and figure 4-2).

4-51. The output signal from the emitter of chip Q6 is coupled through a differentiating network, consisting of capacitor C8 and resistor R15, to the input of peak-detector A3Z1-6. Peak detector A3Z1 is a Schmitt trigger designed to trigger on the positive going edge of the differentiated signal and to cut-off on the negative going edge where the polarity changes from a positive to a negative voltage (figure 4-5). The output of A3Z1 is coupled through a negative clipping circuit, consisting of resistor R23 and diode CR5, to the input of level converter A4Z2 pin 6. Output signal from A4Z2 pin 8 is coupled to the input of J-K flip-flop A5 pins 1 and 12. The negative going edge of this signal sets the output signal at A5-3 to a Logic 1. This output remains at a Logic 1 until a DC

reset signal arrives at A5-13. Digital output data from A5-3 is coupled through inverter A6Z1 to connector J10-9.

4-52. DC RESET SIGNAL. Threshold detector A3Z2 is a Schmitt trigger. The threshold voltage level at A3Z2-9 is developed at the intersection of resistors R34 and R35. The DC voltage at the intersection of R34 and R35 has two possible DC levels. The DC levels are determined on whether the Allow Write ($\overline{\text{TWRAL}}$) signal input is ON or OFF (refer to paragraph 4-46). The output of threshold detector A3Z2-13 is coupled through a negative clipping circuit, consisting of resistor R23 and diode CR5, to the input of level converter A4Z2 pin 9. The inverted signal at the output of A4Z2 pin 11 is the DC reset signal for the J-K flip-flop A5.

4-53. TAPE PHASE REFERENCE. The Tape Phase Reference ($\overline{\text{TPREF}}$) signal shows the relationship of the polarity of the output signal at the Read Head sense amplifier (TP1) to the output digital signal at inverter A6Z1-12 (TP5). See figure 4-6 for an example of the relationship between signals.

4-54. Tape Phase Reference circuits consist of transistors Q8 and Q9. Output signal from A2Z2-13 is coupled to the base of transistor Q8. Output signal from emitter resistor R62 is coupled to the base of transistor Q9. The output signal from collector resistor R63 is the Tape Phase Reference ($\overline{\text{TPREF}}$) signal. This signal is coupled to connector J10-11. The collector voltage applied at the top of resistor R63 depends on whether A4Z2 pin 11 is conducting or not conducting.

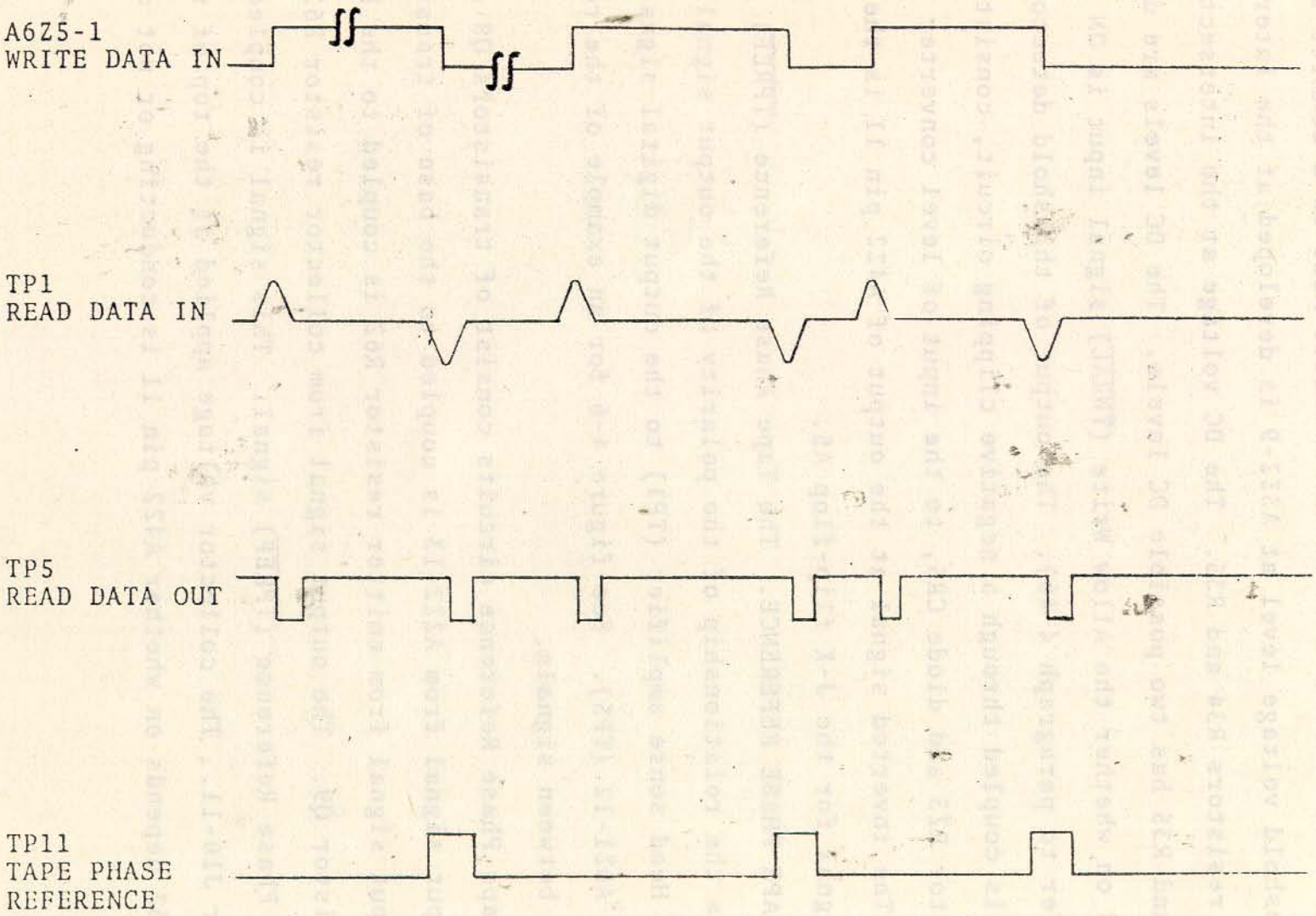


Figure 4-6. Tape Phase Reference Signal Compared to Read and Write Data.

4-55. LEADER DETECTION CIRCUITRY.

4-56. LEADER DETECTED. The photo diode detector senses reflected light from the End-Of-Tape (EOT) leader resulting in the DC voltage at the intersection of resistor R39 and R57 to go from a negative voltage to a positive voltage. Variable resistor R40 together with resistors R39 and R41 form a voltage divider network. Variable resistor R40 controls the sensitivity of the Leader Detection Circuitry.

4-57. When End-Of-Tape leader is detected the voltage between resistor R39 and R40 goes from a negative DC voltage (between -5 and -8 volts) to a positive DC voltage (between 5 and 8 volts positive). This positive going edge is coupled to the base of transistor Q7 resulting in the emitter voltage to go from a minus 9 volts to a plus 6 volts. Capacitor C18 in the emitter circuit of transistor Q7 prevents rapid fluctuation in the DC voltage (figure 4-7). This positive going voltage is coupled to the input of Schmitt trigger A1Z2-6. The positive going voltage triggers the Schmitt trigger resulting in the output of A1Z2-1 to go from +7 volts to -8 volts. When the End-Of-Tape leader comes to an end, the output of the Schmitt trigger goes from a -8 volts to +7 volts. The pulse width at the output of A1Z2-1 is approximately the length of the End-Of-Tape leader.

4-58. Due to the integrating action of capacitor C18 the leading edge of the output pulse at A1Z2-1 is delayed with respect to the leading edge at Q7 emitter. The output of A1Z2-1 is coupled through a negative limiting circuit to the base of transistor Q1. Resistor R46 and diode CR9 together from a negative limiter. The Leader Detection (TLEDER) signal from the collector of transistor Q1 is

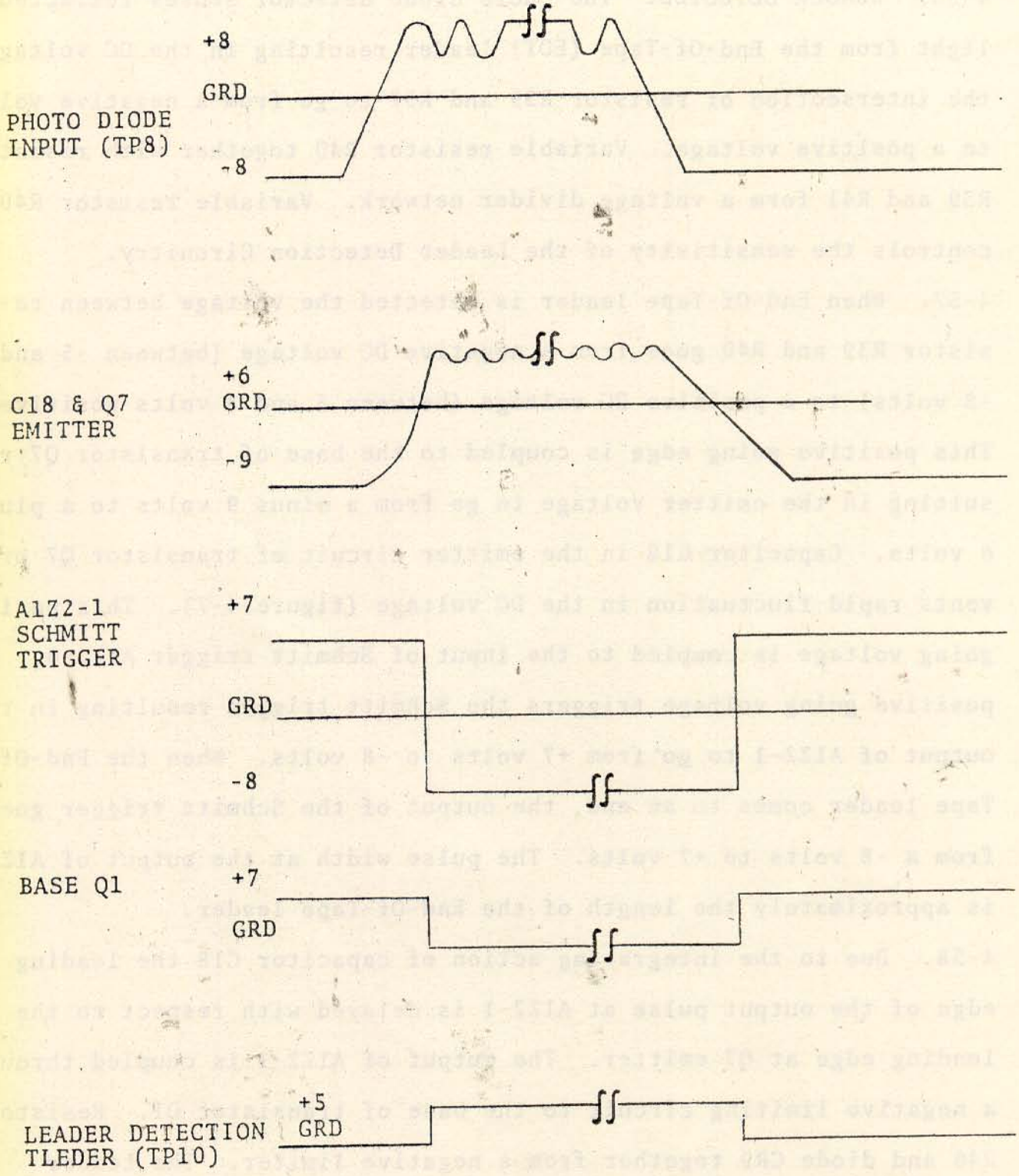


Figure 4-7. Lead Detector Circuit Timing Diagram.

coupled to connector J10-8 and to the base of transistor Q3 through resistor R50.

4-59. Clutch Solenoid Voltage. Transistor Q3 is forward biased for a period of time that is equal to the Leader Detection pulse width. Transistor Q3 provides a ground for voltage divider network consisting of resistor R51 and R52. When transistor Q3 is conducting, the 24 volts DC at the base of amplifier Q4 drops to 12 volts DC. This decrease in voltage reduces current flow through transistor Q4 and its emitter resistor R53. The voltage drop developed across emitter resistor R53 decreases to approximately 12 volts. This decrease in voltage decreases the forward bias on the base of transistor Q5 reducing current flow through the transistor. This results in 12 volts to be at the emitter of Q5. The effect of 12 volts being applied to the clutch solenoid coils is to reduce the clutch plate torque from 40 + 5 to 30 ±5 inch/ounces.

4-60. LEADER NOT DETECTED. When reflected light is not detected from the End-Of-Tape (EOT) leader by the photo diode detector the DC voltage at the intersection of resistor R39 and R57 is between -5 and -8 volts. This results in the emitter of transistor Q9 to be at -9 volts and the output of Schmitt trigger A1Z2-1 to be at + 7 volts. The output of transistor Q1 is normally at ground. This ground is coupled to base of transistor Q3 reverse biasing it. This results in 24 volts to be at the intersection of resistor R51 and R52. This positive voltage is coupled to the base of transistor Q4 resulting in 24 volts to be developed by emitter resistor R53. This positive voltage is coupled to the base of transistor Q5 allowing maximum current flow through the transistor.

4-61. SWITCH SIGNAL DETECTION, MECHANICAL.

4-62. The Cassette Transport contains three mechanical switches which provide controls signals for external circuitry (i.e., external to the TLE). The switches are as follows:

- o REWIND SWITCH — With tape cassette not in place, this switch is normally open. One side of switch is connected to J10-4 (switch common); the other side of switch is connected to J10-1.
- o WRITE ENABLE SWITCH — With tape cassette not in place, this switch is normally closed. One side of switch is connected to J10-4 (switch common); the other side of switch is connected to J10-2.
- o CASSETTE-IN-PLACE SWITCH — With tape cassette not in place, this switch is normally closed. One side of the switch is connected to J10-4 (switch common); the other side is connected to J10-3.

4-63. TAPE TRANSPORT CONTROL.

4-64. The Tape Transport Control (TTC) is a MOS device which performs the basic functions required for the reading and writing of data on the Cassette Transport. Figure 4-8 is a functional block diagram of the TTC. Figure 4-9 illustrates the TTC with its pin designations and signal assignments. Refer to table 2-1 for signal functions. The TTC provides two methods of reading and writing. These methods are described in paragraphs 3-12 and 3-17.

4-65. CONTROL TIMING. Due to the synchronous operation of the TTC, clock signals must be provided from an external source. Henseforth, these clock signals will be designated $\overline{\emptyset 1}$ (CLOCK PULSE) and $\overline{\emptyset 2}$ (MAIN CLOCK). The TTC employs these clock signals to produce the read clock ($\overline{\text{CRDCLK}}$) and write clock ($\overline{\text{CWRCLK}}$) used to synchronize data transfer between the TTC and the external source. In conjunction with their associated data signals, the read and write clocks are also used to produce the timing required for writing data on tape and its eventual recovery.

4-66. Since $\overline{\emptyset 1}$ and $\overline{\emptyset 2}$ are not provided by the TTC but must be generated from an external source, a recommend clock source is illustrated in figure 4-10.

4-67. READ MODE. Recovery of data is possible in either direction of tape motion. The level $\overline{\text{ANYFWD}}$ will govern tape motion direction.

4-68. Forward Read. Under the assumption that the transport is not busy ($\overline{\text{CMPBSY}}$ is off), when $\overline{\text{ANYFWD}}$ and $\overline{\text{CREAD}}$ go on, $\overline{\text{CMTBSY}}$ goes on approximately four microseconds later and the tape begins

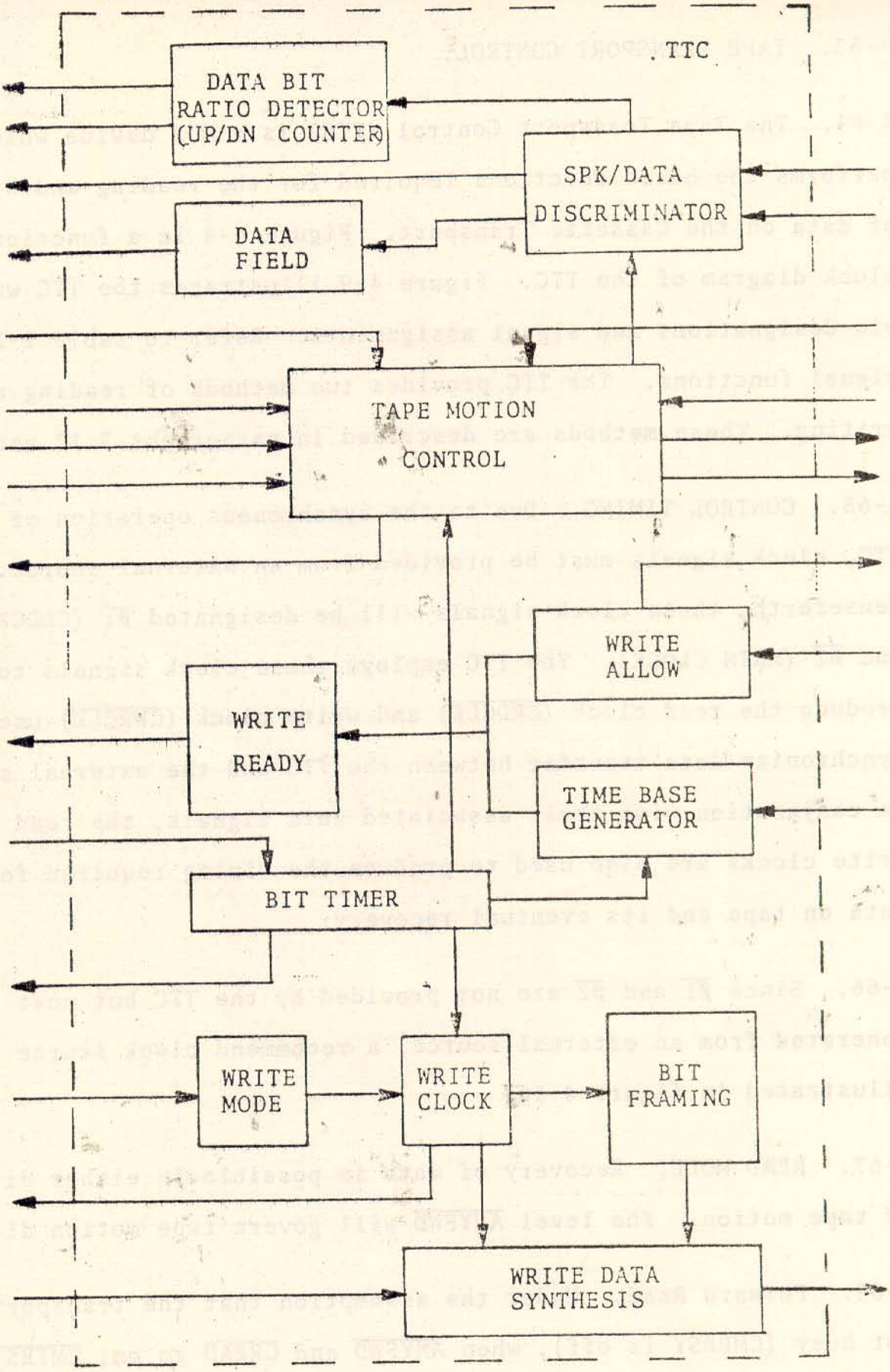


Figure 4-8. Tape Transport Control, Functional Block Diagram.

motion in the forward direction. As soon as data is available to be read, the level, $\overline{\text{CRACTV}}$, is produced to indicate that an active read is being performed. Once a data block has passed the read head, $\overline{\text{CRACTV}}$ terminates indicating the completion of data retrieval. When no other data blocks are to be read, the levels $\overline{\text{ANYFWD}}$ and $\overline{\text{CREAD}}$ should now be terminated. Approximately 15 microseconds afterward, $\overline{\text{CMTBSY}}$ terminates, and the tape motion comes to a halt. The TTC is now ready for new action.

4-69. Reverse Read. Retrieval of data in the reverse direction is accomplished in the same manner as data retrieval in the forward direction except for the initial conditions. In order to read tape in the reverse direction, $\overline{\text{ANYFWD}}$ must be off at all times. This causes the tape to move in a reverse direction when $\overline{\text{CREAD}}$ goes on.

4-70. Data Transfer. Data is recovered from tape in either tape direction. While $\overline{\text{CRACTV}}$ is on, indicating active read, each data bit is recovered from tape and is presented to the output in the form of $\overline{\text{CRDATA}}$. The signal $\overline{\text{CRDCLK}}$ is then gated with $\overline{\text{CRDATA}}$ to produce a serial stream of data. This serial data stream is then transferred by the clock pulse $\overline{\text{Ø1}}$ to the external source. This assures proper data sampling.

4-71. WRITE MODE. Unlike data recovery, data recording may only be accomplished in the forward direction of tape motion.

4-72. Forward Write. When $\overline{\text{ANYFWD}}$ goes on, $\overline{\text{CMTBSY}}$ goes on approximately four microseconds later and the tape begins motion in the forward direction. When the tape is up to speed, $\overline{\text{CØKTWR}}$ goes on

indicating that data may now be recorded on tape.

4-73. Data Transfer. Data bits may now be introduced to the TTC in the form of $\overline{\text{CWDATA}}$. This signal causes $\overline{\text{CWRITE}}$ to be accepted by the TTC. The signal, $\overline{\text{CWRCLK}}$, then clocks one bit of data from $\overline{\text{CWDATA}}$ approximately every 80 microseconds to the external source. The format of data on $\overline{\text{CWDATA}}$ must be such to allow $\overline{\text{CWRCLK}}$ to clock out one bit (whether 0 or 1) approximately every 80 microseconds. The signal $\overline{\text{CWRCLK}}$ is produced as long as $\overline{\text{CWRITE}}$ remains on.

4-74. When the last bit of data is clocked out by $\overline{\text{CWRCLK}}$, the level $\overline{\text{CWRITE}}$ must be terminated no more than 80 microseconds later. This terminates $\overline{\text{CWRCLK}}$ from possibly clocking out any extraneous data which may be present on $\overline{\text{CWDATA}}$. Since the data being recorded on tape is also being read back, $\overline{\text{CRACTV}}$ is on. After the last data block is read, $\overline{\text{CRACTV}}$ terminates. This level should then reset $\overline{\text{ANYFWD}}$. Approximately 15 milliseconds afterward, $\overline{\text{CMTBSY}}$ terminates. and the tape motion comes to a halt.

4-75. TAPE REWINDING. Rewinding of the tape is possible when $\overline{\text{CMTBSY}}$ is off by energizing $\overline{\text{CARWN}}$ or by manually pressing the rewind button on the Cassette Transport. The tape will begin to rewind until the BOT leader on tape is detected. During rewind $\overline{\text{CMTBSY}}$ goes on and remains on until rewinding is completed. At which time, $\overline{\text{CMTBSY}}$ goes off indicating the Cassette Transport is not busy and ready for new action.

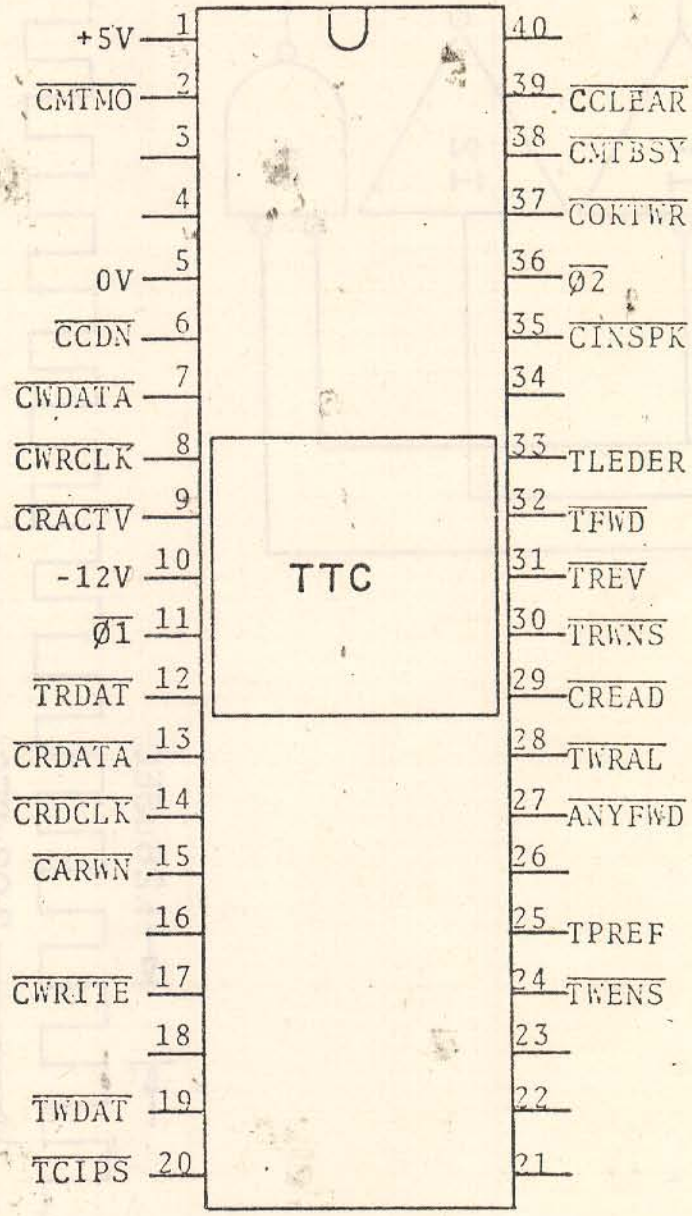


Figure 4-9. Tape Transport Control, Pin Designations.

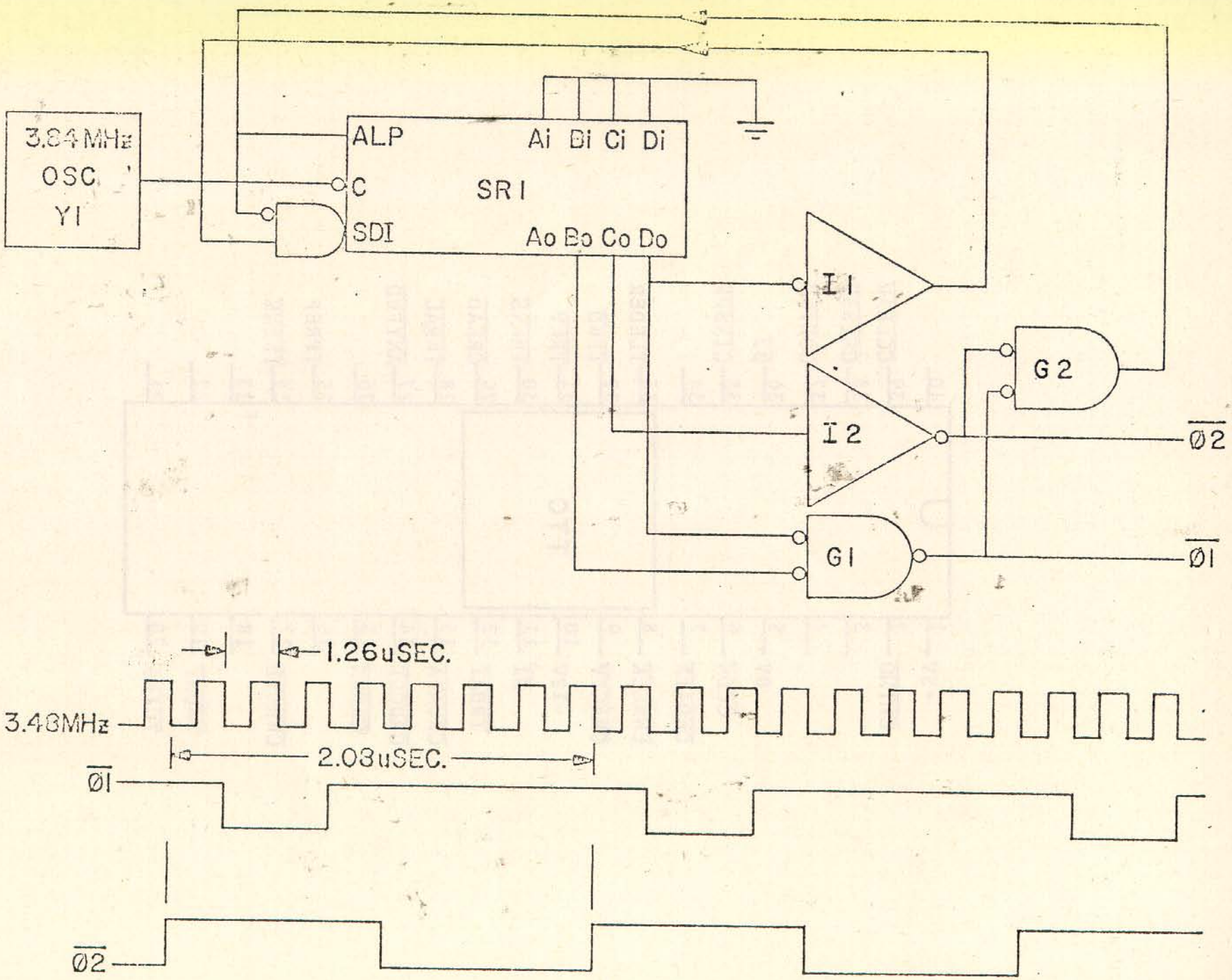


Figure 4-10 TTC Parameter [illegible]

SECTION V. MAINTENANCE

5-1. GENERAL.

5-2. This section contains information required to maintain and fault isolate malfunctions in the Cassette Transport. The maintenance section is divided into four main areas as follows: Preventive Maintenance, Fault Isolation, Removal and Replacement, and Mechanical Alignment.

5-3. Supporting information that is to be used with this section is located in Section VI (Illustrated Parts Breakdown) and Section VII (Reference Drawings).

5-4. PREVENTIVE MAINTENANCE.

5-5. After the Cassette Transport has been properly installed, any irregularities that occur in the performance of the Cassette Transport can be attributed to the failure of a component part. Since the Cassette Transport has been factory adjusted, sealed, and tested, no preventive maintenance is required except for cleaning and lubrication.

5-6. CLEANING. The Magnetic Head and End-Of-Tape (EOT) Block is to be cleaned once a month or as often as required depending on environmental conditions and operation interval.

CAUTION

Component parts on the Front Plate Assembly are made of plastic; it is possible to damage these parts by using incorrect cleaning solvents.

5-7. MAGNETIC HEAD. It is recommended that the Magnetic Head be cleaned with a cleaning solvent such as Isopropyl Alcohol using a cotton swab.

5-8. END-OF-TAPE BLOCK. The above procedure for cleaning the Magnetic Head is also recommended for the End-Of-Tape Block.

5-9. LUBRICATION. The electric Motor located on the Speed Package Assembly requires a few drops of light machine oil in each bearing part once a year.

5-10. FAULT ISOLATION PROCEDURE.

5-11. FAULT ISOLATION. This procedure presents a systematic approach for isolating malfunctions in the Cassette Transport by the use of a Fault Isolation Flow Chart (figure 5-3). In addition, a Voltage/Resistance chart, Signal Waveform chart and an Interconnecting Wiring Block Diagram (figure 5-2), are included to further isolate a malfunction to a printed circuit board, the Tape Local Electronic (TLE) assembly, or discrete component.

5-12. The presentation of material in the maintenance section is in a form that the level of isolating a malfunction may be to an assembly, subassembly, or discrete component. For example, if a malfunction exists on the Tape Local Electronic (TLE) printed circuit board, either the printed circuit board may be replaced or the discrete component causing the malfunction may be replaced. The level of isolation is only limited by the rules set forth by the servicing department.

5-13. TEST EQUIPMENT. Test equipment required to service the cassette transport is listed in table 5-1. All special tools built by

TABLE 5-1. TEST EQUIPMENT REQUIRED

EQUIPMENT	TYPE
DC Power Supply, +24V, 0.75A	Harrison 620313
DC Power Supply, +5V, 3A	Hewlett-Packard 6216A
DC Power Supply, -12V, 0.5A	
Oscilloscope	Tektronix 310A
Multimeter	Triplett 20,000 ohms/volt
Torque Watch	Waters Model 651C-1
Torque Watch	Waters Model 651C-2
Torque Watch	Waters Model 651C-3
Alignment Tool	Redactron No. T-2001W

Redactron have their respective drawings, if applicable, in Section VII. The special tools may be bought through Redactron or fabricated by the customer.

5-14. VOLTAGE/RESISTANCE CHART. Voltage/Resistance readings for isolating malfunctions related to the Tape Local Electronic (TLE) board are located in table 5-2. All readings were made using a 20,000 ohm per volt multimeter. Readings are taken between test point and chassis ground. All input control signals are set to a Logic 1.

5-15. SIGNAL WAVEFORMS. Signal waveforms for isolating a malfunction related to the Tape Local Electronic (TLE) board are located in figure 5-1. Waveforms presented in figure 5-1 are mainly for the Read and Write Channel Circuitry only.

5-16. REMOVAL AND REPLACEMENT PROCEDURE.

5-17. The removal and replacement procedure contains detailed information for the removal and replacement of certain component parts that require special techniques. For removal and replacement of all other components not mentioned herein refer to Illustrated Parts Breakdown, Section VI.

5-18. FRONT BEZEL/DOOR ASSEMBLY.

5-19. Remove Front Bezel/Door Assembly as follows:

a. Open plastic door.

b. Loosen two 1/4-turn Captive Fasteners (figure 6-1, item 2) by turning screwdriver in clockwise direction.

c. Remove Front Bezel/Door Assembly.

d. Replace Front Bezel/Door Assembly in reverse order of removal.

TABLE 5-2. VOLTAGE/RESISTANCE CHART FOR TLE (Cont)

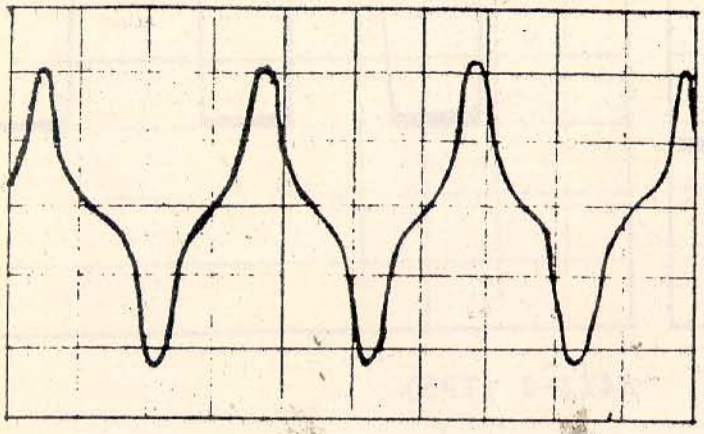
SEMI-CONDUCTOR	DC VOLTAGE*	RESISTANCE**
WRITE CHANNEL CIRCUITRY		
A12Z4-3	+.15V	1.7K
Intersection of R61 & R34	+.25V	300 ohms
Intersection of R34 & R35	+.05V	100 ohms
A13-5	+12V	3.5K
A13-3	+12V	3.5K
A13-8	+4.8V	2.1K
TAPE DRIVE CIRCUITRY		
A11-8	+4.8	2.1K
A11-5	+23V	Inf
A11-3	+23V	Inf

	E	B	C	E	B	C
Q2	OV	.65V	.05V	6K	3.5K	200K

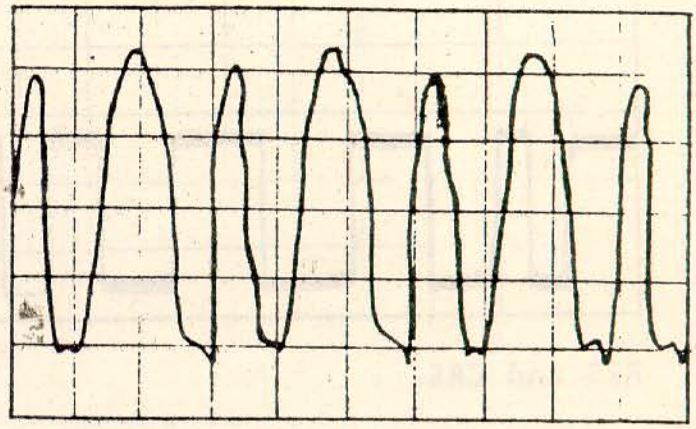
LEADER DETECTOR CIRCUITRY

A1Z2-6

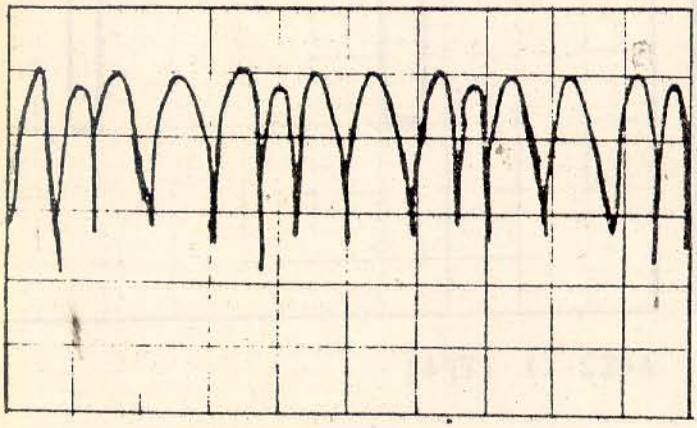
	E	B	C	E	C	C
Q7	-9V	-8V	7V	30K	9K	5K
Q1	OV	.65V	.05V	0 ohms	1.8K	2.8K
Q3	OV	.05V	24V	0 ohms	1.9K	100K
Q4	24V	24V	24V	60K	100K	100K
Q5	24V	24V	24V	inf	75K	100K



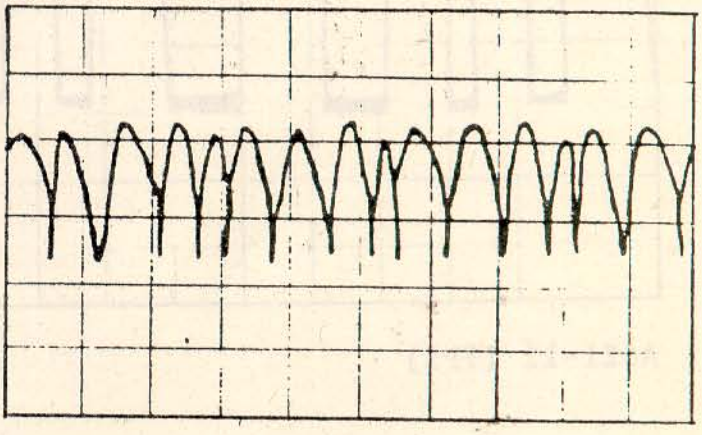
C3 and R5 (TP1)



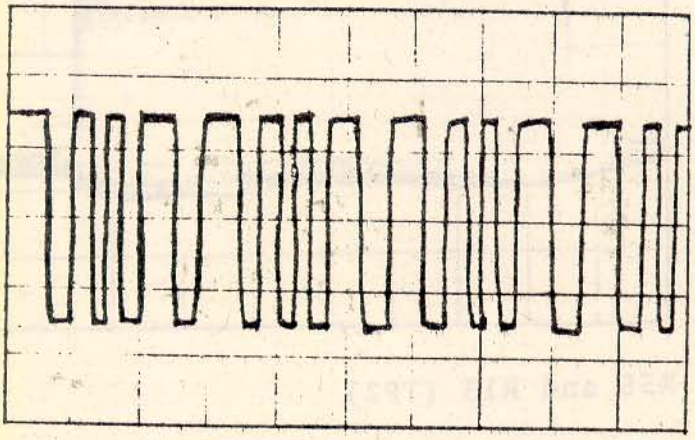
A2Z1-1



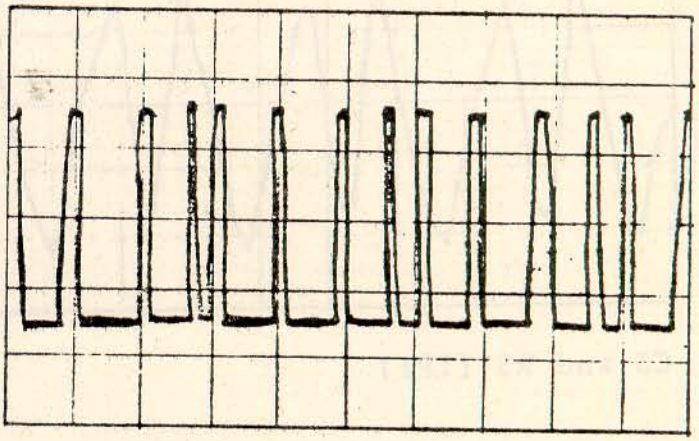
R55 and R13 (TP2)



R56 and C8 (TP5)

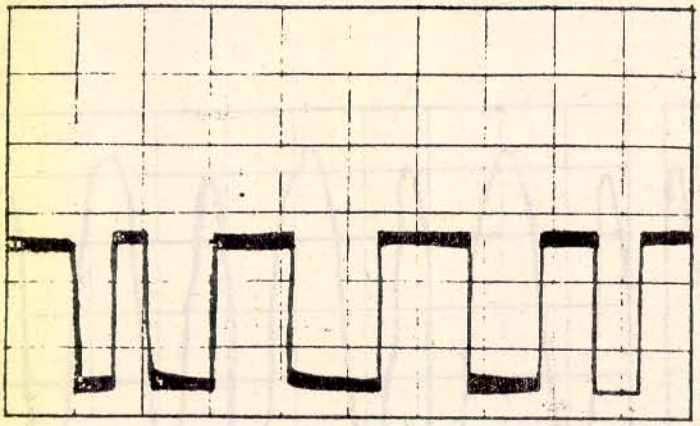


A3Z1-1

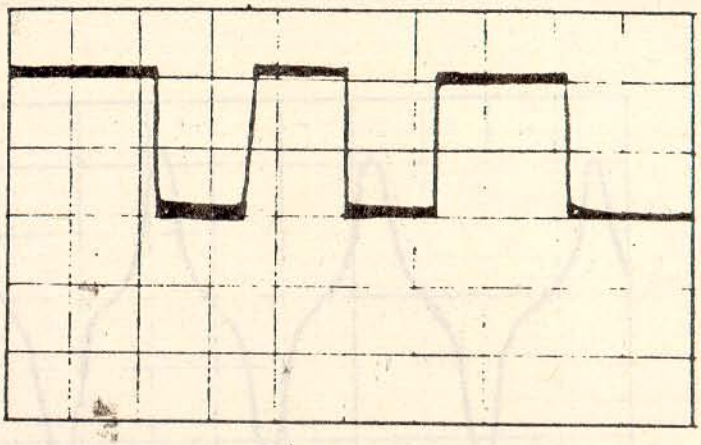


A3Z2-13

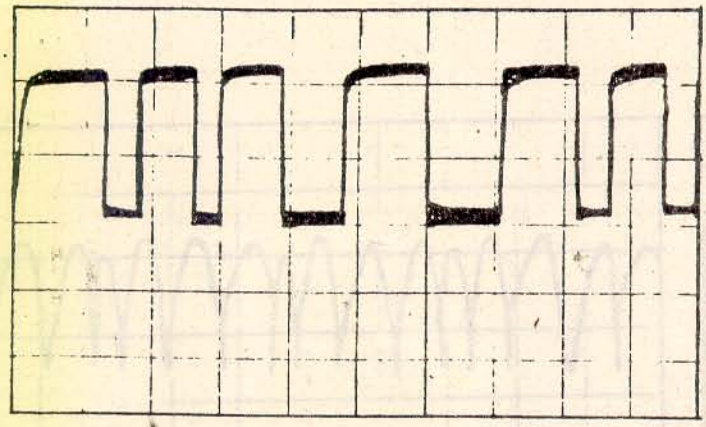
Figure 5-1. Tape Local Electronic (TLE) Waveforms
(Sheet 1 of 2)



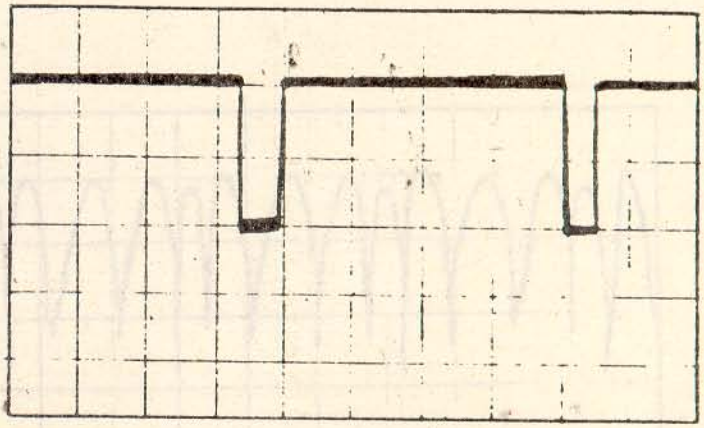
R23 and CR5



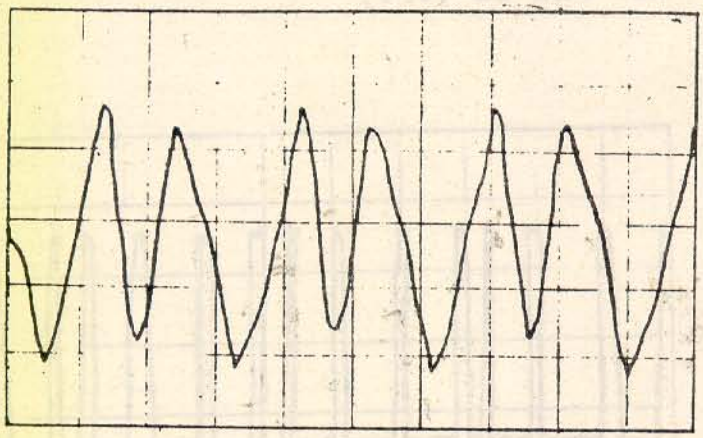
A4Z2-8 (TP3)



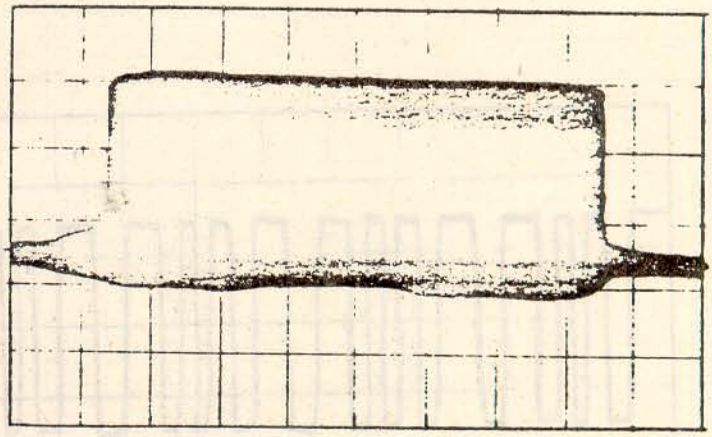
A6Z1-12 (TP5)



A4Z2-11 (TP4)



C3 and R5 (TP1)



R55 and R13 (TP2)

Figure 5-1. Tape Local Electronic (TLE) Waveforms
(Sheet 2 of 2)

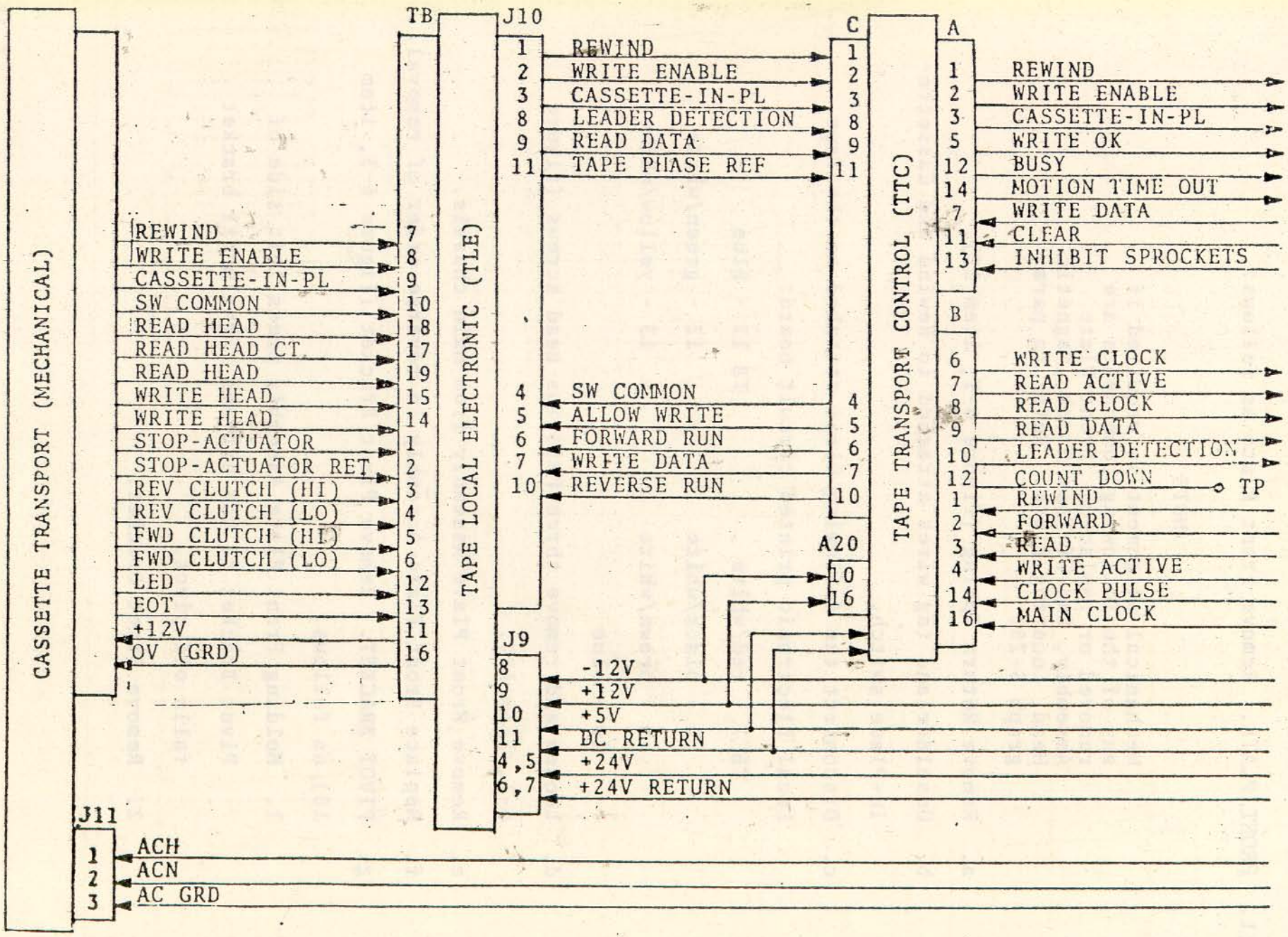


Figure 5-2. Interconnecting Wiring Block Diagram, Cassette Transport

5-20. FRONT PLATE ASSEMBLY

5-21. FRONT PLATE. Remove Front Plate as follows:

NOTE

Mechanical alignment is required if any of the following components are removed or replaced: Front Plate Assembly, End-Of-Tape Block, Magnetic Head, Locating Block. Refer to paragraph 5-26.

a. Remove Return Spring (figure 6-1, item 22).

b. Unsolder and tag wires attached to Rewind and Cassette-In-Place switch.

c. Disconnect the following wires attached to the Tape Local Electronic printed circuit board:

TB 7 - red/white	TB 11 - blue
8 - black/white	12 - green/white
9 - brown/white	13 - yellow/white
10 - blue	

d. Loosen and remove three Phillips head screws (figure 6-1, item 19).

e. Remove Front Plate Assembly from main chassis.

f. Replace Front Plate Assembly in reverse order of removal.

g. PIVOT BRACKET. Remove Pivot Bracket (figure 6-3, item 10) as follows:

1. Holding Front Plate Assembly press left side of Pivot Bracket to the extreme right until bracket falls off pivot.

2. Remove Pivot Bracket.

3. Tag and unsolder wire leads to mechanical switches.

4. Replace component in the reverse order of removal.

5-22. BEARING PLATE ASSEMBLY.

5-23. BEARING PLATE. Remove Bearing Plate Assembly as follows:

NOTE

If any of the following components are removed or replaced mechanical alignment is required refer to paragraph 5-27; Clutch-Spindle Assembly, paragraph 5-37; Brake Shoe Lining, paragraph 5-25.

a. Remove Front Plate Assembly as outlined in paragraph 5-21 Steps a through e.

b. Using two fingers rotate motor-pulley drive. At the same time gently push motor belt to the left until belt slips off pulley.

c. Disconnect the following wires attached to the Tape Local Electronic printed circuit board:

TB 1 - orange/white	TB 5 - white
2 - red	6 - white
3 - white (Blue)	16 - green
4 - white (Blue)	

d. Loosen and remove four Phillips head screws (figure 6-1, item 24).

e. Remove Bearing Plate Assembly from main chassis.

f. Replace Bearing Plate Assembly in reverse order of removal.

5-24. CLUTCH-SPINDLE ASSEMBLY. Remove Clutch-Spindle Assembly as follows:

a. Remove brake bar (figure 6-4, item 6).

b. Remove Pulley (figure 6-4, items 19 and 20) and belt.

c. Loosen and remove three Phillips head screws (figure 6-4, item 22).

d. Remove Clutch-Spindle Assembly.

e. Refer to Clutch-Spindle alignment procedure paragraph 5-37.

f. Replace Clutch-Spindle Assembly in reverse order of removal.

5-25. BRAKE-SHOE LINING. Remove Brake-Shoe Lining as follows:

a. Remove two Phillips head screws on Disc Brake Clapper (figure 6-4, items 12 and 14).

b. Slide Disc Brake Clapper until it is free of inertial disk.

c. Brake-Shoe Linings will fall out with ball bearing.

d. Replace both Brake-Shoe Linings with respective ball bearings.

e. Replace Disc Brake Clapper in reverse order of removal.

5-26. MECHANICAL ALIGNMENT PROCEDURE.

5-27. The mechanical alignment procedure consists of mechanical and electrical adjustment necessary when certain components or assemblies are removed or replaced. This procedure is to be used in conjunction with Removal and Replacement Procedure, paragraph 5-16.

NOTE

In order to maintain a high reliability rate, it is important that the mechanical alignment procedures be accurately followed.

5-28. FRONT PLATE ASSEMBLY.

5-29. FRONT PLATE. Perform Front Plate alignment as follows:

a. Secure Front Plate Assembly to main chassis. Do not tighten the three securing screws to main chassis.

b. Insert Redactron Tool Number T-2001W into cassette locating blocks.

c. Adjust Front Plate Assembly until locating blocks are snug against Redactron Tool.

d. Secure the Front Plate Assembly to main chassis by tightening the three screws.

5-30. END-OF-TAPE BLOCK. The End-Of-Tape (EOT) Block alignment consists of a mechanical and electrical adjustment. Proceed as follows:

a. Mechanical Adjustment.

1. Insert Redactron Tool Number T-2001W into cassette locating blocks.

2. Adjust EOT Block until it is snug against Redactron tool.

3. Secure EOT Block to Front Plate Assembly.

b. Electrical Adjustment (EOT Threshold Adjust).

1. Apply full power to the Cassette Transport.

2. Insert tape cassette in Cassette Transport.

3. Allow tape to run until leader (EOT) is not reflecting light into photo diode sensor.

4. On Tape Local Electronic board connect multimeter between TP8 and ground.

5. Adjust potentiometer R40 for -2.0 Vdc.

6. Return tape leader to End-Of-Tape position.

7. Observe that multimeter indicates +6 Vdc or greater.

5-31. MAGNETIC HEAD. Perform Magnetic Head electrical adjustment as follows:

NOTE

The Magnetic Head is mechanically adjusted and sealed at the factory and is NOT to be adjusted in the field. If Magnetic Head needs replacing, return Front Plate Assembly to factory.

a. Electrical Adjustment.

1. Place Cassette Transport in read mode.

2. Connect oscilloscope leads between TP2 (see schematic diagram) and ground.

3. Adjust oscilloscope control for a waveform presentation as in figure 5-1 (TP2).

4. Observe oscilloscope and adjust R5 for maximum amplitude without flattening the peaks of the waveforms.

5. Amplitude should be between 3 and 4 volts.

5-32. TOP-STOP, CASSETTE. Perform Cassette Top-Stop alignment as follows:

a. Insert Redactron Tool Number T2001W into cassette locating blocks.

b. Loosen Top-Stop screw (figure 6-3, items 18 and 19).

c. Position Top-Stop so that a snug fit (behind and on top) exists between it and Redactron tool.

d. Tighten Top-Stop screw.

5-33. WRITE ALLOW SWITCH. Perform Write Allow Switch adjustment as follows:

a. Insert Redactron Tool Number T-2001W into cassette locating blocks.

b. Loosen two screws holding switch to Pivot Bracket (figure 6-3, items 5, 6 and 7).

c. Push switch downward, allowing switch to touch top of Redactron tool until an audible click is heard.

d. Tighten two screws holding switch to Pivot Bracket.

5-34. CASSETTE-IN-PLACE SWITCH. Adjustment procedure is the same as in paragraph 5-33.

5-35. BEARING PLATE ASSEMBLY.

5-36. BEARING PLATE. Mount Bearing Plate as follows:

a. Mount Bearing Plate to main chassis. Do not tighten screws.

b. Push Bearing Plate to the left and in an upward direction so that all slack is taken up.

c. Tighten screws.

5-37. CLUTCH-SPINDLE. Perform the Clutch-Spindle alignment as follows:

NOTE

Before performing alignment procedure check that one Clutch-Spindle Assembly is tightly secured to Bearing Plate.

a. Mount Clutch-Spindle Assembly, that is being replaced, to Bearing Plate. Do not tighten the three mounting screws.

b. Position the Redactron alignment tool over both spindles. Tighten the three screws that hold the Clutch-Spindle Assembly to the Bearing Plate.

c. Remove the alignment tool. This tool must be removed and replaced several times to ensure perfect alignment between spindle centers.

d. If need be, loosen the three mounting screws and shift position of Clutch-Spindle Assembly for a smooth on-off movement of the alignment tool.

e. Tighten mounting screws and repeat step c.

5-38. PULLEY-BELT SYSTEM. Perform Pulley-Belt adjustment as follows:

a. Loosen idler pulley screw on Bearing Plate (figure 6-4 item 30).

b. Loosen Speed Package Assembly mounting screws and remove motor drive belt.

c. Mount Bearing Plate drive belt over pulleys as shown in diagram below.

d. Adjust idler pulley for maximum belt wrap-around of reverse pulley.

e. Performing step d results in dimension "A" to be approximately 3/16 inches.

f. Tighten idler pulley screw in step a.

g. Using a spring scale, deflect the center of the longest span to 3/16 inches. The scale must indicate 2-3 lbs. of tension.

h. Check that belt is approximately centered on both left and right pulley (i.e., belt is not hanging over edge of pulley).

i. Place motor belt on its respective pulleys.

j. Slide motor mounting to take up motor belt slack.

k. Tighten mounting screws on Speed Package Assembly.

l. Repeat Step g.

m. Energize motor and observe that both belts do not creep off pulley or overlap edge of pulley.

5-39. STOP-ACTUATOR. Perform Stop-Actuator (Brake) alignment as follows:

a. Loosen two screws located on Disc Brake Bracket (figure 6-4, items 13 and 14).

b. Push spindle assembly to the rear until all slack is taken up.

c. Insert feeler gauge with a $0.003\ ^{+0.002}_{-0.001}$ thickness between outer brake shoe lining and inertia disc.

d. Slide disc bracket until all slack is taken up between inertia disc and brake shoe lining.

e. Tighten both screws on Disc Brake Bracket.

f. Repeat steps a through e for other Disc Brake Bracket.

g. Start motor running and actuate brake.

h. Back off both adjusting screws (figure 6-4, item 5) until they clear the movable Disc Brake Clapper (figure 6-4, item 12).

i. Observe that brake bar (figure 6-4, item 6) is parallel to top surface of Disc Brake Bracket.

j. If necessary, readjust Disc Brake Bracket.

k. Alternately adjust the two adjusting screws until both inertial discs just stop turning.

l. Continue adjusting both adjusting screws equally until a $0.005\ ^{+0.002}_{-0.001}$ gap exists between actuator (solenoid coil) and solenoid clapper.

5-40. CLUTCH TORQUE TEST.

5-41. Three torque tests are required for the Clutch-Spindle Assembly. They are outlined below.

5-42. CLUTCH-STALL TORQUE. Perform Clutch Stall Torque test as follows:

a. Connect torque watch to Forward Spindle.

b. Apply AC and DC power to Cassette Transport.

c. Energize Forward Clutch-Spindle Assembly by applying FWD RUN signal (Logic 0).

d. Observe that when spindle starts to stall, the torque watch must indicate between 35 and 45 inch/ounces.

e. Repeat steps a through d for Reverse Spindle, except apply REV RUN signal in step c.

5-43. RESIDUAL TORQUE. Perform Residual Torque test as follows:

a. Turn all power to Cassette Transport to OFF position.

b. Connect torque watch to Forward Spindle.

c. Turn torque watch until Forward Spindle just begins to turn.

d. The torque watch must indicate less than 0.25 inch/ounces.

e. Repeat steps a through c for Reverse Spindle.

5-44. MANUAL TORQUE. Perform Manual Torque test as follows:

a. De-energize Forward, and Reverse Clutch-Spindle Assemblies.

b. Observe that Brake is energized.

c. Turn Forward Spindle by hand.

d. Observe that Forward Inertia Disc does not turn.

e. Repeat steps b through d for Reverse Spindle and Inertia Disc.

5-45. SPINDLE SLIP TORQUE. Perform Spindle Slip Torque test as follows:

a. De-energize Forward, and Reverse Clutch-Spindle Assemblies.

b. Observe that Brake is energized.

c. Connect torque watch to Forward Spindle.

d. Observe Spindle and turn torque watch until Spindle just begins to turn (slip).

e. Torque watch must indicate between 0.75 and 1.5 inch/ounces.

f. Repeat steps a through e in reverse direction.

g. Repeat steps d through f for Reverse Spindle.

VISUAL CHECK
Power Off

(Cassette Removed)

G

1. Inspect Transport for damaged wires or parts.
2. Repair damaged wires.
3. Replace damaged parts as per par 5-16

G

1. Rotate FWD, & REV Clutch-Spindle by hand.
2. Observe that Clutch-Spindles rotate smoothly.
3. Check Brake Shoe Lining.

G

NG

1. Replace Clutch-Spindle Assy as per par 5-24.
2. Replace Brake Shoe Lining per par 5-25.

G

1. Check motor drive belt tension.
2. Check Bearing Plate Pulley-Belt for max. wrap around.

G

NG

1. Perform belt adjustment as per par 5-38.

G

INITIAL CHECK
Power on

(Cassette Removed)

G

1. Apply AC & DC pwr to Cassette Transport
2. Set TFWD & TREV to Logic 1.
3. Check AC & DC voltages as per table 2-1.

NG

1. Check external voltage source & related wires.
2. Refer to fig 5-2.

G

1. Observe motor is running.
2. Observe that inertia disks are not turning

G

NG

1. Check TLE PC board refer to par 4-28.
2. Check mechanical adjustment as per par 5-39.

GG

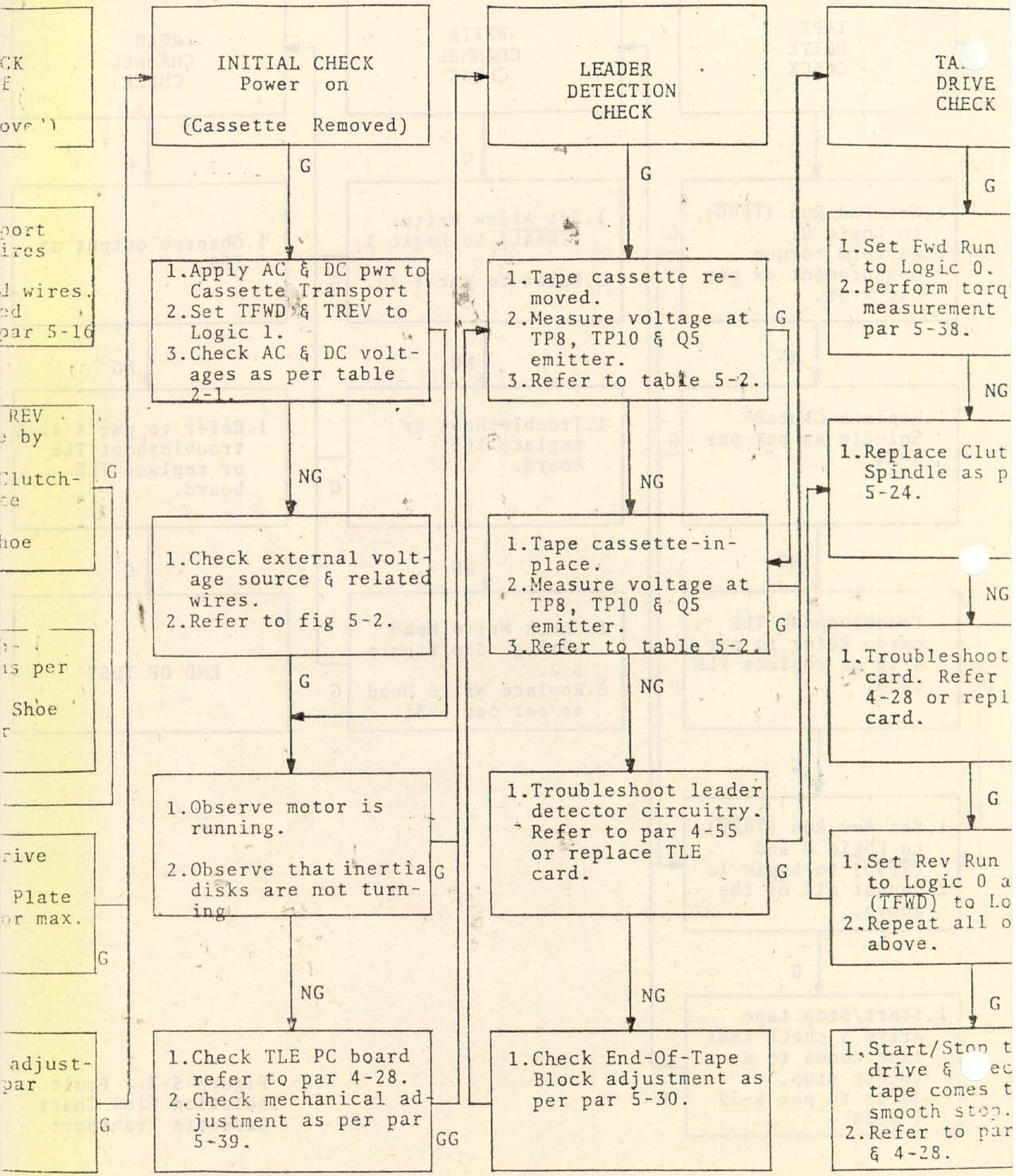
LEAI
DETEC
CHE

1. Tape cas moved.
2. Measure TP8, TP1 emitter.
3. Refer tc

1. Tape cas place.
2. Measure TP8, TP1 emitter.
3. Refer to

1. Troubles detector Refer to or repla card.

1. Check En Block ad per par


INITIAL CHECK
Power on
(Cassette Removed)
G
1.Apply AC & DC pwr to Cassette Transport
2.Set TFWD & TREV to Logic 1.
3.Check AC & DC voltages as per table 2-1.
NG
1.Check external voltage source & related wires.
2.Refer to fig 5-2.
G
1.Observe motor is running.
2.Observe that inertia disks are not turning
G
NG
1.Check TLE PC board refer to par 4-28.
2.Check mechanical adjustment as per par 5-39.
GG
LEADER DETECTION CHECK
G
1.Tape cassette removed.
2.Measure voltage at TP8, TP10 & Q5 emitter.
3.Refer to table 5-2.
G
NG
1.Tape cassette-in-place.
2.Measure voltage at TP8, TP10 & Q5 emitter.
3.Refer to table 5-2.
G
NG
1.Troubleshoot leader detector circuitry. Refer to par 4-55 or replace TLE card.
G
NG
1.Check End-Of-Tape Block adjustment as per par 5-30.
TA
DRIVE
CHECK
G
1.Set Fwd Run to Logic 0.
2.Perform torq measurement par 5-38.
NG
1.Replace Clut Spindle as p 5-24.
NG
1.Troubleshoot card. Refer 4-28 or repl card.
G
1.Set Rev Run to Logic 0 a (TFWD) to Lo
2.Repeat all o above.
G
1.Start/Stop t drive & ec tape comes t smooth stop.
2.Refer to par & 4-28.

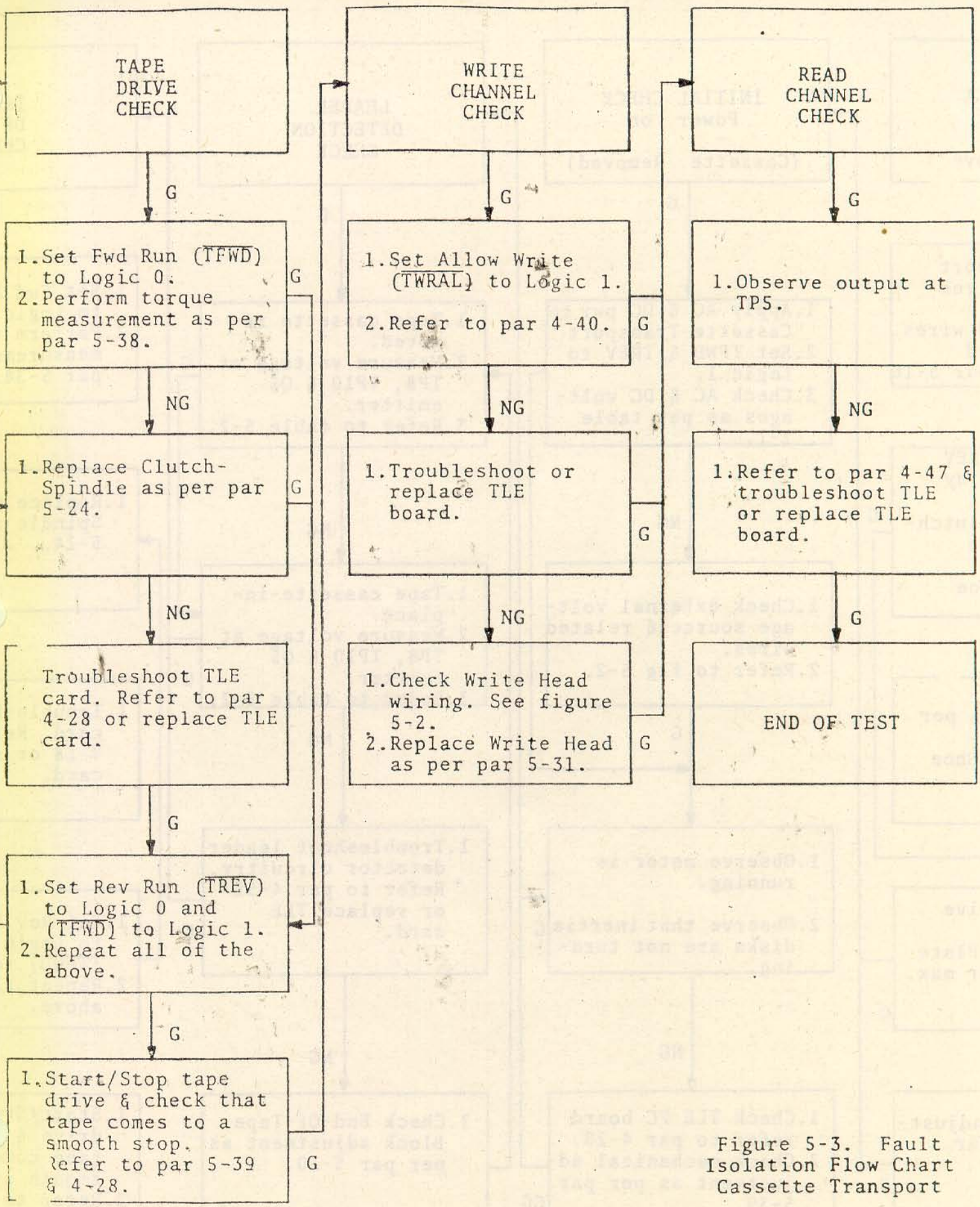


Figure 5-3. Fault Isolation Flow Chart Cassette Transport

SECTION VI. ILLUSTRATED PARTS BREAKDOWN

6-1. GENERAL.

6-2. This section illustrates and lists component parts pertaining to the Magnetic Tape Cassette Transport Model 100.

6-3. PURPOSE. The Illustrated Parts Breakdown is used as follows: locate component parts, locate component parts for order of disassembly for maintenance purposes, cross-reference component parts to Redactron part numbers. Also, a manufacturer's list is provided in table 6-1.

6-4. FIGURE AND INDEX NUMBER. The index number on the figure (illustration) provides a cross-reference between component parts on the figure and the figure and Index Number column.

6-5. PART NUMBER. For each index number there is an associated parts number. This part number is a Redactron part number and is to be used when ordering parts.

6-6. DESCRIPTION. This column provides a description of each component part. All component parts are listed in order of disassembly with the exception of attaching parts. Attaching parts are preceded by notation "ATTACHING PARTS" and finish when last attaching parts are followed by symbol "_ _ _ * _ _ _".

6-7. UNITS PER ASSEMBLY. This column indicates the quantity of component part(s) required for the assembly or subassembly in which that part appears. The notation "NP" indicates that the part is non-procurable. The notation "A/R" indicates "as required".

6-8. USABLE ON CODE. An alphanumeric code is used in this column to indicate, when applicable, the interchangeability of component parts for similar assemblies.

TABLE 6-1. MANUFACTURER'S LIST

CODE	MANUFACTURER	ADDRESS
	Amperex Electronic Corp.	Hauppauge, New York, 11787
	Augat Inc.	Attleboro, Mass., 02703
	Barden/NMB	Manhasset, New York, 11030
	Centrolab Div. of Globe Union Inc.	Milwaukee, Wisconsin, 53201
	Erie County Plastic Corp.	Corry, Penna., 16407
	General Electric Corp.	Schenactady, New York, 12305
	General Time Corp.	Torrington, Conn., 06790
	H. H. Smith	Brooklyn, New York, 11207
	Motorola Semiconductor Productions Inc.	Phoenix, Arizona, 85036
	Palnut	Mountanside, New Jersey, 07092
	PIC Design	Ridgefield, Conn., 06877
	Radio Corporation of America	New York, New York, 10020
	Richloek Corp.	Chicago, Illinois, 60646
	Simmonds Fastener	Albany, New York, 12201
	Sprague Electric Co.	North Adams, Mass., 01247
	Standard Press Steel	Jenkintown, Penna., 19046
	Thermalloy Co.	Dallas, Texas, 75247
	Waldes Kohinoor Inc.	Long Island City, N.Y. 11101

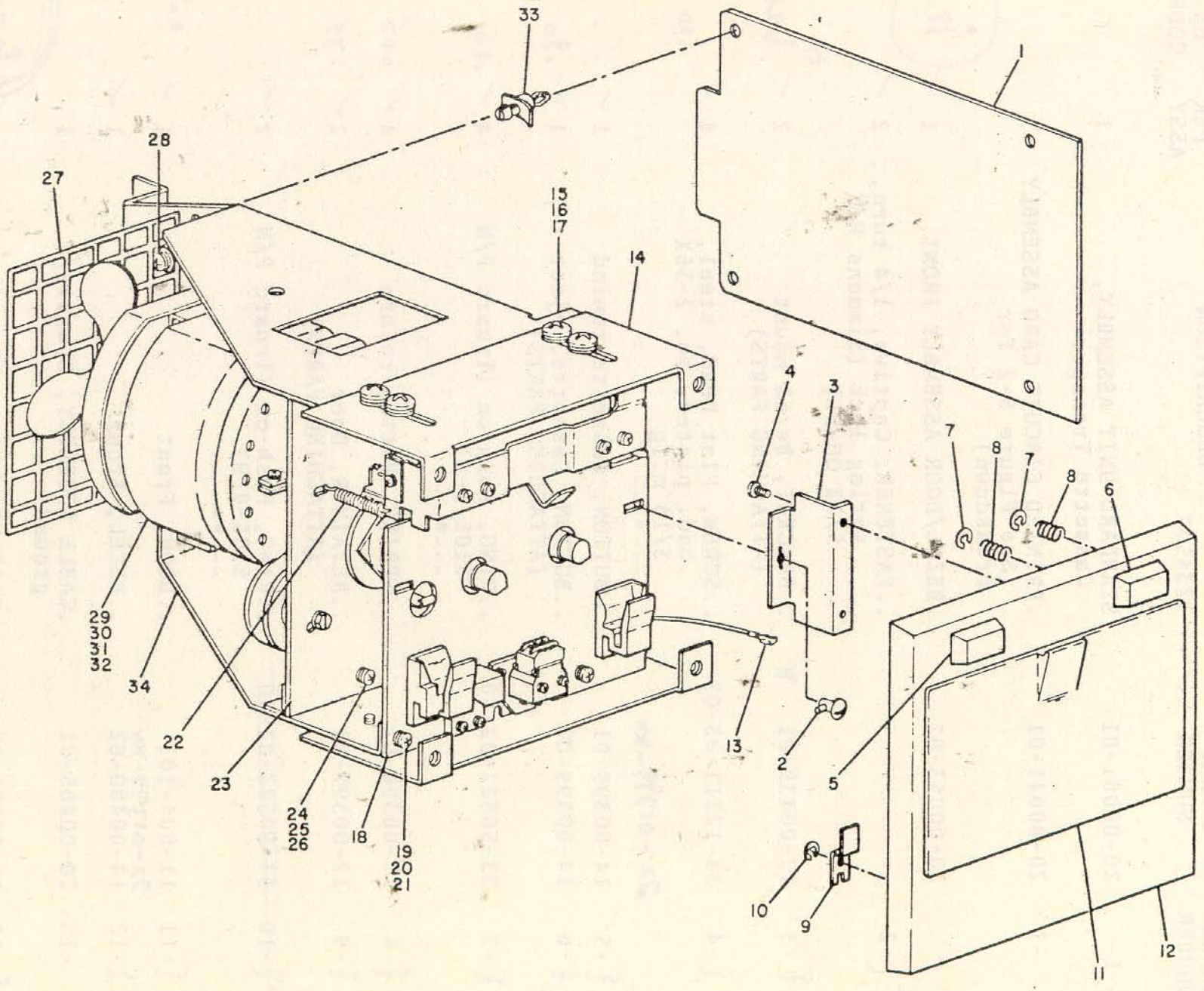


Figure 6-1. Magnetic Tape Cassette Transport, Model 100

FIG & INDEX NUMBER	REDACTRON PART NUMBER	DESCRIPTION 1234567	UNITS PER ASSY	USABLE ON CODE
6-1-	20-00001-01	STANDARD UNIT ASSEMBLY, Cassette Transport	1	
-1	20-00041-01	.PRINTED CIRCUIT CARD ASSEMBLY (See Figure 6-2 for breakdown)	1	
1 {	20-00053-02	.BEZEL/DOOR ASSEMBLY FRONT	1 ✓	18.85
1 { -2		..FASTENER, Captive, 1/4 turn, spring lock (Simmons P/N 5/32 OH-SL)	2 ✓	
2 { -3	12-00439-01 ¥	..BRACKET, Bezel mount (ATTACHING PARTS)	2 ✓	1.20
4 { -4	33-12211-03-03	..SCREW, Flat head, steel, cad. plated, No. 2-56X 3/16 m.lg	4 ✓	.10
	22-01379-xx	---*---		
1 { -5	14-00399-01	..BUTTON, Cassette rewind	1 ✓	
1 { -6	14-00399-02	..BUTTON, Cassette, eject (ATTACHING PARTS)	1 ✓	.80
2 { -7	33-50522-02-00	..RING, Push-on (Truarc P/N 5105-9-H)	4 ✓	.10
		---*---		
2 { -8	13-00398-01	..SPRING, Button return	4 ✓	1.05
1 { -9	12-00397-01	..RETAINER, Door (ATTACHING PARTS)	2 ✓	.35
~~1 { -10~~	~~33-50522-02-00~~	..RING, Push-on (Truarc P/N 5105-9-H)	2 ✓	
		---*---		
1 { -11	11-004-101	..DOOR, Front	1 ✓	metals
	22-01374-xx			
1 { -12	14-00400-02	..BEZEL, Front	1 ✓	
-13	20-00465-01	.CABLE ASSEMBLY, Chassis/ ground	1	
2 { -14	12-00050-01	.BRACKET, Adjustable	2 ✓	2.70 ≠
-15	33-15211-14-06	..SCREW, Phillips recess truss head, steel cad plated, No. 8-32 X 3/8 in lg	8	

FIG & INDEX NUMBER	REDACTRON PART NUMBER	DESCRIPTION 1234567	UNITS PER ASSY	USABLE ON CODE
6-1-16	33-32011-14-00	..WASHER,Lock,ext.tooth,steel, cad. plated No. 8	8	
-17	33-31011-14-00	..WASHER,Flat,steel,cad, plated No. 8	8	
-18	20-00003-01	.PLATE ASSEMBLY, Front (See figure 6-3 for breakdown) (ATTACHING PARTS)	1	
-19	33-11111-12-05	.SCREW,Phillips recess pan head, steel, cad. plated, No.6-32 X 5/16 in. lg	3	
-20	33-32011-12-00	.WASHER,Lock,ext tooth, steel, cad. plated, No. 6	3	
-21	33-31011-12-00	.WASHER,Flat,steel,cad. plated, No. 6 ---*---	3	
-22	13-00048-01	.SPRING, Return, pivot bracket	1	
-23	20-00016-01	.PLATE ASSEMBLY, Bearing (See figure 6-4 for breakdown) (ATTACHING PARTS)	1	
-24	33-11111-12-05	.SCREW,Phillips recess pan head, steel, cad. plated, No. 6-32 X 5/16 in. lg	4	
-25	33-32011-12-00	.WASHER,Lock,ext tooth,steel, cad. plated, No. 6	4	
-26	33-31011-12-00	.WASHER,Flat,steel,cad. plated, No. 6 ---*---	4	
-27	13-00533-01	.GUARD, Fan (ATTACHING PARTS)	1	
-28	33-11111-12-03	.SCREW,Phillips recess pan head, steel, cad. plated, No. 6-32 X 3/16 in. lg ---*---	2	

FIG & INDEX NUMBER	REDACTRON PART NUMBER	DESCRIPTION 1234567	UNITS PER ASSY	USABLE ON CODE
6-1-29	20-00034-01	.SPEED PACKAGE ASSEMBLY (See figure 6-5 for breakdown) (ATTACHING PARTS)	1	
-30	33-14211-17-08	.SCREW, slotted hexagon head, steel, cad. plated. No. 10-32 X 1/2 in. lg	4	
-31	33-32011-17-00	.WASHER, Lock, ext. tooth, steel, cad. plated, No. 10	4	
-32	33-31011-17-00	.WASHER, Flat, steel, cad. plated, No. 10	4	
		---*---		
-33	31-41001-22-00	.TERMINAL, standoff (Richlok Corp. P/N CBS-4R)	4	
-34	12-00002-01	.CHASSIS, Cassette	1	

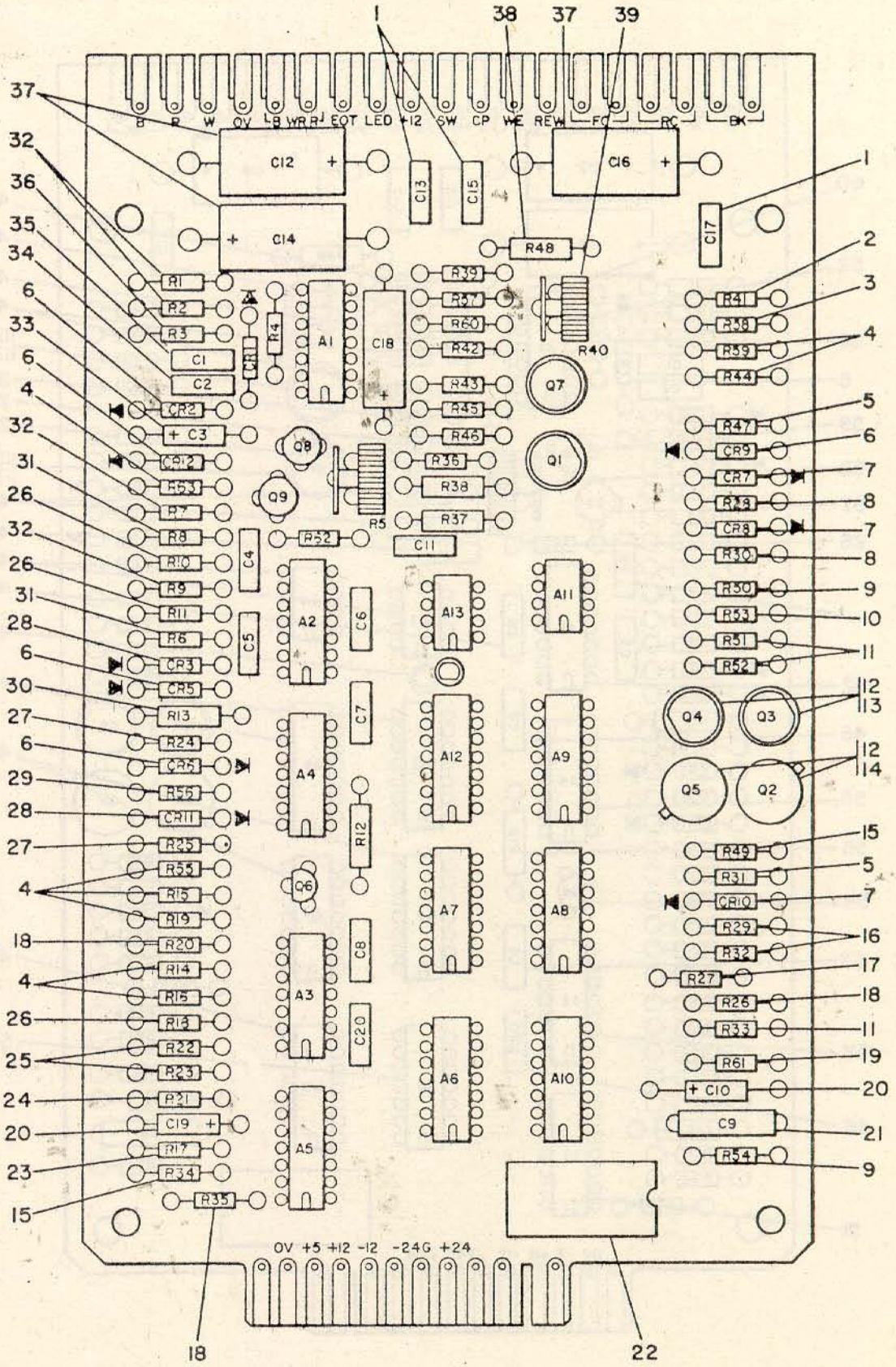


Figure 6-2. Tape Local Electronic, PC Card (Sheet 1 of 2)

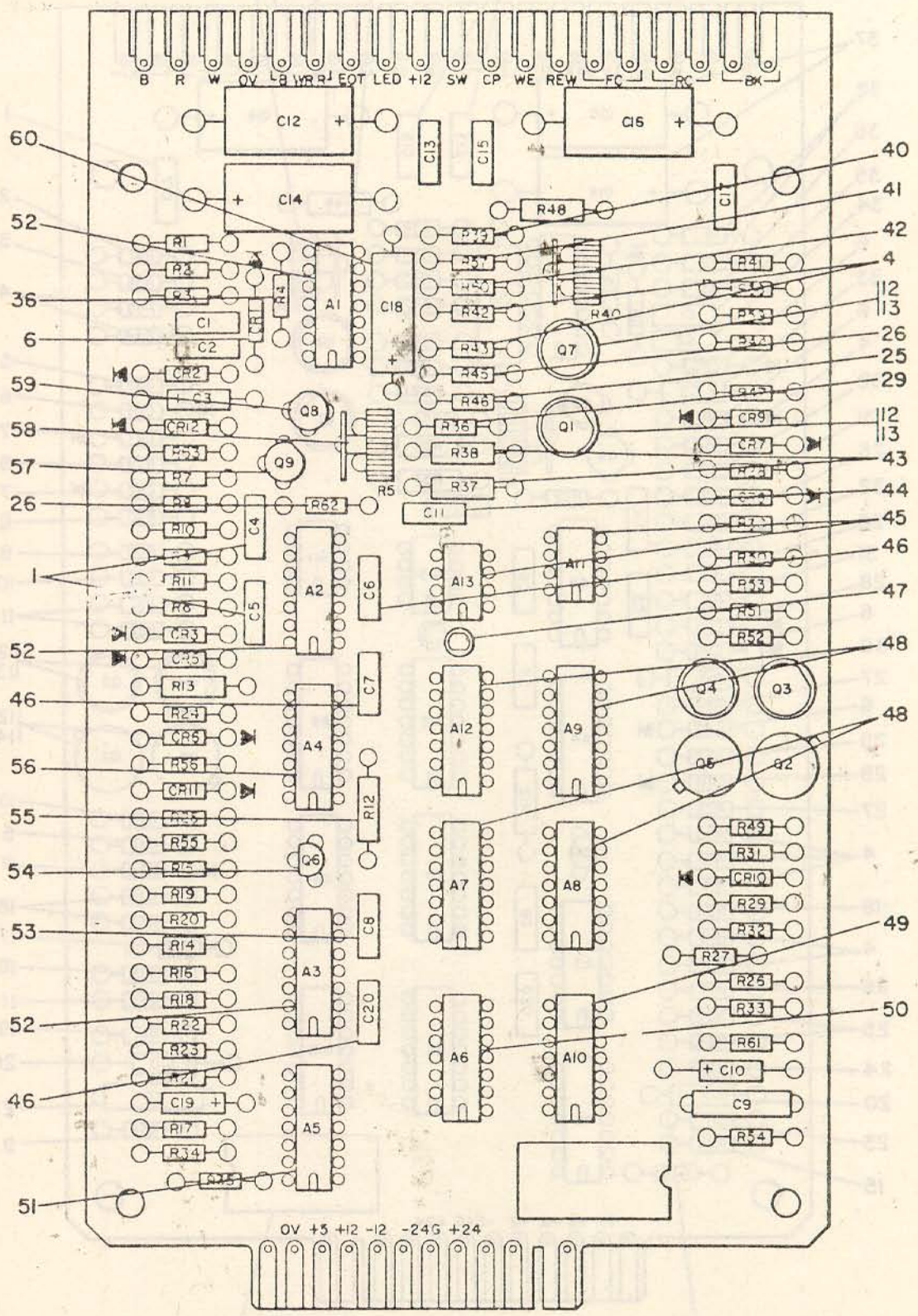


Figure 6-2. Tape Local Electronic, PC Card (Sheet 2 of 2)

FIG & INDEX NUMBER	REDACTRON PART NUMBER	DESCRIPTION 1234567	UNITS PER ASSY	USABLE ON CODE
6-2-	20-00041-01	PRINTED, Circuit card Assembly (See figure 6-1-1 for next higher assembly)	Ref	
-1		.CAPACITOR, Fixed, ceramic, disc, 0.01uf (Sprague P/N C023B101F103M)	5	
-2	37-12204-21	.RESISTOR, Fixed, 200k, 1/4w, ±5%	1	
-3	37-12682-21	.RESISTOR,Fixed,6.8K,1/4w,±5%	1	
-4	37-12103-21	.RESISTOR,Fixed,10K,1/4w,±5%	10	
-5	37-12681-21	.RESISTOR,Fixed,680ohms,1/4w, ±5%	2	
-6	36-30002-01	.SEMICONDUCTOR DEVICE,DIODE (IN281)	6	
-7	36-30003-01	.SEMICONDUCTOR,DEVICE,Diode (IN2069A)	3	
-8	37-12470-21	.RESISTOR,Fixed,47ohms,1/4w, ±5%	2	
-9	37-12302-21	.RESISTOR,Fixed,3K,1/4w,±5%	2	
-10	37-12683-21	.RESISTOR,Fixed,68K,1/4w,±5%	1	
-11	37-12242-21	.RESISTOR,Fixed,2.4K,1/4w,±5%	3	
-12		.SPACER,Transistor (Thermolloy P/N 7717-86N-WHITE)	6	
-13	36-10003-01	.TRANSISTOR (2N3566)	4	
-14	36-10002-01	.TRANSISTOR (2N3053)	2	
-15	37-12201-21	.RESISTOR,Fixed,200 ohms,1/4w, ±5%	2	
-16	37-12331-21	.RESISTOR,Fixed,330 ohms,1/4w, ±5%	2	
-17	37-12752-21	.RESISTOR,Fixed,7.5k,1/4w,±5%	1	
-18	37-12101-21	.RESISTOR,Fixed,100 ohms,1/4w, ±5%	3	
-19	37-12122-21	.RESISTOR,Fixed,1.2K,1/4w,±5%	1	

FIG & INDEX NUMBER	REDACTRON PART NUMBER	DESCRIPTION 1234567	UNITS PER ASSY	USABLE ON CODE
6-2-20		.CAPACITOR,Fixed,tantalum, 1 uf, 35v (Sprague P/N 150D105X9035A2)	2	
-21		.CAPACITOR,Fixed,ceramic,disc, 0.22 uf (AMP P/N C280AE/ P220K)	1	
-22	30-30001-01	.SOCKET,1c,16 pin (Augat P/N 516-AGID)	1	
-23	37-12152-21	.RESISTOR,Fixed,1.5K,1/4w,±5%	1	
-24	37-12563-21	.RESISTOR,Fixed,56K,1/4w,±5%	1	
-25	37-12223-21	.RESISTOR,Fixed,22K,1/4w,±5%	3	
-26	37-12104-21	.RESISTOR,Fixed,100K,1/4w,±5%	5	
-27	37-12471-21	.RESISTOR,Fixed,470 ohms, 1/4w, ±5%	2	
-28	36-30001-01	.SEMICONDUCTOR,DEVICE,Diode (IN914)	2	
-29	37-12102-21	.RESITOR,Fixed,1K,1/4w,±5%	2	
-30	37-12102-21	.RESITOR,Fixed,1K,1/2w,±5%	1	
-31	37-12472-21	.RESISTOR,Fixed,4.7K,1/4w,±5%	2	
-32	37-12512-21	.RESISTOR,Fixed,5.1K,1/4w,±5%	4	
-33		.CAPACITOR,Fixed,electrolytic, 6.4uf CAMP P/N C426AR/F6.4	1	
-34		.CAPACITOR,Fixed,ceramic,disc, 10pf (Centralab P/N DD100)	1	
-35		.CAPACITOR,Fixed,ceramic,disc, 0.001uf (Centralab P/NDD102)	1	
-36	37-12514-21	.RESISTOR,Fixed,510K,1/4w,±5%	2	
-37		.CAPACITOR,Fixed,electrolytic, 50uf (AMP P/N C426AR/G50)	3	
-38	37-13221-21	.RESISTOR,Fixed,220 ohms,1/2w, ±5%	1	

FIG & INDEX NUMBER	REDACTRON PART NUMBER	DESCRIPTION 1234567	UNITS PER ASSY	USABLE ON CODE
6-2-39	37-80005-01	.RESISTOR,Variable,470K (AMP P/N E086BC/470KW)	1	
-40	37-12153-21	.RESISTOR,Fixed,15K,1/4w,±5%	1	
-41	37-12473-21	.RESISTOR,Fixed,47K,1/4w,±5%	1	
-42	37-12244-21	.RESISTOR,Fixed,240K,1/4w,±5%	1	
-43	37-13621-21	.RESISTOR,Fixed,620 ohms,1/2w, ±5%	2	
-44		.CAPACITOR,Fixed,ceramic,disc, 0.005uf (Sprague P/N CO23B101E502M)	1	
-45	36-40005-01	.INTEGRATED Circuit (Motorola) P/N SN75451P)	2	
-46		.CAPACITOR,Fixed,ceramic,disc 25 pf (Centralab P/NDD250)	3	
-47	11-00478-01	.SUPPORT,P.C.Card	1	
-48	36-40001-01	.INTEGRATED circuit (Motorola P/N SN7400N	4	
-49	36-40002-01	.INTEGRATED circuit (Motorola P/N SN74121N)	1	
-50	36-40004-01	.INTEGRATED Circuit (Motorola P/N SN7404N)	1	
-51	36-40003-01	.INTEGRATED circuit (Motorola P/N SN74107N)	1	
-52	36-40006-01	.INTEGRATED circuit (Motorola P/N MC1303L)	3	
-53		.CAPACITOR,Fixed,ceramic,disc, 250 pf (Centralab P/N DD251)	1	
-54	36-10007-01	.TRANSISTOR (Motorola P/N PS-A13)	1	
-55	37-13201-21	.RESISTOR,Fixed,200 ohms, 1/2w, ±5%	1	
-56	36-40007-01	.INTEGRATED circuit (RCA P/N CA3046)	1	

FIG & INDEX NUMBER	REDACTRON PART NUMBER	1234567 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
6-2-57		.TRANSISTOR (2N3565)	1	
-58	37-80003-01	.RESISTOR,Variable,4.7K (AMP P/N E086BC/4K7W)	1	
-59		.TRANSISTOR (2N4249)	1	
-60		.CAPACITOR,Fixed,electrolytic, 1uf, 40v (AMP P/N C426AR/ G1)	1	

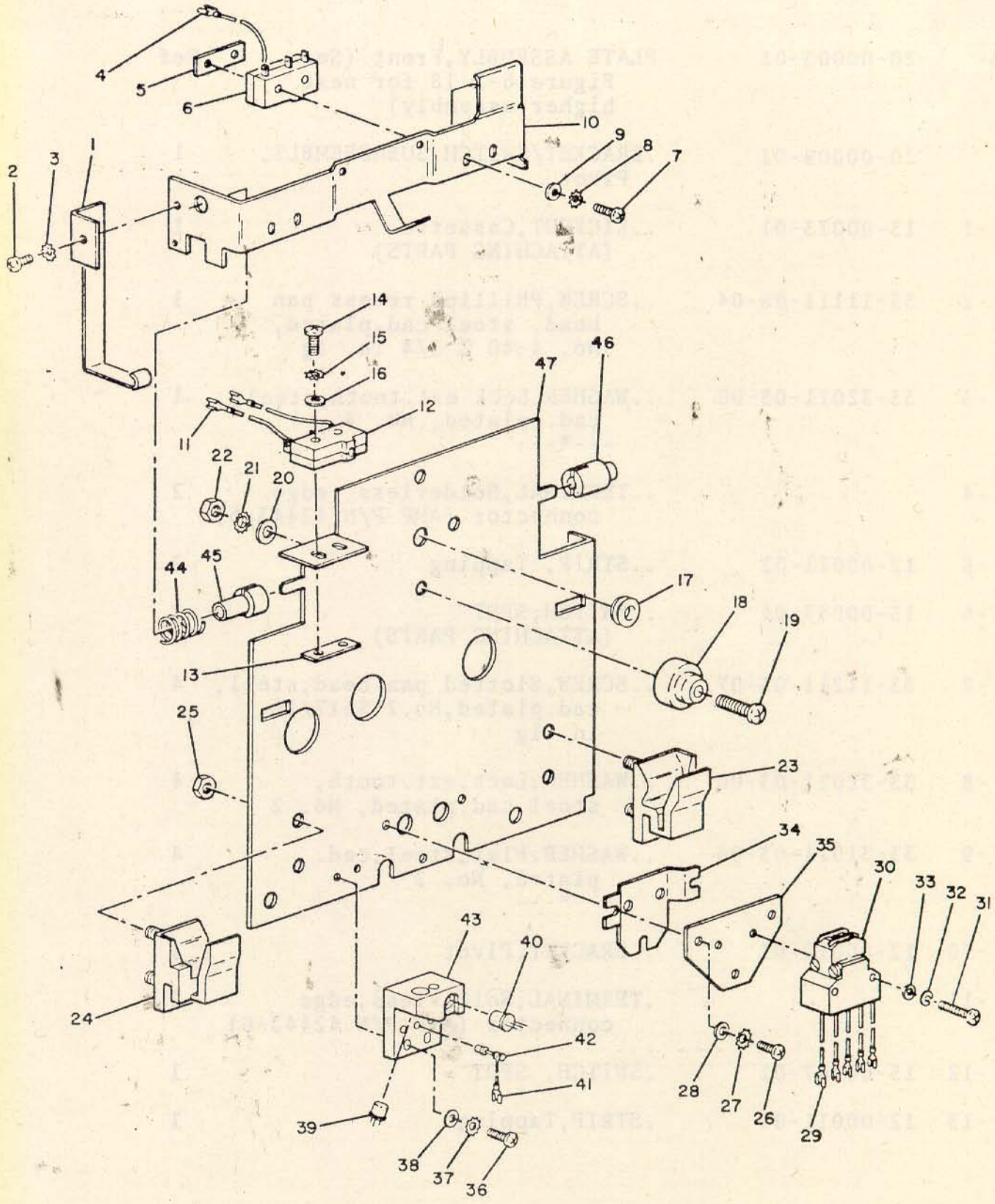


Figure 6-3. Front Plate Assembly, Cassette Transport

FIG & INDEX NUMBER	REDACTRON PART NUMBER	DESCRIPTION 1234567	UNITS PER ASSY	USABLE ON CODE
6-3-	20-00003-01	PLATE ASSEMBLY,Front (See Figure 6-1-18 for next higher assembly)	Ref	
	20-00009-01	.BRACKET/SWITCH SUBASSEMBLY, Pivot	1	
-1	13-00073-01	..KICKOUT,Cassette (ATTACHING PARTS)	1	
-2	33-11111-08-04	..SCREW,Phillips recess pan head, steel cad.plated, No. 4-40 X 1/4 in. lg	1	
-3	33-32011-08-00	..WASHER,Lock ext.tooth,steel, cad. plated, No. 4 ---*---	1	
-4		..TERMINAL,Solderless, edge connector (AMP P/N 42443-6)	2	
-5	12-00011-01	..STRIP, Tapping	2	
-6	15-00067-01	..SWITCH,SPDT (ATTACHING PARTS)	2	
-7	33-11211-03-07	..SCREW,Slotted pan head,steel, cad.plated,No.2-56X7/16 in. lg	4	
-8	33-32011-03-00	..WASHER,Lock,ext.tooth, steel cad.plated, No. 2	4	
-9	33-31011-03-00	..WASHER,Flat,steel,cad. plated, No. 2 ---*---	4	
-10	12-00010-01	..BRACKET,Pivot	1	
-11		.TERMINAL,Solderless,edge connector (AMP P/N 42443-6)	2	
-12	15-00067-01	.SWITCH, SPDT	1	
-13	12-00011-01	.STRIP,Tapping	1	

FIG & INDEX NUMBER	REDACTRON PART NUMBER	DESCRIPTION 1234567	UNITS PER ASSY	USABLE ON CODE
		(ATTACHING PARTS)		
6-3-14	33-11211-03-07	.SCREW,slotted pan head, steel, cad plated,No.2-56 X 7/16 in. lg	2	
-15	33-32011-03-00	.WASHER,Lock,ext.tooth,steel, cad.plated,No. 2	2	
-16	33-31011-03-00	.WASHER,Flat,Steel,cad,plated, No. 2 ---*---	2	
-17	31-40001-21-06	.GROMMET,Rubber (H.H.Smith P/N 2172)	1	
-18	11-00007-01	.BUMPER,Locating (ATTACHING PARTS)	1	
-19	33-11211-08-09	.SCREW,Slotted pan head, steel,cad.plated,No.4-40 X 9/16 in. lg	1	
-20	33-31011-05-00	.WASHER,Flat,steel,cad.plated No. 4	1	
-21	33-33011-08-00	.WASHER,Lock,ext.tooth,steel, cad.plated,No. 4	1	
-22	33-21011-08-00	.NUT,HEXAGON,steel,cad. plated, No. 4-40 ---*---	1	
-23	11-00015-01	.BLOCK,Locating, RH	1	
-24	11-00015-01	.BLOCK,Locating, LH (ATTACHING PARTS)	1	
-25	33-29084-09-00	.NUT,Speed,self thread (Palnut P/N SR188006) ---*---	4	
	20-00038-01	.PLATE SUBASSEMBLY,Magnetic head	1	

FIG & INDEX NUMBER	REDACTRON PART NUMBER	DESCRIPTION 1234567	UNITS PER ASSY	USABLE ON CODE
		(ATTACHING PARTS)		
6-3-26	33-11111-08-05	.SCREW,Phillips recess pan head, steel, cad. plated, No. 4-40 X 5/16 in. lg.	3	
-27	33-32011-08-00	.WASHER,Lock,ext.tooth,steel cad.plated, No. 4	3	
-28	33-31011-08-00	.WASHER,Flat,steel,cad.plated, No. 4 ---*---	3	
-29		..TERMINAL,Solderless,edge connector (AMP P/N 42443-6)	5	
-30	15-00062-01	..MAGNETIC HEAD (ATTACHING PARTS)	1	
-31	33-11211-03-09	..SCREW,slotted pan head,steel, cad.plated No.2-56 X 9/16 in. lg.	2	
-32	33-34011-03-00	..WASHER,Lock,split,steel, cad.plated, No. 2	2	
-33	33-31011-03-00	..WASHER,Flat,steel,cad. plated, No. 2 ---*---	2	
-34	13-00040-01	..SPRING,Adjusting	1	
-35	12-00039-01	..PLATE,Magnetic head	1	
	20-00012-01	.END OF TAPE ASSEMBLY (ATTACHING PARTS)	1	
-36	33-11211-03-05	.SCREW,Slotted pan head,steel, cad.plated,No.2-56X5/16 in. lg.	2	
-37	33-32011-03-00	.WASHER,Lock,ext.tooth,steel, cad.plated, No. 2	2	
-38	33-31011-03-00	.WASHER,Flat,steel,cad. plated No. 2 ---*---	2	
-39		..LAMP,Infrared,miniature (GE P/N SSL-4)	1	

FIG & INDEX NUMBER	REDACTRON PART NUMBER	DESCRIPTION 1234567	UNITS PER ASSY	USABLE ON CODE
		(ATTACHING PARTS)		
6-3-14	33-11211-03-07	.SCREW,slotted pan head, steel, cad plated,No.2-56 X 7/16 in. lg	2	
-15	33-32011-03-00	.WASHER,Lock,ext.tooth,steel, cad.plated,No. 2	2	
-16	33-31011-03-00	.WASHER,Flat,Steel,cad,plated, No. 2 ---*---	2	
-17	31-40001-21-06	.GROMMET,Rubber (H.H.Smith P/N 2172)	1	
-18	11-00007-01	.BUMPER,Locating (ATTACHING PARTS)	1	
-19	33-11211-08-09	.SCREW,Slotted pan head, steel,cad.plated,No.4-40 X 9/16 in. lg	1	
-20	33-31011-05-00	.WASHER,Flat,steel,cad.plated No. 4	1	
-21	33-33011-08-00	.WASHER,Lock,ext.tooth,steel, cad.plated,No. 4	1	
-22	33-21011-08-00	.NUT,HEXAGON,steel,cad. plated, No. 4-40 ---*---	1	
-23	11-00015-01	.BLOCK,Locating, RH	1	
-24	11-00015-01	.BLOCK,Locating, LH (ATTACHING PARTS)	1	
-25	33-29084-09-00	.NUT,Speed,self thread (Palnut P/N SR188006) ---*---	4	
	20-00038-01	.PLATE SUBASSEMBLY,Magnetic head	1	

FIG & INDEX NUMBER	REDACTRON PART NUMBER	DESCRIPTION 1234567	UNITS PER ASSY	USABLE ON CODE
		(ATTACHING PARTS)		
6-3-26	33-11111-08-05	.SCREW,Phillips recess pan head, steel, cad. plated, No. 4-40 X 5/16 in. lg.	3	
-27	33-32011-08-00	.WASHER,Lock,ext.tooth,steel cad.plated, No. 4	3	
-28	33-31011-08-00	.WASHER,Flat,steel,cad.plated, No. 4 ---*---	3	
-29		..TERMINAL,Solderless,edge connector (AMP P/N 42443-6)	5	
-30	15-00062-01	..MAGNETIC HEAD (ATTACHING PARTS)	1	
-31	33-11211-03-09	..SCREW,slotted pan head,steel, cad.plated No.2-56 X 9/16 in. lg.	2	
-32	33-34011-03-00	..WASHER,Lock,split,steel, cad.plated, No. 2	2	
-33	33-31011-03-00	..WASHER,Flat,steel,cad. plated, No. 2 ---*---	2	
-34	13-00040-01	..SPRING,Adjusting	1	
-35	12-00039-01	..PLATE,Magnetic head	1	
	20-00012-01	.END OF TAPE ASSEMBLY (ATTACHING PARTS)	1	
-36	33-11211-03-05	.SCREW,Slotted pan head,steel, cad.plated,No.2-56X5/16 in. lg.	2	
-37	33-32011-03-00	.WASHER,Lock,ext.tooth,steel, cad.plated, No. 2	2	
-38	33-31011-03-00	.WASHER,Flat,steel,cad. plated No. 2 ---*---	2	
-39		..LAMP,Infrared,miniature (GE P/N SSL-4)	1	

FIG & INDEX NUMBER	REDACTRON PART NUMBER	DESCRIPTION 1234567	UNITS PER ASSY	USABLE ON CODE
6-3-40		..SENSOR,Light,planar silicon, P.D. amplifier (GE P/N 2N5779, Type L14B3)	1	
-41		..TERMINAL,Solderless,edge connector (AMP P/N 42443-6)	3	
-42		..TERMINAL, LUG NURL-LOC FUZZ BUTTON HOLDER (EMC P/N TYPE 31-5089-P2)	3	
-43	11-00079-01	..BLOCK, End of tape	1	
-44	13-00014-01	.SPRING, Pivot bracket	1	
	20-00004-01	.PLATE SUBASSEMBLY, Front	1	
-45	13-00006-01	..BUSHING, Spring	1	
-46	13-00005-01	..BUSHING, Pivot	1	
-47	12-00008-01	..PLATE, Front	1	

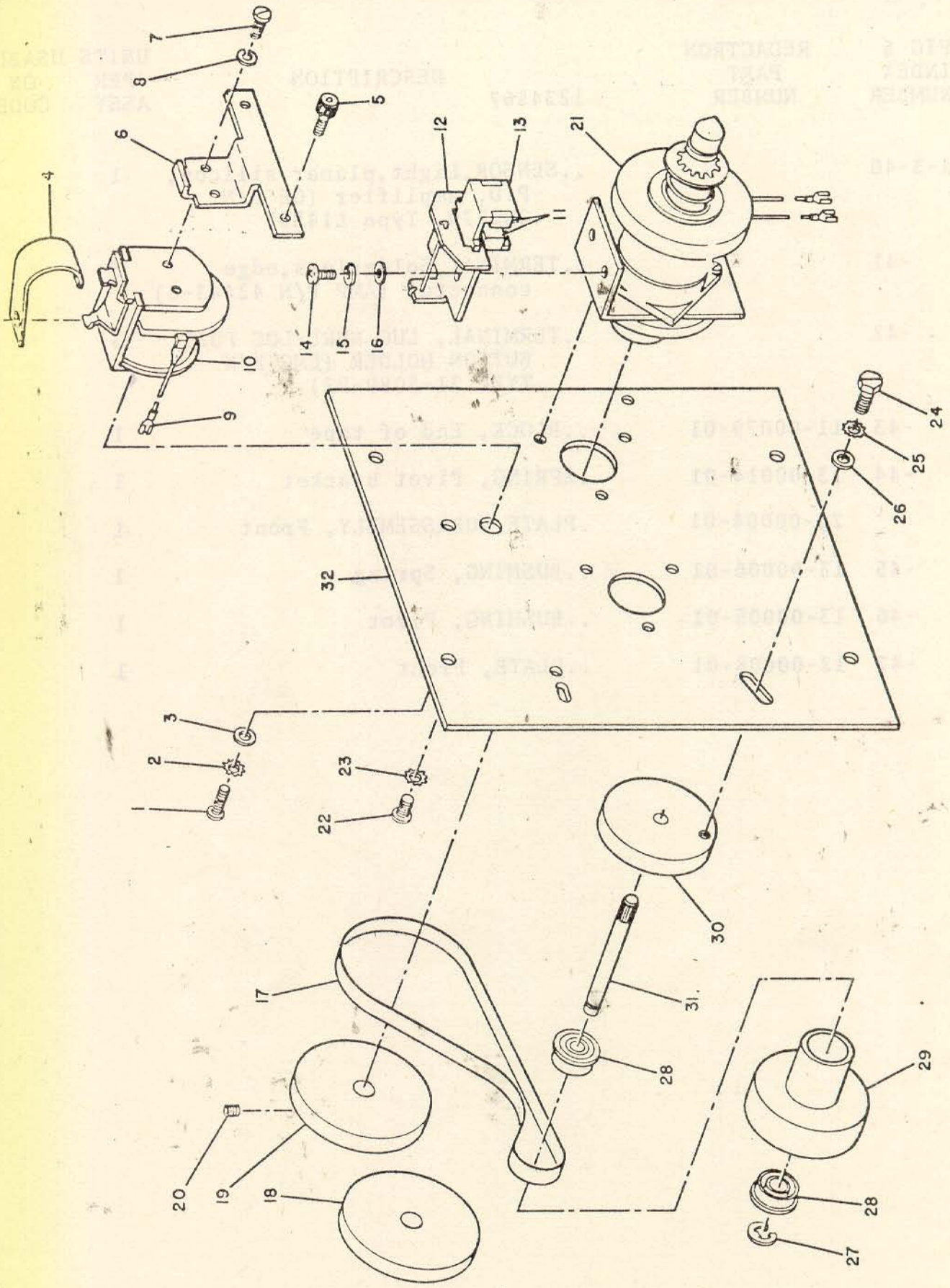


Figure 6-4. Bearing Plate Assembly, Cassette Transport

FIG & INDEX NUMBER	REDACTRON PART NUMBER	DESCRIPTION 1234567	UNITS PER ASSY	USABLE ON CODE
6-4-	20-00016-01	PLATE ASSEMBLY, Bearing (See figure 6-1-23 for next higher assembly)	Ref	
	20-00074-01	.BAR SUBASSEMBLY, Actuator/ brake (ATTACHING PARTS)	1	
-1	33-11111-12-06	.SCREW,Phillips recess pan head,steel,cad.plated,No. 6-32 X 3/8 in. lg.	1	
-2	33-32011-12-00	.WASHER,Lock,ext.tooth,steel, cad.plated, No. 6	1	
-3	33-31011-12-00	.WASHER,Flat,steel,cad. plated, No. 6 ---*---	1	
-4	13-00077-01	..SPRING, Return	1	
-5	33-13333-08-04	..SCREW,Socket head cap,black oxide, No. 4-40 X 1/4 in. lg (Unbrako P/N LOC-WEL)	2	
-6	12-00076-01	..BAR, Brake (ATTACHING PARTS)	1	
-7	33-11211-03-02	..SCREW,slotted pan head,steel, cad.plated,No.2-56X1/8 in. lg.	2	
-8	33-34011-03-00	..WASHER,Locksplit,steel, cad.plated, No. 2 ---*---	2	
-9		..TERMINAL,Solderless, edge connector (AMP P/N 42443-6)	2	
-10	15-00075-01	..ACTUATOR	1	
-11	13-00071-01	.BRAKE shoe, Disc brake	4	
-12	12-00070-01	.CLAPPER, Disc brake	2	

FIG & INDEX NUMBER	REDACTRON PART NUMBER	DESCRIPTION 1234567	UNITS PER ASSY	USABLE ON CODE
6-4-13	12-00069-01	.BRACKET,Adjusting,disc brake (ATTACHING PARTS)	2	
-14	33-11211-03-04	.SCREW,Slotted pan head,steel, cad.plated,No.2-56 X 1/4 in. lg.	4	
-15	33-34011-03-00	.WASHER,Lock,split,steel, cad.plated, No. 2	4	
-16	33-31011-03-00	.WASHER,Flat,Steel,cad. plated No. 2 ---*---	4	
-17	11-00054-02	.BELT,Endless (8.75)	1	
-18	13-00026-02	.PULLEY,Driven,Flat	1	
-19	13-00026-01	.PULLEY,Driven,crown (ATTACHING PARTS)	1	
-20	33-19333-08-03	.SETSCREW,Alloy steel,black oxide,No. 4-40 X 3/16 in. lg. (Unbrako P/N LOC-WEL) ---*---	2	
-21	20-00513-01	.SPINDLE/CLUTCH ASSEMBLY (ATTACHING PARTS)	2	
-22	33-11111-12-04	.SCREW,Phillips recess pan head,steel,cad.plated,No. 6-32X1/4 in. lg.	6	
-23	33-32011-12-00	.WASHER,Lock,ext.tooth,steel, cad.plated, No. 6 ---*---	6	
	20-00020-01	..SPINDLE SUBASSEMBLY	1	
	13-00022-01	...SPRING, Spindle (ATTACHING PARTS)	1	
	33-50622-10-00	...RING,Push-on (Truarc P/N 5115-34-H) ---*---	1	
	13-00023-01	...WASHER, Keyed	2	
	20-00063-01	...DISC SUBASSEMBLY Inertia	1	
	11-00064-01	...LINER,Inertia disc	1	

FIG & INDEX NUMBER	REDACTRON PART NUMBER	1234567 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE
6-4-	13-00024-01	....DISC,Inertia	1	
	11-00021-01	...SPINDLE	1	
→	33-40001-01	..BEARING,Single shield (NMB P/N RI-418Z	1	
	33-50311-03-00	..RING,Retaining (Truarc P/N 5103-12-5)	1	
→	33-40002-01-00	..BEARING,Flanged,single shield (NMB P/N RIF-418Z)	1	
	33-52022-03-00	..SPACER,Bearing 1/8 bore X .010 thick (PIC P/N B4-4)	2	
	33-50411-05-00	..RING,Grip (Truarc P/N 5555-18-S)	2	
→	33-40003-01-00	..BEARING,Flanged,single shield, ext race (NMB P/N RIF6632-ZEE)	4	
	20-00018-01	..SHAFT AND ROTOR SUBASSEMBLY	2	
	15-00061-01	...ROTOR,Clutch (General Time Corp. P/N FLO8-0300-5010)	Ref	
	13-00019-01	...SHAFT,Spindle	1	
	15-00061-01	..HOUSING,Clutch (ATTACHING PARTS)	2	
	33-11211-03-04	..SCREW,Slotted pan head, steel,cad.plated, No. 2-56 X 1/4 in. lg.	4	
	33-34011-03-00	..WASHER,Lock,split,steel, cad.plated, No. 2	4	
		---*---		
	13-00065-01	..SPRING, Retaining	2	
	15-00061-01	..FACE PLATE, Clutch	2	
		..TERMINAL,Solderless,edge connector (AMP P/N 42443-6)	4	

FIG & INDEX NUMBER	REDACTRON PART NUMBER	DESCRIPTION 1234567	UNITS PER ASSY	USABLE ON CODE
6-4-				
	12-00068-01	..BRACKET,Mounting,disc brake	2	
	13-00025-01	..COLLAR, Bearing	2	
	20-00029-01	.PULLEY SUBASSEMBLY, Stepped (ATTACHING PARTS)	1	
-24	33-14211-14-06	.SCREW,Slotted hexagon head, steel,cad.plated,No. 8-32 X 3/8 in. lg.	1	
-25	33-32011-14-00	.WASHER,Lock,ext.tooth, steel,cad.plated,No. 8	1	
-26	33-31011-14-00	.WASHER,Flat,steel,cad. plated, No. 8	1	
		---*---		
-27	33-50311-05-00	..RING,Retaining (Truarc P/N 5103-18-S)	1	
-28	33-40003-01	..BEARING,Flanged,single shield ext race (NMB P/N RIF6632-ZEE)	2	
-29	13-00033-01	..PULLEY, Stepped	1	
	20-00030-01	..COLLAR/SHAFT SUBASSEMBLY	1	
-30	13-00031-01	...COLLAR, Adjustable	1	
-31	13-00032-01	...SHAFT, Idler	1	
-32	12-00017-01	.PLATE, Bearing	1	

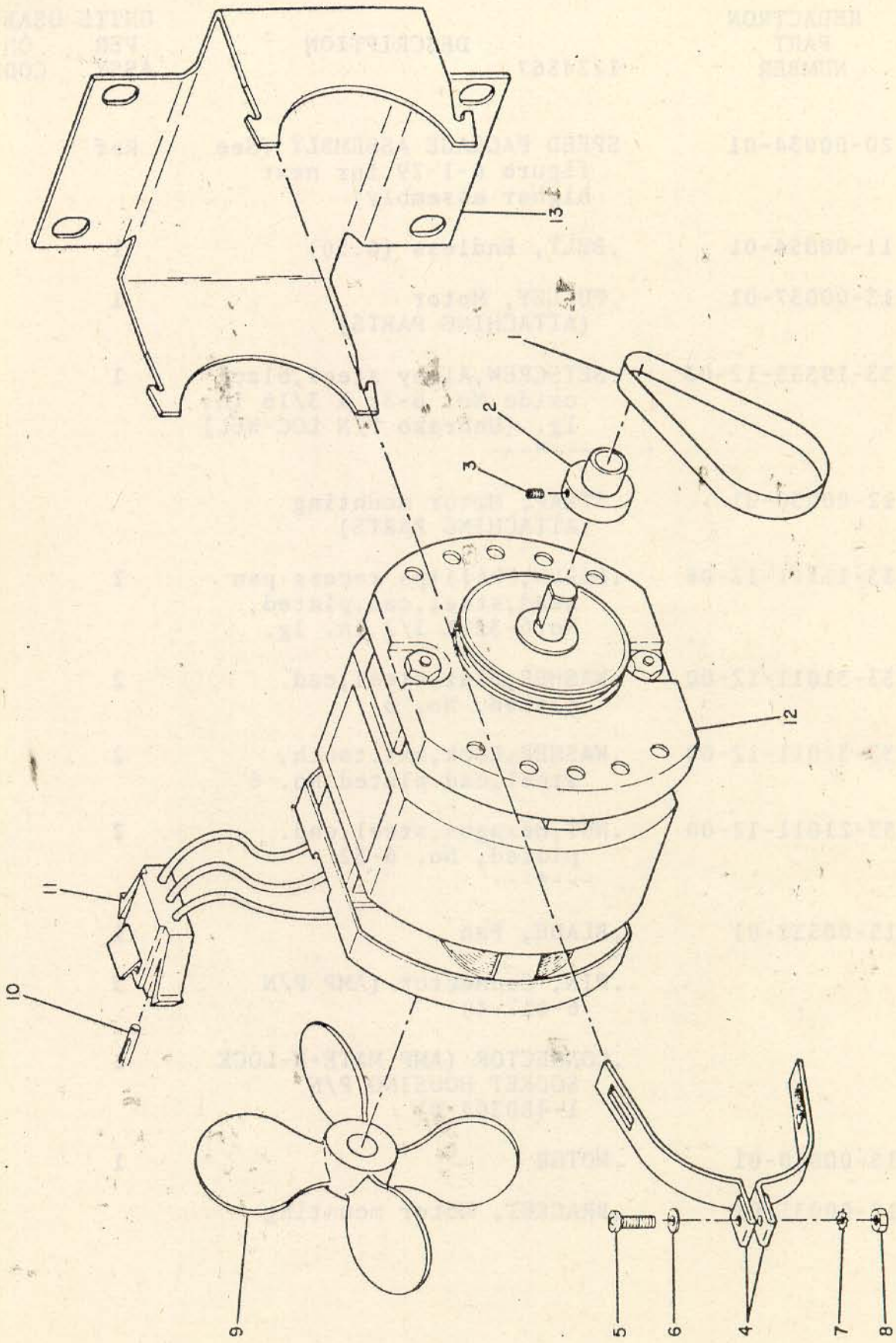


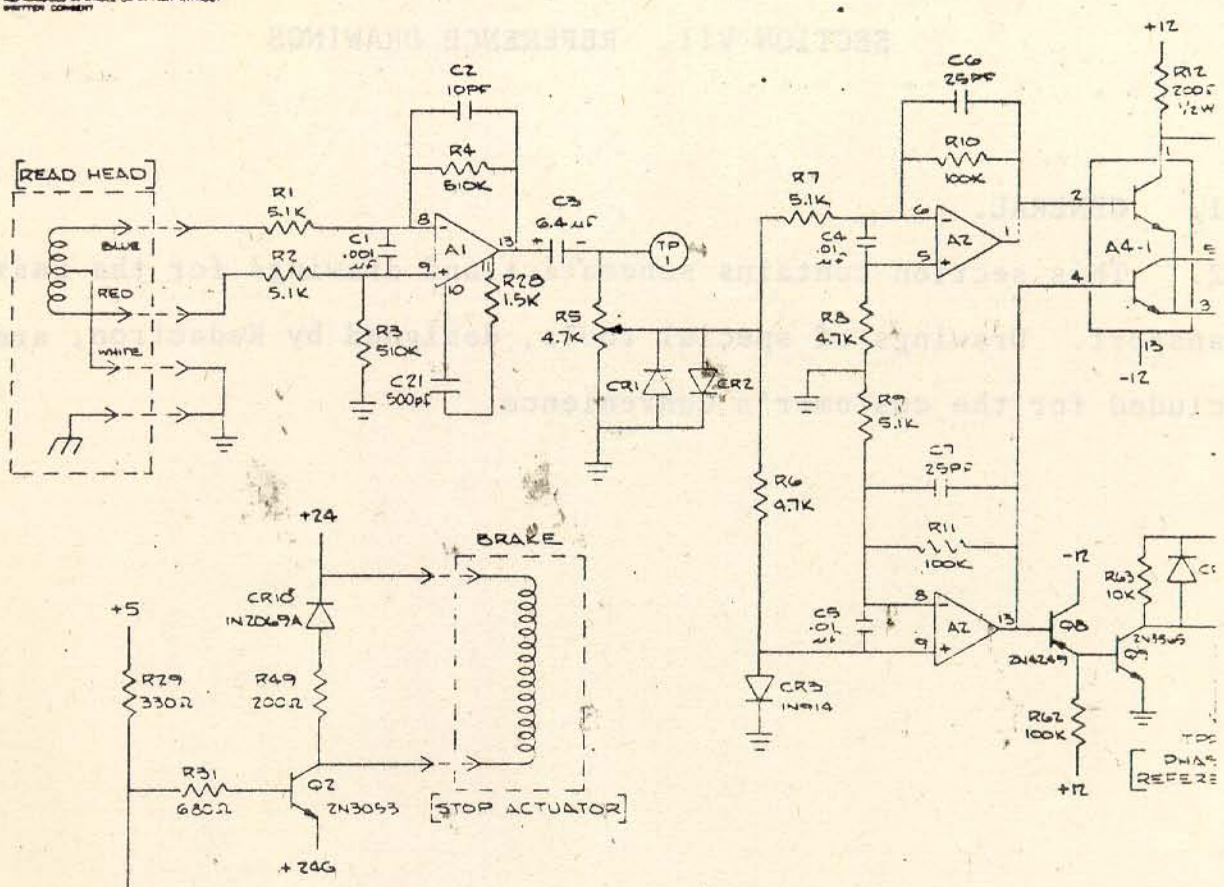
Figure 6-5. Speed Package Assembly, Cassette Transport

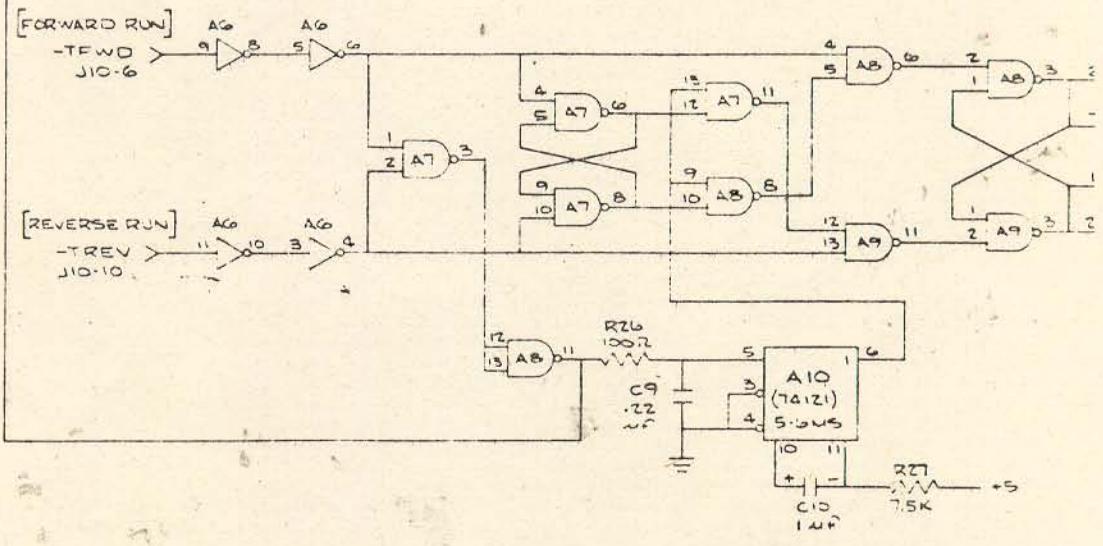
FIG & INDEX NUMBER	REDACTRON PART NUMBER	DESCRIPTION 1234567	UNITS PER ASSY	USABLE ON CODE
6-5-	20-00034-01	SPEED PACKAGE ASSEMBLY (See figure 6-1-29 for next higher assembly)	Ref	
-1	11-00054-01	.BELT, Endless (6.50)	1	
-2	13-00037-01	.PULLEY, Motor (ATTACHING PARTS)	1	
-3	33-19333-12-03	.SETSCREW,Alloy steel,black oxide No. 6-32 X 3/16 in. lg. (Unbrako P/N LOC-WEL) ---*---	1	
-4	12-00036-01	.STRAP, Motor mounting (ATTACHING PARTS)		
-5	33-11111-12-08	.SCREW,Phillips recess pan head,steel,cad.plated, No.6-32 X 1/2 in. lg.	2	
-6	33-31011-12-00	.WASHER,Flat,steel,cad. plated, No. 6	2	
-7	33-32011-12-00	.WASHER,Lock,ext.tooth, steel,cad.plated,No. 6	2	
-8	33-21011-12-00	.NUT,Hexagon,steel,cad. plated, No. 6-32 ---*---	2	
-9	15-00532-01	.BLADE, Fan	1	
-10		.PIN, Connector (AMP P/N 6-617-4)	3	
-11		.CONNECTOR (AMP MATE-N-LOCK SOCKET HOUSING P/N 1-480304-0)	1	
-12	15-00060-01	.MOTOR	1	
-13	12-00035-01	.BRACKET, Motor mounting		

SECTION VII. REFERENCE DRAWINGS

7-1. GENERAL.

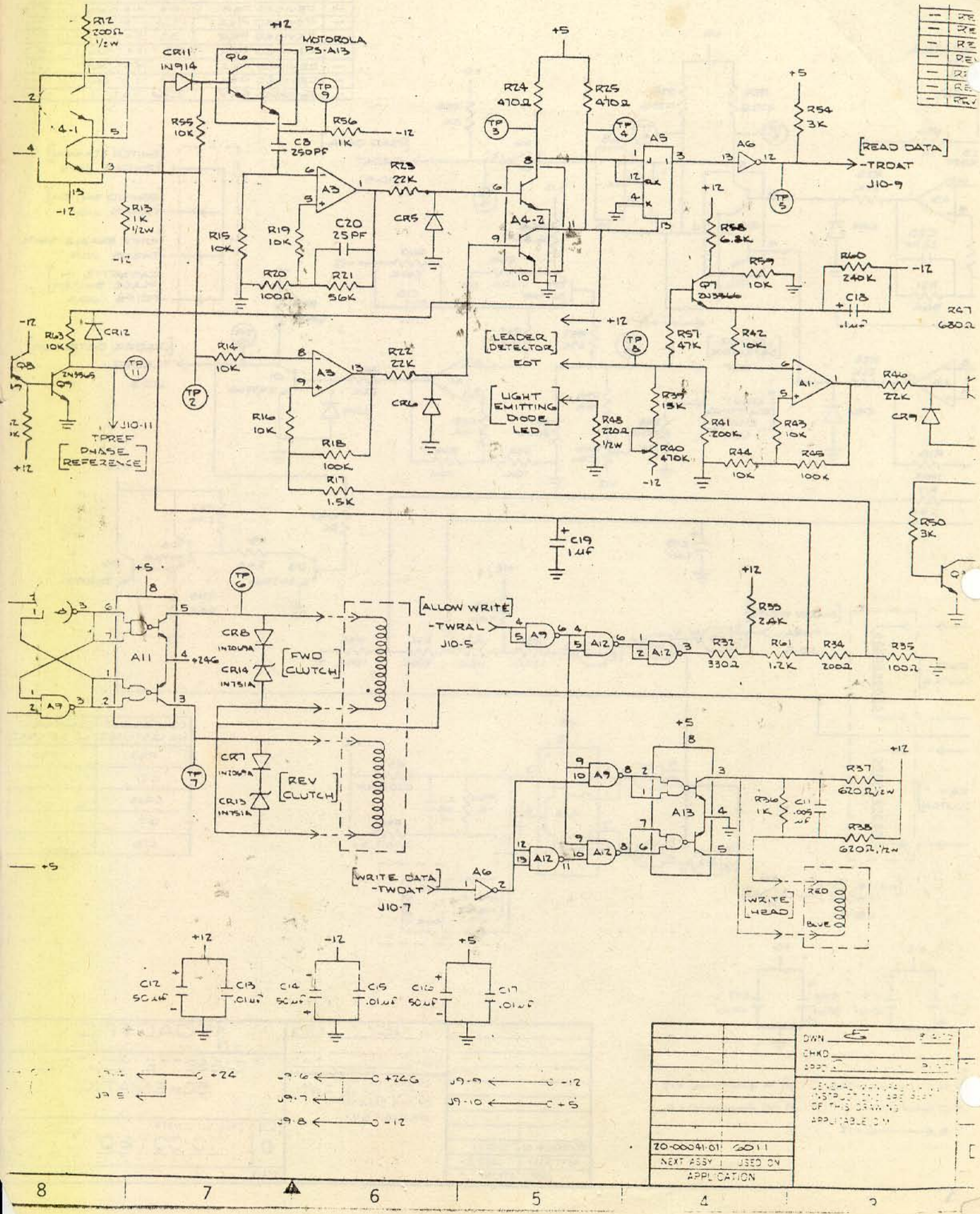
7-2. This section contains schematics and drawings for the Cassette Transport. Drawings of special tools, designed by Redactron, are included for the customer's convenience.



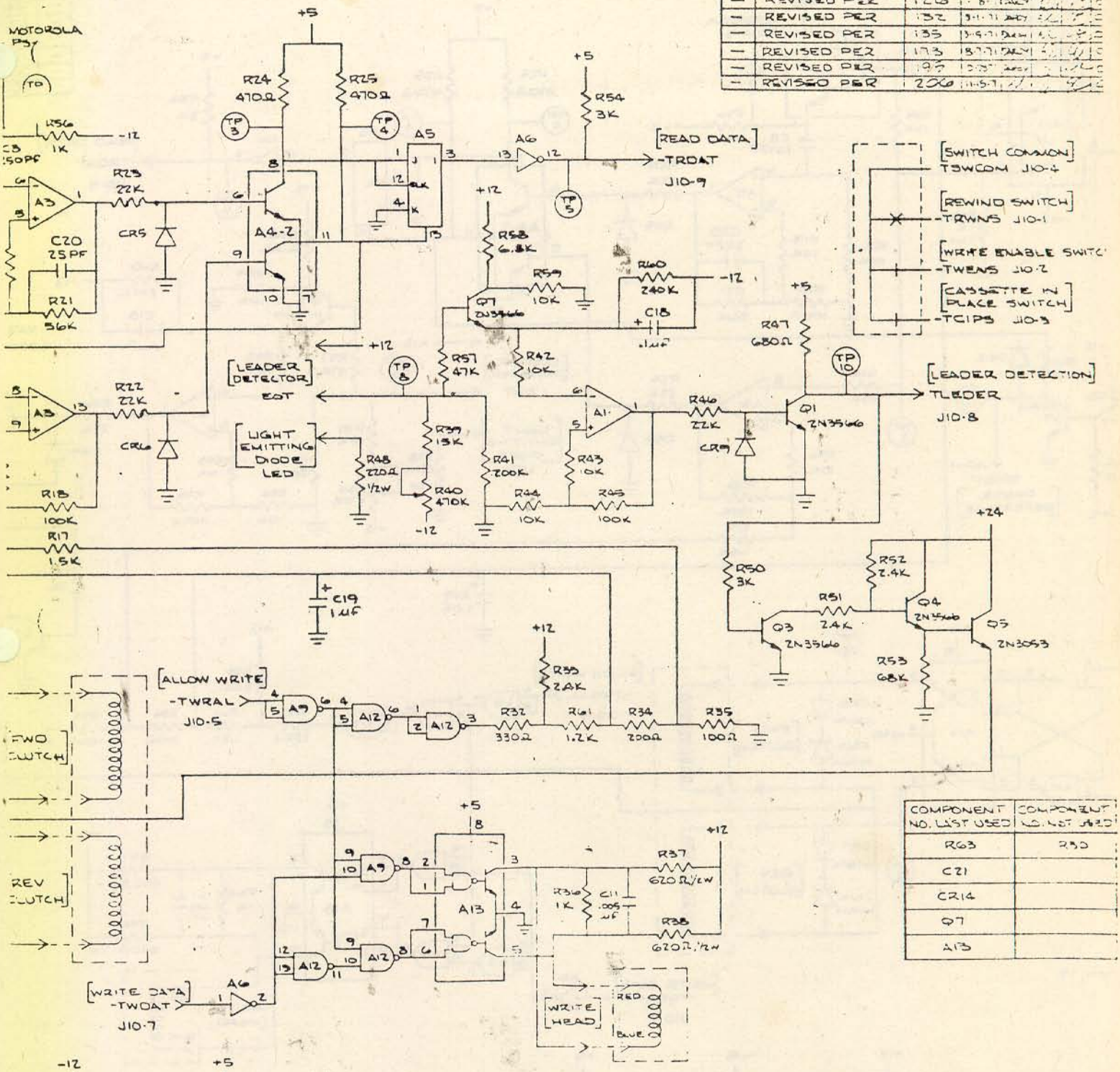


3. NAMES IN BRACKETS REFER TO REDACTRON SPECIFICATIONS # 90-00-54-01
2. IN CHIPS A1, A2, A3 PIN 7 = GRD PIN 14 = +12
C. ON ALL CHIPS PIN 7 = GRD PIN 14 = Vcc (+5)
B. ALL DIODES ARE IN914
A. ALL RESISTORS ARE 1/4W 5% CARBON
1. UNLESS OTHERWISE SPECIFIED

NOTES:


R12 200Ω 1/2W
CR11 IN914
Q6
MOTOROLA PS-A13
+12
TP 9
R55 10K
R56 1K
-12
C8 250PF
4-1
R13 1K 1/2W
A3
R15 10K
R19 10K
C20 25PF
R20 100Ω
R21 56K
R23 22K
CR5
R24 470Ω
R25 470Ω
+5
TP 3
TP 4
A5
A4-2
A6
R54 3K
[READ DATA]
-TRDAT
J10-9
TP 5
R58 6.3K
R59 10K
R60 240K
C18 .1uf
Q7 2N3906
R47 680Ω
R63 10K
CR12
Q8
Q9 2N3565
TP 11
TP 2
R14 10K
R22 22K
CR6
R16 10K
R18 100K
R17 1.5K
J10-11
TPREF
PHASE REFERENCE
[LEADER DETECTOR EOT]
TP 8
R57 47K
R42 10K
[LIGHT EMITTING DIODE LED]
R48 220Ω 1/2W
R39 15K
R40 470K
R41 200K
R43 10K
R44 10K
R45 100K
A1
R46 22K
CR9
R50 3K
C19 1uf
A11
TP 6
CR8 IN2071A
CR14 IN751A
[FWD CLUTCH]
[ALLOW WRITE]
-TWRAL
J10-5
A9
A12
R32 330Ω
R61 1.2K
R34 200Ω
R35 100Ω
R55 2.4K
CR7 IN2071A
CR13 IN751A
[REV CLUTCH]
TP 7
A13
R36 1K
C11 .005 uf
R37 620Ω 1/2W
R38 620Ω 1/2W
[WRITE DATA]
-TWDAT
J10-7
WRITE HEAD
RED
BLUE
C12 50uf
C13 .01uf
C14 50uf
C15 .01uf
C16 50uf
C17 .01uf
J9-5
J9-6
J9-7
J9-8
J9-9
J9-10
+24
-12
+5
DWN
CHKD
20-00041-01
6011
NEXT ASSY
USED ON
APPLICATION

REVISIONS				
ZONE	DESCRIPTION	E.R. / ECO	DATE	SIGN OFF
—	ORIGINAL ISSUE	0005		
—	REVISED PER	05		
—	REVISED PER	126		
—	REVISED PER	132		
—	REVISED PER	135		
—	REVISED PER	173		
—	REVISED PER	193		
—	REVISED PER	206		

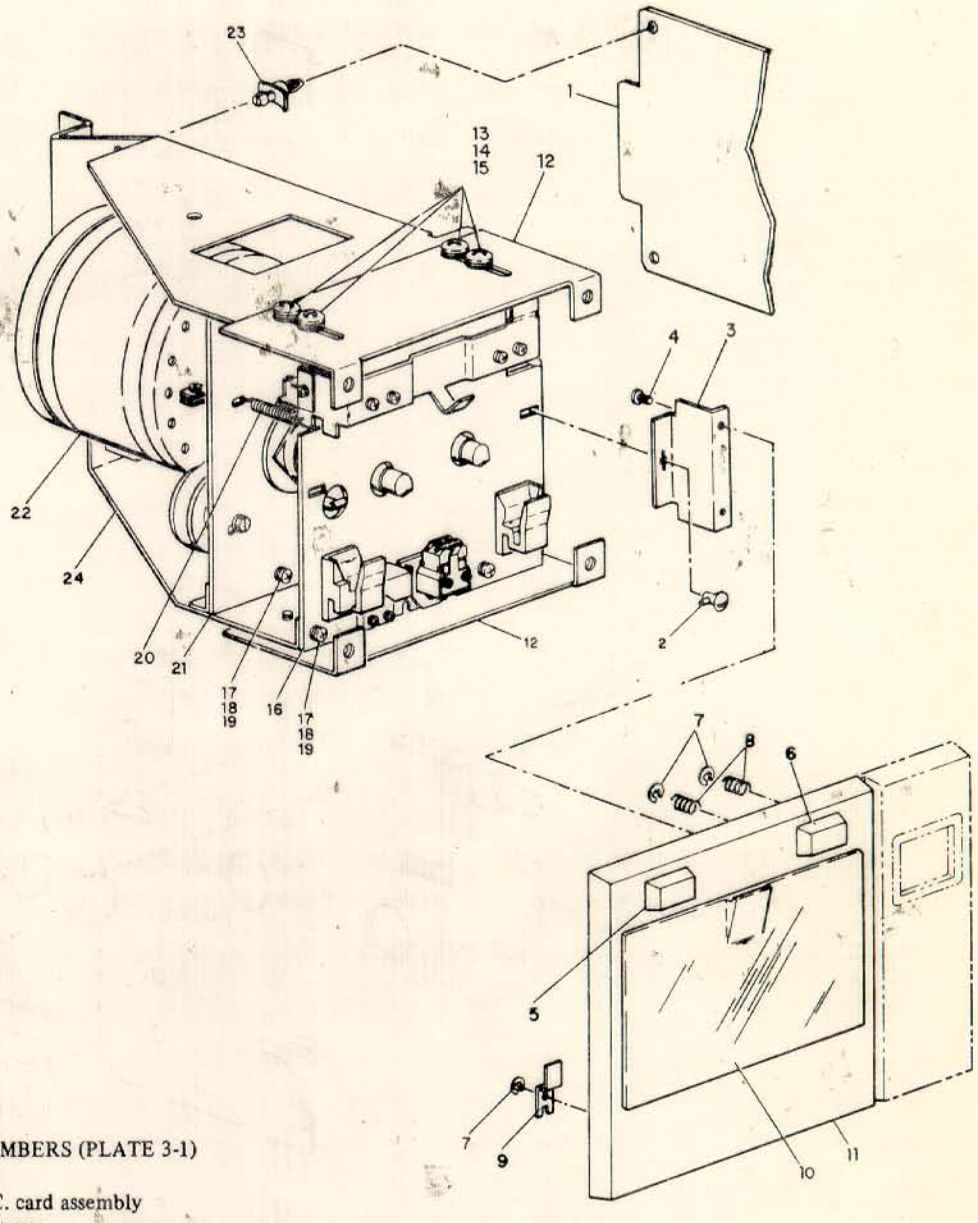


COMPONENT NO. LIST USED	COMPONENT NO. NOT USED
R63	R50
C21	
CR14	
Q7	
A13	

	DRAWN	REDACTRON
	CHKD	TITLE: CASSETTE CONTROL SCHEMATIC
	APPD	
	GENERAL MFG. PARTS LIST & INSTRUCTIONS ARE PART OF THIS DRAWING APPLICABLE G.M.I.	
20-00041-01 6011		SIZE: D DRAWING NUMBER: 70-00160-011-07
NEXT ASSY USED ON		
APPLICATION		SCALE: SHEET 1 OF 1

SECTION 3
MAGNETIC TAPE CASSETTE TRANSPORT

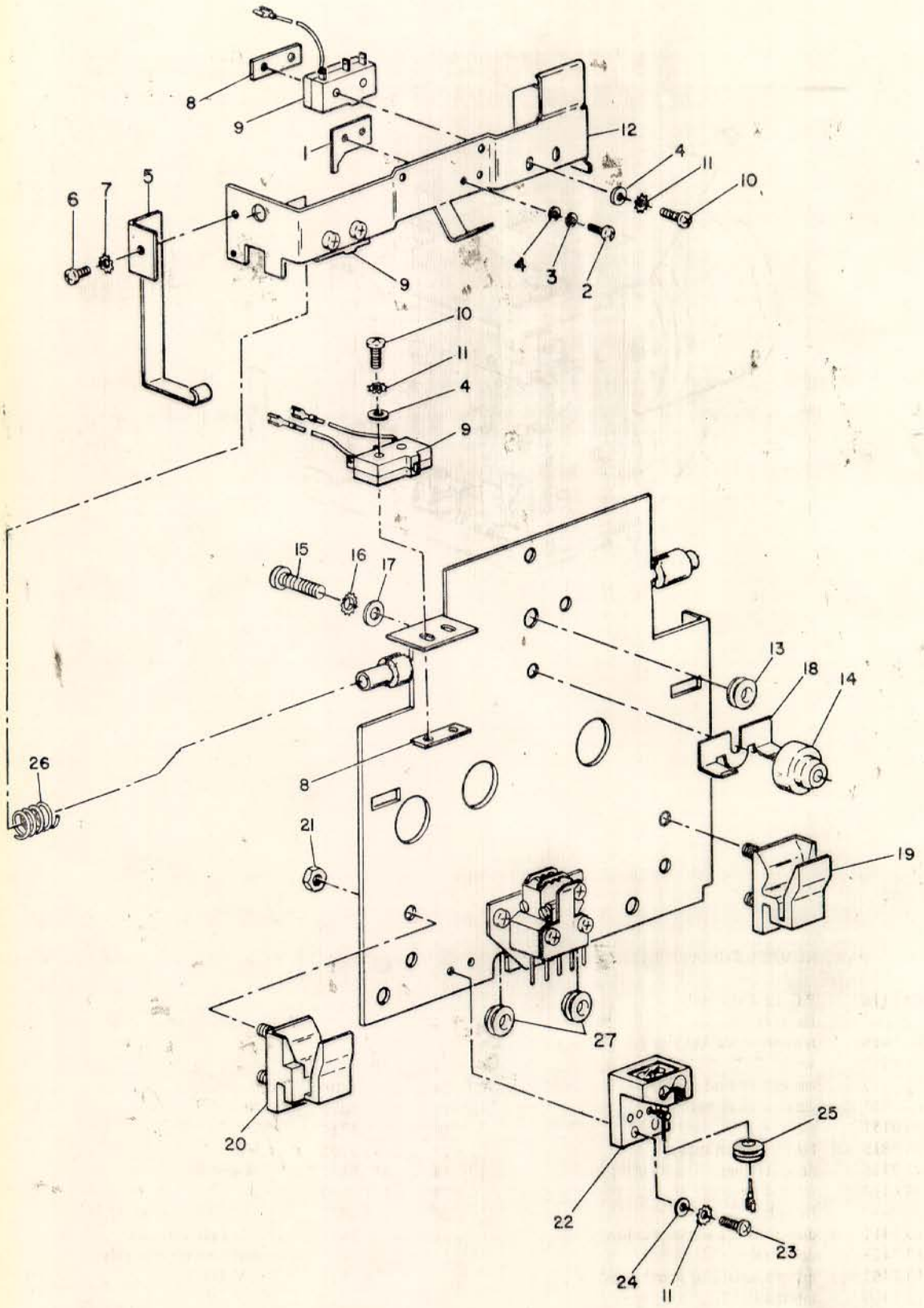
CASSETTE TRANSPORT (PLATE 3-1)



PART NUMBERS (PLATE 3-1)

1	2900 4116	P.C. card assembly
2	2942 0007	fastener
3	2904 3916	mounting bracket
4	2941 6997	screw
5	2913 7916	cassette rewind button
6	2913 7924	cassette eject button
7	2940 0157	push-on ring
8	2903 9815	button return spring
9	2903 9716	door retainer
10	2904 0110	front door
11	— —	front bezel
	2913 7411	domestic, for search window
	2913 7429	domestic
	2913 7452	international, for search window
	2913 7460	international
12	2900 3514	adjustable bracket
	2905 5415	adjustable bracket kit, not used on editing typewriter, includes 12 thru 15
13	2941 7243	screw
14	2941 8209	lockwasher
15	2941 8076	washer
16	2915 1214	front plate kit
17	2941 5981	screw
18	2941 8191	lockwasher
19	2941 8050	washer
20	2900 4819	pivot bracket return spring
21	2900 1617	bearing plate assembly
22	— —	speed package assembly
	2900 3415	115V, 60 Hz } refer to CASSETTE
	2900 3423	115V, 50 Hz } SPEED PACKAGE
	2900 3431	230V, 50 Hz }
23	2941 9843	standoff
24	2900 0213	cassette chassis

CASSETTE FRONT PLATE (PLATE 3-2)

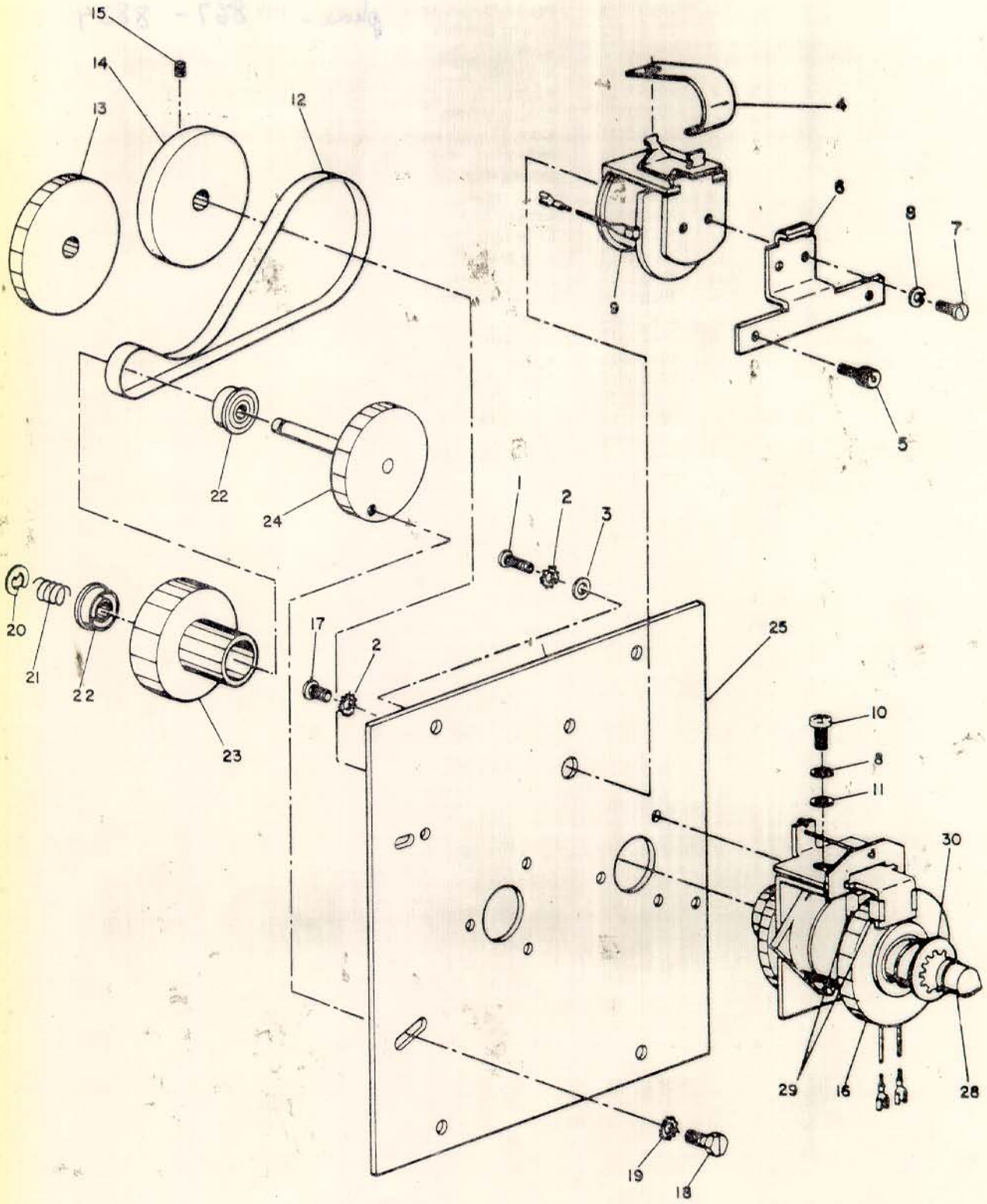


PART NUMBERS ON NEXT PAGE

PART NUMBERS (PLATE 3-2)

	2915 1214	Front Plate Assembly, includes 13 thru 27
	2900 0916	Bracket/Switch Assembly, includes 1 thru 12
1	2909 0412	cassette interlock
2	2941 6476	screw
3	2941 8167	lockwasher
4	2941 8027	washer
5	2900 7317	cassette kickout
6	2941 5841	screw
7	2941 8175	lockwasher
8	2900 1112	tapping strip
9	2900 6715	SPDT switch
10	2941 6500	screw
11	2941 8159	lockwasher
12	2900 1013	pivot bracket
13	2948 8525	rubber grommet
14	2910 3116	locating bumper
15	2941 5890	screw
16	2948 8517	lockwasher
17	2941 8035	washer
18	2910 3017	cassette loading spring
19	2900 1526	locating block, R.H.
20	2900 1518	locating block, L.H.
21	2941 8001	speednut
22	2900 1211	end of tape assembly
23	2941 6484	screw
24	2941 8688	washer
25	2941 5429	grommet
26	2900 1419	pivot bracket spring
27	2941 5189	grommet

CASSETTE BEARING PLATE (PLATE 3-3)



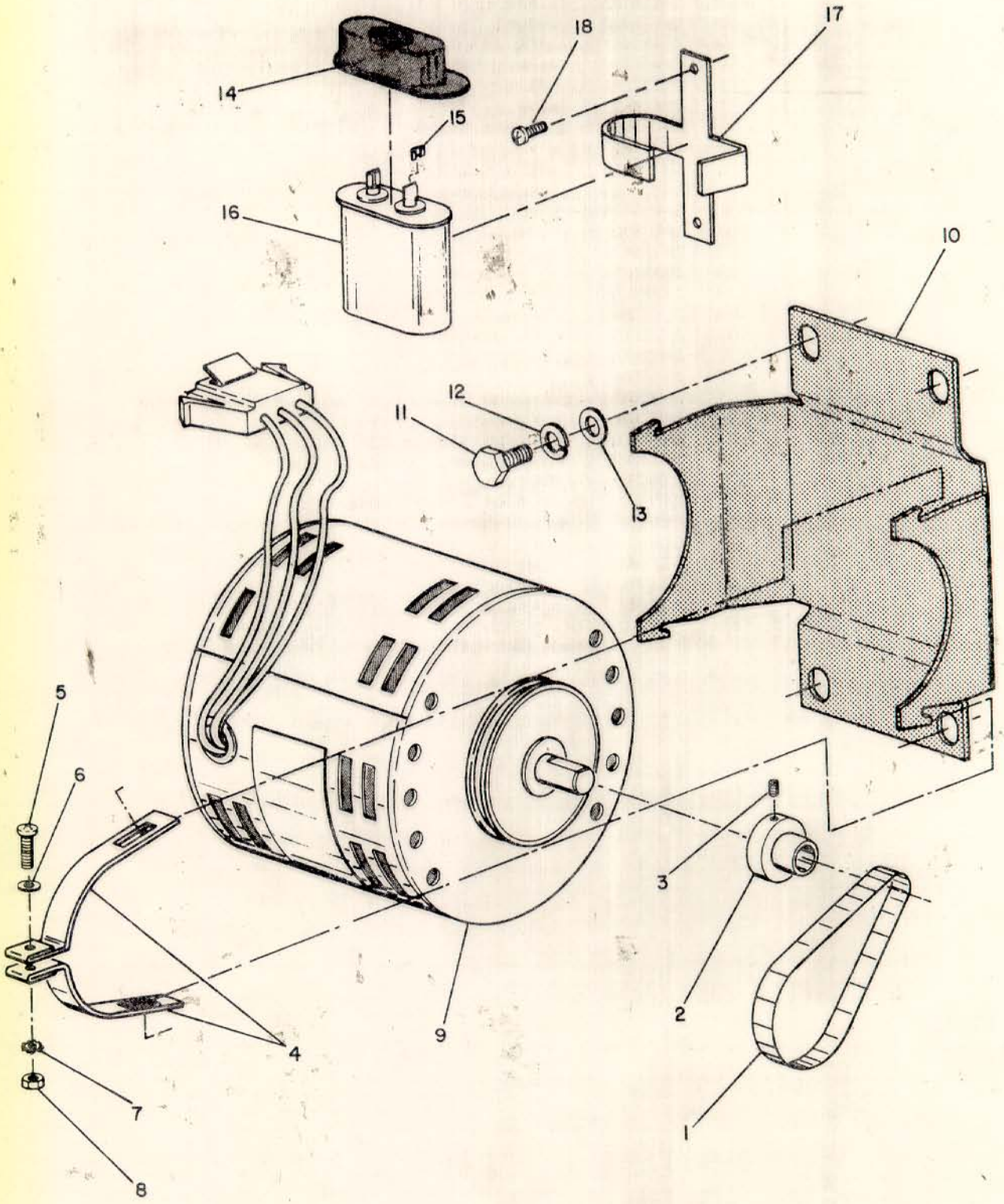
PART NUMBERS ON NEXT PAGE

PART NUMBERS (PLATE 3-3)

	2900 1617	Cassette Bearing Plate
1	2941 5999	screw
2	2941 8191	lockwasher
3	2941 8050	washer
4	2900 7713	return spring
5	2941 7136	screw
6	2900 7614	brake bar
7	2941 6450	screw
8	2941 8308	lockwasher
9	2900 7515	actuator
	2900 7416	actuator/brake bar assembly, includes 4 thru 9
10	2941 6476	screw
11	2941 8019	washer
12	2900 5428	driven belt
13	2900 2623	driven pulley, flat
14	2900 2615	driven pulley, crown
15	2941 7680	setscrew
16	2905 1315	spindle/clutch assembly
17	2941 5973	screw
18	2941 7243	screw
19	2941 8209	lockwasher
20	2943 5245	retaining ring
21	2909 9611	bearing preload spring
22	2941 8456	flanged bearing
23	2900 3316	idler pulley
	2900 2912	idler pulley assembly, includes 20 thru 24
24	2900 3019	collar/shaft assembly
25	2900 1716	bearing plate
28	2927 0618	spindle kit
29	2923 3111	brake shoe
30	2940 0173	push-on ring

Numbers not used: 26, 27

CASSETTE SPEED PACKAGE (PLATE 3-4)

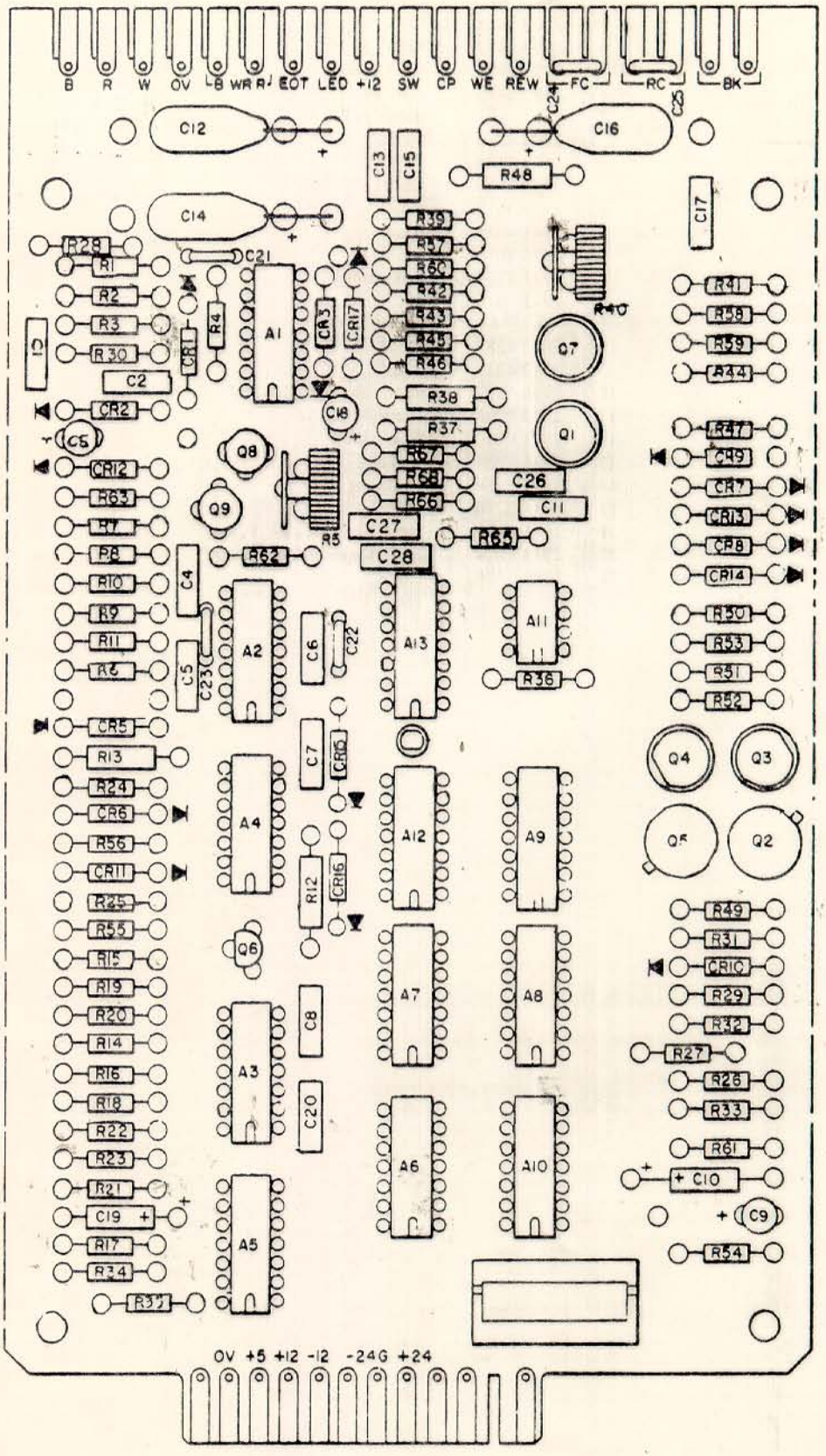


PART NUMBERS ON NEXT PAGE

PART NUMBERS (PLATE 3-4)

	— —	Speed Package
	2900 3415	115V, 60 Hz
	2900 3423	115V, 50 Hz
	2900 3431	230V, 50 Hz
1	2900 5410	drive belt
2	— —	motor pulley
	2908 4316	60 Hz
	2908 4324	50 Hz
3	2941 7730	setscrew
4	2900 3613	motor mounting strap
5	2941 6039	screw
6	2941 8050	washer
7	2941 8191	lockwasher
8	2941 7870	nut
9	— —	motor
	2943 4289	115V
	2943 4271	230V
10	2908 4217	motor mounting bracket
11	2941 7268	screw
12	2941 6500	lockwasher
13	2941 8084	washer
14	2941 5536	insulating boot
15	2941 2210	lug
16	2941 5932	capacitor (3mF, 370V, ± 10%)
17	2914 8814	capacitor mounting bracket
18	2941 7508	screw

TAPE CASSETTE LOCAL ELECTRONICS (PLATE 3-5)



PART NUMBERS ON NEXT PAGE

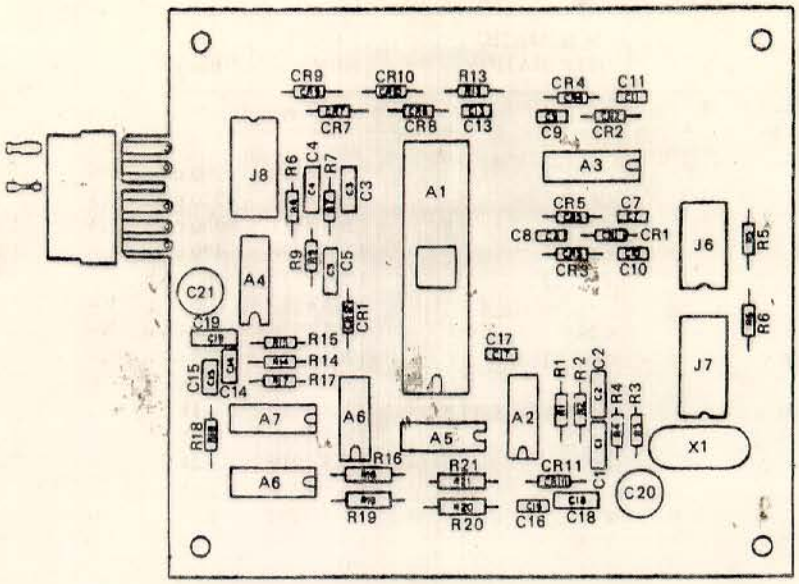
PART NUMBERS (PLATE 3-5)

2900 4116 Printed Circuit Card Assembly

PART NUMBER	DESCRIPTION			SCHEMATIC DESIGNATION
CAPACITORS				
2941 4356	10pF			C2
2945 5763	15pF			C6, 7
2942 1203	25pF			C20
2942 2334	250pF			C8
2942 2367	330pF			C22, 23
2941 4406	500pF			
2942 2425	750pF	1KV		C26
2942 2300	0.002uF	1KV		C11, 27
2941 4372	0.001uF			C1
2942 2474	.01uF	100V		C4, 5, 13, 15, 17, 24, 25
2941 9009	0.22uF	35V		C9
2942 2847	1uF	35V		C19
2942 2839	1uF	35V	± 5%	C10
2941 4489	1uF	35V	±10%	C18
2941 4562	6.8uF	35V	±10%	C3
2941 4547	47uF	35V	±20%	C12, 14, 16
DIODES				
2047 6982	1N270			CR2, 5, 6, 12, 15, 16
1285 5839	1N914			CR3, 11, 17
1760 2616	1N751A			CR13, 14
1072 7931	1N4003			CR7, 8, 10
INTEGRATED CIRCUITS				
2942 0890	CA3046			A4
2942 1161	LM1303			A1, 3
2942 0882	MC1303L			A2
2943 5195	MC75450P			A13
1447 3516	SN7400N			A7, 8, 9, 12
1447 3532	SN7404N			A6
1447 3615	SN74107N			A5
1447 3706	SN74121N			A10
2942 0924	SN75451AP			A11
POTENTIOMETERS				
2942 2003	5K	variable		R5
2942 2136	200K	variable		R40
RESISTORS				
1265 3978	100 ohms	¼W	± 5%	R20, 26
1265 4190	200 ohms	¼W	± 5%	R34, 49

PART NUMBER	DESCRIPTION			SCHEMATIC DESIGNATION
RESISTORS				
1265 4208	200 ohms	½W	± 5%	R12
1265 9025	220 ohm	1W	± 5%	R48
1265 4331	300 ohm	¼W	± 5%	R29, 32
1265 4455	470 ohm	¼W	± 5%	R24, 25
1265 4513	560 ohm	¼W	± 5%	R35
1265 4562	620 ohm	½W	± 5%	R37, 38
1265 4570	680 ohm	¼W	± 5%	R31, 47
1265 4612	750 ohm	¼W	± 5%	R61
1265 4695	1K	¼W	± 5%	R56, 65, 67
1265 4711	1K	½W	± 5%	R13
1265 4810	1.5K	¼W	± 5%	R17, 28
1265 4919	2K	¼W	± 5%	R66 68
1265 4976	2.4K	¼W	± 5%	R33, 51, 52
1265 4992	2.7K	¼W	± 5%	R1, 2
1265 5031	3K	¼W	± 5%	R36, 50, 54
1265 5296	6.8K	¼W	± 5%	R58
1265 5338	7.5K	¼W	± 5%	R6
1265 5353	8.2K	¼W	± 5%	R8
1142 7572	8.25K	¼W	± 1%	R7, 27
1142 7580	9.09K	¼W	± 1%	R9
1265 5411	10K	¼W	± 5%	R14, 15, 16, 19, 39, 42, 43, 44, 55, 59, 63
1265 5650	22K	¼W	± 5%	R22, 23, 46
1265 5890	47K	¼W	± 5%	R57
1265 5957	56K	¼W	± 5%	R21
1265 6013	68K	¼W	± 5%	R53
1265 6138	100K	¼W	± 5%	R18, 30, 45, 62
2940 0397	150K	¼W	± 1%	R10, 11
1265 6351	200K	¼W	± 5%	R41
1265 6419	240K	¼W	± 5%	R60
1265 6492	330K	¼W	± 5%	R3
TRANSISTORS				
2942 0072	2N3053			Q2, 5
2942 0064	2N3565			Q9
2942 0080	2N3566			Q1, 3, 4, 7
2942 0130	2N4249			Q8
2942 0122	PS-A13			Q6
MISCELLANEOUS				
2904 7818	P.C. card support			
2941 0768	socket, 8 pin			for A11
2943 9387	socket, 16 pin			
2941 5510	thermolloy spacer			for Q1, 2, 3, 4, 5, 7

CASSETTE TRANSPORT CONTROLLER PCB (PLATE 3-6)



PART NUMBERS (PLATE 3-6)

2907 8912	Magnetic Tape Transport Controller Assembly
2907 8920	Magnetic Tape Transport Controller Assembly, Option A
2907 8938	Magnetic Tape Transport Controller Assembly, Option B
2907 6312	Tape Transport Controller PCB
2907 6338	Tape Transport Controller PCB, Option A, B

PART NUMBER	DESCRIPTION			SCHEMATIC DESIGNATION
CAPACITORS				
2941 4398	200pF	1KV	±10%	C3, 4, 5
2941 4406	500pF	1KV	±10%	C1
2942 2474	0.01uF	35V	±10%	C17, 18, 19
2942 2516	0.05uF	100V	±20%	C2
2942 2821	0.1uF	35V	±10%	C7, 8, 9, 10, 11, 14, 15
2942 2946	3.3uF	35V	±20%	C13, 16
2941 4547	47uF	35V	±20%	C20, 21
DIODES				
2047 6982	1N270			CR7, 9, 12
1760 2616	1N751A			CR11
1285 5839	1N914			CR1, 2, 3, 4, 5
1072 7931	1N4003			CR8, 10
INTEGRATED CIRCUITS				
2600 4911	SN7402N			A6
1447 3532	SN7404N			A2
1674 4963	SN7406N			A8
1447 9596	SN7437N			A7
2201 7560	SN7495N			A5
1536 2809	SN74L04N			A4
2904 2413	resistor pack			A3
2904 6216	RTTC			A1

PART NUMBER	DESCRIPTION			SCHEMATIC DESIGNATION
OSILLATOR				
2942 0692	3.84MHz, crystal			X1
RESISTORS				
1265 4356	330 ohm	½W	±5%	R20, 21
1265 4372	360 ohm	¼W	±5%	R15, 18
1265 4398	390 ohm	¼W	±5%	R13, 14, 17
1265 4711	1K	½W	±5%	R16, 19
1265 4810	1.5K	¼W	±5%	R2
1265 4935	2.2K	¼W	±5%	R3, 4, 5, 6, 11
1265 5171	4.7K	¼W	±5%	R7, 8, 9
MISCELLANEOUS				
2941 1568	connector pin			
2941 1576	connector, 6 pin			
2941 1527	key			
2941 0776	socket, 14 pin			J6
2941 0792	socket, 16 pin			J7, 8
2941 0834	socket, 40 pin			for A1


0
1
REWIND
EJECT
REWIND
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side 1
CERTIFIED DIGITAL CASSETTE
CONFORMS TO A.N.S.I. X3B5/40
MODEL 7250
200 FT
PROT
– 0 –
R/W
PROT
– 1 –
R/W
ARB – 79
UnReel
Belden


OXIDIZER
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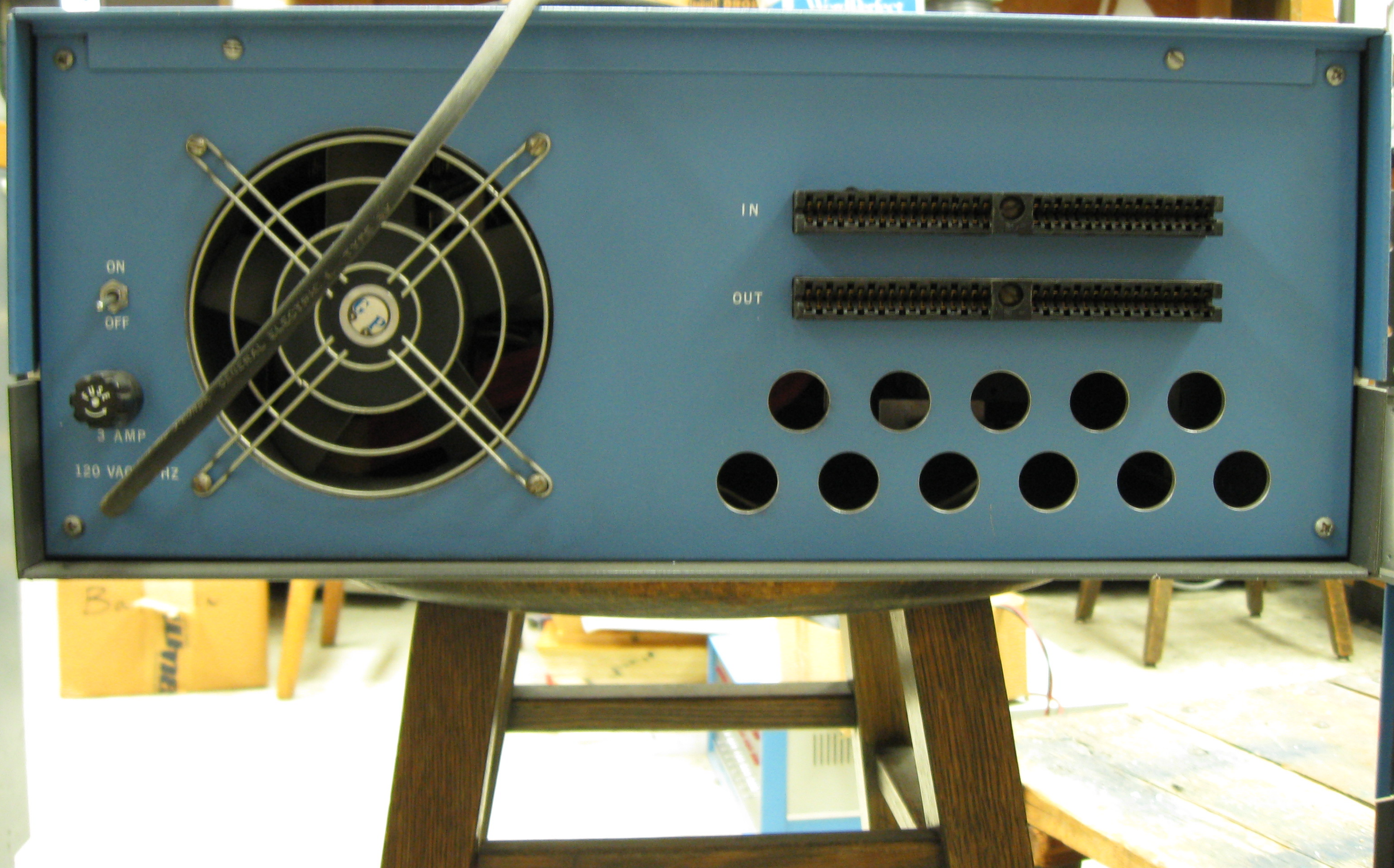
ARB - 79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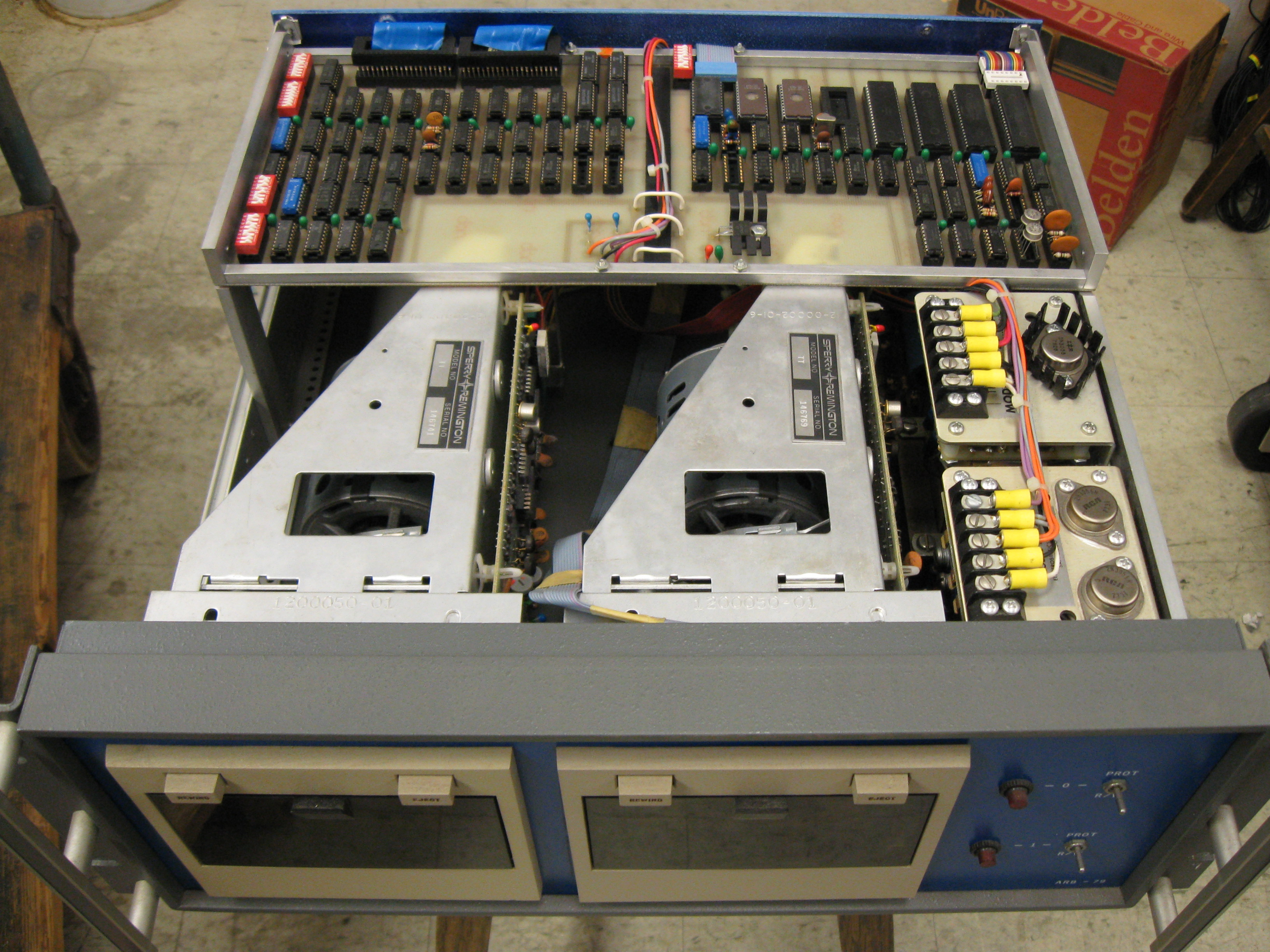
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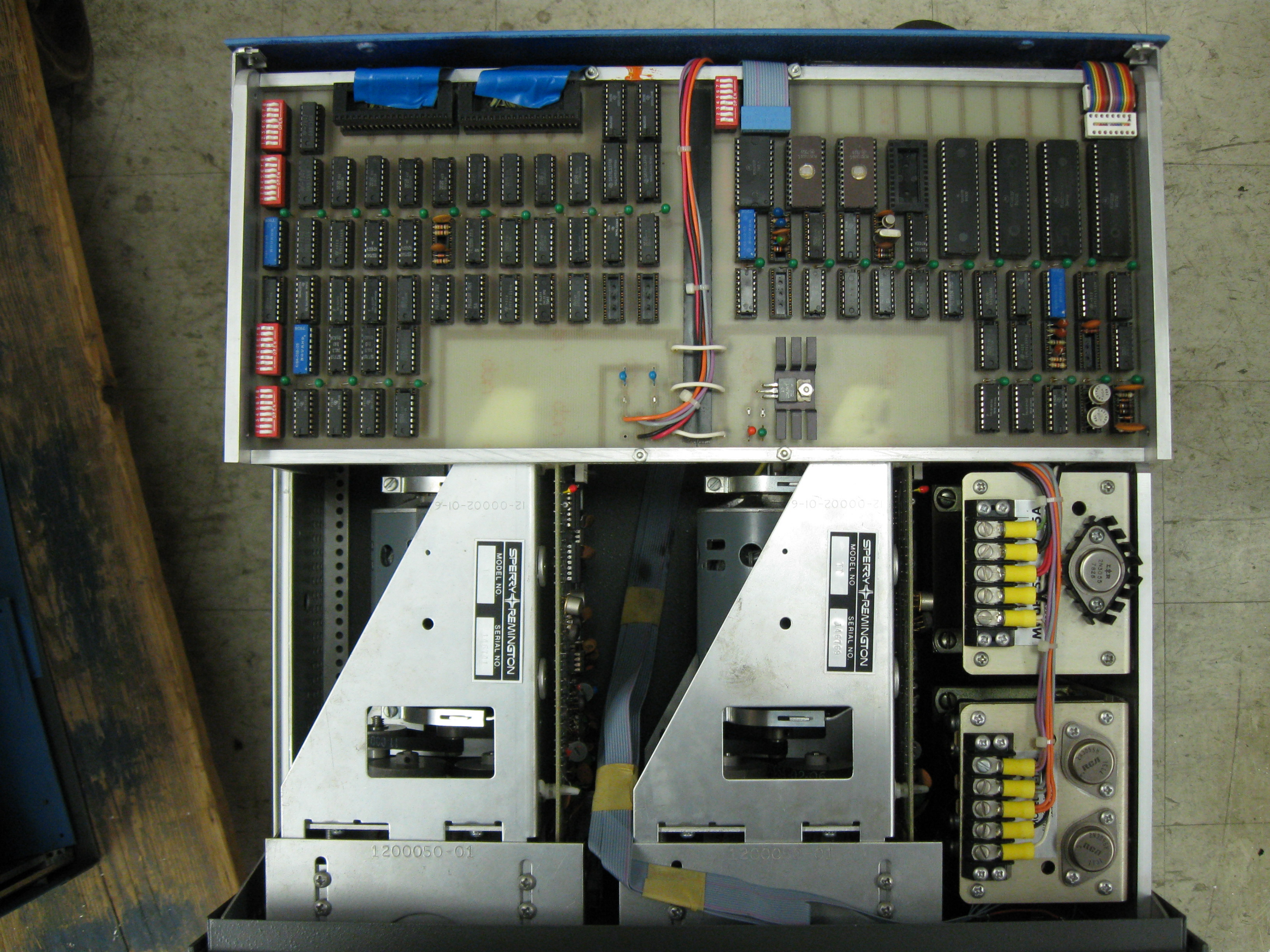
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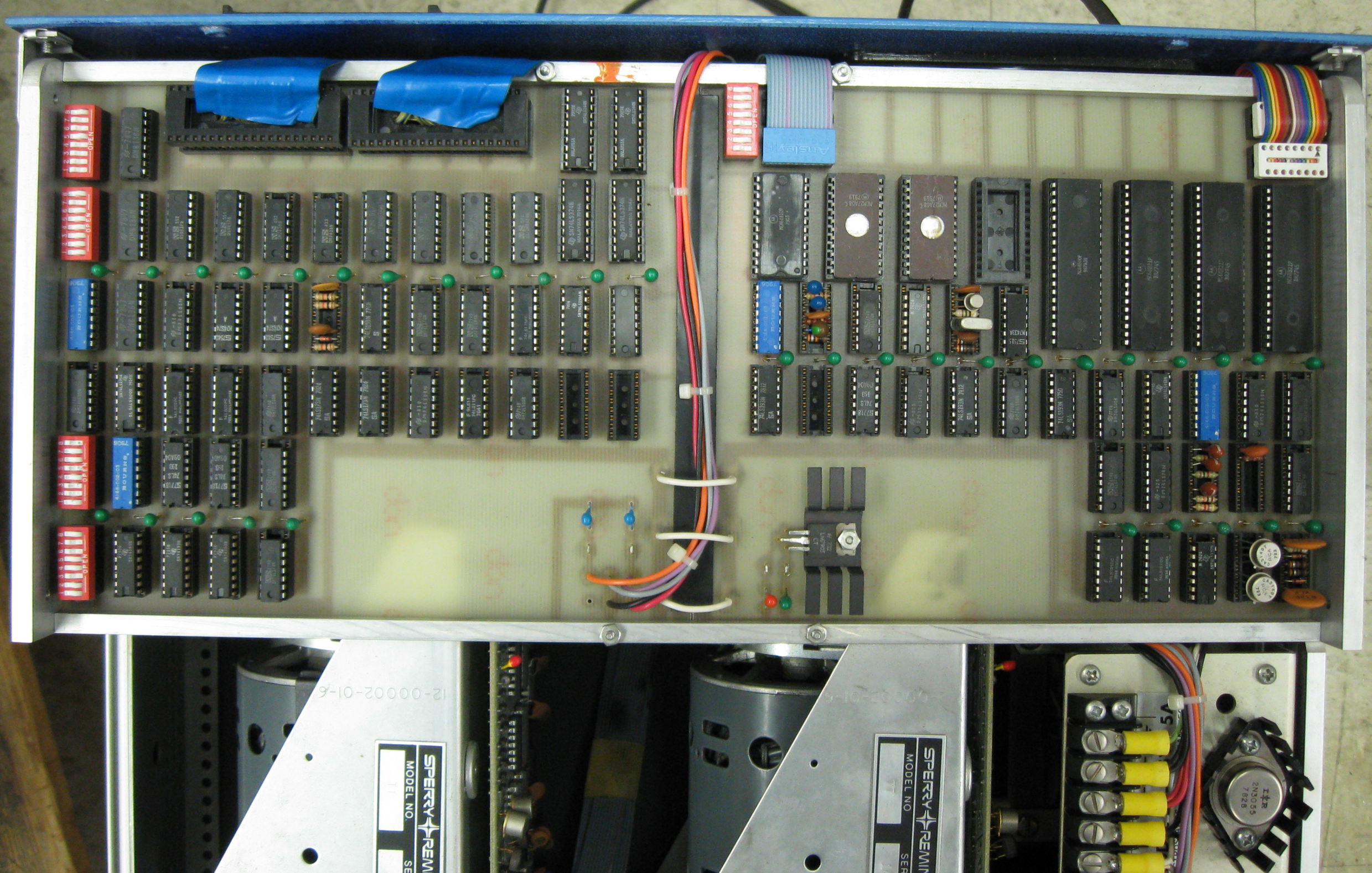
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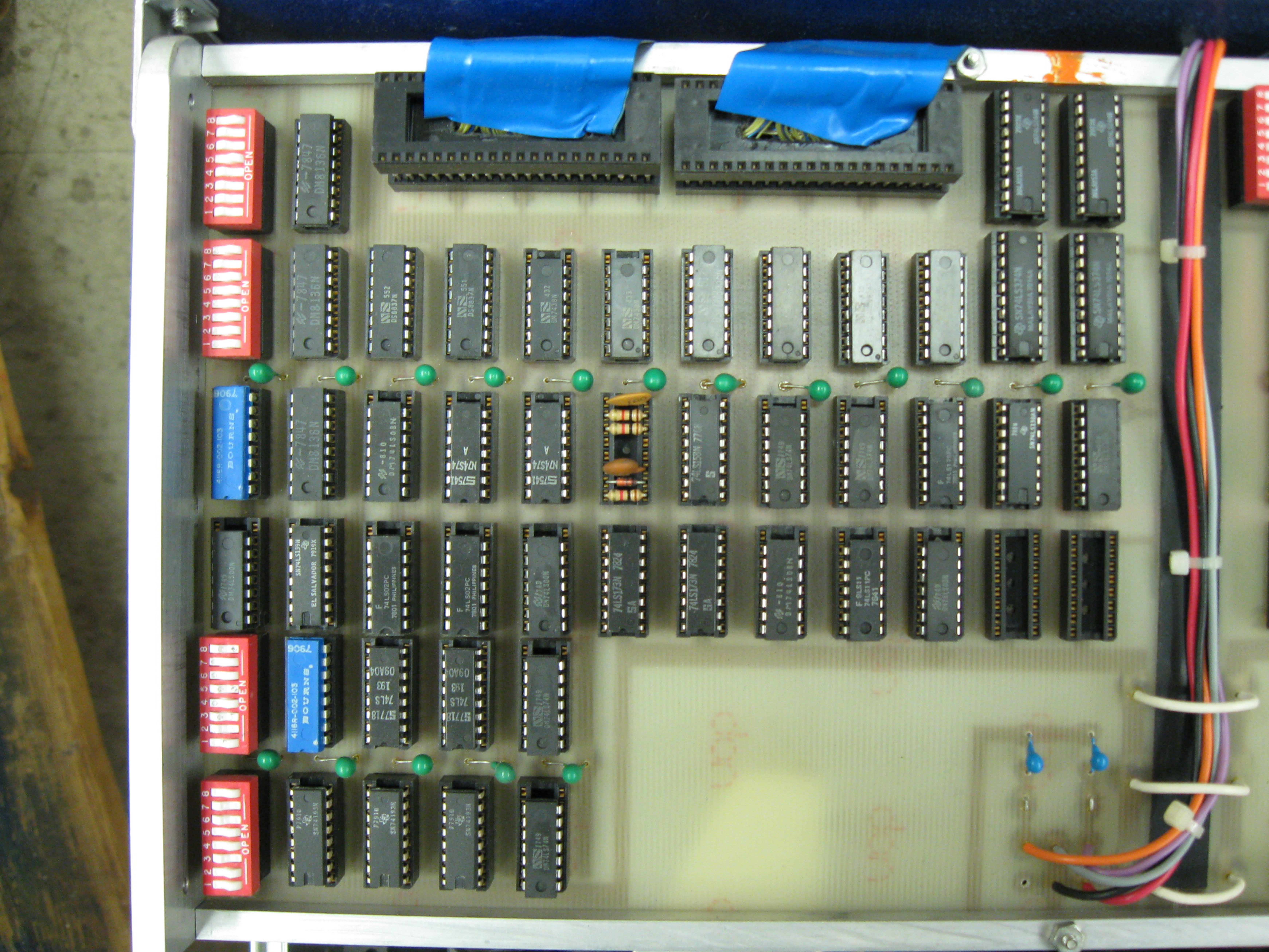
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DM7438N
7906
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4116R-002-103
-810
DM74LS08N
N74S74
A
S7541
74LS158N 7714
5
SN74LS139N
EL SALVADOR 7919X
F
74LS02PC
7801 PHILIPPINES
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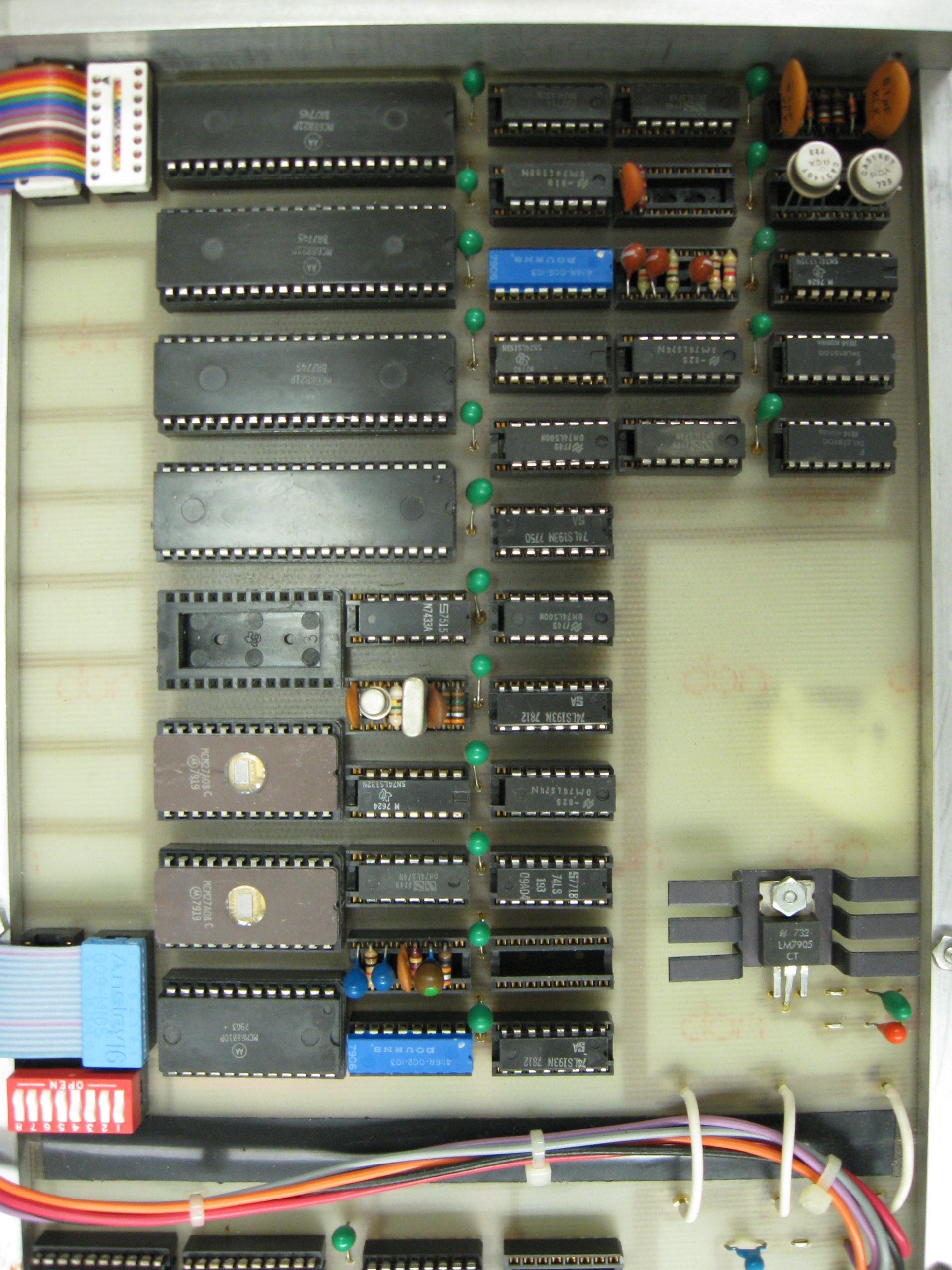
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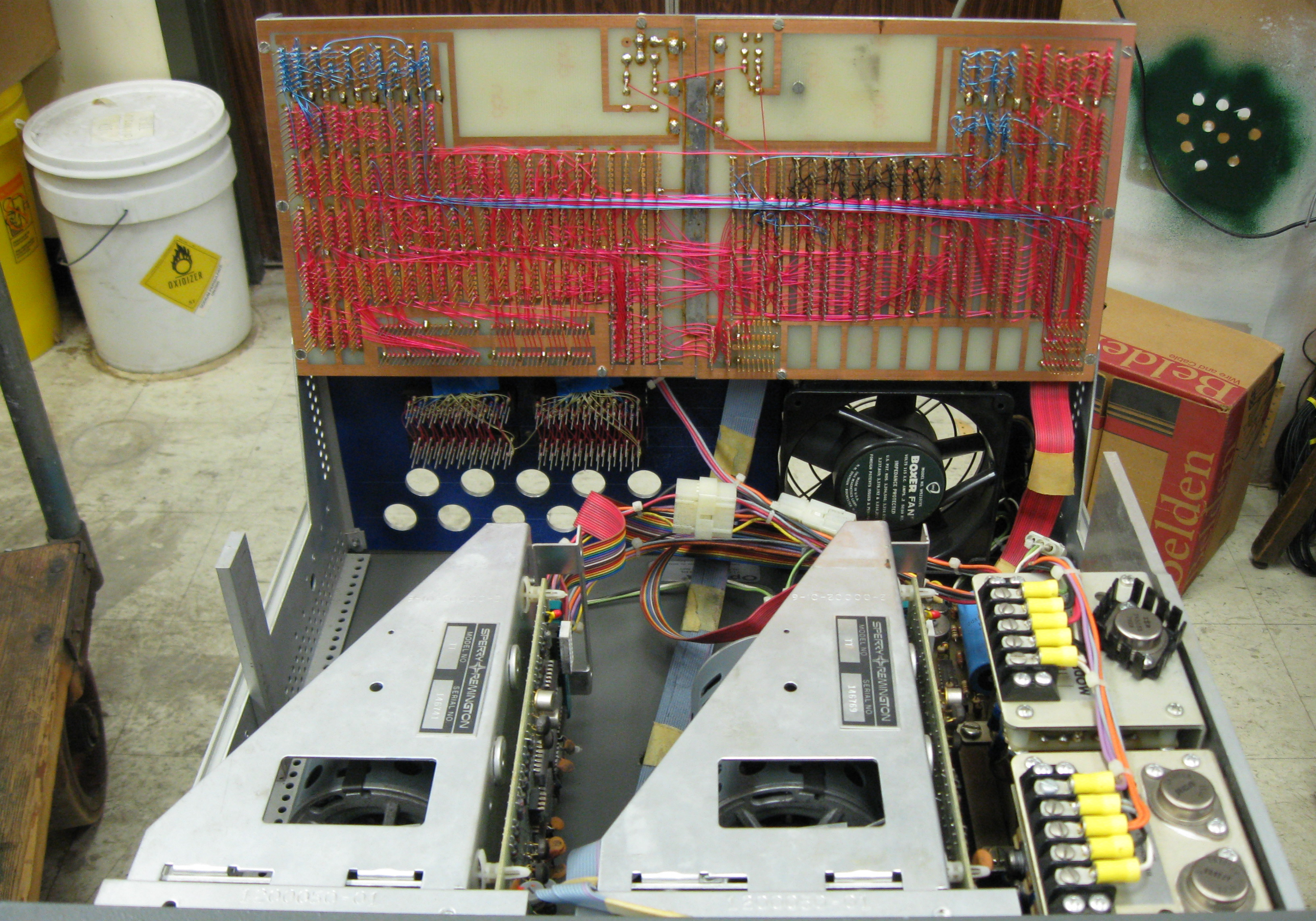
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Belden
Wire and Cable
BOXER FAN
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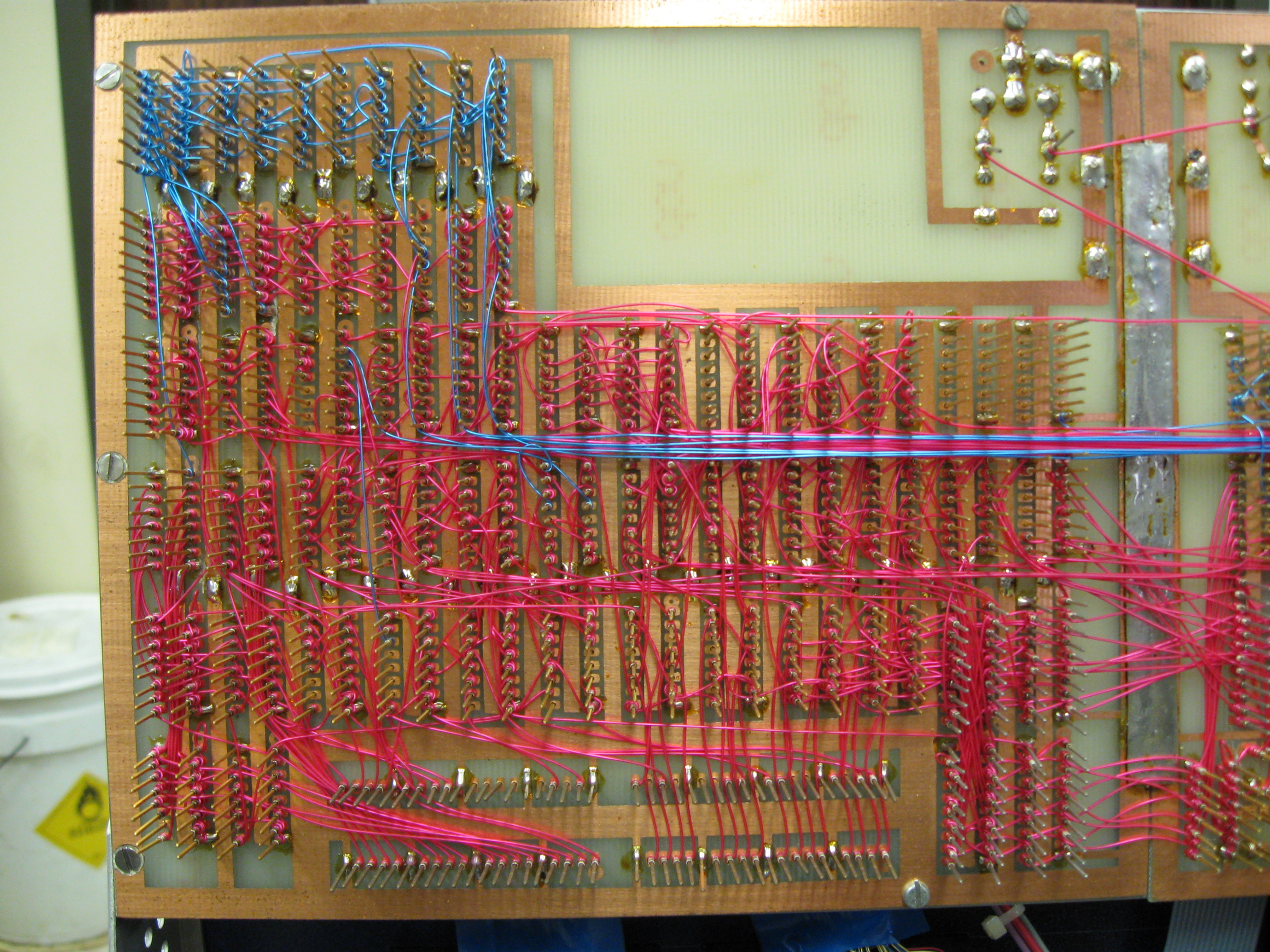
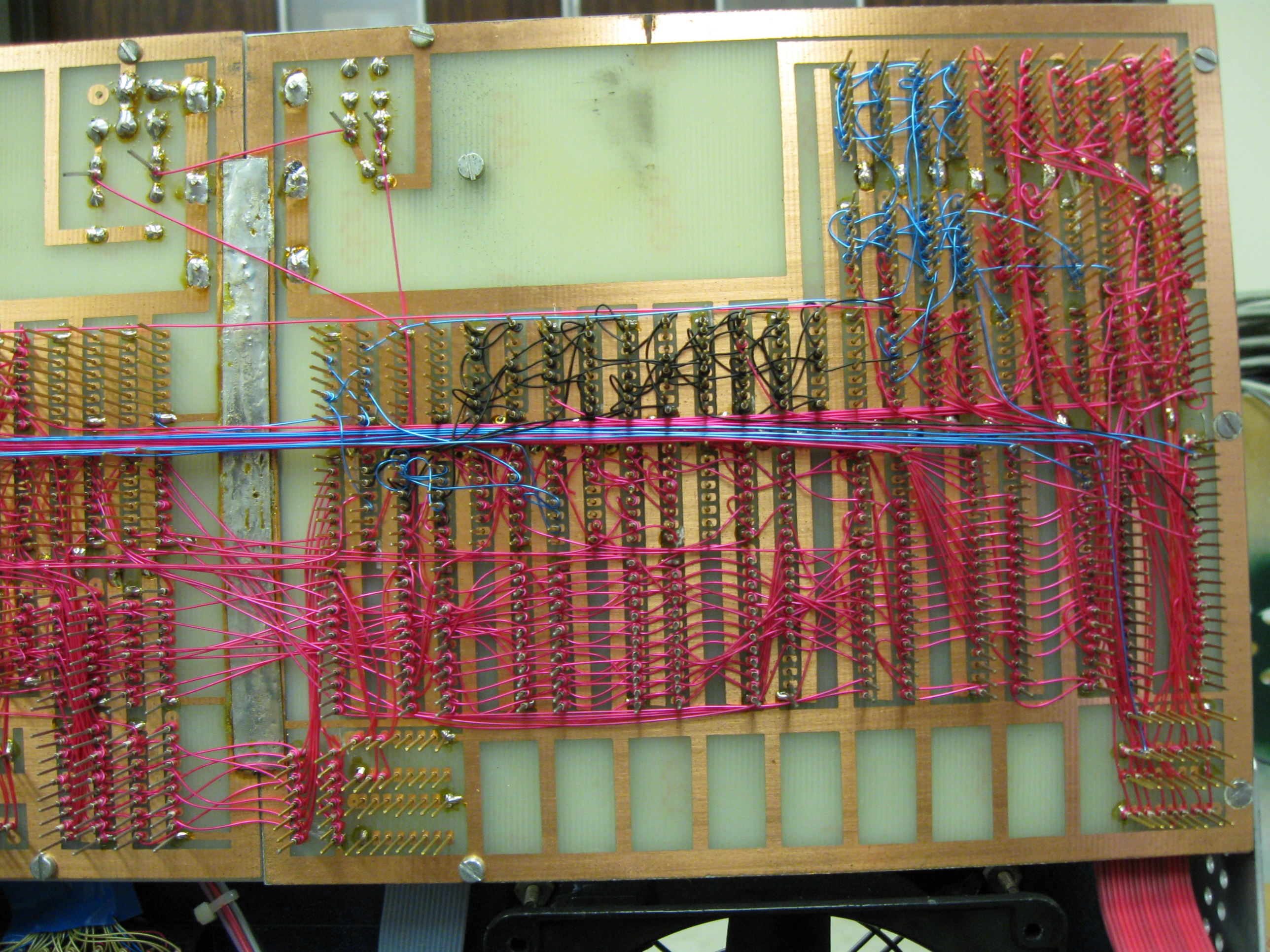
MODEL NO
SERIAL NO





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12-00002-01-6

SPERRY REMINGTON

MODEL NO. TT

SERIAL NO. 1A6741

1200050-01

12-00002-01-6

SPERRY REMINGTON

MODEL NO TT

SERIAL NO 1A6741

DC POWER SUPPLY
MODEL 20 24V .5A
ELECTROSTATICS, INC. SAN DIEGO