Dual Floppy Disc
& Controller

NATIONAL | 53-110
Made in U.S.A.

Dual Floppy Disc & Controller

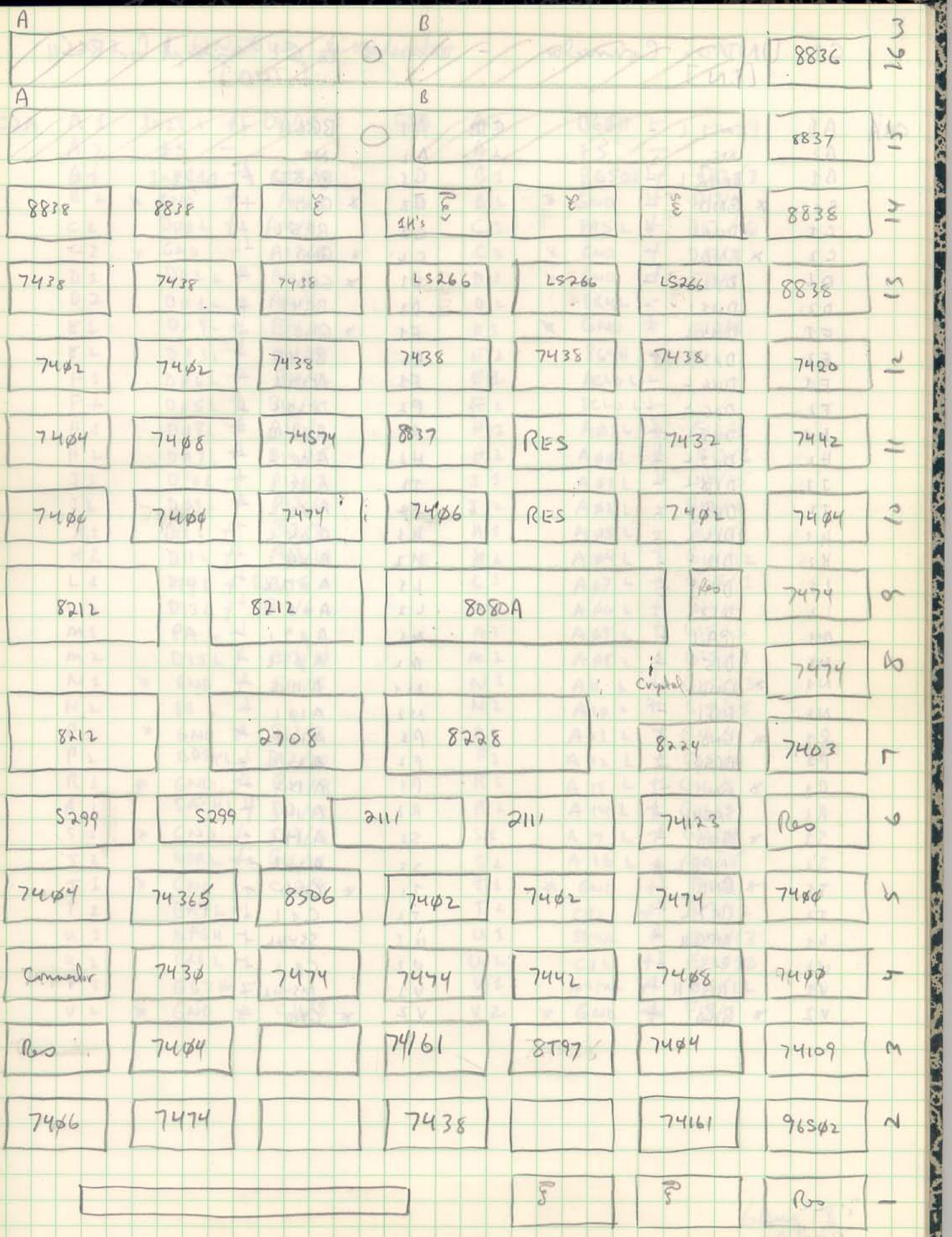
Basic Controller is adapted from the
FD-11 -100 Dual Floppy System
Manufactured by
Charles River Data Systems, Inc
235 Bear Hill Road
Waltham, Mass. 02154

6 Aug 78
ADD

Controller Board Layout —

A
C1
A
C2
8
74
7
7
7
74
C
R
7

6Aug78
ABD


A
B
C1
8836
A
B
C2
8837
8838
8838
8838
8838
7438
7438
7438
LS266
LS266
LS266
8838
74ø2
74ø2
7438
7438
7438
7438
7420
74ø4
74ø8
74S74
8837
RES
7432
7442
74ø0
74ø0
7474
74ø6
RES
74ø2
74ø4
8212
8212
8080A
7474
Crystal
7474
8212
2708
8228
8224
7403
S299
S299
2111
2111
74123
74ø4
74365
8506
74ø2
74ø2
7474
74ø0
Counter
743ø
7474
7444
7442
74ø8
74ø0
74161
8T97
74ø4
74109
74ø6
7474
7438
74161
96S02
A
B
C
D
E
F
G

C1 UNIBUS Connector [IN] - connected to C2 except for BG5H

C2A

C1A				C1B				
A1		INIT L	⊥	A1		BG6H	⊥	
A2		NC		A2		NC		
B1		INTR L	⊥	B1		BG5IH	⊥	D11/3
B2	*	GND	⊥	B2	*	GND	⊥	
C1		DØØL	⊥	C1		BR5L	⊥	
C2	*	GND	⊥	C2	*	GND	⊥	
D1		DØ2L	⊥	D1	*	GND	⊥	
D2		DØ1L	⊥	D2		BR4L	⊥	
E1		DØ4L	⊥	E1	*	GND	⊥	
E2		DØ3L	⊥	E2		BG4H	⊥	
F1		DØ6L	⊥	F1		ACLOL	⊥	
F2		DØ5L	⊥	F2		DCLOL	⊥	
H1		DØ8L	⊥	A1		AØ1L	⊥	
H2		DØ7L	⊥	H2		AØØL	⊥	
J1		D1ØL	⊥	J1		AØ3L	⊥	
J2		DØ9L	⊥	J2		AØ2L	⊥	
K1		D12L	⊥	K1		AØ5L	⊥	
K2		D11L	⊥	K2		AØ4L	⊥	
L1		D14L	⊥	L1		AØ7L	⊥	
L2		D13L		L2		AØ6L	⊥	
M1		PAL	⊥	M1		AØ9L	⊥	
M2		D15L	⊥	M2		AØ8L	⊥	
N1	*	GND	⊥	N1		A11L	⊥	
N2		PBL	⊥	N2		A1ØL	⊥	
P1	*	GND	⊥	P1		A13L	⊥	
P2		BBSYL	⊥	P2		A12L	⊥	
R1	*	GND	⊥	R1		A15L	⊥	
R2		SACKL	⊥	R2		A14L	⊥	
S1	*	GND	⊥	S1		A17L	⊥	
S2		NPRL	⊥	S2		A16L	⊥	
T1	*	GND	⊥	T1	*	GND	⊥	
T2		BR7L	⊥	T2		C1L	⊥	
U1		NPGH	⊥	U1		SSYNL	⊥	
U2		BR6L	⊥	U2		CØL	⊥	
V1		BG7H	⊥	V1		MSYNL	⊥	
V2	*	GND	⊥	V2	*	GND	⊥	

C2 UNIBUS Connector [OUT]

C2A	A 1		INIT L	+	D11/15	C2B	A 1		BGBIH	-	
	A 2		+5	-			A 2		+5	-	
	B 1		INTR L	+	C13/3		B 1		BG5OH	+	D12/3
	B 2	*	GND	+	A14/8		B 2	*	GND	+	D13/8
	C 1		DØØL	+	A14/4		C 1		BR5L	+	D12/6
	C 2	*	GND	+	A13/8		C 2	*	GND	+	D12/8
	D 1		DØ2L	+	A14/12		D 1	*	GND	+	E14/8
	D 2		DØ1L	+	A14/1		D 2		BR4L	-	
	E 1		DØ4L	+	B14/4		E 1	*	GND	+	E13/8
	E 2		DØ3L	+	A14/15		E 2		BG4H	-	
	F 1		DØ6L	+	B14/12		F 1		ACLOL	-	
	F 2		DØ5L	+	B14/1		F 2		DCLOL	-	
	H 1		DØ8L	+	A13/3		H 1		AØ1L	+	G13/1
	H 2		DØ7L	+	B14/15		H 2		AØØL	+	E12/6
	J 1		DIØL	+	A13/13		J 1		AØ3L	+	G14/15
	J 2		DØ9L	+	A13/6		J 2		AØ2L	+	G13/4
	K 1		DI2L	+	B13/3		K 1		AØ5L	+	G14/1
	K 2		DI1L	+	A13/14		K 2		AØ4L	+	G14/12
	L 1		DI4L	+	G13/15		L 1		AØ7L	+	G15/1
	L 2		DI3L	+	B13/6		L 2		AØ6L	+	G14/4
	M 1		PA L	-			M 1		AØ9L	+	G15/5
	M 2		DI5L	+	B13/14		M 2		AØ8L	+	G15/3
	N 1	*	GND	+	B14/8		N 1		A11L	+	G15/13
	N 2		PB L	-			N 2		AIØL	+	G15/15
	P 1	*	GND	+	B13/8		P 1		A13L	+	G16/11
	P 2		BDSYL	+	D12/10		P 2		A12L	+	G15/11
	R 1	*	GND	+	B12/8		R 1		A15L	+	G16/6
	R 2		SACKL	+	D12/13		R 2		A14L	+	G16/7
	S 1	*	GND	+	C13/8		S 1		A17L	+	G16/4
	S 2		NPRL	+	G16/14		S 2		A16L	+	G16/5
	T 1	*	GND	+	C12/8		T 1	*	GND	+	F14/8
	T 2		BR7L	-			T 2		C1L	+	G13/12
	U 1		NPGH	-			U 1		SSYNL	+	E12/13
	U 2		BR6L	-			U 2		CØL	+	E12/10
	V 1		BG7H	-			V 1		MSYNL	+	G16/12
	V 2	*	GND	+	C11/8		V 2	*	GND	+	F13/8

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Disc Drive connector

1		2	Dev Ø WRP	+ A3/15
3		4	WRPØ +	+ A5/1
5		6	Dev 1 WRP	+ A3/13
7		8	WRP1 +	+ A5/15
9		10		
11		12	DISK CHANGE	−
13		14		
15		16	IN USE L (Low Current?)	+ A2/6
17		18	HEAD LOAD L	+ A2/1Ø
19		20	INDEX L	+ E1/5
21		22	READY L	+ E1/7
23		24	SECTOR L	−
25	GND	26	Drive Ø Sel L	+ A2/14
27		28	Drive 1 Sel L	+ A2/12
29		30	Drive 2 Sel L	−
31		32	Drive 3 Sel L	−
33		34	Direction	+ A2/4
35		36	STep L	+ A2/2
37		38	write data	+ D2/1Ø
39		40	write gate	+ D2/13
41		42	TRACH ØØ L	+ E1/4
43		44	WRITE PROT L	+ E1/6
45		46	READ DATA L	+ E1/8
47		48	SEP DATA L	−
49		50	SEP CLOCH L	−

Standard Control instruction Set

Register/Vector Addresses

DCS — 777170_8
Disk Control & Status

DDB — 777172_8
Disk Data Buffer

Interrupt Vector — 264_8

Com

15

R

Error

Bit

0

1-3

Command & STATUS Register 777170₈ (addressing always by word)

R = Read Only ; W = Write Only
R/W = read/write

Error
initialize
Transfer Request
Interrupt Enable
Drive
Unit select
Function
Go

Bit	Function
0	Go Bit — initiates the selected operation
1-3	Function Code — selects operation to be performed
	0 0 0 — Fill buffer
	0 0 1 — empty buffer
	0 1 0 — Write a sector
	0 1 1 — read a sector
	1 00 — Special Functions
	1 01 — Read status
	1 1 0 — Write deleted Data Sector
	1 1 1 — Read Error register

Bit	FUNCTION
4	Unit Select Bit - selects which of two disks for selected operation
5	Done Bit - indicates completion of operation if interrupt enable is asserted then an interrupt will occur when Bit is set
6	Interrupt Enable - enables program interrupt
7	Transfer request Bit - this bit indicates Controller is ready to transfer data
8-13	unused :-
14	Initialize - initializing Disk system a) reset done b) move head of dev 1 to Track 04 c) move head of dev 0 to Track 00 d) clear error & status register e) set initialize done f) sets drive ready when drive 0 ready g) Sector 1 of Track 0 of dev 0 is read into buffer
15	Error - any error sets bit cleared by initialize or new command

Disk Data Buffer Register 777172_8

This register has 5 funktions determined by the protocal of the operation.

The register maybe read when the controller is not executing a funktion.

When a funktion is being executed the DDB register may be read or written to only when the TR bit is set

Data Buffer

serves as a 1 byte data path between the CPU and the Controller when filling or emptying the internal 128 Byte buffer

Sector Address Register

which of 26_{10} sectors are to used in a read/write command

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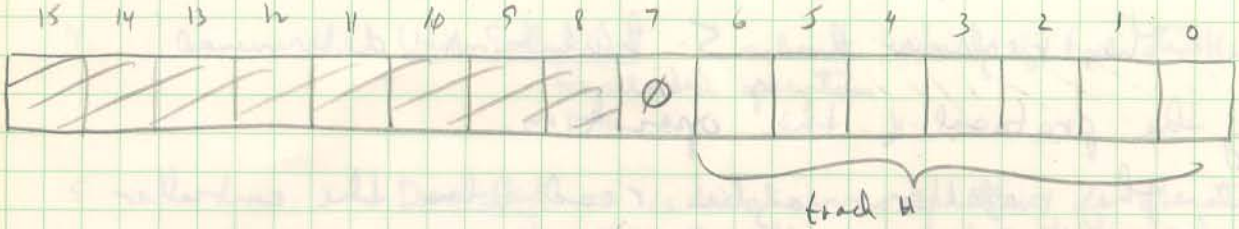
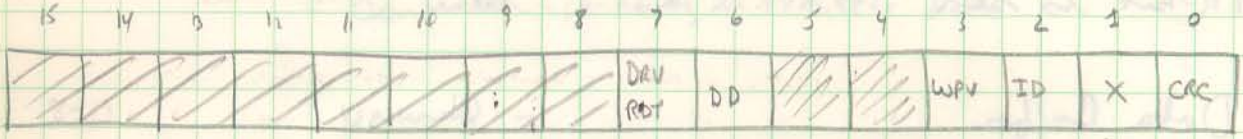
Track Address Register



selects track # $0-76_{10}$ which is to be used in a read write operation

STATUS Register



Bit	Description
0	a cyclic redundancy error has occurred in a read operation
1	DEC system error (Not implemented)
2	initialize DONE - Indicates initialize routine
3	write protect violation - an attempt was made to write on a protected diskette
6	deleted data mark found during a read, or last operation was write deleted data mark
7	bit indicates selected drive is ready

valid only after a read status function / a initialization

Error Code Register

accessed by a read error function

coding (octal)	Meaning
10	Drive 0 failed to see home on initialization
40	tried to access a track greater than 76
60	data error during self-diagnostic
70	desired sector could not be found after looking at 52 headers (2 revolutions)
120	preamble could not be found
130	preamble found but no I/O mark found within allotted time.
140	CRC error on what was thought to be a header
150	the header track address of a good header does not match with desired track

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DRD

Command Functions And Their Protocols

* Fill Data Buffer (ØØØ) *

This function is used to fill the internal 128 byte buffer with data from the CPU. The contents of the buffer are normally written onto the disk by a subsequent command.

procedure

(1) store function code ØØØ and go bit in DCS

(2) wait for TR bit to set in DCS

(3) transfer 1 byte of data to DDB

(4) repeat steps (2) & (3) until 128 bytes have been transferred

the Done bit will set upon completion

* Empty Data Buffer (ØØ1) *

this function is used to empty the 128 byte internal buffer into the CPU

procedure

(1) store function code ØØ1 and go bit in DCS

(2) wait for TR bit to set in DCS

(3) read 1 byte of data from DDB

(4) repeat steps (2) & (3) for 128 bytes

the Done bit will set upon completion

* Write Sector (010)

This function writes the contents of the buffer onto the disk

procedure

(1) store function code 010 and go bit into DCS
(2) check for TR bit set
(3) transfer sector address to DDB
(4) check for TR bit set
(5) transfer track address to DDB
(6) at completion Done bit will be set and DDB will contain the status register

* Read Sector (011)

This function reads a diskette sector into the internal buffer

procedure: same as write sector!!

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* Special Function Code (100)

three added features:

Bootstrap:	ØØ1001	11_8
Diagnostic:	Ø1ØØ1	31_8
Format	1Ø1ØØ1	51_8

Bootstrap – will boot from disk Ø when using a system disk

procedure:

(1) Load Address 777170_8

(2) set Enable/Halt to Halt

(3) START

(4) deposit 11_8

(5) Load address $Ø_8$

(6) Enable

(7) START

Diagnostic – writes and reads all sectors on diskette

on error – routine halts – check error register for cause

routine will continue indefinitely if no errors are found

procedure:

(1) place Test diskette in drive and set select switch to #5

(2) Load Addrs 777170_8

(3) Deposit 400008

(4) Examine

(5) Deposit 31_8

(6) drive will now step through each track on unit 5 testing all sectors. after reaching track 76 it goes to track 0 and repeats

FORMAT — the format allows reformatting of the diskette - previous data is lost

procedure:

(1) place diskette in drive and set select switch to #5

(2) Load Addrs 777170_8

(3) Deposit 40000_8

(4) Examine

(5) Deposit 51_8

(6) the controller will format the disk ~1 minute

(7) upon completion use the Diagnostic to write data fields on the diskette

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* Read STATUS (101)

When this function is executed the status register will be loaded into the DDB

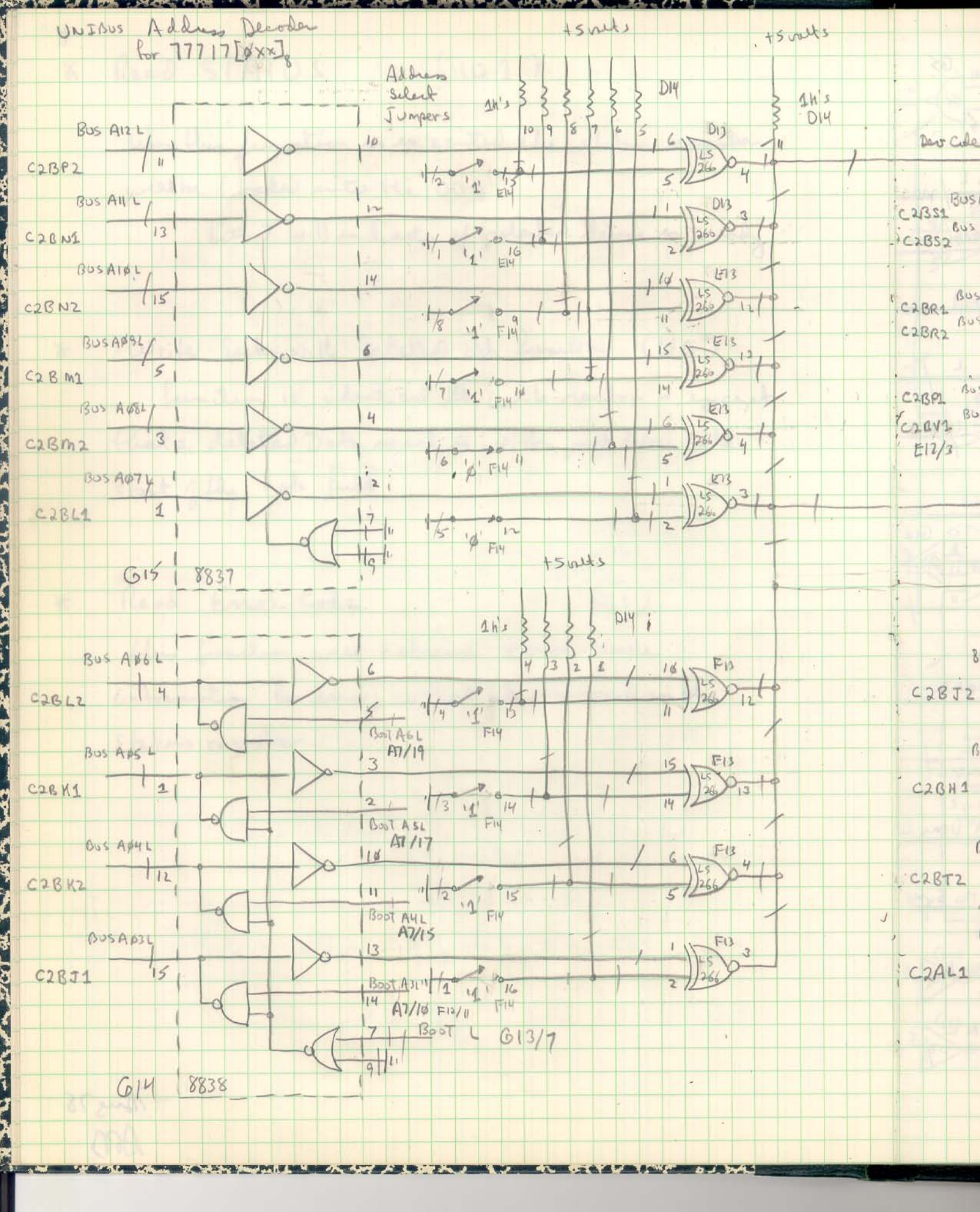
bit 7 will indicate if selected device is ready

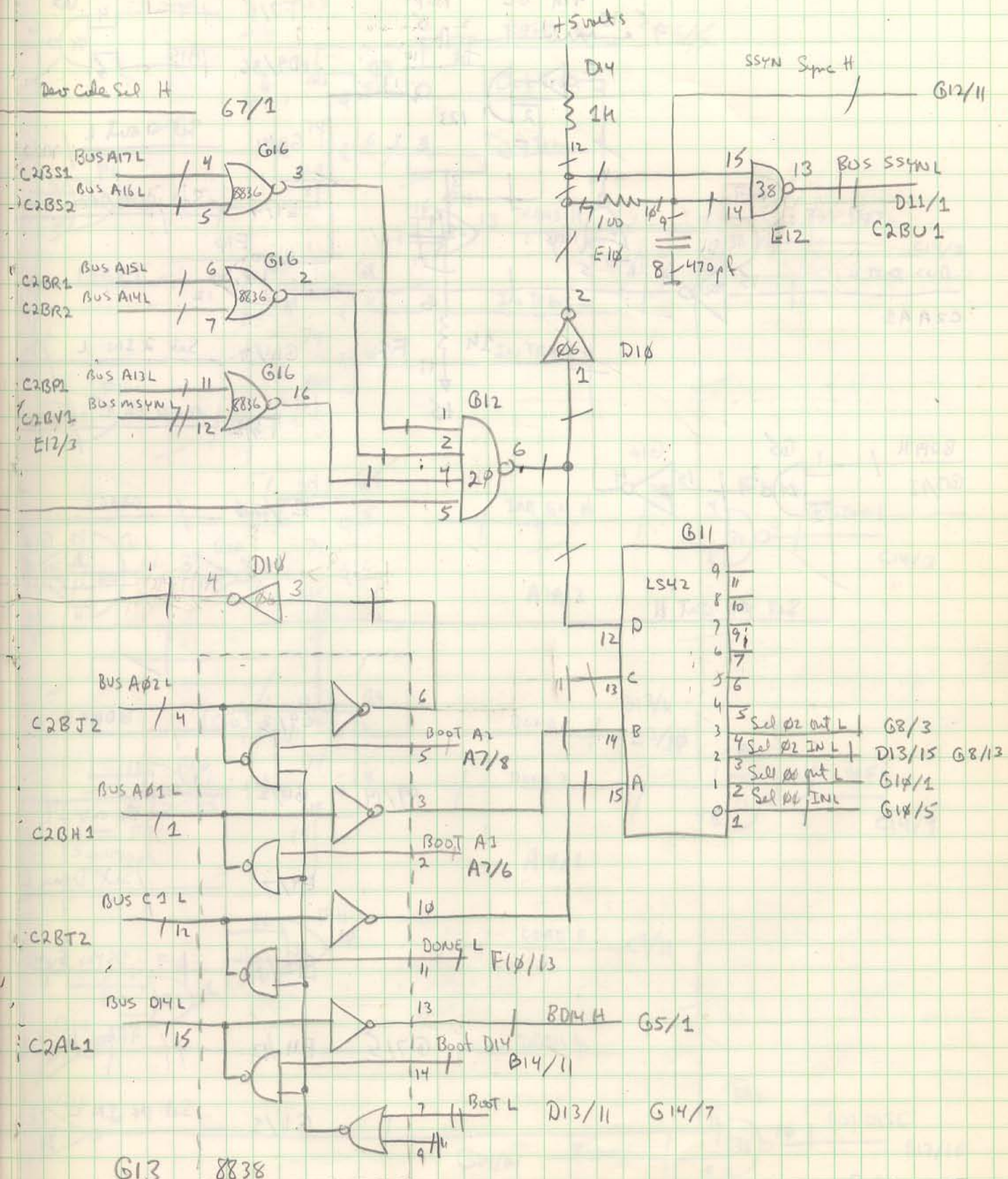
* Write Sector with Deleted Data function (110)

function is identical to write sector - except that a deleted Data mark is written just before the start of the data field

* Read Error Code (111)

this function will retrieve error code information for errors without bits assigned in the status register


UNIBUS Address Decoder
for 777170[0xx]8
+5 volts
+5 volts
Address Select Jumpers
1K's
D14
1K's D14
Bus A12 L
C2BP2
Bus A11 L
C2BN1
Bus A10 L
C2BN2
Bus A09 L
C2BM1
Bus A08 L
C2BM2
Bus A07 L
C2BL1
G15 8837
+5 volts
1K's
D14
Bus A06 L
C2BL2
Boot A6L
A7/19
Bus A05 L
C2BK1
Boot A5L
A7/17
Bus A04 L
C2BK2
Boot A4L
A7/15
Bus A03 L
C2BJ1
Boot A3L
A7/16 F12/11
Boot L G13/7
G14 8838
Dev Code
C2BS1
C2BS2
C2BR1
C2BR2
C2BP1
C2BV1
E12/3
C2BJ2
C2BH1
C2BT2
C2AL1


+5 volts
D14
1H
SSYN Sync H
G12/11
Dev Code Sel H
67/1
BUS A17L
C2BS1
BUS A16L
C2BS2
G16
8836
BUS A15L
C2BR1
BUS A14L
C2BR2
BUS A13L
C2BP1
BUS MSYNL
C2BV1
E12/3
G12
2Ø
D10
Ø6
E10
100
16pf
470pf
E12
38
BUS SSYNL
D11/1
C2BU1
G11
LS42
Sel Ø2 out L
Sel Ø2 IN L
Sel Ø0 out L
Sel Ø0 IN L
G8/3
D13/15
G8/13
G10/1
G10/5
D10
BUS AØ2L
C2BJ2
BUS AØ1L
C2BH1
BUS C1L
C2BT2
BUS D14L
C2AL1
BOOT A2
A7/8
BOOT A1
A7/6
DONE L
F10/13
BDI4H
G5/1
Boot DI4
B14/11
BOOT L
D13/11
G14/7
G13
8838
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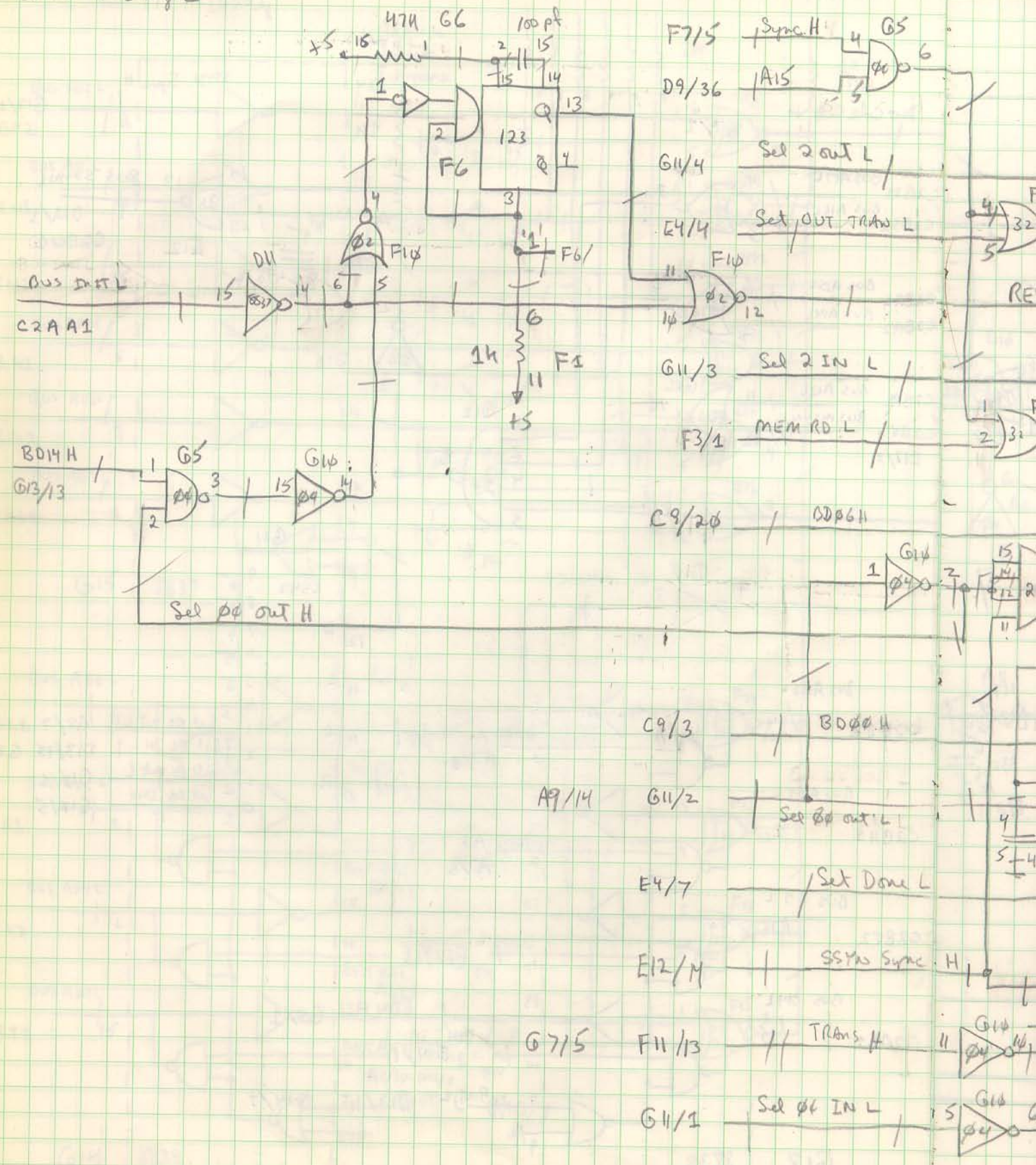
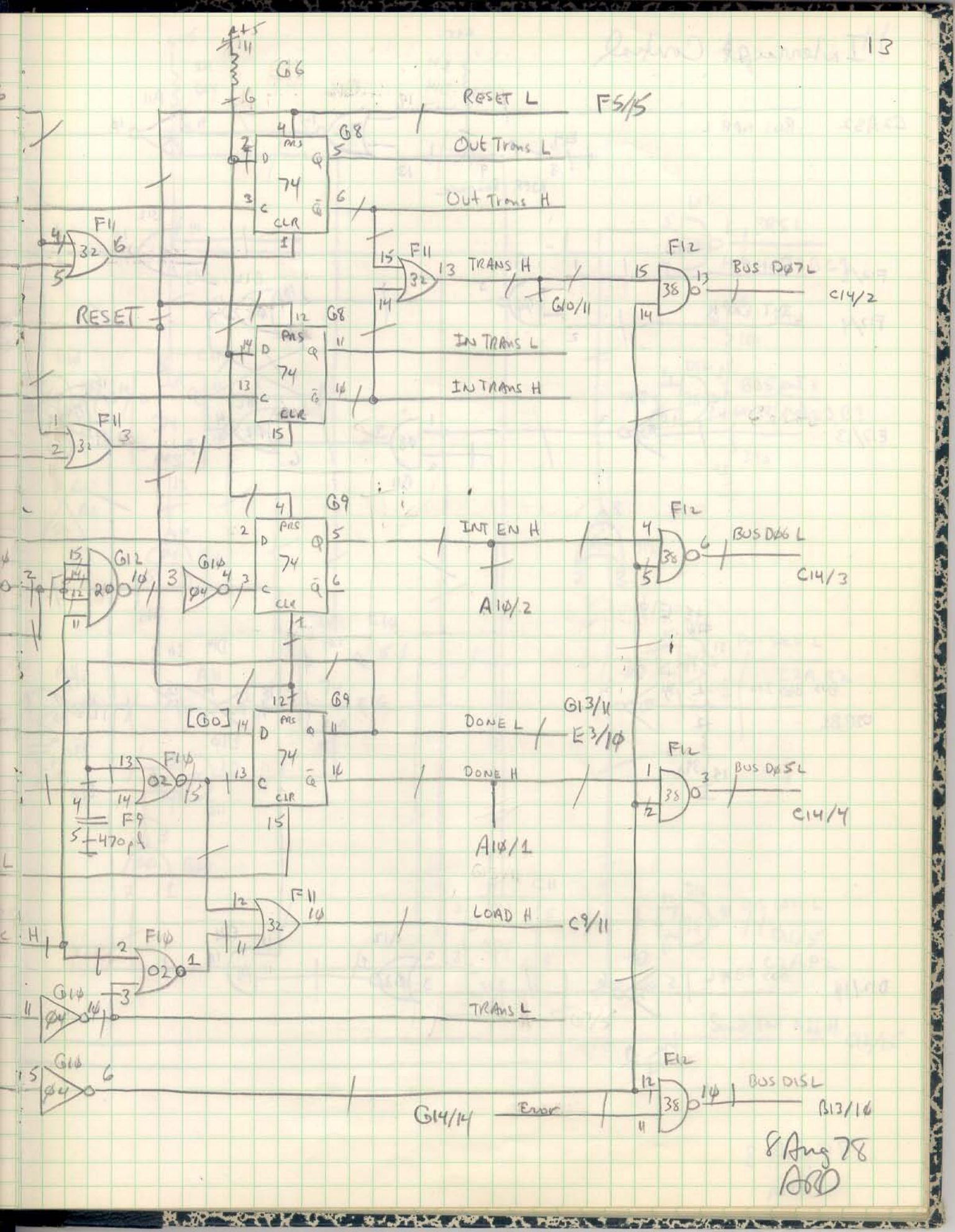
Control Logic




G6
RESET L
F5/15
G8
OUT TRANS L
OUT TRANS H
F11
TRANS H
G10/11
F12
BUS D07L
C14/2
RESET
G8
IN TRANS L
IN TRANS H
G9
INT EN H
BUS D06 L
C14/3
A10/2
G12
G10
[G0]
DONE L
G13/11
E3/10
DONE H
BUS D05L
C14/4
A10/1
F9
470pf
F10
LOAD H
C9/11
TRANS L
BUS D15L
B13/16
G14/14
Error
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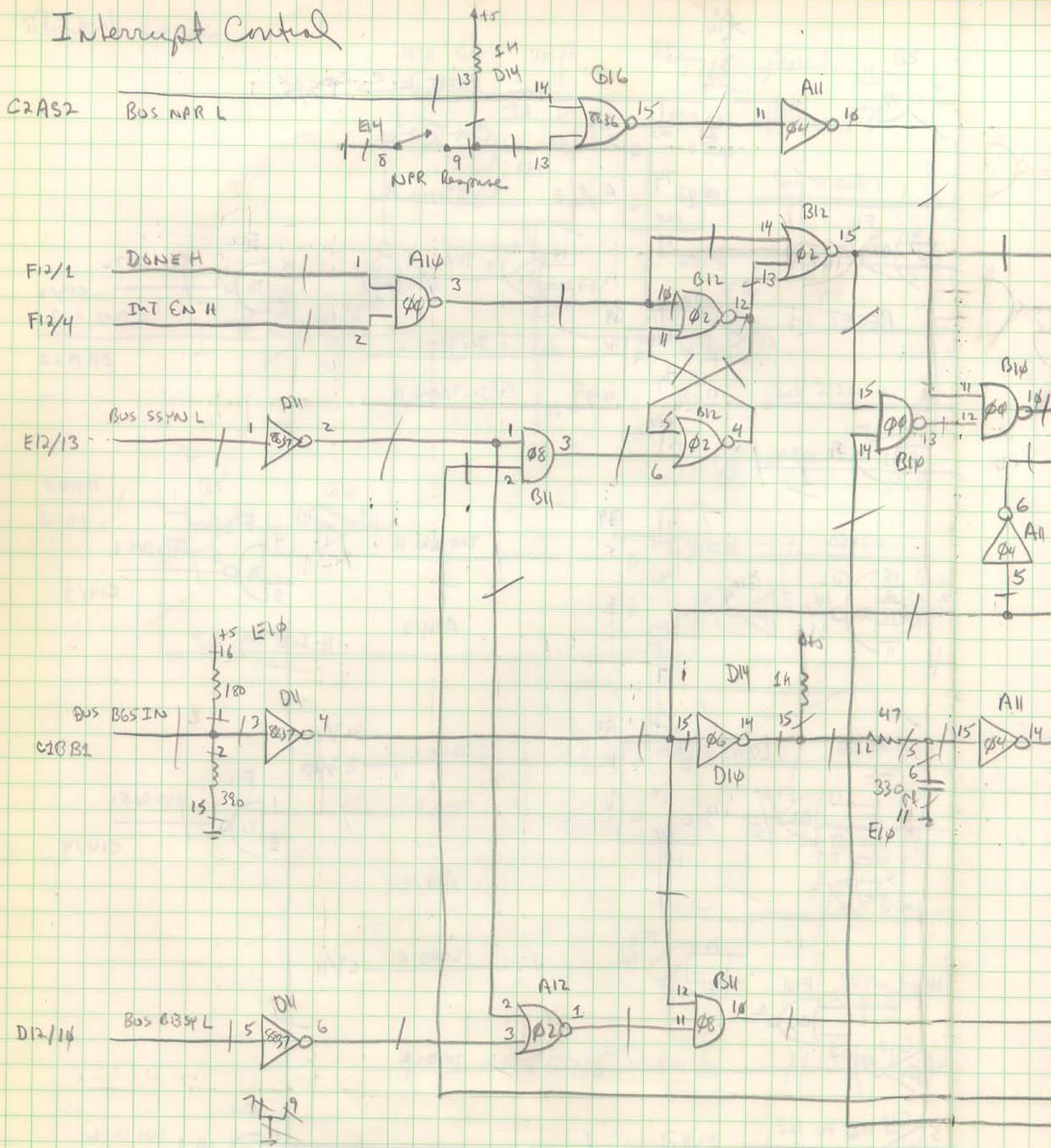
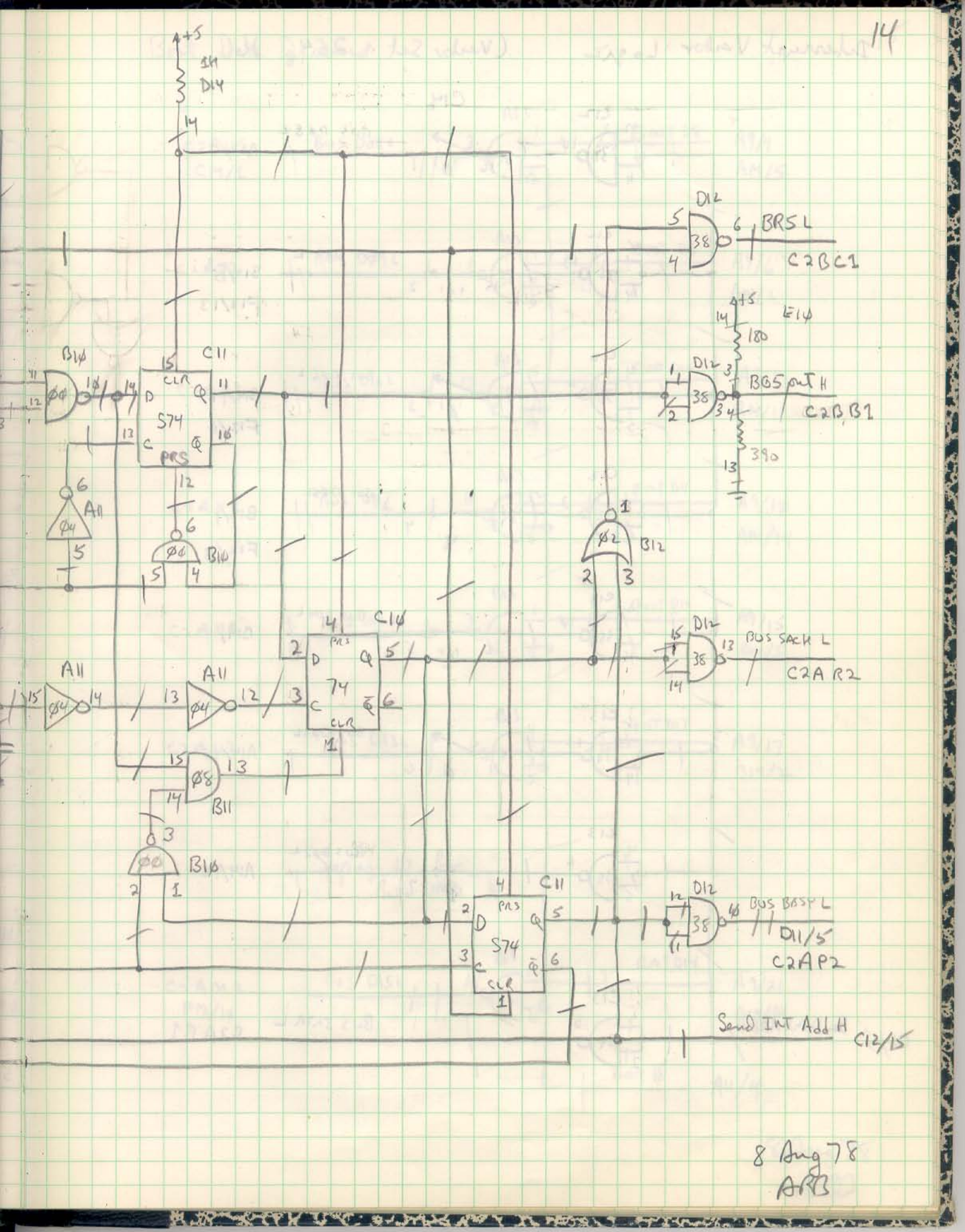
Interrupt Control




+5
1K
D14
14
D12
5
38
6
BRSL
C2BC1
4
+5
E14
14
180
B14
C11
15
CLR
D
Q
11
S74
C
PRS
13
12
6
A11
B14
5
4
1
B12
2
3
C14
4
PRS
2
D
Q
5
74
A11
A11
C
CLR
11
15
13
B11
3
B14
2
1
C11
4
PRS
2
D
Q
5
S74
3
C
CLR
1
D12
1
3
BGSACKH
C2B,B1
2
3
4
390
13
D12
15
13
BUS SACK L
C2A R2
14
D12
12
10
BUS BASY L
D11/5
C2AP2
11
Send INT Add H
C12/15

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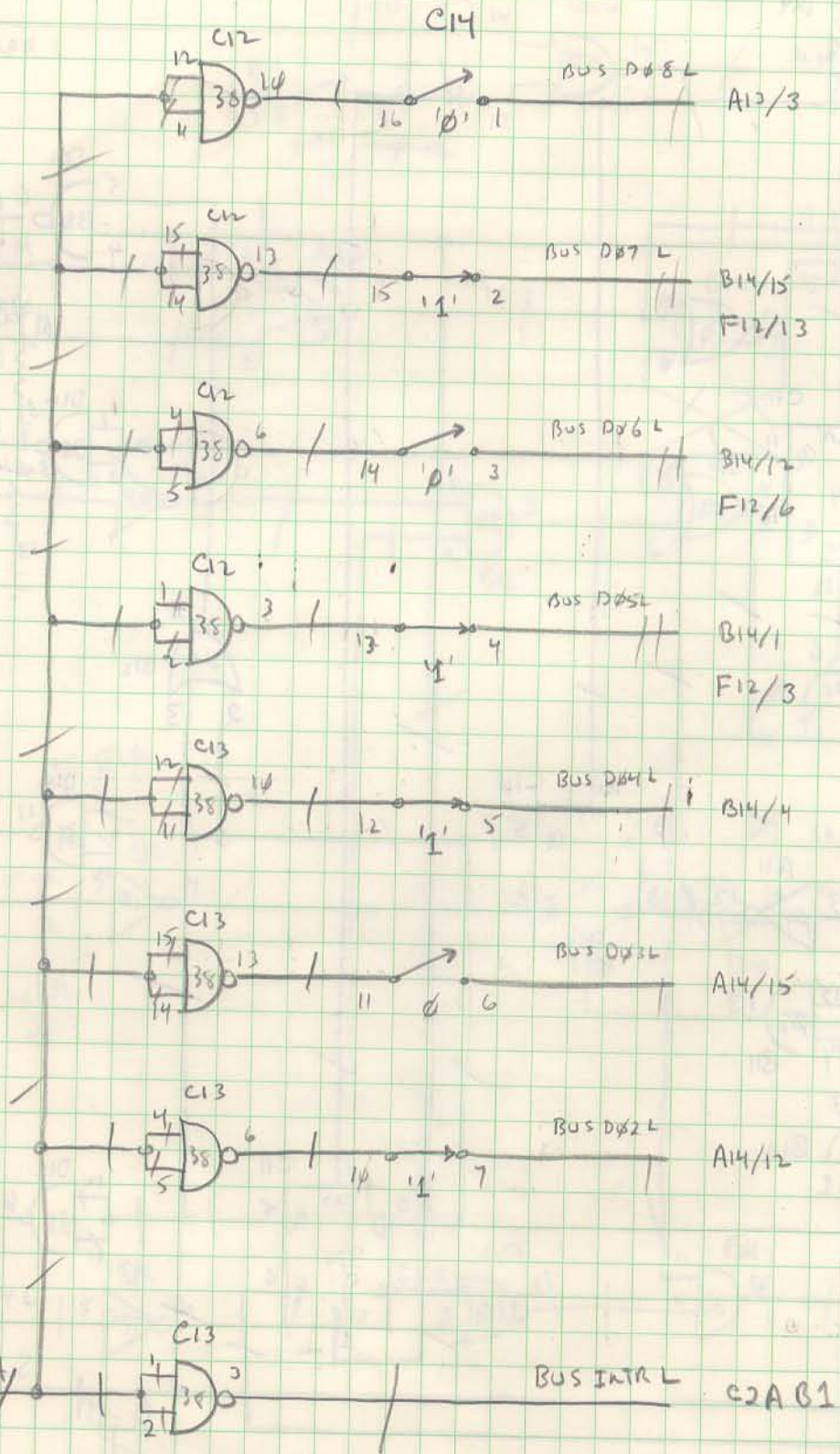
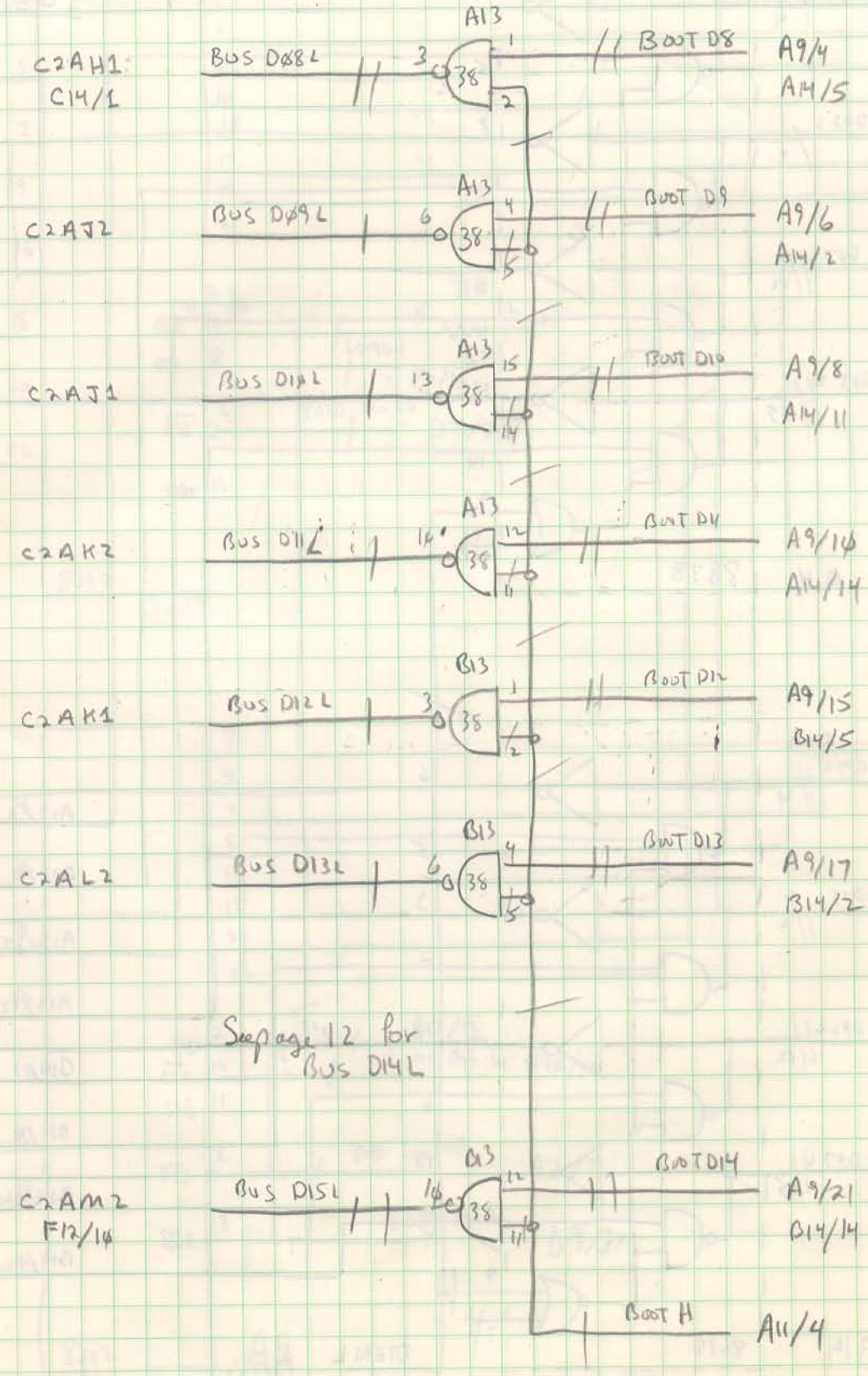
Interrupt Vector Logic (Vector Set = 264$_8$)



Boot Data Drivers



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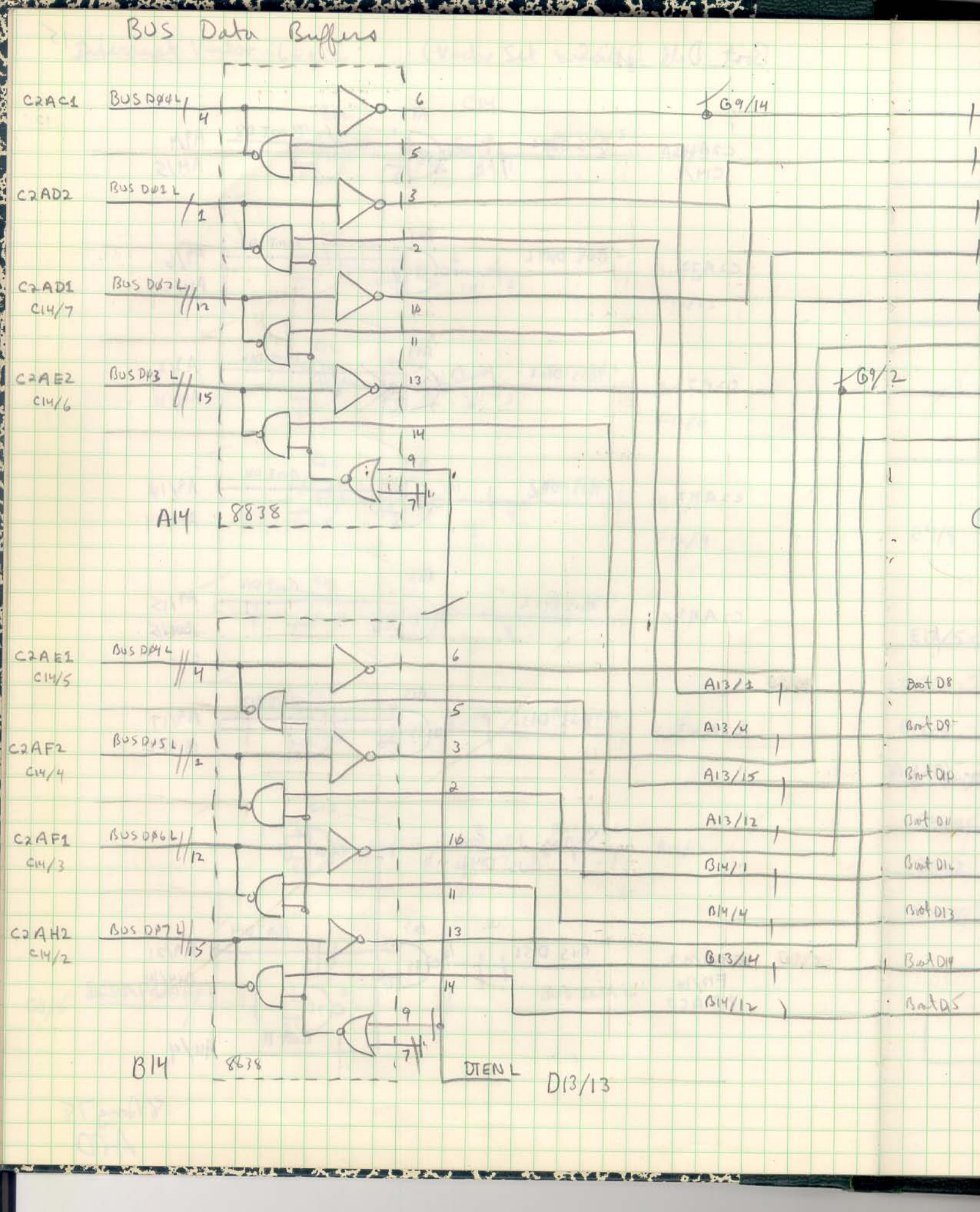
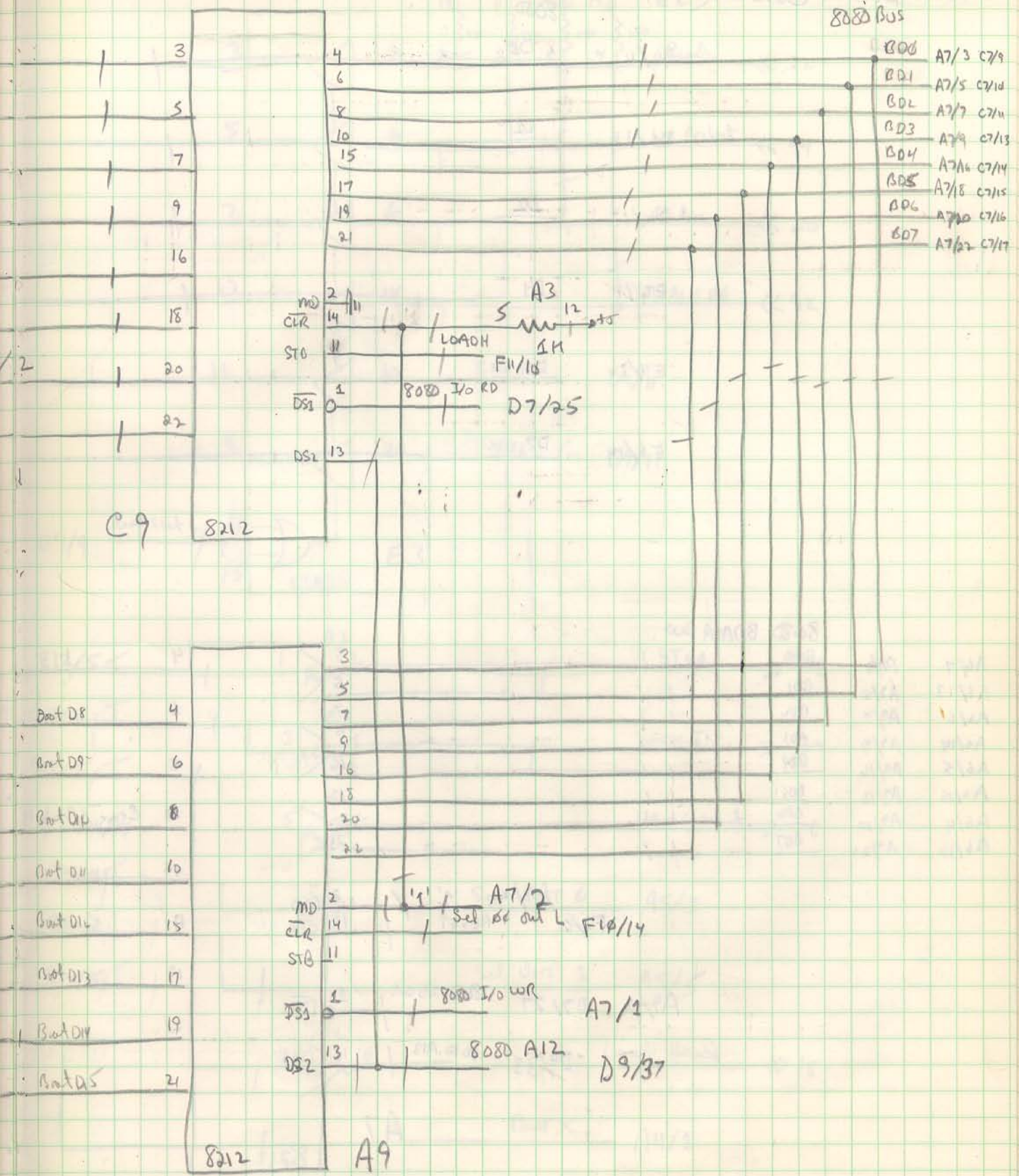
BUS Data Buffers




8080 Bus
BD0 A7/3 C7/9
BD1 A7/5 C7/10
BD2 A7/7 C7/11
BD3 A7/9 C7/13
BD4 A7/16 C7/14
BD5 A7/18 C7/15
BD6 A7/20 C7/16
BD7 A7/22 C7/17
A3
LOADH
FII/16
8080 I/O RD
D7/25
C9
8212
Boot D8
Boot D9
Boot D10
Boot D11
Boot D12
Boot D13
Boot D14
Boot D15
'1'
A7/2
Set
FIP/14
8080 I/O WR
A7/1
8080 A12
D9/37
A9
8212

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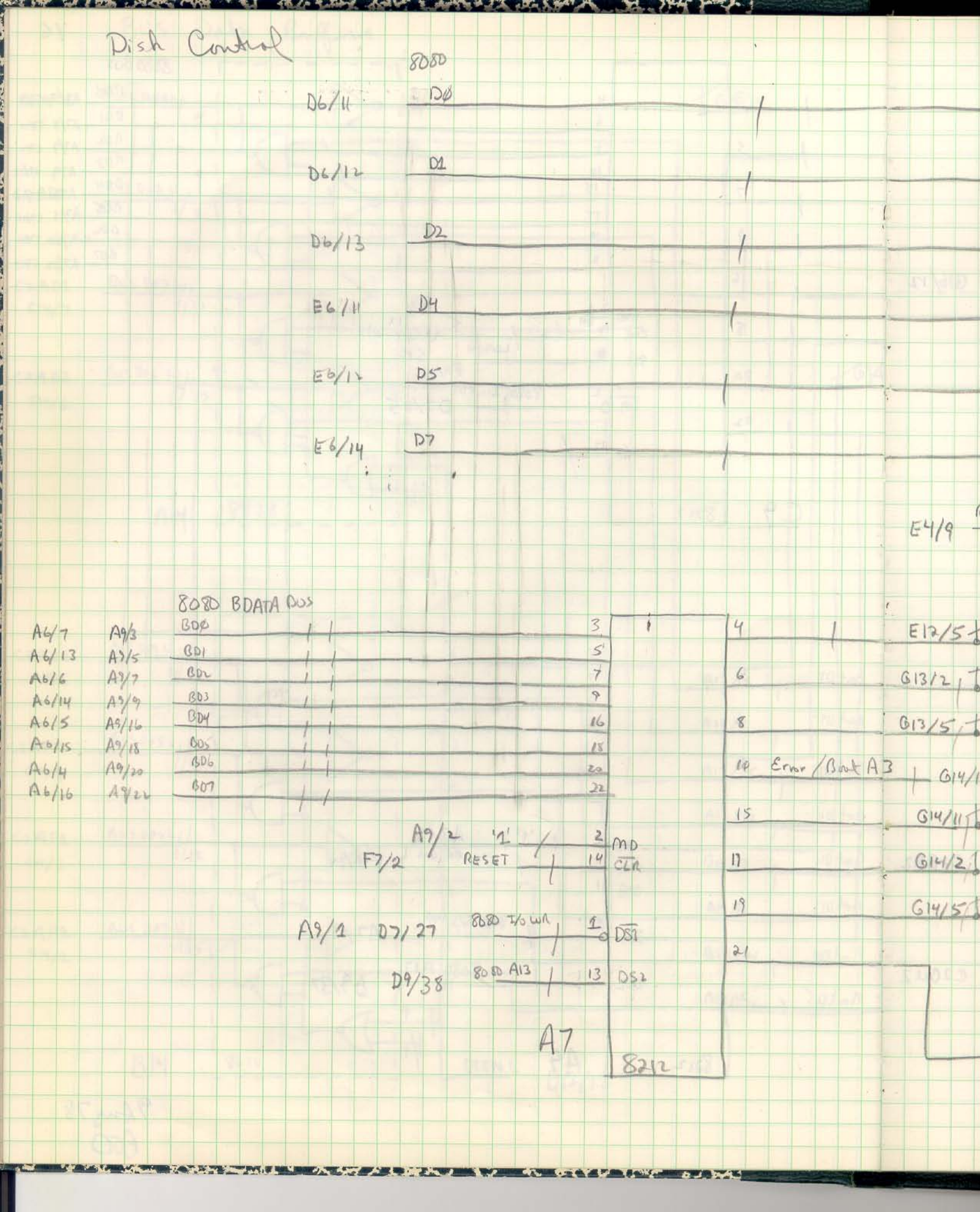
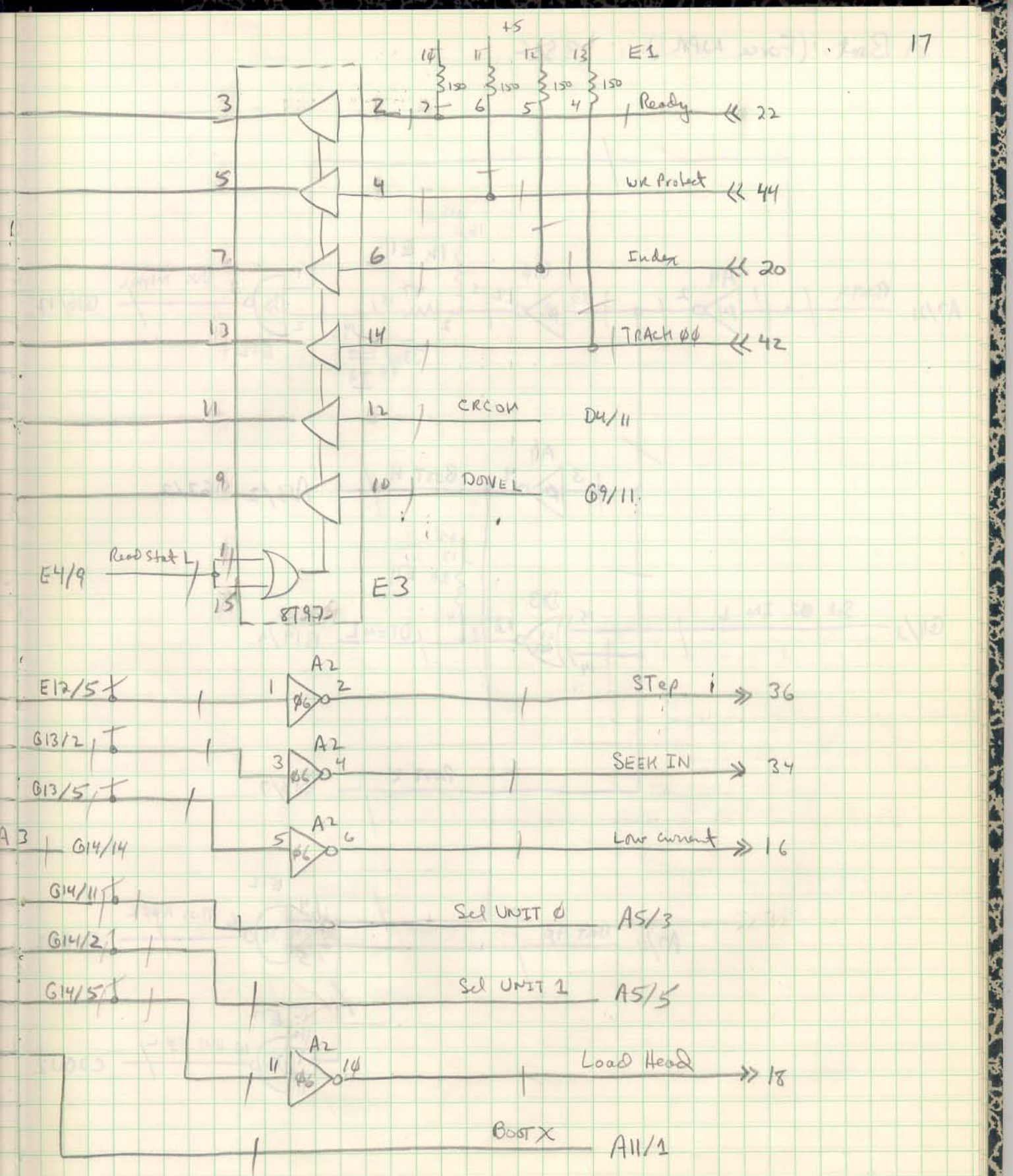
AOD

Disk Control




+5
10
11
12
13
E1
150
150
150
150
3
2
7
6
5
4
Ready
22
5
4
Wr Protect
44
7
6
Index
20
13
14
TRACK 00
42
11
12
CRCOM
D4/11
9
10
DONEL
G9/11
E4/9
Read Stat L
11
15
8T97
E3
A2
E12/5
1
2
STep
36
G13/2
3
4
SEEK IN
34
G13/5
A3
G14/14
5
6
Low current
16
G14/11
Sel UNIT 0
A5/3
G14/2
G14/5
Sel UNIT 1
A5/5
11
10
Load Head
18
BootX
A11/1

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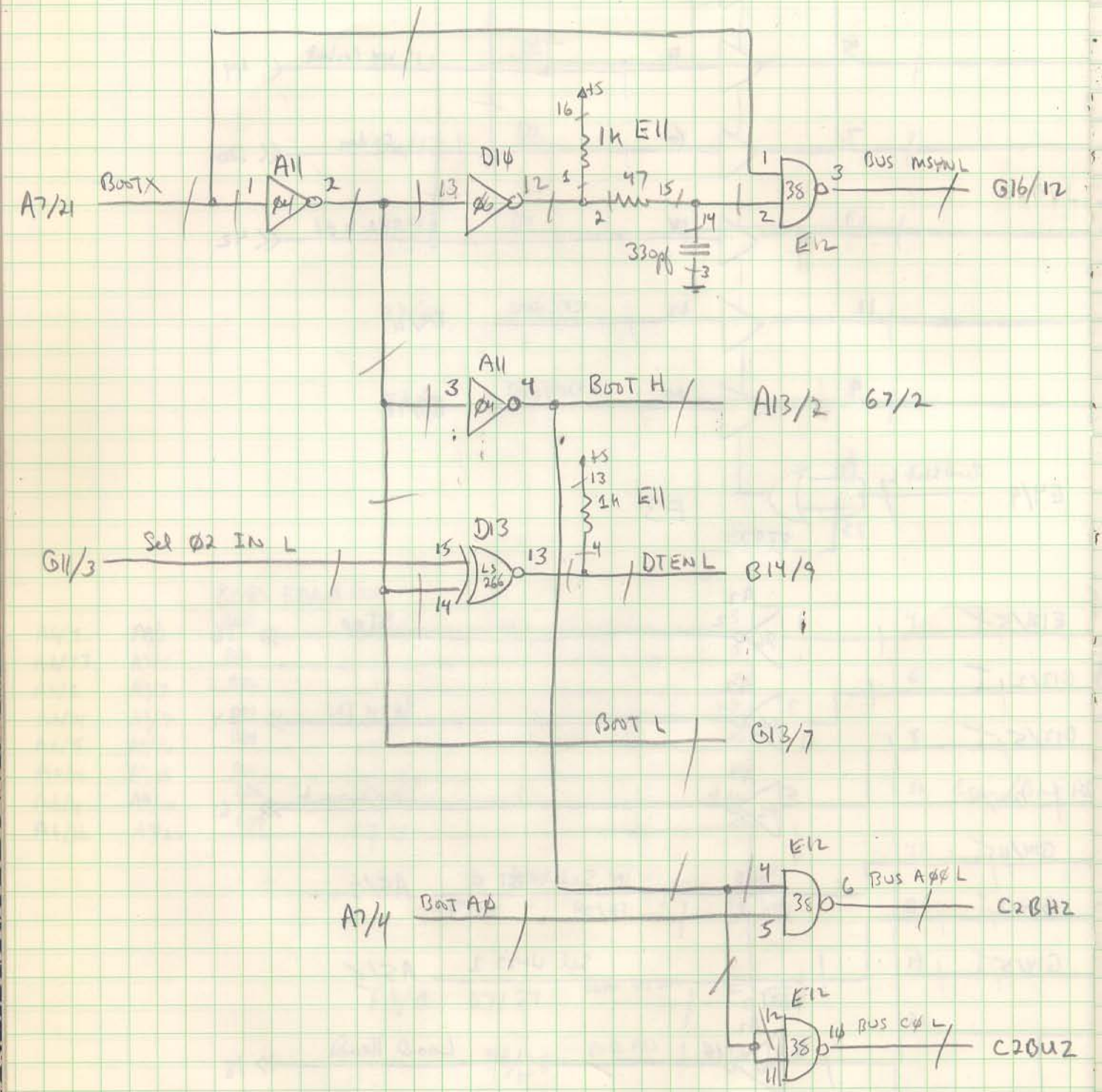
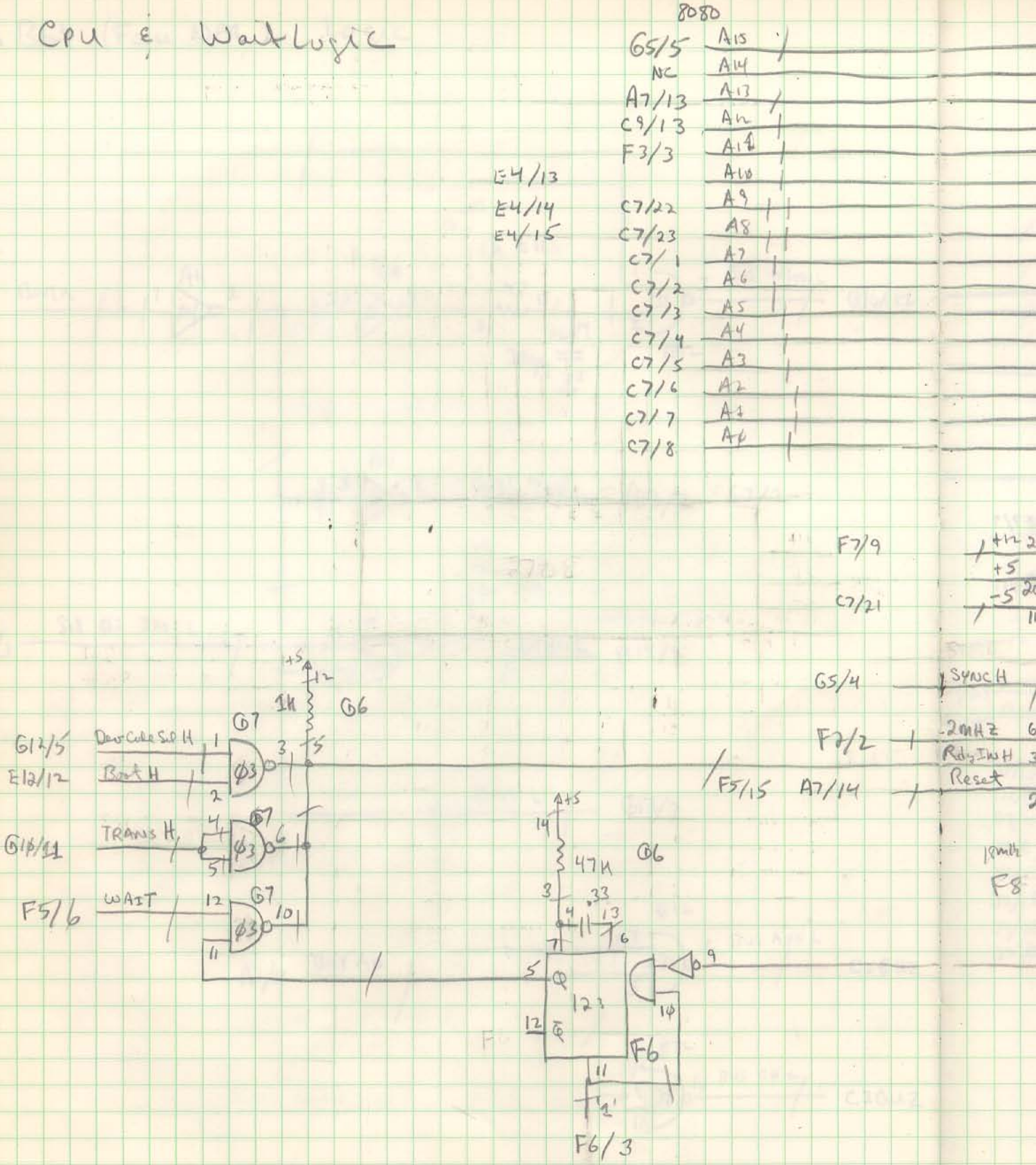
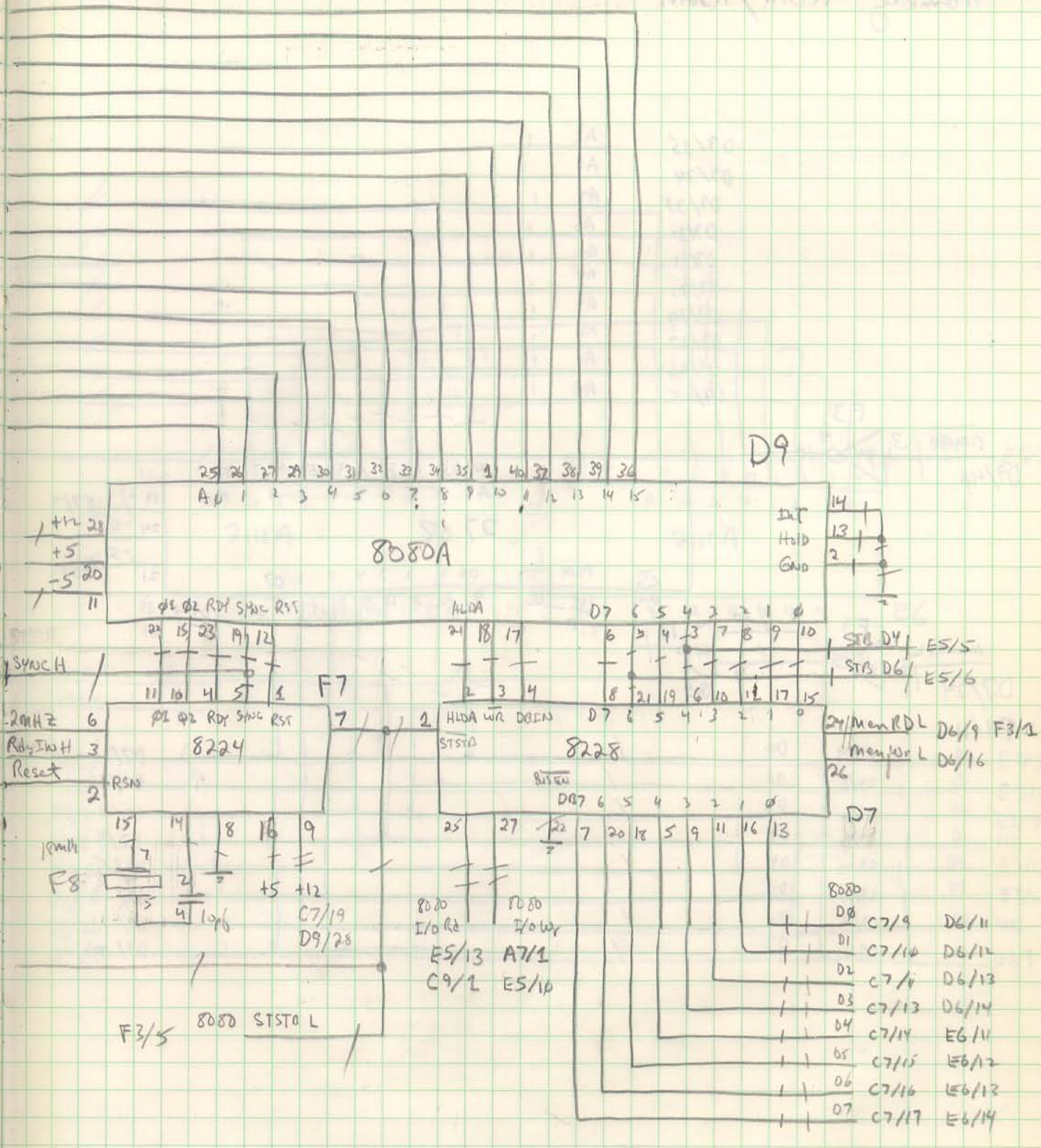
Boot (Force NPR) Logic



CPU & Wait Logic




D9
8080A
A0
INT
Hold
GND
+12
+5
-5
ϕ1 ϕ2 RDY SYNC RST
HLDA
D7 6 5 4 3 2 1 ϕ
STB D4
STB D6
E5/5
E5/6
SYNC H
F7
2MHZ
RdyInH
Reset
RSN
8224
HLDA WR DBIN
STSTB
8228
BUSEN
DB7 6 5 4 3 2 1 ϕ
MemRDL
MemWrL
D6/9 F3/1
D6/16
D7
18mHz
F8
10pf
+5
+12
C7/19
D9/28
8080 I/O Rd
8080 I/O Wr
E5/13
A7/1
C9/1
E5/10
F3/5
8080 STSTB L
8080
D0 C7/9 D6/11
D1 C7/10 D6/12
D2 C7/11 D6/13
D3 C7/13 D6/14
D4 C7/14 E6/11
D5 C7/15 E6/12
D6 C7/16 E6/13
D7 C7/17 E6/14

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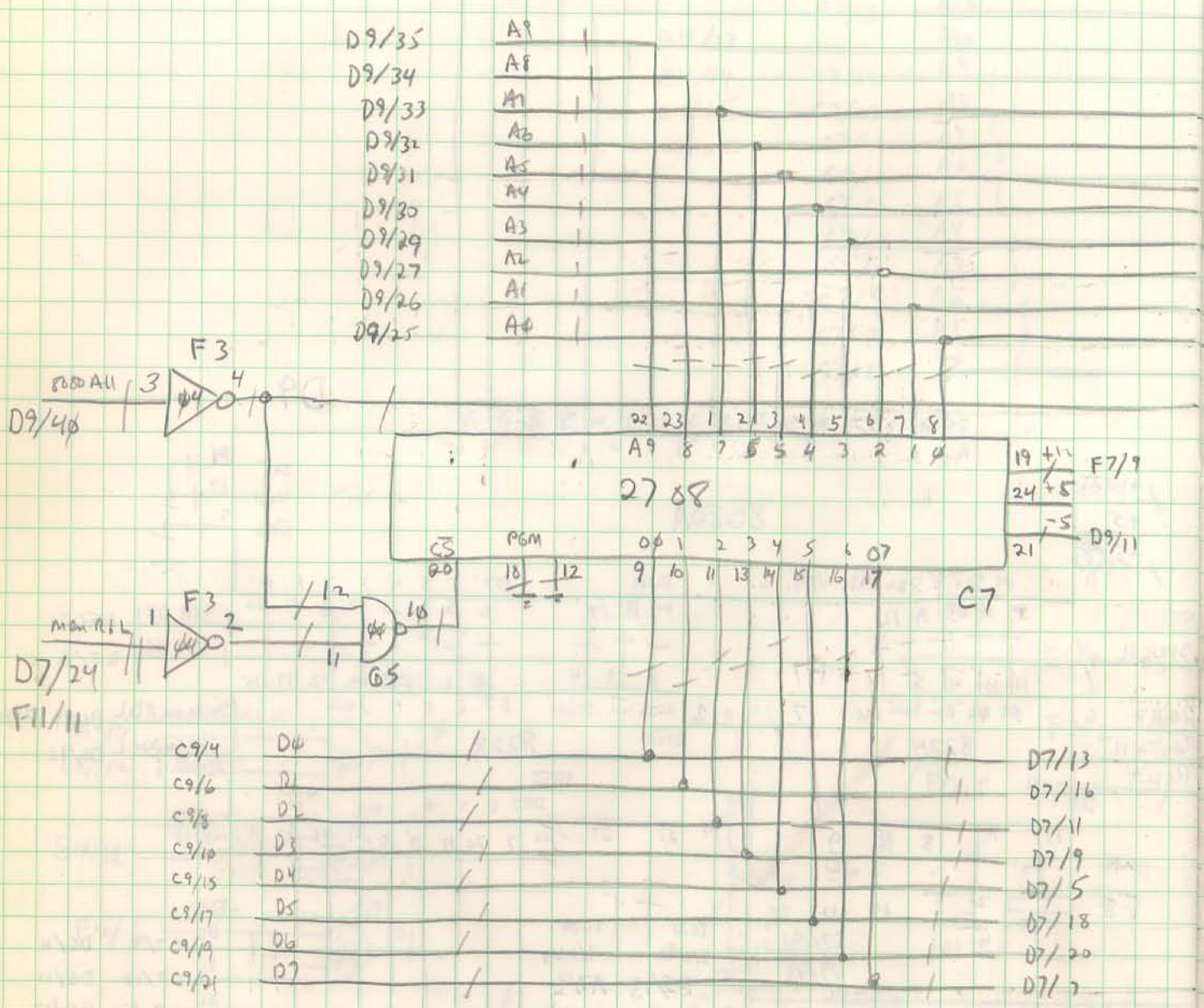
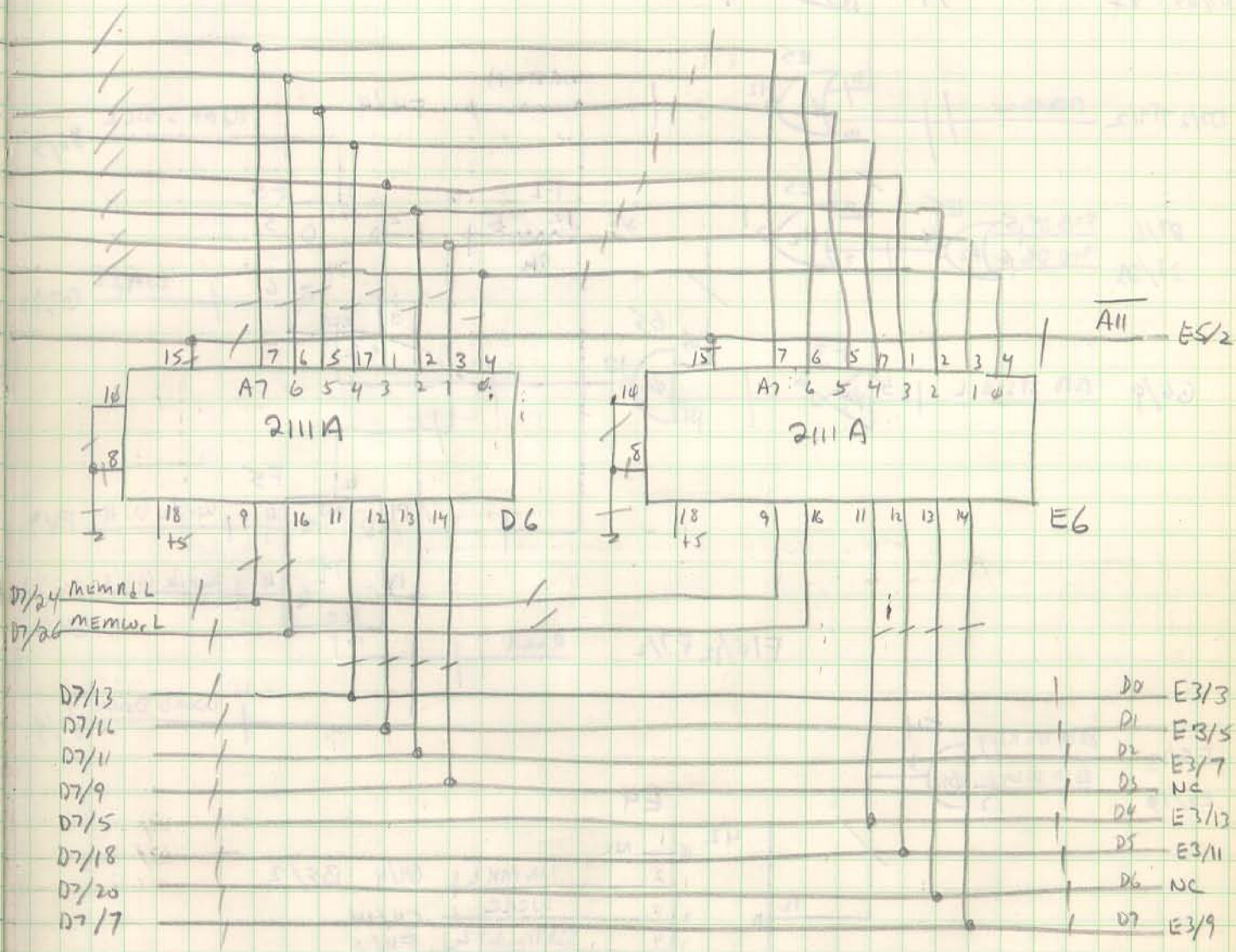
Memory Rom/Ram




A11
E5/2
2111A
A7 6 5 4 3 2 1 0
D6
E6
+5
D7/24 MEMRdL
D7/26 MEMWrL
D7/13
D7/16
D7/11
D7/9
D7/5
D7/18
D7/20
D7/7
D0 E3/3
D1 E3/5
D2 E3/7
D3 NC
D4 E3/13
D5 E3/11
D6 NC
D7 E3/9

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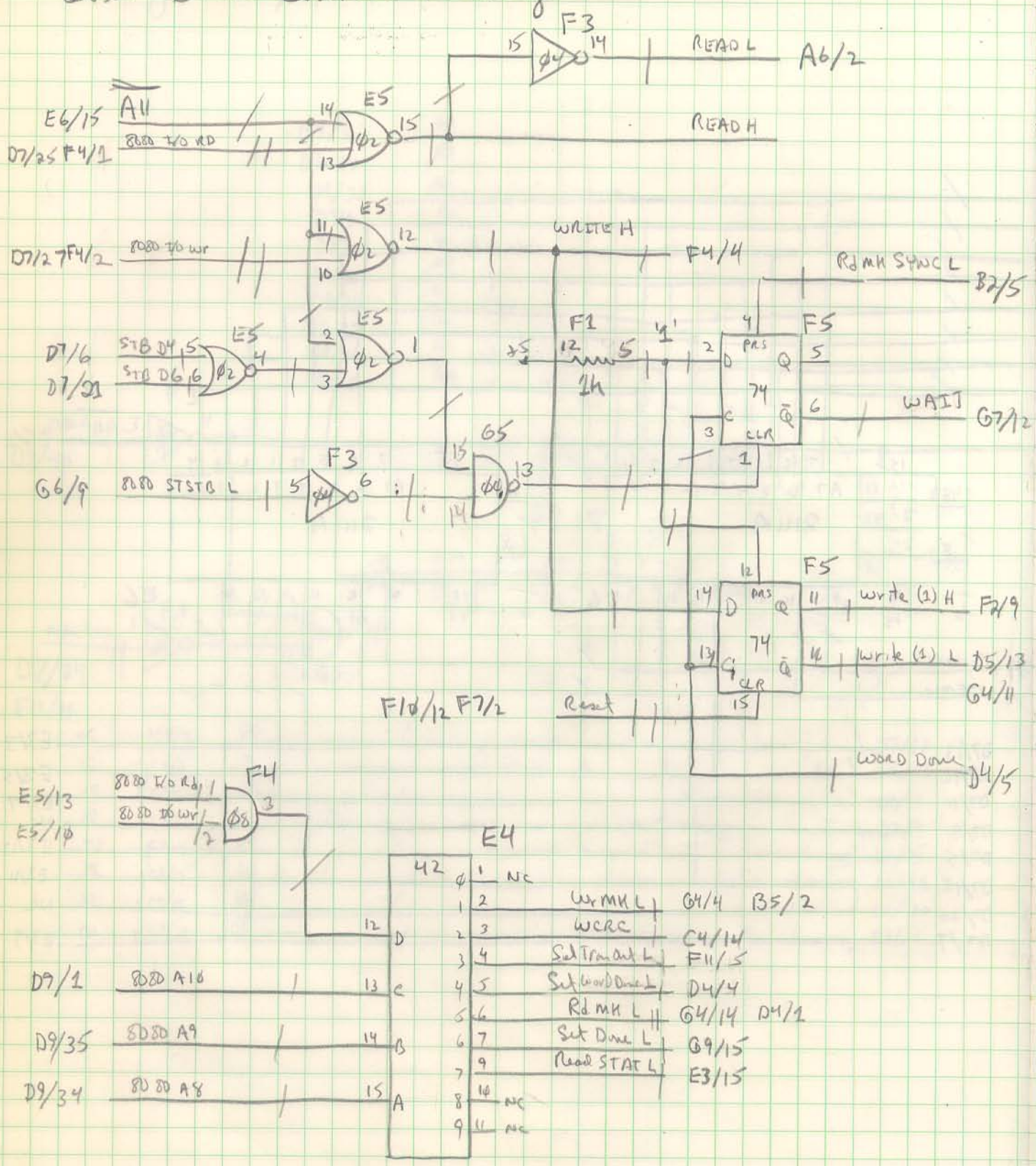
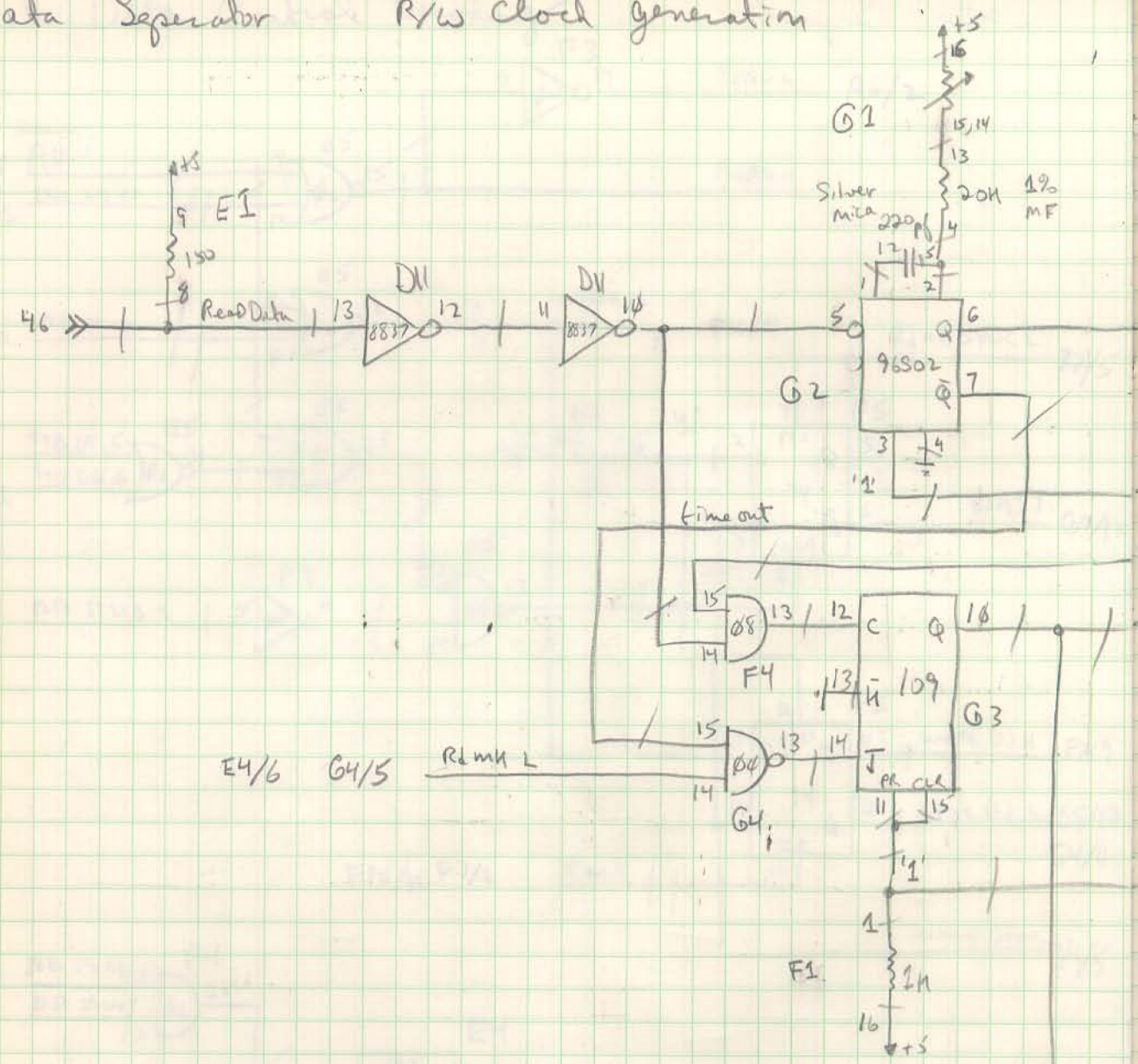
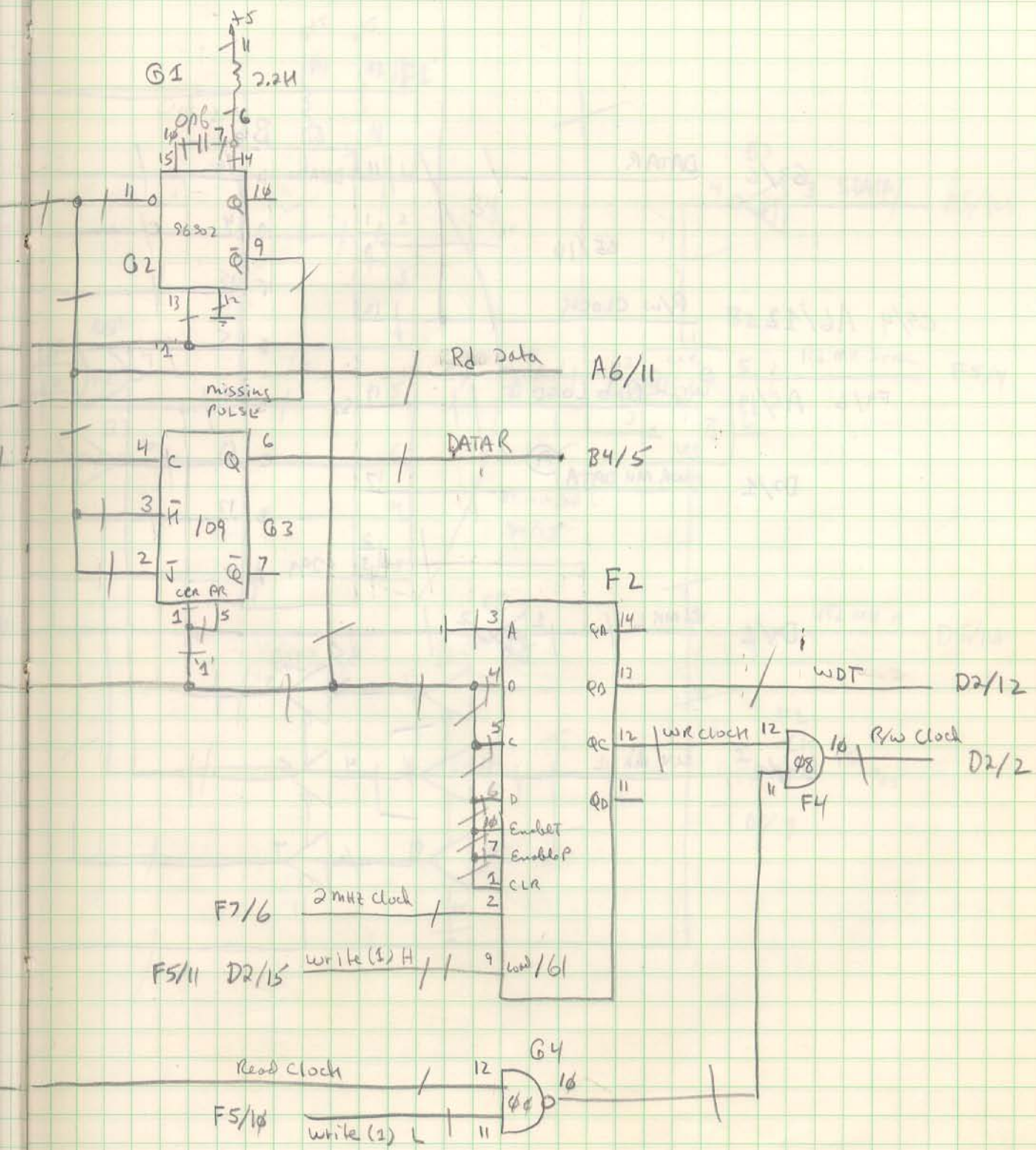
Disk Data Control Decoding



Data Separator R/W clock generation




+5
G1
2.2H
opb
96502
G2
Rd Data
A6/11
missing PULSE
DATAR
B4/5
109
G3
CLR PR
F2
WDT
D2/12
WR clock
R/w clock
D2/2
F4
Enable T
Enable P
CLR
2 MHz clock
F7/6
write (1) H
F5/11 D2/15
161
G4
Read clock
F5/10
write (1)

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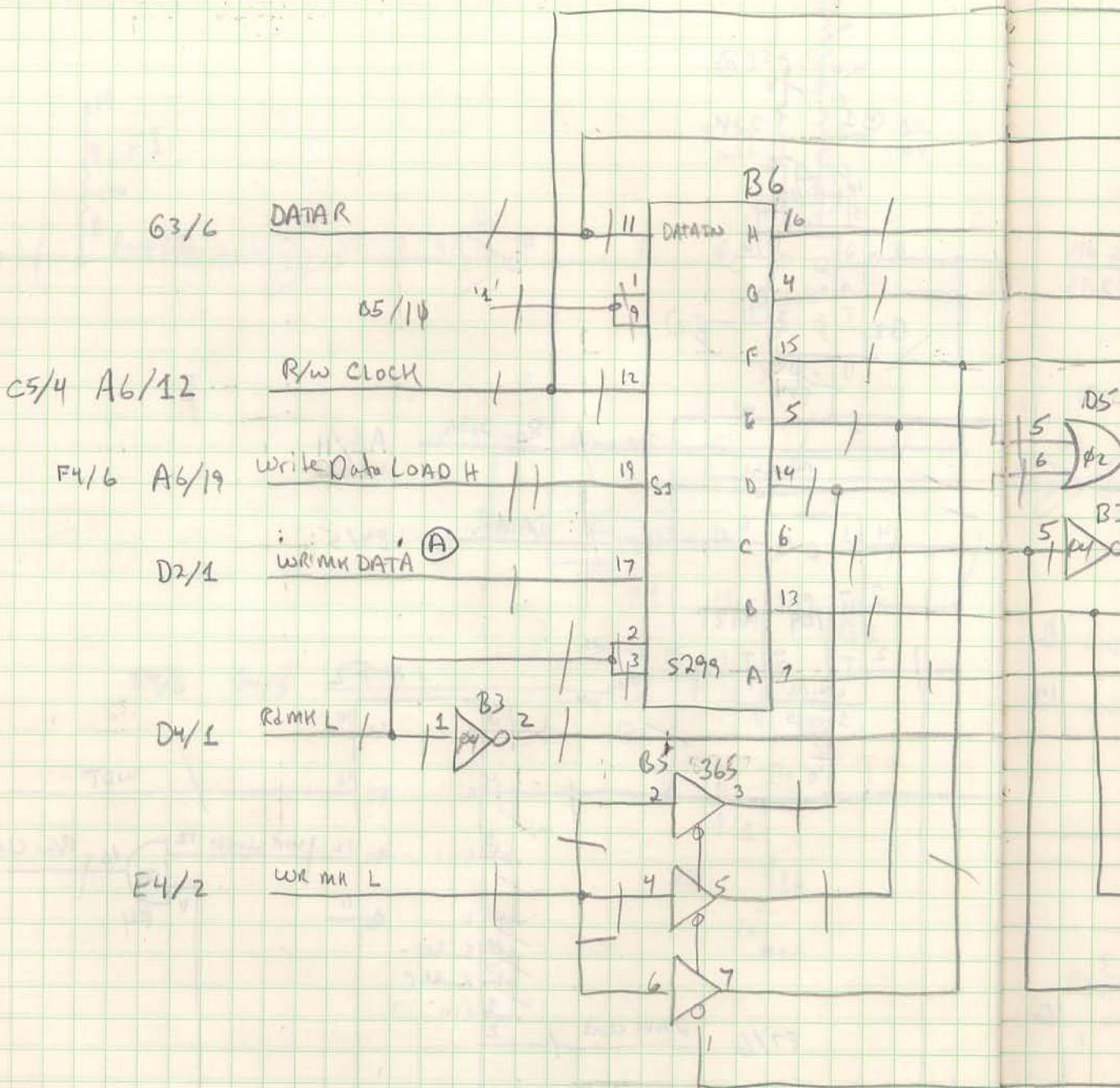
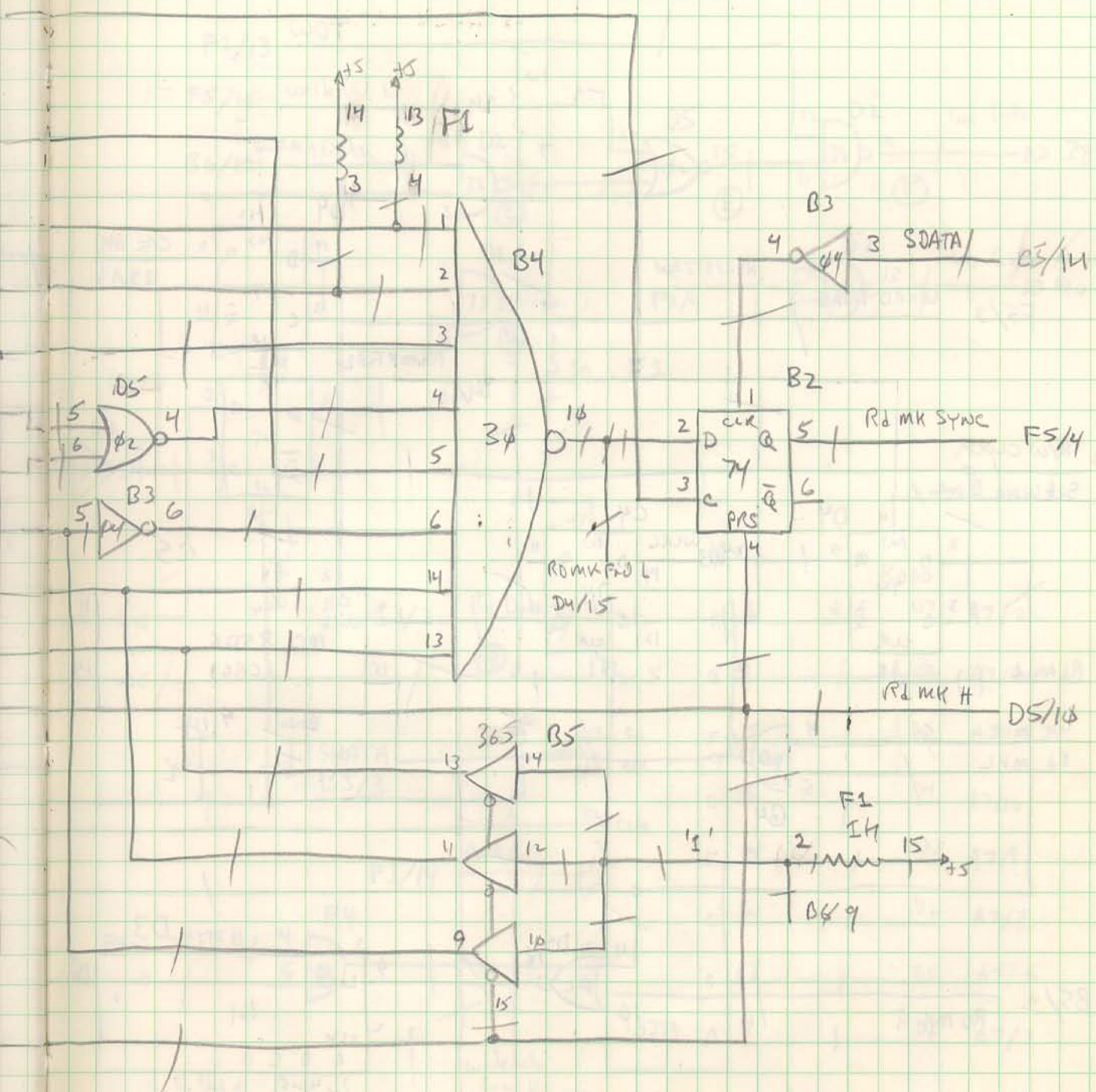
ARO

Rd Mark Detection




+5
+5
14
13
F1
3
4
B4
B3
4
3 SDATA
C5/14
B2
DS
5
6
4
B3
5
6
1
2
3
4
5
6
14
13
3Φ
1Φ
CLK
D
C
74
PRS
Q
Q
5
6
4
RdMK SYNC
FS/4
RDMKFND L
D4/15
RdMK H
DS/1Φ
365
B5
13
14
11
12
9
10
15
'1'
F1
14
2
15
+5
B6 9

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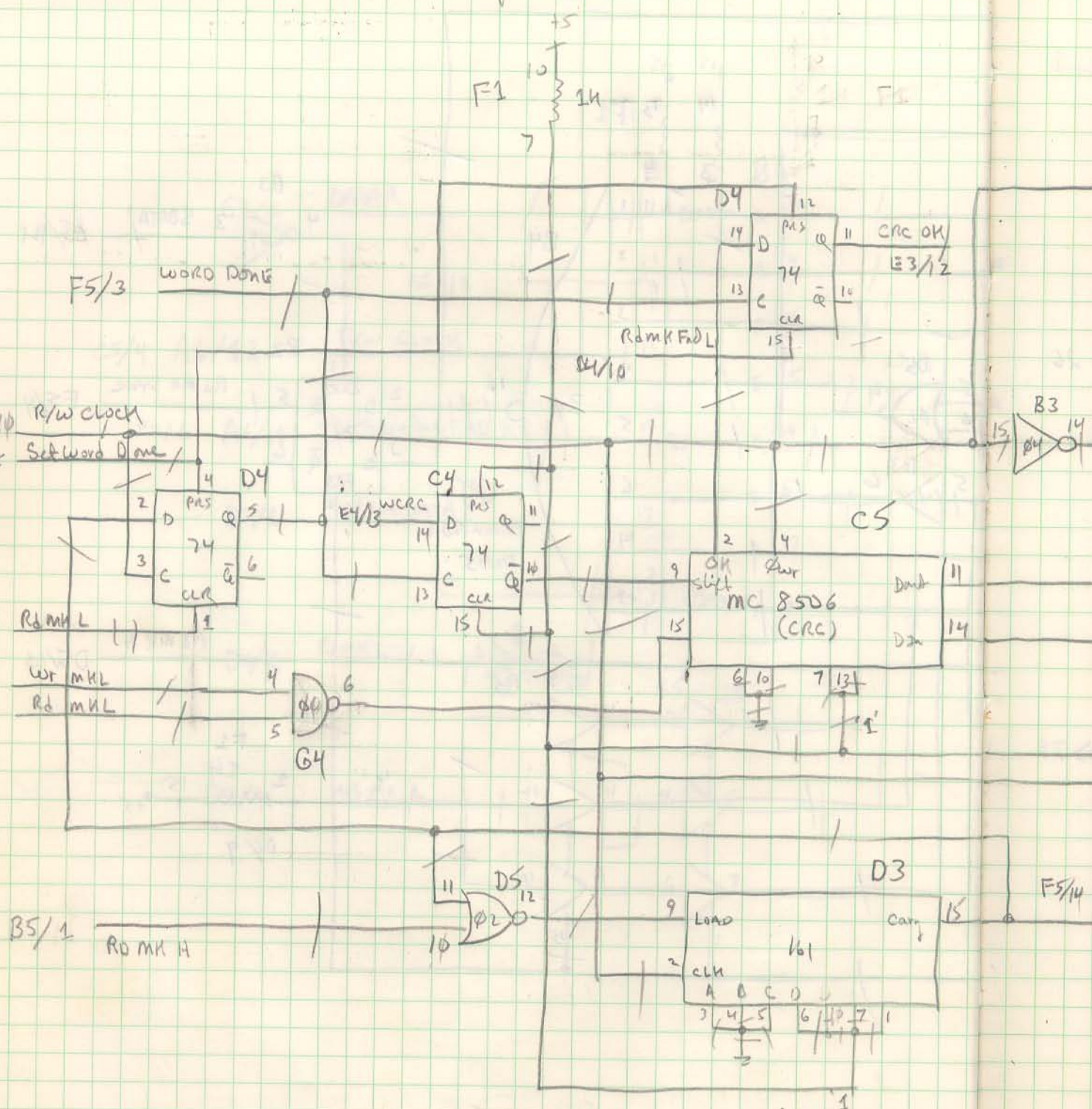
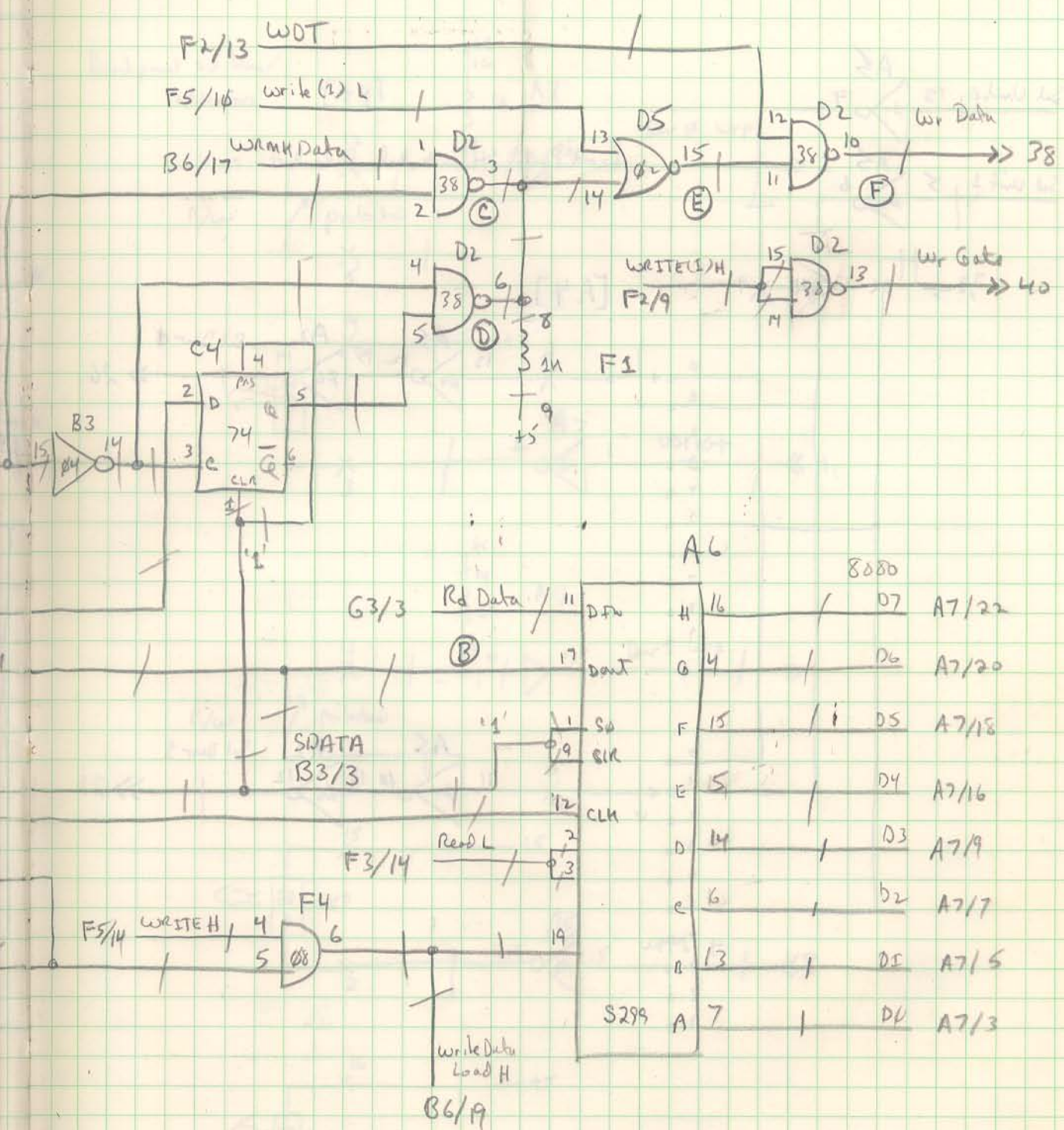
ARD

Write Data Drivers / Data Shifter / CRC checker




F2/13 WOT
F5/16 write (1) L
B6/17 WRMK Data
D2
D5
Wr Data
>> 38
WRITE(1)H
F2/9
Wr Gate
>> 40
C4
74
PRS
CLR
B3
1K
F1
A6
8080
G3/3 Rd Data
DIN
DOUT
SO
SIR
CLK
SDATA
B3/3
'1'
F3/14 Read L
F4
F5/14 WRITE H
S299
Write Data Load H
B6/19
D7 A7/22
D6 A7/20
D5 A7/18
D4 A7/16
D3 A7/9
D2 A7/7
D1 A7/5
D0 A7/3

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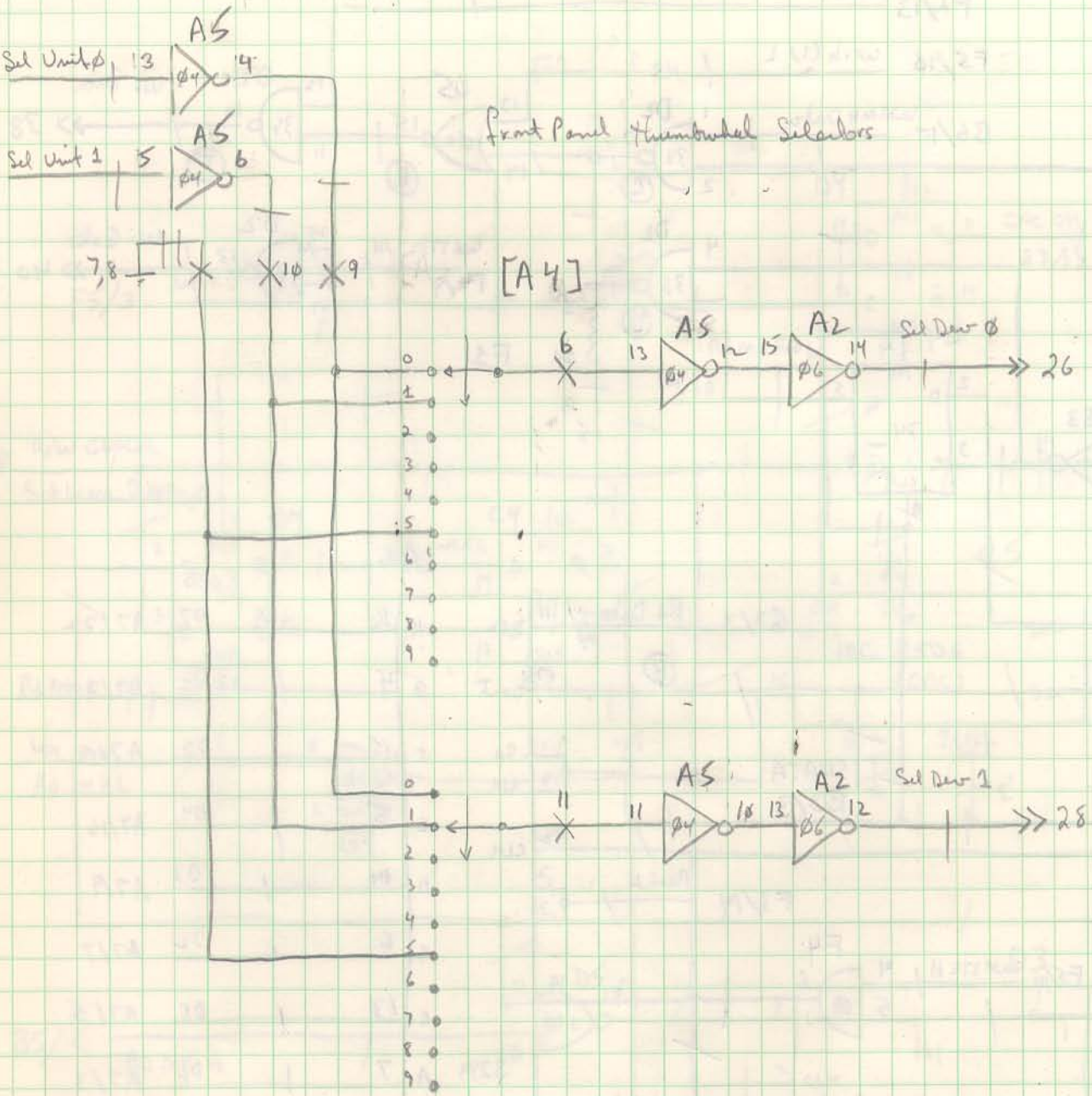
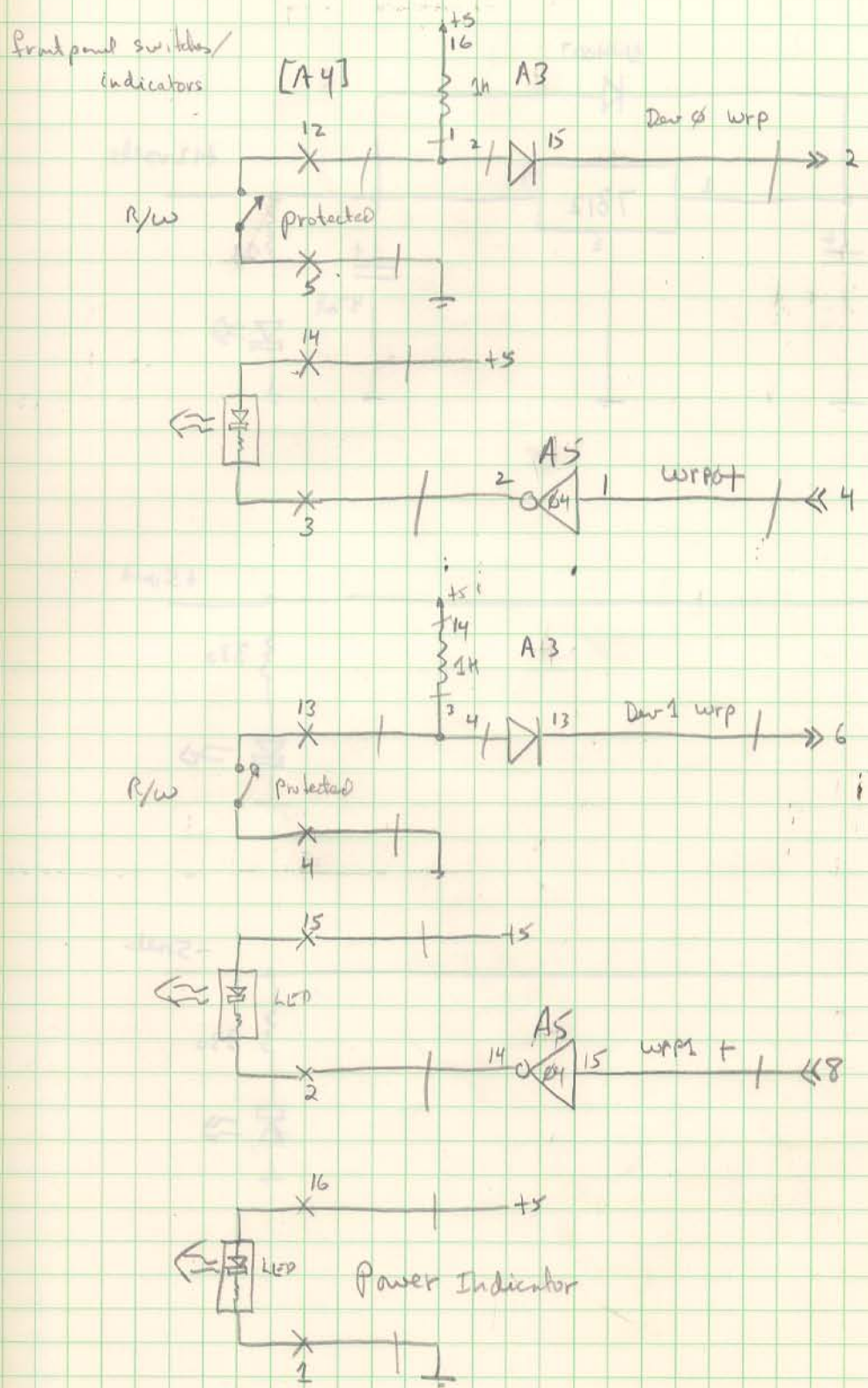
ABD

Device Selectors



Write Protect Logic / Power Indicator



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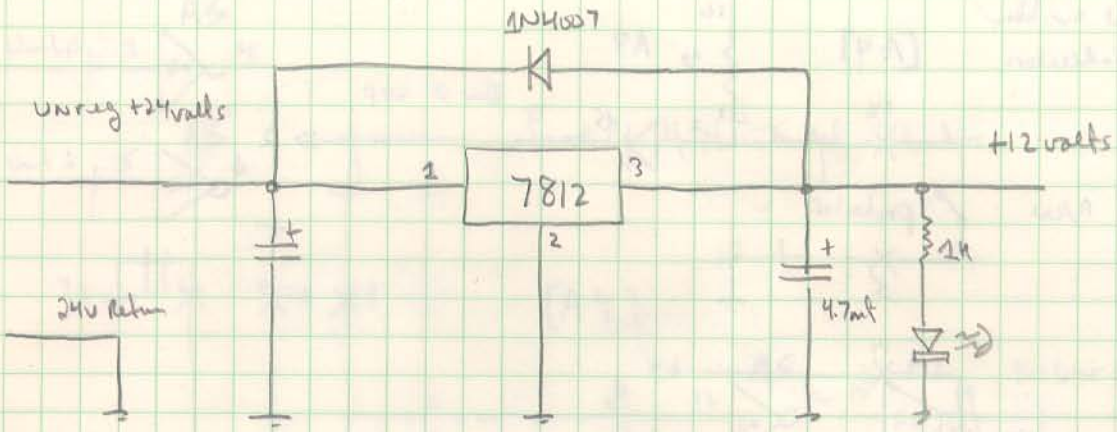
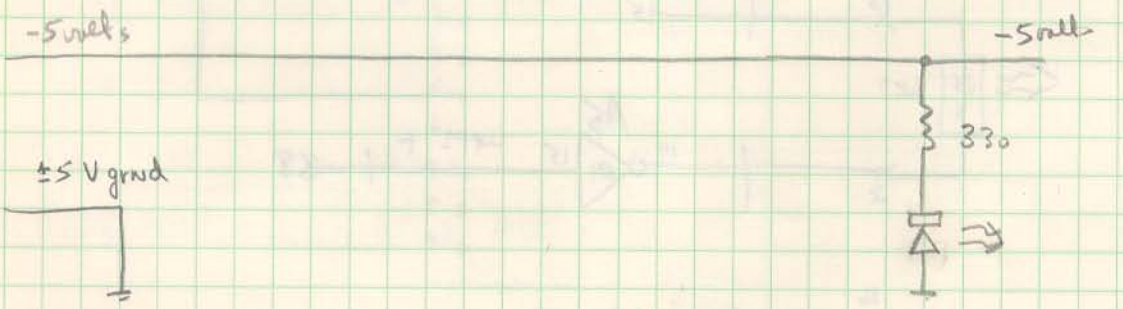
ASD

Regulator / Power Lamps





IC LOCATIONS

A2	7406	17, 25
A3	RES	16, 25
A4	Connector	25
A5	7404	25
A6	74S299	24
A7	8212	17.
A9	8212	16
A10	7400	14
A11	7404	14, 18
A12	7402	14
A13	7438	15
A14	8838	16

B2	7474	23
B3	7404	23, 24
B4	7430	23
B5	74365	23
B6	745299	23

B10	7406	14
B11	7408	14
B12	7402	14
B13	7438	15
B14	8838	16

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ARD

C2	--	
C3	--	
C4	7474	24
C5	MC8506	24
C7	2708	20
C9	8212	16
C10	7474	14
C11	74S74	14
C12	7438	15
C13	7438	15
C14	Switches	15

D2	7438	24
D3	74161	24
D4	7474	24
D5	7402	23, 24
D6	2111A	20
D7	8228	1,9
D9	8080A	19
D10	7406	12, 14, 18
D11	8837	13, 14, 22
D12	7438	14
D13	74LS266	12, 18
D14	Resistors	12, 14

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ARD

E1	Resistors	17, 22
E2	— —	
E3	8T97	17
E4	7442	21
E5	7402	21
E6	2111A	20
E10	Resistors	12, 14
E11	Resistors	18
E12	7438	18
E13	74LS266	12
E14	Switches	12

F1	Resistors	21, 23
F2	74161	22
F3	7404	20, 21
F4	7408	21, 22, 24
F5	7474	21
F6	74123	13, 19
F7	8224	19
F8	Crystal	19
F9	Resistors	13
F10	7402	13
F11	7432	13
F12	7438	13
F13	74LS266	12
F14	Switches	12

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G1	Resistors	22
G2	965Ø2	22
G3	74109	22
G4	74ØØ	22, 24
G5	7400	13, 2Ø, 21
G6	Resistors	13, 19
G7	74Ø3	19
G8	7474	13
G9	7474	13
G1Ø	74Ø4	13
G11	7442	12
G12	7420	12
G13	8838	12
G14	8838	12
G15	8837	12
G16	8836	12, 14

Softwom Registers –

Addrem

@ 4000	Sector Address	$\emptyset_8$
4001	Track #	
4002	Disk Control	
4004	Error Register	
4006	Wn MM data	
4003	Unit 1 Track #	
4023	Unit $\emptyset$ Track #	
4177	PDP-11 Disk STATUS Register	
Stack @ 4176 and down		10_8
Data Buffer byte #	4201 – 4377 , 4200 $\emptyset$ – 127 , 128	

14_8

Controller Software [8080 Assembly]

Software Decoded by Hand ~ 5 days work after listing converted to instruction form. AHO

Address				
$\emptyset_8$	RESET:	$\emptyset$	NOP	Power up/Reset entry Point
		$\emptyset$	NOP	
		41 176 1$\emptyset$	LXI H 4176_8	Load H & L with 4176_8
		303 136 2	JMP START (1136_8)	go start program
$1\emptyset_8$	RST 1:	301	POP B	Pop stack into B & C
		303 247 3	JMP DIAG (1647_8)	Go Return DIAGNOSTIC
14_8	PATCH:	64	INC M	increment data @ H & L
		303 112 3	JMP FORMN (1512_8)	

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AHO

Clear/Set Bit Subroutine (on register B)

Address

20_8	RST2:	343	XTHL	Exchange Top of Stack with H & L	40_8
		365	PUSH PSW	Save A & STATUS	
		176	MOV A, M	get Data after RST2 Call!	
		332	JC ORB (31_8)	if Carry=1 OR Bit!	
		31			
		0			
		57	CMA	Complement A	
		240	ANA B,	Mask out Bit	
		6	MVI B	Dummy instruction !!! if carry=0	
31_8	ORB:	260	(ORA B)	(OR in Bit if Carry = 1)	50_8
		107	MOV B, A	place result in B	
		361	POP PSW	restore A & STATUS	
		43	INX H	increment return address past Data	
		343	XTHL	restor H & L	
		311	RET	Return to Caller	

60_8

Step Line Control Subroutine

Address

40_8	RST4:	327	RST 2	Mask in step Bit (in reg B)
		1		
		170	MOV A, B	Mov reg B into A
		323	OUT 40	send control information
		40		to Disc Control Register
		77	CMC	Complement the carry Bit
		311	RET	Return to Caller

WAIT Subroutine (A milliseconds)

50_8	RST5:	36	MVI E 144_8	Move H 144_8 into E
		144		
		367	RST 6	Call Routine RST 6
		75	DCR A	Count down to zero
		302	JNZ RST5	if A ≠ 0 Loop back to repeat
		50		
		ø		
		311	RET	Return to Caller
60_8	RST 6:	35	DCR E	Count down to zero
		310	RZ	Return to caller on E = ø
		303	JMP RST6	loop back
		60		
		ø		

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Control Register Checking

Addres					Addres
65_8	CTLCHK:	1 0 0	LXI B "0_8	Load B & C with 0	117_8
		56 2	MVI L "2_8	Load L with "2	
72_8	RDST:	333 7	IN 7	Read Disk Status	
		27	RAL	Rotate Disk STATUS DONE into Carry flag	
		332 117 0	JC DSPTCH	if New command has been entered go to Dispatch Handler	
		3	INX B	increment 16 Bit counter B & C	
		4	INC B	} check if B is Negative yet	
		5	DCR B		
		362 72 0	JP RDST	if B still + go read status again	
		76 277	MVI A "277_8	get "277 into A	
		246	ANA M	Mask previous Disk Control Word with A to 'UNLoad Head'	
		167	Mov M, A	store MASKed control word	
		323 40	OUT 40_8	place word in Control Register	
		303 72 (65) 0 (0)	JMP RDSTAT (CTLCHK)	go check again	

Dispatch Handler

Addres

117_8	DSPTCH:	76 367	MVI A $\#367_8$	Load Aw.th $\#367_8$
		246	ANA M	Clear Error Bit from Disk Control Register
		323 40	OUT 40_8	output new Control Register
		167	MOV M, A	place New Control Both in M
		333 20	IN 20	Read Data from BOS Command Register
		37	RAR	Rotate Command into the 3 LSB's of A
		1 343 2	LXI B $\#1343_8$	Load B&C with 1343_8
		305	PUSH B	Push Return address onto Stack
		127	MOV D, A	Save Areg in D
		346 7	ANI A $\#7_8$	Mask out extraneous Bits Save only Function!
		1 157 0	LXI B #TABLE	Load B&C with $\#157_8$ pointer to Dispatch table
		201	ADD C	Compute pointer to Table only A = A+C
		117	MOV C, A	put A into C
		12	LOAX B	bring Table ENTRY into A
		117	MOV C, A	put A into C
		305	PUSH B	Push routine Address onto Stack

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Addrs

147_8

56 177	MVI L, #177_8	Set L = 177_8
163	MOV M, E	Same E reg @ 4177_8 = Ø
227	CLEAR A	Clear Acc & Carry
323 20	OUT 2Ø	Clear Buffer register
43	INX H	increment regpair H & L = 4200_8
311	RET	Go to Function Routine

Addrs

167_8

Dispatch Table

Addrs

157_8	TABLE:	243	# FILBUF	ØØØ	Fill data Buff from PDP-11
		217	# EMTYBF	ØØ1	Empty data Buff to PDP-11
		347	# WRSCTR	Ø1Ø	Write Sector to disk
		372	# RD SCTR	Ø11	Read Sector from Disk
		167	# SPCLFN	100	Special Functions
		265	# RDSTAT	101	Read STATUS Register
		360	# WRDLDS	110	Write a deleted Data Sector
		333	# RDERR	111	Read Error Register

SPECIAL FUNCTION CHECKER

Addrs				
167_8	SPCLFN:	6 10	MVI B #10_8	set B = 10_8
		172	MOV A, D	get operation from D A = D
		346 30	ANI #30	mask operation to check for Codes 31 or 51 or 11
		312 361 2	JZ LDBOOT (1361_8)	if 11 then go to Boot routine
		127	MOV D, A	Save masked operation code in D reg
		227	SUB A	Clear Acc & Carry
		315 67 3	CALL STAT (1467_8)	will transfer A to Disk Control & Read Disk Stat into A with RDY in Carry
		330	RC	if carry = 1 Return ie goes to (1343_8)
		172	MOV A, D	get MASKed operation code in A
		220	SUB B	compute A = A − 10
		312 247 3	JZ DIAG (1647_8)	if A = 0 then code was a 31 Diagnostic - jump
		220	SUB B	compute A = A − 10
		312 100 3	JZ FORMAT (1500_8)	if A = 0 then code was a 51 Format - jump
		311	RET	else an illegal code Return via (1343_8)

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BDD

Empty Buffer Routine F#1

Addres						Addres
217_8	EMTYBF:	54	INR L		increment L $\therefore = 20\emptyset_8$	243
		176	MOV A,M		A = Data @ 4201_8	244_8
		46 210	MOV I H	$*210_8$	load H with 210_8 i.e. Memy High Address 1Ø + Control to set IN TRANS H Bit !!!	
223_8	MORE1:	323 2Ø	OUT	20_8	Put Data into PDP11 Data Buffer	
		54	INR L		increment Address pointer	
		176	MOV A,M		get Data from location (H,L)	
					* CPU will wait here until PDP-11 takes data from Data Buffer	
		372 223 Ø	JM	MORE1 (223_8)	if L still negative do MORE!	
		72 200 1Ø	LDA	@4200_8	get Last Byte of Data for Transfer	
		323 2Ø	OUT	$2\emptyset_8$	place last Byte in Buffer	
		176	MOV A,M		Dummy Load - waits for PDP-11 to get last Byte	
		303 343 2	JMP	(1343_8)	Terminate operation	

Fill Buffer Routine F#0

Address

243	FILBUF:	54	INR L	increment L to $L = 201_8$
244_8	MORE2:	333 223	IN 223_8	This is command: 1) Sets Word Done F/F to Done 2) sets OUT TRANS Bit 3) Waits Here until PDP-11 sends data 4) Reads Data from BUS Data Buff
		167	MOV M,A	place Data @ H,L
		54	INR L	increment L
		372 244 0	JM MORE2 (244_8)	if L is minus get more!
		333 223	IN 223_8	get last byte from PDP-11
		323 6	OUT 6_8	Tell PDP-11, were DONE! Set Control Reg Done Flag
		62 200 10	STA @4200	place last Byte of Data
		303 352 2	JMP (1352_8)	Terminate operation

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ARD

Read Status Register Routine F#5

Addrs					
265_8	RDSTAT:	56 2	MVI L	Set L = #2_8	
		172	mov A,D	get Command Register	
		346 10	ANI #10_8	Test Unit select Bit	
		6 40	MVI B #40	initialize B for Unit 1	320_8
		312 301 0	JZ $1	if A=0 use unit 1	
		6 20	MVI B #20	else use unit 0	
301_8	$1:	176	mov A, M	get Data A= @(H,L) 4002_8 Disk Control Word	
		346 317	ANI #317	Mask Bits 4 & 5 from Word (ie previous Selects)	
		260	ORA B	OR in Unit select	
		323 40	OUT 40_8	Set Disk control	
		276	CMP M	Compare A & M@(H,L)	
		167	mov M, A	mov A to M	
		312 320 0	JZ $2	if this status is for the previously selected unit Jump ahead	

Address

		76 277	MVI A ^{H}277	get Mask
		246	ANA M	And with Control word
		167	mov M, A	Store new Control (Have Marked at Head Load!)
320_8	$Z:	56 177	MVI L	Set L = 177_8
		333 7	IN 7_8	Read Disk STATUS
		37	RAR	Rotate Ready Bit into Carry
		77	cmc	Complement the carry Bit Carry = 1 if ready!!
		106	mov B, M	get STATUS word from Memory
		327 200	RST2	go set/clear ready bit in control
		160	mov M, B	put STATUS back in Memory
		311	RET	Return to Caller

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ARD

Read Error Register Routine FH7

Address					
333_8	RDERR:	53	DCX H	Decrement H,L	$(= 4177_8)$
		176	MOV A, M	get M(H,L)	
		27	RAL	Rotate Left through Carry	
		173	MOV A, E	A = E = ϕ	
		37	RAR	Rotate Right from Carry	
		167	MOV M, A	Put Data back into Memory	
		72	LDA @4004$_8$	A = M@4004$_8$ (Error Register)	
		4			
		10			
		303	JMP ERRX (1346_8)	go place Error register	
		346			
		2			

Address

347_8

Address

360_8 U

Write Sector Setup F#2

Address

347_8	WRSCTR:	227	SUB A	Clear A & Carry
		62 177 10	STA @4177_8	put Ø @ 4177_8
		76 373	MVI A #373_8	Set A = 373_8
		303 125 1	JMP WRITE (525_8)	go write sector

Write Deleted Data Mark Setup F#6

360_8	WRDLDS:	76 100	MVI A #100	
		62 177 10	STA @4177_8	put 100 @ 4177_8 indicate Deleted Data Mark!
		76 370	MVI A #370	Set A = 370_8
		303 125 1	JMP WRITE (525_8)	go write sector

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Read Sector Routine

Addrs

372_8	RDSCTR:	55	DCR L	Set L = L-1 ($=4177_8$)
		163	MOV M, E	Set M = Ø
		315 265 Ø	CALL RDSTAT (265_8)	M = 200 if ready M = Ø if not ready
		315 224 1	CALL SCTTRK (624_8)	go get Sector/Track Address & position Head Returns after finding correct Track and Sector!
402_8	INITS1:	16 3	MVI C,	C = 3_8
404_8	$LPØ:	333 1Ø	IN $1Ø_8$	Read Byte
		273	CMP E	is Byte = Ø
		302 4 1	JNZ $LPØ	if not - get another byte this finds the preamble to the Data Field
		26 373	MVI D #373_8	get the Data Mark! D = 373
		56 200	MVI L 200_8	L = 200
		333 4	IN 4	Set Word Done F/F
		333 15	IN 15	Wait Here until RDMK or Deleted Data ROMK Detected

442_8

```
                107     MOV  B,A        Save ROMK in B
                366     ORI  #3         OR in #3 for comparison
                  3
                272     CMP  D          Does D=A ?
                302     JNZ  NOTMK (442₈)  if not this is not
                 42                         a ROMK
                  1
                333     IN 7            Read STATUS
                  7
                346     ANI  #40        check if ReadMK was found
                 40
                333     IN 10           Get first Byte of Data
                 10
                312     JZ   READ (454₈)   if ReadMK found
                 54                         go read all of Data
                  1
442₈ NOTMK:     15      DCR  C          else decrement C
                                        timed out yet?
                314     CZ   $130 (1304₈)  Error $130 - NO I/O
                304                        mark found within
                  2                        allotted time
                303     JMP  $LP0 (404₈)   Go try again
                  4
                  1
```

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Addrs

451_8	$LP1:	167	MOV M, A	Put Data into Buffer
		333 10	IN 10_8	read next Byte
454_8	READ:	54	INR L	increment Buffer pointer
		302 51 1	JNZ $LP1 ($451_8$)	more to read - Loop
		62 200 10	STA @4200_8	place last byte in memory
		333 10	IN 10_8	} Read CRC
		333 10	IN 10_8	
		333 10	IN 10_8	Read extra Byte to allow shifting of Last CRC Byte into checker
		333 7	IN 7_8	Check CRC
		56 177	MVI L, 177_8	Set L = 177_8
		365	PUSH PSW	Push A & Flags onto stack

514_8

```
                76      MVI A  #373₈        Data Mark
                373
                270     CMP B               was RD MARK a Data Mark?
                312     JZ  REND  (514₈)    if yes-branch to REND
                114
                  1
                76      MVI A  #370₈        Deleted Data Mark
                370
                270     CMP B               was RD MARK a Deleted Data Mark?
                304     CNZ  $130           NO-Error-invalid RD Mark!
                304       :    .
                  2
                66      MVI M  #100         @4177₈ = 100   set DD in
                100                                        Status
514₈  REND:     361     POP PSW             Restore A & Flags
                27      RAL
                27      RAL                 } Rotate CRC check into
                27      RAL                   Carry
                320     RNC                 Return if CRC OK
                64      INC M               indicate CRC Error
                315     CALL $0             Terminate Operation
                317
                  2
```

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Write Data Sector Subroutine

Addrss					
525_8	WRITE:	62 6 10	STA	#4006	Save Wr MK
		315 265 4	CALL	RDSTAT (265_8)	get Disk status
		333 7	IN 7		Read Status
		37	RAR	}	shift Write protect
		37	RAR	}	into Carry
		77	cmc		Complement Carry Flag
		106	MOV B, M		get STATUS
		327 10	RST 2		Set Write protect Bit in STATUS
		160	MOV M, B		Store STATUS
		334 317 2	CC	$0	Terminate operation if Write protected
		315 224 1	CALL	SCTTRK (624_8)	go get Sector/Track Address & Position Returns after finding current Track & sector
552_8	WRTD:	16 42	MVI C	#42	Set up wait loop to get by 11 Bytes of the Data Preamble
554_8	$LP2	15	DCR C		
		302 154 1	JNZ	$LP2	

Addrss

560_8

564_8

577_8

Addrss

580_8		16 6	MVI C #6	C = 6	
		151	MOV L, C	Set L = 6	
		173	MOV A, E	Set A = ∅	
584_8	$LP3:	15	DCR C		write 6 Bytes of All ∅'s
		323 10	OUT 1∅		
		302 164	JNZ $LP3 ($584_8$)		
		176	MOV A, M	Get WR MK into A @4006!	
		323 11	OUT 11	write the Data Mark!	
		56 201	MVI L #201	L = 201	
577_8	$LP4	176	MOV A, M	get data into A	
		323 1∅	OUT 1∅	Write Byte	
		54	INR L	update Data Buffer Pointer!	
		302 177 1	JNZ $LP4 ($577_8$)	Loop to write 127 Bytes!	
		72 200 10	LDA @4200	get Last data Byte	
		323 1∅	OUT 1∅	write Last data Byte	

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Address			
613_8	323 12	OUT 12	} Write CRC Bytes
	323 12	OUT 12	
	76 377	MVI A #377	A = 377
	323 10	OUT 10	Write a Byte of 1's
	311	RET	Return to caller (via 1343_8)

Addres

624_8

Sector/Track Positioning Routine

Addrss				
62_8	SCTRK:	176	MOV A,M	Get Status
		27	RAL	put Ready bit into Carry
		322 343	JNC	(134_3_8) if not ready - Terminate operation
		2		
		77	CMC	Complement Carry
		37	RAR	regenerate STATUS with Ready Bit clear
		167	MOV M,A	store New Status
		153	MOV L,E	Set L = 0
		333 223	IN 223	1) Set TR Bit 2) Wait for PDP11 to load Sector Add 3) Read Sector Addrss
		346 37	ANI #37_8	Mask Sector Data
		167	MOV M,A	Store Sector Address @ 4000
		54	INR L	increment Memory pointer
		333 223	IN 223	1) Set TR Bit 2) Wait for PDP-11 to load Track Addrss 3) Read Track Addrss
		346 177	ANI #177	Mask Track Data
		167	MOV M,A	Store Track Addrss @ 4001

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Address

Address	Label	Code	Instruction	Comment
650_8		54	INR L	increment memory pointer
651_8	INITSØ:	106	MOV B,M	Load B with Disk Control Word @4002
		376 53	CPI #53	Determine track position and set Head current accordingly
		77	CMC	complement carry
		327 4	RST2	head current bit
		376 115	CPI #115_8	check Track # past 76?
		324 313 2	CNC $40	(1313_8) — Error - track > 76
		54	INR L	increment memory pointer
		117	MOV C,A	Save Track # in C
		76 20	MVI A #2Ø	set A = 2Ø
		240	ANA B	A = A∧B A = 2Ø if unit Ø; A = Ø if unit 1
		265	ORA L	A = A∨#3 A = 23 if unit Ø; A = 3 if unit 1
		157	MOV L,A	L = A
		171	MOV A,C	A = Track Address
		226	SUB M	A = A − M(H,L) A is the difference between the Seek Track and the Current Track!

Address			
675_8	161	MOV M, C	Save New Track Position just Loaded from PDP-11
	56 3	MVI L #3	set L = 3
	77	CMC	Complement Carry (from Subtraction)
	327 2	RST 2	Set Direction Bit for Seek !
	332 310 1	JC SHIN (710_8)	if A is positive - skip ahead ie move head into middle of Disk
	57	CMA	Complement A } make # of steps positive
	74	INR A	& ADD 1 }
710_8 SHIN	117	MOV C, A	Save # of steps in C
	54	INR L	increment memory pointer
	163	MOV M, E	set $4004_8 = 0$
	127	MOV D, A	Save steps in D
	24	INR D	& Add 1
	326 4	SUI #4	Test for more than a 4 track step !
	332 331 1	JC $L4TRK ($731_8$)	if not - skip ahead
	117	MOV C, A	else save Track steps - 4 in C
	123	MOV D, E	set D = 0
	315 123 2	CALL STEP (1123_8)	go move Head C tracks

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Addrss					
727_8		16 4	MVI C #4	set C = 4 (tracks still to step)	
731_8	$L4TRK:	170	MOV A,B	A = B, get Disk control	
		327 100	RST 2	Carry is always set sets Head Load Bit in Disk Control	
		220	SUB B	A = A - B check if head still loaded!	
		170	MOV A,B	A = B New Disk control	
		323 40	OUT 40_8	send control to Disk	
		62 2 10	STA : 4002_8	store Disk Control @ 4002	
		302 354 1	JNZ $STP ($754_8$)	if head was not Loaded go - step to Track	
		15	DCR C	C = C - 1 ; are we at correct track portion ?	
		372 377 1	JM ATTRK (777_8)	if at track - branch	
7		123	MOV D, E	Set D = 0	
		14	INR C	Restore C (= C+1)	
754_8	$STP:	315 123 2	CALL STEP ($1123)_8$	go - step head to Correct Track !	
		76 16	MVI A #16	} go wait 14ms	
		357	RST 5		

Addrss

762_8

777_8

1001_8

Addrss

762_8	25	DCR D	check if Head Loaded
	372 377 1	JM ATTRK	if so - branch ahead
	76 25	MVI A #25	else compute remaining time delay to get head Loaded
	222	SUB D	A = A - D
	222	SUB D	A = A - D
	222	SUB D	A = A - 6 * D
	222	SUB D	
	222	SUB D	
	222	SUB D	
	357	RST 5	go wait A msec.
777_8 ATTRK:	123	MOV D, E	Set D = 0
	153	MOV L, E	Set L = 0
1001_8 $LPS:	315 36 2	CALL SCTRID (1036_8)	Searches for Sector ID mark returns when Sector found

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Addrs

1004_8 365 PUSH PSW Save A & Flags

170 MOV A,B A=B = Sector #

276 CMP M are we at the correct Sector?

312 JZ FNDSTR (1023_8) if we are — branch
23
2

361 POP PSW restor A & Flags

24 INC D } allow only 64 attempts
24 INC D }

362 JP $LPS ($1001_8$) go try again
1
2

315 CALL $7Ø Error - Sector not found in
310 2 revolutions !
2

1023_8 FNDSTR: 361 POP PSW get A & Flags

334 CC $140 ($130_8$) Error — CRC Error in Header
303
2

54 INR L point @ Track #

171 MOV A,C

276 CMP M are we at correct Track?

304 CNZ $150 ($130_8$) Error — wrong track in header
302
2

311 RET else OK - return to Caller

Addrs

1036_8

1041_8

Find SECTOR ID Routine

Addrs

1036_8	SCTRID:	1 350 3	LXI B *1750_8	B = 3 C = 350	allowed count to find Preamble
1041_8	$LP6:	13	DCX B	decrement on each try!	
		170	MOV A,B		
		273	CMP E	timed out yet?	
		314 305 2	CZ $120	yes - error could not find preamble	
		333 14	IN 14		
		273	CMP E	find a Zero Byte?	
		302 41 2	JNZ $LP6 ($1041_8$)	if not go try again	
		333 4	IN 4	if we did - setup to read a RDMK	
		333 15	IN 15	find RDMK	
		376 376	CPI H376	was it a sector ID Mark?	
		302 41 2	JNZ $LP6 ($1041_8$)	if not - go try again	

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Address

Add 10668

```
333   IN 7          Read status
 7
346   ANI #40       was RDMK Detected ?
 40
302   JNZ $LP6      (1041₈) if not - go try again
 41
 2
333   IN 16         get Track Address
 10
117   mov C,A       C = Track Address
333   IN 1Φ         get next Byte (should be = Φ)
 1Φ
333   IN 1Φ         get Sector Address
 1Φ
107   mov B,A       B = Sector Address
333   IN 1Φ         get next Byte (should be = Φ)
 1Φ
333   IN 1Φ         } Read CRC Bytes
 1Φ
333   IN 1Φ         }
 1Φ
333   IN 1Φ         Read one extra Byte
 1Φ                 to allow shift of last CRC Byte through
                    checker
333   IN 7          Read Status
 7
```

Addrss

1117_8	27	RAL	} get CRC check into Carry
	27	RAL	
	27	RAL	
	311	RET	Return to Caller

STep Subroutine

1123_8 STEP:	67	STC	Set carry
	15	DCR C	C is the number of Tracks to step
	370	RM	Return to caller after C steps
	347	RST 4	} generate STep pulse to Selected Unit
	347	RST 4	
	76 6	MVI A #6	load wait time
	357	RST 5	go wait for 6 ms.
	303 123 2	JMP STEP (1123_8)	loop to do more

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START / Initialization Routine

Addres				Addres
1136_8	START:	333 5	IN 5	a) reset RDMK Sync b) clear Done F/F	1164_8
		333 4	IN 4	c) set Done F/F	
		371	SPHL	Load stack pointer from H & L ie = 4176_8	
		76 4	MVI A	same * 4 in memory	
		62 177 10	STA @4177		
		227	SUB A	clear A & Carry	
		157	MOV L, A	Set L = Ø	
		127	MOV D, A	Set D = Ø	
		74	INR A	A = 1	
		167	MOV M, A	@4000 = 1 [Sector Address]	
		43	INX H	increment memory pointer	
		167	MOV M, A	@4001 = 1 [Track Address]	
		6 2Ø	MVI B	set B = 2Ø for Unit Ø	
		315 200 2	CALL INIT (12Ø)	go initialize to Track Ø	

Address

1164_8	227	SUB A	set A = 0
	323 40	OUT 40	Clear Disk Control Register
	127	MOV D, A	set D = 0
	6 40	MVI B #40	B = 40 for unit 1
	315 200 2	CALL INIT (1200_8)	go initialize to track 0
	303 247 2	JMP FINIT $(1247)_8$	go finish initialization

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INIT TO TRACH ∅ Routine

Address				
1200_8	INIT:	67	STC	Set carry Bit
		327 2	RST 2	Set 'seek in' Bit of Control (Breg)
		16 12	MVI C	get 12 into C
		315 123 2	CALL STEP (1123_8)	Do 12 steps IN!
		227	SUBA	Clear A & carry
		327 2	RST 2	clear 'seekin' Bit of Control (Breg)
		116	MOV C,M	C = 1 # of steps
	$LP7:	315 123 2	CALL STEP (1123_8)	single step out to find track ∅
		116	MOV C,M	C = 1 # of steps
		76 20	MVI A #20	} wait 20 ms.
		357	RST 5	
		24	INR D	increment # of steps performed
		362 235 2	JP $TRK∅ ($1235_8$)	if less than 128 steps go check if were at TRK∅

Address 1227_8

Address 1235_8

Addrss

else we have not found TRHϕ

1227_8		170	MOV A, B	get control	this code is supposed to detect if unit 1 did not find TRHϕ — this code doesn't work !!!
		273	CMP E	B = ϕ ?	
		314 316 2	CZ $10	Error —	
		300	RNZ	Return to Caller	
1235_8	TRK\phi$:	333 7	IN 7	Read STATUS	
		27	RAL:	rotate TRHϕ bit into Carry	
		27	RAL		
		27	RAL		
		27	RAL		
		332 214 2	JC $LP7	if not track ϕ Loop	
		311	RET	Return to Caller when @TRHϕ	

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Finish Initialization Routine

Addrs					Addrs
					1303_8
1247_8	FINIT:	227	SUB A	clear A & carry	
		62 3 10	STA @4003	Set Unit 1 @ Trak Ø	
		62 23 1Ø	STA @4023	Set Unit Ø @ Trak 1	
		315 370 3	CALL PTCHA 1770	initialize for Unit 1 & check for ready	
		332 343 2	JC EXIT (1343_8)	if Unit 1 not ready skip read	
		176	MOV A, M	Set A = 1 (Track 1 is where we are going) @4001 @4002 = 1 sector #	
		43	INX H	point at sector	
		Ø	NOP		
		315 251 1	CALL INITSØ (651_8)	go find Track & Sector return after finding Sector 1 Track 1 ID Header	
		315 2 1	CALL INITS1 (401_8)	go Read Data from Sector 1 Track 1 into Data Buffer	
		66 204	MOV I M	set DStatus = 204_8 @4177 = 204	
		303 343 2	JMP EXIT	go to exit routine	

Error / EXIT Routines

Address

1303_8	$150:	34	INRE	Enter with E = 0
	$140:	34	INRE	increments E to indicate
	$130:	34	INRE	Error which occurred
	$120:	34	INRE	
		34	INRE	
		34	INRE	
	$70:	34	INRE	
	$60:	34	INRE	
		34	INRE	
	$40:	34	INRE	
		34	INRE	
		34	INRE	
	$10:	34	INRE	
	$0:	227	SUB A	clear A & carry
		173	MOV A, E	set A = E
		27	RAL	} multiply A × 10_8
		27	RAL	
		27	RAL	
		62	STA @4004	store Error code
		4		
		10		

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Addres

1327_8		227	SUB A	clear A & carry
		137	MOV E,A	set E = 0
		72 2 14	LDA @4002	get Disk control word
		366 10	ORI #10	set Error Bit
		323 40	OUT 40	place error so PDP-11 can read it
		62 2 14	STA @4002	store new Disk control
1343_8	EXIT:	72 177 14	LDA @4177	get D STATUS
1346_8	ERRX:	323 20	OUT 20	place so PDP-11 can read
		323 6	OUT 6	set Done Bit for PDP-11
	FINISH:	41 176 14	LXI H 4176	Load H&L with 4176_8
		371	SPHL	Reset Stack pointer to 4176_8
		303 65 0	JMP CTLCHK (65_8)	go wait for next Command from PDP-11

Add

1361_8

1372_8

Load Boot Routine

Addrs				
1361_8	LDBOOT:	175	MOV A, L	Set A = L = 200,
		323 40	OUT 40	a) deselect Disks b) set BOOTX line will normally crash a RUNNING System
		227	SUB A	Clear A & carry
		323 40	OUT 40	disable BOOTX
		1 11 3	LXI B *BOOT	Load Boot Address into B and C $= 1411_8$
1372_8	$LP8:	12	LDA X	get data @ B, C
		323 20	OUT 20	place data in Data Register
		175	MOV A, L	get Address & BOOTX control
		323 40	OUT 40	start transfer to 11
		227	SUB A	clear A
		323 40	OUT 40	and transfer to 11
		3	INX B	increment Memory pointer
		54	INR L	increment Address
		372 372 2	JM $LP8:	Loop to transfer 128 Bytes
		311	RET	Return to Caller when finished via (343_8)

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PDP-11 Bootstrap Loader

Addres

1411_8

	300 25 64 0	12700	64	mov #64, R0
	301 25 40 2	12701	1040	mov #1040, R1
	302 25 20 0	12702	20	mov #20, R2
LOOP:	41 30	14041		mov -(R0), -(R1)
	302 12	5302		DEC R2
	375 2	1375		BNE LOOP
	111 0	111		JMP (R1)
	3 12	5003		CLR R3
	301 25 70 376	12701	177170	mov #177170, R1
LOOP2:	311 213	105711		TSTB (R1)
	376 3	1776		BEQ LOOP2

Addr

1447_8

Address

1447_8		100 20	10100	mov R1, R0
		320 25	12720	mov #111023, (R0)+
	LOOP4	23 222		[movB (R0), (R3)+]
	LOOP3	311 213	105711	TSTB (R1)
		376 3	1776	BEQ LOOP3
		374 201	100774	BMI LOOP4
		0 12	5000	CLR R0
		7 12	5007	CLR R7

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PTCHB Routine

Addres

Addres				
	STAT:			
1467_8	PTCHB:	62 2 10	STA @4002	place Unit I select
		323 40	OUT 4Ø	set Disk control Register
		333 7	IN 7	Read Disk status
		37	RAR	Rotate Ready into Carry
		311	RET	Return to Caller

Addres

1500_8

1512_8

1522_8

FORMAT Routine

Addrs				
1500_8	FORMAT:	56 1	MVI L #1	Set L = 1
		6 100	MVI B #100	Set B = 100
		165	mov M, L	Set 4001 = 1
		315 200 2	CALL INIT	go find track ø
		163	mov M, E	Set 4001 = ø
		ø	NOP	
1512_8	FORMN:	1 1 102	LXI B, #41001	Load B & C
		305	PUSH B	Save B & C on stack
		170	mov A, B	Set A = 102 ;
		323 40	OUT 4ø	load head / seek in
		125	mov D, L	Set D = 1
1522_8	$LP9:	333 7	IN 7	Wait in Loop until post INDEX mark
		346 4	ANI #4	
		312 122 3	JZ $LP9 ($1522_8$)	

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Addrs					Addrs
1531_8	$LPI0:	333 7	IN 7	} wait for beginning of INDEX mark	1564_8
		346 4	ANI #4		
		302 131 3	JNZ $LPI0 ($1531_8$)		
		6 377	MVI B # 377	all 1's Byte	
		16 117	MVI C * 117	set up to write 117_8 Bytes of 1's	
		170	mov :A, B	set A = 377	
1545_8	$LPI1:	323 10	OUT 10_8	write Byte	
		15	DCR C	C = C-1	
		302 145 3	JNZ $LPI1 ($1545_8$)	Loop to write 117_8 Bytes of 1's	
1553_8	$LPI2:	227	SUB A	clear A.	
		16 6	MVI C #6	set C = 6	
1556_8	$LPI3:	323 10	OUT 10	write Byte	
		15	DCR C	C = C-1	
		302 156 3	JNZ $LPI3 ($1556_8$)	Loop to write 6 Bytes of ϕ's	

Addrs

1564_8

76 376	MVI A # 376	Set A = 376_8 ID Address Mark
323 11	OUT 11	write ID Address Mark
72 1 10	LDA M@4001	Set A = Track Address @4001
323 14	OUT 10	write track Address
227	SUB A	Set A = 0
323 14	OUT 10	write a 0 Byte
172	MOV A, D	set A = Sector # = D
323 14	OUT 10	write Sector Address
227	SUB A	Set A = 0
323 14	OUT 10	write a 0 Byte
323 12	OUT 12	} Write CRC
323 12	OUT 12	
170	MOV A, B	Set A = 377
16 256	MVI C # 256_8	set C = 256

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Addres					Addres
1615_8	$LP14:	323 10	OUT 10	write Byte	1647_8
		15	DCR C	C = C-1	
		302 215 3	JNZ $LP14: ($1615_8$)	loop to write 256_8 Bytes of 1's	1652_8
		24	INR D	increment sector Addres	
		323 10	OUT 10	write another Byte	
		76 33	MVI A, 33_8		
		272	CMP D	is D = 33 ?	
		302 153 3	JNZ $LP12 ($1553_8$)	loop until we have written 26_{10} sectors !	
		301	POP B	restore B & C B = 102 , C = 1	
		315 123 2	CALL STEP ($1123/_8$	step to next track	
		176	MOV A, M	Set A = Track Addres	
		376 114	CPI #114	have we completed 77_{10} tracks ?	
		310	RZ	if finished Return to caller	
		303 14 0	JMP PATCH (14_8)	go increment track address and branch to FORMAT to do next track	

Diagnostic Read/Write Routine

Address

1647_8	DIAG:	56 1	MVI L #1	set L = 1
		163	MOV M, E	set 4001 = ϕ (Track Address)
1652_8	$LP1S:	315 267 3	CALL RDWR (1667_8)	go do Write then Read of one track
		56 1	MVI L #1	set L = 1
		64	INR M	increment Track Address
		176	MOV A, M	get New Track Address
		376 115	CPI #115	upto 77 yet?
		302 252 3	JNZ $LP1S	loop until all Tracks done
		317	RST 1	go restart Diagnostic

30 Aug 78
ABP

Read / Write a Sector (Part of Diagnostic)

Addrs					Addrs
1667_8	RDWR:	56 6	MVI L H6	set L = 6	1717_8
		66 373	MVI M H373	store WRMH character @ 4006, Normal Data Mark	
		103	MOV B,E	set B = Ø	
		116	MOV C,M	C = 373	
		56 200	MVI L H200	set L = 200	
1677_8	$LP16:	12	LDAX B	A = Data @ M(B,C)	
		167	MOV M,A	M@(H,L) = A	
		3	INX B	increment data address	
		54	INR L	increment buffer address	
		372 277 3	JM $LP16 ($1677_8$)	Loop to load 128 Bytes into Buffer	
		227	SUB A	Clear A & carry	
1707_8	$LP17:	365	PUSH PSW	save status	
		153	MOV L,E	Set L = Ø	
		163	MOV M,E	Set 4000 = Ø Sector Address	
1712_8	$LP18:	64	INR M	increment Sector Address	
		176	MOV A,M	A = Sector H	
		62 200 14	STA @4200	put Sector H in data	

Address

1717_8

```
54      INR L           L=1
176     mov A,M         get Tract Address
54      INR L           L=2
315     CALL INITS0!  (651_8)   go position head
251                             at track specified in A
  1

361     POP PSW     }
365     PUSH PSW    }   get carry

324     CNC WRTD    (552_8)     if carry is clear
152                             go write a sector
  1

361     POP PSW     }
365     PUSH PSW    }   get carry again

334     CC  INITS1: (402_8)     if carry is set
  2                             go read a sector
  1

153     mov L,E         set L=0
72      LDA @4200       A=@4200
200
  10

276     CMP M           is A and sector address the
                                same?
304     CNZ $60         if not - error 60!
311
  2
```

30Aug78
ARD

Addrs

1747_8

176	MOV	A, M	A = Sector #
376 32	CPI	#32	check Sector #
302 312 3	JNZ	$LP18	Loop until all sectors tried
361	POP	PSW	get carry
330	RC		if carry = 1 home completed current Track
67	STC		else home finished writing now go read track
303 307 3	JMP	$LP17	loop to do read

Addrs

1763_8

1770_8

1776_8

Addrs

176_8	2	undefined	
	176		
	376		
	32		
	302		
$177\phi_8$	PTCHA: 76	MVI A #40	select unit 1
	40		
	315	CALL PTCHB (1467_8)	set Disk control
	67		test ready from Disk
	3		
	311	RET	Return to Caller
1776_8	324	undefined	
	3		

30 Aug 78
ADD

Patch of Software (incorporated 15Oct78)

1227_8	170	mov A, B	
	376 40	CPI * 40	unit one?
	303 363 3	JMP *1763_8	go to patch

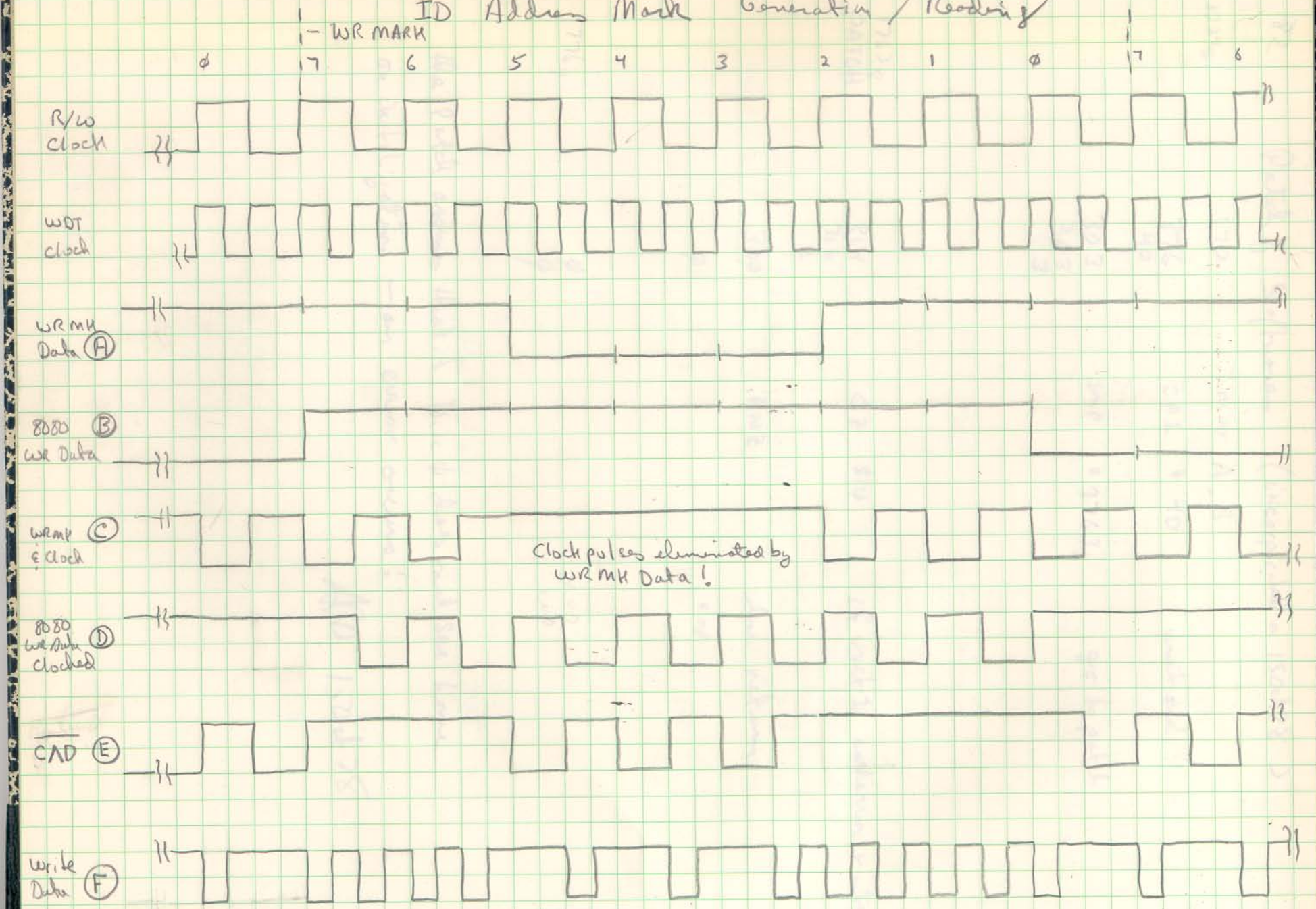
1763_8

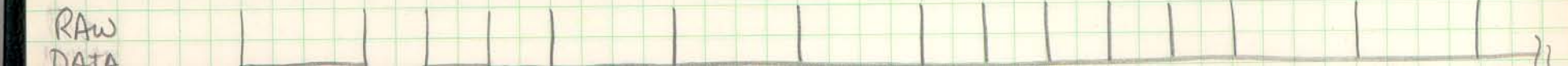
PATCH	314 316 2	CZ $14	if unit 1 call error routine
	300	RNZ	else return
	0	nop	
1776_8	0 0	nop nop	

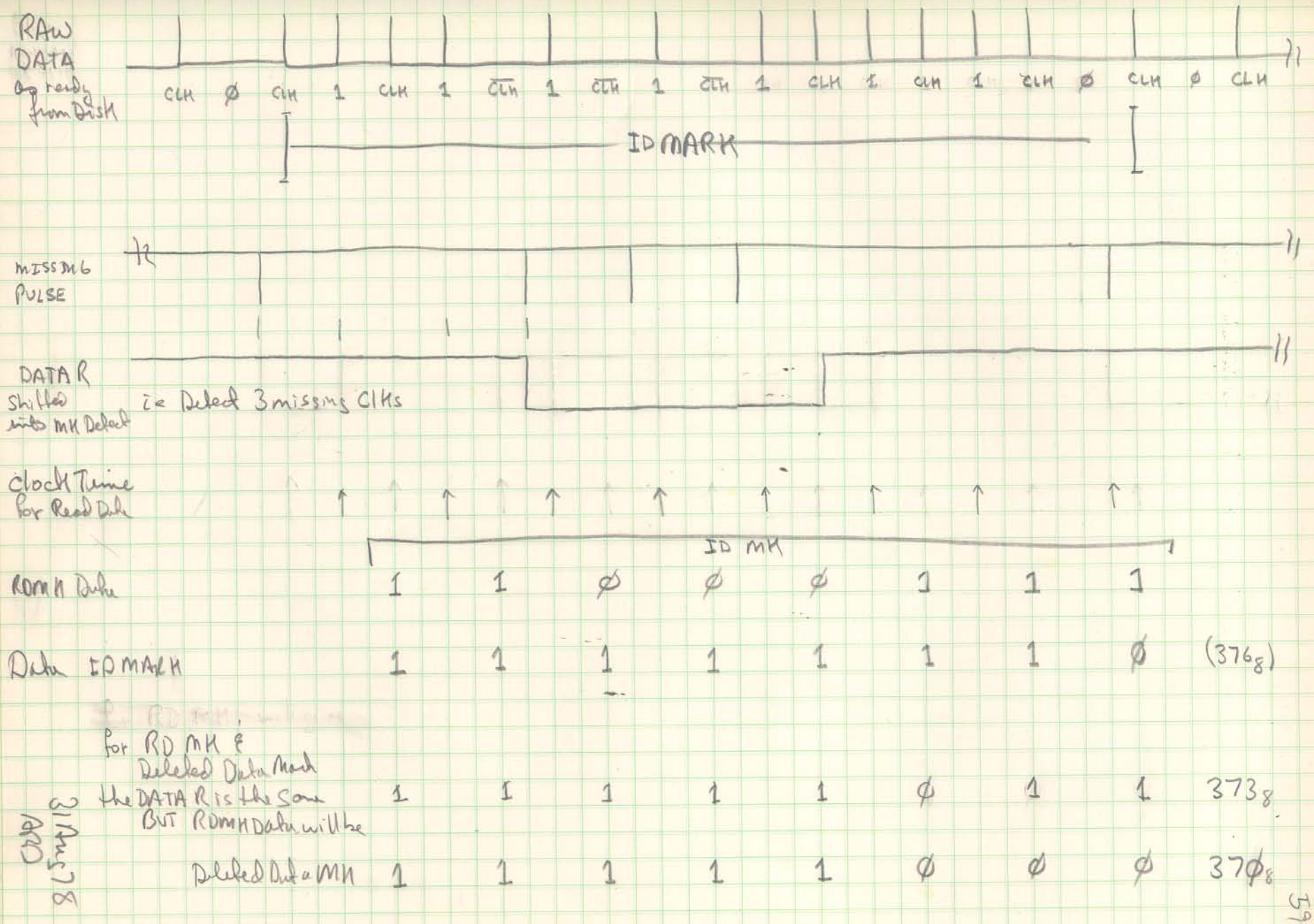
the Patch assumes that if Disc 0 does not see home on initialization — an error occurs!

ARD 15Oct78

ID Address Mark Generation / Reading






RAW DATA as read from Disk
CLK Ø CLK 1 CLK 1 CLK 1 CLK 1 CLK 1 CLK 1 CLK 1 CLK Ø CLK Ø CLK
ID MARK
MISSING PULSE
DATA R Shifted into MK Detect
i.e Detect 3 missing CLKs
Clock Time for Read Data
ID MK
ROM MK Data
1 1 Ø Ø Ø 1 1 1
Data ID MARK
1 1 1 1 1 1 1 Ø (376₈)
For RD MK & Deleted Data Mark the DATA R is the Same BUT ROM MK Data will be
1 1 1 1 1 Ø 1 1 373₈
Deleted Data MK
1 1 1 1 1 Ø Ø Ø 370₈

CRC 376₈

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SA800/801
Diskette
Storage Drive

OEM Manual

Shugart

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LIST OF ILLUSTRATIONS

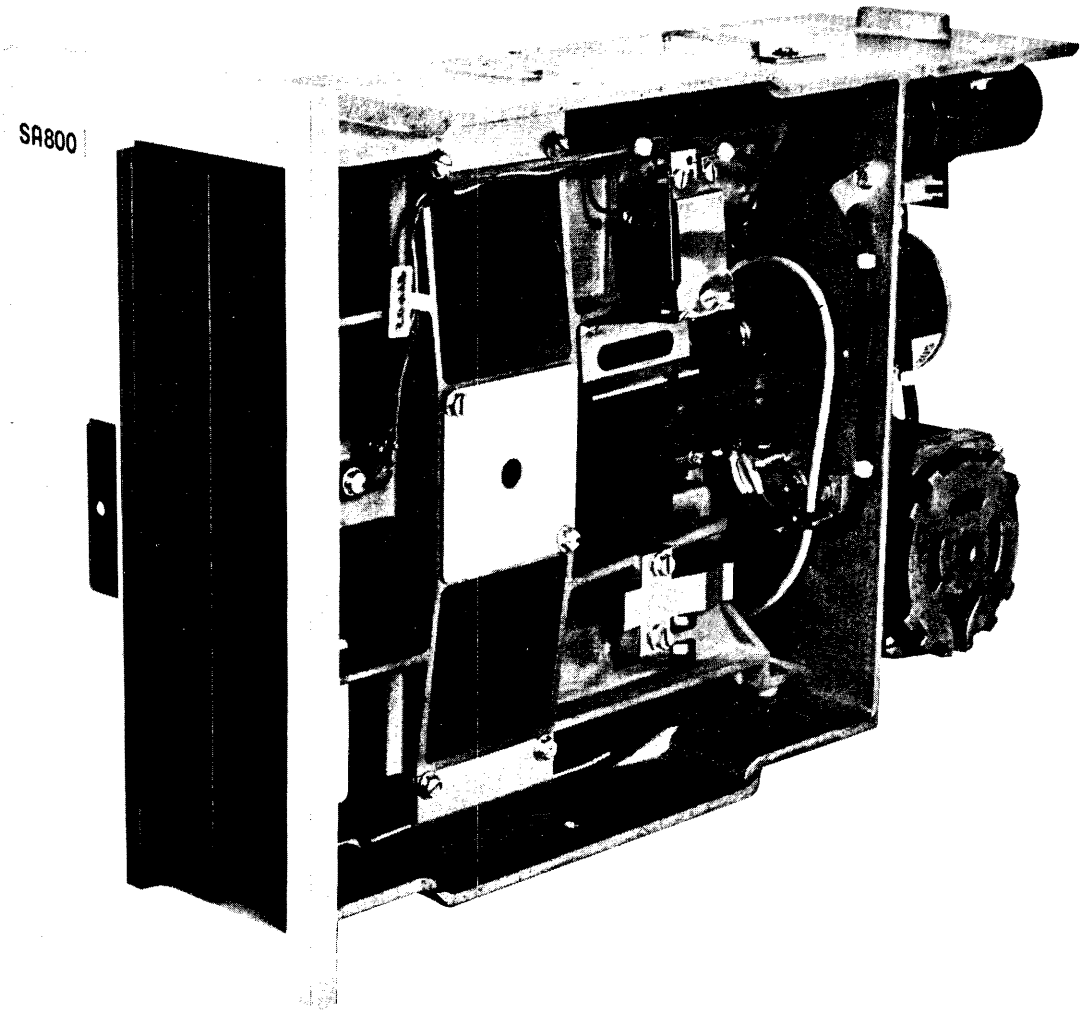


Figure 1. SA800/801 Diskette Storage Drive

1.0 INTRODUCTION

1.1 General Description

The SA800/801 are enhanced versions of the successful SA900/901 Diskette Storage Drive. The SA800/801 provides the customer with a mature and reliable product, manufactured to the same high standard of excellence as the 900/901, but with additional featuress.

The SA800 Diskette Storage Drive can read and write diskettes for interchange with other SA800's, the SA900, IBM 3741, 3742 or 3540 and with the IBM System 32.

The SA801 provides the same features as the SA800 with additional flexibility for those requirements which preclude IBM compatibility.

The SA800/801 Diskette Storage Drives have as standard features: a patented diskette clamping/registration design which eliminates the possibility of damage to the diskette due to misregistration and quarantees over 30,000 interchanges with each diskette; single and double density capability on the same drive for the same price; a proprietary ceramic R/W head designed and manufactured by Shugart Associates to provide media life exceeding 3.5 million passes/track and head life exceeding 15,000 hours; an activity light which indicates drive in use; and ribbon cable or twisted pair connector for ease of packaging. All of these features and more are available with the SA800/801.

SA800/801 Diskette Storage Drive provide the system designer solutions to his applications requirements with greater performance and reliability than cassette or cartridge drives, and lower cost with increased function over I/O and reel-to-reel tape drives.

Applications for the SA800/801 Diskette Storage Drive are key entry systems, point of sale recording systems, batch terminal data storage microprogram load and error logging, minicomputer program and auxiliary data storage, word processing systems and data storage for small business systems.

The SA100 Diskette, IBM Diskette or equivalent, can be read and written interchangeably between any SA800 and IBM 3741/42, 3747 and 3540. The SA101 Diskette can be read or written interchangeably on any SA801. The SA102 and SA103 are used for double density applications.

As a product enhancement, to improve reliability and serviceability, Shugart is incorporating into the SA800 serves drives a PCB Large Scale Integration (LSI) components. These components are:

- *Control Chip*
- *Write Channel*
- *Read Channel*

The LSI Control chip performs the following functions:

- *TRK 00 detector*
- *Index detector*
- *Stepper logic*
- *FM clock/data separator and data window*
- *Sector separator*
- *Write Protect detector*
- *Door open/close detector*
- *Disk change circuit*
- *Ready signal*

The functions listed above are either detected from the drive mechanics or from the Host Interface. As a result, the proper logic generated by the LSI chip either will be used within the drive electronic circuit to perform stepping, read/write operations or will be fed back to the Host Interface.

Also, an internal FM data separator is incorporated inside the chip. A jumper option will allow the user to select the data separator to perform as its predecessor SA800 (jumper FS) or to select the separator to be compatible with the IBM System 3740 data separator (jumper TS). Thus IBM compatibility will allow direct interfacing with LSI single chip floppy disk controllers.

1.2 Specification Summary

1.2.1 Performance Specifications

	Single Density	Double Density
Capacity		
Unformatted		
Per Disk	3.2 megabits	6.4 megabits
Per Track	41.7 kilobits	83.4 kilobits
IBM Format		
Per Disk	2.0 megabits	n/a
Per Track	26.6 kilobits	n/a
Tranfer Rate	250 kilobits/sec.	500 kilobits/sec
Latency (average)	83 ms	83 ms
Access Time		
Track to Track	8 ms	8 ms
Average	260 ms	260 ms
Settling Time	8 ms	8 ms
Head Load Time	35 ms	35 ms

1.2.2 Functional Specifications

	Single Density	Double Density
Rotational Speed	360 rpm	360 rpm
Recording Density		
(inside track)	3200 bpi	6400 bpi
Flux Density	6400 fci	6400 fci
Track Density	48 tpi	48 tpi
Tracks	77	77
Physical Sectors		
SA800	0	0
SA801	32/16/8	32/16/8
Index	1	1
Encoding Method	FM	MFM/M^{2}FM
Media Requirements		
SA800	SA100/IBM Diskette	SA102/IBM Diskette
SA801	SA101	SA103

1.2.3 Physical Specifications

Enviromental Limits	**Operating**	**Shipping**	**Storage**
Ambient Temperature	= 40°F to 115°F (4.4° to 46.1°C)	-40°F to 144°F	-8°F to 117°F
Relative Humidity	= 20% to 80%	1 to 95%	1 to 95%
Maximum Wet Bulb	= 78°F (25°C)	No Condensation	No Condensation

AC Power Requirements
50/60 Hz ± 0.5 Hz
100/115 VAC Installations = 85 to 127V @ .3A typical
200/230 VAC Installations = 170 to 253V @ .18A typical
DC Voltage Requirements
+24 VDC ±5% 1.3A typical
+ 5 VDC ±5% 0.8A typical
† -5 VDC ±5%.05A typical (option -7 to -16 VDC)
Mechanical Dimensions (Reference Figures 18 and 20)
Width = 4 5/8 in. (11.75 cm)
Height = 9 1/2 in. (24.13 cm)
Depth = 14 1/4 in. (36.20 cm)
Weight = 13.0 lbs. (5.91 kg)
Heat Dissipation = 271 BTU/hr. typical (80 Watts)

† Minus voltages are not required for SA800L.

1.2.4 Reliability Specifications

MTBF:	5000 POH under heavy usage 8000 POH under typical usage
PM:	Every 5000 POH under heavy usage Every 15,000 under typical usage
MTTR:	30 minutes
Component Life:	15,000 POH
Error Rates:	
Soft Read Errors:	1 per 10^9 bits read
Hard Read Errors:	1 per 10^{12} bits read
Seek Errors:	1 per 10^6 seeks.
Media Life:	
Passes Per Track	3.5×10^6
Insertions:	30,000 +

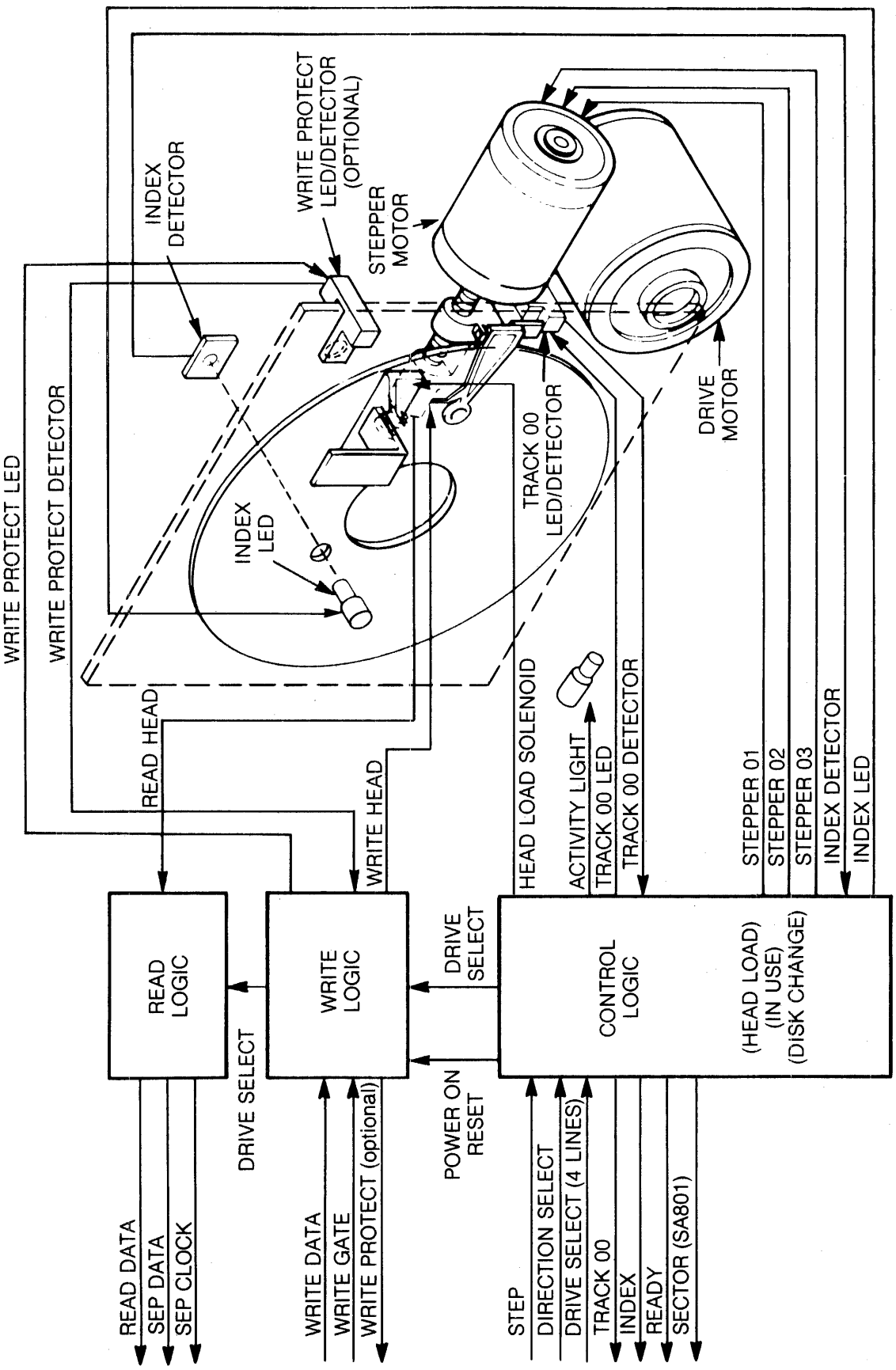


Figure 2. SA800/801 Functional Diagram

2.0 FUNCTIONAL CHARACTERISTICS

2.1 General Operation

The SA800/801 Diskette Storage Drive consists of read/write and controls electronics, drive mechanism, read/write head, track positioning mechanism, and the removable diskette. These components perform the following functions:

Interpret and generate control signals.
Move read/write head to the selected track.
Read and write data.

The relationship and interface signals for the internal functions of the SA800/801 are shown in Figure 2.

The Head Positioning Actuator positions the read/write head to the desired track on the diskette. The Head Load Actuator loads the diskette against the read/write head and data may then be recorded or read from the diskette.

2.2 Read/Write and Control Electronics

The electronics are packaged on one PCB. The PCB contains:

1. Index Detector Circuits. (Sector/Index for 801).
2. Head Position Actuator Driver.
3. Head Load Actuator Driver.
4. Read/Write Amplifier and Transition Detector.
5. Data/Clock Separation Circuits.
6. Write Protect.
7. Drive Ready Detector Circuit.
8. Drive Select Circuits.

2.3 Drive Mechanism

The Diskette drive motor rotates the spindle at 360 rpm through a belt-drive system. 50 or 60 Hz power is accommodated by changing the drive pulley and belt. A registration hub, centered on the face of the spindle, positions the Diskette. A clamp that moves in conjunction with the cartridge guide fixes the Diskette to the registration hub.

2.4 Positioning Mechanism

An electrical stepping motor (Head Position Actuator) and lead screw positions the read/write head. The stepping motor rotates the lead screw clockwise or counterclockwise in 15° increments. A 15° rotation of the lead screw moves the read/write head one track position. The using system increments the stepping motor to the desired track.

2.5 Read/Write Head

The SA800/801 head is a single element ceramic read/write head with straddle erase elements to provide erased areas between data tracks. Thus normal interchange tolerances between media and drives will not degrade the signal to noise ratio and insures Diskette interchangeability.

The read/write head is mounted on a carriage which is located on the Head Position Actuator lead screw. The Diskette is held in a plane perpendicular to the read/write head by a platen located on the base casting. This precise registration assures perfect compliance with the read/write head. The Diskette is loaded against the head with a load pad actuated by the head load solenoid.

The read/write head is in direct contact with the Diskette. The head surface has been designed to obtain maximum signal transfer to and from the magnetic surface of the Diskette with minimum head/Diskette wear.

2.6 Recording Format

The format of the data recorded on the disk is totally a function of the host system, and can be designed around the users application to best take advantage of the total available bits that can be written on any one track.

For a detailed discussion of various recording formats, the systems designer should read one of the following:

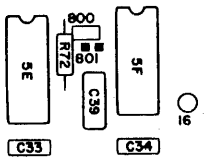
1. IBM Compatibility Manual.
2. Shugart Associates Double Density Design Guide.
3. SA801/901 Track Formats.

2.7 Optional Features

† 1. -12 to -15 Volt DC to replace -5 Volt DC requirement.
2. Dust Cover, Not available on "R"series.
3. Write Protect for SA800. Standard on SA801.
4. Door Lock. Will lock the door when drive is selected or through alternate I/O pin.
5. Horizontal mounting with door opening up.
6. SA800/801 "R" Series. Allows two drives to be horizontally installed in a standard 19" Retma rack. Reference figure 20.

2.8 Model Differences

800-1 - Soft Sectored with an FM (single density) data separator.
800-2 - Soft Sectored without data separator.
800-4 - Mechanics only (No PCB).
801 - Hard Sectored with an FM (single density) data separator and sector separator.



NOTE:

To convert a 801 to a 800 move the shorting plug from the 801 position to the 800 position. A 800 cannot be converted to a 801.

† Minus voltages are not required for SA800L.

3.0 FUNCTIONAL OPERATIONS

3.1 Power Sequencing

Applying AC and DC power to the SA800/801 can be done in any sequence, however, once AC power has been applied, a 2 second delay must be introduced before any Read or Write operation is attempted. This delay is for stabilization of the Diskette rotational speed. Also, after application of DC power, a 90 millisecond delay must be introduced before a Read, Write, or Seek opration or before the control output signals are valid. After powering on, initial position of the R/W head with respect to data tracks is indeterminant. In order to assure proper positioning of the R/W head prior to any read/write operation after powering on, a Step Out operation should be performed until the Track 00 indicator becomes active.

3.2 Drive Selection

Drive selection occurs when a drive's Drive Select line is activated. Only the drive with this line active will respond to input lines or gate output lines. Under normal operation, the Drive Select line will load the R/W head, apply power to the stepper motor, enable the input lines, activate the output lines and light the Activity LED on the front of the drive. Optional modes of operation are available. Reference section 7 for these user installable features.

3.3 Track Accessing

Seeking the R/W head from one track to another is accomplished by:

a. Activating Drive Select line.
b. Selecting desired direction utilizing Direction Select line.
c. Write Gate is being inactive.
d. Pulsing the Step line.

Multiple track accessing is accomplished by repeated pulsing of the Step line until the desired track has been reached. Each pulse on the Step line will cause the R/W head to move one track either in or out depending on the Direction Select line. Head movement is initiated on the trailing edge of the Step Pulse.

3.3.1 Step Out

With the Direction Select line at a plus logic level (2.5V to 5.25V) a pulse on the Step line will cause the R/W head to move one track away from the center of the disk. The pulse(s) applied to the Step line and Direction Select line must have the timing characterisitics shown in Figure 3.

3.3.2 Step In

With the Direction Select line at a minus logic level (0V to .4V), a pulse on the Step line will cause the R/W head to move one track closer to the center of the disk. The pulse(s) applied to the Step line must have the timing characterisitics shown in Figure 3.

3.4 Read Operation

Reading data from the SA800/801 Diskette Storage drive is accomplished by:

a. Activating Drive Select line.
b. Write Gate being inactive.

The timing relationships required to initiate a read sequence are shown in Figure 4. These timing specifications are required in order to guarantee that the R/W head position has stabilized prior to reading.

The timing of the read signals, Read Data, Separated Data, and Separated Clock are shown in Figure 5.

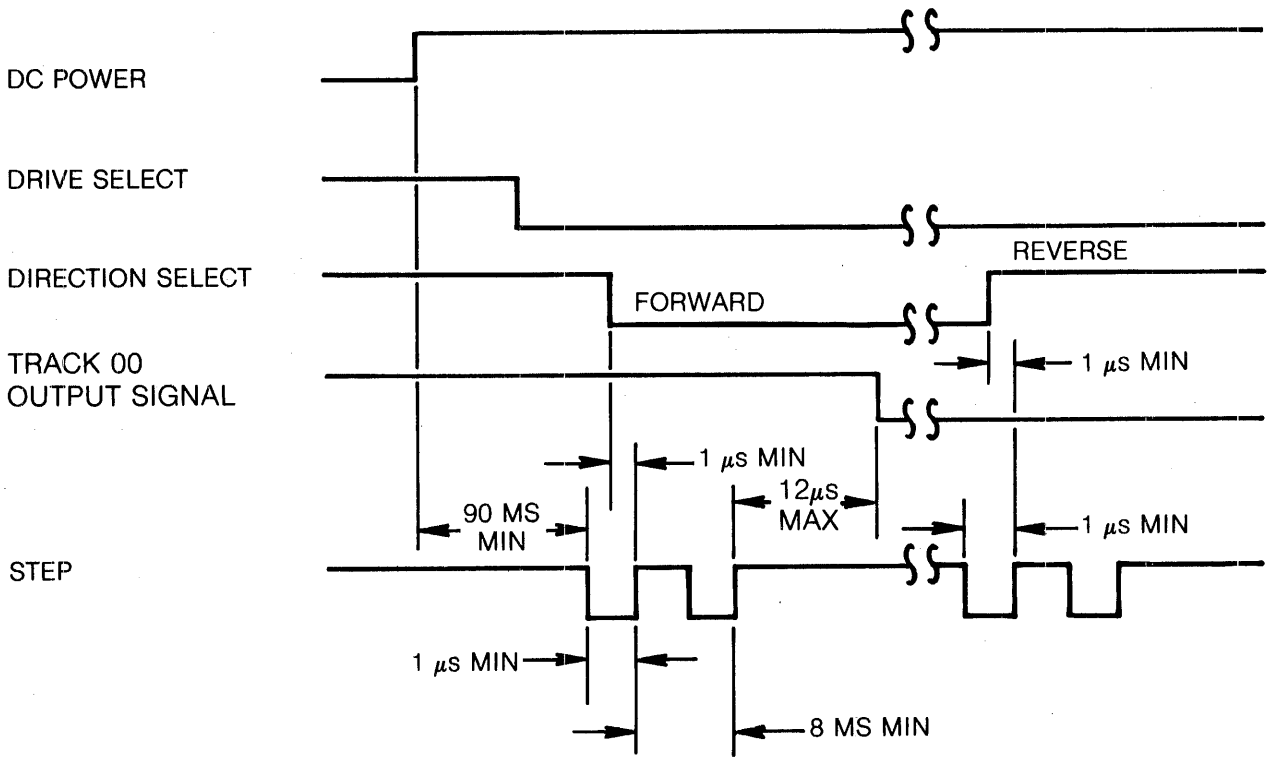
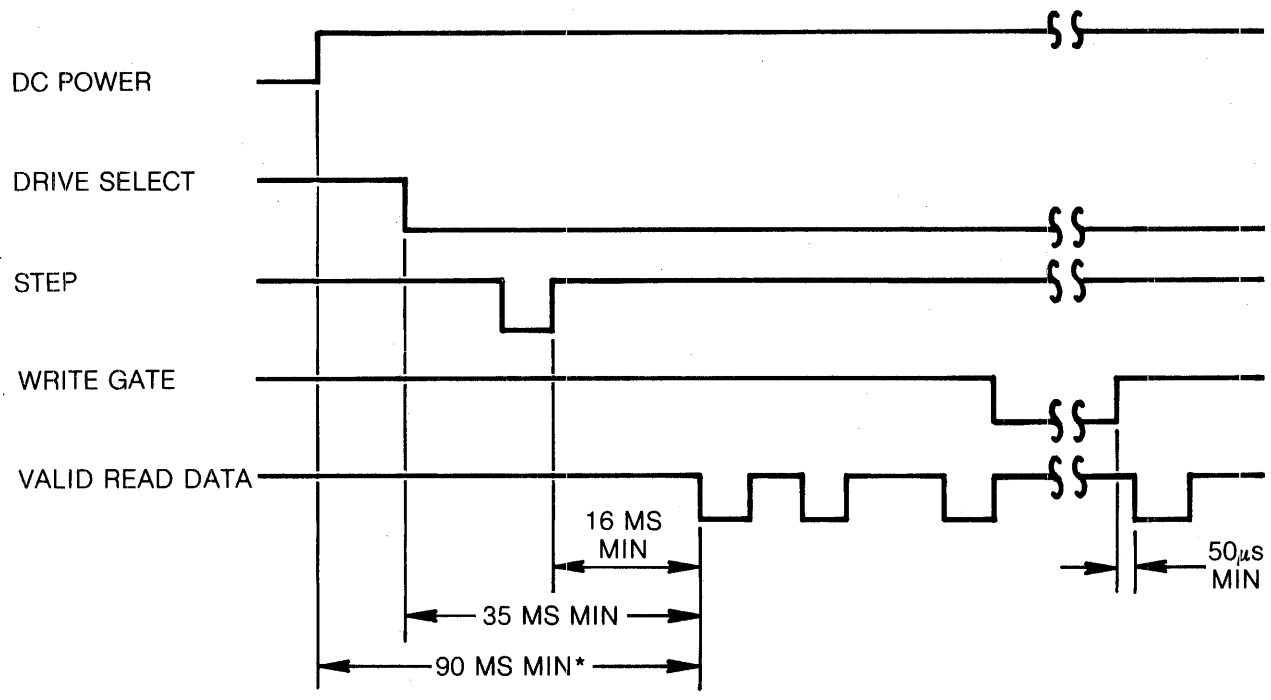
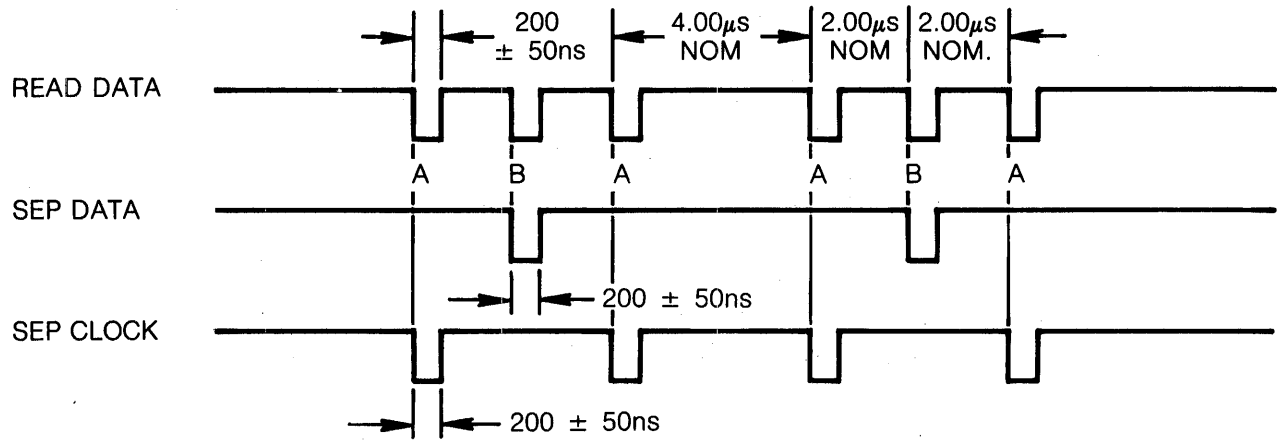


Figure 3. Track Access Timing



* 2 SECONDS IF AC AND DC POWER ARE APPLIED AT SAME TIME

Figure 4. Read Initiate Timing



A = LEADING EDGE OF BIT MAY BE ± 400 ns FROM ITS NOMINAL POSITION.
B = LEADING EDGE OF BIT MAY BE ± 200 ns FROM ITS NOMINAL POSITION.

Figure 5. Read Signal Timing

3.5 Write Operation

Writing data to the SA800/801 is accomplished by:

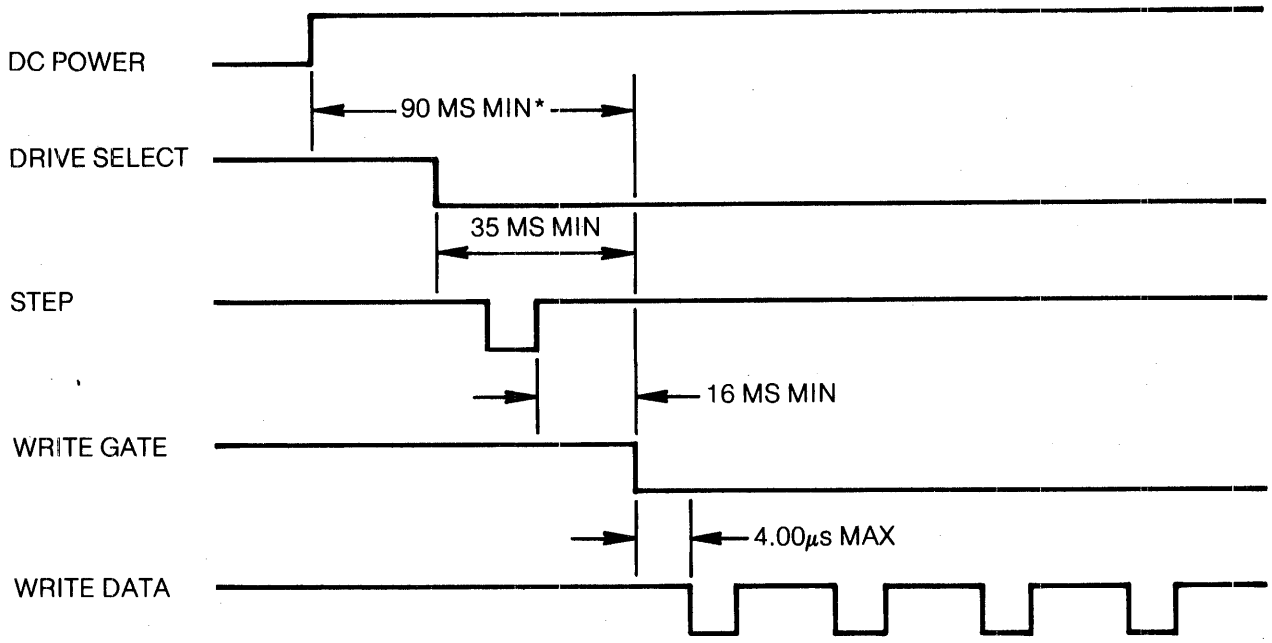
a. Activating the Drive Select line.
b. Activating the Write Gate line.
c. Pulsing the Write Data line with the data to be written.

The timing relationships required to initiate a write data sequence are shown in Figure 6. These timing specifications are required in order to guarantee that the R/W head position has stabilized prior to writing.

The timing specifications for the Write Data pulses are shown in Figure 7.

3.6 Sequence of Events

The timing diagram shown in Figure 8 shows the necessary sequence of events with associated timing restrictions for proper operation.



* 2 SECONDS IF AC AND DC POWER ARE APPLIED AT SAME TIME.

Figure 6. Write Initiate Timing

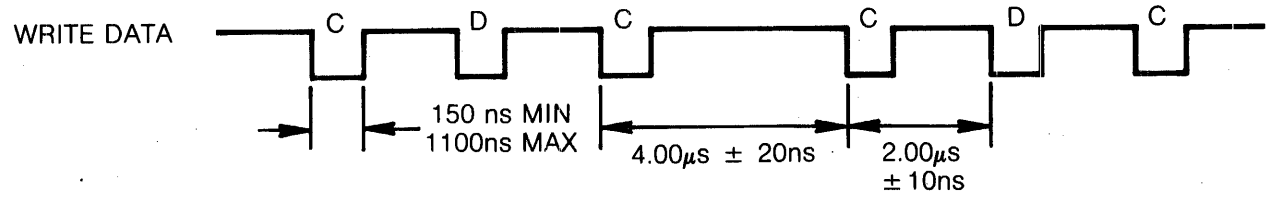
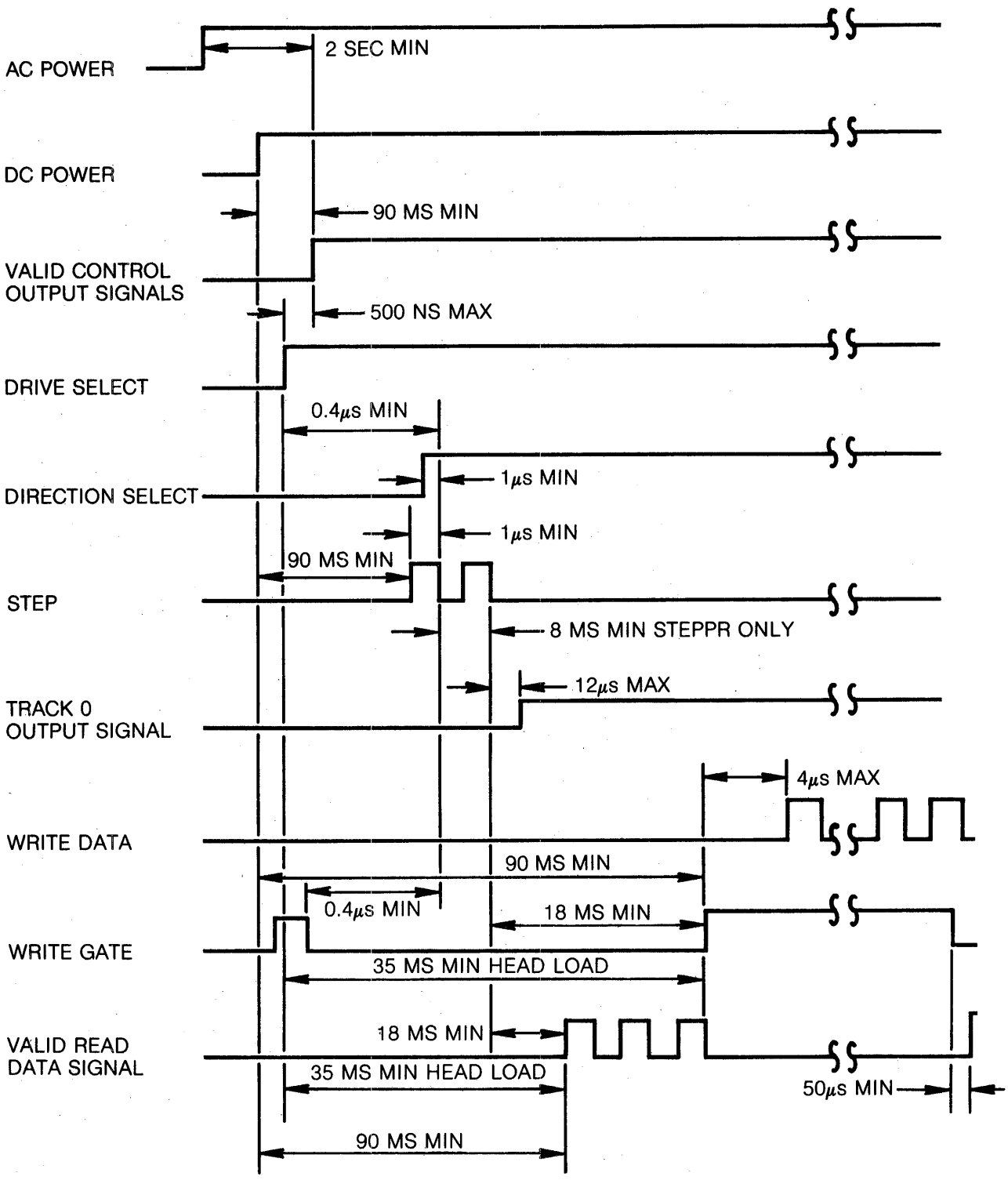


Figure 7. Write Data Timing



NOTE 1: 35ms minimum delay must be introduced after Drive Select to allow for proper head load settling. If stepper power is to be applied independent of Head Load, than and 8ms minimum delay must be introduced to allow for stepper settling.

General Control and Data Timing Requirements

4.0 ELECTRICAL INTERFACE

The interface of the SA800/801 Diskette drive can be divided into two categories:

1. Signal
2. Power

The following sections provide the electrical definition for each line.

Reference Figure 9 for all interface connections.

4.1 Signal Interface

The signal interface consists of two categories:

1. Control
2. Data Transfer

All lines in the signal interface are digital in nature and either provide signals to the drive (input), or provide signals to the host (output), via interface connector P1/J1.

4.1.1 Input Lines

There are ten signal input lines, eight are standard and two are user installable options (reference section 7).

The input signals are of two types, those intended to be multiplexed in a multiple drive system and those which will perform the multiplexing. The input signals to be multiplexed are:

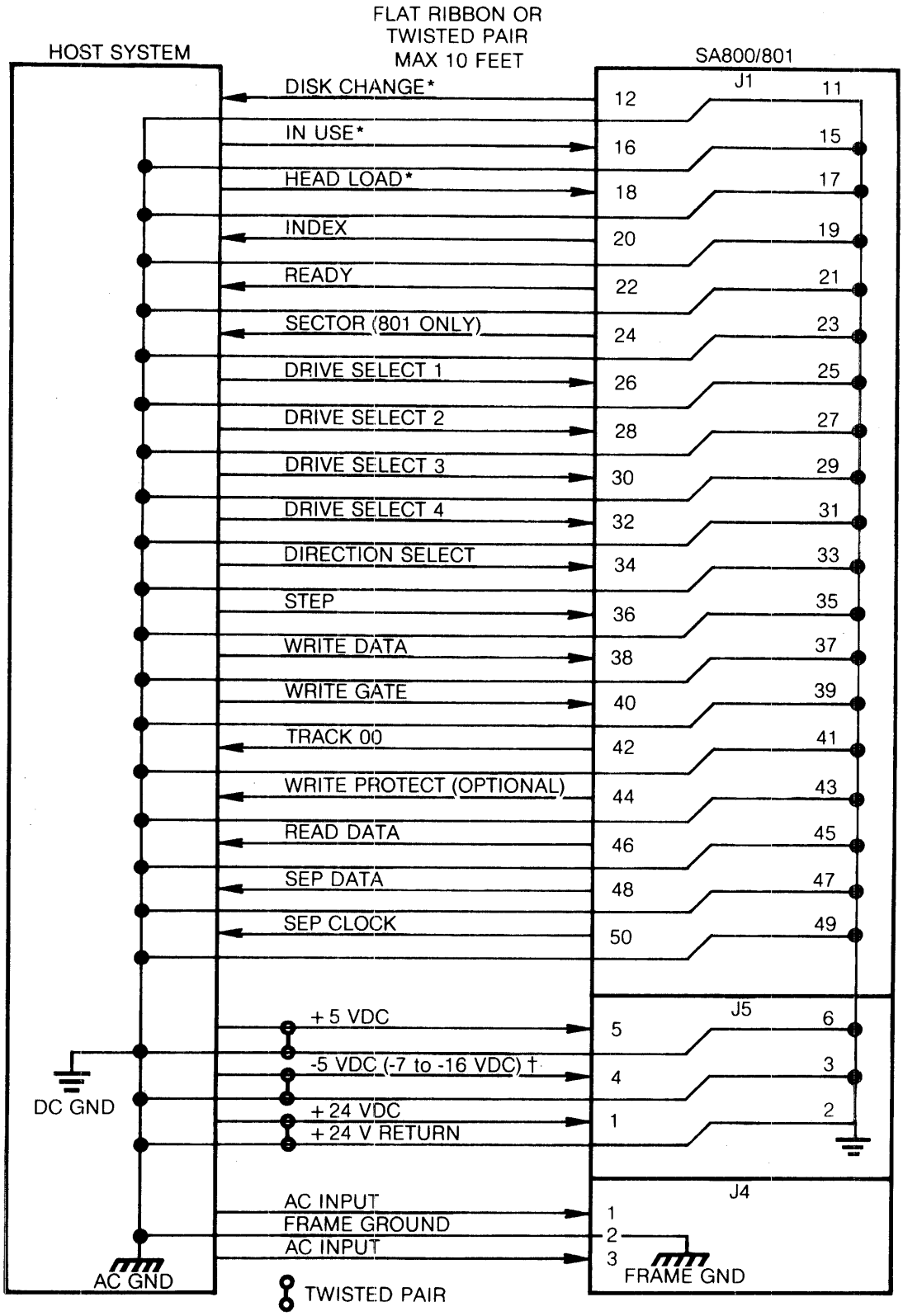
1. Direction Select
2. Step
3. Write Data
4. Write Gate

The input signals which are intended to do the multiplexing are:

1. Drive Select 1
2. Drive Select 2
3. Drive Select 3
4. Drive Select 4

The input lines have the following electrical specifications. Reference Figure 10 for the recommended circuit.

True = Logical zero = Vin ± 0.0V to + 0.4V
@ Iin = 40 ma (max)
False = Logical one = Vin + 2.5V to + 5.25V
@ Iin = 0 ma (open)
Input Impedence = 150 ohms



NOTE: Not shown are 5 of the 9 Alternate I/O connections. The connections for these lines are on pins 2, 4, 6, 8, 10 and 14. Signal return for these lines are on pins 1, 3, 5, 7, 9 and 13 respectively. Reference Section 7 for uses of these lines.

*These lines are alternate input/output lines and they are enabled by jumper plugs. Reference Section 7 for uses of these lines.

† Minus voltages are not required for SA800L.

Figure 9. Interface Connections

4.1.1 Input Line Termination

The SA800/801 has been provided with the capability of terminating the four input lines, which are meant to be multiplexed, by jumpering traces. The four lines and their respective jumpering traces are:

1. Direction Select . . . . . Trace "T3"
2. Step . . . . . Trace "T4"
3. Write Data . . . . . Trace "T5"
4. Write Gate . . . . . Trace "T6"

In order for the drive to function properly, the last drive on the interface must have these four lines terminated. Termination of these four lines can be accomplished by either of two methods.

1. As shipped from the factory, jumpers are installed on the terminator posts T3, T4, T5, and T6. Remove these shorting plugs from all drives except the last one on the Interface.

2. External termination may be used provided the terminator is beyond the last drive. Each of the four lines should be terminated by using a 150 ohm, ¼ watt resistor, pulled up to +5 VDC.

4.1.1.2 Drive Select 1-4

Drive Select when activated to a logical zero level, activates the multiplexed I/O lines and loads the R/W head. In this mode of operation only the drive with this line active will respond to the input lines and gate the output lines.

Four separate input lines, Drive Select 1, Drive Select 2, Drive Select 3, and Drive Select 4, are provided so that up to four drives may be multiplexed together in a system and have separate Drive Select lines. Traces 'DS1', 'DS2', 'DS3', and 'DS4' have been provided to select which Drive Select line will activate the interface signals for a unique drive. As shipped from the factory, a shorting plug is installed on 'DS1'. To select another Drive Select line, this plug should be moved to the appropriate 'DS' pin. For additional methods of selecting drives, see section 7.1.

4.1.1.3 Direction Select

This interface line is a control signal which defines direction of motion the R/W head will take when the Step line is pulsed. An open circuit or logical one defines the direction as "out" and if a pulse is applied to the Step line the R/W head will move away from the center of the disk. Conversely, if this input is shorted to ground or a logical zero level, the direction
of motion is defined as "in" and if a pulse is applied to the step line, the R/W head will move towards the center of the disk.

4.1.1.4 Step

This interface line is a control signal which causes the R/W head to move with the direction of motion as defined by the Direction Select line.

The access motion is initiated on each logical zero to logical one transition, or the trailing edge of the signal pulse. Any change in the Direction Select line must be made at least 1 μs before the trailing edge of the Step pulse. The read/write head may be prevented from stepping past track 00 by using the "NFO" trace option on LSI PCB. Refer to Figure 3 for these timings. **Note:** When going from a reverse seek to a forward seek or vice versa and additional 8 ms delay must be induced before changing direction.

4.1.1.5 Write Gate

The active state of this signal, or logical zero, enables Write Data to be written on the diskette. The inactive state, or logical one, enables the read data logic (Separated Data, Separated Clock, and Read Data) and stepper logic. Refer to Figure 6 for timings.

4.1.1.6 Write Data

This interface line provides the data to be written on the diskette. Each transition from a logical one level to a logical zero level, will cause the current through the R/W head to be reversed thereby writing a data bit. This line is enabled by Write Gate being active. Refer to Figure 7 for timings.

4.1.1.7 Head Load (Alternate Input)

This customer installable option, when enabled by jumpering Trace 'C' and activated to a logical zero level and the diskette access door is closed, will load the R/W head load against the diskette. Refer to section 7 for uses and method of installation.

4.1.1.8 In Use (Alternate Input)

This customer installable option, when enabled by jumpering Trace 'D' and activated to a logical zero level will turn on the Activity LED in the door push button. This signal is an "OR" function with Drive Select. Refer to section 7.8 for uses and method of installation.

4.1.2 Output Lines

There are six standard and one optional output lines from the SA800, and eight output lines from the SA801. Also, there is one Alternate Output available from the drive. The output signals are driven with an open collector output stage capable of sinking a maximum of 40 ma at a logical level or true state with a maximum voltage of 0.4V measured at the driver. When the line driver is off and the collector current is a maximum of 250 microamperes.

Refer to Figure 10 for the recommended circuit.

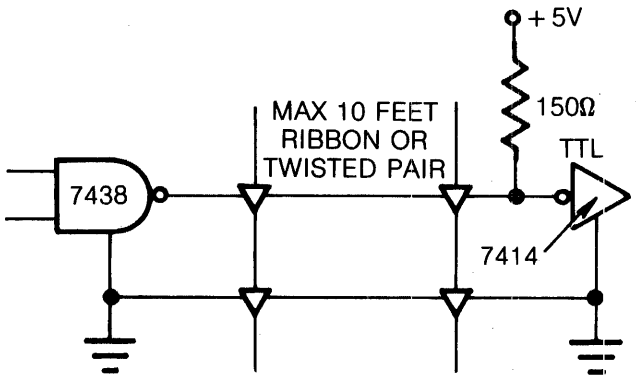


Figure 10. Interface Signal Driver/Receiver

4.1.2.1 Track 00

The active state of this signal, or a logical zero indicates when the drives R/W head is positioned at track zero (the outermost track) and the access circuitry is driving current through phase one of the stepper motor. This signal is at a logical one level, or false state, when the selected drives R/W head is not at track 00.

4.1.2.2 Index

This interface signal is provided by the drive once each revolution of the diskette (166.67 ms) to indicate the beginning of the track. Normally this signal is a logical one and makes the transition to the logical zero level for a period of 1.7 ms (0.4 ms on SA801) once each revolution. The timing for this signal is shown in Figure 11.

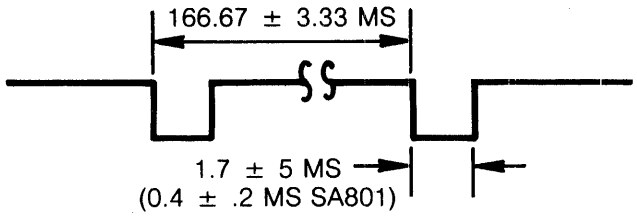


Figure 11. Index Timing

To correctly detect Index at the Host Index should be false at Drive Select time, that is, the Host should see the transition from false to true after the drive has been selected.

For additional methods of detecting Index, refer to section 7.6.

4.1.2.3 Sector (SA801 only)

This interface signal is provided by the drive 32 times each revolution. Normally, this signal is a logical one and makes the transition to a logical zero for a period of 0.4 ms each time a sector hole on the Diskette is detected. Figure 12 shows the timing of this signal and its relationship to the Index pulse.

For additional methods of detecting Sector refer to section 7.7.

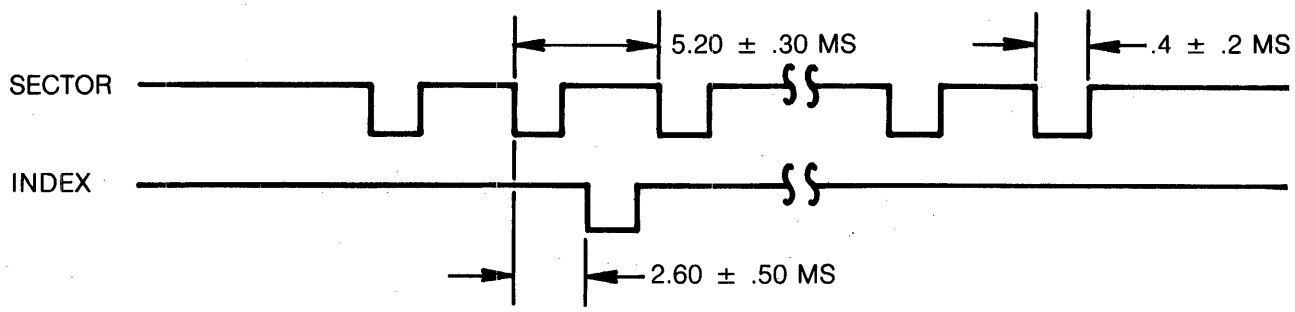


Figure 12. Sector Timing

4.1.2.4 Ready

This interface signal indicates that two index holes have been sensed after properly inserting a diskette and closing the door, or that two index holes have been sensed following the application of +5V power to the drive.

For additional methods of using the Ready line, refer to section 7.5.

4.1.2.5 Read Data

This interface line provides the "raw data" (clock and data together) as detected by the drive electronics. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference Figure 5 for the timing and bit shift tolerance within normal media variations.

4.1.2.6 Sep Data

This interface line furnishes the data bits as separated from the "raw data" by use of the internal data separator. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference Figure 5 for the timing. This line is available on the SA801 and 800 Model 1.

4.1.2.7 Sep Clock

This interface line furnishes the clock bits as separated from the "raw data" by use of the internal data separator. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference Figure 5 for the timing. This line is available on the SA801 and 800 Model 1 and PCB 25136.

NOTE: True separation internally inserting up to three missing clock bits to maintain synchronization, is available on the LSI PCB by using trace option "TS".

4.1.2.8 Write Protect (Optional on SA800)

This interface signal is provided by the drive to give the user an indication when a Write Protected Diskette is installed. The signal is logical zero level when it is protected. Under normal operation, the drive will inhibit writing with a protected diskette installed in addition of notifying the interface.

For other methods of using Write Protect, refer to section 7.9.

4.1.2.9 Disk Change (Alternate Output)

Reference section 7.10.

4.1.3 Alternate I/O Pins

These interface pins have been provided for use with customer installable options. Refer to section 7 for methods of use.

4.2 Power Interface

The SA800/801 Diskette Storage Drive requires both AC and DC power for operation. The AC power is used for the spindle drive motor and the DC power is used for the electronics and the stepper motor.

4.2.1 AC Power

The AC power to the drive is via the connector P4/J4 located to the rear of the drive and below the AC motor capacitor. The P4/J4 pin designations are outlined below for standard as well as optional AC power.

P4 PIN	60 Hz		50 Hz	
	115 V (Standard)	208/230 V	110V	220V
1	85-127 VAC	170-253 VAC	85-127 VAC	170-253 VAC
2	Frame Gnd	Frame Gnd	Frame Gnd	Frame Gnd
3	85-127 V Rtn	170-253 V Rtn	85-127 V Rtn	170-253 V Rtn
MAX CURRENT	0.35 Amps	0.23 Amps	0.35 Amps	0.23 Amps
FREQ TOLERANCE	±0.5 Hz		±0.5 Hz	

4.2.2 DC Power

DC power to the drive is via connector P5/J5 located on non-component side of PCB near the P4 connector. The three DC voltages and their specifications along with their P5/J5 pin designators, are outlined below.

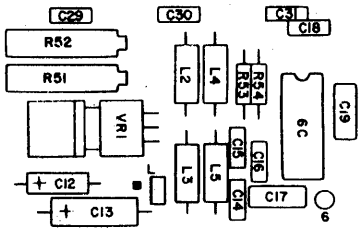
P5 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (p to p)
1	+24 VDC	±1.2 VDC	1.7 A Max** 1.3 A Typ	100 mv
2	+24 V Return*			
3	- 5 V Return			
† 4	- 5 VDC	±0.25 VDC	0.07 A Max 0.05 A Typ	50 mv
	Optional -7 to -16 VDC (trace 'L')***	NA	0.10 A Max 0.07 A Typ	NA
5	+ 5 VDC	±0.25 VDC	1.0 A Max 0.8 A Typ	50 mv
6	+ 5 V Return			

*The +24 VDC power requires a separate ground return line. It, and all other DC grounds must be connected together at the power supply. One line from this common DC connection must go to one common Frame Ground connection near the power supply.

**If either customer installable option described in sections 7.2 and 7.4 are used, the current requirement for the +24 VDC is a multiple of the maximum of +24V current times the number of drives on the line.

***If the shorting plug is in the vertical position the -7 to -16 VDC option can be used. If the shorting plug is in the horizontal position, -5 VDC must be used.

† Minus voltages are not required for SA800L.



5.0 PHYSICAL INTERFACE

The electrical interface between the SA800/801 and the host system is via three connectors. The first connector, J1, provides the signal interface; the second connector, J5, provides the DC power; and the third conector, J4, provides the AC power and frame ground.

This section describes the physical connectors used on the drive and the recommended connectors to be used with them. Refer to Figure 16 for connector locations.

5.1 J1/P1 Connector

Connection to J1 is through a 50 pin PCB edge card connector. The dimensions for this connector are shown in Figure 13. The pins are numbered 1 through 50 with the even numbered pins on the component side of the PCB and the odd numbered pins on the non-component side. Pin 2 is located on the end of the PCB connector closest to the AC motor capacitor and is labeled 2. A key slot is provided between pins 4 and 6 for optional connector keying.

The recommended connectors for P1 are tabulated below.

TYPE OF CABLE	MANUFACTURER	CONNECTOR P/N	CONTACT P/N
Twisted Pair, #26 (crimp or solder)	AMP	1-583717-1	583616-5 (crimp) 58354-3 (solder)
Twisted Pair, #26 (solder term.)	VIKING	3VH25/1JN-5	NA
Flat Cable	3M "Scotchflex"	3415-0001	NA

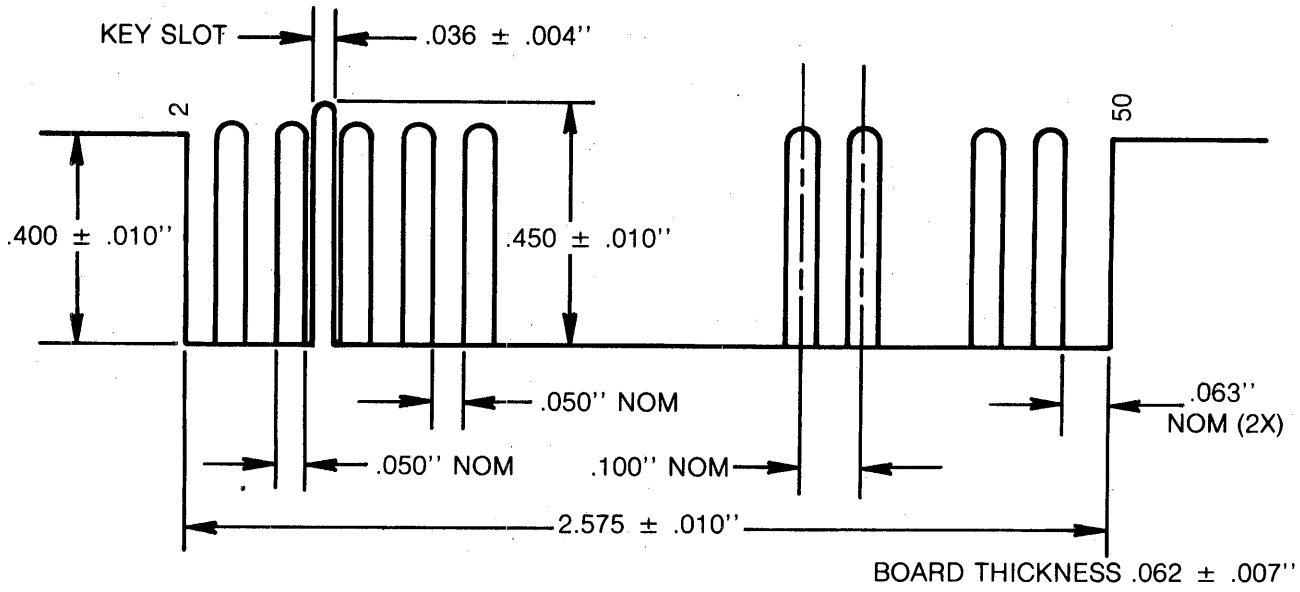


Figure 13. J1 Connector Dimensions

5.2 J5/P5 Connector

The DC power connector, J5, is mounted on the non-component side of the PCB and is located below the AC motor capacitor. J5 is a 6 pin AMP Mate-N-Lok connector P/N 1-380999-0. The recommended mating connector (P5) is AMP P/N 1-480270-0 utilizing AMP pins P/N 60619-1. J5 pins are labeled on the component side of the PCB with pin 5 located nearest J1/P1. Figure 14 illustrates J5 connector as seen on the drive PCB from non-component side.

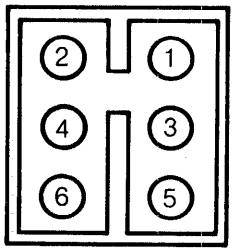


Figure 14. J5 Connector

5.3 J4/P4 Connector

The AC power connector, J4 is mounted on the AC motor capacitor bracket and is located just below the capacitor. J4 connector is a 3 pin connector AMP P/N 1-480305-0 with pins P/N 60620-1. The recommended mating connector (P4) is AMP P/N 1-480303-0 or 1-480304-0 both utilizing pins P/N 60619-1. Figure 15 illustrates J4 connector as seen from the rear of the drive.

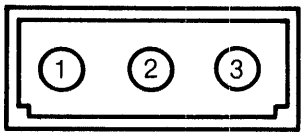


Figure 15. J4 Connector

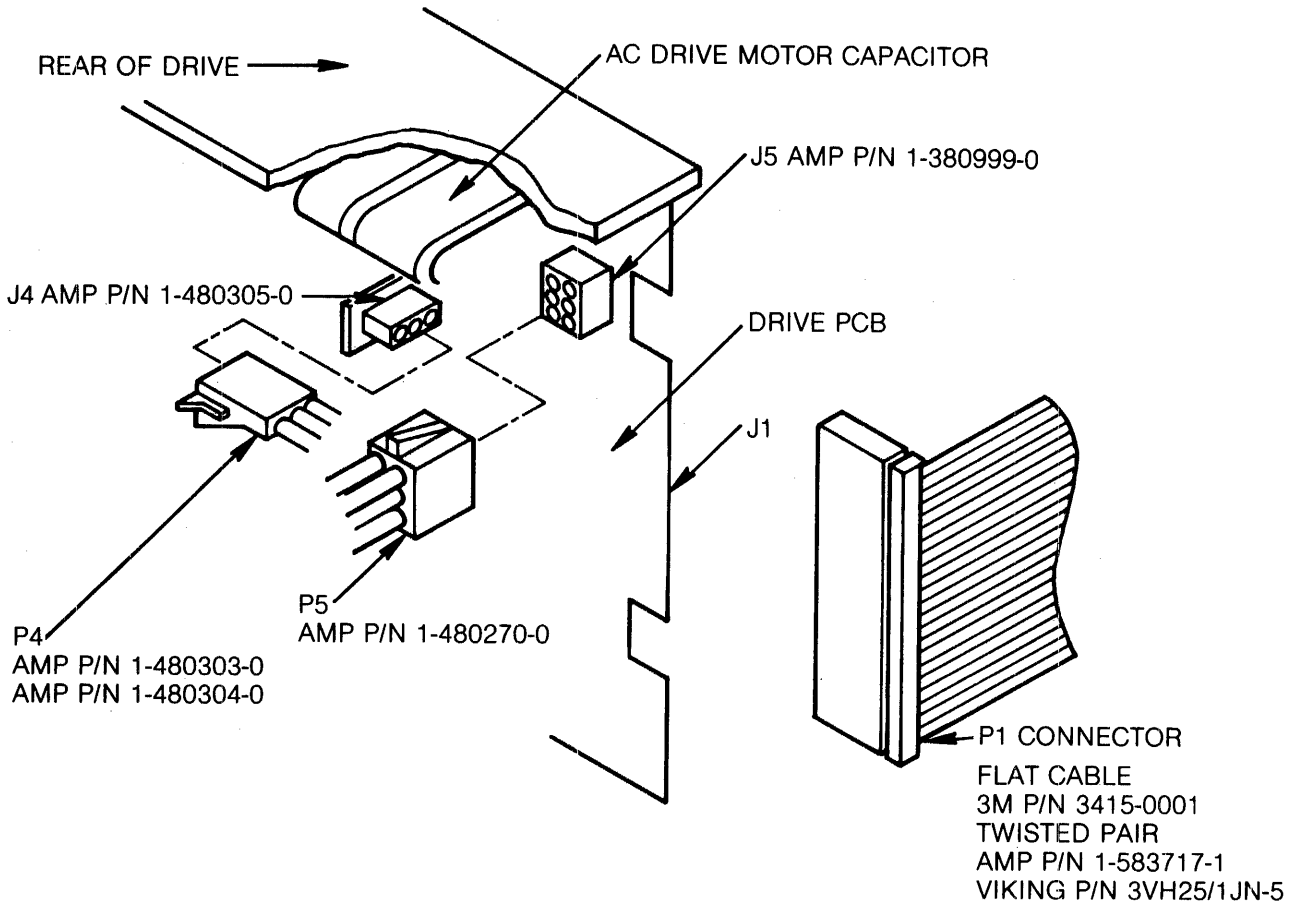


Figure 16. Interface Connectors - Physical Location Diagram

6.0 DRIVE PHYSICAL SPECIFICATIONS

This section describes the mechanical dimensions and mounting recommendations for the SA800/801.

6.1 Drive Dimensions

Reference Figure 18 for dimensions of the SA800/801.

6.2 Mounting Recommendations

The SA800/801 is capable of being mounted in one of the following positions:

1. Vertical-Door opening to the left or right.
2. Horizontal-Door opening up or down.
3. Upright-Door opening towards the front or rear.

6.2.1 Vertical Mounting

The drive, as shipped from the factory, is ready to be mounted in the vertical position, door opening left or right, without any adjustments.

Horizontal Mounting

If the drive is to be mounted horizontally with the door opening down (PCB up), the head load actuator return spring must be repositioned to compensate for gravity. Reference Figure 17 for the proper spring position on the actuator.

If the door is to open up (PCB down), it must be specified when ordering. This feature provides a heavier door opening spring. In addition, the head load actuator return spring will be repositioned to compensate for gravity. Reference Figure 17 for the proper position for the spring on the actuator.

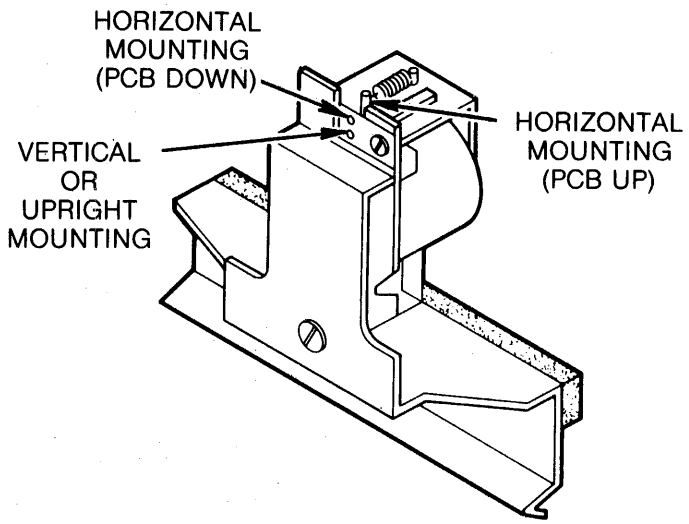


Figure 17. Head Load Actuator Mounting Prerequisites

6.2.3 Upright Mounting

If the Drive is to be mounted in the upright position (IBM 3740 fashion), the spring hook attached to the eject mechanism must be removed and then attach the eject spring to the place the hook was on.

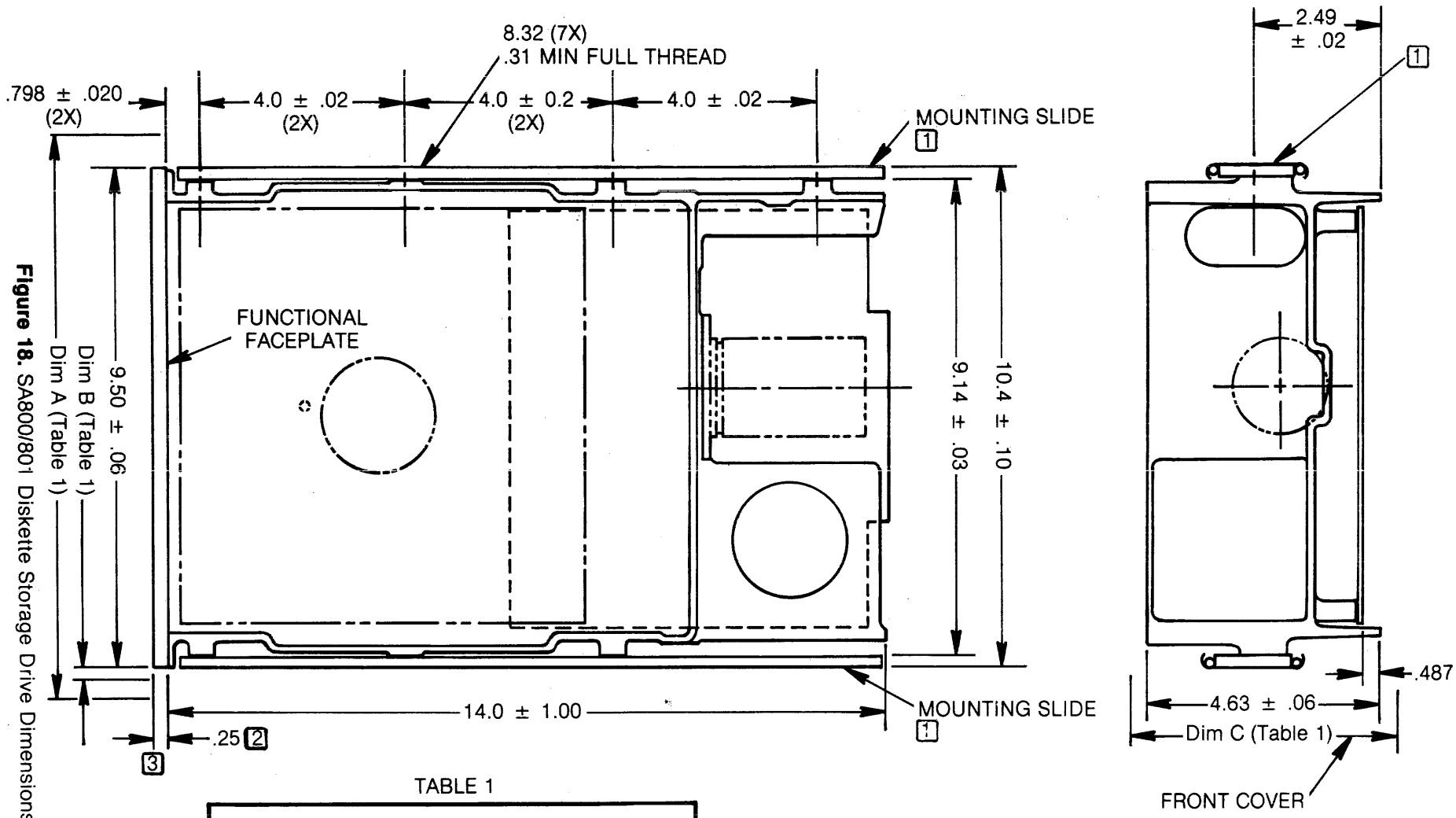


Figure 18. SA800/801 Diskette Storage Drive Dimensions

TABLE 1

Decorative Cover Dimensions			
Cover Size	Dim A	Dim B	Dim C
4-5/8 × 10-1/2	10.50	.240	4.62
5-1/4 × 10	10.00	.240	5.25
5-1/4 × 11	11.00	.740	5.25
Tolerance	± .03	± .030	± .03

[1] If file is mounted on slides, file will extend 14 inches from operating position for servicing.

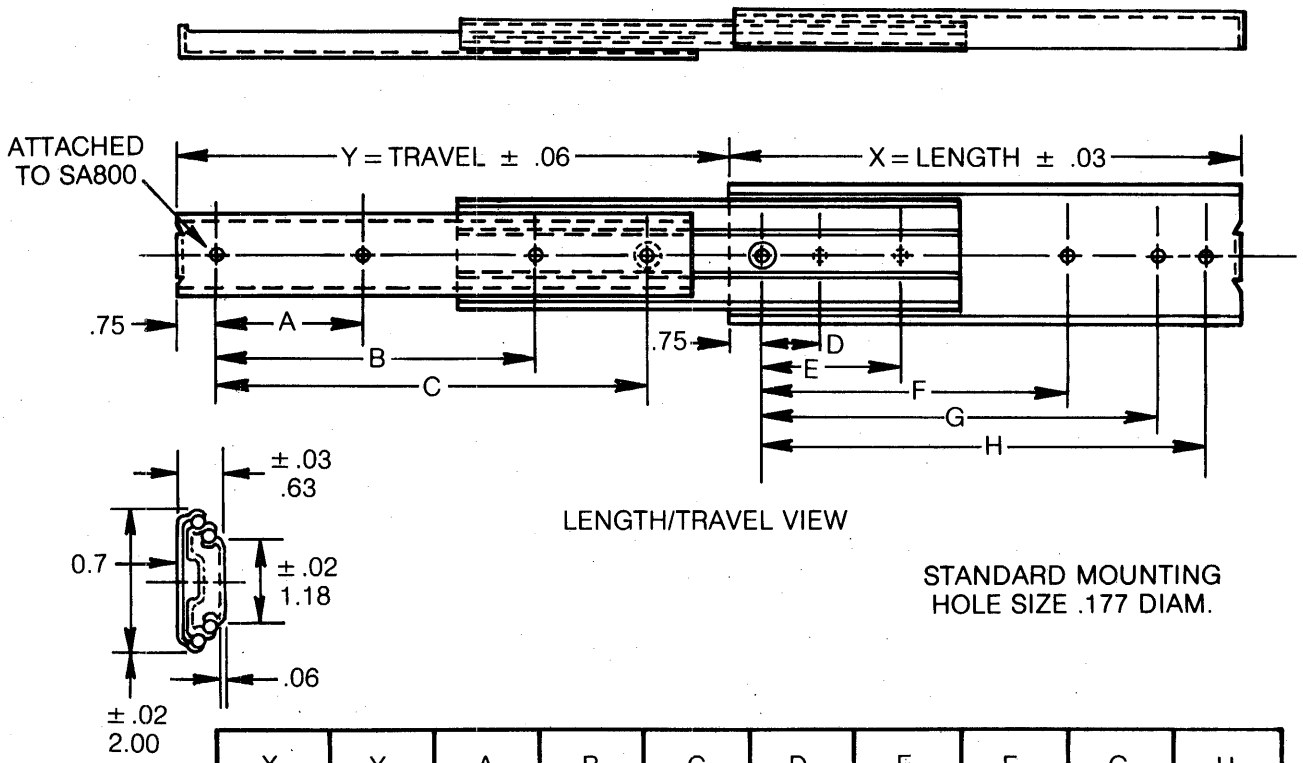
[2] With decorative cover this dimension is .38.

[3] Handle extends .375 beyond faceplate.

[4] All dimensions are in inches.

6.3 Chassis Slide

Available as an optional accessory is a chassis slide kit P/N 50239. This kit contains two slides, one locking and one non-locking, and seven screws. Dimensions of the slide are shown in Figure 19. For use on the standard casting only.



X	Y	A	B	C	D	E	F	G	H
14	15	4.00	8.00	12.00	1.00	3.50	8.50	11.50	12.50

Figure 19. Slide Mounting Dimensions

6.4 Decorative Face Plate

The SA800/801 may be ordered with one of the following decorative face plates:

SIZE	COLOR	PART NO.
4 5/8 × 10 1/2	Tan	50264
4 5/8 × 10 1/2	White	50263
5 1/4 × 10	Tan	50261
5 1/4 × 10	White	50260
5 1/4 × 11	Tan	50258
5 1/4 × 11	White	50257
"R" Series-4 5/8 × 8 11/16	Tan	50675

If another color is required to match the system's color scheme, the face plate may be painted. The following information should be utilized to avoid potential problems in the painting process.

1. The front cover is made from GE's LEXAN. Dimensional stability of LEXAN exists from -60°F +250°F. If the type paint used requires baking, the temperature should not exceed +250°F, including any hot spots which can contact the cover.

2. LEXAN is a polycarbonate. Any paint to be used should be investigated to insure that it does not contain chemicals that are solvents to polycarbonates.

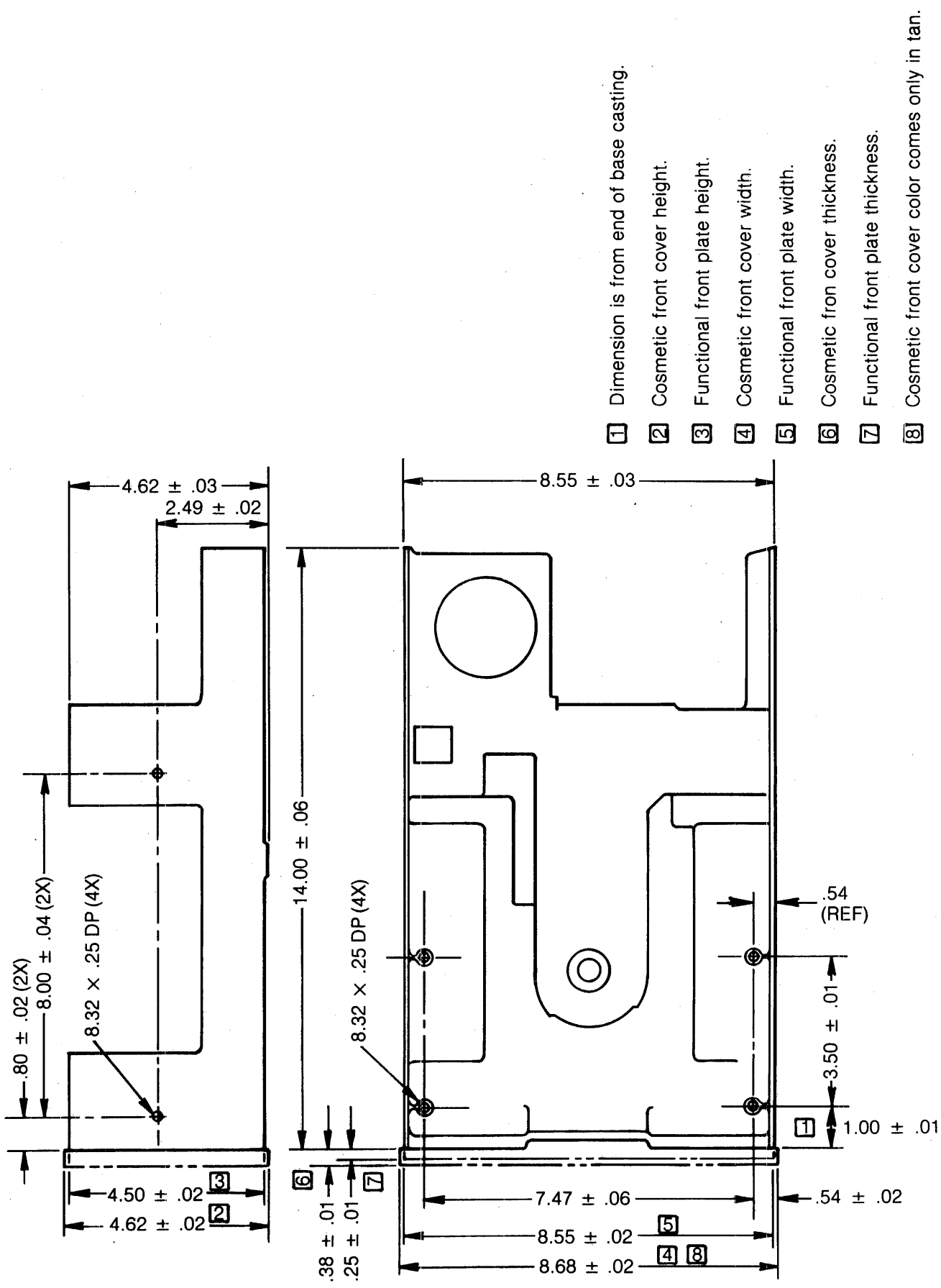


Figure 20. SA800/801R Dimensions

7.0 CUSTOMER INSTALLABLE OPTIONS

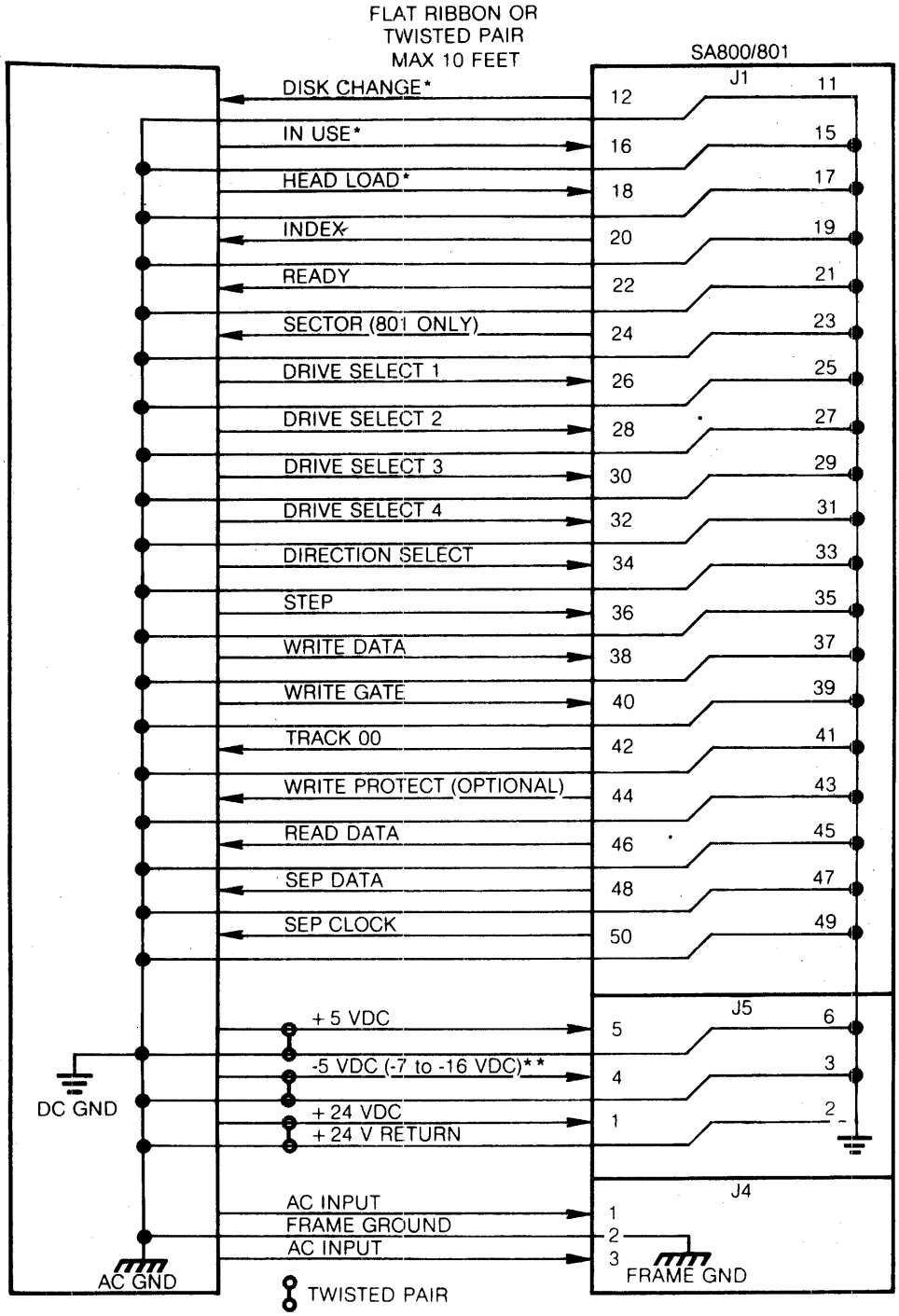
The SA800/801 can be modified by the user to function differently than the standard method as outlined in sections 3 and 4. These modifications can be implemented by adding or deleting traces and by use of the Alternate I/O pins. Some traces are capable of being connected by use of a shorting plug, Shugart P/N 15648 or AMP P/N 530153-2. This section will discuss a few examples of modifications and how to install them. The examples are:

1. Drive Select one to eight drives.
2. Select drive without loading head or enabling stepper.
3. Select drive and enable stepper without loading the head.
4. Load head without selecting drive or enabling stepper.
5. Radial Ready.
6. Radial Index/Sector.
7. Eight, 16, or 32 Sector option.
8. In Use (Activity L.E.D.) optional input.
9. Write Protect options.

Tabulated below are the trace options with the condition of the trace as it is shipped from the factory. Figure 21 shows the location of these traces on the PCB.

CUSTOMER CUT/ADD TRACE OPTIONS

TRACE DESIGNATOR	DESCRIPTION	SHIPPED FROM FACTORY	
		OPEN	SHORT
T3,T4,T5,T6	Terminations for Multiplexed Inputs		Plugged
T1	Terminator for Drive Select		Plugged
T2	Spare Terminator for Radial Head Load	X	
DS1,DS2,DS3,DS4	Drive Select Input Pins	X	DS1 is Plugged
RR	Radial Ready		X
RI	Radial Index and Sector		X
R,I,S	Ready, Index, Sector Alternate Output Pads		X
HL	Stepper Power From Head Load		Plugged
DS	Stepper Power From Drive Select	X	
WP	Inhibit Write When Write Protected		X
NP	Allow Write When Write Protected	X	
8,16,32	8, 16, 32 Sectors (SA801 Only)	8 & 16	32
D	Alternate Input-In Use	X	
2,4,6,8,10,12,14,16,18	Nine Alternate I/O Pins	X	
D1,D2,D4,DDS	Customer Installable Decode Drive Select Option	X	
A,B,X	Radial Head Load		Plugged
C	Alternate Input-Head Load	X	
Z	In Use from Drive Select		Plugged
Y	In Use from HD LD	X	
DC	Alternate Output-Disk Change	X	
NFO	Non Force Out	X	
TS	True FM Data Separation	X	



NOTE: Not shown are 5 of the 9 Alternate I/O connections. The connections for these lines are on pins 2, 4, 6, 8, 10 and 14. Signal return for these lines are on pins 1, 3, 5, 7, 9 and 13 respectively.

*These lines are alternate input/output lines and they are enabled by jumper plugs.

**Not required on LSI PCB's

FIGURE 40. INTERFACE CONNECTIONS

1.9.4 Output Lines

There are seven (7) output lines from the SA800 and eight (8) from the SA801. There also is one (1) optional output line from the SA800/801.

The output signals are driven with an open collector output stage capable of sinking a maximum of 40 ma at a logical zero level or true state with a maximum voltage of 0.4V measured at the driver. When the line driver is in a logical one or false state the driver is off and the collector current is a maximum of 250 microamperes. The receiver should be a Schmidt trigger type device. Refer to Figure 41.

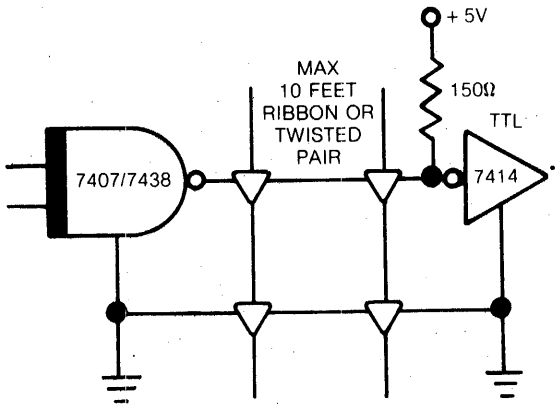


FIGURE 41.

7.1 Drive Select - One to Eight Drives

Customer installed option allows up to eight drives to be multiplexed together. This method of drive selection uses a binary address to select a drive.

To install this feature on a standard drive, the following traces should be added or deleted:

1. Add a 74L85, 4 bit comparator (Motorola P/N MC 14585, National Semiconductor P/N MM 74c85) into position 2B on PCB, (1A on PCB 25136).
2. Connect trace 'DDS'.
3. Insure traces 'DS1' - 'DS4' are plugged.
4. Jumper traces 'D1', 'D2', and 'D4' according to table below for address of each drive.

The four Drive Select lines are to be used for addressing the drives. Pin 26 is used as Drive Select enable and pins 28 (binary 1), 30 (binary 2), and 32 (binary 4), are the address lines. Figure 23 illustrates the circuitry. The table below shows the logical state each line must be at to select each of the drives.

Figure 23 illustrates the circuitry.

ADDRESS	TRACE		
	D1	D2	D4
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

DRIVE	INTERFACE PIN			
	26	28	30	32
0	0	1	1	1
1	0	0	1	1
2	0	1	0	1
3	0	0	0	1
4	0	1	1	0
5	0	0	1	0
6	0	0	1	0
7	0	0	0	0

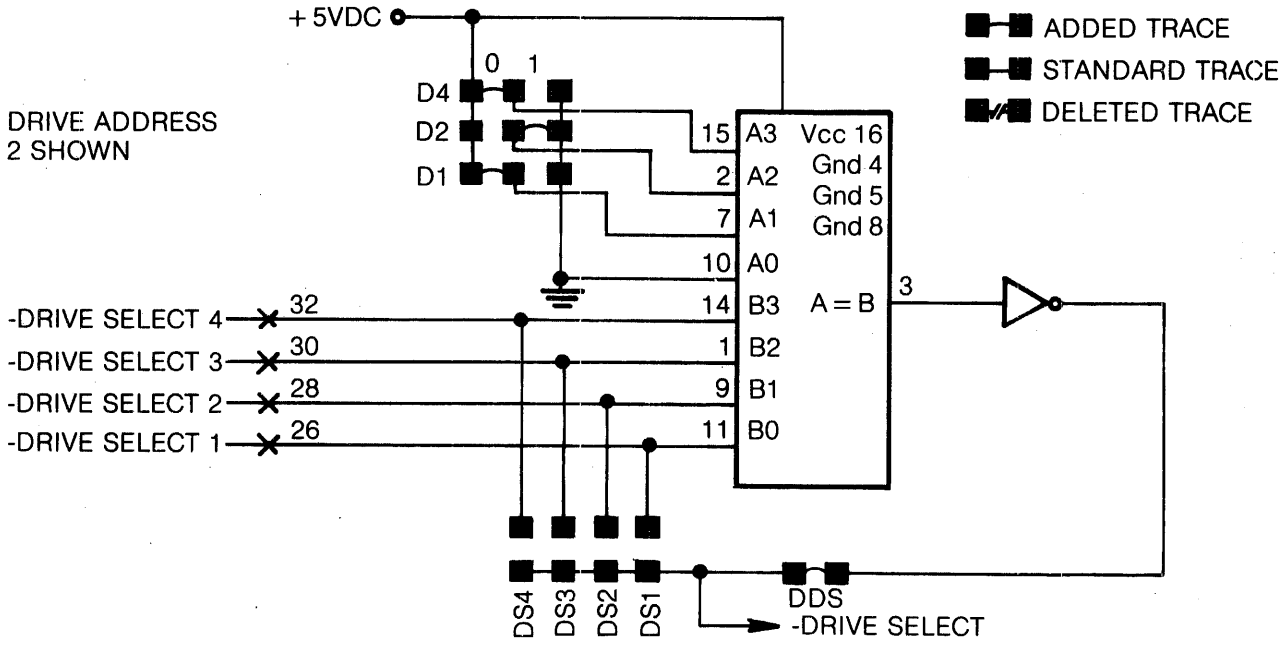


Figure 23. Drive Select Circuitry

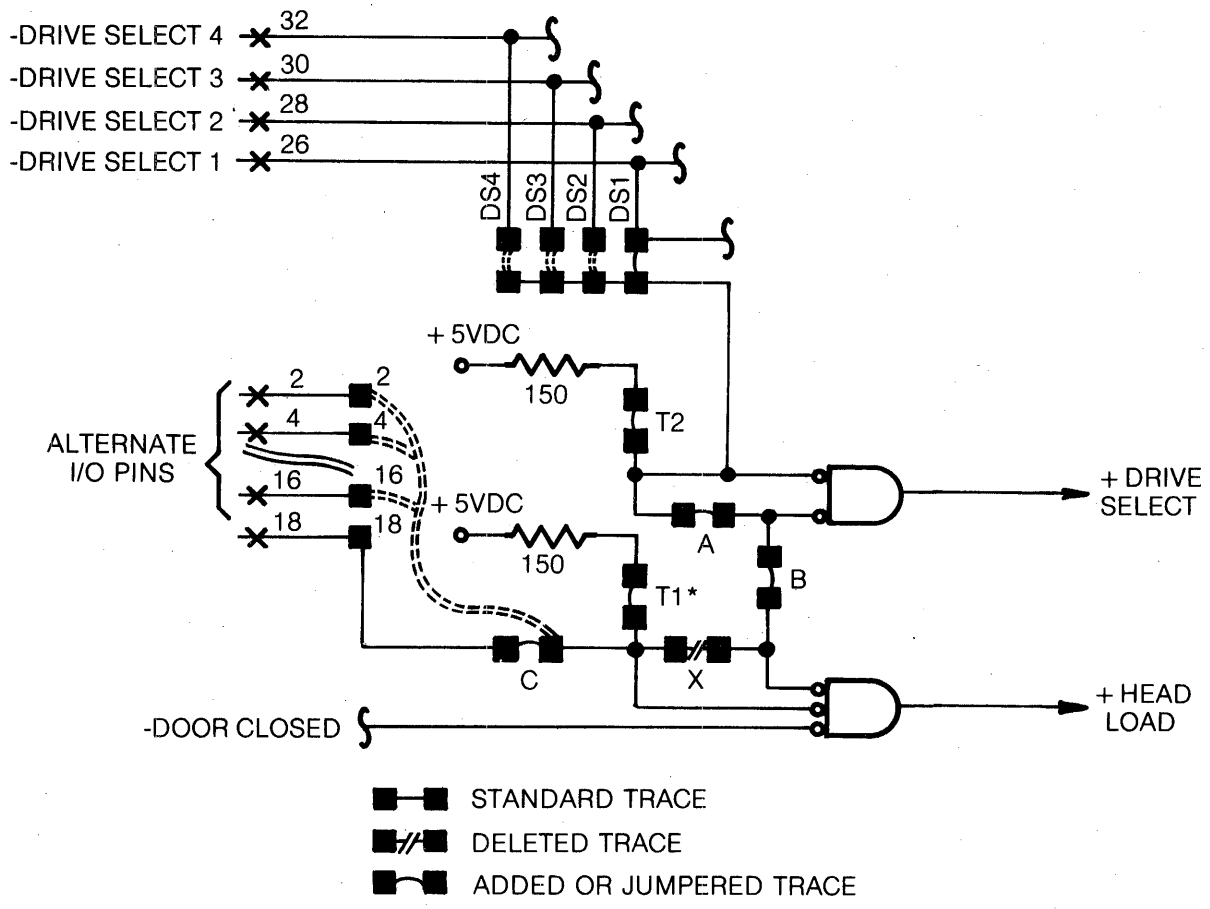
7.2 Select Drive Without Loading Head Or Enabling Stepper Motor

This option would be advantageous to the user who requires a drive to be selected at all times. Normally, when a drive is selected, its head is loaded and the stepper motor is energized. The advantage of this option would be that the output control signals could be monitored (with the exception of Track Zero, which requires the stepper to be energized) while the head was unloaded thereby extending the head and media life. When the system requires the drive to perform a Read, Write, or Seek, the controller would activate the Head Load line (pin 18) which in turn would load the head and energize the stepper motor. After the Head Load line is activated, a 35 ms delay must be introduced before Write Gate and Write Data may be applied or before Read Data is valid.

To install this option on a standard drive, the following traces should be added or deleted:

1. Jumper trace 'T2'.
2. Remove jumper from trace 'X'.
3. Jumper trace 'C'.

Figure 24 illustrates the circuitry.



*NOTE: If the -Head Load line is multiplexed, terminator 'T1' jumper must be removed from each drive except the last one on the line. Also, the current requirement for the +24 VDC supply should be a multiple of the maximum +24 volt current times the number of drives on the line that have Head Load active.

Figure 24. Select Drive Without Loading Head Circuit

7.3 Select Drive and Enable Stepper Without Loading Head

This option is useful to the user who wishes to select a drive and perform a seek operation without the head being loaded or with door open. An example use of this option is that at power on time, an automatic recalibrate (reverse seek to track zero) operation could be performed with the drive access door open. Normally for a seek to be performed, the door must be closed and the head loaded. Other advantages are those listed in section 7.2 in addition to being able to monitor Track Zero. When a Read or Write operation is to be performed, the head must be loaded (pin 18). After the Head Load line is activated, a 35 ms delay must be introduced before Write Gate and Write Data may be applied or before Read Data is valid.

To install this option on a standard drive, the following traces should be added or deleted:

1. Jumper trace 'T2'.
2. Remove jumper from trace 'B'.
3. Remove jumper from trace 'HL'.
4. Jumper trace 'DS'.
5. Jumper trace 'C'.

Figures 24 and 25 illustrate the circuitry.

7.4 Load Head Without Selecting Drive Or Enabling Stepper

This option is useful in disk to disk copy operations. It allows the user to keep the heads loaded on all drives thereby eliminating the 35 ms head load time. The head is kept loaded on each drive via an Alternate I/O pin. Each drive may have its own Head Load line (Radial or Simplexed) or they may share the same line (Multiplexed). When the drive is selected, an 8 ms delay must be introduced before a Read or Write operation can be performed. This is to allow the R/W head to settle after the stepper motor is energized. With this option installed, a drive can only be selected with both Drive Select and Head Load active.

To install this option on standard drive, the following traces should be added or deleted:

1. Jumper trace 'T2'.
2. Remove jumper from trace 'A'.
3. Remove jumper from trace 'HL'.
4. Jumper trace 'DS'.

*5. Jumper trace 'C'.

*If the -Head Load line is multplexed, terminator 'T1' jumper must be removed from each drive except the last one on the line.

Figures 25 and 26 illustrate the circuitry.

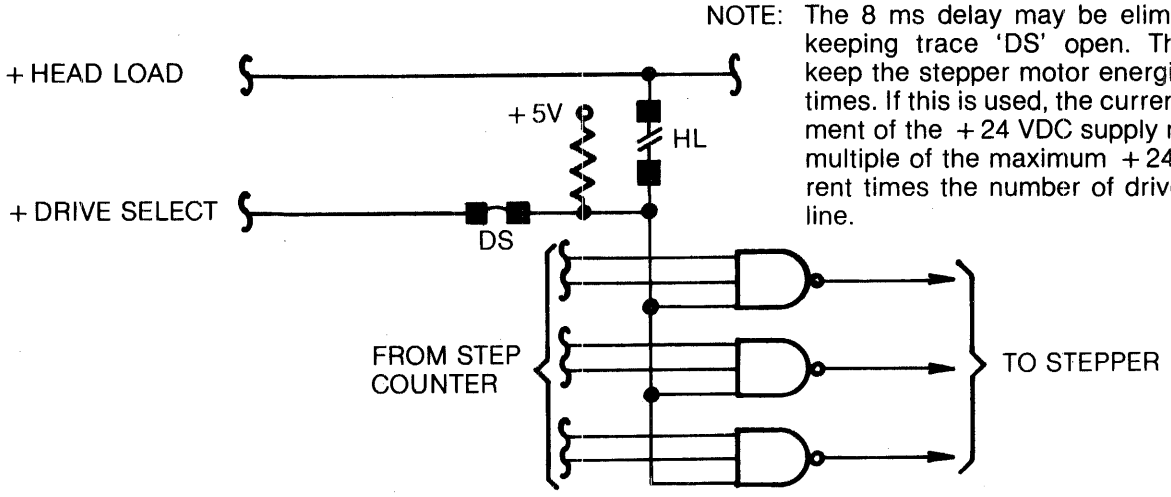


Figure 25. Stepper Motor Enable Circuit

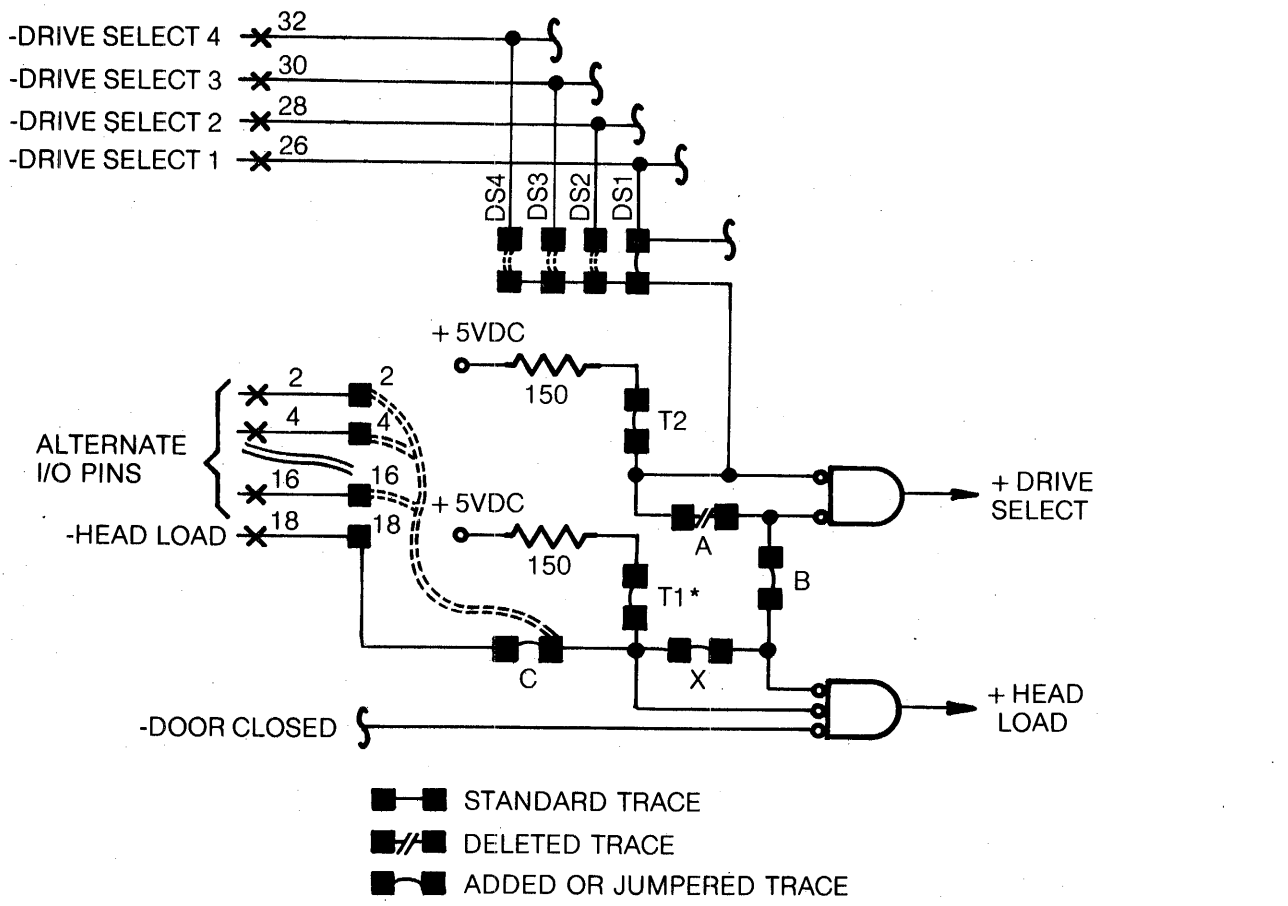


Figure 26. Load Head Without Selecting Drive or Enabling Stepper Circuit

7.5 Radial Ready

This option enables the user to monitor the Ready line of each drive on the interface. This can be useful in detecting when an operator has removed or installed a Diskette in any drive. Normally, the Ready line from a drive is only available to the interface when it is selected.

To install this option on a standard drive, the following traces should be added or deleted:

1. Cut trace 'RR'.
*2. Cut trace 'R'.
*3. Add a wire from pad 'R' to one of the Alternate I/O pins.

*One of the drives on the interface may use pin 22 as its Ready line, therefore, steps 2 and 3 may be eliminated on this drive. All the other drives on the interface must have their own Ready line, therefore steps 2 and 3 must be incorporated.

Figure 27 illustrates the circuitry.

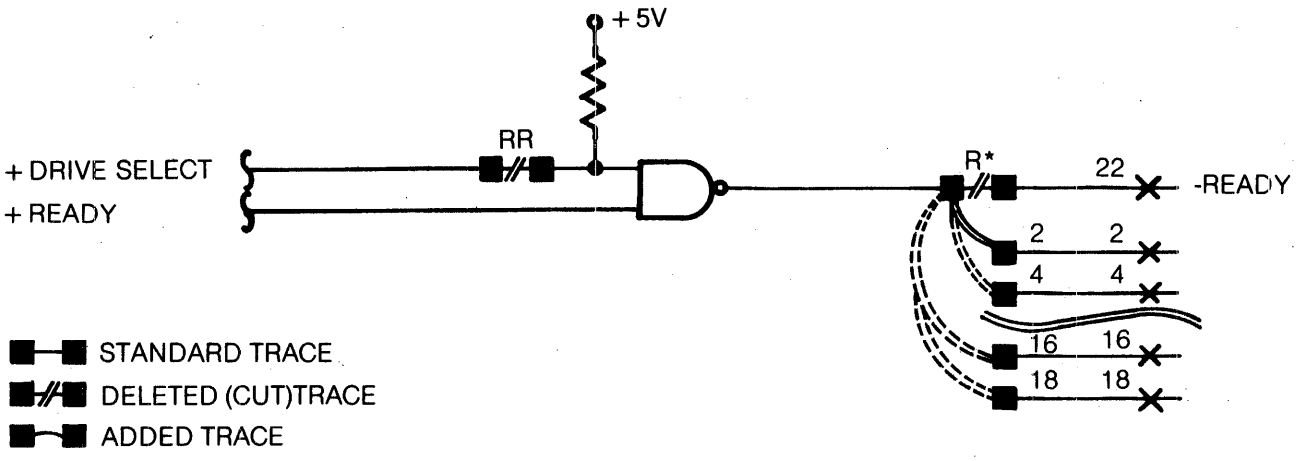


Figure 27. Radial Ready Circuit

7.6 Radial Index/Sector

This option enables the user to monitor the Index and Sector lines at all times so that the drive may be selected just prior to the sector that is to be processed. This option can be used to reduce average latency.

To install this option on a standard drive the following traces should be added or deleted:

1. Cut trace 'RI'.
*2. Cut trace 'I'.
*3. Cut trace 'S'.
*4. Add a wire from trace 'I' to one of the Alternate I/O pins.
*5. Add a wire from trace 'S' to one of the Alternate I/O pins.

*One of the drives on the interface may use pin 20 (-Index) and pin 24 (-Sector) as its Index and Sector lines, therefore, steps 2-5 may be eliminated for this drive. All other drives on the interface must have their own Index and Sector lines, therefore, steps 2-5 must be incorporated.

Figure 28 illustrates the circuitry.

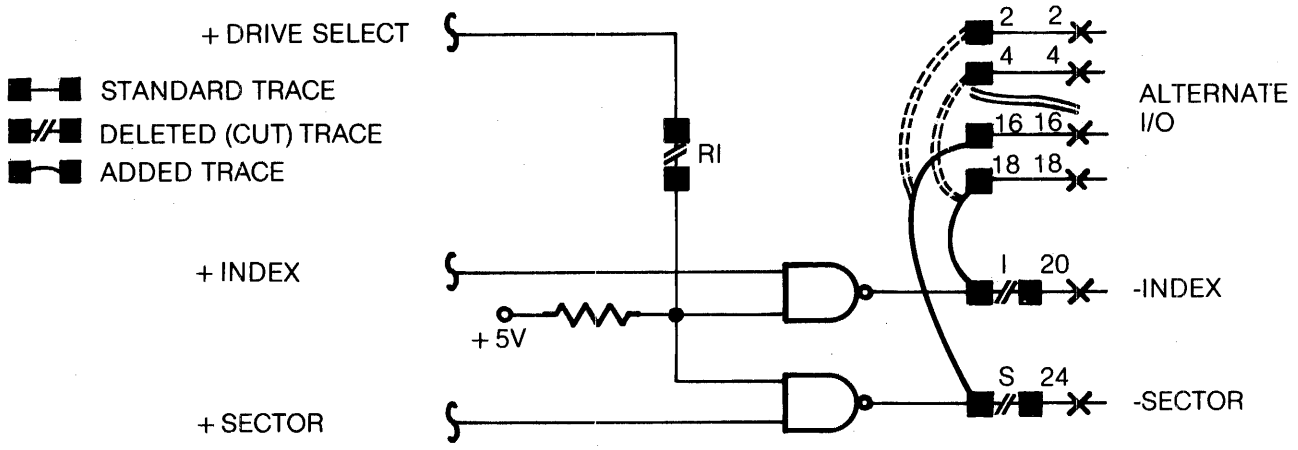


Figure 28. Radial Index/Sector Circuit

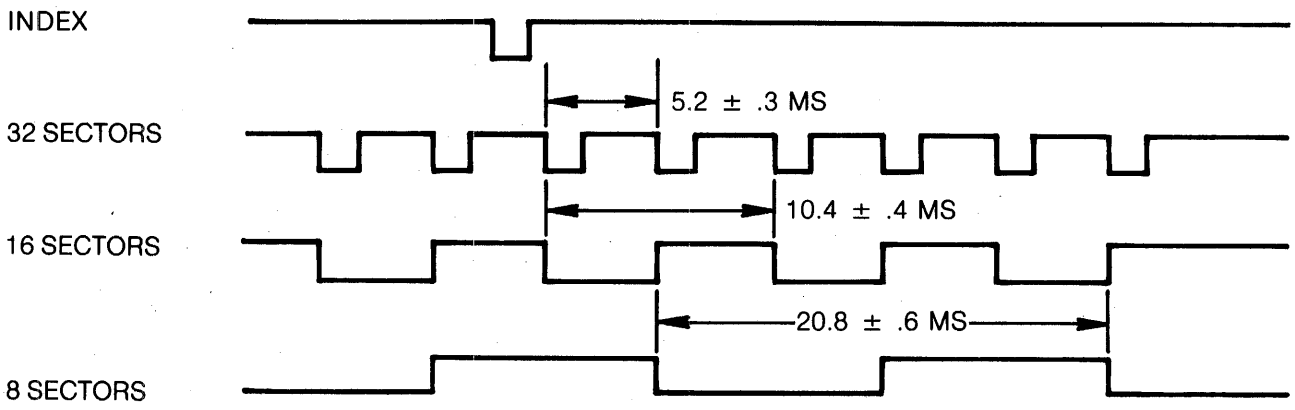
7.7 Eight, 16, Or 32 Sectors

The SA801, as shipped from the factory, is set up to provide 32 Sector pulses per revolution of the Diskette onto the interface. This option is provided for the user who wishes to have eight or 16 Sectors per revolution. The logic divides the Sector pulses by two or four. Reference Figure 29 for the timing relationships.

To install this option on a standard drive (SA801), the following traces should be added or deleted:

1. Cut trace '32'.
2. Connect trace '16' for 16 Sectors or connect trace '8' for eight Sectors.

Figure 30 illustrates the circuitry.



* INDICATES BEGINNING OF SECTOR 1 IN RELATIONSHIP TO INDEX

Figure 29. Sector Timing Relationships

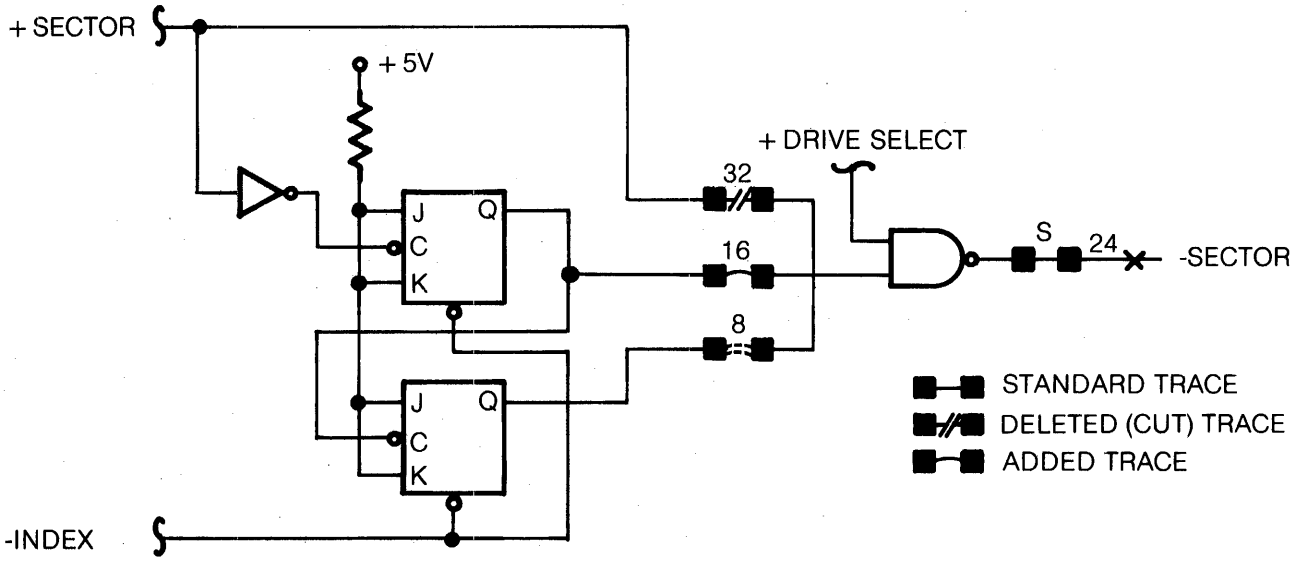


Figure 30. Sector Divide Circuit

7.8 In Use Alternate Input (Activity LED)

This alternate input, when activated to a logical zero level, will turn on the Activity LED mounted in the push bar on the front panel of the drive. It can be used as an indicator to the operator. Examples of some indications are:

1. Write protected Diskette is installed.
2. Drive in which the diskette is to be changed.
3. The operating system drive.
4. Drive with a special configuration.

To install this option on standard drive, jumper trace 'D' and active the interface line pin 16.

This signal is an "OR" function with Drive Select or Head Load. Figure 31 illustrates the circuitry.

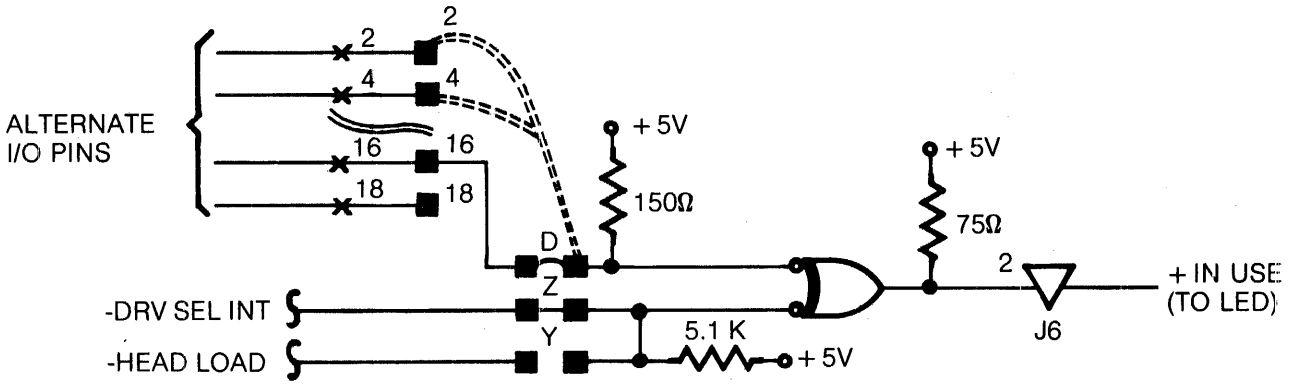


Figure 31. In Use/Activity LED Circuit

7.9 Write Protect Optional Use

As shipped from the factory, the optional Write Protect feature will internally inhibit writing when a Write Protected Diskette is installed. With this option installed, a Write Protected Diskette will not inhibit writing, but it will be reported to the interface. This option may be useful in identifying special use Diskettes.

To install this option on a drive with the Write Protect feature, the following traces should be added or deleted:

1. Cut trace 'WP'.
2. Connect trace 'NP'.

Figure 32 illustrates the circuitry.

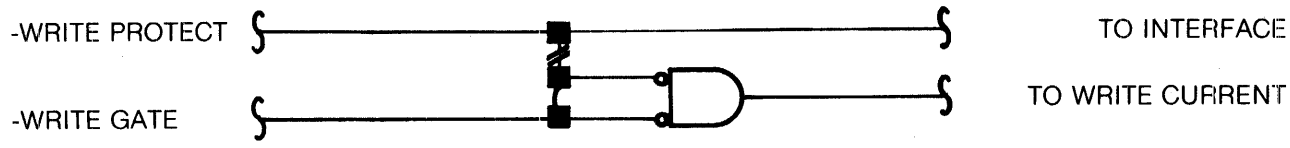


Figure 32. Write Protect Circuit

7.10 Disk Change (Alternate Output)

This customer installable option is enabled by jumpering trace 'DC'. It will provide a true signal (logical zero) onto the interface (pin 12) when Drive Select is activated if while deselected the drive has gone from a Ready to a Not Ready (Door Open) condition. This line is reset on the true to false transition of Drive Select if the drive has gone Ready. Timing of this line is illustrated in Figure 33. The circuitry is illustrated in Figure 34.

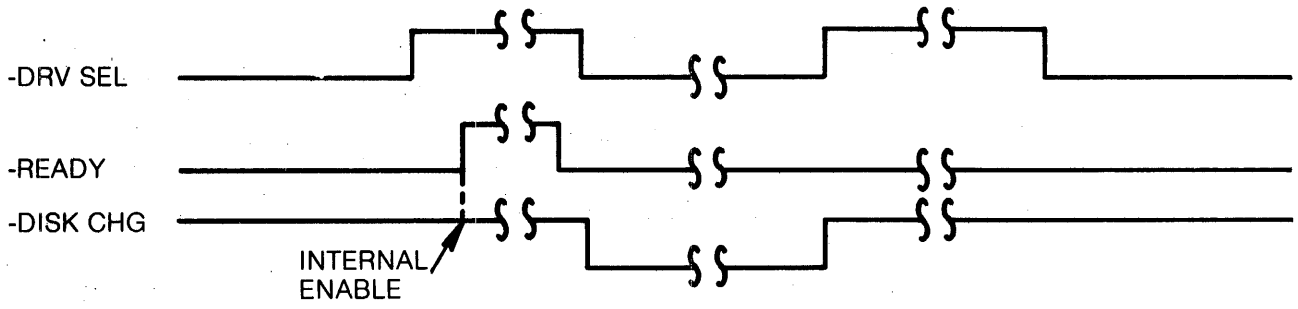


Figure 33. Disk Change Timing

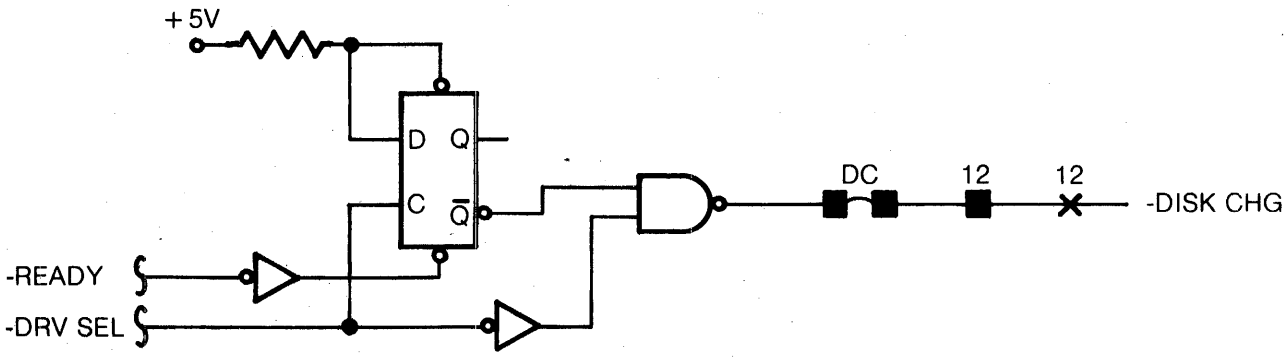


Figure 34. Disk Change Circuit

8.0 OPERATION PROCEDURES

The SA800/801 was designed for ease of operator use to facilitate a wide range of operator oriented applications. The following section is a guide for the handling and error recovery procedures on the diskette and diskette drive.

8.1 Diskette Loading and Handling

The diskette is a flexible disk enclosed in a plastic jacket. The interior of the jacket is lined with a wiping material to clean to disk of foreign material. Figure 35 shows the proper method of loading a diskette in the SA800/801 Diskette Storage Drive. To load the diskette, depress latch, insert the diskette with the label facing out. (See Figure 35). Move the latch handle to the left to lock diskette on drive spindle. The diskette can be loaded or unloaded with all power on and drive spindle rotating.

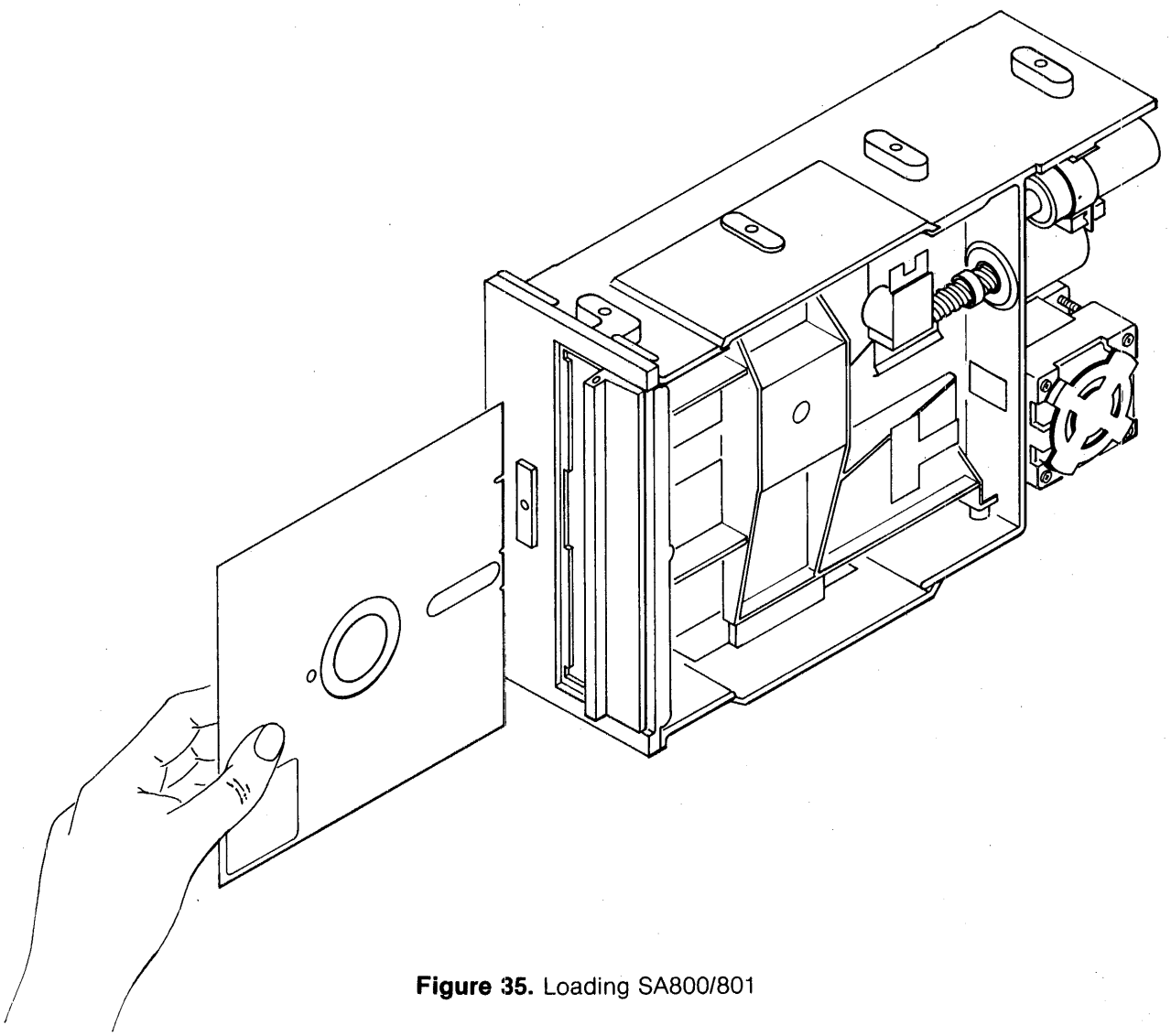


Figure 35. Loading SA800/801

When removed from the drive, the diskette is stored in an envelope. To protect the diskette, the same care and handling procedures specified for computer magnetic tape apply. These precautionary procedures are as follows:

1. Return the diskette to its storage envelope.
2. Keep cartridges away from magnetic fields and from ferromagnetic materials which might become magnetized. Strong magnetic fields can distort recorded data on the disk.
3. Replace storage envelopes when they become worn, cracked or distorted. Envelopes are designed to protect the disk.
4. Do not write on the plastic jacket with a lead pencil or ball-point pen. Use a felt tip pen.
5. Heat and contamination from a carelessly dropped ash can damage the disk.
6. Do not expose diskette to heat or sunlight.
7. Do not touch or attempt to clean the disk surface. Abrasions may cause loss of stored data.

8.2 Write Protecting a Diskette

Shugart Media has the capability of being write protected. The write protect feature is selected by the notch in the media. When the notch is open it is protected; when covered, writing is allowed. The notch is closed by placing a tab over the front of the notch, and the tab folded over covering the rear of the notch. The Diskette can then be write protected by removing the tab. Refer to Figures 36 and 37.

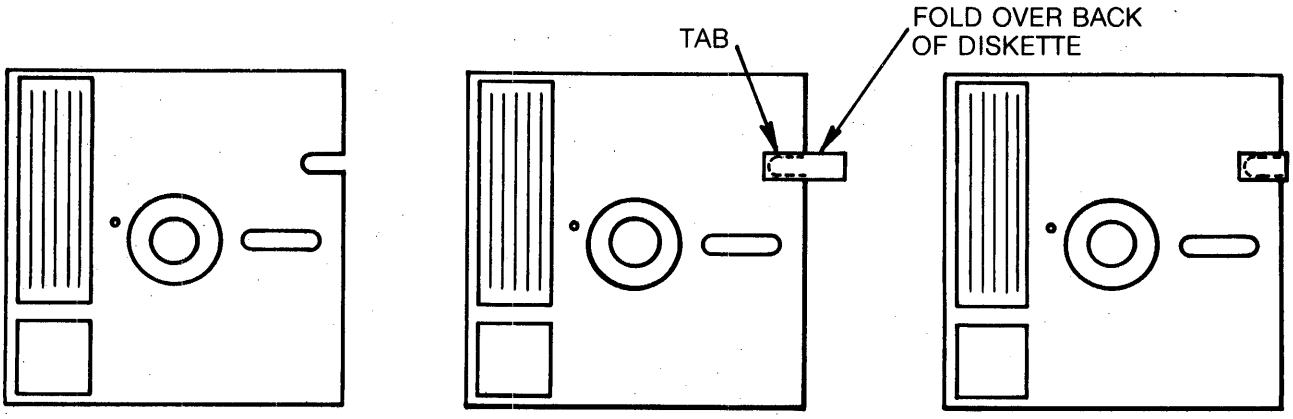


Figure 36. Diskette Write Protected

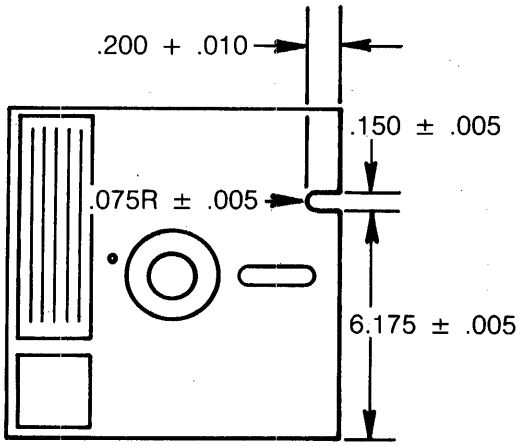


Figure 37. Write Inhibit Notch Specifications

9.0 ERROR DETECTION AND CORRECTION

9.1 Write Error

If an error occurs during a write operation, it will be detected on the next revolution by doing a read operation, commonly called a "write check." To correct the error, another write and write check operation must be done. If the write operation is not successful after ten attempts have been made, a read operation should be attempted on another track to determine if the media or the drive is failing. If the error still persists, the disk should be considered defective and discarded.

9.2 Read Error

Most errors that occur will be "soft" errors; that is, by performing an error recovery procedure the data will be recovered.

Soft errors are usually caused by:

1. Airborne contaminants that pass between the read/write head and the disk. These comtaminants will generally be removed by the cartridge self-cleaning wiper.
2. Random electrical noise which usually lasts for a few μsec.
3. Small defects in the written data and/or track not detected during the write operation which may cause a soft error during a read.

The following procedures are recommended to recover from the above mentioned soft errors:

1. Reread the track ten times or until such time as the data is recovered.
2. If data is not recovered after using step 1, access the head to the adjacent track in the same direction previously moved, then return to the desired track.
3. Repeat step 1.
4. If data is not recovered, the error is not recoverable.

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5/80 50574-4

PRINTED IN U.S.A

SA800/801 Diskette Storage Drive

Maintenance Manual

Shugart Associates®

SA800/801
Diskette Storage Drive

Maintenance Manual

TABLE OF CONTENTS

1.0 MAINTENANCE FEATURES

1.1 Alignment Diskette

The SA120 Alignment Diskette is used for alignment of the SA800/801. The following adjustments can be made using the SA120.

1. R/W Head radial alignment using track 38.
2. R/W Head azimuth alignment using track 76.
3. Index Photo-Detector Adjustment using tracks 01 and 76.
4. Track 00 is recorded with standard IBM 3740 format.
5. TK 75 has 1f + 2f signal for load pad adjustment.

Caution should be exercised in using the SA120 Alignment Diskette. Tracks 00, 01, 36, 37, 38, 39, 40, 75, and 76 should not be written on. To do so will destroy pre-recorded tracks.

1.2 SA809 Exerciser

The SA809 Exerciser is built on a PCB whose dimensions are 8" x 8". The Exerciser PCB can be used in a stand alone mode or it can be built into a test station or used in a tester for field service.

The Exerciser is designed to enable the user to make all adjustments and check outs required on the SA800/801 drives, when used with the SA120 alignment diskette.

The exerciser has no intelligent data handling capabilities but can write both 1f and 2f frequencies. The exerciser can enable read in the drive to allow checking of read back signals.

Refer to Section 6 for illustration.

1.3 Special Tools

The following special tools are available for performing maintenance on the SA800/801.

Description	Part Number
Alignment Diskette	SA120-1
Cartridge Guide Adj. Tool	50377-1
Head Penetration Gauge	50380-0
Load Bail Gauge	50391-0
Exerciser	50619-0
Spanner Wrench	50752-0

2.0 DIAGNOSTIC TECHNIQUES

2.1 Introduction

Incorrect operating procedures, faulty programming, damaged diskettes, and "soft errors" created by airborne contaminants, random electrical noise, and other external causes can produce errors falsely attributed to drive failure or misadjustment.

Unless visual inspection of the drive discloses an obvious misalignment or broken part, attempt to repeat the fault with the original diskette, then attempt to duplicate fault on second diskette.

2.2 "Soft Error" Detection and Correction

Soft errors are usually caused by:

1. Airborne contaminants that pass between the read/write head and the disk. Usually these contaminants can be removed by the cartridge self-cleaning wiper.
2. Random electrical noise that usually lasts for a few μ sec.
3. Small defects in the written data and/or track not detected during the write operation that may cause a soft error during a read.
4. Worn or defective load pad.

The following procedures are recommended to recover from the above mentioned soft errors:

1. Reread the track ten (10) times or until such time as the data is recovered.
2. If data is not recovered after using step 1, access the head to the adjacent track in the same direction previously moved, then return to the desired track.
3. Repeat step 1.
4. If data is not recovered, the error is not recoverable.

2.3 Write Error

If an error occurs during a write operation, it will be detected on the next revolution by doing a read operation, commonly called a "write check." To correct the error, another write and write check operation must be done. If the write operation is not successful after ten (10) attempts have been made, a read operation should be attempted on another track to determine if the media or the drive is failing. If the error still persists the diskette

should be replaced and the above procedure repeated. If the failure still exists, consider the drive defective. If the failure disappears, consider the original diskette defective and discard it.

2.4 Read Error

Most errors that occur will be "soft" errors. In these cases, performing an error recovery procedure will recover the data.

2.5 Seek Error

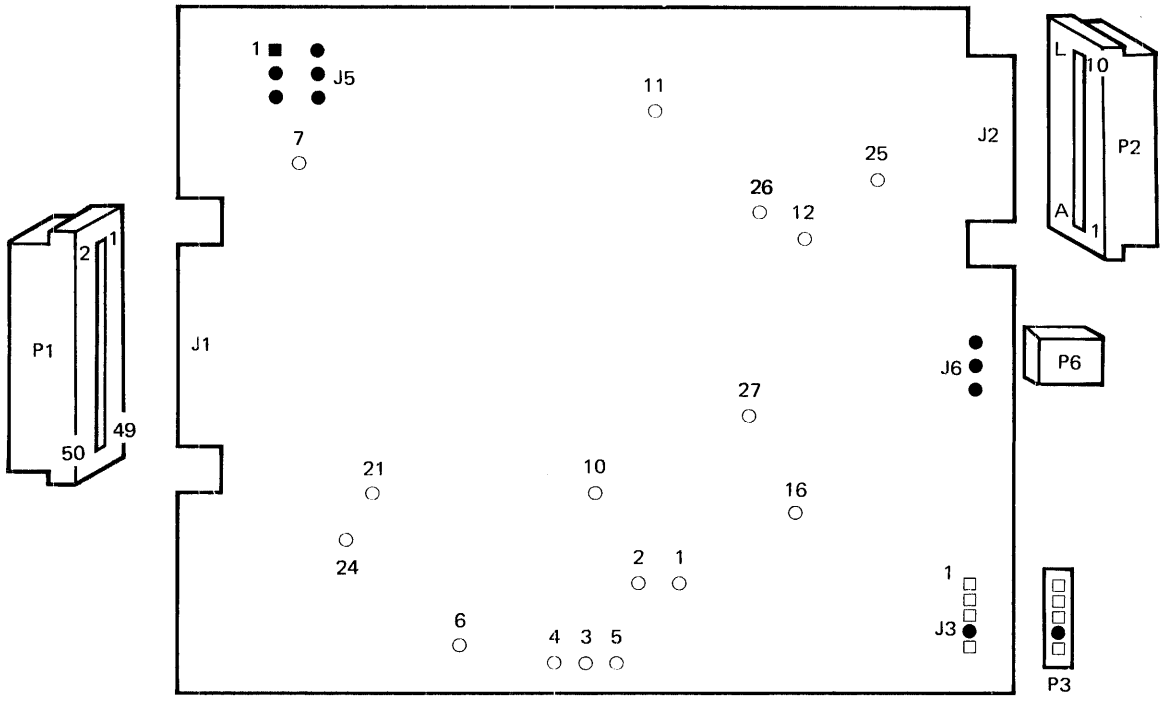
1. Stepper malfunction.
2. Improper carriage torque.

To recover from a seek error recalibrate to track 00 and perform another seek to the original track.

2.6 Test Points–800/801

TP	1	Read Data Signal
	2	Read Data Signal
	3	Read Data (Differentiated)
	4	Read Data (Differentiated)
	5	Signal Ground
	6	Signal Ground
	7	Signal Ground
	10	– Index
	11	+ Head Load
	12	– Index and 801 Sector Pulses
	16	+ Read Data
	21	– Data Separator Time + 1
	24	– Data Separator Time + 2
	25	+ Write Protect
	26	+ Detect Track 00.
	27	+ Gated Step Pulses

2.7 Test Point Locations



3.0 PREVENTIVE MAINTENANCE

3.1 Introduction

The prime objective of any preventive maintenance activity is to provide maximum machine availability to the user. Every preventive maintenance operation should assist in realizing this objective. Unless a preventive maintenance operation cuts machine downtime, it is unnecessary.

Visual inspection is the first step in every scheduled maintenance operation. Always look for corrosion, dirt, wear, binds, and loose connections. Noticing these items during PM may save downtime later.

Remember, do not do more than recommended preventive maintenance on equipment that is operating satisfactorily.

3.2 Preventive Maintenance Procedures

Details of preventive maintenance operations are listed in Figure 1. During normal preventive maintenance, perform only those operations listed on the chart for that preventive maintenance period. Details on adjustments and service checks can be found in the maintenance manual. Observe all safety procedures.

3.3 Cleanliness

Cleanliness cannot be overemphasized in maintaining the SA800/801. Do not lubricate the SA800/801; oil will allow dust and dirt to accumulate. The read/write head should be cleaned only when signs of oxide build up are present.

UNIT	FREQ MONTHS	CLEAN	OBSERVE
Read/Write Head	12	Clean Read/Write Head ONLY IF NECESSARY	Oxide build up
R/W Head Load Button	12*	Replace	
Stepper Motor and Lead Screw	12 12	Clean off all oil, dust, and dirt	Inspect for nicks and burrs
Belt	12		Frayed or weakened areas
Base	12	Clean base	Inspect for loose screws, connectors, and switches
Read/Write Head	12		Check for proper alignment

*Assumes normal usage

Figure 1 PM Procedures

4.0 REMOVALS, ADJUSTMENTS

For parts location, see Section 5.

4.1 Motor Drive

4.1.1 Drive Motor Assembly: Removal and Installation

a. Extract 3 contacts to disconnect motor from AC connector.

b. Loosen two screws holding capacitor clamp to the base. Remove rubber boot and disconnect motor leads from capactior.

c. Remove connectors from PCB and remove PCB.

d. Remove belt from drive pulley.

e. Remove 4 screws holding the motor to the base casting and remove motor.

f. Reverse the procedure for installation.

Note: Insure ground lead is installed between capacitor clamp and base.

4.1.2 Motor Drive Pulley

a. Loosen set screw and remove pulley.

b. Reverse procedure for installation.

Note: When installing a new pulley, the drive pulley must be aligned with the spindle pulley so that the belt tracks correctly.

4.2 Side Cover: Removal

a. Retract screw from upper casting wall sufficiently to allow the side cover to be rocked out.

b. Lift cover off screw in lower casting wall.

4.3 Cartridge Guide Access

a. Remove side cover (Section 4.2).

b. Position head to approximate center of head load bail (to prevent load arm damage).

c. Loosen 2 screws holding cartridge guide to door latch plate.

d. Swing cartridge guide out.

e. When the guide is swung in, it must be adjusted as per Section 4.9.2.

4.4 Sector/Index LED Assembly: Removal and Installation

a. Remove side cover (Section 4.2).

b. Disconnect the wires to the LED terminals (solder joints).

c. Remove the screw holding the LED assembly to the cartridge guide.

d. Reverse the procedure for installation.

e. Check index timing and readjust if necessary.

4.5 Write Protect Detector: Removal and Installation

a. Remove connectors from PCB and remove PCB.

b. Extract wires from P2 connector, pins L3, L4, R5 (E), and R8 (S).

c. Remove cable clamps.

d. Remove side cover (Section 4.2).

e. Remove screw holding the detector bracket and remove assembly.

f. Reverse procedure for reinstalling. Connect the wires to P2 by the following: Red to '3' (L3), Grey to '4' (L4), Black to 'E' (R5) and White to 'J' (R8).

4.5.1 Write Protect Detector Adjustment

a. Insert SA101 diskette into drive. Write protect hole must be open.

b. Set oscilloscope to AUTO sweep, 2V/div. and monitor TP25.

c. Loosen screw on detector assembly and adjust until maximum amplitude is achieved. Tighten screw.

4.6 Head Load Actuator

4.6.1 Head Load Actuator: Removal and Installation

a. Remove side cover (Section 4.2).

b. Disconnect the wires to the actuator terminals (solder joints).

c. Swing out the cartridge to guide assembly (Section 4.3).

d. Remove screw holding the actuator to the cartridge guide.

CAUTION: Restrain the head load arm to prevent its impact with the head.

e. Reverse the procedure for installation.

4.6.2 Head Load Actuator Adjustment

a. Remove side cover.

b. Energize Head Load Coil.

c. Place Head Load Actuator adjustment tool, P/N 50391, on platen.

d. Adjust down stop so that the top of Head Load Bail is flush with top of tool within ± .005" at track 76. Reference Figure 3.

e. Step carriage to track 38.

f. De-energize Head Load Coil.

g. Place adjustment tool onto R/W Head and place load button in cup of tool.

h. Adjust up stop on actuator so that bail just touches Head Load Arm or has .005" clearance or lifts Load Arm .005". Reference Figure 2.

i. Energize Head Load Coil and step carriage between track 00 and 76. Insure that there is a clearance of a minimum of .010" between Head Load Bail and Head Load Arm.

j. Replace side cover.

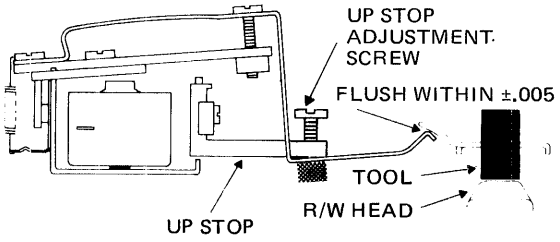


FIGURE 2 HEAD LOAD ACTUATOR UPSTOP ADJUSTMENT

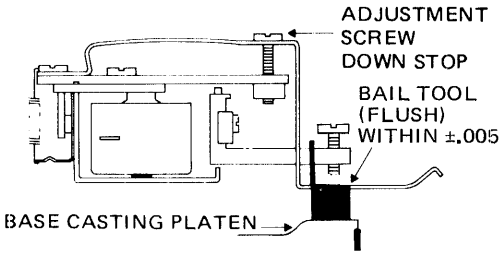


FIGURE 3 HEAD LOAD ACTUATOR DOWN STOP ADJUSTMENT

4.6.3 Head Load Actuator Timing

a. Insert Alignment Diskette (SA120).

b. Step carriage to track 00.

c. Sync oscilloscope on TP11 (+ Head Load). Set time base to 10MSEC/division.

d. Connect one probe to TP1 and the other to TP2. Ground probes to the PCB. Set the inputs to add and invert one input

e. Energize the Head Load solonoid and observe the read signal on the oscilloscope. The signal must be at 50% of full amplitude by 35Msec. Reference Figure 4.

f. If this is not met, continue on with the procedure.

g. Check adjustments outlined in paragraph 4.6.2.

h. If item 'g' is ok, adjust down stop screw (Figure 6) clockwise until timing is met.

Note: Not to exceed ¼ turn.

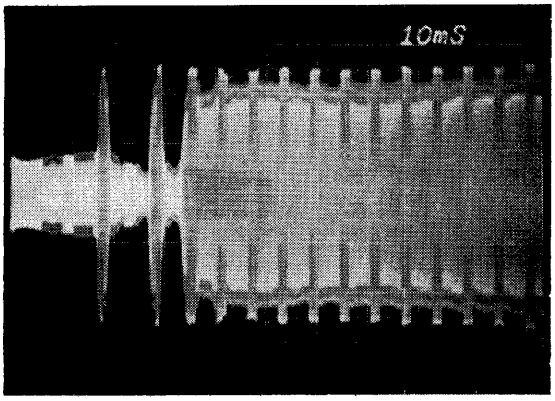


FIGURE 4 HEAD LOAD ACTUATOR TIMING

4.7 Index/Sector Photo Transistor Assembly

4.7.1 Index/Sector Photo Transistor Assembly: Removal and Installation

a. Disconnect P2 connector from PCB.

b. Remove wires from Door Closed switch and extract wires from P2 connector pin 9 (L9) Black, H (R7) Brown, 6 (L6) Red and B (R2) Orange.

c. Remove cable clamp holding wires from detector.

d. Remove screw holding detector to the base plate and remove assembly.

e. To install reverse procedure.

4.7.2 Index/Sector Photo Transistor Potentiometer Adjustment

a. Insert Alignment Diskette (SA120).

b. Using oscilloscope monitor TP-12 (– Index), sync internal negative, DC coupled, set vertical scale to 2 V/cm.

c. Adjust the potentiometer on the Sector/Index Phototransistor to obtain a pulse of 1.7 msec. ± .5 msec. duration.

d. Continue adjustment in Section 4.7.3.

4.7.3 Index/Sector Adjustment

a. Insert Alignment Diskette (SA120).

b. Step carriage to track 01.

c. Sync oscilloscope, external negative, on TP 12 (– Index). Set time base to 50 μsec/division.

d. Connect one probe to TP 1 and the other to TP 2. Ground probes to the PCB. Set the inputs to AC, Add and invert one channel. Set vertical deflection to 500 MV/division.

e. Observe the timing between the start of the sweep and the first data pulse. This should be 200 ± 100 μsec. If the timing is not within tolerence, continue on with the adjustment. Reference Figure 5.

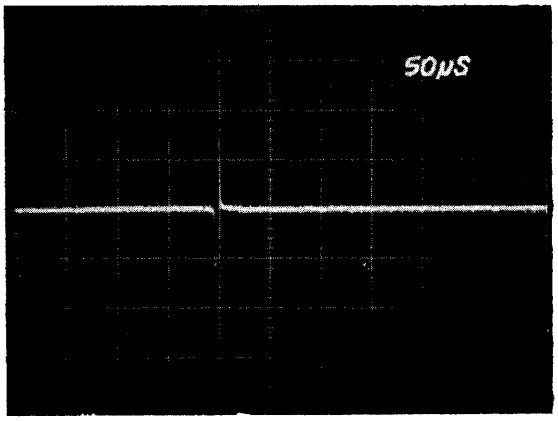


FIGURE 5 INDEX TIMING

f. Loosen the holding screw in the Index Transducer until the transducer is just able to be moved.

g. Observing the timing, adjust the transducer until the timing is 200 ± 100 μsec. Insure that the transducer assembly is against the registration surface on the base casting.

h. Tighten the holding screw.

i. Recheck the timing.

j. Seek to track 76 and reverify that the timing is 200 ± 100 μsec.

4.8 Spindle Assembly

a. Remove side cover (Section 4.2).

b. Swing out cartridge guide (Section 4.3).

c. Remove the nut and washer or 2 spring washers holding the spindle pulley. On late level drives, Spanner Wrench 50752 may be used to hold spindle.

CAUTION: The pre-loaded rear bearing may fly out when spindle pulley is removed.

d. Withdraw spindle hub from opposite side of baseplate.

e. Reverse the procedure for installation.

f. Tighten nut to 20 in./lbs. If spring washers are used, insure they are compressed. Add a drop of LOCTITE® #290 to threads.

4.8.1 Clamp Hub Removal

a. Remove hub clamp plate. Reference Figure 6.

b. Remove clamp hub and spring.

c. To install, reverse the procedure. No adjustment necessary.

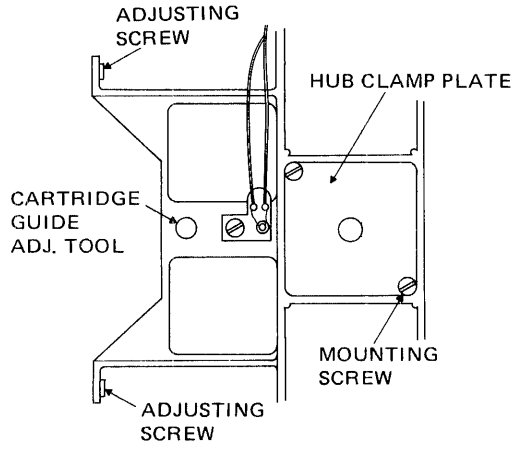


FIGURE 6 CARTRIDGE GUIDE ADJUSTMENT

4.9.1 Cartridge Guide Removal

a. Perform steps 4.3 through 4.6.1.

b. Remove C-clip form pivot shaft. Reference Figure7.

c. Remove pivot shaft.

d. Tilt the cartridge guide slightly, and remove it from the upper pivot.

e. To install the cartridge guide, reverse the procedure.

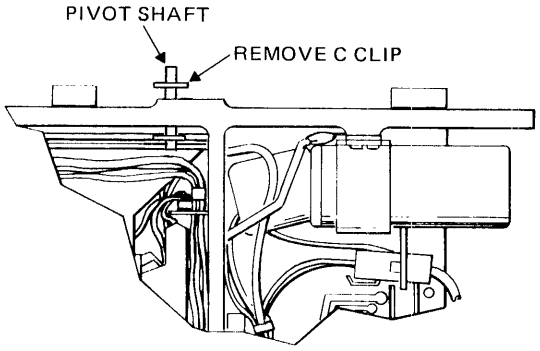


FIGURE 7 CARTRIDGE GUIDE REMOVAL

4.9.2 Cartridge Guide Adjustment

a. Insert the shoulder screw (tool P/N 50377-1) through the adjustment hole in the cartridge guide and screw completely into the base casting (hand tight). Reference Figure 6.

b. Move the handle into the latched position and hold it lightly against the latch.

c. Tighten two screws holding the cartridge guide to the latch plate.

d. Remove the tool and check to determine the flange on the clamp hub clears the cartridge guide when the spindle is rotating. If the clamp hub rubs on the cartridge guide, repeat the adjustment procedure.

e. Check index alignment per Section 4.7.3.

f. Insert diskette, close and open door, then check for proper operation.

4.10 Front Plate Assembly: Removal

a. Remove side cover (Section 3.4.2).

b. Swing out the cartridge guide assembly (Section 4.3).

c. Remove 4 screws holding the front plate assembly to the base casting.

d. To install, reverse the procedure.

e. Check Index adjustment Section 4.7.3.

4.11 Head Amplitude Check

These checks are only valid when writing and reading back as described below. If this amplitude is below the minimum specified, the load pad should be replaced and the head should be cleaned if necessary before re-writing and re-checking. Insure the diskette used for this check is not "worn" or otherwise shows evidence of damage on either the load pad or head side.

a. Install good media.

b. Select the drive and step to TK 76.

c. Sync the oscilloscope on TP-12 (– Index) connect one probe on TP-2 and one on TP-1, on the drive PCB. Ground the probes to the PCB add and invert one input. Set volts per division to 50mv and time base to 20 M sec. per division.

d. Write the entire track with 2F signal (all one's).

e. The average minimum read back amplitude, peak to peak, should be 110 millivolts.

If the output is below minimum and a new load pad and different media is tried and the output is still low, it will be necessary to install a new head and carriage assembly.

4.11.1 Stepper/Carriage Assembly; Removal and Installation

a. Remove cable clamp holding R/W head cable on PCB side of drive.

b. Remove side cover (Section 4.2).

c. Extract stepper cable contacts from P2 connector. Black 10 (L10), Red 2 (L2), Brown 5 (L5), and Orange 8 (8).

Note: This step is only necessary if the stepper motor is to be replaced.

d. Loosen (2) screws and swing clamp down to allow withdrawl of motor.

CAUTION: DO NOT LOOSEN THREE SCREWS COATED WITH GLYPTOL.

e. Remove the grommet on the cable that is inserted into a slot on the Track 00 Detector bracket.

f. Turn stepper shaft until the carriage runs off the end of the lead screw.

g. To install stepper/carriage assembly, reverse procedure. Note steps "h" and "i".

h. If installing a new carriage, set the pre-load nut in the #2 notch. Reference Figure 8.

i. When threading lead screw into carriage assembly, press the pre-load nut slightly against spring in order to start thread. After threading, insure there is a gap between pre-load nut and rear of carriage.

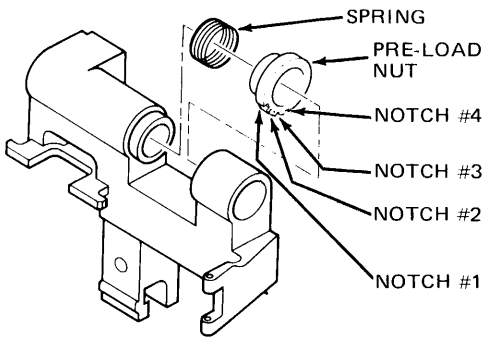


FIGURE 8 CARRIAGE ASSEMBLY

4.11.2 Carriage Assembly Readjustment After Replacement

a. Loosen Track 00 stop collar and manually move the carriage towards the stepper by rotating the lead screw until the carriage load arm tab is near the edge of the load bail. Tighten the collar set screw.

b. Position the Track 00 flag approximately in the center of its slot and tighten the screw. Move the carriage towards the spindle by rotating the lead screw until the flag is clear of the detector.

c. Insert the SA120 alignment diskette and load the head. Set the scope as explained in Section 4.11.3 steps c and d.

d. Step the carriage towards track 00 until the track 00 signal is detected on the interface pin 42.

e. Loosen the 2 stepper motor mounting screws slightly and slowly rotate the stepper motor case until a read data signal off of track 00 appears. Continue rotation until maximum amplitude is obtained. This is only a rough adjustment.

CAUTION: DO NOT LOOSEN THREE SCREWS COATED WITH GLYPTOL.

f. Step the carriage to TK 38 and proceed with head radial adjustments. Refer to Section 4.11.3.

g. Adjust Track 00 stop (Section 4.11.7).

h. Adjust Track 00 flag (Section 4.11.8).

i. Adjust index (Section 4.7.3).

j. Adjust Azimuth (Section 4.11.9).

4.11.3 Head Radial Alignment

Note: Head radial alignment should be checked prior to adjusting index/sector, Track 00 flag or carriage stop.

a. Load alignment diskette (SA120).

Note: Alignment diskette should be at room conditions for at least twenty minutes before alignment.)

b. Step the carriage to track 38.

c. Sync the oscilloscope, external negative, on TP 12 (- CE Index). Set the time base to 20 Msec per division. This will display over one revolution.

d. Connect one probe to TP 1 and the other to TP 2. Ground the probes on the PCB. Set the inputs to AC, Add and invert one channel. Set the vertical deflection to 100 MV/dev.

e. The two lobes must be within 70% amplitude of each other. If the lobes do not fall within the specification, continue on with the procedure. Reference Figure 9.

f. Loosen the two mounting screws which hold the motor clamp to the mounting plate.

CAUTION: DO NOT LOOSEN THREE SCREWS COATED WITH GLYPTOL.

g. Rotate the stepper motor to radially move the head in or out. If the left lobe is less than 70% of the right, turn the stepper motor counter-clockwise as viewed from the rear. If the right lobe is less than 70% of the left lobe, turn the stepper motor clockwise as viewed from the rear.

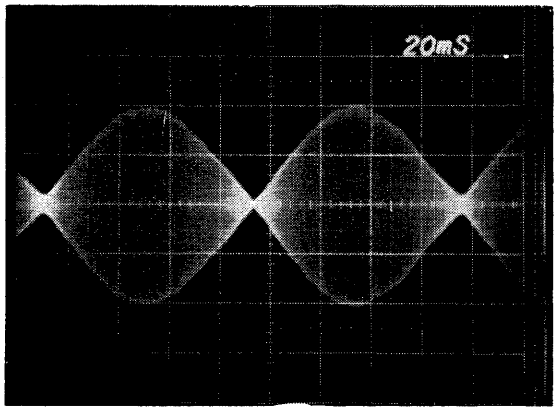


FIGURE 9 HEAD RADIAL ALIGNMENT

h. When the lobes are of equal amplitude, tighten the motor clamp mounting screws. Reference Figure 9.

i. Check the adjustment by stepping off track and returning. Check in both directions and readjust as required.

j. Whenever the Head Radial Alignment has been adjusted, the Track 00 flag adjustment (Section 4.11.8), Track 00 stop (Section 4.11.7) and R/W head azimuth (Section 4.11.9) must be checked.

4.11.3 Read/Write Head Load Button: Removal and Installation

a. Remove side cover if installed.

b. To remove the old button, hold the arm out away from head, squeeze the locking tabs together with a pair of needle nose pliers and press forward.

c. To install load button, press the button into the arm, from the head side, and it will snap in place. Reference Figure 10.

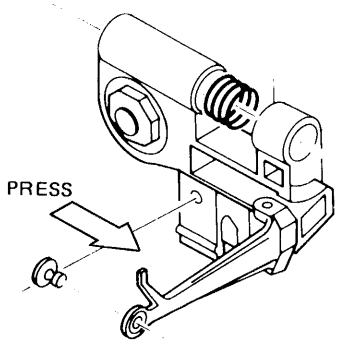


FIGURE 10

d. Adjust according to Section 4.11.4.

Note: The load arm should never be opened over 90° from carriage assembly or while at track 00 to prevent possible damage to the torsion spring.

4.11.4 Read/Write Head Load Button Adjustment

a. Insert Alignment Diskette (SA120).

b. Connect oscilloscope to TP 1 and 2, added differentially and sync negative external on TP 12 (- INDEX).

c. Step carriage to track 75.

d. Observing read signal on oscilloscope, rotate the load button counter-clockwise in small increments (10°) until maximum amplitude is obtained.

4.11.5 Head Penetration Adjustment

Note: This adjustment is not normally done in the field. The only time that this adjustment need be done is when the stepper mounting plate has been loosened or removed.

a. Place the penetration tool (P/N 50380) on the gauge block and insure that the gauge reads .030 (3 on the small hand) and zero the dial for the large hand. This results in a reading of .030".

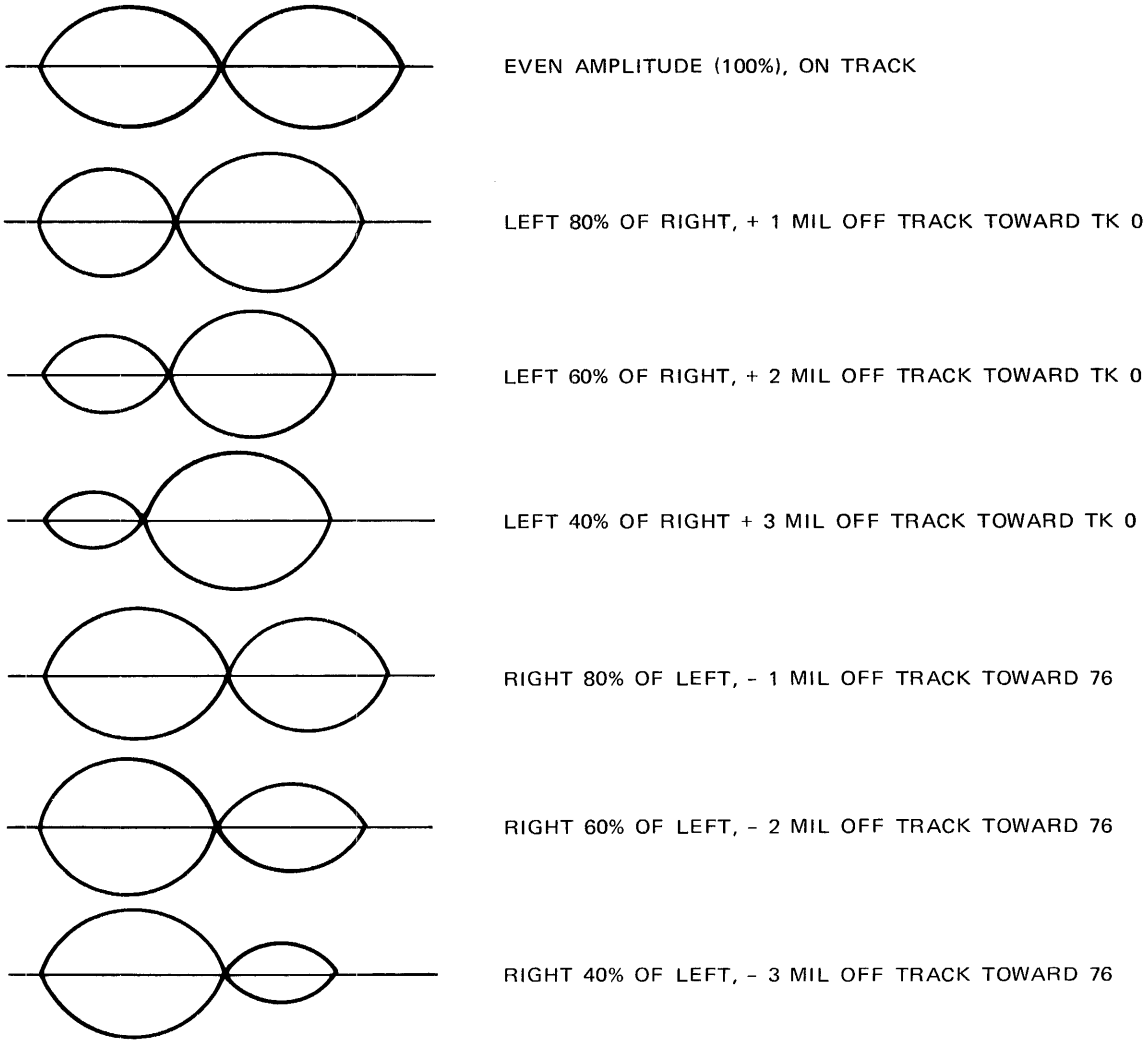


Figure 11 R/W Head Radial Alignment

b. Swing open the cartridge as per Section 4.3.

c. Place the penetration tool on the base assembly with the short leg on the platen, the long leg on the carriage guide bar, and the plastic tip in the center of the R/W head.

d. The head penetration should be .030" ± .003" read on the gauge.

e. If the head does not meet this adjustment, move the stepper plate laterally until the gauge reads .030".

f. Tighten the screws and recheck the adjustment.

g. Return cartridge guide and adjust as per Section 4.9.2.

h. Adjust Azimuth (Section 4.11. 9).

4.11.6 Track 00 Detector: Removal and Installation

a. Remove side cover (Section 4.2).

b. Swing cartridge guide open (Section 4.3).

c. Manually rotate stepper shaft and move carriage all the way in.

d. Remove 2 screws holding bracket to base casting and remove bracket and detector.

e. Remove PCB connector and remove PCB.

f. Extract cable from P2 connector; Brown, A (R1); Black, C (R3); Red, F (R6); and Orange K (R9).

g. Remove cable clamps and remove Detector assembly.

h. To install, reverse the procedure.

i. Adjust according to Section 4.11.8.

4.11.7 Track 00 Stop Adjustment

a. Remove side cover (Section 4.2).

b. Step carriage to track 00. Verify that carriage is at 00 by checking P1 pin 42 is minus (ground).

c. Check that stop is .040" ± .020" between collar and carriage. Turn DC power OFF, and manually rotate lead screw clockwise until carriage stops. Check that stop is .020" ± .010" between collar and carriage.

d. If clearances are not within tolerance, continue on with adjustment procedure.

e. Turn DC power ON.

f. Step carriage to track 02.

g. Loosen Track 00 stop collar.

h. Grasp end of lead screw, in back of stepper motor, with a pair of pliers and manually turn lead screw clockwise to the track -01 position. (Next detent position on stepper motor.)

i. Position the stop collar axially along the lead screw so there is .020" ± .010" between collar and carriage. Rotate the collar toward inside until the stop on the collar contacts the carriage stop surface. Tighten screw.

j. Turn DC Power OFF and back ON. Carriage should move to track 00. Verify that there is data at track 00.

k. Step carriage between track 00 and 76 and check for any binding or interference between the carriage, lead screw, stop and head cable.

4.11.8 Track 00 Flag Adjustment

a. Remove side cover (Section 4.2).

b. Check head radial alignment and adjust if necessary before making this adjustment.

c. Connect oscilloscope probe to TP 26. Set vertical deflection to 1 v/division and sweep to continuous.

d. Step carriage to track 01. TP 26 should be high (+5 volts).

e. If TP 26 is not high, loosen screw holding Track 00 flag and move flag towards stepper until TP 26 just goes high.

f. Step carriage to track 2. TP 26 should go low. Adjust flag towards spindle if not low.

g. Check adjustment by stepping carriage between tracks 00 and 02, observing that TP 26 is low at track 02 and high at tracks 01 and 00.

h. Replace side cover.

4.11.9 R/W Head Azimuth Alignment

This adjustment can only be made on SA800/801's at MLC 3 or higher with a new style stepper plate which has 50112-4 stamped on it. This adjustment is only necessary when the stepper or carriage assembly has been replaced or if the stepper plate has been loosened.

a. If stepper plate has been loosened or replaced adjust head penetration, Section 4.11.5.

b. Align R/W head, 4.11.3.

c. Install C.E. alignment diskette SA 120-1. Select the drive and step to track 76.

d. Sync the scope external negative on TP 12, set time base to .5 MSec per DIV.

e. Connect one probe to TP 1 and the other to TP 2. Invert one channel and ground the probes to TP 5 & 6. Set the inputs to AC, ADD and 50 MV per division.

f. Compare the wave form to Figure 13. If not within the range shown the head Azimuth will require adjustment. If required, proceed to next step.

g. Slightly loosen the 2 R.H. stepper plate mounting screws only. Reference Figure 12. Do not loosen the L.H. screw as this will effect the head penetration adjustment.

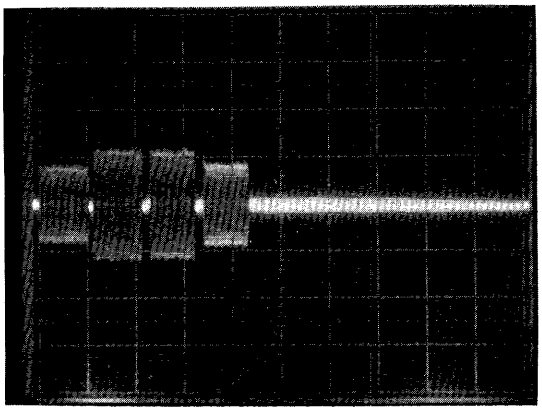


FIGURE 13

h. Push the stepper down towards the A.C. drive motor until the 1st sector is larger than the 2nd sector.

i. Pry the R.H. side of the stepper plate up with a medium screw driver until the 1st and 4th sectors have equal to or less amplitude than the middle 2 sectors. Reference Figure 13.

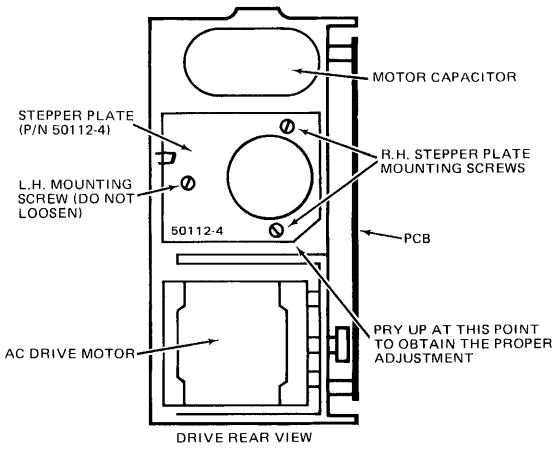


FIGURE 12

j. Re-tighten the 2 R.H. screws. If either of the outside 2 sectors increase in amplitude greater than the inside 2 after re-tightening the screws, perform the adjustment again.

k. Check and re-adjust the index timing and head radial adjustment if required.

4.11.10 Stepper Plate Removal and Adjustment

a. Remove PCB.

b. Remove head and carriage assembly from stepper lead screw, section 4.11.1.

c. Pull the stepper motor out thru the stepper plate until the lead screw is completely clear of the plate.

d. Remove the 3 stepper plate mounting screws.

e. Reinstall the stepper plate.

NOTE: If the stepper plate is P/N 50112-4, there must be a nylon bushing in the L.H. hole and all 3 screws must have a flat washer and a black spring washer.

f. Reinstall head and carriage and stepper motor assemblies.

g. Adjust penetration, Section 4.11.5. If the stepper plate is P/N 50112-4, there will remain a gap between the bottom of the stepper plate and the machined surface on the casting. All other style stepper plates must remain flush with machined surface.

h. Readjust carriage assembly, Section 4.11.2.

i. Check and adjust Azimuth alignment, Section 4.11.10.

4.12 Activity Light Removal and Installation (Standard)

a. Remove P6 connector from PCB.

b. Remove cable clamp holding the cable and remove cable from clamp.

c. Remove the 2 screws holding the push button.

d. Remove push button and activity light from the front as an entire assembly.

e. Install the light and push button assembly by reversing the removal procedure.

f. No special orientation is required when installing P6 onto the PCB. No adjustments are required to the push button assembly.

4.13 Door Lock

a. Disconnect P6 connector.

b. Disconnect red wire near IC 2G.

c. Remove front plate (Section 4.10).

b. Remove two screws holding assembly to front plate.

c. Remove two allen head screws holding assembly to push button.

d. Grasp both ends of push button and bow outwards to remove LED.

e. Reverse procedure to assemble.

f. Adjustment of the door lock should not be necessary. If it has to be, the gap between the armature tab and the latch should be .015 ± .010. This adjustment can be made by loosening the two screws on the armature.

4.14 Activity Light (with Door Lock Option)

a. Follow procedure for door lock (4.13).

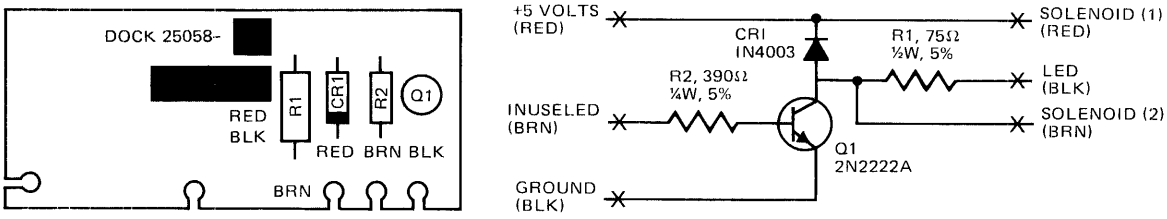
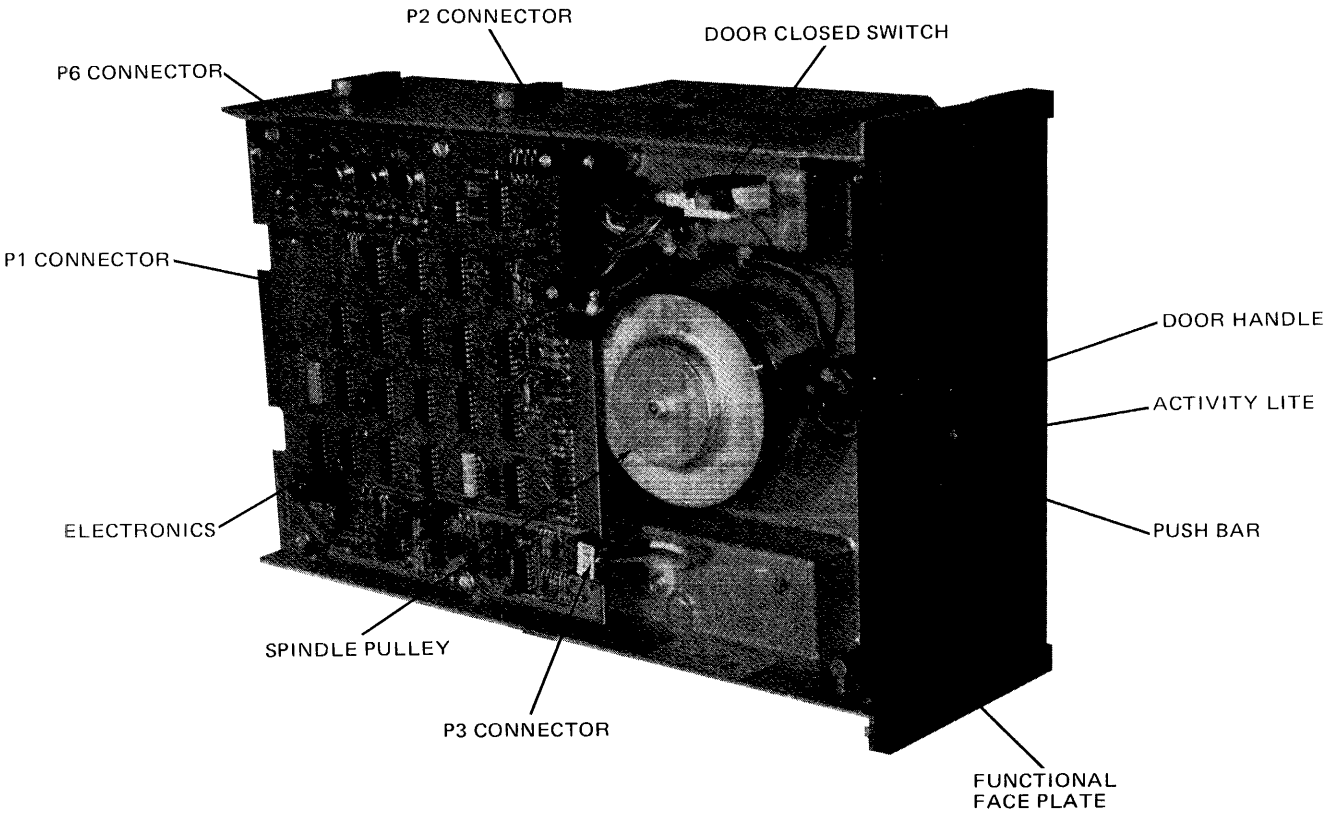
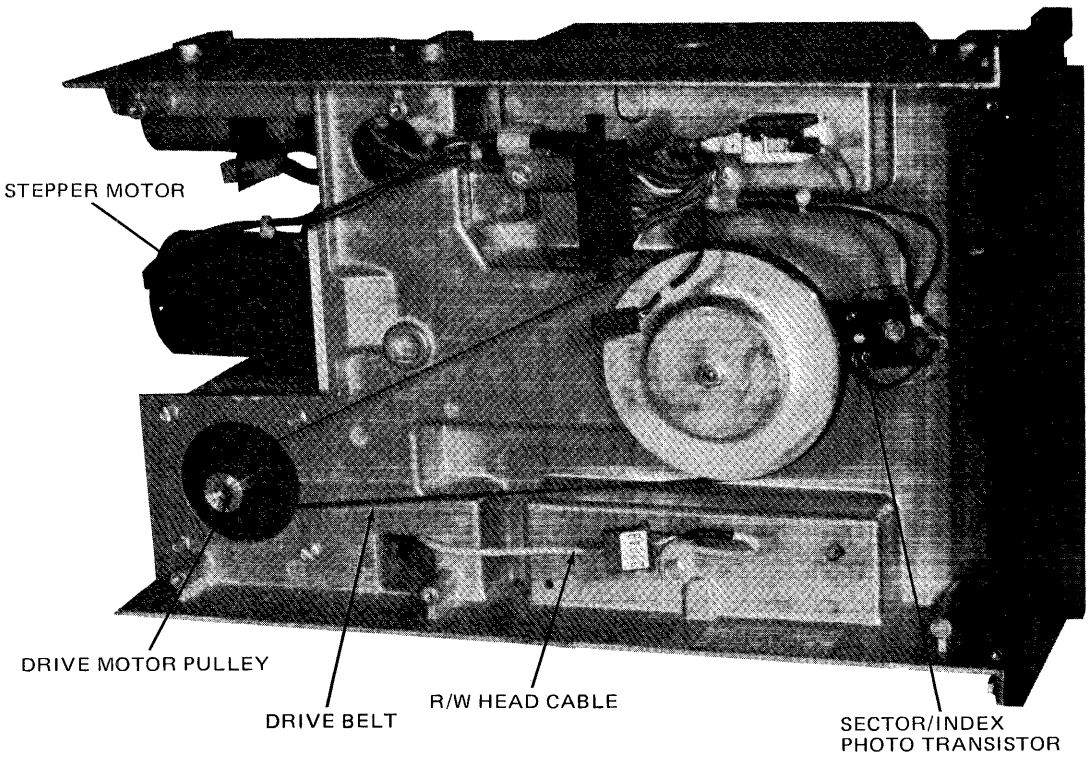
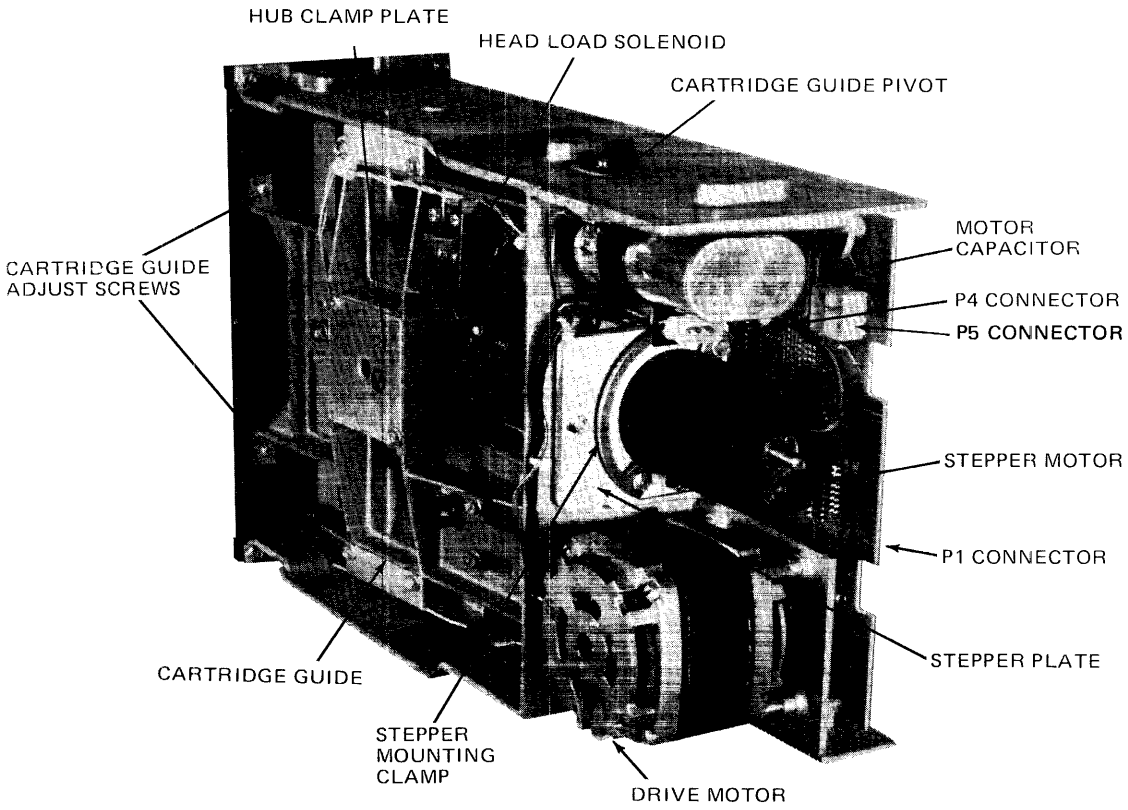
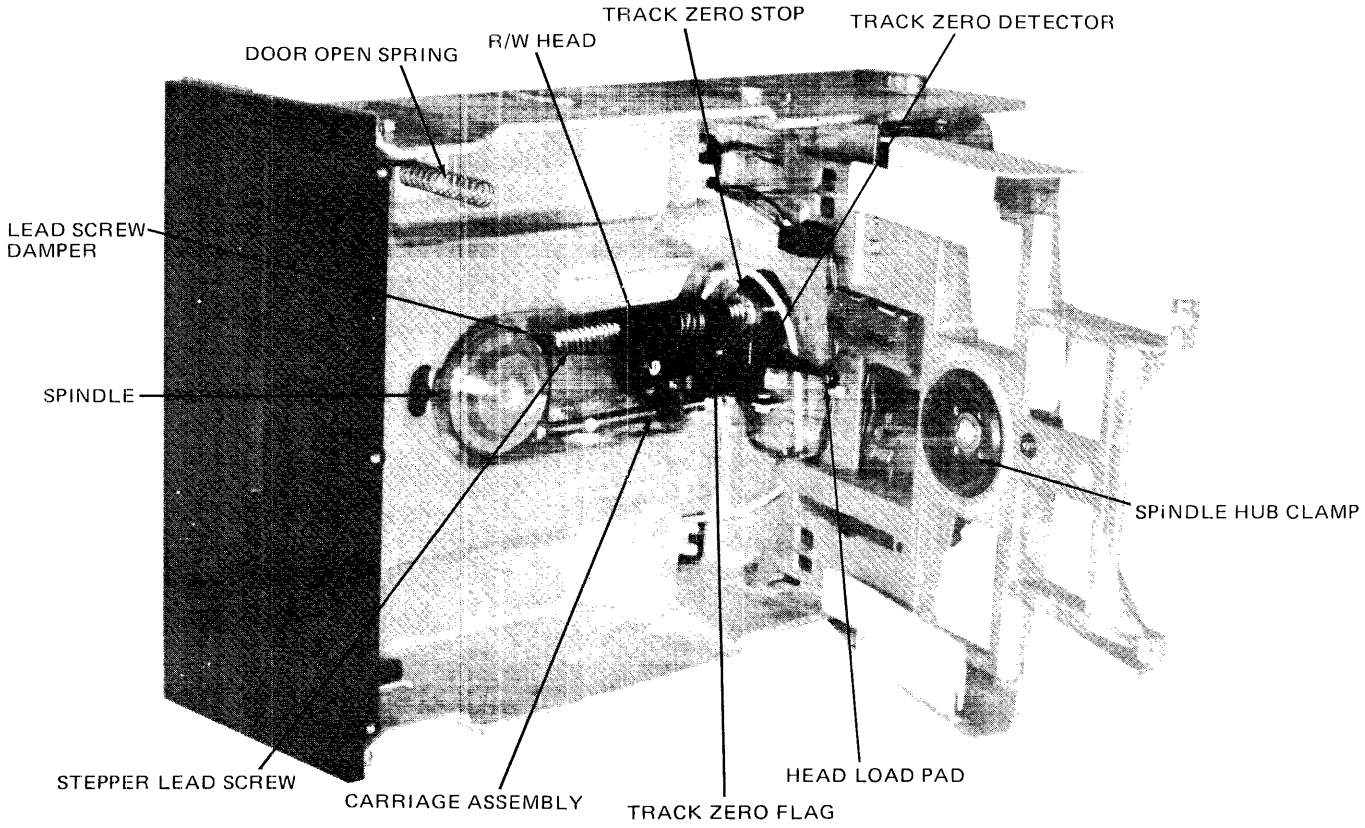


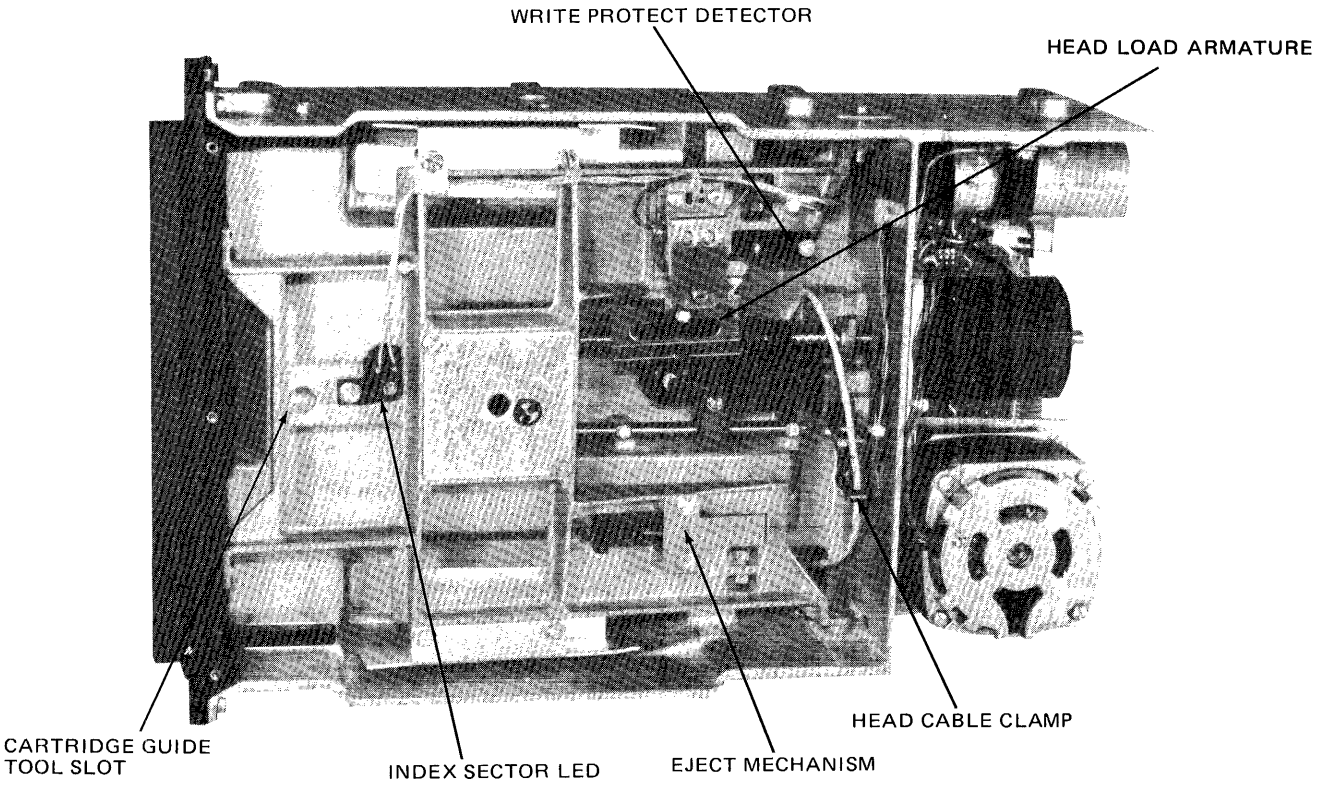
FIGURE 14 DOOR LOCK SCHEMATIC


P2 CONNECTOR
DOOR CLOSED SWITCH
P6 CONNECTOR
P1 CONNECTOR
DOOR HANDLE
ACTIVITY LITE
ELECTRONICS
PUSH BAR
SPINDLE PULLEY
P3 CONNECTOR
FUNCTIONAL
FACE PLATE

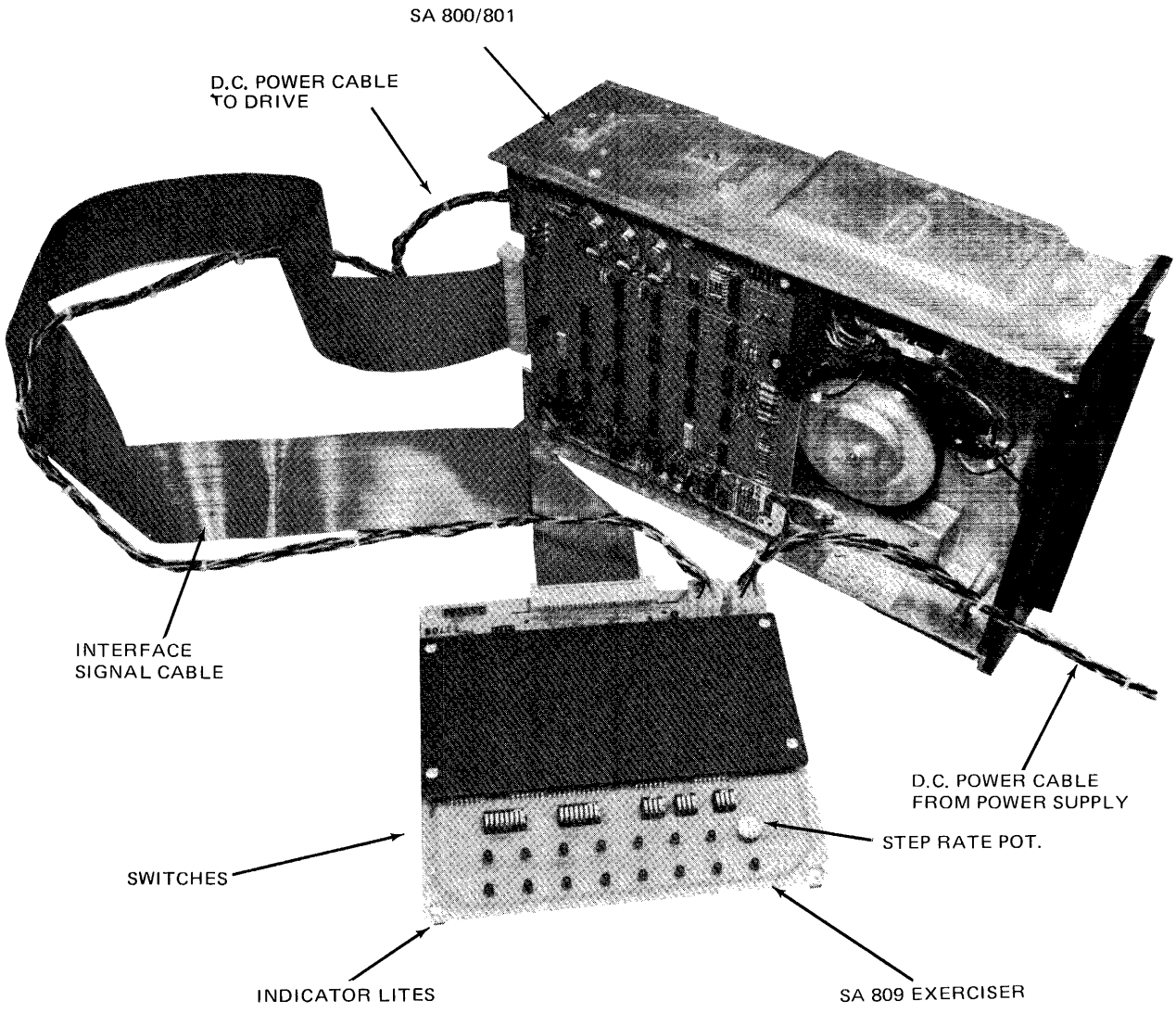

STEPPER MOTOR
DRIVE MOTOR PULLEY
DRIVE BELT
R/W HEAD CABLE
SECTOR/INDEX
PHOTO TRANSISTOR

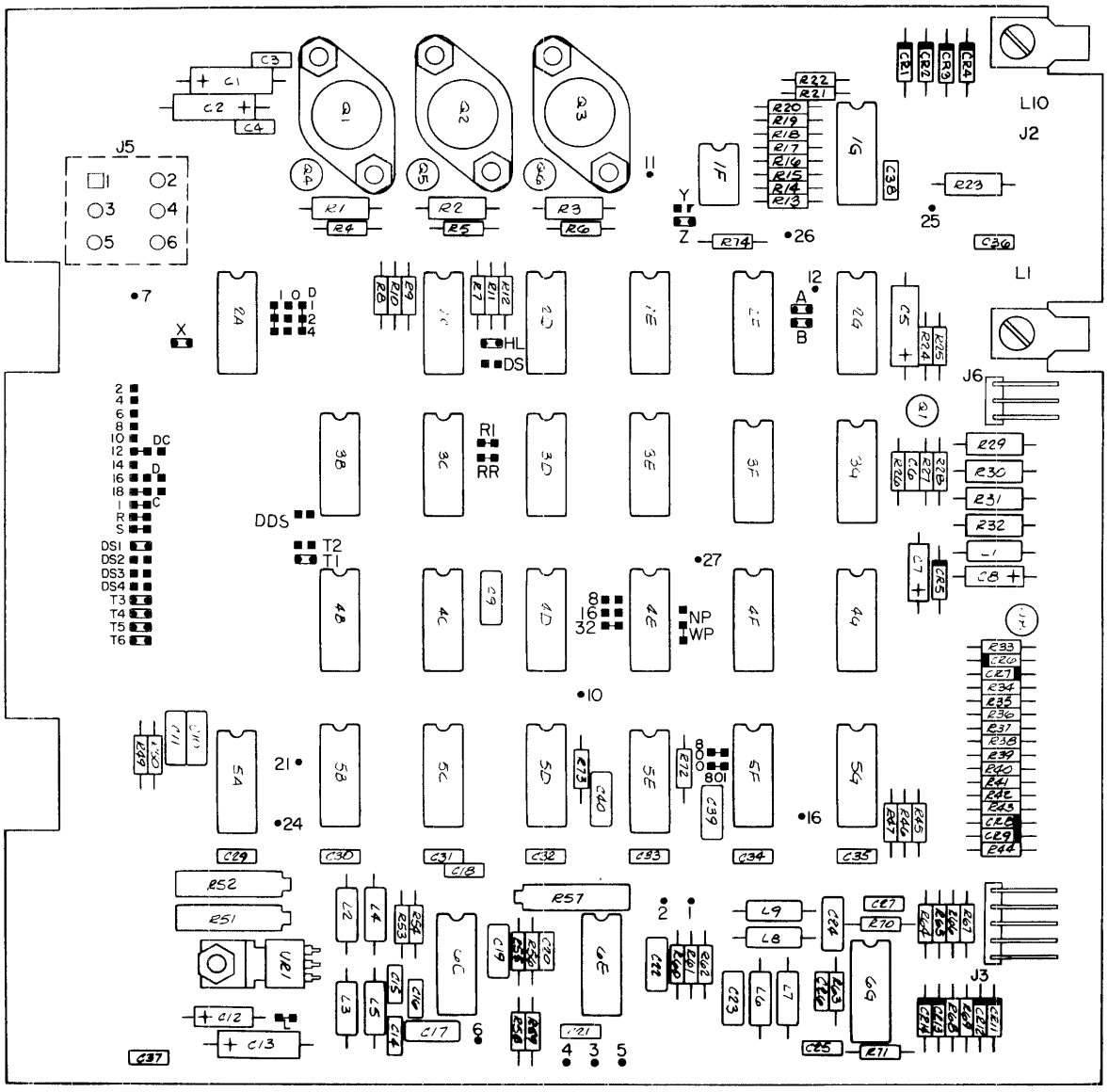

HUB CLAMP PLATE
HEAD LOAD SOLENOID
CARTRIDGE GUIDE PIVOT
CARTRIDGE GUIDE ADJUST SCREWS
MOTOR CAPACITOR
P4 CONNECTOR
P5 CONNECTOR
STEPPER MOTOR
P1 CONNECTOR
STEPPER PLATE
CARTRIDGE GUIDE
STEPPER MOUNTING CLAMP
DRIVE MOTOR


TRACK ZERO STOP
TRACK ZERO DETECTOR
DOOR OPEN SPRING
R/W HEAD
LEAD SCREW DAMPER
SPINDLE
SPINDLE HUB CLAMP
STEPPER LEAD SCREW
CARRIAGE ASSEMBLY
TRACK ZERO FLAG
HEAD LOAD PAD


WRITE PROTECT DETECTOR
HEAD LOAD ARMATURE
CARTRIDGE GUIDE TOOL SLOT
INDEX SECTOR LED
EJECT MECHANISM
HEAD CABLE CLAMP

6 SA809 EXERCISER CONNECTION





■ Jumper Plug Installed as Shipped

• Test Point

SA800/801 PCB Component Location

PART NO. 50591-0

LOGIC MANUAL DRIVE SN _____

INDEX

TABLE III

CUSTOMER CUT TRACE OPTIONS

DESIGNATOR	DESCRIPTION	SHIPPED FROM FACTORY OPEN	SHIPPED FROM FACTORY SHORT
T3,T4,T5 & T6	TERMINATIONS FOR MULTIPLEXED INPUTS		[1] X
T2	SPARE TERMINATOR FOR RADIAL HEAD LOAD	X	
TI	TERMINATION FOR DRIVE SELECT		[1] X
DSI	DRIVE SELECT INPUT – ALTERNATE PINS: DS2, DS3, DS4		[1] X
RR	RADIAL READY		X
RI	RADIAL INDEX AND SECTOR		X
R,I,S	READY, INDEX, SECTOR ALTERNATE OUTPUT PROVISION		X
A,B,X	RADIAL HEAD LOAD		[1] X
HL	STEPPER POWER FROM HD LD		[1] X
DS	STEPPER POWER FROM DRIVE SELECT	X	
WP	INHIBIT WRITE WHEN WRITE PROTECTED		X
NP	ALLOW WRITE WHEN WRITE PROTECTED	X	
8,16,32	8, 16 OR 32 SECTORS		
D	ALTERNATE INPUT – IN USE	X	
2,4,6,8,10,12,14,16,18	NINE ALTERNATE I/O PINS	X	
DI, D2, D4, DDS	CUSTOMER INSTALLABLE DECODE DRIVE SELECT OPTION	X	
C	ALTERNATE INPUT – HEAD LOAD	X	
Z	INUSE LED FROM DRIVE SELECT		[1] X
Y	INUSE LED FROM HD LD	X	
DC	ALTERNATE OUTPUT – DISK CHANGE	X	

FACTORY CUT TRACE OPTIONS AND HISTORY CHART

L	-5 OR -7 TO -16V	SEE TABLE II
800	INDEX ONLY (800)	SEE TABLE II
801	INDEX AND SECTOR (801)	SEE TABLE II

[1] OPEN TRACE WITH SHORTING PLUG INSTALLED.

TABLE I

OPTIONAL FEATURES

PCB ASM NO.	OPTIONAL FEATURES -5V	-7 TO -16V	DATA SEP	SECTOR SEP
25102	X			
25103		X		
25104	X		X	
25105		X	X	
25106	X		X	X
25107		X	X	X

WRITE PROTECT CAN BE ORDERED WITH ANY OF THE ABOVE

TABLE II

FACTORY CUT TRACE OPTIONS

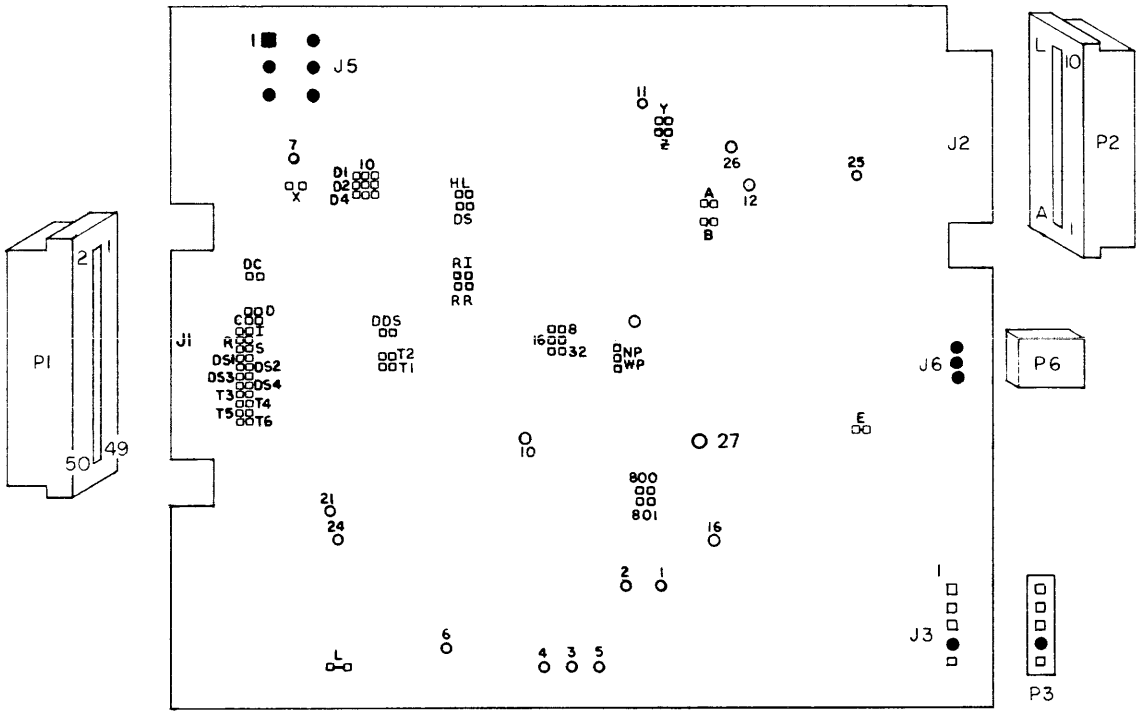
PCB ASM NO	TRACE "L"	TRACE "801"	TRACE "800"
25102	SHORTED	OPEN	SHORTED
25103	OPEN	↕	↕
25104	SHORTED	↕	↕
25105	OPEN	OPEN	SHORTED
25106	SHORTED	SHORTED	OPEN
25107	OPEN	SHORTED	OPEN

LOGIC MANUAL P/N 50590-1

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY DATE	NO.	SHUGART ASSOCIATES	
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	6-75	0398	TITLE INDEX	
	LINEAR ±.XX	1-76	0509	DETAIL	RELEASED FOR ASSEMBLY
CASE DEPTH	±.XXX			DESIGN	50590
HARDNESS	ANGULAR±			APPRO	SHEET 1 OF 1
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX / INSIDE MAX			C SCALE — DOC CODE OD PART NO 50591-0 REV/EC 0509	

AA001

PART NO. 50592-0

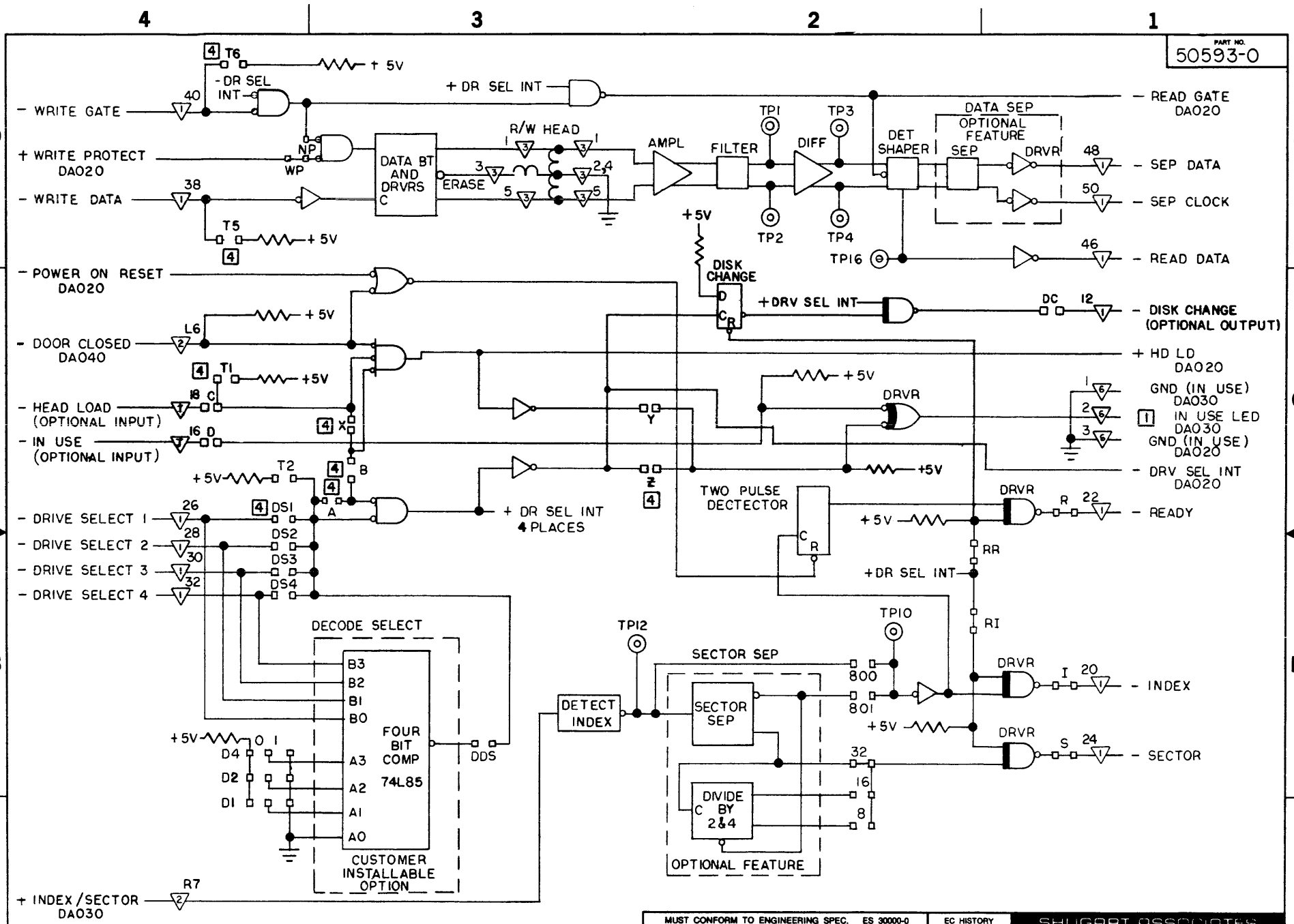


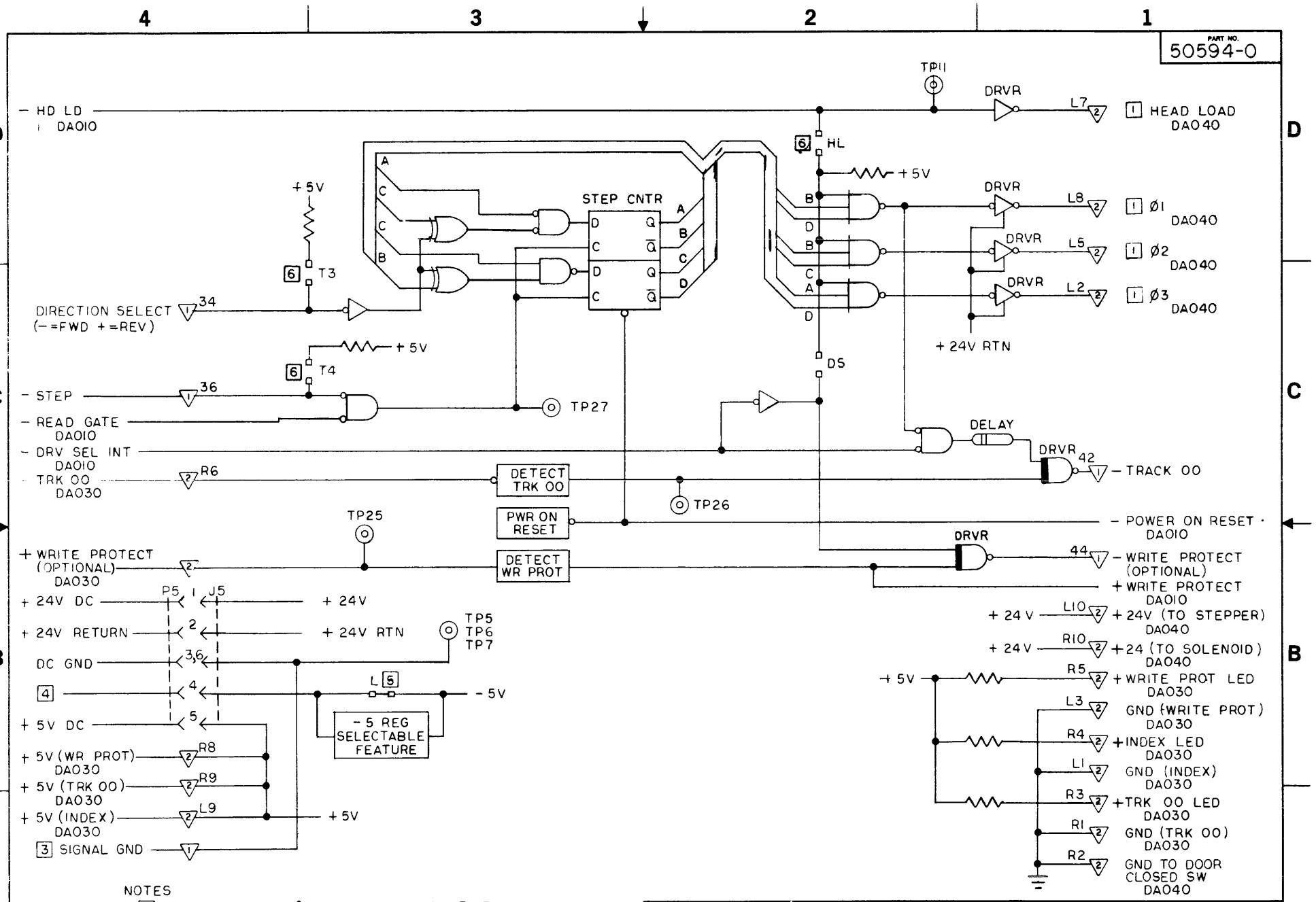
TEST POINTS	
TP1‡TP2	FILTERED READ SIGNAL
TP3‡TP4	DIFFERENTIATED READ SIGNAL
TP5,TP6,TP7	SIGNAL GROUND
TP10	−INDEX (TTL)
TP11	−LOAD HEAD (TTL)
TP12	−DETECTED INDEX/SECTOR HOLES(TTL)
TP16	+READ DATA (TTL)
TP21	DATA SEPARATOR TIME t1 (TTL)
TP24	DATA SEPARATOR TIME t2(TTL)
TP25	+WRITE PROTECT
TP26	+DETECTED TRACK ZERO (TTL)
TP27	+GATED STEP PULSE (TTL)

NOTES:
1. ⊓–⊓/⊓⊓ DENOTES CUT TRACE/JUMPER OPTION.
2. ○ DENOTES TEST POINTS.

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0			EC HISTORY		SHUGART ASSOCIATES		
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED		DATE	NO.	TITLE	PCB TRACE AND TEST POINT LOCATION	
			6-75	0398			
	LINEAR ±.XX		1-76	0509	DETAIL	6-6-75	RELEASED FOR ASSEMBLY
CASE DEPTH	±.XXX				DESIGN		50590
HARDNESS	ANGULAR ±				APPRO	6-7-75	SHEET OF
SURFACE TREATMENT ES	CORNERS EDGES BROKEN	OUTSIDE MAX			SCALE	DOC CODE	PART NO. / REV/EC
		INSIDE MAX			C —	OD	50592-0 / 0509

AB010


PART NO. 50593-0
- WRITE GATE
+ WRITE PROTECT DA020
- WRITE DATA
- DR SEL INT
+ DR SEL INT
NP
WP
DATA BT AND DRVRS
ERASE
R/W HEAD
AMPL
FILTER
DIFF
DET SHAPER
DATA SEP OPTIONAL FEATURE
SEP
DRVR
TP1
TP2
TP3
TP4
TP16
+5V
T5
T6
- READ GATE DA020
- SEP DATA
- SEP CLOCK
- READ DATA
- POWER ON RESET DA020
DISK CHANGE
+DRV SEL INT
- DISK CHANGE (OPTIONAL OUTPUT)
- DOOR CLOSED DA040
L6
T1
- HEAD LOAD (OPTIONAL INPUT)
- IN USE (OPTIONAL INPUT)
+ HD LD DA020
GND (IN USE) DA030
IN USE LED DA030
GND (IN USE) DA020
- DRV SEL INT DA020
T2
- DRIVE SELECT 1
- DRIVE SELECT 2
- DRIVE SELECT 3
- DRIVE SELECT 4
DS1
DS2
DS3
DS4
+ DR SEL INT 4 PLACES
TWO PULSE DECTECTOR
- READY
RR
RI
DECODE SELECT
FOUR BIT COMP 74L85
DDS
CUSTOMER INSTALLABLE OPTION
TP12
TP10
SECTOR SEP
DETECT INDEX
800
801
DIVIDE BY 2&4
OPTIONAL FEATURE
- INDEX
- SECTOR
+ INDEX/SECTOR DA030
R7
NOTES:
1. GND WHEN INACTIVE AND + 1.5VDC WHEN ACTIVE
2. CONNECTOR SYMBOL REFERENCE ①=J1, ②=J2, ③=J3, ⑥=J6
3. ALL ODD NUMBERED PINS ON J1 CONNECTOR ARE GROUND.
4. SHORTING PLUG INSTALLED.
DA010
MUST CONFORM TO ENGINEERING SPEC. ES 30000-0
MATERIAL
TOLERANCE UNLESS OTHERWISE NOTED
LINEAR ±.XX ±.XXX
ANGULAR±
CASE DEPTH
HARDNESS
SURFACE TREATMENT ES
CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX
EC HISTORY
DATE NO.
6-75 0398
1-76 0509
SHUGART ASSOCIATES
TITLE READ/WRITE/INDEX/SECTOR
DETAIL RELEASED FOR ASSEMBLY
DESIGN 50590
APPRO SHEET 1 OF 1
C SCALE — DOC CODE OD PART NO. 50593-0 REV/EC 0509



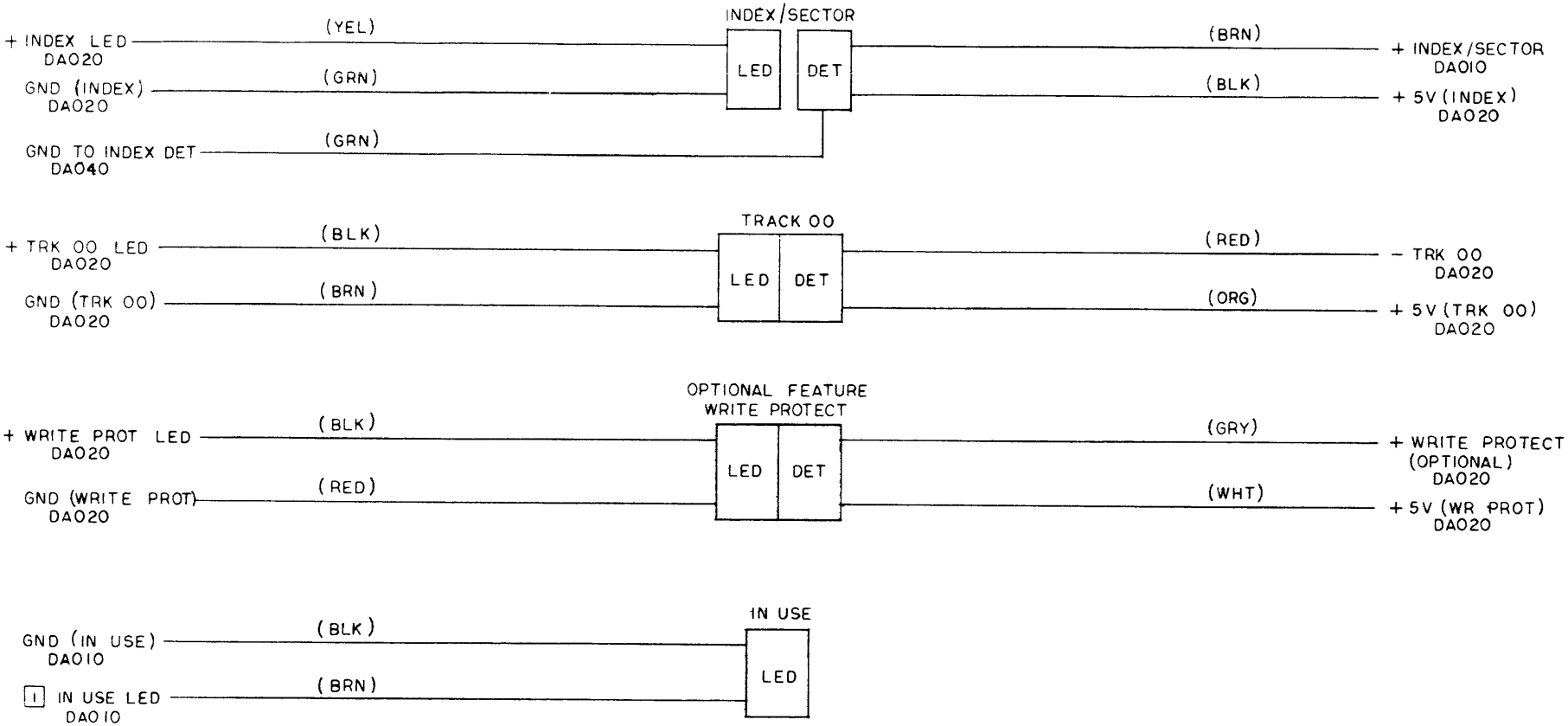
NOTES

1. GND WHEN ACTIVE & + 24VDC WHEN INACTIVE
2. CONNECTOR SYMBOL REFERENCE ▽=J1, ▽2=J2, ▽5=J5.
3. ALL ODD NUMBERED PINS ON J1 CONNECTOR ARE GROUND.
4. -5V OR -7V TO -16V SELECTABLE FEATURE.
5. CUT TRACE L FOR -7V TO -16V INPUT AT P5-4. SEE PAGE AA001, TABLE II
6. SHORTING PLUG INSTALLED.

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY		SHUGART ASSOCIATES	
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.	TITLE	STEPPER CONTROL
		6-75	0398		
	LINEAR ±.XX ±.XXX	1-76	0509	DETAIL C.W. 6-6-75	RELEASED FOR ASSEMBLY
CASE DEPTH				DESIGN	50590
HARDNESS	ANGULAR ±			APPRO	SHEET OF
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX			C —	DOC CODE OD PART NO. 50594-0 REV/EC 0509

DA020

PART NO. 50595-0

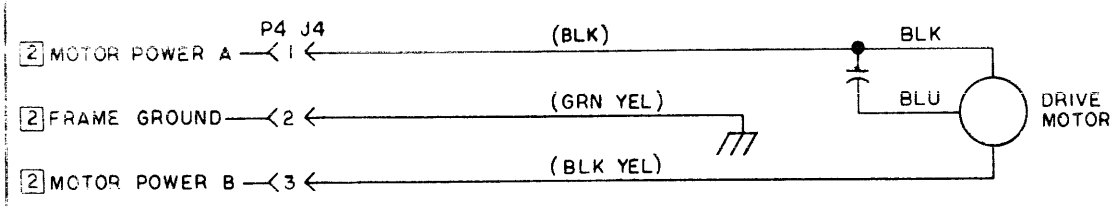


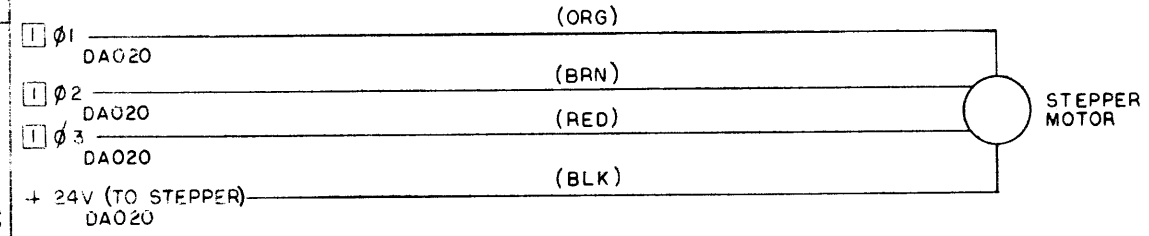
NOTES:
[1] GND WHEN INACTIVE AND +1.5VDC WHEN ACTIVE

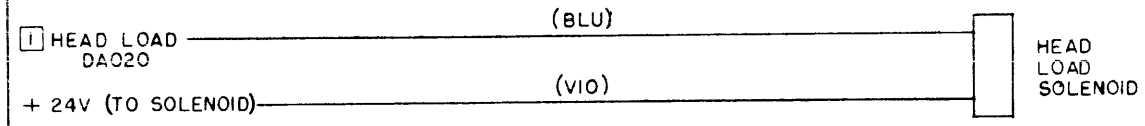
MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY		SHUGART ASSOCIATES	
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.	TITLE	DETECTORS
		6-75	0398	DETAIL	RELEASED FOR ASSEMBLY
CASE DEPTH	LINEAR ±.XX ±.XXX			DESIGN	50590
HARDNESS	ANGULAR±			APPRO	SHEET 1 OF 1
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX			C	SCALE — DOC CODE 00 PART NO 50595-0 REV/EC 0398

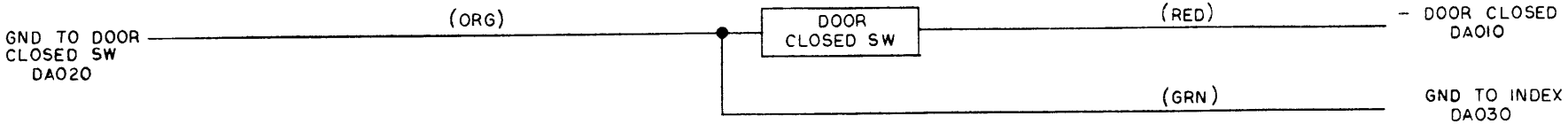
DA030

PART NO. 50596-0









NOTES:
1. GND WHEN ACTIVE & +24V WHEN INACTIVE.
2. 115 OR 230 VAC

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY		SHUGART ASSOCIATES	
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.	TITLE	MOTORS/SOLENOID/SWITCH
		6-75	0398		
	LINEAR ±.XX	1-75	0509	DETAIL 6[illegible] 6-68	RELEASED FOR ASSEMBLY
CASE DEPTH	LINEAR ±.XXX			DESIGN	50590
HARDNESS	ANGULAR±			APPRO 6-7 6-75	SHEET 1 OF 1
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX / INSIDE MAX			C — 00	PART NO. 50596-0 REV/EC 0509

DA040

SA800/801 SCHEMATIC DIAGRAMS

PART NO. 25100-2

— WRITE DATA
+ WRITE PROT XSBO1
— WRITE GATE
+ PULL UP XSBO1
— DRIVE SELECT 1
2
3
4
DS
+ TRACK ZERO XSBO1
— HEAD LOAD (JUMPER OPTIONABLE I/O)
— DOOR CLOSED
— IN USE (JUMPER OPTIONABLE I/O)
+ 24V
+ 24V RETURN
+ 5V
GROUND
— 5V OR -7V TO -16V
— STEP
+ DIRECTION SELECT

CUSTOMER INSTALLED OPTION

ALL ODD NUMBERED PINS

+24VA
+24V RTN
+5VT
+5VA
+5V
-5VA
-5VT

2N2222A
QT 2N2222A

— READ/WRITE (1) XSBO1
— XSBO1
+ READ/WRITE (2)
+ ERASE DRV (3)
— READ GATE XSBO1
— DRV SEL INT XSBO1
— TRACK ØØ
+ DRV SEL INT XSBO1
— HEAD LOAD
— DOOR CLOSED XSBO1
+ IN USE LED
— POR XSBO1
Ø1
Ø2
Ø3

NOTES, UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V, +80,-20%.
3. ALL INDUCTORS ARE 100MH, 10%.
4. ALL DIODES ARE IN4148.
5. ALL TRANSISTORS ARE 2N2907A.
6. -□-□- INDICATES CUT-TRACE OPTION.
7. -□ □- INDICATES JUMPER OPTION.
8. CONNECTOR SYMBOL REFERENCES; (X) = J1, (2) = J2, (3) = J3, (5) = J5, (6) = J6.
9. I.C. LOCATION 4B IS A RESISTOR PACK, 150Ω, 1/2W, 5%.
10. I.C. LOCATION 3B IS A RESISTOR PACK, 2K, 1/4W, 5%.
11. ADD JUMPER L FOR -7V TO 16V ON ASSEMBLIES; 25103, 25105, 25107.
12. PINS 8 AND 9 OF 1G ARE GROUND.
13. SHORTING PLUG INSTALLED.
14. REMOVE JUMPER FROM 800 AND INSTALL IN 801.

XSBOO

REFERENCE DESIGNATION

LAST USED	NOT USED
C40	C28(RESERVED)
CR14	CR10
L9	
Q8	
R74	R48
TP27	TP8,9,13,14,15,17-20,22,23,
VR1	

TYPE	POSITION	UNUSED ELEMENTS	VCC PIN	GND PIN
7400	5C,2E,5F	2E1,4,5F2,4	14	7
7402	4E	4E3		
7404	3E			
7405	4D	4D2,3		
7407	4G			
7410	5B,2C	5B1		
7438	3C,4C			
7474	2D,3D,5D,4F			
7476	3F		5	13
7486	2G	2G4	14	7

TYPE	POSITION	UNUSED ELEMENTS	VCC PIN	GND PIN
74LS5	2B		16	8
75452P	1F		8	4
8T20	6C		~	8
9602	5A,5E,3G		16	8
LM339	1G	1G3	3	12
NE592A	6E		~	~
2QT2222	6G		~	~
2QT2905	5G		~	~
7428	2F		14	7
7427	2A	2A1,2	14	7

USED ON ASSEMBLY
25102-4
25103-4
25104-4
25105-4
25106-4
25107-4

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0

EC HISTORY	DATE	NO.
	10-76	0591
	11-76	0702

MATERIAL
TOLERANCE UNLESS OTHERWISE NOTED
LINEAR ±.XX ±.XXX
ANGULAR±
CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX
CASE DEPTH
HARDNESS
SURFACE TREATMENT ES

SHUGART ASSOCIATES

TITLE SCHEMATIC DIAGRAM DISKETTE, 800 SERIES

DETAIL	A.Ja.	3-75	RELEASED FOR ASSEMBLY
DESIGN			T25100
APPRO	[illegible]	6-75	SHEET 1 OF 2

SCALE ~ DOC CODE SC PART NO. 25100-2 REV/EC 0702

PART NO. 25100-2

- TRACK ZERO
- DRV SEL INT XS800
+ WRITE PROTECT
+ DRV SEL INT XS800
- DOOR CLOSED XS800
- POR XS800
+ INDEX/SECTOR
+ READ/WRITE (1) XS800
+ READ/WRITE (2) XS800
- READ GATE XS800

+ TRACK ZERO XS800
- DISK CHANGE
+ WRITE PROTECT XS800
- WRITE PROT
+ PULL UP XS800
- READY
- INDEX
- SECTOR
- READ DATA
- SEP DATA
- SEP CLOCK
+ WRITE PROT LED
+ TRK ØØ LED
+ INDEX LED

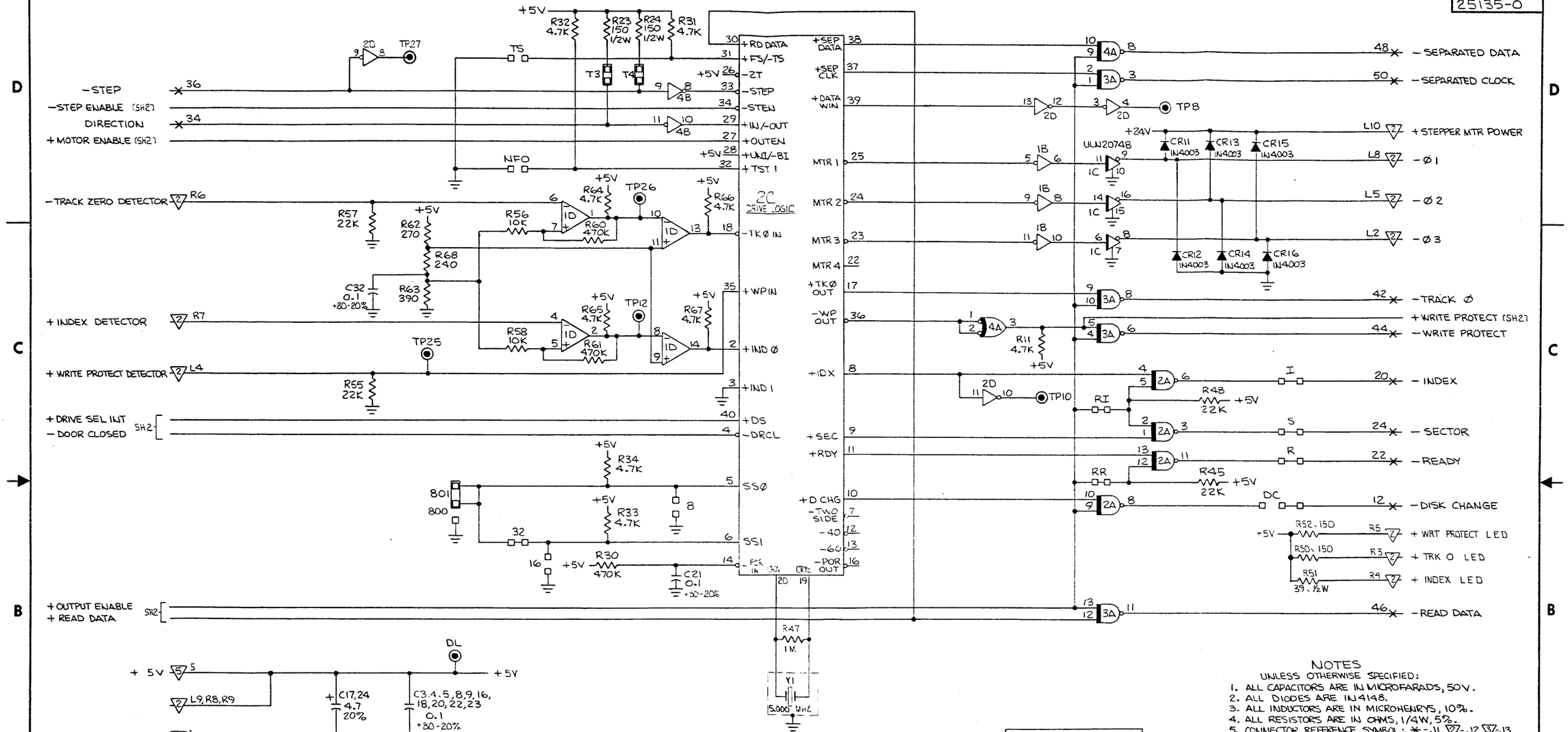
SECTOR SEPERATOR
USED ON ASSEMBLY
25106
25107

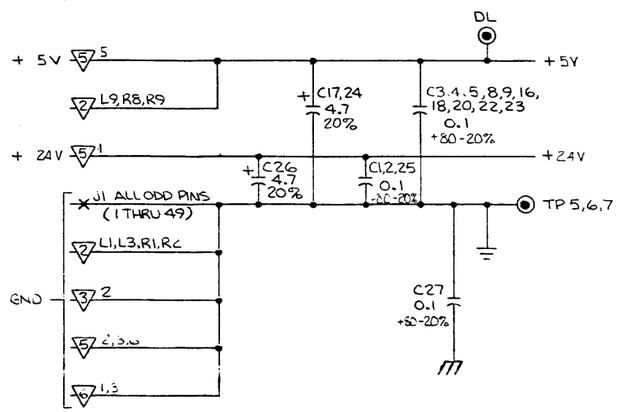
DATA SEPERATOR
USED ON ASSEMBLY
25104
25105
25106
25107

XS801

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY	SHUGART ASSOCIATES
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE / NO.	TITLE SCHEMATIC DIAGRAM DISKETTE, 800 SERIES
	LINEAR ±.XX ±.XXX		DETAIL A.L. 5-75 RELEASED FOR ASSEMBLY
CASE DEPTH			DESIGN T25100
HARDNESS	ANGULAR±		APPRO 6-7 6-75 SHEET 2 OF 2
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX / INSIDE MAX		D SCALE ~ DOC CODE 5C PART NO 25100-2 REV/EC 0702

PART NO 25135-0





TYPE	POSITION	UNUSED ELEMENTS	+12V PIN	+5V PIN	GND PIN(S)
7404	1B,4B,2D	2D1	–	14	7
7427	4C	–	–	14	7
7438	2A,3A,4A	–	–	14	7
74L85	1A	–	–	16	8
75462	2E	–	–	8	4
16270-1	4D	–	–	10	3,12
16271-0	2C	–	–	1	21
16276-01	3E	–	18	11	5
LM339	1D	–	–	3	12
ULN-2074B	1C	1C1	–	–	4,5,12,13

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C32	C30
CR17	–
L3	–
Q1	–
R70	R58,47,47,59,69
TP27	TP3,4,9,13-15,17-24

NOTES

UNLESS OTHERWISE SPECIFIED:

1. ALL CAPACITORS ARE IN MICROFARADS, 50V.
2. ALL DIODES ARE IN4148.
3. ALL INDUCTORS ARE IN MICROHENRYS, 10%.
4. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
5. CONNECTOR REFERENCE SYMBOL: ✳-J1, 2-J2, 3-J3, 5-J5, 6-J6.
6. -□-□- INDICATES CUT-TRACE OPTION.
7. -□ □- INDICATES JUMPER OPTION.
8. ▭ SHORTING PLUG INSTALLED.

USED ON ASSEMBLY
25136-0

MUST CONFORM TO ENGINEERING S/EC. ES 30000-0		EC HISTORY		SHUGART ASSOCIATES	
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.	TITLE SCHEMATIC DIAGRAM PCB	
	LINEAR .XX ±.XXX			DETAIL SH	5-79 RELEASED FOR ASSEMBLY
CASE DEPTH				DESIGN FORMENKO	4-78
HARDNESS	ANGULAR ±			APPRO	SHEET 1 OF 2
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX			D	SCALE – DOC CODE SC PART NO. 25135-0 REV/EC 1062

25135-0

PART NO. 25135-0

-WRITE DATA
+WRITE PROTECT (SH1)
-WRITE GATE
-DRIVE SELECT 1
-DRIVE SELECT 2
-DRIVE SELECT 3
-DRIVE SELECT 4
-HEAD LOAD (JUMPER-OPTIONABLE I/O)
-DOOR CLOSED
-IN USE (JUMPER-OPTIONABLE I/O)
READ/WRITE 1
READ/WRITE 2

T5 R25 150,1/2W +5V
R1 1.8K,1/2W
R2 1.8K,1/2W
R3 1.8K,1/2W
CR1
ERASE
CENTER TAP
CR9 +24V
R14 1.5K Q1 2N2222A
R9 4.7K
R10 4.7K
R49 4.7K
R44 4.7K
R7 10K 1/8W,1%
C31 150pf 5%
WR DATA
WR GATE
SIDE ZERO
VREF
WR/CHNL
IREF
+I2 SEL
R/W1
R/W2
ERD
CTO
ER1
CT1
VBB
-STEP ENABLE
+OUTPUT ENABLE
+DRIVE SEL INT
+MOTOR ENABLE
SH1
T6 R26 150,1/2W +5V
T2 R22 150,1/2W +5V
DS1 DS2 DS3 DS4 DDS
WP NP
T1 R70 150,1/2W +5V
R54 150 1/2W
R53 100,1/2W +5V
DS HL
TP11
L7 -HEAD LOAD SOLENOID
R10 +HEAD LOAD SOLENOID
CR10 IN4003 +24V
R46 75 1/2W +5V
+IN USE LED
-DOOR CLOSED
R12 4.7K +5V
TP16
+READ DATA
CUSTOMER INSTALLED OPTION
1A
D1 D2 D4
R8 4.7K +5V
R4 470K +24V
R6 11K R5 11K
R16 4.7K
CR3 CR2 CR17 CR6 CR5
R15 15K
CR4 CR7
R17 24K R13 24K
R18 1.5K R19 1.5K
C10 .022 10%
R27 47
C28 4.7, 20%
C29 0.1 +80 -20%
CR8 IN5242B 12V
R20 1.5K L1 330 R28 1.5K
C7 150pf 5%
R21 1.5K L2 330 R29 1.5K
TP2 TP1
C13 0.1 +80-20%
C15 27pf 5%
C14 0.1 +80-20%
C6 0.1 +80-20%
R35 12K R36 2K
C11 150pf 5%
C12 150pf 5%
3E
DIFF IN
DIFF IN
OS1
OS1
OS2
OS2
BB
DIFF COMP
DIFF COMP
DATA OUT
RD AMP
L3 62 R37 270 C19 680pf 5%
R39 15K
R43 50K, 3/4W
R41 10K

USED ON ASSEMBLY
25136-0

MUST CONFORM TO ENGINEERING SPEC ES 30000-0			EC HISTORY		SHUGART ASSOCIATES
MATERIAL		TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.	TITLE SCHEMATIC DIAGRAM PCB SA 5EC 061
		LINEAR ±.XX			DETAIL SH 5-79 RELEASED FOR ASSEMBLY
CASE DEPTH		±.XXX			DESIGN [illegible] 4-78 T25135
HARDNESS		ANGULAR=			APPRO SHEET 2 OF
SURFACE TREATMENT	ES	CORNERS EDGES BROKEN OUTSIDE MAX / INSIDE MAX			D SCALE — DOC CODE SC PART NO. 25135-0 REV/EC 1062

25135-0

PART NO 25100-2

- TRACK ZERO
- DRV SEL INT XS800
+ WRITE PROTECT
+ DRV SEL INT XS800
- DOOR CLOSED XS800
- POR XS800
+ INDEX/SECTOR
+ READ/WRITE (1) XS800
+ READ/WRITE (2) XS800
- READ GATE XS800

+ TRACK ZERO XS800
- DISK CHANGE
+ WRITE PROTECT XS800
- WRITE PROT
+ PULL UP XS800
- READY
- INDEX
- SECTOR
- READ DATA
- SEP DATA
- SEP CLOCK
+ WRITE PROT LED
+ TRK 00 LED
+ INDEX LED

SECTOR SEPERATOR
USED ON ASSEMBLY
25106
25107

DATA SEPERATOR
USED ON ASSEMBLY
25104
25105
25106
25107

XS801

MUST CONFORM TO ENGINEERING SPEC ES XXXXII		EC HISTORY	SHUGART ASSOCIATES
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE NO	TITLE SCHEMATIC DIAGRAM DISKETTE, 800 SERIES
CASE HEIGHT	LINEAR .XX .XXX	DETAIL A.L. 5-75	RELEASED FOR ASSEMBLY
HARDNESS	ANGULAR	DESIGN	T25100
SURFACE TREATMENT	MIN MAX OUTSIDE MIN MAX	APPRO K.A.S. 5-75	SHEET 2 OF 2
		D SCALE ~	XXX-XXX SC PART NO 25100-2 REV EC 5C2

PART NO 25100-2

— WRITE DATA
+ WRITE PROT XS801
— WRITE GATE
+ PULL UP XS801
— DRIVE SELECT 1
2
3
4
+ TRACK ZERO XS801
— HEAD LOAD (JUMPER OPTIONABLE I/O)
— DOOR CLOSED
— IN USE (JUMPER OPTIONABLE I/O)
+ 24V
+ 24V RETURN
+ 5V
GROUND
— 5V OR -7V TO -16V
— STEP
+ DIRECTION SELECT

CUSTOMER INSTALLED OPTION

ALL ODD NUMBERED PINS

R37, 4.02K 1/8W, 1%
R38 422 1/8W 1%
R41 422 1/8W 1%
R42 1.1K 1/8W 1%
R40 422 1/8W 1%
R39, 4.02K 1/8W, 1%
R47, 274 1/8W, 1%
R46 909 1/8W 1%
R45 75 1/8W 1%
R43 20K
R44 20K
R33 390
R34 3K
R35 390
R36 510
R23 100, 1/2W
R24 47K
R25 5.1K
R74 5.1K
R29 75, 1/2W
R7 510
R8 390
R10 510
R9 390
R11 510
R12 390
R1 51 1/2W
R2 51 1/2W
R3 51 1/2W
R4 510
R5 510
R6 510

C1 4.7 10%
C2 4.7 10%
C3 .1
C4,29-36 .1
C5 4.7 10%
C8 1.0, 35V, 10%
C9 510PF 500V 5%
C12 1.0 10%
C13 4.7 10%
C14,25 .1
C15,27 .1
C37 .015 10%

CR1 IN4003
CR2 IN4003
CR3 IN4003
CR4 IN4003
CR6
CR7
CR8
CR9

Q1 2N4231
Q2 2N4231
Q3 2N4231
Q4
Q5
Q6
Q7 2N2222A
Q8 2N2222A

VR1 79M05

L1
L2
L3
L4
L5

TP5,6,7
TP11
TP27

+24VA
+24V RTN
+5VT
+5VA
-5VA
-5VT

+ READ/WRITE (1)
XS801
XS801
+ READ/WRITE (2)
+ ERASE DRV (3)
— READ GATE XS801
— DRV SEL 1 XS801
— TRACK 00
+ DRV SEL 1 XS801
— HEAD LOAD
— DOOR CLOSED XS801
+ IN USE LED
— POR XS801
Ø1
Ø2
Ø3

DS
DDS
HL

NOTES, UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V, +80, -20%.
3. ALL INDUCTORS ARE 100MH, 10%.
4. ALL DIODES ARE IN4148.
5. ALL TRANSISTORS ARE 2N2907A.
6. -O-O- INDICATES CUT-TRACE OPTION.
7. -O O- INDICATES JUMPER OPTION.
8. CONNECTOR SYMBOL REFERENCES; (X)=J1, (V)=J2, (3)=J3, (5)=J5, (W)=J6.
9. I.C. LOCATION 4B IS A RESISTOR PACK, 150Ω, 1/2W, 5%.
10. I.C. LOCATION 3B IS A RESISTOR PACK, 2K, 1/4W, 5%.
11. ADD JUMPER L FOR -7V TO 16V ON ASSEMBLIES; 25103, 25105, 25107.
12. PINS 8 AND 9 OF 1G ARE GROUND.
13. SHORTING PLUG INSTALLED.
14. REMOVE JUMPER FROM 800 AND INSTALL IN 801.

REFERENCE DESIGNATION

LAST USED	NOT USED
C40	C28 (RESERVED)
CR14	CR10
L9	
Q8	
R74	R48
TP27	TP8,9,10,14,15,17-20,22,23
VR1	

TYPE	POSITION	UNUSED ELEMENTS	VCC PIN	GND PIN
7400	5C,2E,5F	2E1,4,5F2,4	14	7
7402	4E	4E3		
7404	3E			
7405	4D	4D2,3		
7407	4G			
7410	5B,2C	5B1		
7438	3C,4C			
7474	2D,3D,5D,4F			
7476	3F		5	13
7486	2G	2G4	14	7

TYPE	POSITION	UNUSED ELEMENTS	VCC PIN	GND PIN
74LS5	2B		16	8
75452P	1F		8	4
8T20	6C		~	8
9602	5A,5E,3G		16	8
LM339	1G	1G3	3	12
NE592A	6E		~	~
2QT2222	6G		~	~
2QT2905	5G		~	~
7428	2F		4	7
7427	2A	2A1,2	14	7

USED ON ASSEMBLY
25102-4
25103-4
25104-4
25105-4
25106-4
25107-4

MUST CONFORM TO ENGINEERING SPEC ES 30000 Ø
MATERIAL
TOLERANCE UNLESS OTHERWISE NOTED
LINEAR .XX .XXX
ANGULAR
CASE DEPTH
HARDNESS
SURFACE TREATMENT ES
BREAK ALL SHARP EDGES OUTSIDE MAX INSIDE MAX

EC HISTORY

DATE	NO
10-76	0591
1-76	0702
DETAIL A.L. 3-79	RELEASED FOR ASSEMBLY
DESIGN	
APPRO	

SHUGART ASSOCIATES

TITLE SCHEMATIC DIAGRAM DISKETTE, 800 SERIES
T25100
SHEET 1 OF 2
SCALE ~ DOC CODE SC PART NO 25100- REV EC 0702

X5800

Shugart Associates
435 Oakmead Parkway, Sunnyvale, California 94086
Phone: (408) 733-0100 TWX: 910 339 9355 SHUGART SUVL

50575-4 2/78

PRINTED IN U.S.A.

July 2, 1979

TO: SHUGART SA800 CUSTOMERS

FROM: Bill Klevesahl

SUBJECT: SA800 LSI PCB

Shugart will be delivering a new PCB in the 1Q80, that incorporates three custom LSI chips. The read and write chips are produced by Motorola, the third chip is the controller and is manufactured by AMI.

The differences between the present PCB and the new one are listed below.

1. Interface

   a) The LSI PCB is completely interchangeable with the current board. The interface is identical at each connector.

   b) The LSI PCB does not use the -5V/-15V pins at J5. The pin at J5 is not terminated to anything.

2. Optional Features

   a) All functions available on the fully loaded 801 are on the LSI PCB.

   b) An add-trace option "NFO" prevents the head from being forced out past tract Ø.

   c) An add-trace option "TS" enables true FM data separation, maintaining synchronization during address marks.

3. Test Points

   a) Most test points are retained:

      1,2 Amplified read signal
      5,6,7 Ground
      10 Index
      11 + Head Load
      12 Index/Sector Pulses
      16 + Read Data
      25 + Write Protect
      26 + Detect Track Ø
      27 + Step Pulse (No longer gated with read gate)

Test Points, Continued:

b) Test Points Not Needed

3,4 Differentiated read signal (buried inside read chip)
21,24-Data separator timing (no pot alignment is necessary)

c) Test Points Added

8 + Data Window (for troubleshooting FM data separation)

d) The door lock option terminal pin "DL" is available to check voltage on the +5V bus.

e) No adjustment of the sector separator or data separator is necessary.

Enclosed you will find a circuit diagram and a component overlay to help you understand the PCB.

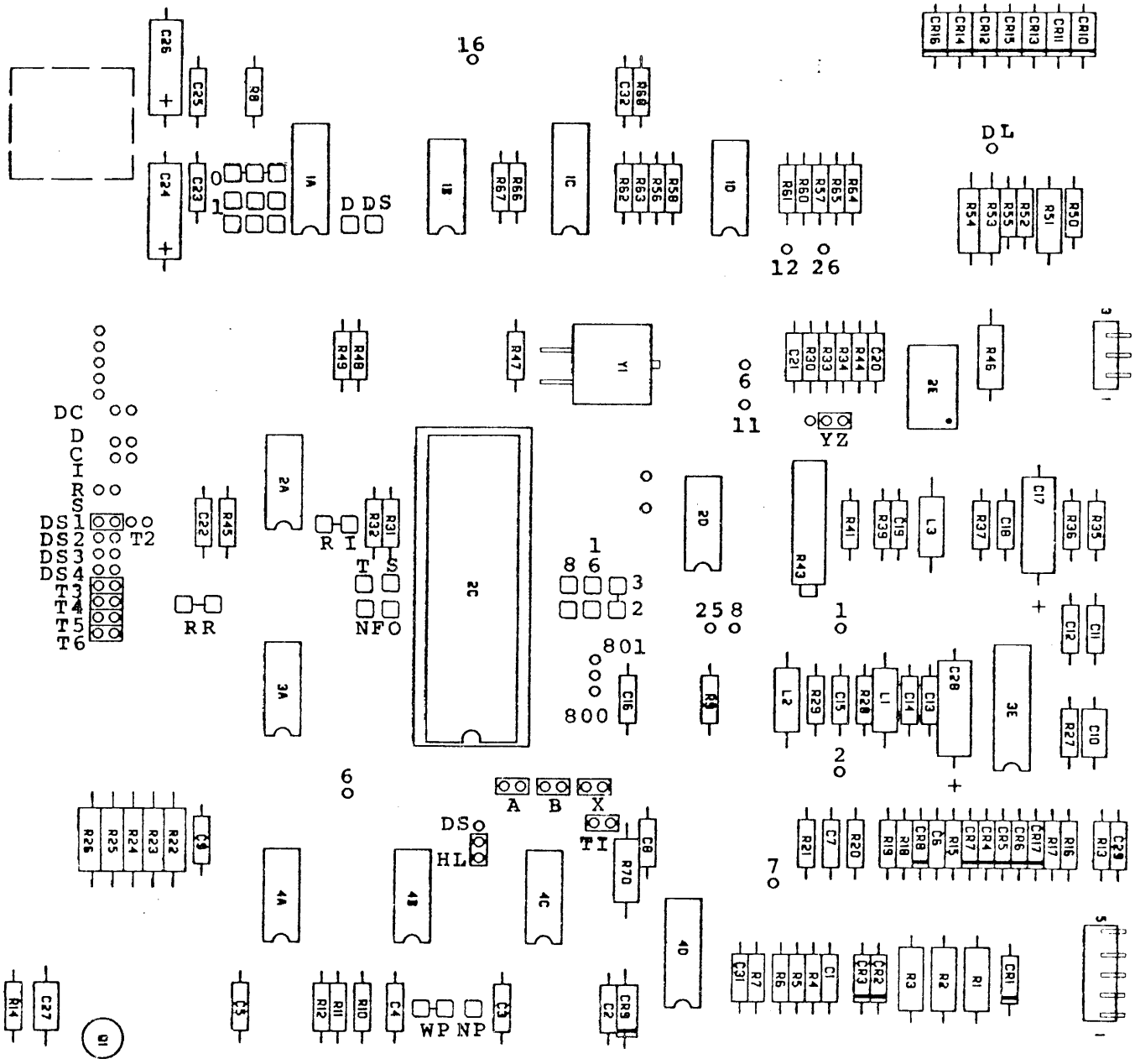
All the SA800 Series drives will be shipped in a SA801 configuration, to change to a 800-1 or -2 simply move the jumper from position 801 to 800 on the PCB.

Since we are delivering the new PCB in the 1Q80, I would appreciate feedback on the evaluation units at your earliest convenience. If there are any questions or problems regarding the PCB, feel free to contact me.

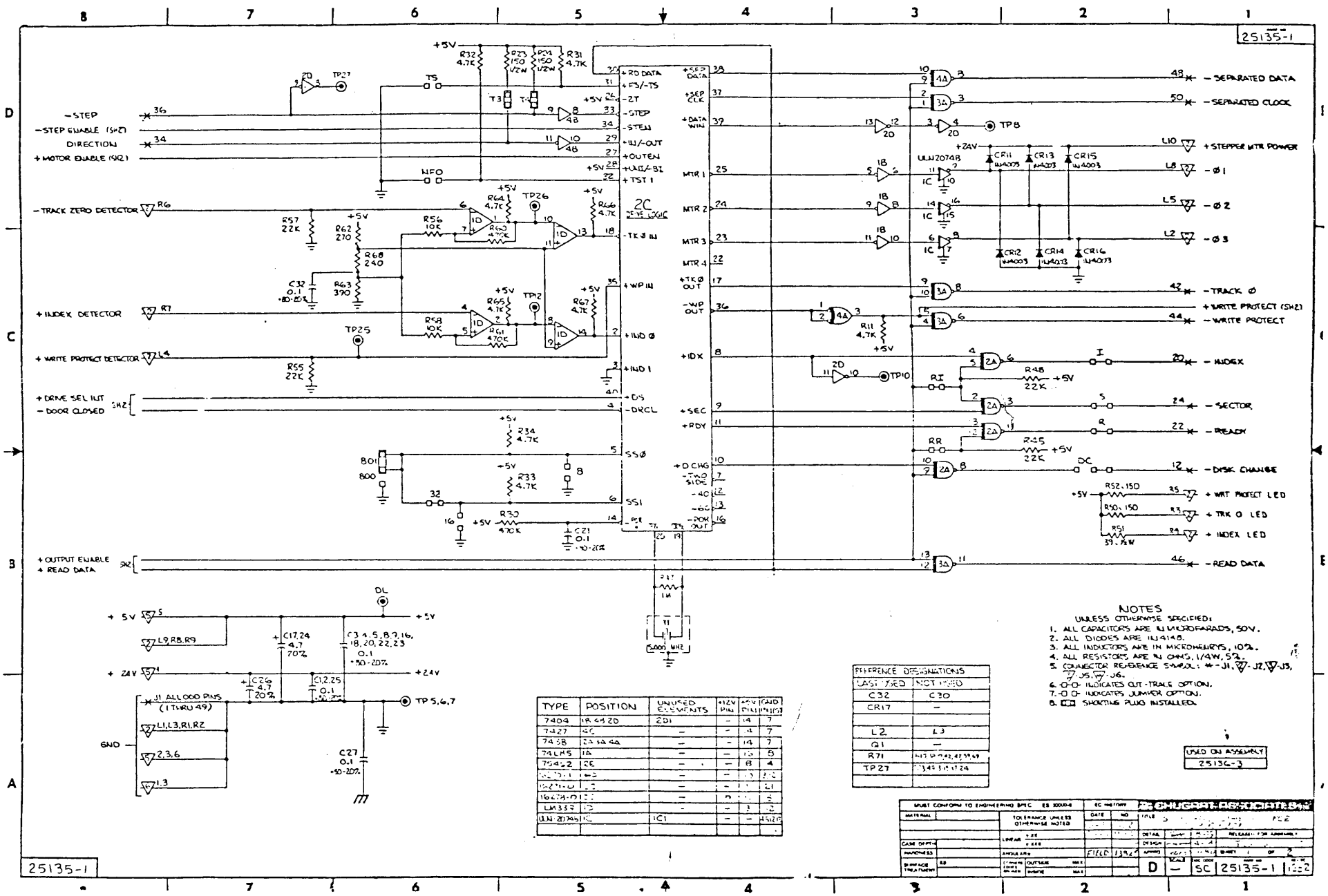
Bill Klevesahl

Bill Klevesahl

REDUCE TO 7.000 ± .005



TITLE: PCB ARTWORK. 800/801			FILM LAYER: ASM OVERLAY LAYER 3 OF 5		
CODE	PART NUMBER	DASH	EC. REV	SCALE	S.C.
AM	25135	0	1062	2:1	



TYPE	POSITION	UNUSED ELEMENTS	+12V PIN	+5V PIN	GND PIN
7404	1A 4A 2D	2D1	-	14	7
7427	4C	-	-	4	7
7438	2A 3A 4A	-	-	14	7
74LS5	1A	-	-	10	5
7542	2C	-	-	8	4
[illegible]	[illegible]	-	-	[illegible]	[illegible]
[illegible]	[illegible]	-	-	[illegible]	[illegible]
1624-0	[illegible]	-	-	[illegible]	[illegible]
1624-01	[illegible]	-	-	[illegible]	[illegible]
LM339	1C	-	-	3	12
ULN-2074B	1C	1C1	-	-	4&12

REFERENCE DESIGNATIONS	
USED	NOT USED
C32	C30
CR17	-
L2	L3
Q1	-
R71	[illegible]
TP27	[illegible]

FIGURE 6-3. SCHEMATIC DIAGRAM, P/N 25136 (SHEET 1 OF 2)

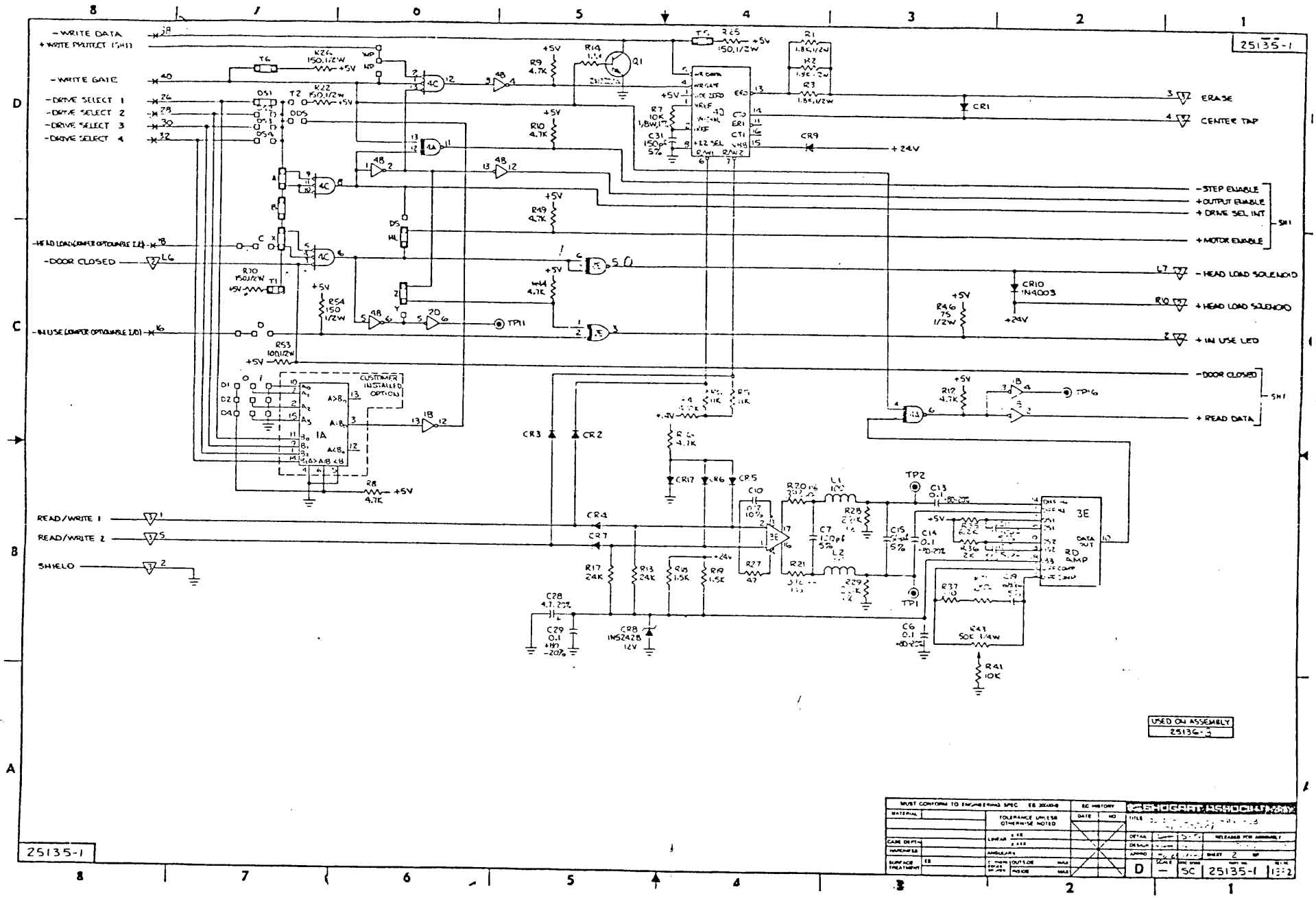


FIGURE 6-3. SCHEMATIC DIAGRAM, P/N 25136 (SHEET 2 OF 2)

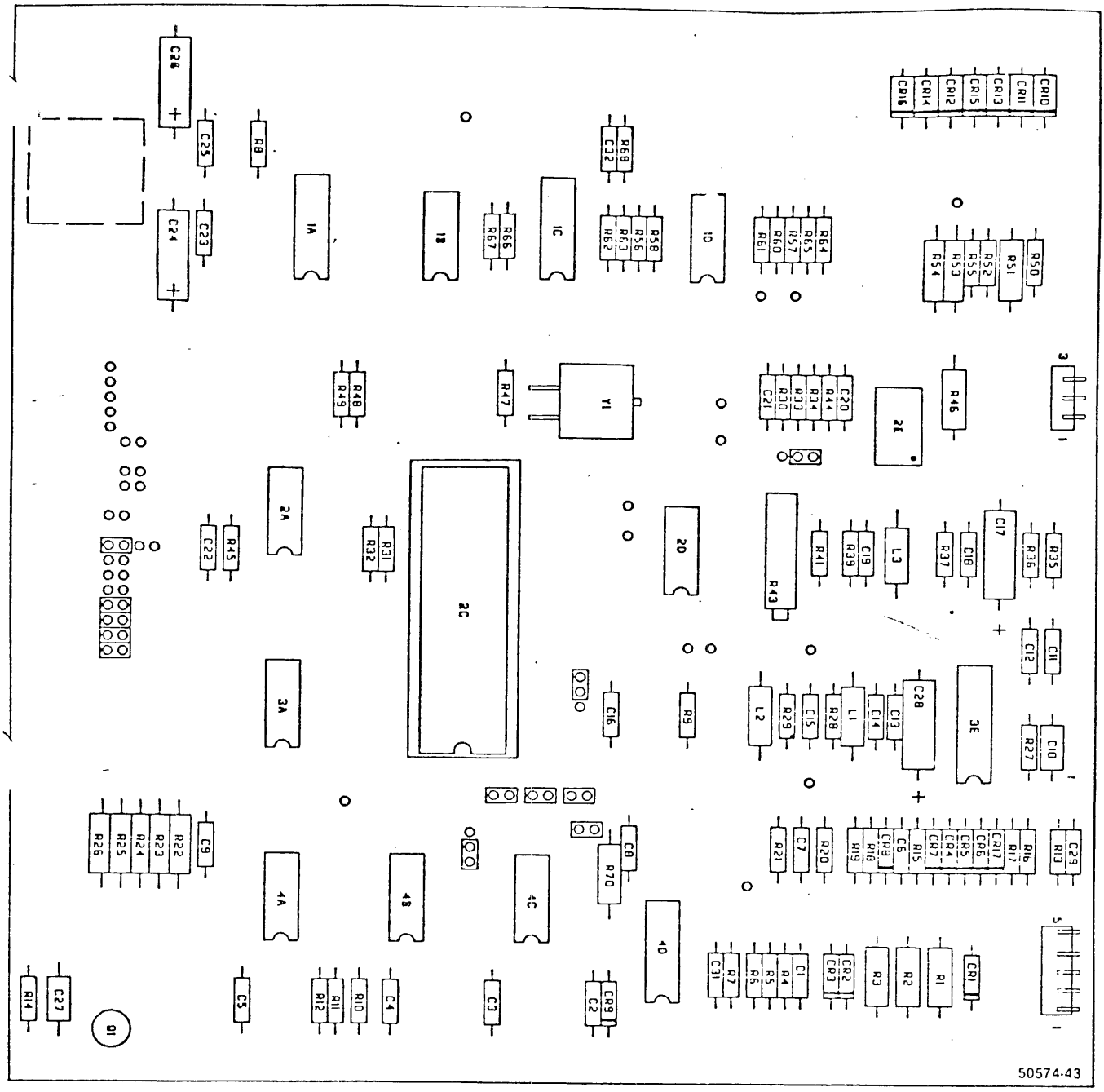


FIGURE 7-7. PCB COMPONENT LOCATIONS P/N 25136

SA800/801

Illustrated Parts Catalog

Shugart Associates®

SA800/801

Illustrated Parts Catalog

TABLE OF CONTENTS

DESCRIPTION

General

The Illustrated Parts Catalog is arranged so that the figures will always precede the parts listings and when possible be on the opposite page.

The first number in the list will always refer to the figure and the second number to the reference number of the part within the figure.

When an assembly is referred to within a figure and a further breakdown is shown on another figure then the reference figure will be called out.

Indented Level

The parts list is indented to show the levels of assembly within a figure. The major assembly will always be level 1, all parts or assemblies that attach to that assembly will be level 2 and assemblies within level 2 will have their attaching parts level 3 and so on.

Quantity Per Assembly

The quantity listed is the quantity used on the major assembly. Major Assemblies will never have a quantity listed.

Numerical Index

The numerical index lists all parts in part number sequence and is cross referenced to the figure and reference number.

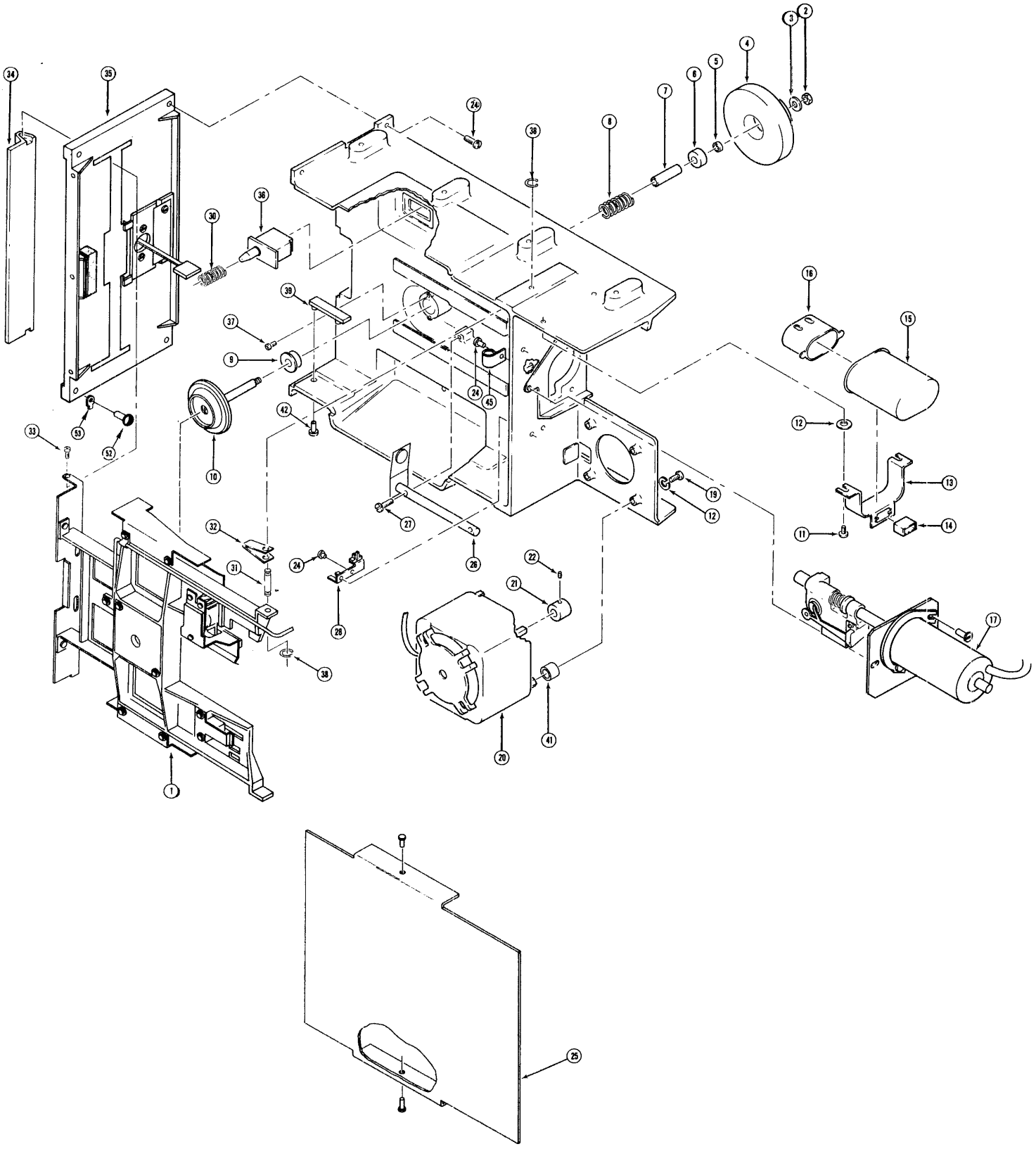


Figure 1 (1 of 2)

FIGURE & REF. NUMBER	PART NUMBER	DESCRIPTION 1 2 3 4	QTY PER ASM.
1		DRIVE ASSEMBLY SA800/801	
-1	50550	. CARTRIDGE GUIDE ASSEMBLY (SEE FIG. 3)	1
-2	10025	. NUT, 8-32	1
-3	12509	. WASHER, SPRING	2
-4	50016	. PULLEY ASSEMBLY, SPINDLE	1
-5	50019	. SPACER, SPINDLE-SHORT	1
-6	10800	. BEARING, SPINDLE	1
-7	50018	. SPACER, SPINDLE--LONG	1
-8	50166	. SPRING, SPINDLE	1
-9	10801	. FLANGED BEARING, SPINDLE	1
-10	50561	. HUB ASSEMBLY, SPINDLE	1
-11	12015	. SCREW, 8-32x.312	5
-12	12500	. WASHER; LOCK # 8	2
-13	50098	. BRACKET	1
-14	10150	. HOUSING, 3 PIN CONNECTOR	1
-15	10095	. CAPACITOR, 110 V 50/60 HZ (BODINE MTR ONLY)	1
	15004	. CAPACITOR, 220 V 50/60 HZ OR 110V ORIENTAL MTR	
-16	10148	. RUBBER BOOT	1
-17		. STEPPER/CARRIAGE ASSEMBLY (SEE FIG. 2)	1
-19	12028	. SCREW, 8-32x.750	4
-20	50443	. MOTOR, 110 VOLT 50/60 HZ KIT	1
	50301	. MOTOR, 208/230/220 VOLT 50/60 HZ	
-21	50358	. PULLEY, 60 HZ	1
	50357	. PULLEY, 50 HZ	
-22	11904	. SCREW, SET 6-32x.125	1
-23	10378	. CABLE CLAMP, 1/8 INCH	1
-24	12013	. SCREW 6-32x.312 (12014 FOR ZINC FACEPLATE)	11
	10191	. SCREW 6-32x.438 –800R	2
-25	50440	. DUST COVER KIT (OPTIONAL)	1
	12023	. . SCREW, THD. FORM, PAN HD.	2
	50009	. . COVER	1
-26	50522	. SPRING/GUIDE ASM	1
-27	12012	. SCREW, 4-40x.375	2
-28	50121	. DETECTOR ASSEMBLY, TRACK 0	1
-30	50582	. SPRING ASSEMBLY, DOOR OPEN (STANDARD)	1
	50583	. SPRING ASSEMBLY, DOOR OPEN (HORZ. MNT, PCB DOWN)	
-31	50167	. PIVOT TOP	1
	50670	. PIVOT TOP (STANDARD) (800R)	
-32	50168	. SPRING, BIAS	1
-33	11905	. SCREW, B.V.	2
-34	50142	. HANDLE	1
-35		. FRONT PLATE ASSEMBLY (SEE FIG. 4)	1
-36	17200	. SWITCH, DOOR OPEN	1
-37	12011	. SCREW, 4-40x.250	2
-38	11305	. CLIP	2
-39	50559	. DEFLECTOR	2
-41	50602	. SPACER	4
-42	12032	. SCREW, # 8x.50 LG TAPPING	2

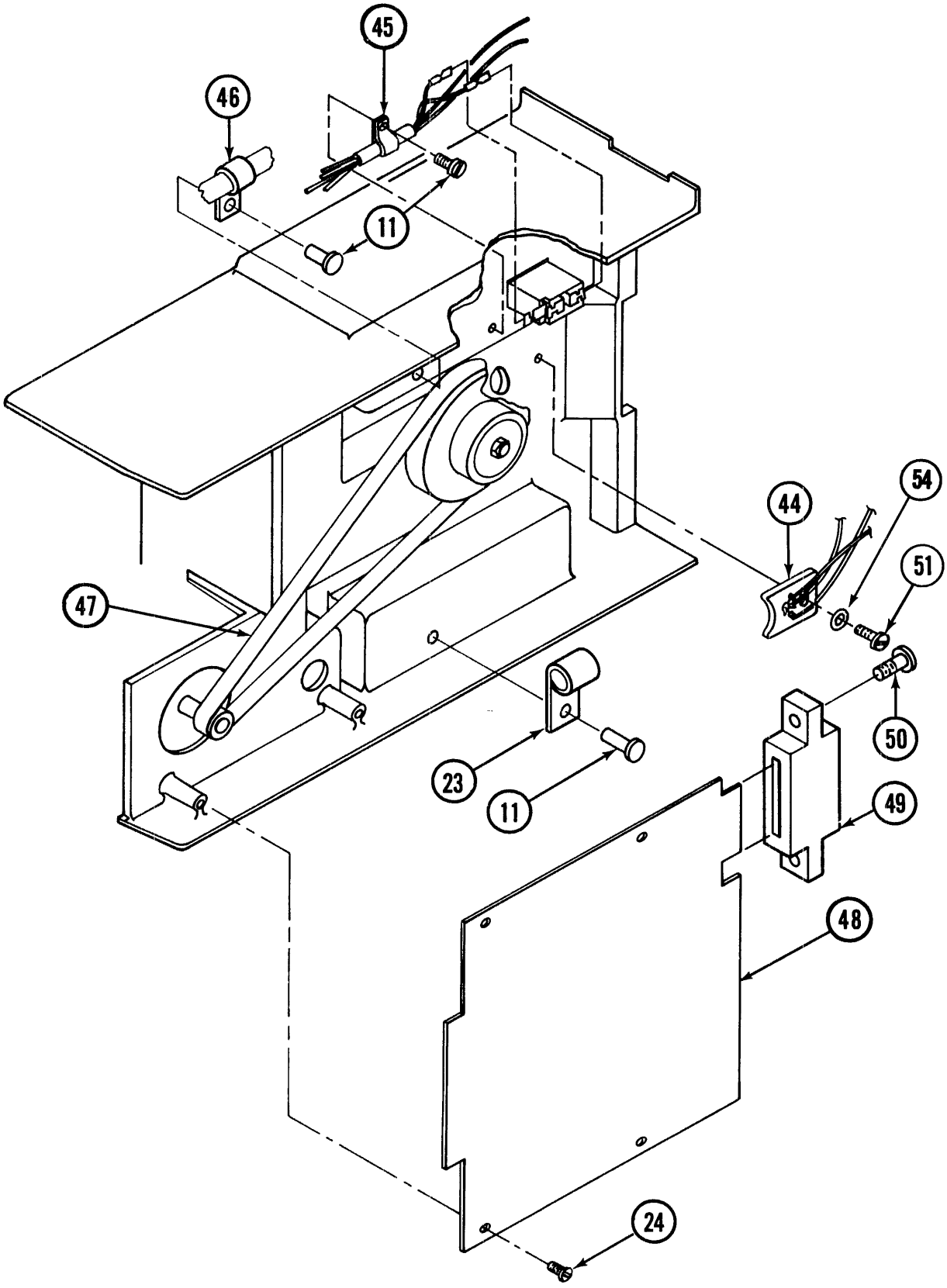


Figure 1 (2 of 2)

FIGURE & REF. NUMBER	PART NUMBER	DESCRIPTION 1 2 3 4	QTY PER ASM.
-44	50128	. PHOTRANSISTOR AND CABLE ASSEMBLY	1
-45	10375	. CABLE CLAMP, 3/16"	2
-46	10264	. CABLE CLAMP, 3/8"	1
-47	50356	. BELT (60 HZ)	1
	50355	. BELT (50 HZ)	1
-48	25102	. PCB (SA 800, -5V, NO DATA SEP)	1
	25103	. PCB (SA 800, -12/-15V, NO DATA SEP)	
	25104	. PCB (SA 800, -5V, WITH DATA SEP)	
	25105	. PCB (SA 800, -12/-15V, WITH DATA SEP)	
	25106	. PCB (SA 801, -5V)	
	25107	. PCB (SA 801, -12/-15V)	
-49	10140	. BLOCK, PCB CONN	1
-50	10174	. .SCREW, 4-40	2
-51	12036	. SCREW, 8-32x.375	1
-52	10187	. SCREW, 6-32x.250 -800R	2
-53	50669	. CLIP, FACE PLATE MOUNT–800R	2
-54	10014	. WASHER	1

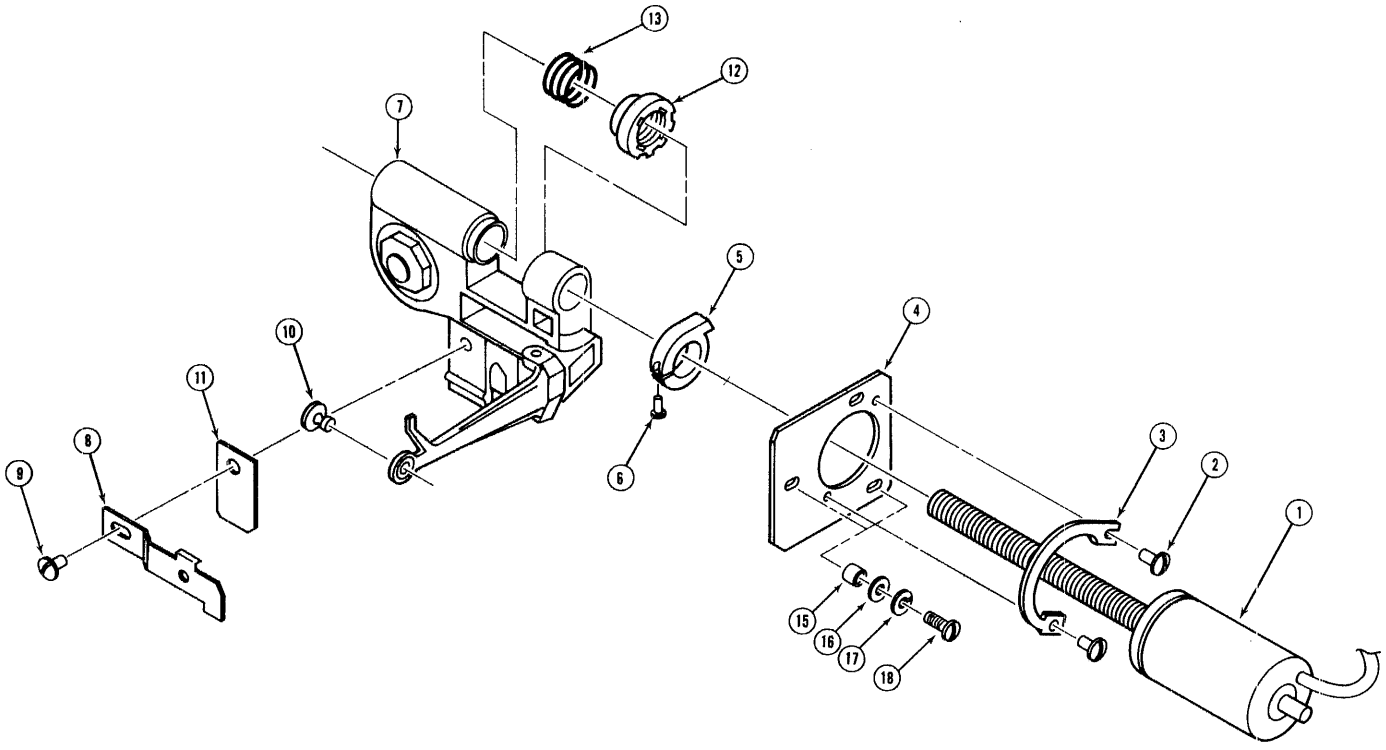


Figure 2

FIGURE & REF. NUMBER	PART NUMBER	DESCRIPTION 1 2 3 4	QTY PER ASM.
2-		STEPPER/CARRIAGE ASSEMBLY	
-1	50130	. STEPPER MOTOR ASSEMBLY	1
-2	12016	. SCREW, 8-32x.375	2
-3	50584	. MOUNTING CLAMP	1
-4	50112-4	. PLATE, STEPPER MOTOR	1
-5	50245	. STOP, LIMIT - LEAD SCREW	1
-6	11903	. SCREW, CAP 2-56x.250	1
-7	50562	. CARRIAGE ASSEMBLY	1
-8	50529	. . FLAG, TRACK 0	1
-9	11910	. . SCREW. 4-40x.250	1
-10	50542	. . LOAD BUTTON	1
-11	50362	. . SPRING, PLATE	1
-12	50087	. . NUT	1
-13	50088	. . SPRING, PRE-LOAD	1
-14	10012	. . WASHER	1
-15	50707	. SPACER	1
-16	10013	. WASHER, #6 FLAT	3
-17	12510	. WASHER, SPRING	3
-18	12027	. SCREW, 6-32x.500	3

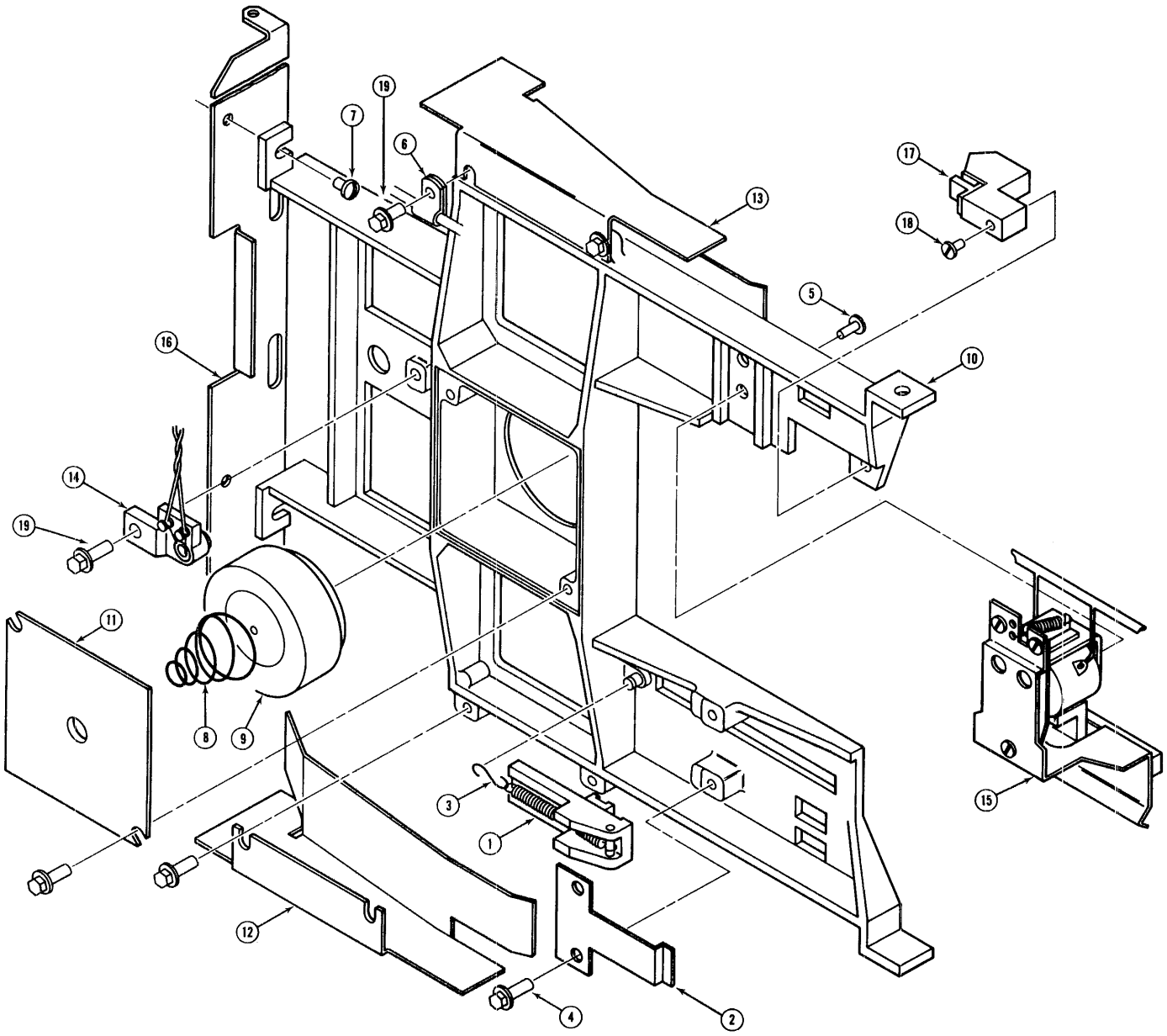


Figure 3

FIGURE & REF. NUMBER	PART NUMBER	DESCRIPTION 1 2 3 4	QTY PER ASM.
3-	50550	CARTRIDGE GUIDE ASSEMBLY	
1	50609	. EJECTOR ASSEMBLY	1
2	50555	. SPRING, CLAMP, EJECTOR	1
3	50556	. HOOK, SPRING	1
4	12015	. SCREW 8-32x.312	7
5	12013	. SCREW 6-32x.312	1
6	10378	. CLAMP, CABLE	1
7	10187	. SCREW 6-32x.250	2
8	50031	. SPRING, HUB CLAMP	1
9	50254	. HUB CLAMP ASSEMBLY	1
10	50544	. GUIDE	1
11	50546	. PLATE, HUB CLAMP	1
12	50547	. STRIPPER, BOTTOM	1
13	50548	. STRIPPER, TOP	1
14	50557	. L.E.D. ASSEMBLY	1
15	50558	. HEAD LOAD ACTUATOR ASSEMBLY	1
16	50579	. LATCH PLATE	1
17	50313	. WRITE PROTECT DETECTOR ASSEMBLY	1
18	12026	. SCREW 4-40x.625	1
19	12016	. SCREW 8-32x.375	2

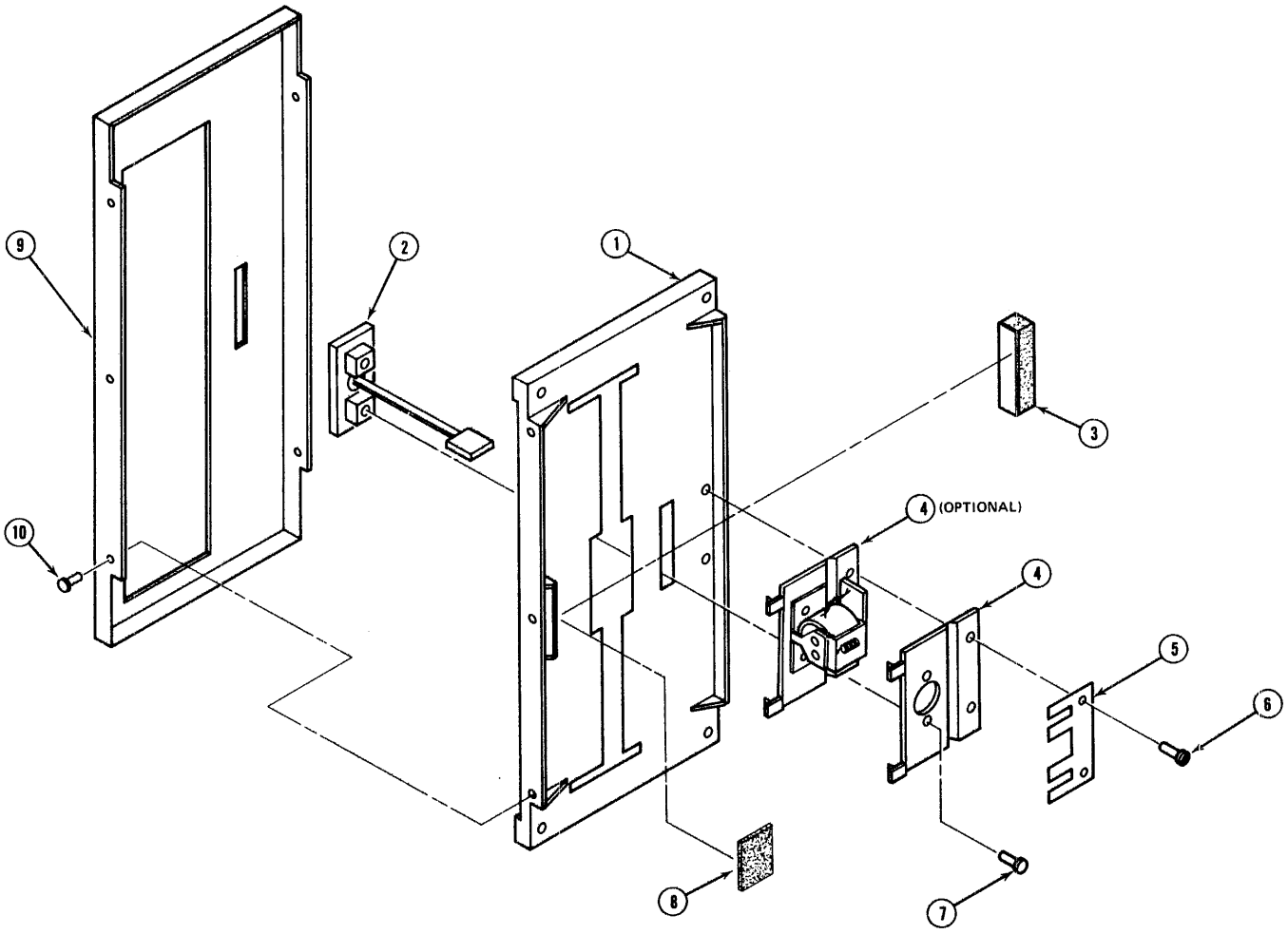


Figure 4

FIGURE & REF. NUMBER	PART NUMBER	DESCRIPTION 1 2 3 4	QTY PER ASM.
4-	50733	FRONT PLATE ASSEMBLY (WITH LITE)	
	50731	FRONT PLATE ASSEMBLY (WITHOUT LITE)	
	50735	FRONT PLATE ASM KIT (WITH DOOR LOCK)	
	50679	FRONT PLATE ASM–800R (WITHOUT LITE)	
	50680	FRONT PLATE ASM–800R (WITH LITE)	
	50724	FRONT PLATE ASM–800R (WITH DOOR LOCK)	
-1	50729	. FRONT PLATE	1
	50667	. FRONT PLATE–800R	1
-2	50727	. PUSH BUTTON (WITH LITE)	1
	50726	. PUSH BUTTON, DOOR LOCK OPTION	
	50728	. PUSH BUTTON (WITHOUT LITE)	1
-3	50183	. BUMPER	1
-4	50156	. LATCH	1
	50690	. LATCH ASM, DOOR LOCK OPTION	
-5	50691	. SPRING PLATE	1
-6	12013	. SCREW 6-32x.312	2
-7	12035	. SCREW 4-40x.250	2
-8	50580	. SNATCH	1
-9	50257	COVER, FRONT 5-1/4 x 11 WHITE	1
	50258	COVER, FRONT 5-1/4 x 11 TAN	1
	50260	COVER, FRONT 5-1/4 x 10 WHITE	1
	50261	COVER, FRONT 5-1/4 x 10 TAN	1
	50263	COVER, FRONT 4-5/8 x 10-1/2 WHITE	1
	50264	COVER, FRONT 4-5/8 x 10-1/2 TAN	1
	50675	COVER, FRONT–800R TAN	1
-10	10261	SCREW, FL. HD. 4-40x.250	5

PART NUMBER	FIG. REF.
10012	2-14
10013	2-16
10014	1-54
10025	1-2
10095	1-15
10140	1-49
10148	1-16
10150	1-14
10174	1-50
10187	3-7
	1-52
10191	1-24
10261	4-10
10264	1-46
10375	1-45
10378	1-23
	3-6
10800	1-6
10801	1-9
11305	1-38
11903	2-6
11904	1-22
11905	1-33
11910	2-9
12011	1-37
12012	1-27
12013	1-24
	3-5
	4-6
12015	1-11
	3-4
12016	
	2-2
	3-19
12023	1-25
12026	3-18
12027	2-18
12028	1-19
12032	1-42
12036	1-51
12500	1-12
12509	1-3
12510	2-17
15004	1-15
17200	1-36
25102	1-48
25103	1-48
25104	1-48
25105	1-48
25106	1-48
25107	1-48
50009	1-25
50016	1-4
50018	1-7
50019	1-5
50031	3-8

PART NUMBER	FIG. REF.
50087	2-12
50088	2-13
50098	1-18
50112-4	2-4
50121	1-28
50128	1-44
50130	2-1
50142	1-34
50156	4-4
50166	1-8
50167	1-31
50168	1-32
50183	4-3
50245	2-5
50254	3-9
50257	4-9
50258	4-9
50260	4-9
50261	4-9
50263	4-9
50264	4-9
50301	1-20
50313	3-17
50355	1-47
50356	1-47
50357	1-21
50358	1-21
50362	2-11
50440	1-25
50443	1-20
50522	1-26
50529	2-8
50542	2-10
50544	3-10
50546	3-11
50547	3-12
50548	3-13
50550	1-1
	3
50555	3-2
50556	3-3
50557	3-14
50558	3-15
50559	1-39
50561	1-10
50562	2-7
50579	3-16
50580	4-8
50582	1-30
50583	1-30
50584	2-3
50602	1-41
50609	3-1
50667	4-1
50669	1-53
50670	1-31

PART NUMBER	FIG. REF.
50675	4-9
50679	4
50680	4
50690	4-4
50691	4-5
50707	2-15
50724	4
50726	4-2
50727	4-2
50728	4-2
50729	4-1
50731	4
50733	4
50735	4

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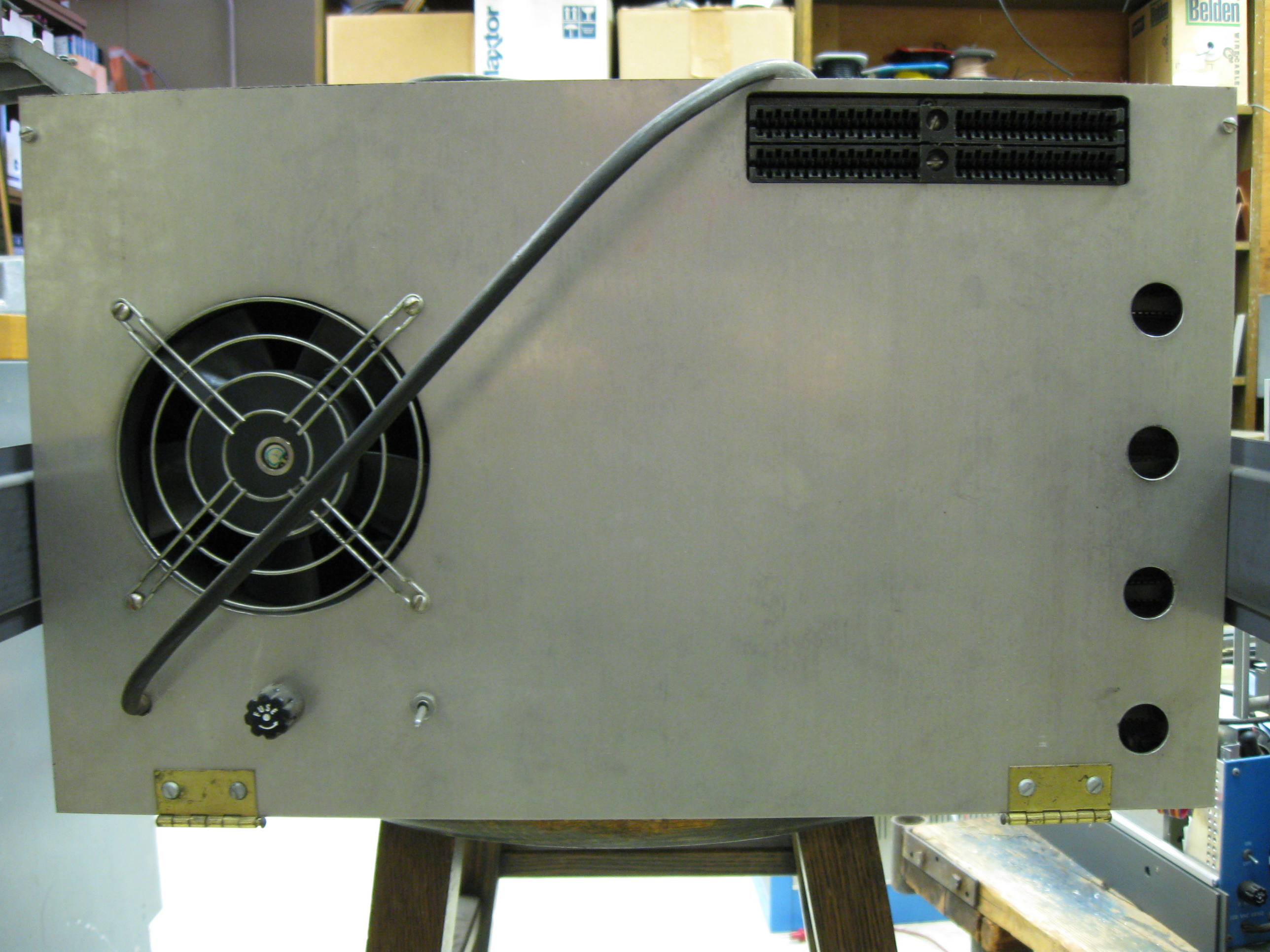
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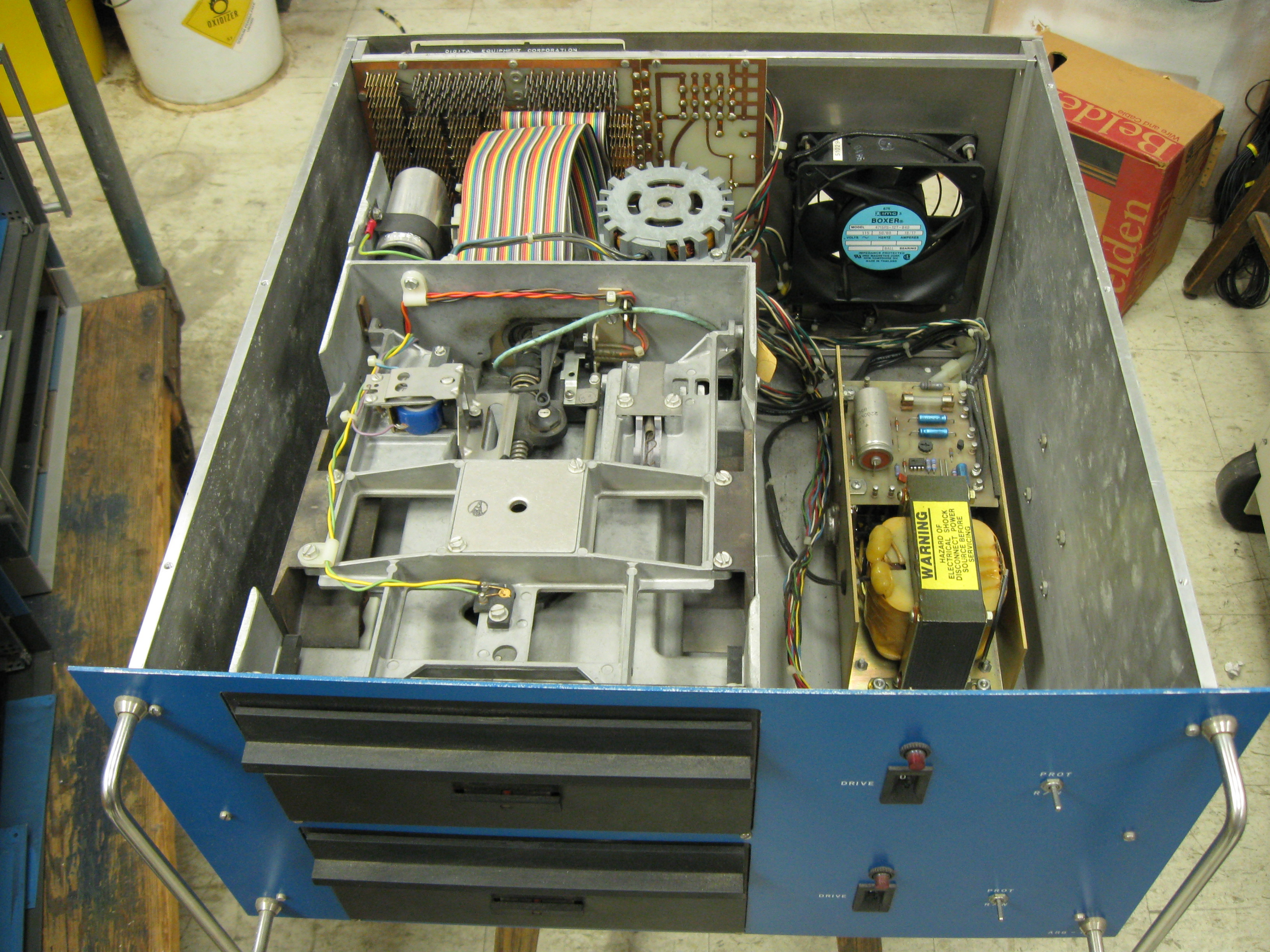
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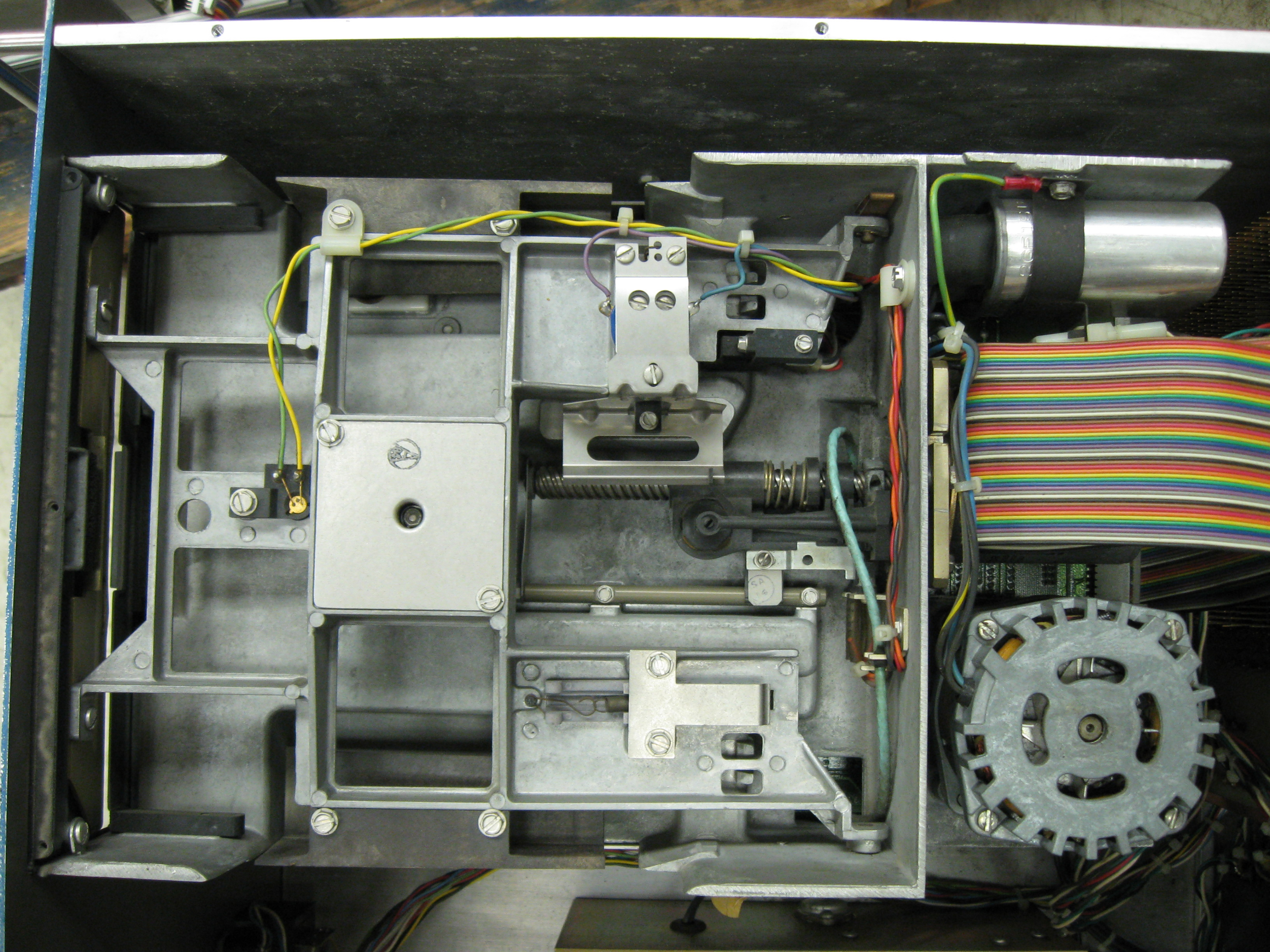

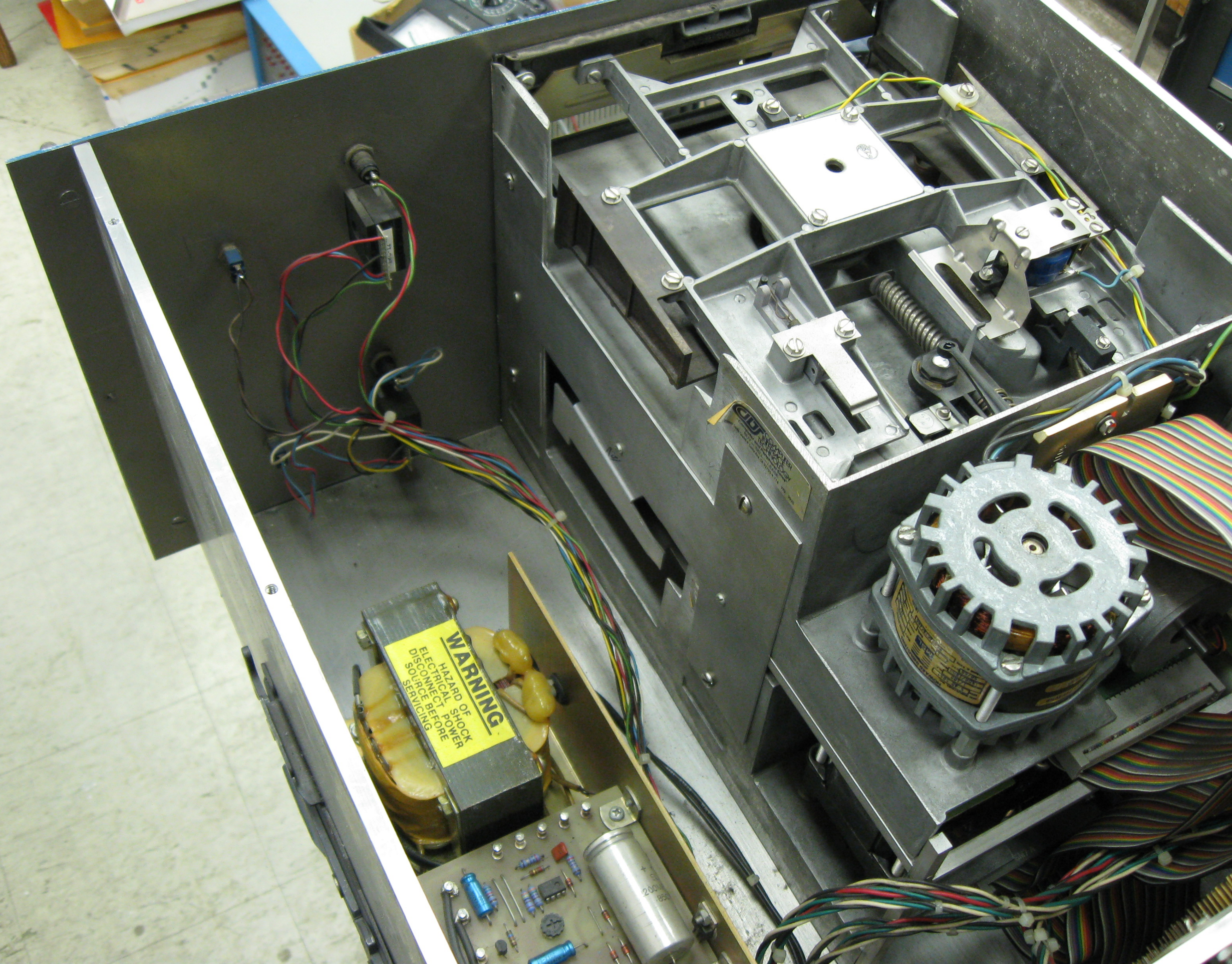
WARNING
HAZARD OF ELECTRICAL SHOCK
DISCONNECT POWER
SOURCE BEFORE
SERVICING