MODEL 1900

LSI-11 TO UNIBUS TRANSLATOR

INSTRUCTION MANUAL

addac corporation

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corporation

70 tower office park, woburn, ma. 01801 telephone (617) 935-6668 telex 949329

PRICE: $25.00

MODEL 1900

LSI-11 TO UNIBUS TRANSLATOR

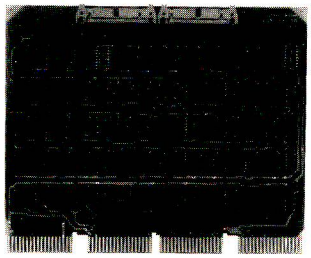
INSTRUCTION MANUAL

IM- 883
A2-10060, Rev. 9A

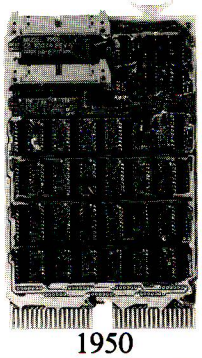
adac corporation

BUS INTERFACE CARDS

ADAC MODEL	COMPATIBLE WITH
1900	DEC UNIBUS
1950	ADAC 1000 & 2000 Systems DEC LSI-11, 11/2 & 11/23 Microcomputer Series



1900



1950

GENERAL DESCRIPTION

The Model 1900 is the first bus translator that allows Digital Equipment Corporation LSI-11 peripherals to operate with a Unibus CPU (any of the PDP-11 series). The Model 1900 can be inserted **directly** into the Unibus. It allows peripherals located on the expander side to be communicated with in the exact manner as if the peripherals were inserted directly in the CPU bus. Peripherals on either side of the translator can transfer data to and from peripherals on its own bus or through the translator to the other bus with no significant loss of speed. Furthermore, the expander bus can be located up to 40 feet from the CPU bus.

Peripherals on the expander side of the translator can be operated under program control, program interrupt or direct memory access.

In addition to 16 bits of data, a full addressing capability of 18 bits is supplied across the translator. All inputs are buffered through low current input receivers and all outputs are either high powered open collector drivers or tri-state outputs. All inputs and outputs are terminated in 120 ohm characteristic impedances.

The Model 1900 consists of a quad size board (8½″ × 10″) that can be plugged into the C-D-E-F positions of any of the four slots of a DEC DD11A system unit. Two 40 pin headers are mounted on the edge of the board away from the bus. Connection to the LSI-11 bus is made by means of two flat, high speed transmission cables. For connection to the ADAC System 1000 series, connectors are supplied to allow the cable to be plugged directly into its backplane. For connection to a PDP-11/03 or other LSI-11 backplanes, the cables are terminated on a half quad (8½″ × 5″) board that plugs into one slot.

The Model 1900 translator allows Unibus users to take full advantage of the substantially lower cost memories and peripherals that are available for the LSI-11 bus structure. It also allows all PDP-11 systems to operate with the ADAC System 1000 series of LSI-11 bus structured peripheral expanders. The System 1000 series can house up to 11 full quad or 22 half quad LSI-11 compatible peripherals in a 7″ high rack mounted enclosure. The LSI-11 structured backplane when used with the Model 1900 can contain any peripheral but cannot contain an LSI-11 CPU.

GENERAL DESCRIPTION

The Model 1950 bus repeater is designed for use with DEC LSI-11 compatible buses. It is used when it is necessary to employ a greater number of bus devices or longer cables than may be accommodated by the basic bus. This capability is especially useful in data acquisition and process control systems which, by their nature, must contain a large number of analog and digital channels.

The repeater circuitry is contained on a one-half quad size board (8½″ × 5″). The board may be configured by a single jumper for use either as the last card in the card cage containing the CPU or as the first card in the expansion cage. The best choice is usually to install the card as the last card in the CPU cage if long cables are to be run (greater than 15′). Several repeaters may be used in a system to daisy chain card cages together as long as total system delay does not cause a bus time out (approximately 10 microseconds).

In addition to the repeater card, the Model 1900 BC-XX cable set is supplied as the bus cables for carrying the bus signals from the repeater card. The XX digits specify the cable length up to 50 feet. If the Model 1000-BP card cage is used the cables connect directly to connectors supplied on the backplane. For use with other card cages the Model 1900 CT may be used to terminate the cables to the backplane. The 1900 CT is a half-quad card (8½″ × 5″) with two 40 pin cable connectors and provisions for termination networks for special applications.

Whenever cables are run in a bus system, careful attention must be paid to delays, signal skewing and degraded rise times as well as ringing. In the Model 1950 and associated support hardware careful attention is paid to the impedance of cables and terminators to reduce ringing. Timing problems are avoided by the introduction of additional delay (approximately 100 nanoseconds) to the bus control signals.

Cable delays are about 2 nanoseconds per foot and repeater delays are 5 nanoseconds for data and related signals and 150 nanoseconds for control signals. Total system delay, then, depends on the system configurations.

The repeater system is totally transparent from the programmer's point of view.

CABLE AND BUS TERMINATIONS

The Model 1900 is a quad size card that plugs directly into the Unibus. On the side of the board opposite the Unibus are mounted two 40 pin headers that carry the LSI bus signals and allow connection to the LSI bus by means of the Model 1900-B cable set. The 1900-BC cable set consists of two forty wire flat cables supplied in several configurations. All models have 40 pin strain relief connectors on both ends. The length and type of cable can vary. For 10′ and 15′ lengths the cable is supplied as 120 ohm flat ribbon cable. For 20′, 30′ and 40′ lengths, the cable is supplied as 120 ohm flat twisted pair, with an individual ground wire twisted with each signal wire.

If the Model 1900 is operated with the ADAC System 1000 Series, the strain relieved connector can plug directly into headers provided on its backplane. If the Model 1900 is to be used with the DEC LSI-11 backplane, or equivalent, the strain relieved connector can plug into the ADAC Model 1900-CT cable terminator. The Model 1900-CT is a ½ quad board (8½″ × 5″) that plugs directly into an LSI-11 configured backplane. The edge of the board opposite the bus contains two 40 pin headers in order to be able to accept the 1900-BC cable set.

SPECIFICATIONS
MODEL 1900
LSI-11 TO UNIBUS TRANSLATOR

Function	Provides translation of all Unibus signals into LSI-11 bus signals (and vice versa) to allow LSI-11 peripherals to function directly with any PDP-11 Unibus computer.
Point of Insertion	Unit is plugged directly into Unibus.
Method of Connection to PDP-11/03	Connects to LSI-11 bus via Model 1900-BC bus Cable and Model 1900-CT Cable Terminator.
Method of Connection to ADAC System 1000	Connects to bus of System 1000 Series via Model 1900-BC Bus Cable which plugs directly into backplane.
Unibus Loading	One bus load.
LSI-11 Drive Capability	15 bus loads on LSI-11 bus plus 120 ohm terminator on each line, mounted on Model 1900.
Module Types-LSI Side	All standard modules designed to interface to LSI-11 bus, except LSI-11 CPU. This includes A/D, D/A, memory, floppy disc controllers, etc.
Communication Methods with LSI Peripherals	Program control, program interrupt and direct memory access.
Interfacing Technique	Completely asynchronous, interlocking handshake interface between Unibus and LSI-11 bus.
Effects on Unibus Programming	None. All PDP-11 instructions can operate across the interface. Operation is transparent to programmer.
Max. Delay Through Interface	200 ns, plus cable delay.
Service Request Methods	Program interrupt, or non-processor request.
Interrupt Priority Level	A flexible jumper arrangement allows the Model 1900 to request interrupt on one of four request lines - BR7, BR6, BR5 or BR4. Unless otherwise specified, unit is wired for lowest priority - BR4.
Interrupt Daisy Chain Continuity	All unused bus request lines and bus grant lines are jumpered through to preserve daisy chain integrity.
Non-processor Request	A DMA device plugged into LSI-11 bus can request bus mastership by asserting its BDMR line. This causes the NPR line to be asserted in the Unibus. Once granted mastership, the requesting device can then transfer data directly to any device on the LSI-11 bus or to any device on the Unibus.
Non-processor Grant Continuity	The NPG signal is passed through the Model 1900 unaltered if the requesting device is not on the LSI side of the translator.

PHYSICAL & ENVIRONMENTAL

Size	8½″ × 10″ × 0.375″ (standard DEC quad).
Unibus Compatibility	System Units DD11A & DD11B: Any slot, 1 through 4; Positions C-D-E-F (Use of Non-processor Request requires removal of one wire-wrap jumper and addition of one other). Backplane DD11-CK: Any slot, 1 through 4; Positions C-D-E-F Backplane DD11-DK: Any slot, 1 through 9; Positions C-D-E-F Backplane DD11-PK: Any slot, 3 through 9; Positions C-D-E-F
Power	+5V ±5% @ 2 amps
Temperature Range of Operation	0°C to 55°C

SPECIFICATIONS
MODEL 1950
BUS REPEATER

Function	Provides bi-directional drive capability for all DEC LSI-11 bus signals. Allows master backplane (with CPU) to drive a slave backplane (without CPU). Can be used with any system structured around LSI-11 bus.
Point of Insertion	Unit can be inserted as last card in master backplane or first card in slave backplane.
Method of Expansion	Connection from 1950 to expansion chassis made by means of Model 1900-BC bus cables. The cables plug into two headers on the 1950 and into the Model 1900-CT cable terminator on the other end. The 1900-CT plugs into one card slot of the expansion backplane. When used with the ADAC System 1000 Series, the 1900-BC plugs directly into the backplane without need for the 1900-CT.
Bus Loading	One bus load or each line on master side.
Drive Capability	15 bus loads for each line on slave side.
Configuration	Back to back bi-directional open-collector transceivers.
Bus Terminators	Provision for 120 ohm terminator networks on both sides of repeater. Normally supplied with networks on expansion side only.
Communications Method with Slave Peripherals	Program control/program interrupt and direct memory access.
Interfacing Technique	Completely asynchronous, interlocking handshake interface between busses.
Effects on LSI-11 Programming	None. All LSI-11 instructions can operate across the repeater. Operation is transparent to programmer.
Max. Delay Through Repeater	200 ns, plus cable delay.
Service Request Methods	Program interupt and DMA.
Interrupt Daisy Chain Continuity	The interrupt acknowledge input (BIAKI) is jumpered to interrupt acknowledge output (BIAKO) on the master bus side to preserve daisy chain integrity.
Direct Memory Access	A DMA device plugged into expander bus can request bus mastership by asserting its BDMR line. Once granted mastership, the requesting device can then transfer data directly to any device on either side of the repeater.

PHYSICAL & ENVIRONMENTAL

Size	8½″ × 5″ × 0.375″ (standard DEC half quad)
Power	+5V ±5% @ 1.5 amps
Termperature Range of Operation	0°C to +55°C

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MODEL 1900

LSI-11 TO UNIBUS TRANSLATOR

GENERAL DESCRIPTION

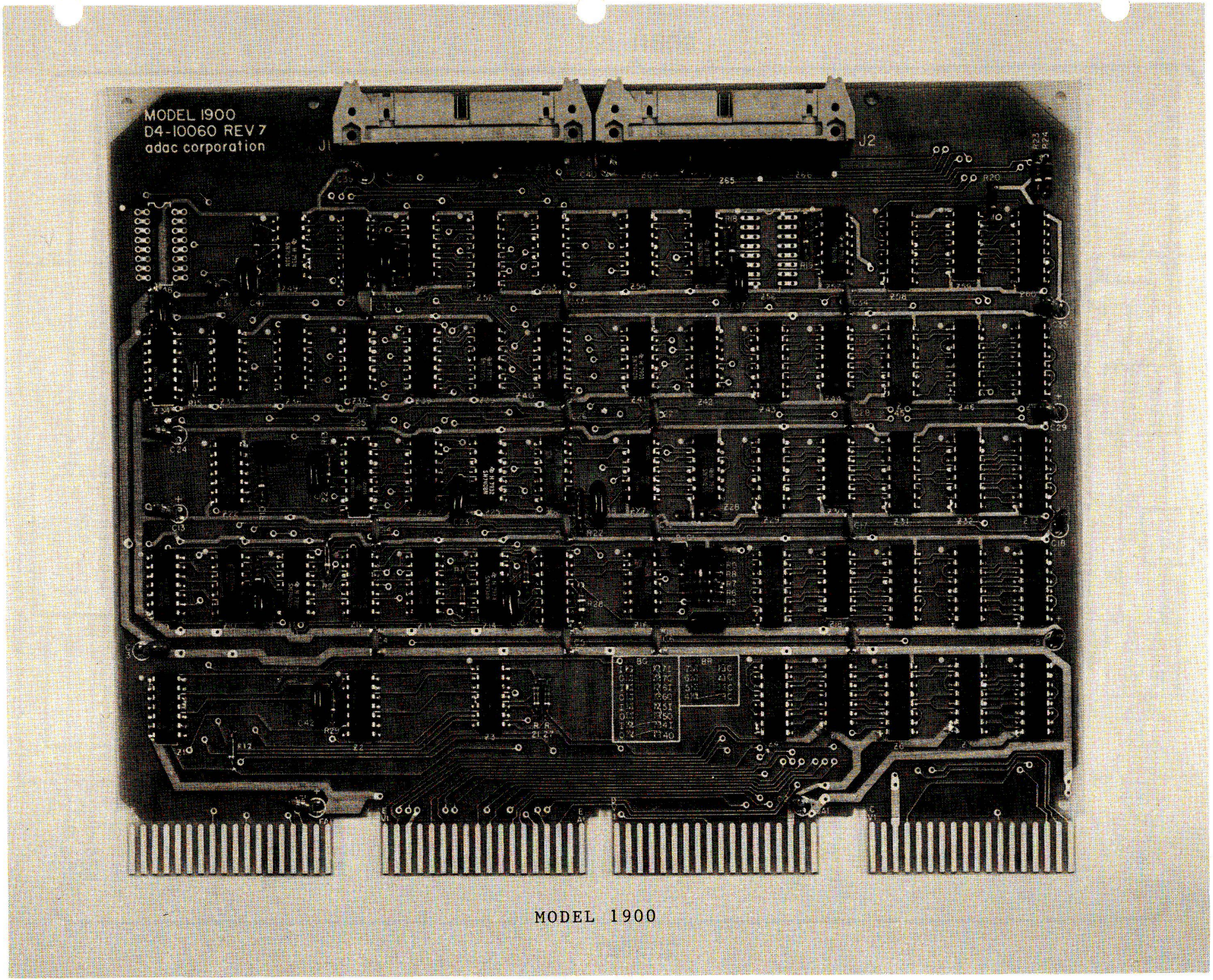
The Model 1900 is the first bus translator that allows Digital Equipment Corporation LSI-11 peripherals to operate with a Unibus CPU (any of the PDP-11 series). The Model 1900 can be inserted directly into the Unibus. It allows peripherals located on the expander side to be communicated with in the exact manner as if the peripherals were inserted directly in the CPU bus. Peripherals on either side of the translator can transfer data to and from peripherals on its own bus or through the translator to the other bus with no significant loss of speed. Furthermore, the expander bus can be located up to 40 feet from the CPU bus.

Peripherals on the expander side of the translator can be operated under program control, program interrupt or direct memory access.

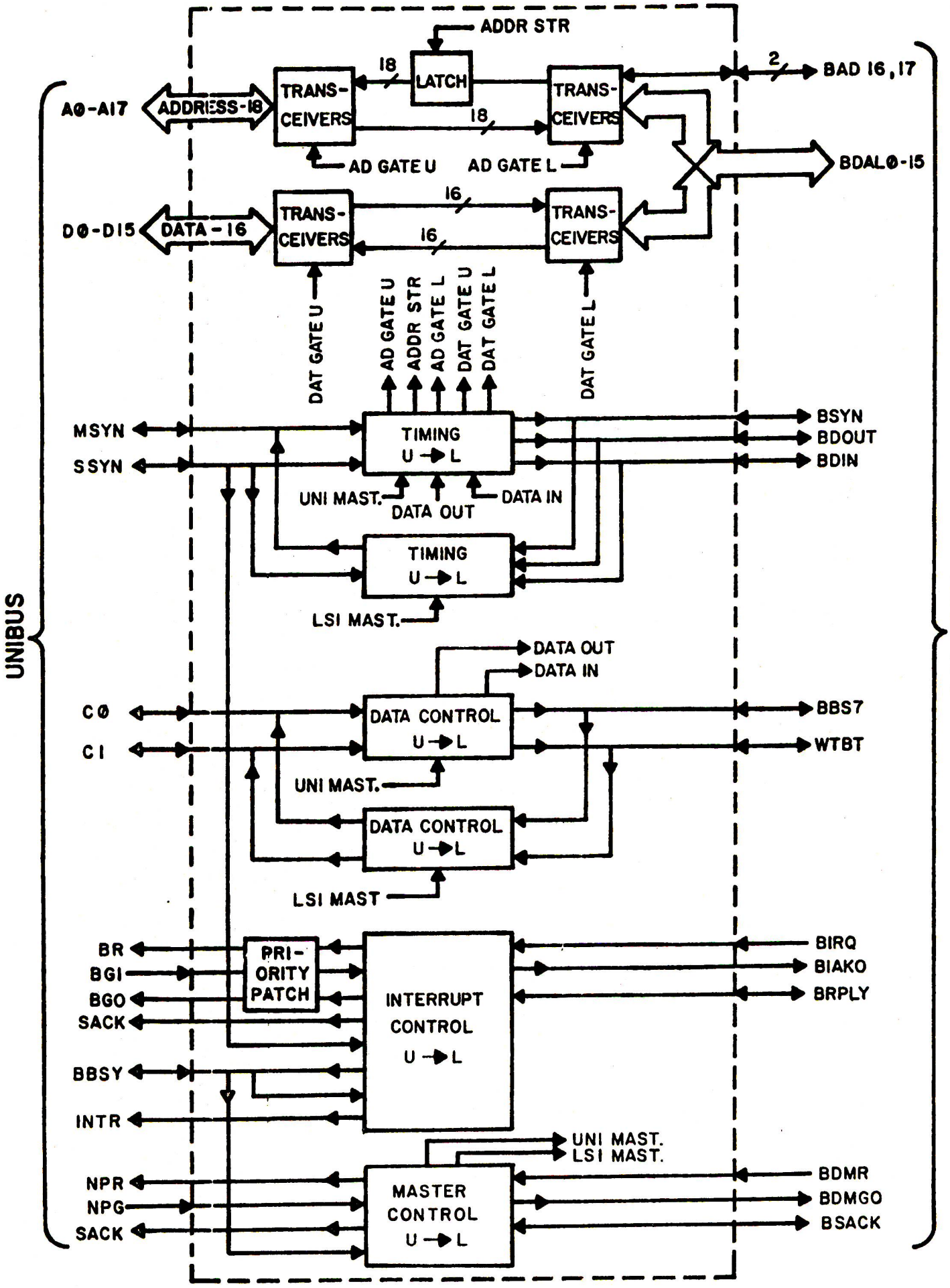
In addition to 16 bits of data, a full addressing capability of 18 bits is supplied across the translator. All inputs are buffered through low current input receivers and all outputs are either high powered open collector drivers. All inputs and outputs are terminated in 120 ohm characteristic impedances.

PHYSICAL DESCRIPTION

The Model 1900 consists of a quad size board (8 1/2" x 10") that can be plugged into the C-D-E-F positions of any of the four slots of a DEC DD11A system unit. Two 40 pin headers are mounted on the edge of the board away from the bus. Connection to the LSI-11 bus is made by means of two flat, high speed transmission cables. For connection to the ADAC System 1000 or 2000 series, connectors are supplied to allow the cable to be plugged directly into its backplane. For connection to a PDP-11/03 or other LSI-11 backplanes, the cables are terminated on a half quad (8 1/2" x 5") board that plugs into one slot.



MODEL 1900



BLOCK DIAGRAM - MODEL 1900 - BUS TRANSLATOR

APPLICATION

The Model 1900 translator allows Unibus users to take full advantage of the substantially lower cost memories and peripherals that are available for the LSI-11 bus structure. It also allows all PDP-11 systems to operate with the ADAC System 1000 series of LSI-11 bus structured peripheral expanders. The System 1000 series can house up to 11 full quad or 22 half quad LSI-11 compatible peripherals in a 7" high rack mounted enclosure. The System 1000, which can operate with a resident LSI-11 CPU, can also be used as a slave expander chassis to any PDP-11 by inserting the Model 1900 into the Unibus and plugging the bus cable directly into its backplane.

THEORY OF OPERATION

The Model 1900 Bus Translator acts with the capacity of a traffic controller between a Unibus (with CPU) and an LSI-11 bus (without CPU). A master control section determines whether a module in the Unibus or a module in the LSI bus is to be master. The control is initialized so that the Model 1900 assumes that the Unibus is master unless the LSI bus requests and is granted bus mastership through a non-processor request.

When the Unibus is master, the timing and data control sections of the 1900 convert the Unibus signals such as MSYN, SSYN, CØ and C1 into properly timed LSI signals, such as BSYN, BDOUT, BDIN, BBSD and BWTBT. This allows any device in the Unibus to transfer data to and from any device in the LSI-11 bus.

The 16 address lines and 16 data lines of the Unibus are connected to the 16 multiplexed data address lines of the LSI bus through bidirectional transceivers. The two most significant address lined (A16, A17) are also carried through transceivers to the LSI extended address lines, BAD 16 and BAD 17 for future expansion capability.

The direction of signal flow through the address and data transceivers is determined by the master control section. When the Unibus is master, AD GATE L allows the address on the Unibus to be gated into the LSI bus at the beginning of MSYN. After the end of AD GATE L, either DAT GATE L or DAT GATE U is asserted, depending upon whether a Data Out or Data In operation is to be performed. These signals turn on the appropriate data drivers on the LSI bus for Data Out and on the Unibus for Data In. The timing signals, BDOUT or BDIN are also generated, with appropriate delays so that they can be used for data strobing purposes.

In all cases, and for each type of operation, complete interlocking handshaking of control signals occur between the Unibus and LSI bus to allow complete asynchronous operation. Signal delays through the translator and the bus extension cable are essentially of no significance because of the interlocking action employed. Also a minimum of 150 nanoseconds of delay is generated between data and the edge of any control signal to allow for deskewing of the address and data lines and for decoding by the bus devices.

Under program control, the PDP-11 CPU can access any device inserted in the LSI bus in the same manner as it would communicate with another device plugged into the Unibus. The addressing of memory and other peripherals located in the LSI bus have to be considered in the same vein as if the devices were plugged into the Unibus.

The interrupt control section of the Model 1900 translator allows any device plugged into the LSI bus to request an interrupt of the PDP-11. The interrupting level is jumper selectable on the 1900 to be one of four priority levels 7, 6, 5 or 4. Unless otherwise specified, the Model 1900 is shipped with the LSI bus requesting and being granted on priority level 7, which is the highest level. The request and grant signals for levels 6, 5 and 4 are jumpered through the board.

The interrupt control section supplies all the interlocking handshaking circuitry needed for proper Unibus operation. A vector produced on the LSI bus is passed through to the Unibus at the appropriate time.

The Model 1900 also allows a DMA device located in the LSI bus to request bus mastership. Once granted, the DMA device may then transfer data directly to a memory or storage device located in the LSI bus or located across the translator in the Unibus. With the LSI being granted master, the Model 1900 transforms all LSI bus control signals into appropriately timed Unibus signals. During the address portion of the LSI cycle, the address is stored in latches before driving the transceivers on the Unibus. The address and data is then presented in parallel, as required by the Unibus.

CABLE AND BUS TERMINATIONS

As mentioned earlier, the Model 1900 is a quad size card that plugs directly into the Unibus. On the side of the board opposite the Unibus are mounted two 40 pin headers that carry the LSI bus signals and allow connection to the LSI bus by means of the Model 1900-BC cable set. The 1900-BC cable set consists of two forty wire flat cables supplied in several configurations. All models have 50 pin strain relief connectors on both ends. The length and type of cable can vary. For 10' and 15' lengths the cable is supplied as 120 ohm flat ribbon cable. For 20', 30' and 40' lengths, the cable is supplied as 120 ohm flat twisted pair, with an individual ground wire twisted with each signal wire.

If the Model 1900 is operated with the ADAC System 1000 Series, the strain reliefed connector can plug directly into headers provided on its backplane. If the Model 1900 is to be used with the DEC LSI-11 backplane, or equivalent, the strain reliefed connector can plug into the ADAC Model 1900-CT cable terminator. The Model 1900-CT is a 1/2 quad board (8 1/2" x 5") that plugs directly into an LSI-11 configured backplane. The edge of the board opposite the bus contains two 40 pin headers in order to be able to accept the 1900-BC cable set.

INSTALLATION INSTRUCTIONS

The Model 1900 plugs into any slot, 1 through 4, positions C-D-E-F of a DEC DD11A or DD11B system unit. It can also be used in printed circuit backplanes such as used on the PDP 11/04. On the DD11-CK backplane, it may be inserted in any slot, 1 through 4, positions C-D-E-F. In the DD11-DK backplane, use any slot, 3 through 9, positions C-D-E-F.

On current production backplanes, DEC places a wire wrap jumper from pin CA1 to pin CB1 to preserve daisy chain continuity on the Non-Processer Grant signal. This jumper must be removed for proper operation of the 1900. On older system units, the NPG signal path is from 1AU1 to 4AU1. In this application, this wire must be removed and two wires must be added - from 1AU1 to CA1 on the 1900 slot and from CB1 on the 1900 slot to 4AU1. There must be no other wires on CA1 and CB1.

MODEL 1900

CONNECTOR J1

1.	Spare	2.	GROUND
3.	BDAL1L	4.	
5.	BDALØL	6.	
7.	BINITL	8.	
9.	BDMGIL	10.	
11.	BREFL	12.	
13.	BBS7L	14.	
15.	HALTL	16.	
17.	BDMRL	18.	
19.	BIAKOL	20.	
21.	BIRQL	22.	
23.	BWTBTL	24.	
25.	BSYNL	26.	
27.	BDINL	28.	
29.	BRPLYL	30.	
31.	BDOUTL	32.	
33.	BAD17L	34.	
35.	BAD16L	36.	
37.	BUS Spare 2	38.	
39.	BUS Spare 1	40.	

MODEL 1900

CONNECTOR J2

1.	Spare	2.	GROUND
3.	BDAL15L	4.	
5.	BDAL14L	6.	
7.	BDAL13L	8.	
9.	BDAL12L	10.	
11.	BEVNTL	12.	
13.	BDAL11L	14.	
15.	BUS Spare 6	16.	
17.	BDAL1ØL	18.	
19.	BSACKL	20.	
21.	BDAL9L	22.	
23.	BDAL8L	24.	
25.	BDAL7L	26.	
27.	BDAL6L	28.	
29.	BDAL5L	30.	
31.	BDAL4L	32.	
33.	BDAL3L	34.	
35.	BDAL2L	36.	
37.	BPOKH	38.	
39.	BDCOKH	40.	

SPECIFICATIONS

MODEL 1900

LSI-11 TO UNIBUS TRANSLATOR

Function	Provides translation of all Unibus signals into LSI-11 bus signals (and vice versa) to allow LSI-11 peripherals to function directly with any PDP-11 Unibus computer.
Point of Insertion	Unit is plugged directly into Unibus.
Method of Connection to PDP-11/03	Connects to LSI-11 bus via Model 1900-BC Bus Cable and Model 1900-CT Cable Terminator.
Method of Connection to ADAC System 1000	Connects to bus of System 1000 Series via Model 1900-BC Bus Cable which plugs directly into backplane.
Unibus Loading	One bus load.
LSI-11 Drive Capability	15 bus loads on LSI-11 bus plus 120 ohm terminator on each line, mounted on Model 1900.
Module Types - LSI Side	All standard modules designed to interface to LSI-11 bus, except LSI-11 CPU. This includes A/D, D/A, memory floppy disc controllers, etc.
Communication Methods with LSI Peripherals	Program control, program interrupt and direct memory access.
Interfacing Technique	Completely asynchronous, interlocking handshake interface between Unibus and LSI-11 bus.

Effects on Unibus Programming	None. All PDP-11 instructions can operate across the interface. Operation is transparent to programmer.
Max Delay Through Interface	200 ns, plus cable delay.
Service Request Methods	Program interrupt, or non-processor request.
Interrupt Priority Level	A flexible jumper arrangement allows the Model 1900 to request interrupt on one of four request lines - BR7, BR6, BR5 or BR4. Unless otherwise specified, unit is wired for highest priority - BR7.
Interrupt Daisy Chain Continuity	All unused bus request lines and bus grant lines are jumpered through to preserve daisy chain integrity.
Non-processor Request	A DMA device plugged into LSI-11 bus can request bus mastership by asserting its BDMR line. This causes the NPR line to be asserted in the Unibus. Once granted mastership, the requesting device can then transfer data directly to any device on the LSI-11 bus or to any device on the Unibus.
Non-processor Grant Continuity	The NPG signal is passed through the Model 1900 unaltered if the requesting device is not on the LSI side of the translator.
Physical & Environmental Size	8 1/2" x 10" x 0.375" (standard DEC quad).
Unibus Compatibility	System Units DD11A & DD11B: Any slot, 1 through 4; Positions C-D-E-F (Use of Non-processor Request requires removal of one wire-wrap jumper and addition of one other). Backplane DD11-CK: Any slot, 1 through 4; Positions C-D-E-F Backplane DD11-DK: Any slot, 1 through 9; Positions C-D-E-F Backplane DD11-PK: Any slot, 3 through 9; Positions C-D-E-F
Power	+5V $\pm$ 5% @ 2 amps
Temperature Range of Operation	$0^{o}C$ to $55^{o}C$

WARRANTY

ADAC Corporation warrants all data acquisition systems it manufactures to be free from defects in material and factory workmanship, and agrees to repair or replace any system that, under normal use, reveals such a defect within 90 days after shipment to customer.

This warranty shall not apply to any system that has been:

1. repaired, worked on, or altered by persons unauthorized by ADAC, in such a manner as to injure, in ADAC's sole judgment, the performance, stability, or reliability of the system.

2. subject to misuse, negligence, or accident: or

3. connected, installed, adjusted, or used otherwise than in accordance with the instructions furnished by ADAC.

This warranty is in lieu of any other warranty, expressed or implied, including the warranty of merchantability and fitness for particular purposes, and is applicable to any system bearing the "ADAC data conversion systems warranty," and so designated in the literature pertaining to that system.

ADAC reserves the right to make any changes in the design or construction of its systems at any time, without incurring any obligation to make any change whatever in units previously delivered.

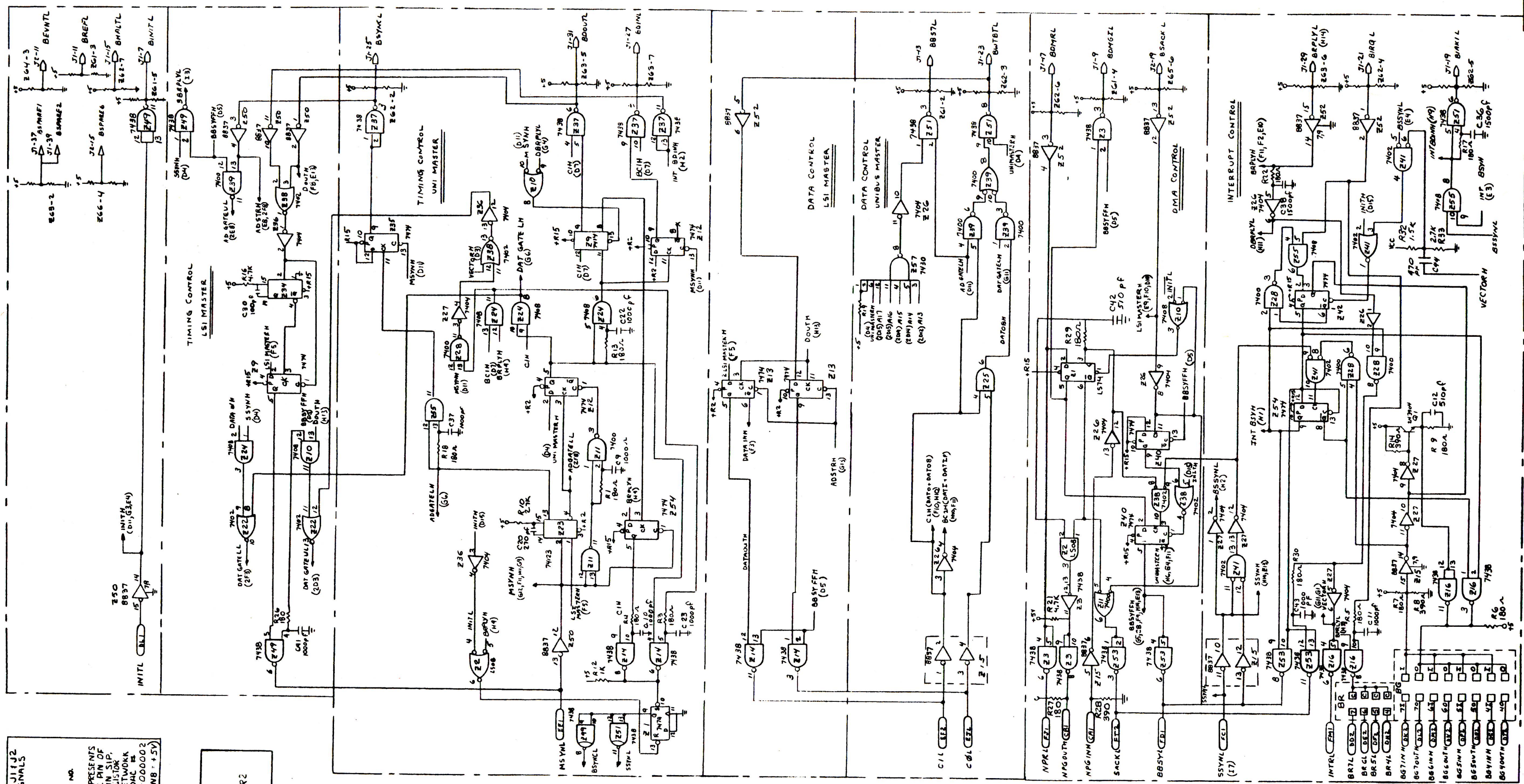
ADAC's sole liabilities, and the buyer's sole remedies, under this agreement shall be limited to a refund of the purchase price, or, at ADAC's sole discretion, to the repair or replacement of any system that proves, upon ADAC's examination, to be defective when returned to the ADAC factory, transportation prepaid by the buyer, within 90 days from the date of original shipment.

ADAC shall in no way be liable for damages consequential or incidental to defects in any system, for failure of delivery in whole or in part, for injuries resulting from its use, or for any other cause.

The warranty and the writing attached constitute the full understanding of the manufacturer and buyer, and no terms, conditions, understanding, or agreement purporting to modify or vary the terms hereof shall be binding unless hereafter made in writing and signed by an authorized officer of ADAC Corporation.

REVISIONS

REV	ECO	DESCRIPTION	DWN	APPLS	DATE
9	0594	ARTWORK REVISIONS	EHM		3 JAN 83
9A	0606	TIMING ERROR CORRECTION	EHM		4 · 4 · 83



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES

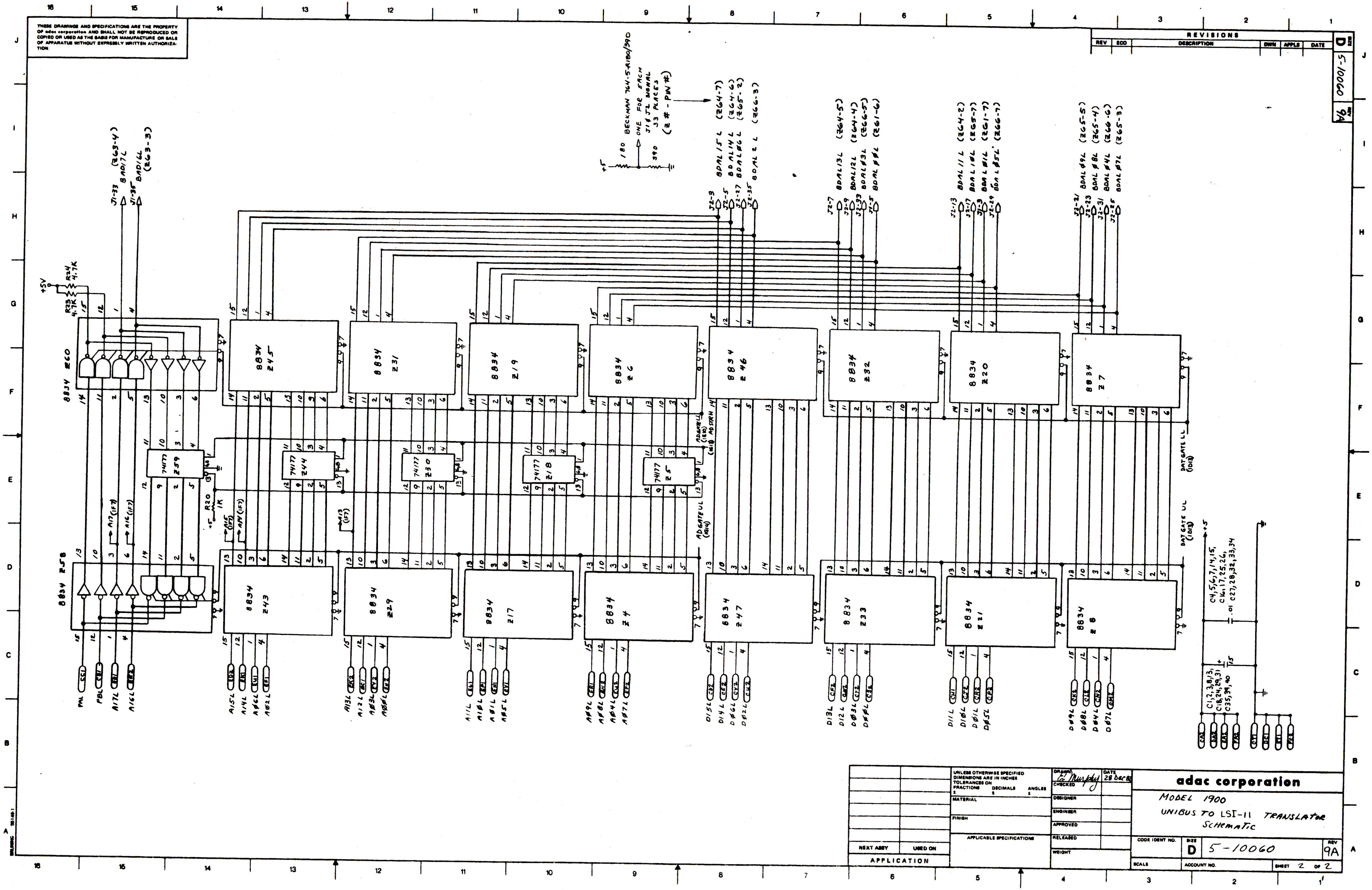
DRAWN Murphy DATE 3 JAN 83

adac corporation

MODEL 1900
UNIBUS TO LSI-11 TRANSLATOR
SCHEMATIC

SIZE D 5 - 10060 REV 9A

SHEET 1 OF 2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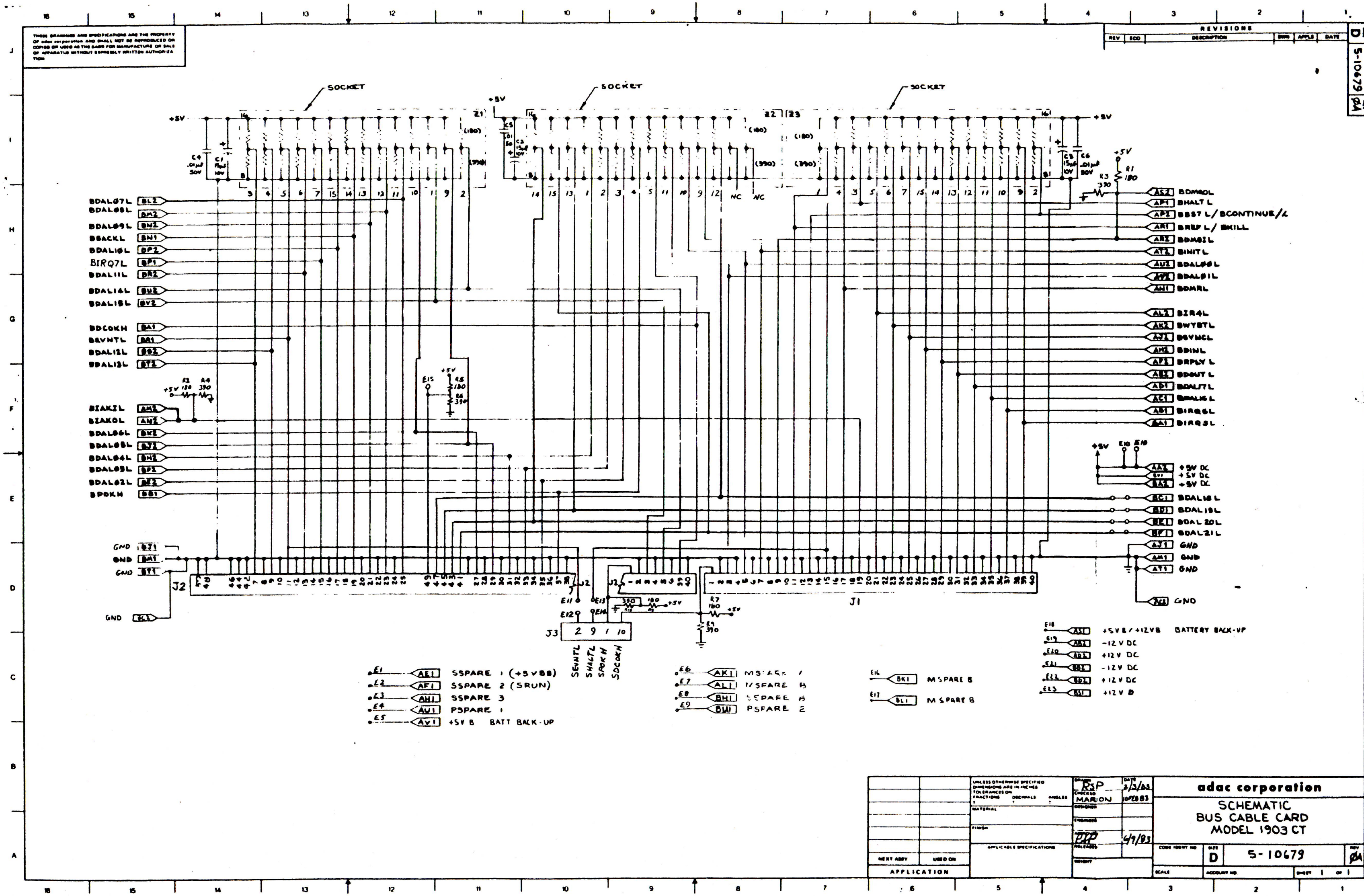
REVISIONS
D 5-10060 9A
BECKMAN 764-5-A180/390
ONE FOR EACH J1 & J2 SIGNAL 33 PLACES
(Z # - PN #)
8834
74177
adac corporation
MODEL 1900
UNIBUS TO LSI-11 TRANSLATOR
SCHEMATIC
DRAWN C. Murphy
DATE 28 Dec 83
D 5-10060
REV 9A
SHEET 2 OF 2
APPLICATION



adac corporation

SCHEMATIC
BUS CABLE CARD
MODEL 1903 CT

DRAWN	RSP 2/3/83
CHECKED	MARION 10FEB83
RELEASED	6/9/83
SIZE	D
DWG NO	5-10679
REV	ØA
SHEET	1 OF 1

APPLICATION: NEXT ASSY / USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS / DECIMALS / ANGLES. MATERIAL. FINISH. APPLICABLE SPECIFICATIONS.

APPENDIX
Q-BUS SIGNAL
PIN-LIST

CARD-EDGE SEQUENTIAL LIST:

CABLE I/O PIN	BUS PIN	Q-BUS MNEMONIC	SIGNAL DESCRIPTION
J1 - 39	AA1	BIRQ5 L	BUS INTERRUPT REQUEST LEVEL 5
J1 - 37	AB1	BIRQ6 L	BUS INTERRUPT REQUEST LEVEL 6
J1 - 35	AC1	BDAL16 L	DATA/ADDRESS SIGNAL LINE (mem parity ctrl) 16
J1 - 33	AD1	BDAL17 L	DATA/ADDRESS SIGNAL LINE (mem parity ctrl) 17
---	AE1	SSPARE1	SPECIAL SPARE - NOT BUSSED (alternate +5B)
---	AF1	SSPARE2	SPECIAL SPARE - NOT BUSSED (SRUN L in slot 1)
---	AH1	SSPARE3	SPECIAL SPARE - NOT BUSSED
---	AJ1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	AK1	MSPAREA	MAINTENANCE SPARE - NOT BUSSED (AK1-AL1 tied in some
---	AL1	MSPAREA	MAINTENANCE SPARE - NOT BUSSED .. DEC backplanes)
---	AM1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
J1 - 17	AN1	BDMR L	DMA REQUEST
J1 - 15	AP1	BHALT L	PROCESSOR HALT COMMAND LINE
J1 - 11	AR1	BREF L	REFRESH ADDRESS MODE / SLAVE ASSERTS DATBIO CONTINUE
---	AS1	+12B/+5B	+12/+5 Vdc BATTERY BACK-UP
---	AT1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	AU1	PSPARE1	SPARE - NOT ASSIGNED
---	AV1	+5B	+5 Vdc BATTERY BACK-UP
J2 - 39	BA1	BDCOK H	DC VOLTAGES OKAY (master drives slave signal)
J1 - 01	BA1	BDCOK H	SDCOK H (slave pwr supply drives master signal) <J3-10 on 1903CT>
J2 - 37	BB1	BPOK H	AC POWER OK (master drives slave signal)
J2 - 01	BB1	BPOK H	SPOK (slave pwr supply drives master signal) <J3-01 on 1903CT>
J2 - 47	BC1	BDAL18 L	ADDRESS / BUS PARITY formerly "SSPARE4"
J2 - 45	BD1	BDAL19 L	ADDRESS / BUS PARITY formerly "SSPARE5"
J2 - 43	BE1	BDAL20 L	ADDRESS / BUS PARITY formerly "SSPARE6"
J2 - 41	BF1	BDAL21 L	ADDRESS / BUS PARITY formerly "SSPARE7"
---	BH1	SSPARE8	SPECIAL SPARE - NOT BUSSED
---	BJ1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	BK1	MSPAREB	MAINTENANCE SPARE - NOT BUSSED (BK1-BL1 tied in some
---	BL1	MSPAREB	MAINTENANCE SPARE - NOT BUSSED .. DEC backplanes)
---	BM1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
J2 - 19	BN1	BSACK L	SYNCHRONOUS ACKNOWLEDGE (DMA BUS BUSY)
J2 - 15	BP1	BIRQ7 L	BUS INTERRUPT REQUEST LEVEL 7
J2 - 11	BR1	BEVENT L	60 HZ CLOCK OR OTHER INTERRUPT RQST <J3-02 on 1903CT>
---	BS1	+12B	+12vdc BATTERY BACKUP (not connected to "AS1")
---	BT1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	BU1	PSPARE2	SPARE - NOT ASSIGNED
---	BV1	+5	LOGIC VOLTAGE SUPPLY

CABLE I/O PIN	BUS PIN	Q-BUS MNEMONIC	SIGNAL DESCRIPTION
---	AA2	+5VDC	LOGIC VOLTAGE SUPPLY
---	AB2	-12VDC	LOGIC VOLTAGE SUPPLY
---	AC2	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	AD2	+12VDC	LOGIC VOLTAGE SUPPLY
J1 - 31	AE2	BDOUT L	DATA OUT, FROM MASTER TO SLAVE
J1 - 29	AF2	BRPLY L	REPLY, XFER ACKNOWLEDGE FROM SLAVE
J1 - 27	AH2	BDIN L	DATA IN (slave to master) / VECTOR RQST
J1 - 25	AJ2	BSYNC L	L-E ADDR. STRB, ACTIVE FOR FULL XFR CYCLE
J1 - 23	AK2	BWTBT L	WRITE AT ADDR-STR / BYTE AT DATO, DATOB, DATBO
J1 - 21	AL2	BIRQ4 L	BUS INTERRUPT REQUEST LEVEL 4
J1 - 19	AM2	BIAKI L	INTERRUPT ACKNOWLEDGE D-CHAIN INPUT
---	AN2	BIAKO L	INTERRUPT ACKNOWLEDGE D-CHAIN OUTPUT
J1 - 13	AP2	BBS7 L	I/O PAGE ADDRESS / DATBI => ONE MORE TRANSFER
J1 - 09	AR2	BDMGI L	DMA GRANT D-CHAIN INPUT
---	AS2	BDMGO L	DMA GRANT D-CHAIN OUTPUT
J1 - 07	AT2	BINIT L	INITIALIZE HARDWARE DEVICES
J1 - 05	AU2	BDAL00 L	DATA/ADDRESS SIGNAL LINE 00
J1 - 03	AV2	BDAL01 L	DATA/ADDRESS SIGNAL LINE 01
---	BA2	+5VDC	LOGIC VOLTAGE SUPPLY
---	BB2	-12VDC	LOGIC VOLTAGE SUPPLY
---	BC2	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	BD2	+12	LOGIC VOLTAGE SUPPLY
J2 - 35	BE2	BDAL02 L	DATA/ADDRESS SIGNAL LINE 02
J2 - 33	BF2	BDAL03 L	DATA/ADDRESS SIGNAL LINE 03
J2 - 31	BH2	BDAL04 L	DATA/ADDRESS SIGNAL LINE 04
J2 - 29	BJ2	BDAL05 L	DATA/ADDRESS SIGNAL LINE 05
J2 - 27	BK2	BDAL06 L	DATA/ADDRESS SIGNAL LINE 06
J2 - 25	BL2	BDAL07 L	DATA/ADDRESS SIGNAL LINE 07
J2 - 23	BM2	BDAL08 L	DATA/ADDRESS SIGNAL LINE 08
J2 - 21	BN2	BDAL09 L	DATA/ADDRESS SIGNAL LINE 09
J2 - 17	BP2	BDAL10 L	DATA/ADDRESS SIGNAL LINE 10
J2 - 13	BR2	BDAL11 L	DATA/ADDRESS SIGNAL LINE 11
J2 - 09	BS2	BDAL12 L	DATA/ADDRESS SIGNAL LINE 12
J2 - 07	BT2	BDAL13 L	DATA/ADDRESS SIGNAL LINE 13
J2 - 05	BU2	BDAL14 L	DATA/ADDRESS SIGNAL LINE 14
J2 - 03	BV2	BDAL15 L	DATA/ADDRESS SIGNAL LINE 15

FUNCTIONALLY GROUPED SIGNAL LIST:

CABLE I/O PIN	BUS PIN	Q-BUS MNEMONIC	SIGNAL DESCRIPTION
INTERRUPT HANDLING SIGNALS:			
J2 - 11	BR1	BEVENT L	60 HZ CLOCK OR OTHER INTERRUPT RQST <J3-02 on 1903CT>
J1 - 21	AL2	BIRQ4 L	BUS INTERRUPT REQUEST LEVEL 4
J1 - 39	AA1	BIRQ5 L	BUS INTERRUPT REQUEST LEVEL 5
J1 - 37	AB1	BIRQ6 L	BUS INTERRUPT REQUEST LEVEL 6
J2 - 15	BP1	BIRQ7 L	BUS INTERRUPT REQUEST LEVEL 7
J1 - 19	AM2	BIAKI L	INTERRUPT ACKNOWLEDGE D-CHAIN INPUT
---	AN2	BIAKO L	INTERRUPT ACKNOWLEDGE D-CHAIN OUTPUT
DMA TRANSACTION SIGNALS:			
J1 - 17	AN1	BDMR L	DMA REQUEST
J2 - 19	BN1	BSACK L	SYNCHRONOUS ACKNOWLEDGE (DMA BUS BUSY)
J1 - 09	AR2	BDMGI L	DMA GRANT D-CHAIN INPUT
---	AS2	BDMGO L	DMA GRANT D-CHAIN OUTPUT
TRANSFER CONTROL SIGNALS:			
J1 - 31	AE2	BDOUT L	DATA OUT, FROM MASTER TO SLAVE
J1 - 29	AF2	BRPLY L	REPLY, XFER ACKNOWLEDGE FROM SLAVE
J1 - 27	AH2	BDIN L	DATA IN (slave to master) / VECTOR RQST
J1 - 25	AJ2	BSYNC L	L-E ADDR. STRB, ACTIVE FOR FULL XFR CYCLE
J1 - 23	AK2	BWTBT L	WRITE AT ADDR-STR / BYTE AT DATO, DATOB, DATBO
DATA AND ADDRESS LINES:			
J1 - 05	AU2	BDAL00 L	DATA/ADDRESS SIGNAL LINE 00
J1 - 03	AV2	BDAL01 L	DATA/ADDRESS SIGNAL LINE 01
J2 - 35	BE2	BDAL02 L	DATA/ADDRESS SIGNAL LINE 02
J2 - 33	BF2	BDAL03 L	DATA/ADDRESS SIGNAL LINE 03
J2 - 31	BH2	BDAL04 L	DATA/ADDRESS SIGNAL LINE 04
J2 - 29	BJ2	BDAL05 L	DATA/ADDRESS SIGNAL LINE 05
J2 - 27	BK2	BDAL06 L	DATA/ADDRESS SIGNAL LINE 06
J2 - 25	BL2	BDAL07 L	DATA/ADDRESS SIGNAL LINE 07
J2 - 23	BM2	BDAL08 L	DATA/ADDRESS SIGNAL LINE 08
J2 - 21	BN2	BDAL09 L	DATA/ADDRESS SIGNAL LINE 09
J2 - 17	BP2	BDAL10 L	DATA/ADDRESS SIGNAL LINE 10
J2 - 13	BR2	BDAL11 L	DATA/ADDRESS SIGNAL LINE 11
J2 - 09	BS2	BDAL12 L	DATA/ADDRESS SIGNAL LINE 12
J2 - 07	BT2	BDAL13 L	DATA/ADDRESS SIGNAL LINE 13
J2 - 05	BU2	BDAL14 L	DATA/ADDRESS SIGNAL LINE 14
J2 - 03	BV2	BDAL15 L	DATA/ADDRESS SIGNAL LINE 15
J1 - 35	AC1	BDAL16 L	DATA/ADDRESS SIGNAL LINE (mem parity ctrl) 16
J1 - 33	AD1	BDAL17 L	DATA/ADDRESS SIGNAL LINE (mem parity ctrl) 17
J2 - 47	BC1	BDAL18 L	ADDRESS / BUS PARITY formerly "SSPARE4"
J2 - 45	BD1	BDAL19 L	ADDRESS / BUS PARITY formerly "SSPARE5"
J2 - 43	BE1	BDAL20 L	ADDRESS / BUS PARITY formerly "SSPARE6"
J2 - 41	BF1	BDAL21 L	ADDRESS / BUS PARITY formerly "SSPARE7"
J1 - 13	AP2	BBS7 L	I/O PAGE ADDRESS / DATBI => ONE MORE TRANSFER

FUNCTIONALLY GROUPED SIGNAL LIST:

BUS PIN	MNEMONIC	DESCRIPTION
SYSTEM CONTROL SIGNALS:		
J1 - 15 AP1	BHALT L	PROCESSOR HALT COMMAND LINE
J1 - 11 AR1	BREF L	REFRESH ADDR MODE / SLAVE ASSERTS DATBIO CONTINUE
J2 - 39 BA1	BDCOK H	DC VOLTAGES OKAY (master drives slave bus signal)
J1 - 01 BA1	BDCOK H	SDCOK H (slave pwr supply drives master signal) <J3-10 on 1903CT>
J2 - 37 BB1	BPOK H	AC POWER OK (master drives slave bus signal)
J2 - 01 BB1	BPOK H	SPOK (slave pwr supply drives master signal) <J3-01 on 1903CT>
J1 - 07 AT2	BINIT L	INITIALIZE HARDWARE DEVICES
SPARE AND RESERVED LINES:		
--- AE1	SSPARE1	SPECIAL SPARE - NOT BUSSED (alternate +5B)
--- AF1	SSPARE2	SPECIAL SPARE - NOT BUSSED (SRUN L in slot 1)
--- AH1	SSPARE3	SPECIAL SPARE - NOT BUSSED
J2 - 47 BC1	BDAL18 L	ADDRESS / BUS PARITY formerly "SSPARE4"
J2 - 45 BD1	BDAL19 L	ADDRESS / BUS PARITY formerly "SSPARE5"
J2 - 43 BE1	BDAL20 L	ADDRESS / BUS PARITY formerly "SSPARE6"
J2 - 41 BF1	BDAL21 L	ADDRESS / BUS PARITY formerly "SSPARE7"
--- BH1	SSPARE8	SPECIAL SPARE - NOT BUSSED
--- AK1	MSPAREA	MAINTENANCE SPARE - NOT BUSSED (AK1-AL1 tied in some
--- AL1	MSPAREA	MAINTENANCE SPARE - NOT BUSSED .. DEC backplanes)
--- BK1	MSPAREB	MAINTENANCE SPARE - NOT BUSSED (BK1-BL1 tied in some
--- BL1	MSPAREB	MAINTENANCE SPARE - NOT BUSSED .. DEC backplanes)
--- AU1	PSPARE1	SPARE - NOT ASSIGNED
--- BU1	PSPARE2	SPARE - NOT ASSIGNED
--- BS1	+12B	+12vdc BATTERY BACKUP (not connected to "AS1")
POWER LINES:		
--- AJ1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
--- AM1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
--- AT1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
--- BJ1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
--- BM1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
--- BT1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
--- AC2	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
--- BC2	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
--- BV1	+5	LOGIC VOLTAGE SUPPLY
--- AA2	+5VDC	LOGIC VOLTAGE SUPPLY
--- BA2	+5VDC	LOGIC VOLTAGE SUPPLY
--- AD2	+12VDC	LOGIC VOLTAGE SUPPLY
--- BD2	+12	LOGIC VOLTAGE SUPPLY
--- AB2	-12VDC	LOGIC VOLTAGE SUPPLY
--- BB2	-12VDC	LOGIC VOLTAGE SUPPLY
--- AV1	+5B	+5 Vdc BATTERY BACK-UP
--- AS1	+12B/+5B	+12/+5 Vdc BATTERY BACK-UP

SIGNALS FROM THE Q-BUS FOUND ON I/O CONNECTOR J1:

CABLE I/O PIN	BUS PIN	Q-BUS MNEMONIC	SIGNAL DESCRIPTION
J1 - 01	BA1	BDCOK H	SDCOK H (slave pwr supply drives master signal) <J3-10 on 1903CT>
J1 - 03	AV2	BDAL01 L	DATA/ADDRESS SIGNAL LINE 01
J1 - 05	AU2	BDAL00 L	DATA/ADDRESS SIGNAL LINE 00
J1 - 07	AT2	BINIT L	INITIALIZE HARDWARE DEVICES
J1 - 09	AR2	BDMGI L	DMA GRANT D-CHAIN INPUT
J1 - 11	AR1	BREF L	REFRESH ADDRESS MODE / SLAVE ASSERTS DATBIO CONTINUE
J1 - 13	AP2	BBS7 L	I/O PAGE ADDRESS / DATBI => ONE MORE TRANSFER
J1 - 15	AP1	BHALT L	PROCESSOR HALT COMMAND LINE
J1 - 17	AN1	BDMR L	DMA REQUEST
J1 - 19	AM2	BIAKI L	INTERRUPT ACKNOWLEDGE D-CHAIN INPUT
J1 - 21	AL2	BIRQ4 L	BUS INTERRUPT REQUEST LEVEL 4
J1 - 23	AK2	BWTBT L	WRITE AT ADDR-STR / BYTE AT DATO, DATOB, DATBO
J1 - 25	AJ2	BSYNC L	L-E ADDR. STRB, ACTIVE FOR FULL XFR CYCLE
J1 - 27	AH2	BDIN L	DATA IN (slave to master) / VECTOR RQST
J1 - 29	AF2	BRPLY L	REPLY, XFER ACKNOWLEDGE FROM SLAVE
J1 - 31	AE2	BDOUT L	DATA OUT, FROM MASTER TO SLAVE
J1 - 33	AD1	BDAL17 L	DATA/ADDRESS SIGNAL LINE (mem parity ctrl) 17
J1 - 35	AC1	BDAL16 L	DATA/ADDRESS SIGNAL LINE (mem parity ctrl) 16
J1 - 37	AB1	BIRQ6 L	BUS INTERRUPT REQUEST LEVEL 6
J1 - 39	AA1	BIRQ5 L	BUS INTERRUPT REQUEST LEVEL 5

SIGNALS ON THE 1953 I/O CONNECTOR J2:

CABLE I/O PIN	BUS PIN	Q-BUS MNEMONIC	SIGNAL DESCRIPTION
J2 - 01	BB1	BPOK H	SPOK (slave pwr supply drives master signal)
J2 - 03	BV2	BDAL15 L	DATA/ADDRESS SIGNAL LINE 15
J2 - 05	BU2	BDAL14 L	DATA/ADDRESS SIGNAL LINE 14
J2 - 07	BT2	BDAL13 L	DATA/ADDRESS SIGNAL LINE 13
J2 - 09	BS2	BDAL12 L	DATA/ADDRESS SIGNAL LINE 12
J2 - 11	BR1	BEVENT L	60 HZ CLOCK OR OTHER INTERRUPT RQST <J3-02 on 1903CT>
J2 - 13	BR2	BDAL11 L	DATA/ADDRESS SIGNAL LINE 11
J2 - 15	BP1	BIRQ7 L	BUS INTERRUPT REQUEST LEVEL 7
J2 - 17	BP2	BDAL10 L	DATA/ADDRESS SIGNAL LINE 10
J2 - 19	BN1	BSACK L	SYNCHRONOUS ACKNOWLEDGE (DMA BUS BUSY)
J2 - 21	BN2	BDAL09 L	DATA/ADDRESS SIGNAL LINE 09
J2 - 23	BM2	BDAL08 L	DATA/ADDRESS SIGNAL LINE 08
J2 - 25	BL2	BDAL07 L	DATA/ADDRESS SIGNAL LINE 07
J2 - 27	BK2	BDAL06 L	DATA/ADDRESS SIGNAL LINE 06
J2 - 29	BJ2	BDAL05 L	DATA/ADDRESS SIGNAL LINE 05
J2 - 31	BH2	BDAL04 L	DATA/ADDRESS SIGNAL LINE 04
J2 - 33	BF2	BDAL03 L	DATA/ADDRESS SIGNAL LINE 03
J2 - 35	BE2	BDAL02 L	DATA/ADDRESS SIGNAL LINE 02
J2 - 37	BB1	BPOK H	AC POWER OK (master drives slave signal)
J2 - 39	BA1	BDCOK H	DC VOLTAGES OKAY (master drives slave signal)
2 - 41	BF1	BDAL21 L	ADDRESS / BUS PARITY formerly "SSPARE7"
J2 - 43	BE1	BDAL20 L	ADDRESS / BUS PARITY formerly "SSPARE6"
J2 - 45	BD1	BDAL19 L	ADDRESS / BUS PARITY formerly "SSPARE5"
J2 - 47	BC1	BDAL18 L	ADDRESS / BUS PARITY formerly "SSPARE4" <J3-01 on 1903CT>

CABLE I/O PIN	BUS PIN	Q-BUS MNEMONIC	SIGNAL DESCRIPTION
---	AE1	SSPARE1	SPECIAL SPARE - NOT BUSSED (alternate +5B)
---	AF1	SSPARE2	SPECIAL SPARE - NOT BUSSED (SRUN L in slot 1)
---	AH1	SSPARE3	SPECIAL SPARE - NOT BUSSED
---	AJ1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	AK1	MSPAREA	MAINTENANCE SPARE - NOT BUSSED (AK1-AL1 tied in som
---	AL1	MSPAREA	MAINTENANCE SPARE - NOT BUSSED .. DEC backplanes)
---	AM1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	AS1	+12B/+5B	+12/+5 Vdc BATTERY BACK-UP
---	AT1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	AU1	PSPARE1	SPARE - NOT ASSIGNED
---	AV1	+5B	+5 Vdc BATTERY BACK-UP
---	BH1	SSPARE8	SPECIAL SPARE - NOT BUSSED
---	BJ1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	BK1	MSPAREB	MAINTENANCE SPARE - NOT BUSSED (BK1-BL1 tied in som
---	BL1	MSPAREB	MAINTENANCE SPARE - NOT BUSSED .. DEC backplanes)
---	BM1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	BS1	+12B	+12vdc BATTERY BACKUP (not connected to "AS1")
---	BT1	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	BU1	PSPARE2	SPARE - NOT ASSIGNED
---	BV1	+5	LOGIC VOLTAGE SUPPLY
---	AA2	+5VDC	LOGIC VOLTAGE SUPPLY
---	AB2	-12VDC	LOGIC VOLTAGE SUPPLY
---	AC2	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	AD2	+12VDC	LOGIC VOLTAGE SUPPLY
---	AN2	BIAKO L	INTERRUPT ACKNOWLEDGE D-CHAIN OUTPUT
---	AS2	BDMGO L	DMA GRANT D-CHAIN OUTPUT
---	BA2	+5VDC	LOGIC VOLTAGE SUPPLY
---	BB2	-12VDC	LOGIC VOLTAGE SUPPLY
---	BC2	GND	GROUND - SIGNAL GROUND AND D.C. RETURN
---	BD2	+12	LOGIC VOLTAGE SUPPLY

APPLICATION NOTE

AN-13

22 BIT ADDRESSING CONSIDERATIONS

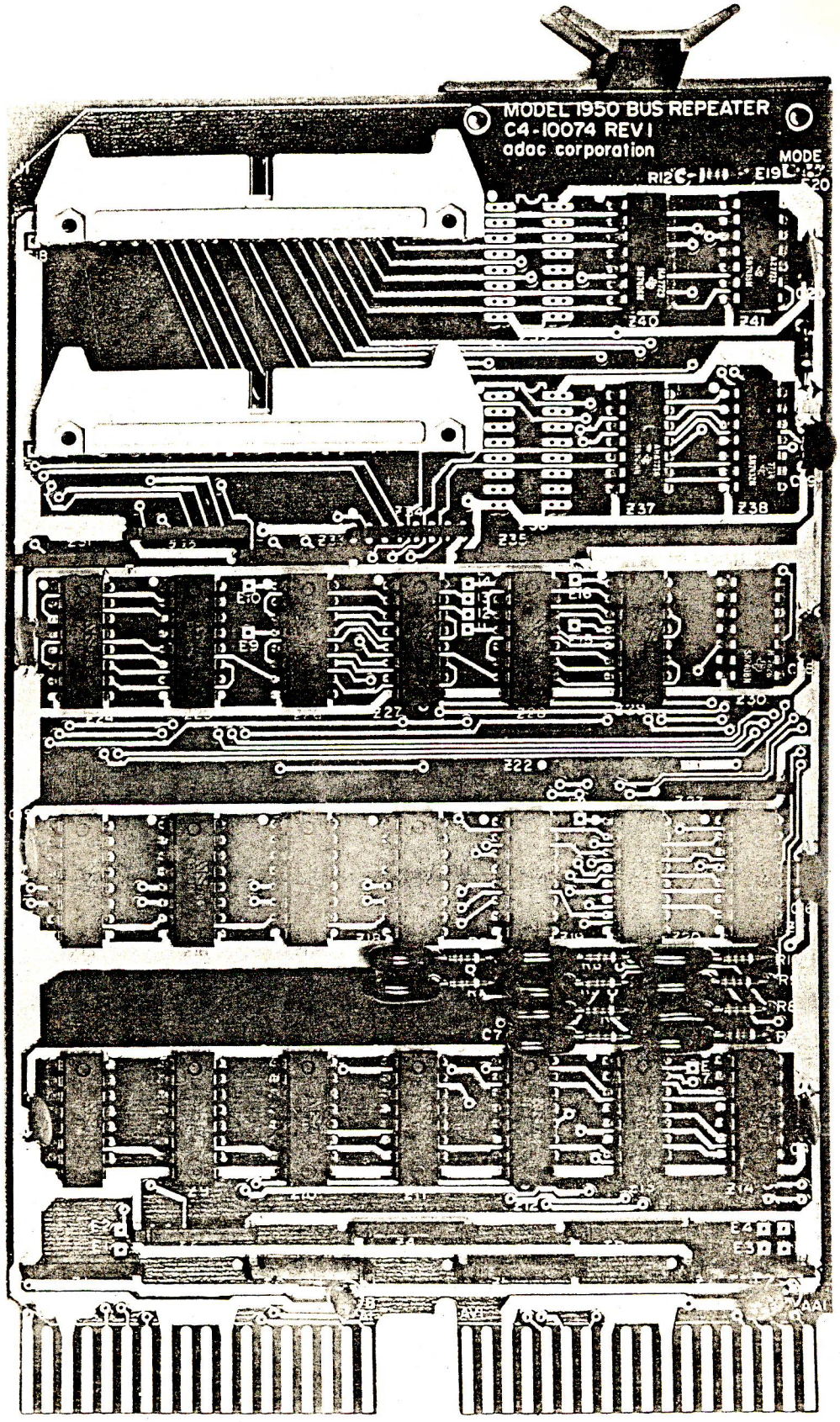
Consistent with Digital Equipment Corporation's announcement of the use of 22 bit addressing, the Model 1200 was announced as a system that contains the full 22 bit addressing scheme. The Model 1200 contains 22 Q-BUS positions arranged in a configuration that allows two dual height boards to be plugged in side by side. The relative positions in the backplane are identified as the AB and CD sides. In the Model 1200 all 22 slots are connected for the full 22 bit addressing. This is fully consistent with the use of the LSI-11/23.

A problem arises if a user is planning to employ an LSI-11/2 processor intermixed with other cards that are structured for 22 bit addressing. Digital Equipment Corporation had used the lines now configured for the four extra address bits for internal maintenance functions on the LSI-11/2. Therefore, it is mandatory that the extension address bits be disconnected on the individual controller cards. This is generally done with the use of jumpers on boards such as the controller card for the Model 830 floppy disk.

In instances where it is desirable to use the LSI-11/2 with 22 bit controllers, a solution has been implemented. ADAC has assigned Mod 204 to handle this rather unique combination. The essence of the Mod is to disconnect both the AB and the CD connections in slot 1 from the rest of the backplane. This is accomplished with seven etch cuts and three jumpers on the backplane. In the Mod 204 configuration position AB of slot 1 is reserved for the LSI-11/2 processor. The CD position of slot 1 can be used by any board that has a maximum of 18 bit addressing. All other 20 slots can be used by either 18 or 22 bit devices.

MOD 204

Cut etch between the following pins:	Add wire wrap jumpers between:
1B-C1 to 2B-C1	2B-C1 to 2D-C1
1B-D1 to 2B-D1	2B-D1 to 2D-D1
1B-E1 to 2B-E1	2B-E1 to 2D-E1
1B-F1 to 2B-F1	
1D-C1 to 2D-C1	
1D-D1 to 2D-D1	
1D-E1 to 2D-E1	


MODEL 1950 BUS REPEATER
C4-10074 REV I
adac corporation
MODE