COMPUTER DESIGN (2)

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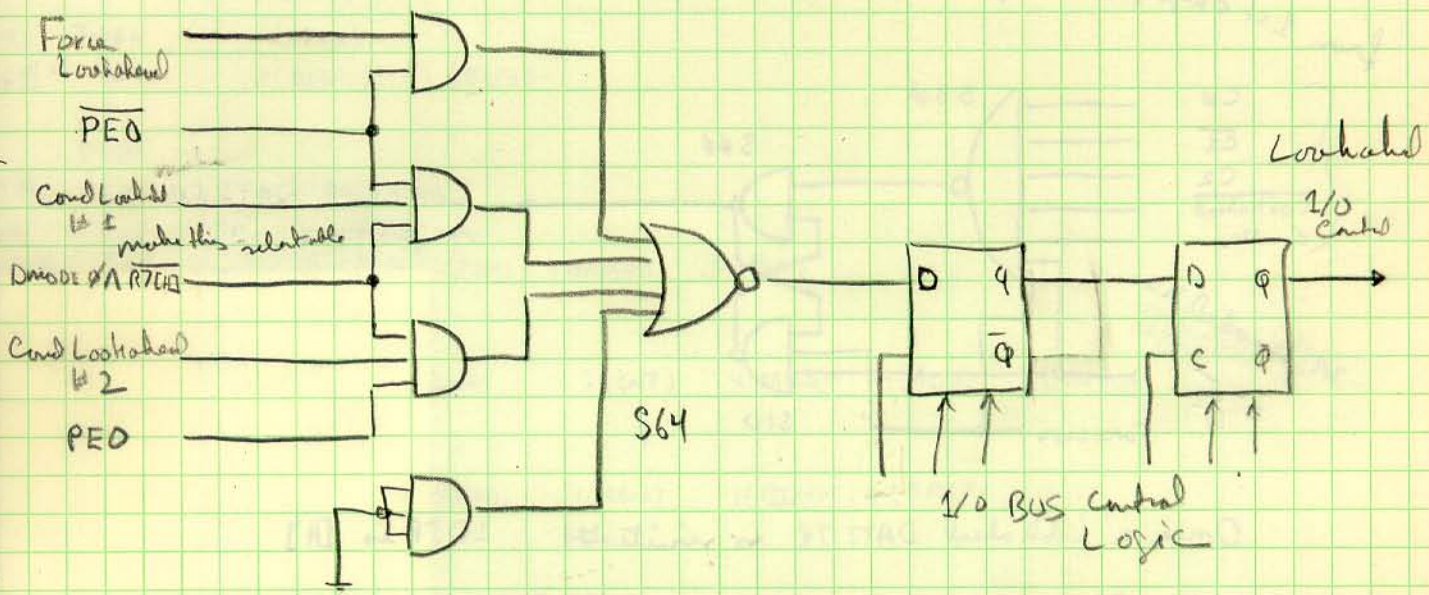
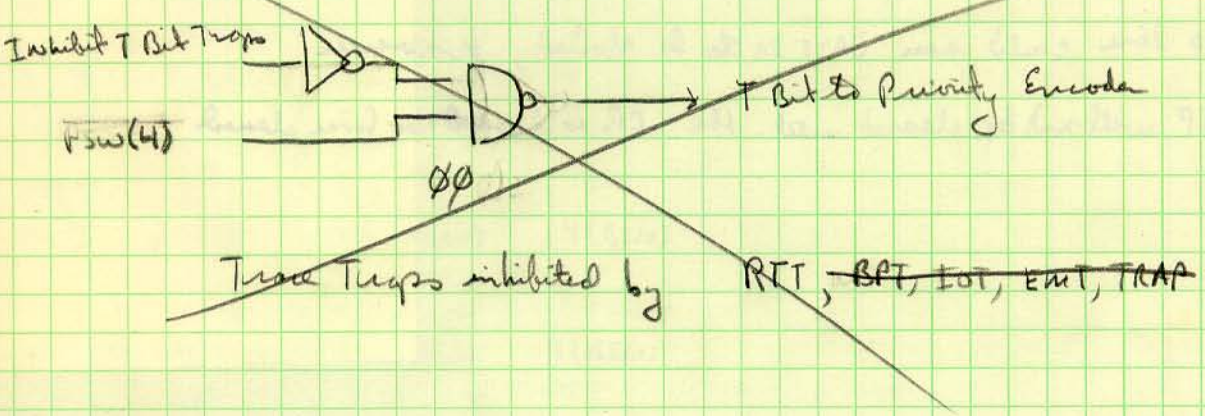
(7 June -

DATI IR Lookahead Enables

Add 3 Lookahead lines to IR Decode PROM



T Bit Logic

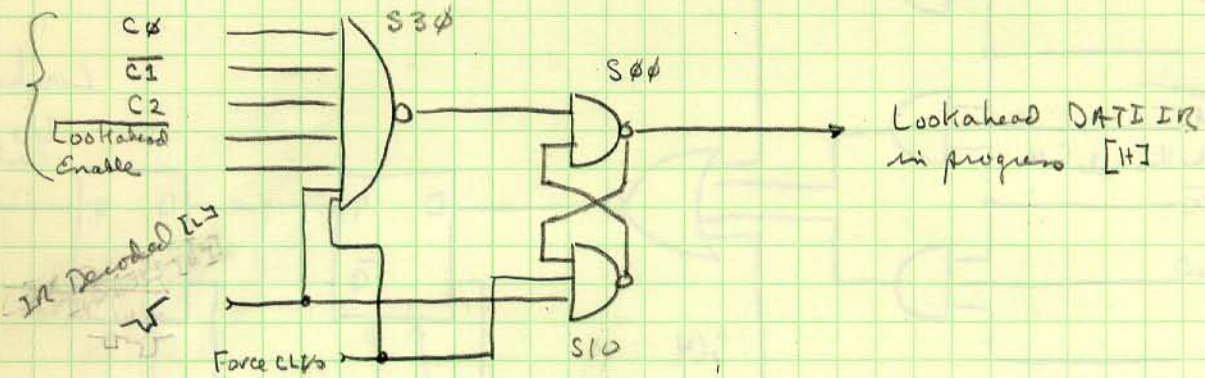


7 June 1976
ARD

Added Logic for Branch Control / Signal indicating Lookahead DATI IR is in progress

Circuitry Added to I/O Logic

from 1st stage I/O Buffers



Once a Lookahead DATI IR is initiated LDIP is [H] until the I/O operation is completed or some Bus / Force Errors will automatically clear the LDIP Flip/Flop

NDSP line could cause DATI IR to be aborted, however LDIP will not be cleared until the IR is loaded or force cleared

Integrated Circuit estimates

(10)	7400	1(INTR)	1(CLK)	2(BI/O)	1(PRI)			
30AJ ✓	S00	1(BYPOP)	2(INTR)	3(INT)	4(IRDCO)	2(MCNTL)	1(CLK)	3(CNTR)
10AJ ✓	L00	1(INTR) 1(PRI)	1(CLK)	3(BI/O)	7(BI/O)	2(PRI)		
(4)	7402	1(IRDCO)						
5E ✓	S02	2(MCNTL)	1(BI/O)					
	7404							
(3)	7405	2(SOR)						
(10)	7408	7(PRI)						
10A ✓	S08	1(CPU RC)	1(PSW)	1(IRDCO)	3(CLK)			
	7410							
20AJ ✓	S10	2(ADD)	1(INTR)	2(INT)	4(IRDCO)	4(BI/O)	3(PRI)	
	7411							
10AJ ✓	S11	2(INT)	4(IRDCO)	1(DRDS)	1(BI/O)	1(PRI)		
40D ✓	7416	40(FPNL)						
40D	7417	40(FPNL)						
(2)	7420	1(BI/O)						
10AJ ✓	S20	1(ADD)	2(NPR)	1(INT)	1(IRDCO)	1(MCNTL)	2(BI/O)	
2A ✓	L20	1(BI/O)						
	7421							
5A ✓	S21	1(IRDCO)	1(PRI)					
	7430							
10A	S30	1(INTR)	1(CNTR)	4(BI/O)				
(2)	7432	1(CLK)						
10A ✓	S32	2(INTR)	2(PSW)	1(BI/O)				
(10)	7438	1(INTR)						
10A ✓	7442	1(INT)	4(PRI)					
	Am2909	3(Micro Control)						
	Am2901	4(CPU)						

(3)	7451	1 (BrkOP)	1 (BR67 Ds)					
	S51							
~~3A~~ 4J ✓	S64	1 (BI/O)	1 (LHAD)					
25E ✓	74174	1 (IRLoad)	1 (CLK)	1 (BIO)	13 (PRI)			
	S74	1 (CNTR)	2 (PRI)					
(3)	7483	2 (CNTR)						
(4)	7486	1 (IRDCD)						
	S86	1 (CPUS/R)	1 (Carry IN)					
~~8~~D ✓	7489	8 (VCTR)						(12)
(6)	74123	1 (IRLoad)	1 (BI/O)					50J
	74125	1 (IRDCD)	4 (DBUS)					
	74126	1 (IRDCD)						150E ✓
	74S133	3 (CPUCode)						
~~3A~~	74S138	1 (IRDCD)						
8D ✓	74148	1 (INT)	2 (IRDCD)	3 (PRI)				
25E ✓	74150	16 (CPUIS)	1 (IRDCD)	4 (CCD)	9 (IRDecode)			
(8)								
5E ✓	74151	1 (Carry IN)						
5~~3~~A ✓	S151	3 (PRI)						
10D ✓	74153	8 (Acc ADD)						
4~~5~~J ✓	S153	~~2 (PRI)~~						
	74154							
20E ✓	74157	4 (IRDCD)	8 (DBUS)		2 (PSW)			
5A ✓	S157	1 (CPU CC)	1 (Bytes OP)	5 (MMGT)	1 (PSW)	1 (IRDCD)	1 (Carry Prop)	
10E ✓	74S172	4 (CPU)						
10E ✓	74174	6 (FAIL)						
25E ✓	74175	6 (BADD)	2 (SLR)		3 (PSW)	11 (MCDR)		
30E ✓	S175	3 (INT)	3 (IRDCD)	2 (MCNTL)	4 (DBUS)	2 (CNTR)	6 (BI/O)	3 (PRI)
				5 (MCDR)				
5A ✓	74S251	5 (CPUSR)						
5E ✓	74S257	4 (PSW)						

74366 ③

total as of 8 June 360 IC's

			W/W	Solder
~25	24 pin		30 D ✓	20 J ✓
~ 3	28 pin		3 D ✓	
~ 4	40 pin	(40 antennas)	40 D ✓	40 J ✓
~330	16 pin		500 D	

(12) 8838

7

50 J ✓ 74S48

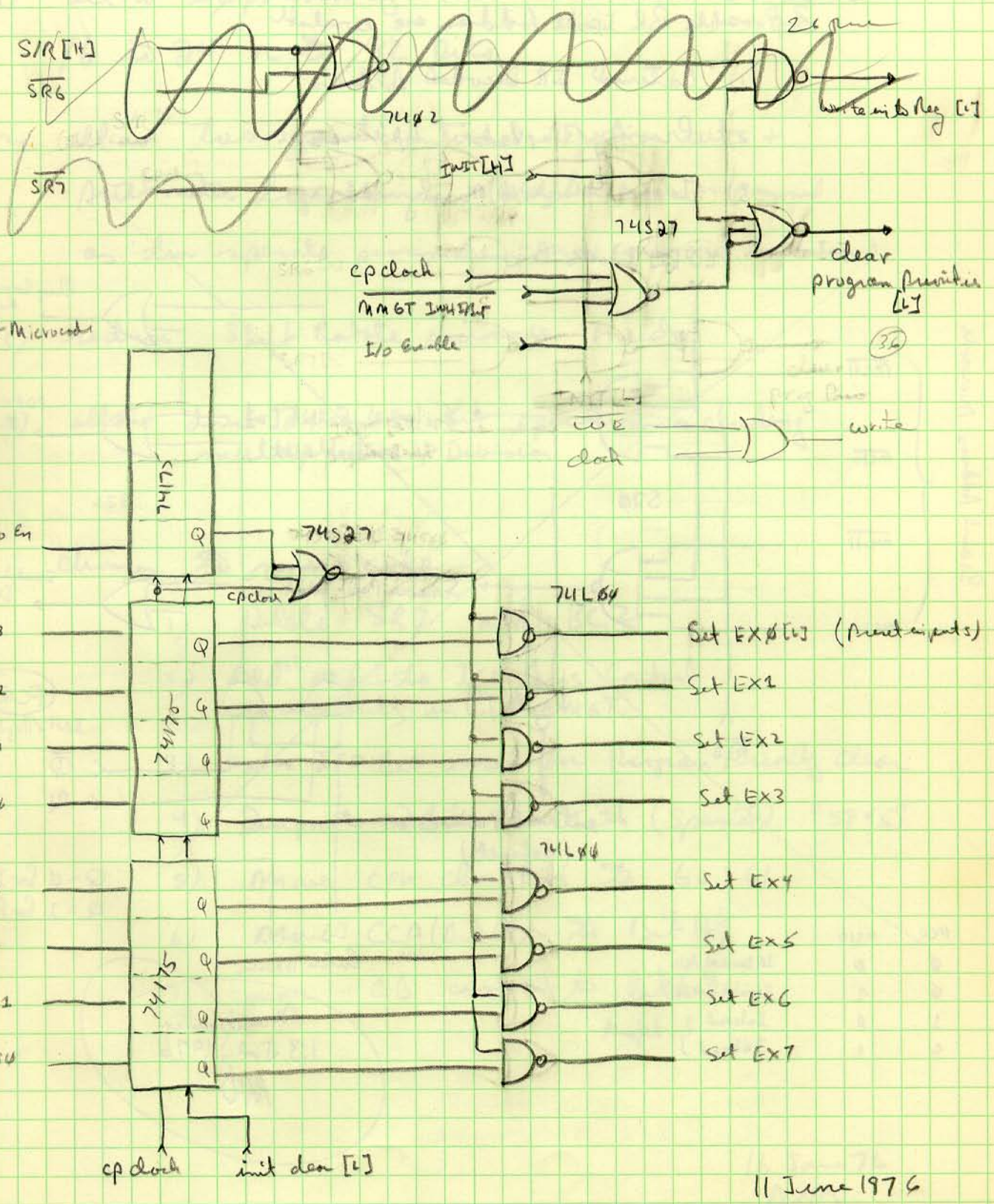
150 E ✓ 74S37

( ) indicate from Physics

D ordered from Digi Key
E ordered from Eltron
A ordered from Ancrona
J ordered from Jameco

✓ received

Clear / Set Program Flow Priorities and inter flow Registers



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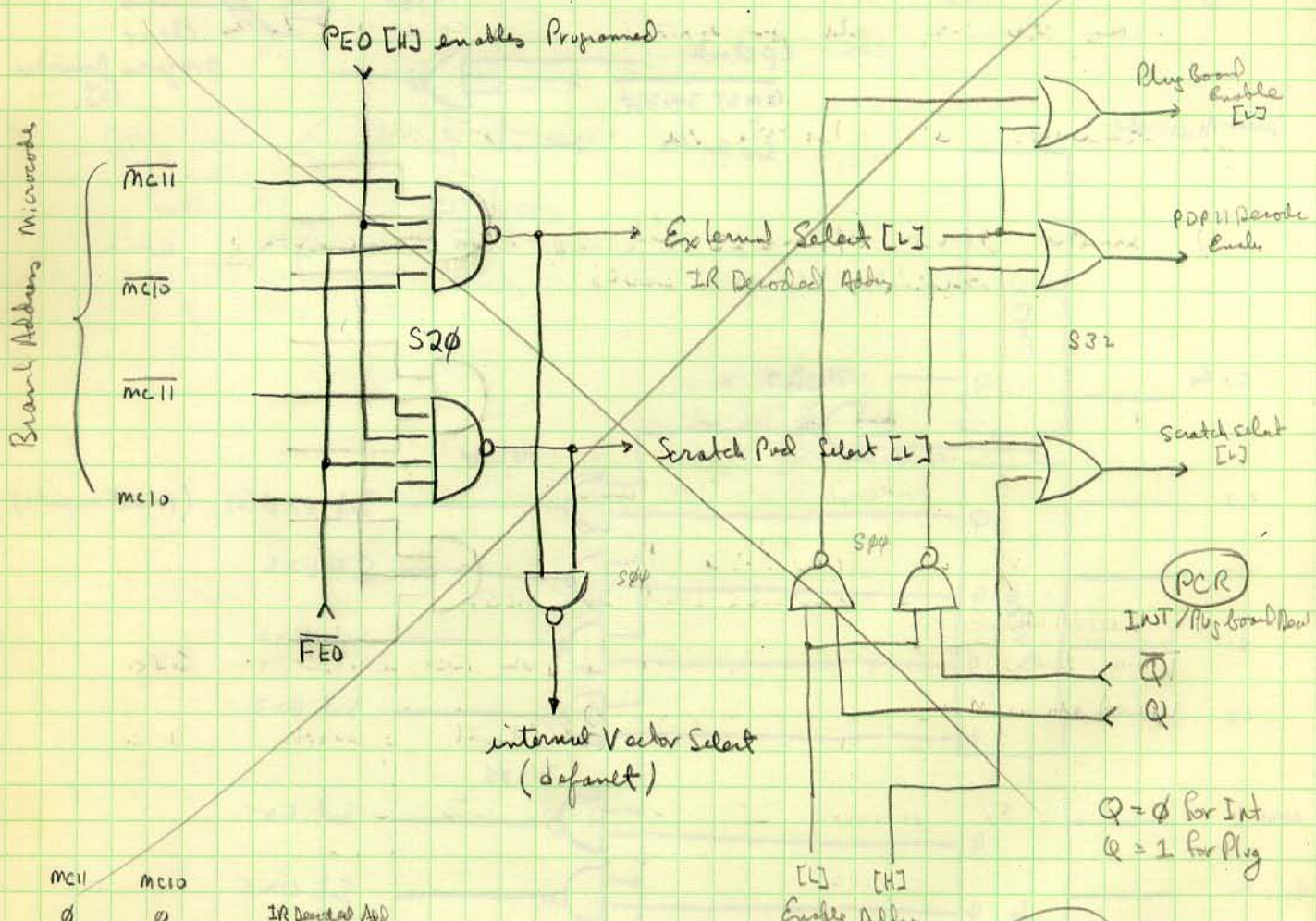
Programmed BR Icode Address Sector

3 possible BR Icode Addresses are available

1) External IR Decoded Address
2) Priority/TrapVector Addresses
3) Internal ScratchPad Memory Address



MC11	MC10	
ϕ	ϕ	IR Decoded Add
ϕ	1	Scratch Pad Add
1	ϕ	Internal } default
1	1	Internal]

Model Circuitry
13 July 1976
ABD

Redesign of Main Processor to

1) allow expansion of Processor Word length from 16 to 24 or to 32 bits

2) allow two seperate internal Register sets + Arithmetic logic units (may be microprogrammed as two seperate processors - non concurrent execution)

3) reduce Shift Rotate microcode needs

4) allow direct 24 and 32 bit operations including multiplication + Division

changes to micro code

1) Delete SR7 add BC2
2) add a bit to I/O Bus control to explicitly initiate MM6T
3) extra I/O Bit used for Program Priority clear
4) Designate 2 Bits for Math (Special) #58:59
5) Move CPU clock Bits to 60:61
6) Move CCA (Bit 61) to Bit 95
7) move CB console bit to Bit 69

16 June 76
ARD

Processor Control (Processor segments not selected are coded for NO OP's)

Microcode Bits

	BC2	BC1	BC0			
0	0	0	0	LB <07:00>	Byte Operation Low Processor Word	1
1	0	0	1	LW <15:00>	Word Operation Low Processor Word	1
2	0	1	0	UB <23:16>	Byte Operation Upper Processor Word	0
3	0	1	1	UW <31:16>	Word Operation Upper Processor Word	0
4	1	0	0	LW <15:00>/LB <07:00>	Conditional Word/Byte Low Processor Word	1
5	1	0	1	UW<31:16>/UB<23:16>	Conditional Word/Byte Upper Processor Word	0
6	1	1	0	3B <23:00>	24 Bit Processor Operation	1
7	1	1	1	4B <31:00>	32 Bit Processor Operation	1

B1D - Byte 1 Disable [L]
B2D - Byte 2 Disable [L]
B3D - Byte 3 Disable [L]
B4D - Byte 4 Disable [L]

S0, S1 } Processor Status Selects

UPWO Upper Word Only enable [L], also controls CPUO Tristates

A	UB/24 Bit	Down shift enable [L]	I7 = 0 for Down shift
B	LW	Down shift enable [L]	I7 = 1 for Up shift
C	UW	Up shift enable [L]	
D	LB	Down shift enable [L]	

output control states

B1D	B2D	B3D	B4D	S1	S0	fast UPWD	A	B	C	D	CPUZ
1	ϕ	ϕ	ϕ	ϕ	ϕ	1	1	1	1	I7	ZLB
1	1	ϕ	ϕ	ϕ	1	1	1	I7	1	1	ZLW
ϕ	ϕ	1	ϕ	1	ϕ	ϕ	I7	1	$\overline{I7}$	1	ZUB
ϕ	ϕ	1	1	1	1	ϕ	1	1	$\overline{I7}$	1	ZUW
1	$\overline{Byte[H]}$	ϕ	ϕ	ϕ	$\overline{Byte[H]}$	1	1	I7	1	I7∧Byte[H]	CPUZ'
ϕ	ϕ	1	$\overline{Byte[H]}$	1	$\overline{Byte[H]}$	ϕ	I7∧Byte[H]	1	$\overline{I7}$	1	CPUZ'
1	1	1	ϕ	1	ϕ	1	I7	1	1	1	Z3B
1	1	1	1	1	1	1	1	1	1	1	Z4B

S1	S0	CPUC	CPUV	CPUN	CPUZ'	CPUNor MSBR R<>	MSBQ Q<>
ϕ	ϕ	C_8	V_8	N_8	ZLB	R<7>	Q<7>
ϕ	1	C_{16}	V_{16}	N_{16}	ZLW	R<15>	Q<15>
1	ϕ	C_{24}	V_{24}	N_{24}	ZUB	R<23>	Q<23>
1	1	C_{32}	V_{32}	N_{32}	ZUW	R<31>	Q<31>

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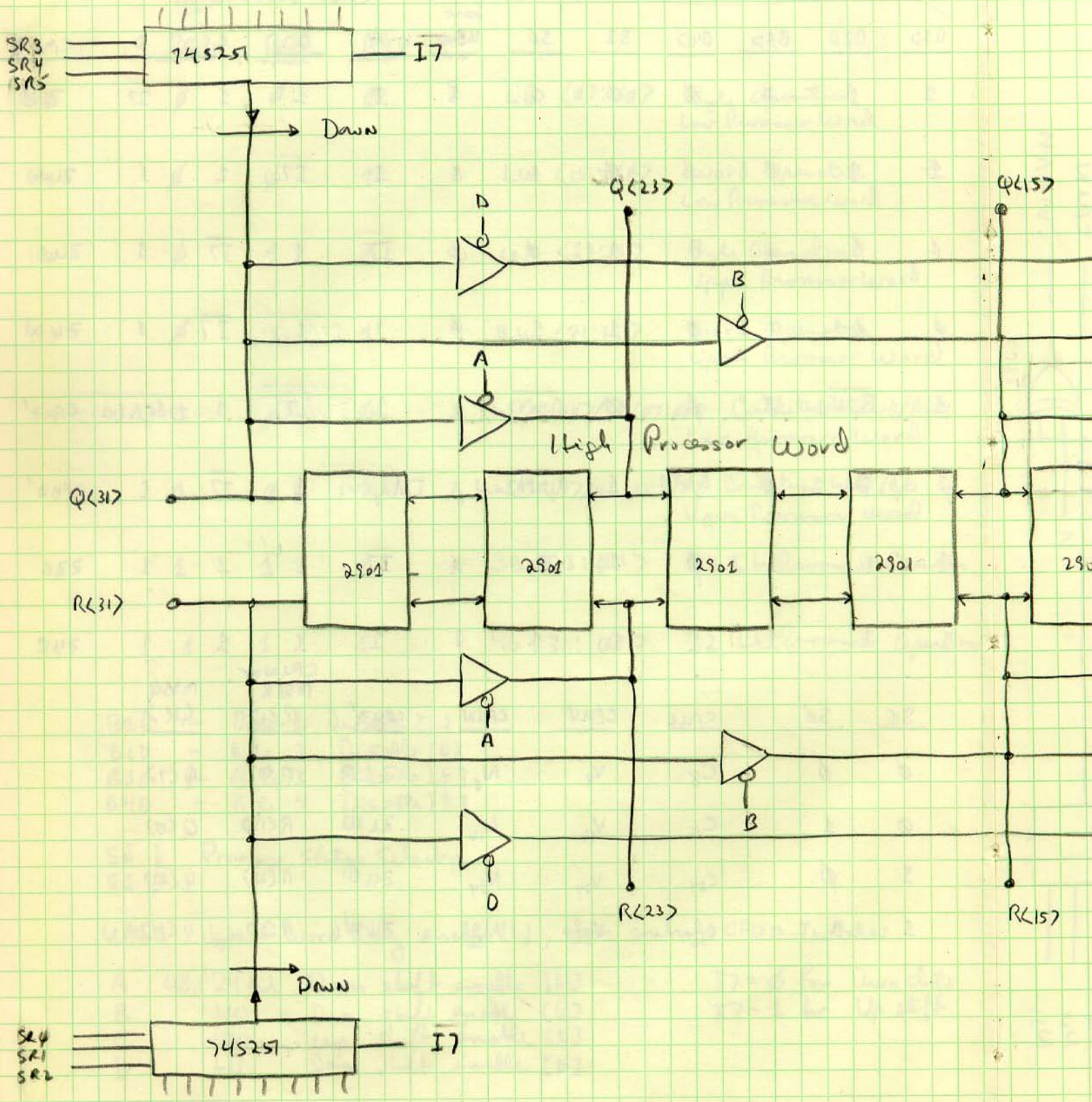
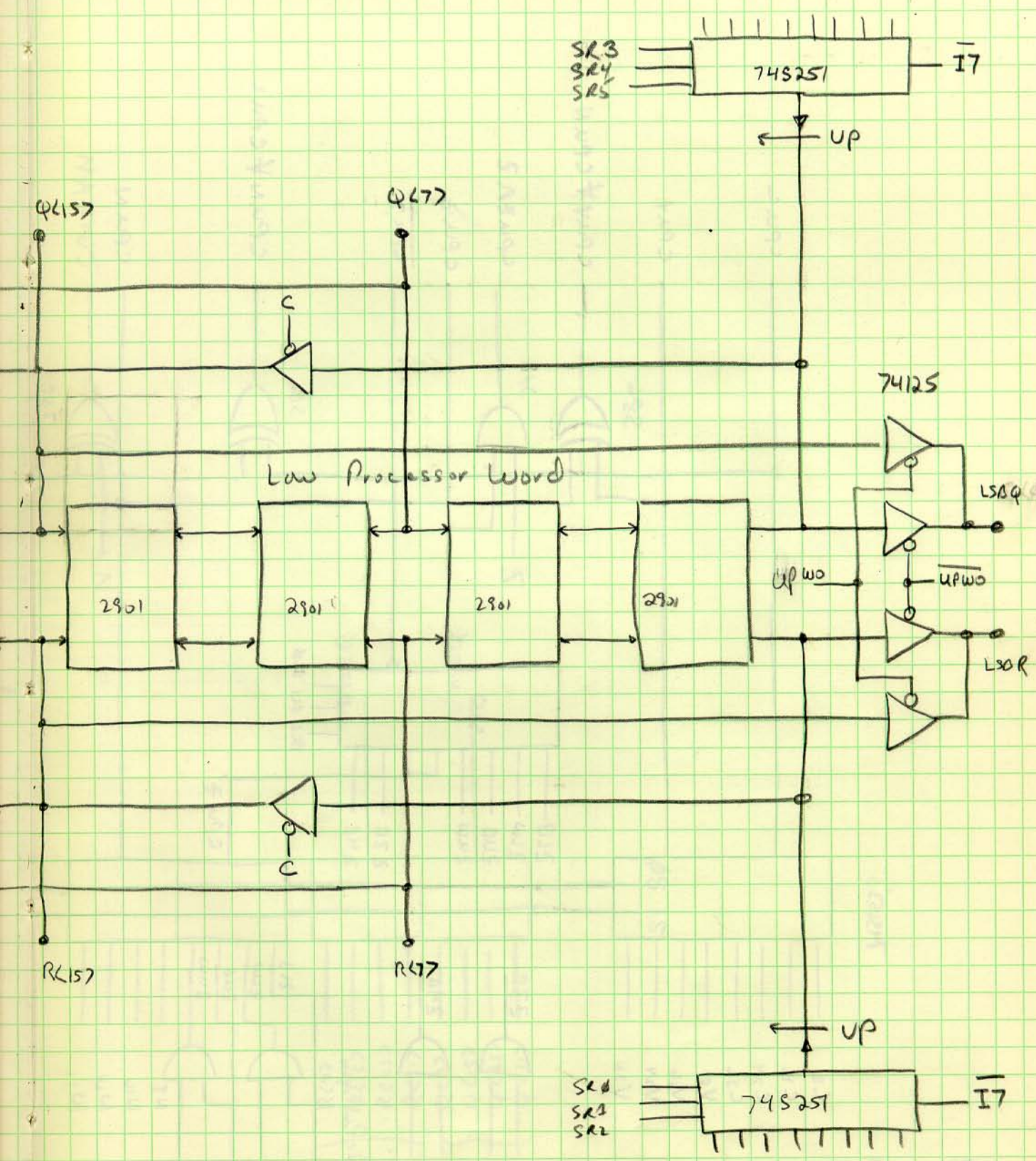
ARS

Processor Shift Ratate Logic





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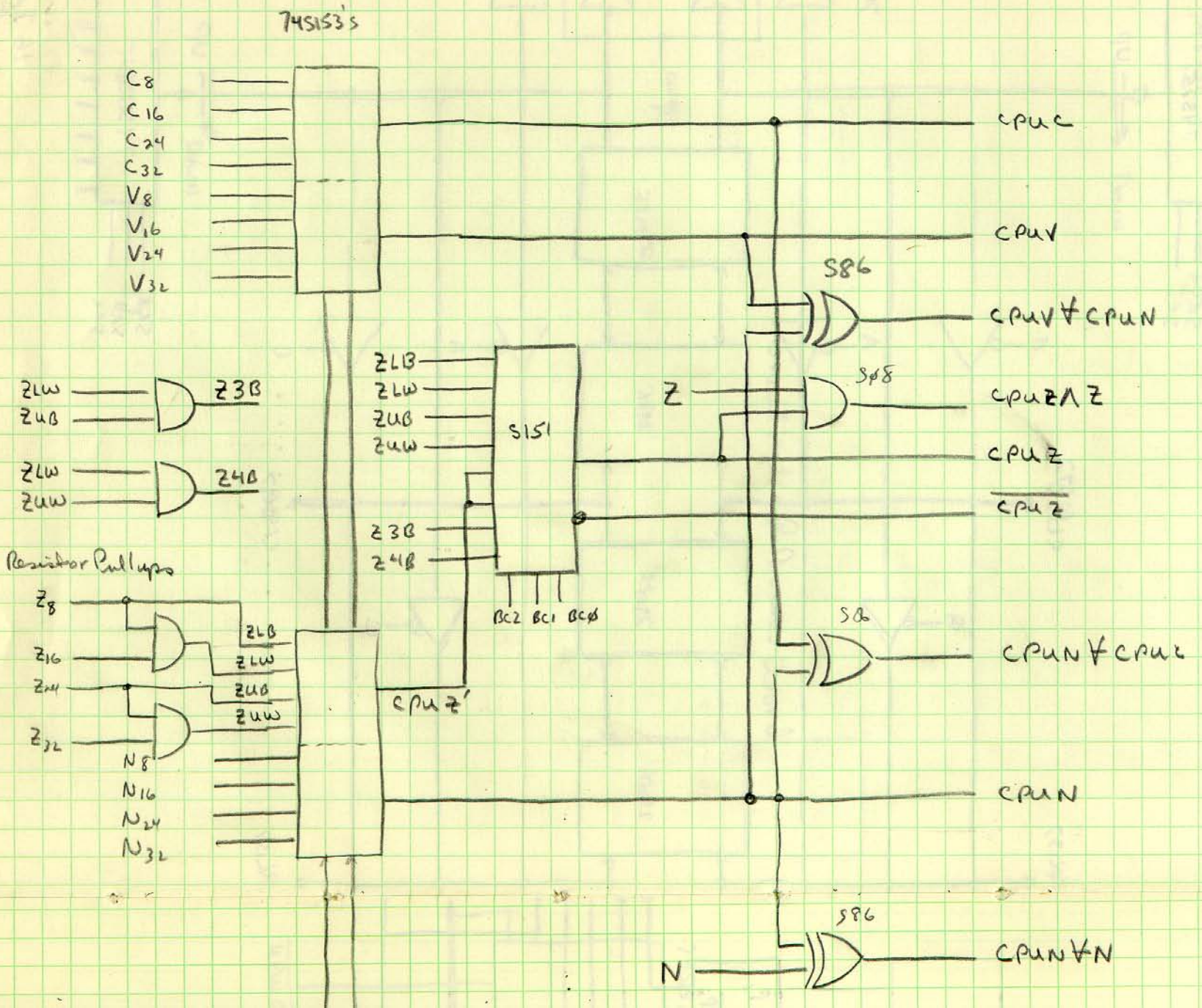
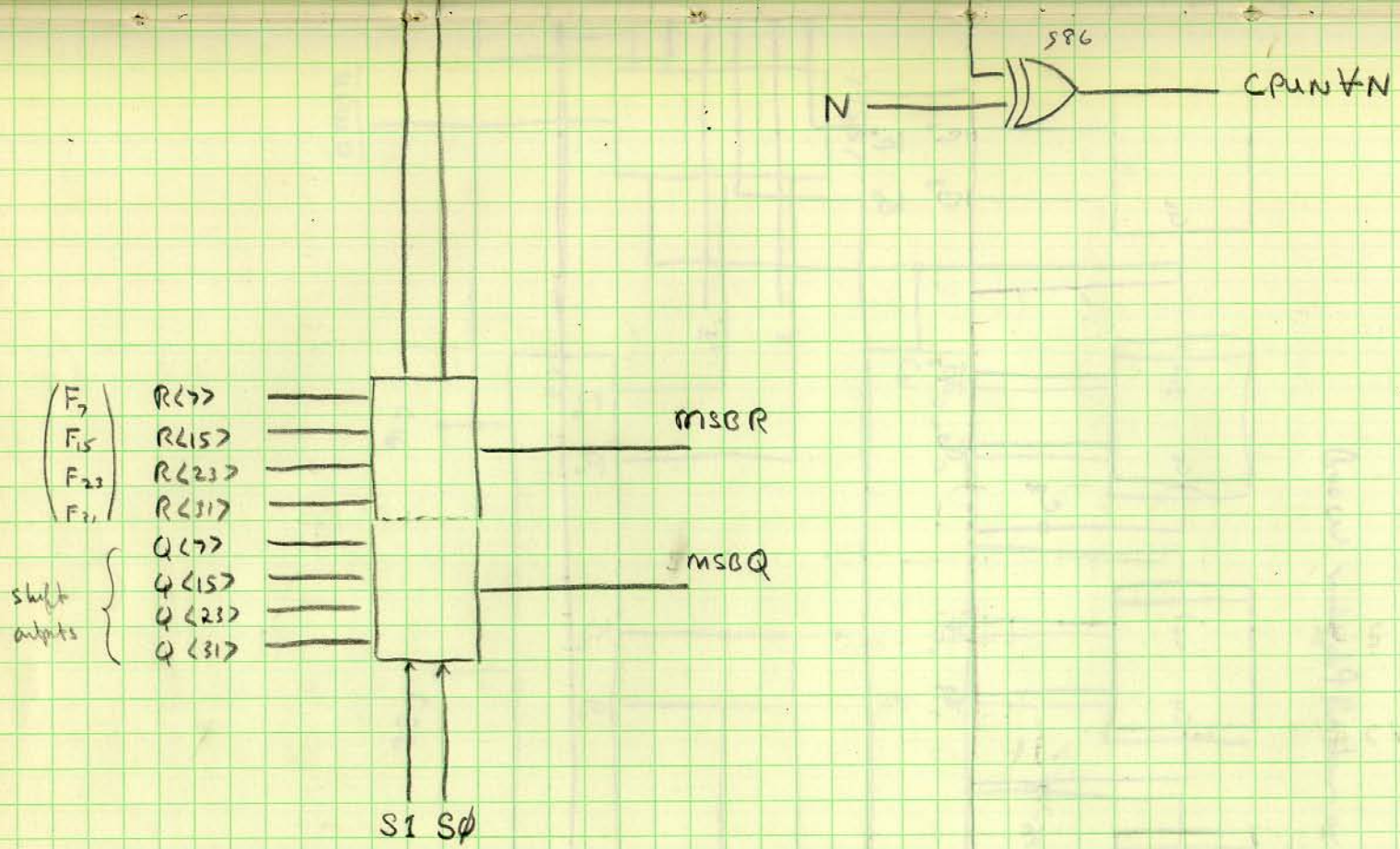
Processor Status Control





CWD
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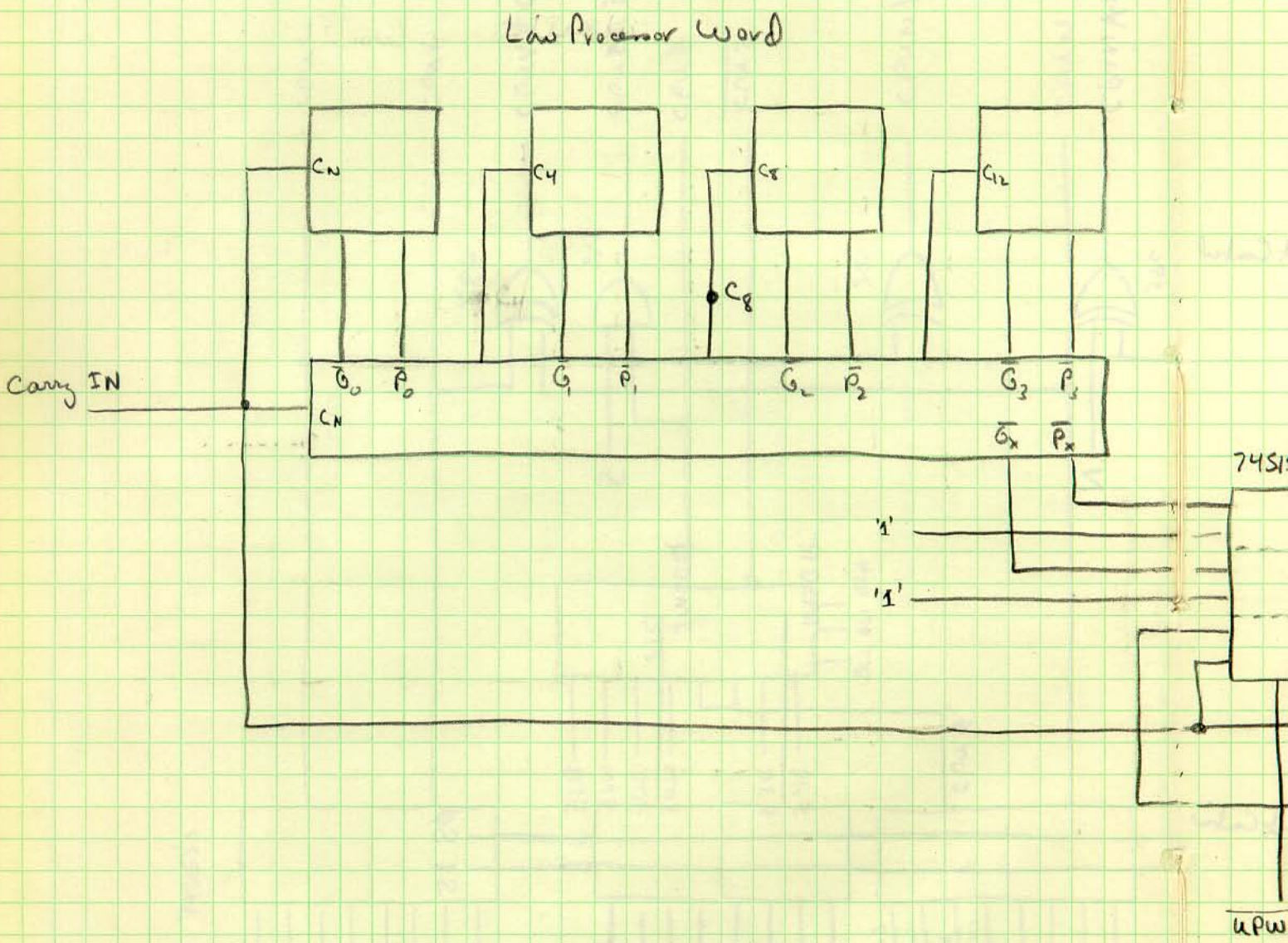
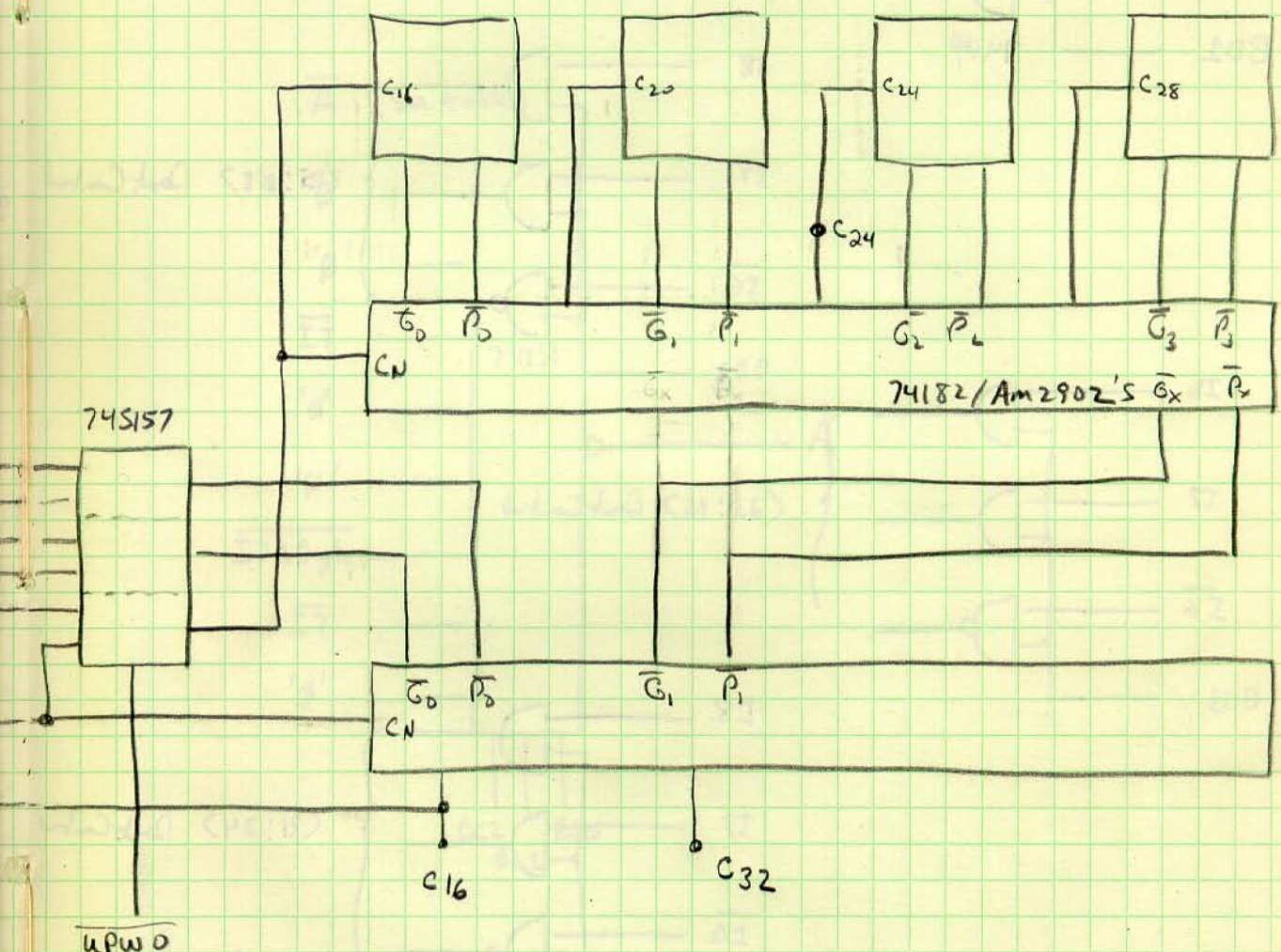
Processor Carry Generation



High Processor Word



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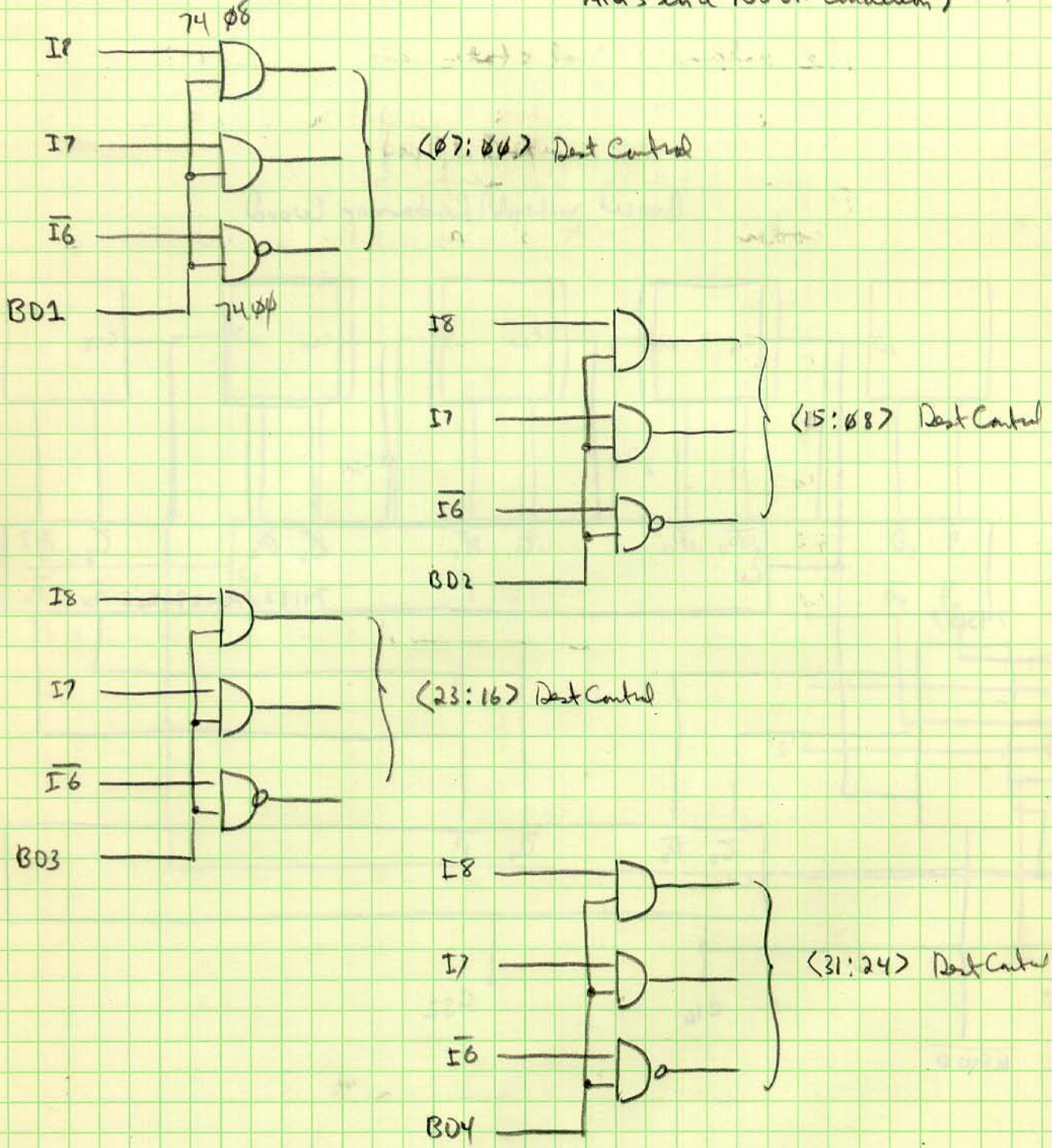
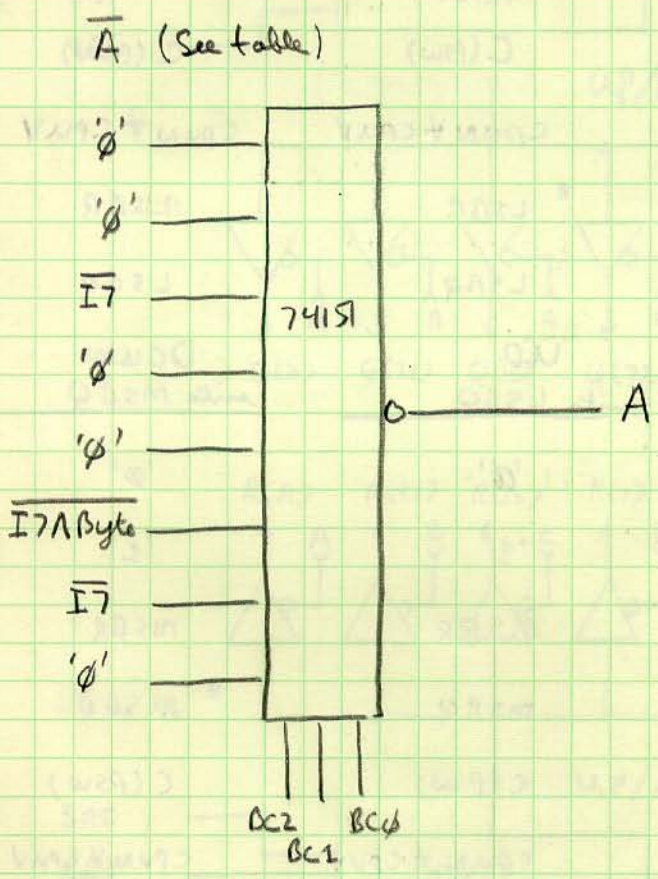
Processor Byte Disable Logic (any BDx [L] places related ALU's in a NO OP condition)



Output Control State generation

The output control states are generated by using one of 8 selectors coded by BC2, 1, Ø -
a typical coding is given for A -
(all coders are 74151's except for UPWO - 74S151)



Notes: Code S1 is identical to B3D
Code B1D is identical to UPWO
total of 9 coders required!

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Shift/Rotate Selects

SR2	SR1	SR0	UP into LSBR	DOWN into MSBR
0	0	0	'0'	'0'
0	0	1	'1'	'1'
0	1	0	MSBR	MSBR
0	1	1	MSBQ	MSBQ
1	0	0	C(PSW)	C(PSW)
1	0	1	CPUN ⊕ CPUV	CPUN ⊕ CPUV
1	1	0	* LSBR	LSBR
1	1	1	LSBQ	LSBQ

SR5	SR4	SR3	UP into LSBQ	DOWN into MSBQ
0	0	0	'0'	'0'
0	0	1	'1'	'1'
0	1	0	MSBR	MSBR
0	1	1	MSBQ	* MSBQ
1	0	0	C(PSW)	C(PSW)
1	0	1	CPUN ⊕ CPUV	CPUN ⊕ CPUV
1	1	0	LSBR	LSBR
1	1	1	* LSBQ	LSBQ

* indeterminate states

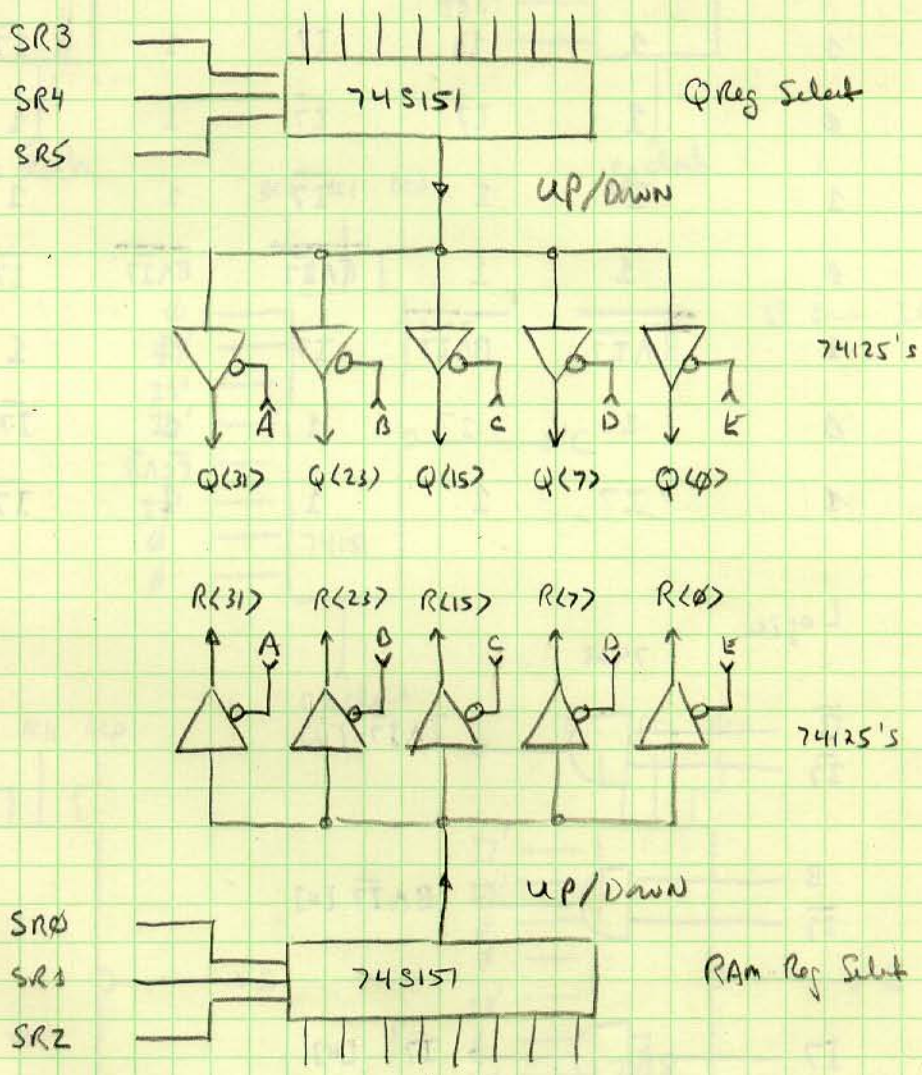
MSBR are direct F states

Simplified designs the Shift Rotate selectors

1) reduces Selectors from 4 (74S251's) to 2 (74S157's)

2) ensures tristates are never simultaneously enabled

Notes: Replaces Logic on page 7 & Control states A, B, C, D on page 6



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ARD

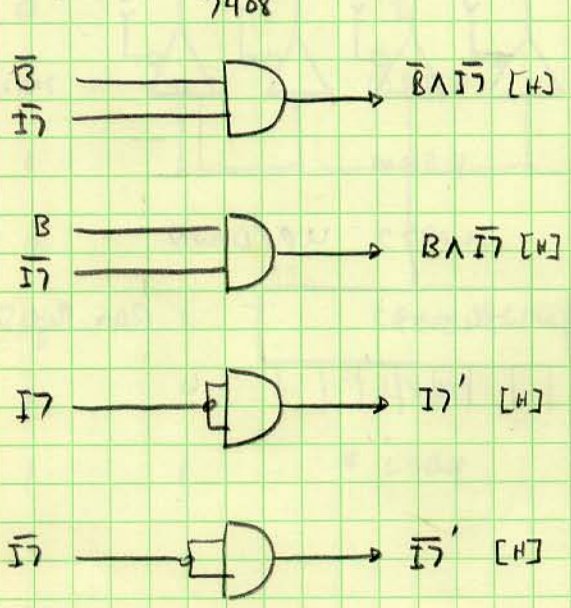
Down = $\overline{I7}$/[L]
Up = I7/[H]

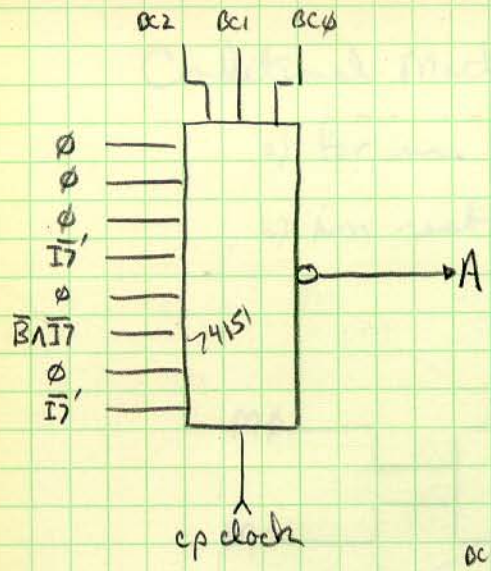
Tristates enabled by [L]
output states (input states are inverses)

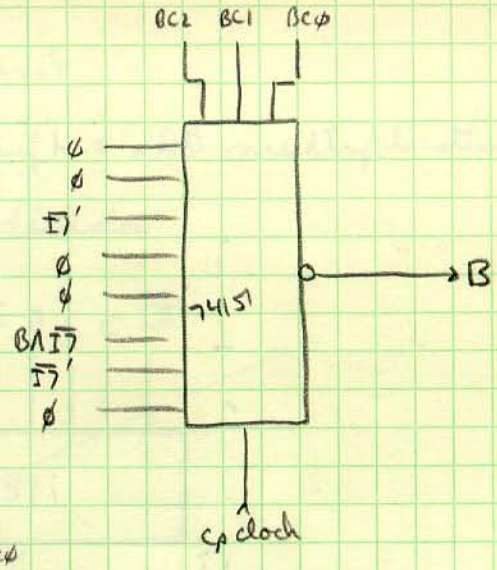
BC2	BC1	BC0	A	B	C	D	E
0	0	0	1	1	1	I7	$\overline{I7}$
0	0	1	1	1	I7	1	$\overline{I7}$
0	1	0	1	I7	$\overline{I7}$	1	1
0	1	1	I7	1	$\overline{I7}$	1	1
1	0	0	1	1	$\overline{B \wedge I7}$	$\overline{B \wedge I7}$	$\overline{I7}$
1	0	1	$\overline{B \wedge I7}$	$B \wedge \overline{I7}$	$\overline{I7}$	1	1
1	1	0	1	I7	1	1	$\overline{I7}$
1	1	1	I7	1	1	1	$\overline{I7}$

Logic

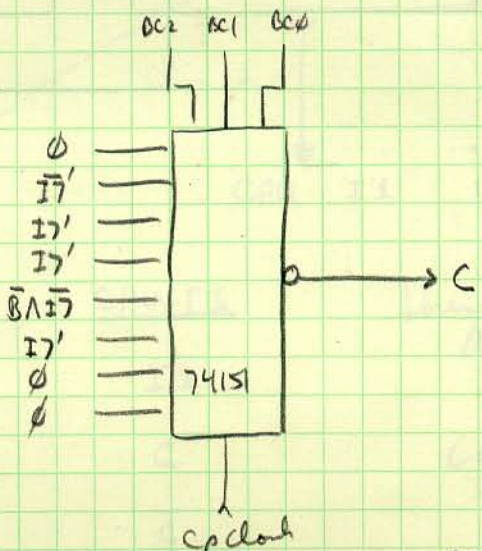
7408

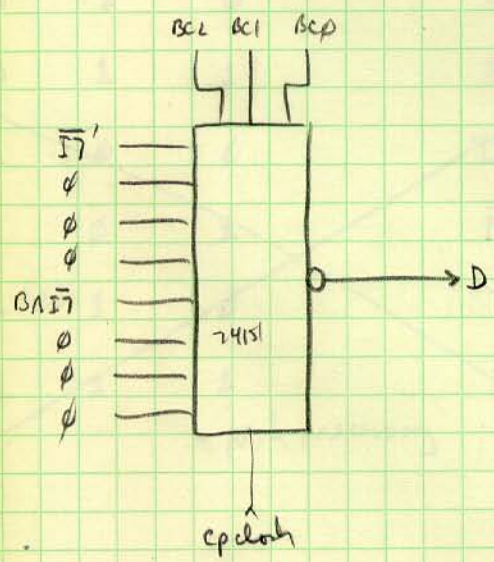


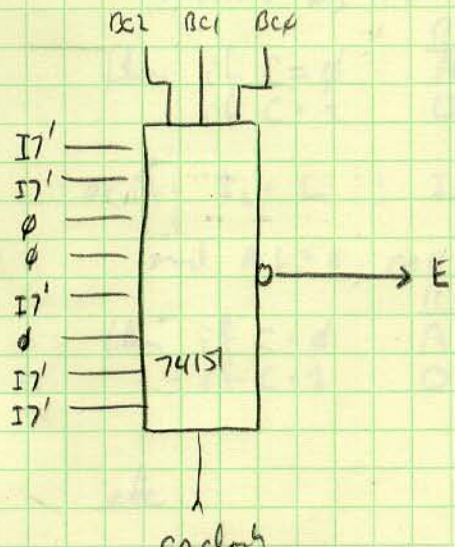




B from IR Decoding





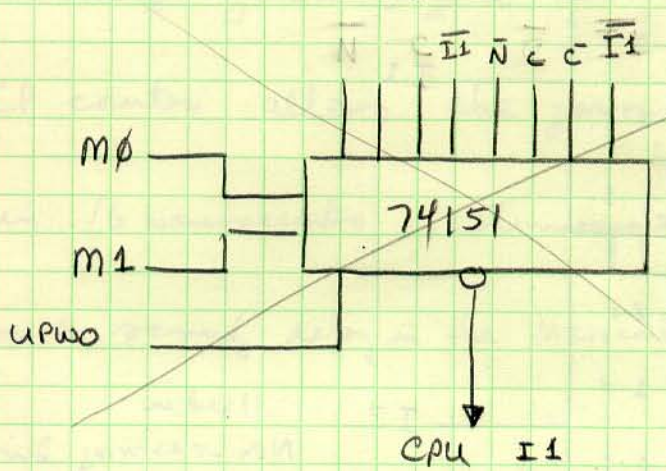


17 June 1976
AFD

Conditional Math control

a) for use in shift & add multiplication

b) non restoring division



UPWO	M1	M∅	CPU I1
∅	∅	∅	I1
∅	∅	1	C
∅	1	∅	$\overline{C}$
∅	1	1	$\overline{I1}$
1	∅	∅	I1
1	∅	1	N
1	1	∅	Z
1	1	1	$\overline{Z}$

Not necessary

these conditionally alter the ALU Source Operands

ie for $I_2 = L$; $I_0 = L$

and M1 = ∅; M∅ = 1

	R	S
then if C = ∅	A	Q
if C = 1	0	Q

or if $I_2 = L$; $I_0 = H$

and M1 = ∅; M∅ = 1

	R	S
then if C = ∅	A	B
if C = 1	0	B

etc.

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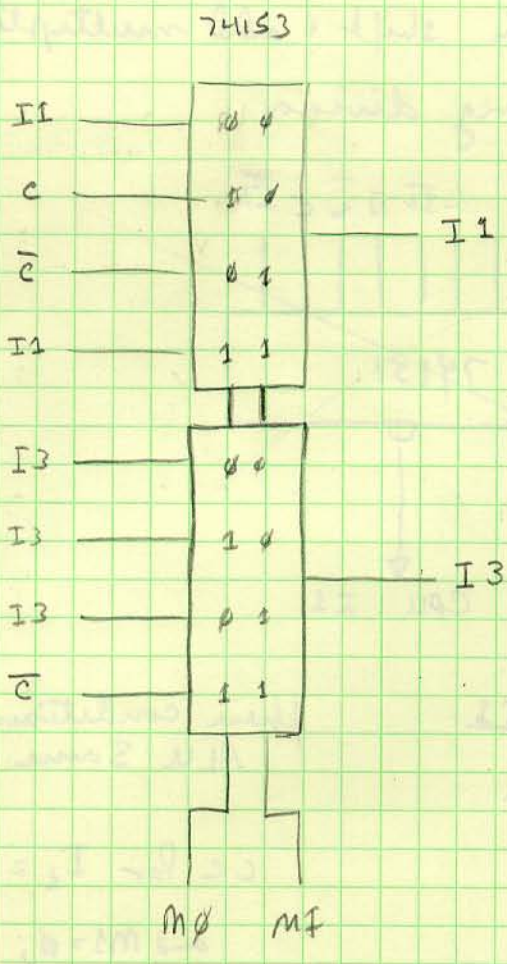
ARB

Modified Conditional Math Control

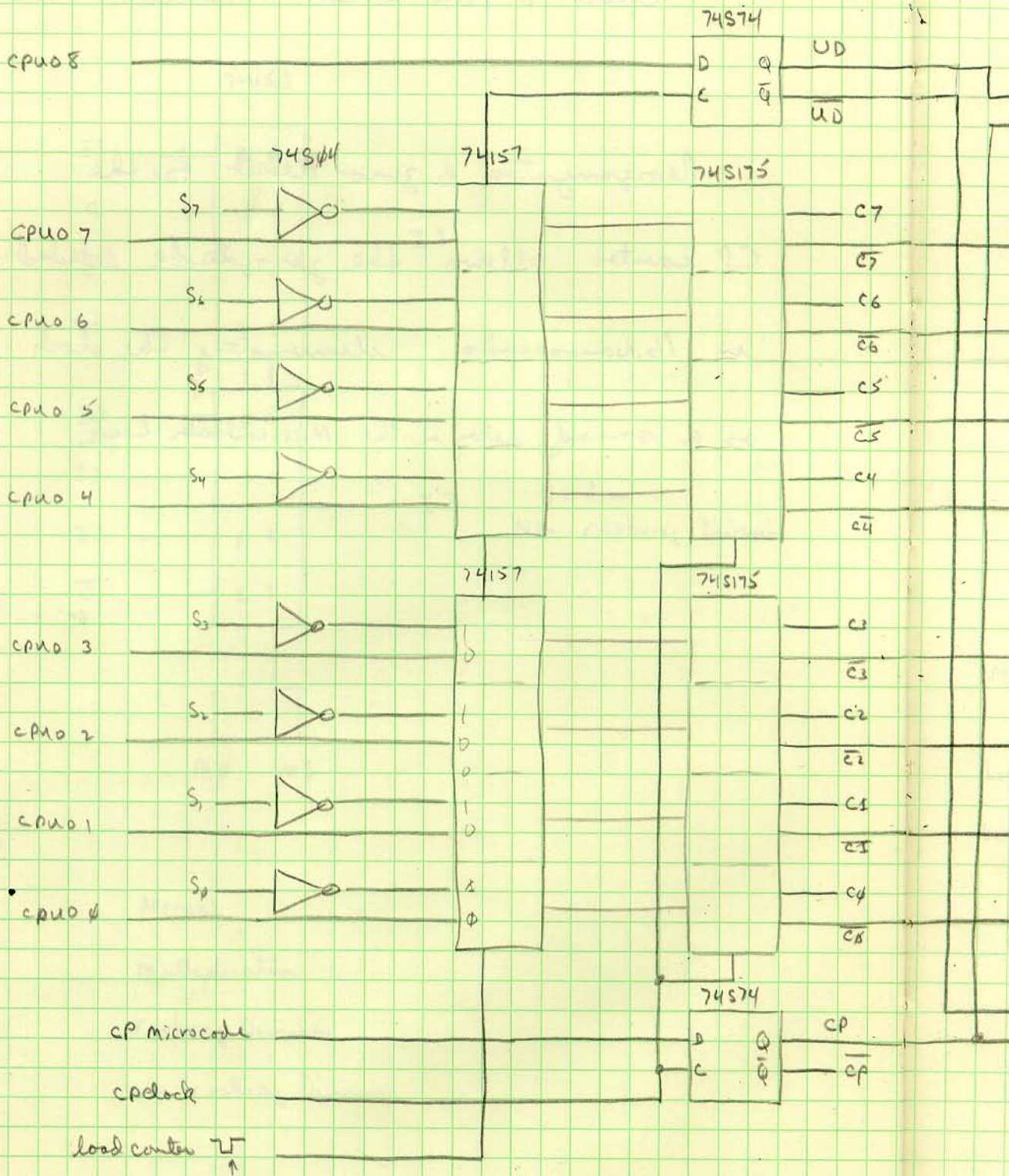


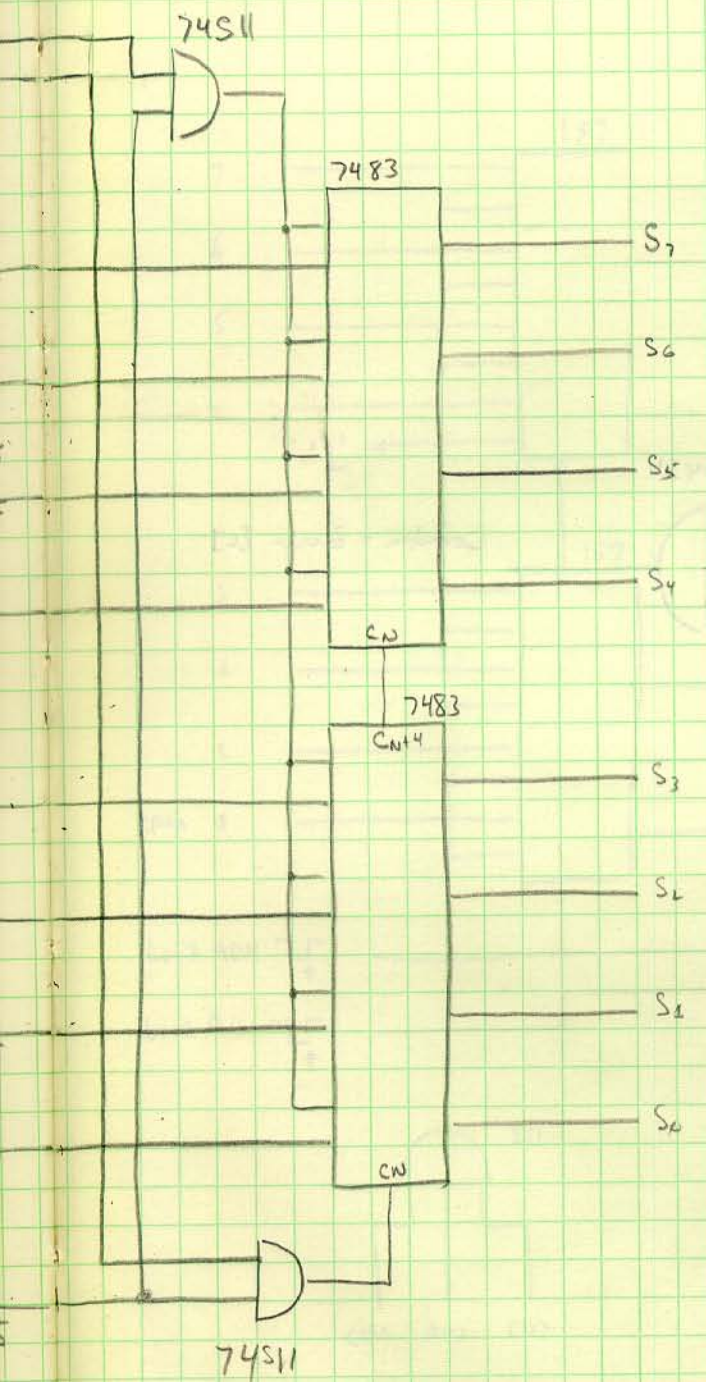
Used in
Non-restoring Division

M1	M0	
0	0	Normal
0	1	Multiplication
1	0	restoring Division
1	1	Non-restoring Division

Speed up of the CP counter zero detection logic

Reorganization of zero detect for the CP counter allows the zero to be detected in 16 nanoseconds, eliminating the clock as a source of delay in the Microcontroller logic


74S74
CPU0 8
D
C
Q
$\overline{Q}$
UD
$\overline{UD}$
74S04
74157
74S175
S_7
CPU0 7
S_6
CPU0 6
S_5
CPU0 5
S_4
CPU0 4
C7
$\overline{C7}$
C6
$\overline{C6}$
C5
$\overline{C5}$
C4
$\overline{C4}$
74157
74S175
S_3
CPU0 3
S_2
CPU0 2
S_1
CPU0 1
S_0
CPU0 0
C3
$\overline{C3}$
C2
$\overline{C2}$
C1
$\overline{C1}$
C0
$\overline{C0}$
74S74
CP microcode
cpclock
load counter
CP
$\overline{CP}$



to CPU IS

$\phi\phi \xrightarrow{I} 11$
$+ \quad 11$
$01 \quad C \xrightarrow{I} 10$ decrement

$10 \rightarrow \phi 1$
$+ \quad 11$
$10 \quad C \xrightarrow{I} 01$ count

$\phi\phi \rightarrow 11$
$+1$
$0\phi \quad C \rightarrow 11$ decrement

$11 \rightarrow \phi\phi$
$+1$
$10 \xrightarrow{I} 01$ decrement

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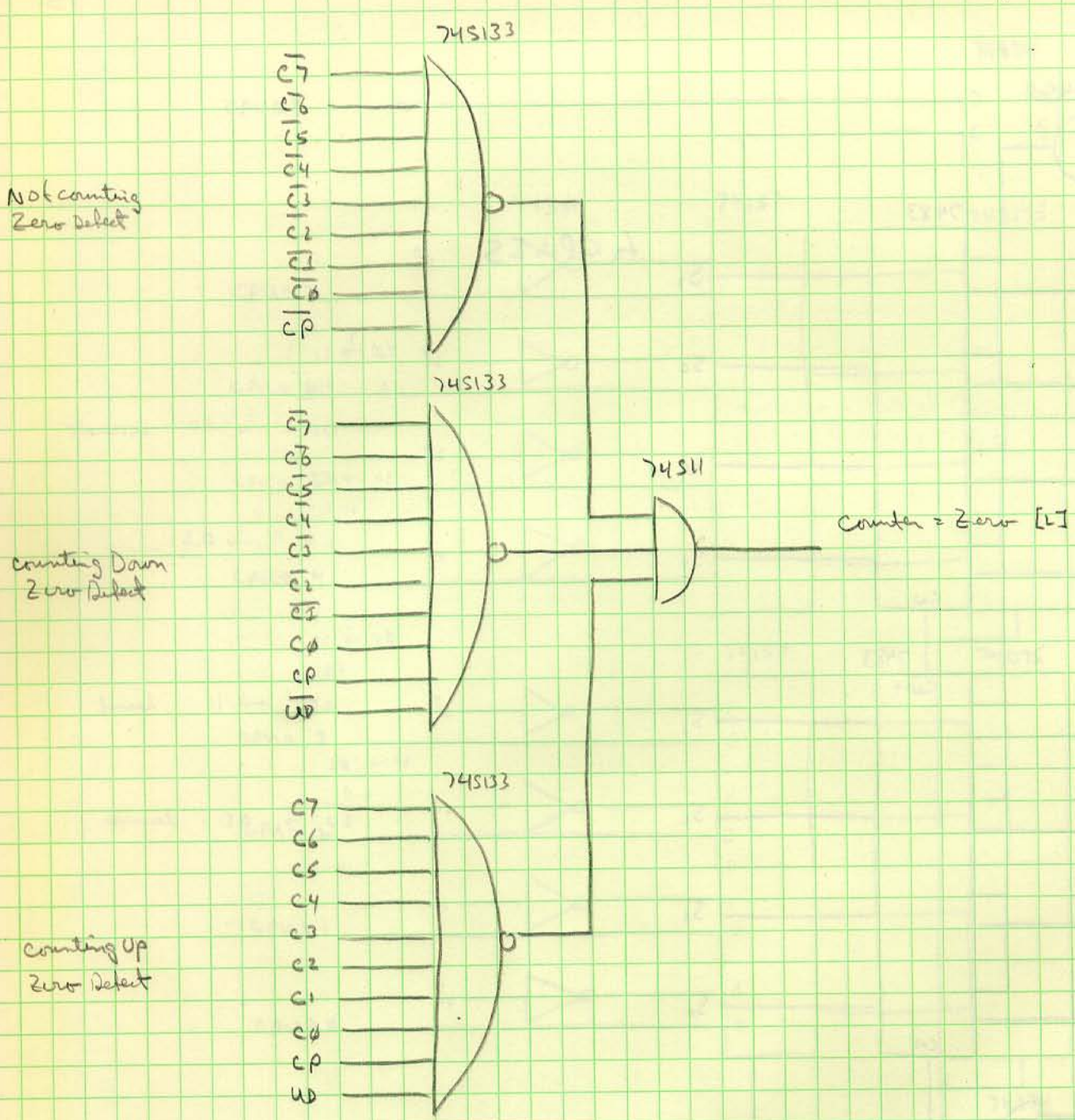
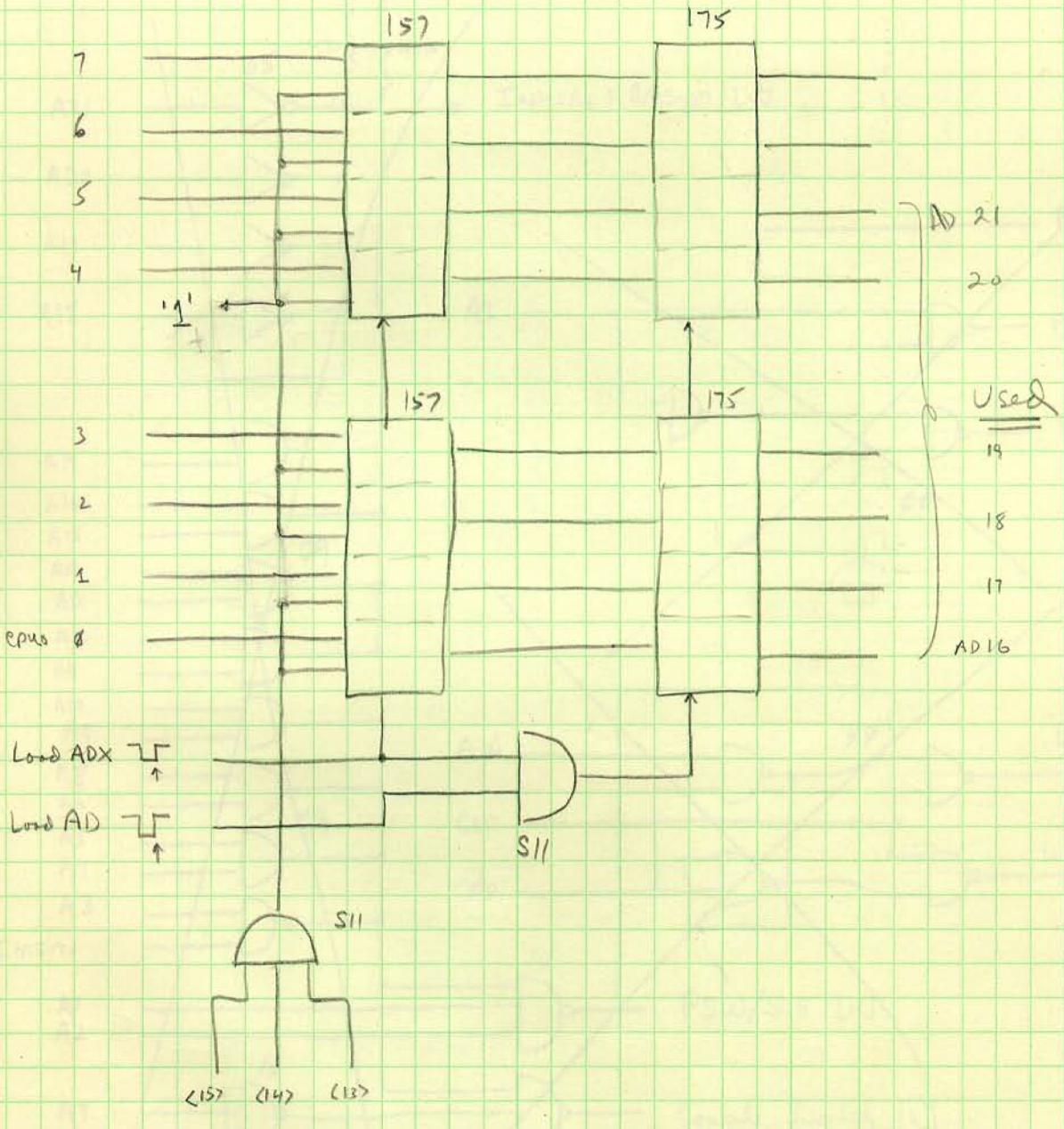
ARB

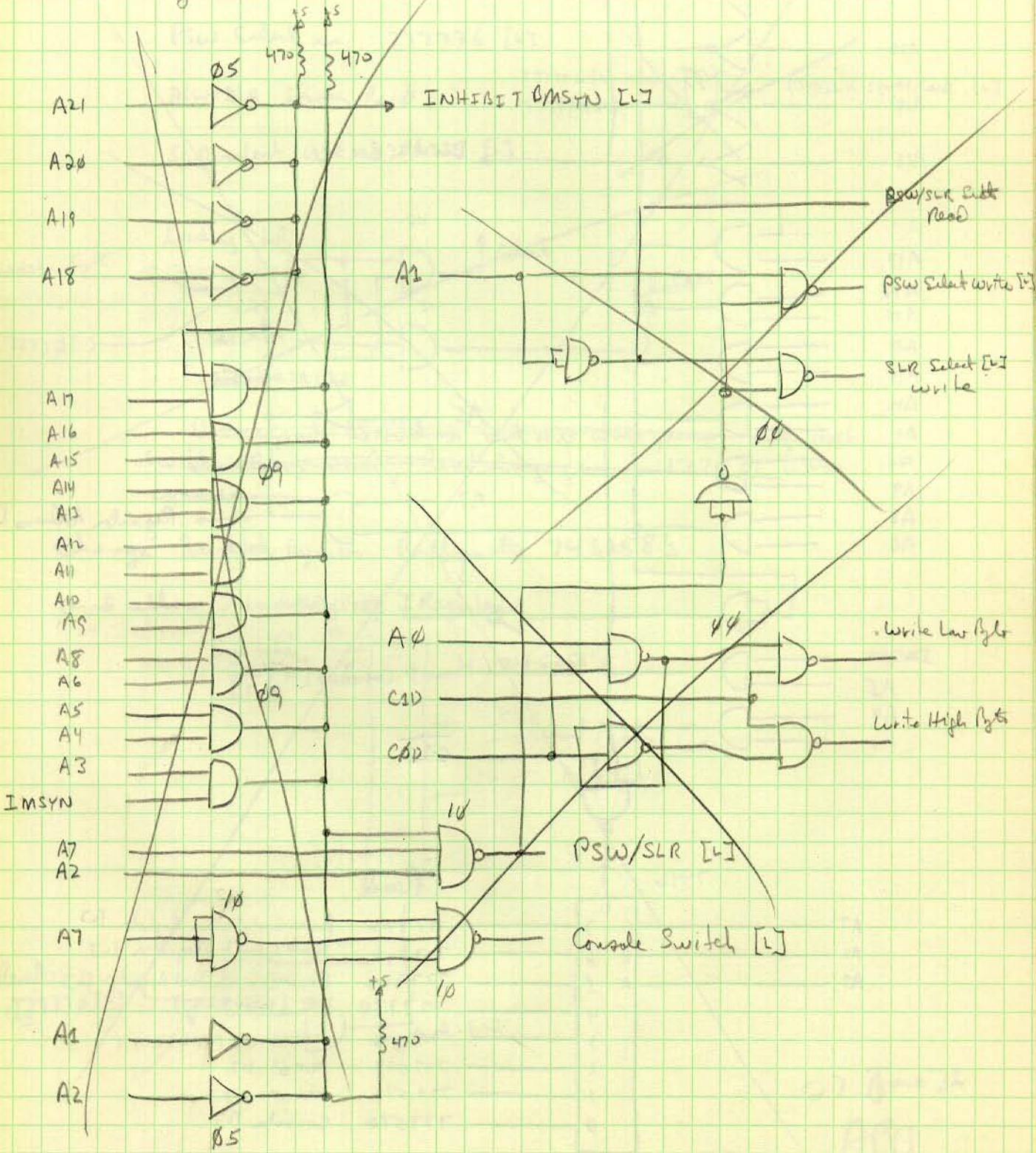

74S133
$\overline{C7}$
$\overline{C6}$
$\overline{C5}$
$\overline{C4}$
$\overline{C3}$
$\overline{C2}$
$\overline{C1}$
$\overline{C0}$
$\overline{CP}$
Not counting
Zero Detect
74S133
$\overline{C7}$
$\overline{C6}$
$\overline{C5}$
$\overline{C4}$
$\overline{C3}$
$\overline{C2}$
$\overline{C1}$
C0
CP
UD
counting Down
Zero Detect
74S11
Counter = Zero [L]
74S133
C7
C6
C5
C4
C3
C2
C1
C0
CP
UD
counting Up
Zero Detect

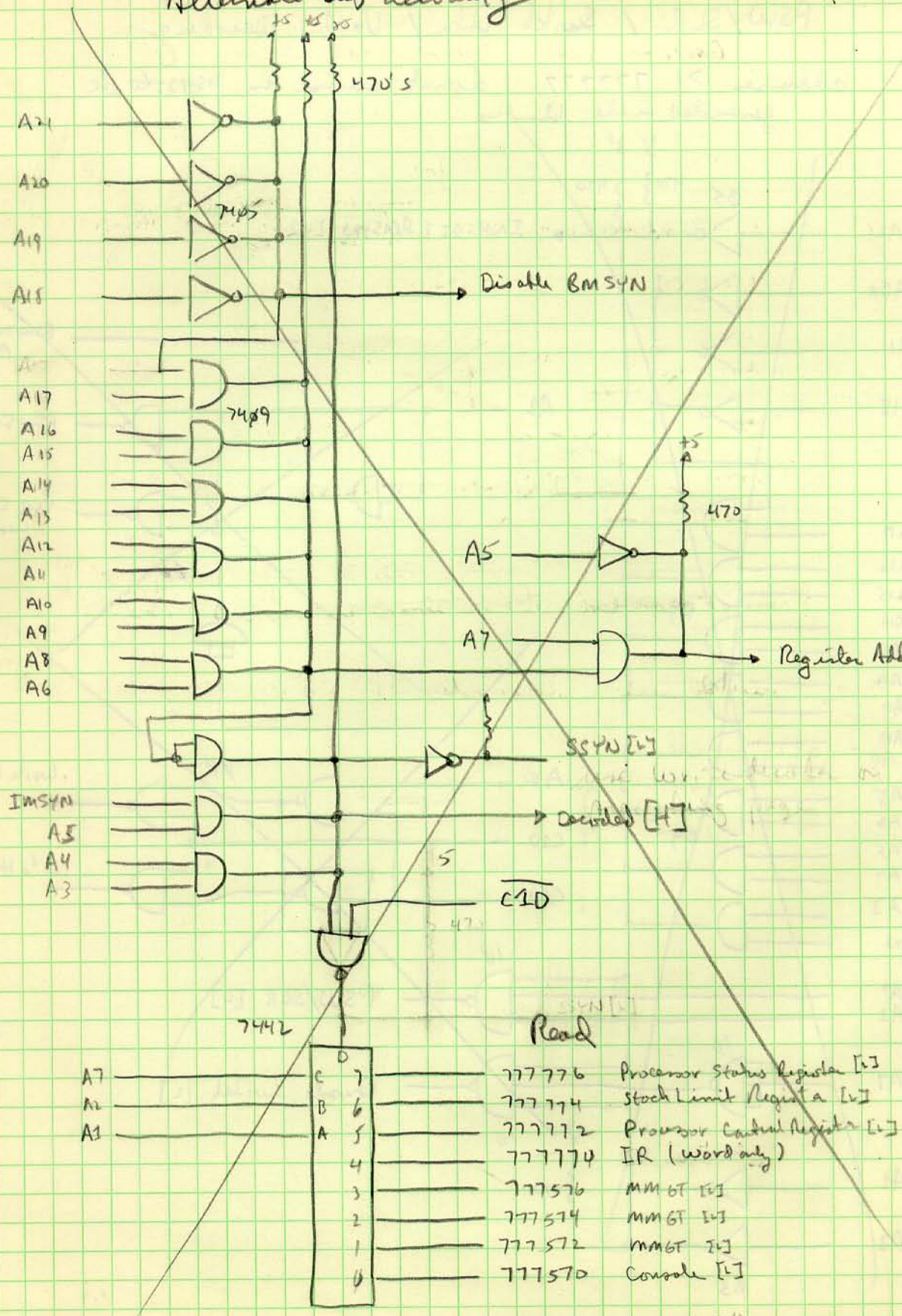
ADX Logic (extended to 22 Bits)



PSW/SLR / Switch Data / Unibus Decoding

address > 777777 donat cause an MSYN ~~to be~~ generated on the Unibus



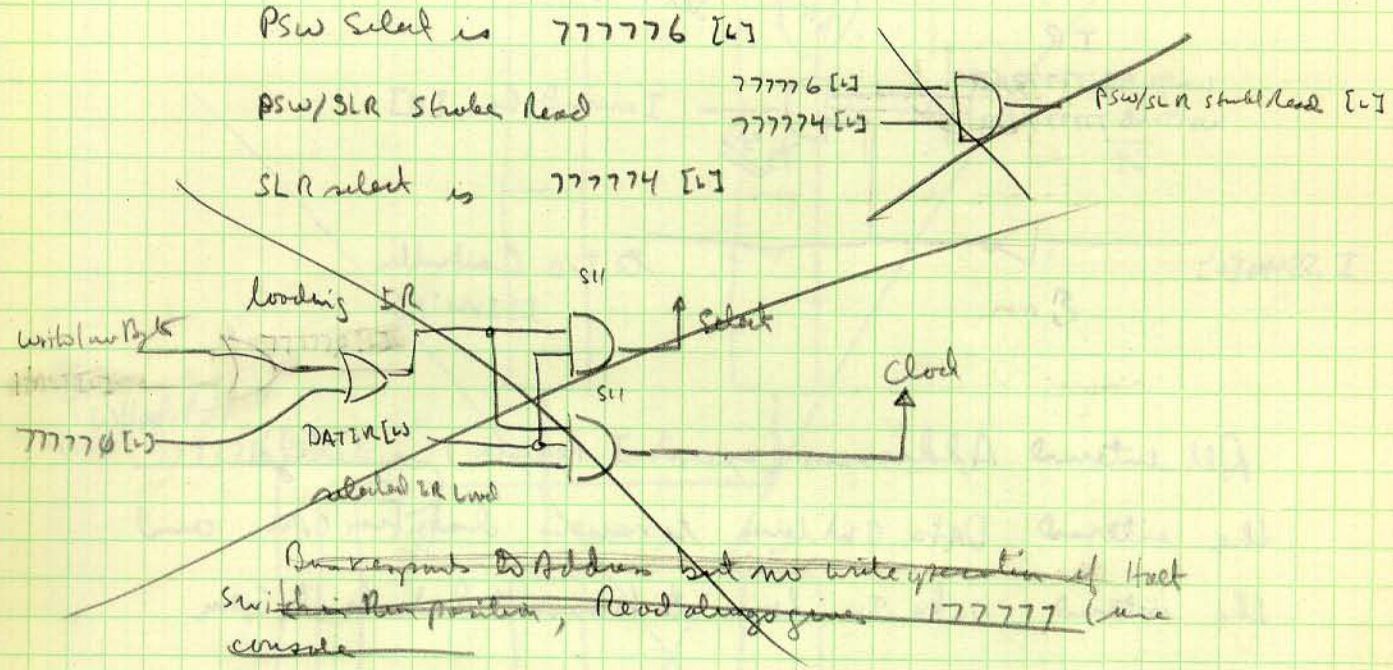

Alternate bus decoding
+5
470's
A21
A20
A19
A18
7425
Disable BMSYN
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A6
7429
+5
470
A5
A7
Register Address [H]
SSYN [L]
IMSYN
A5
A4
A3
Decoded [H]
5
C10
7442
Read
A7
A2
A1
C
B
A
D
0
1
2
3
4
5
6
7
777776 Processor Status Register [L]
777774 Stack Limit Register [L]
777772 Processor Control Register [L]
777770 IR (word only)
777576 MMGT [L]
777574 MMGT [L]
777572 MMGT [L]
777570 Console [L]

Added control for Select Logic

PSW Select is 777776 [L]

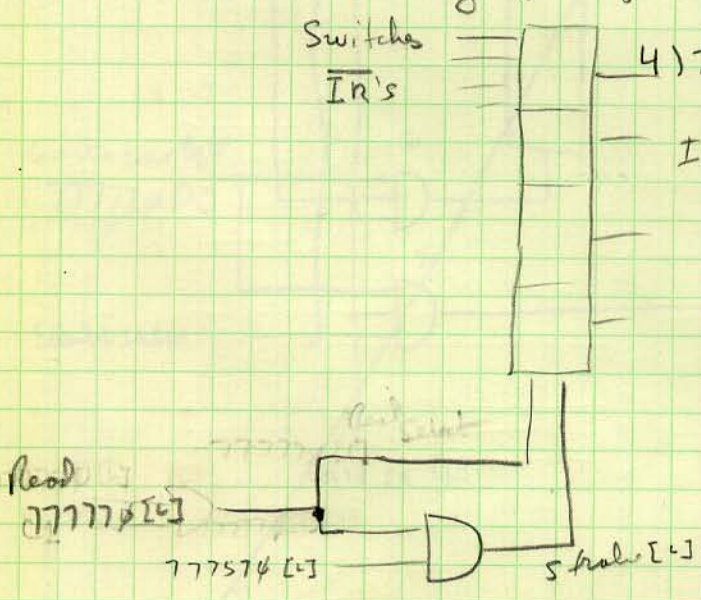
PSW/SLR Strobe Read

SLR select is 777774 [L]



~~Bus responds to Address but no write operation if Test Switch in Run position, Read always gives 177777 (wire console~~

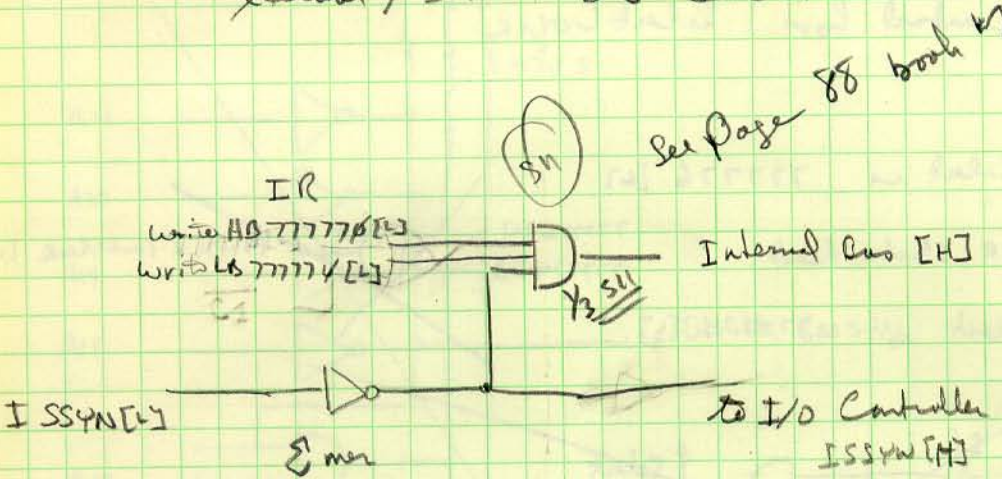
Change Switch Register Buffers to 74S258's and allow reading of I Register



27 June 76

ARB

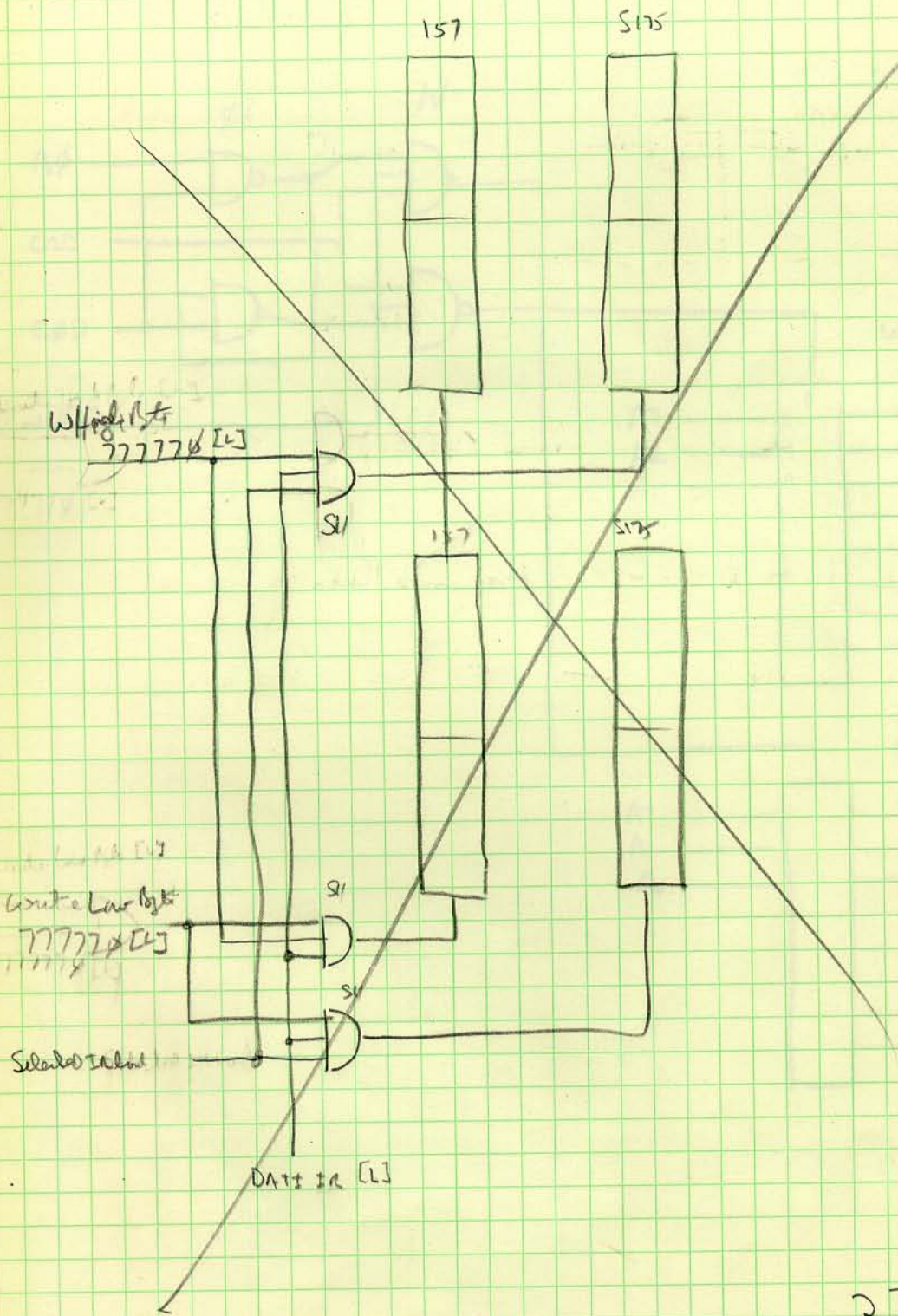
External / Internal Bus Select



All internal Addresses (except I Register) utilize the internal DATA Out lines to receive data from CPU and the internal Data In lines to transmit data to the CPU

the IRegister expects its data on the Data IN lines!

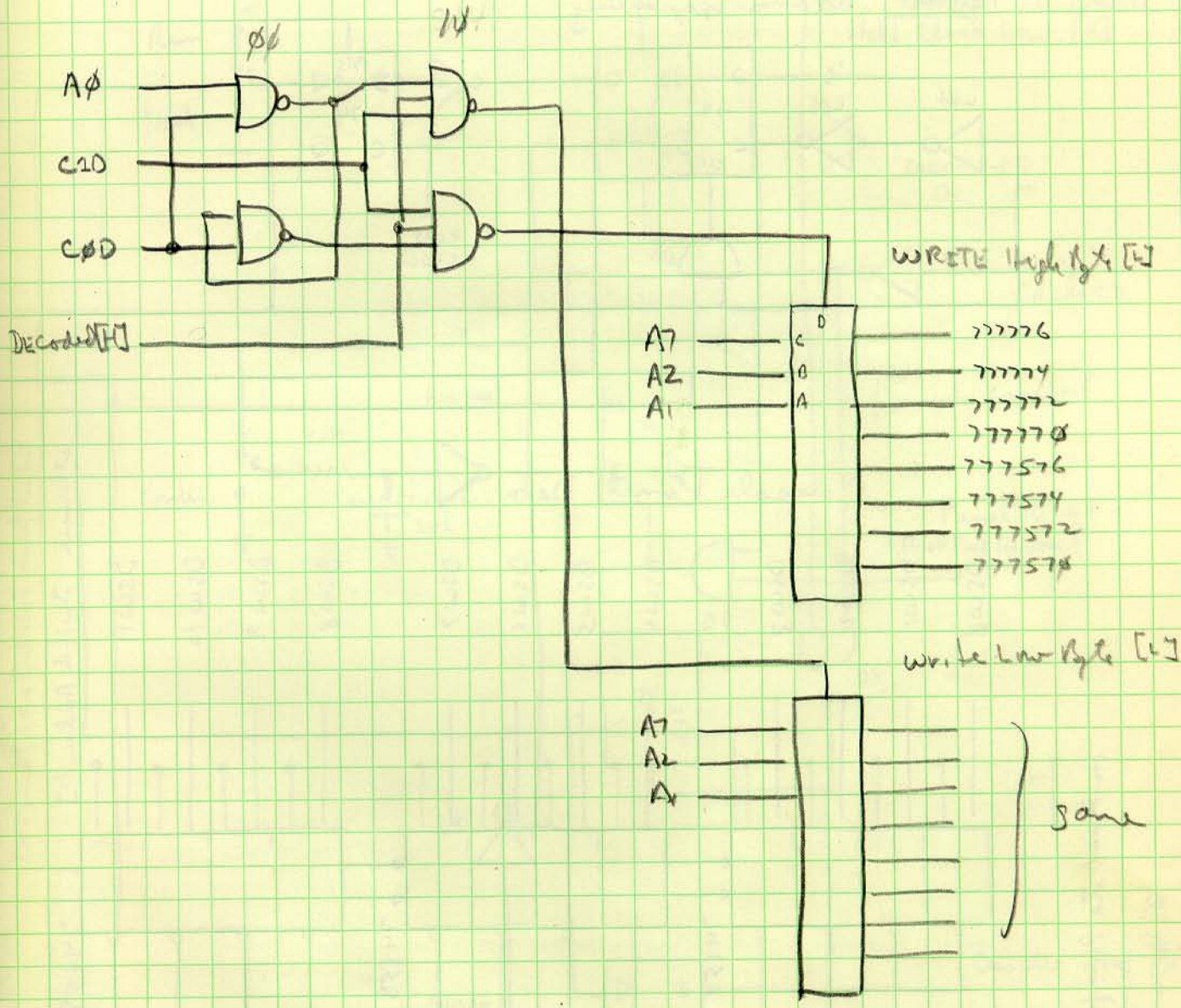
I Register Write Logic



27 June 1976

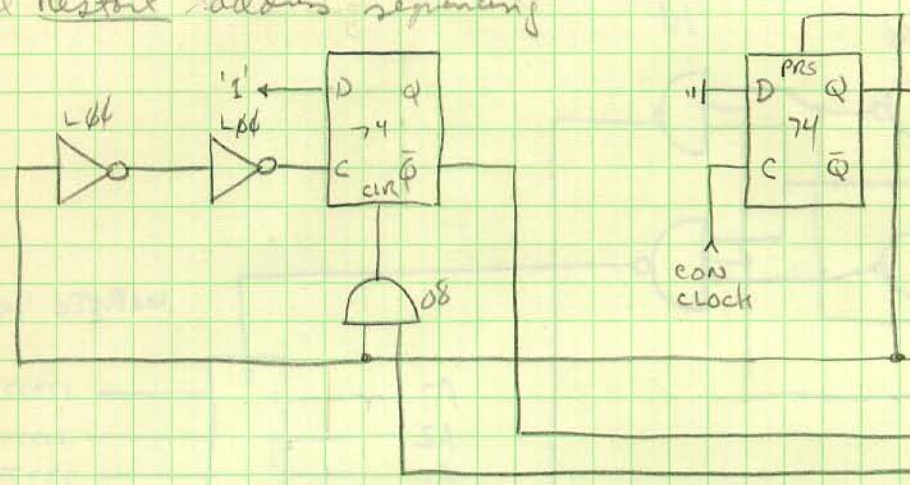
ARB

Write Decoder

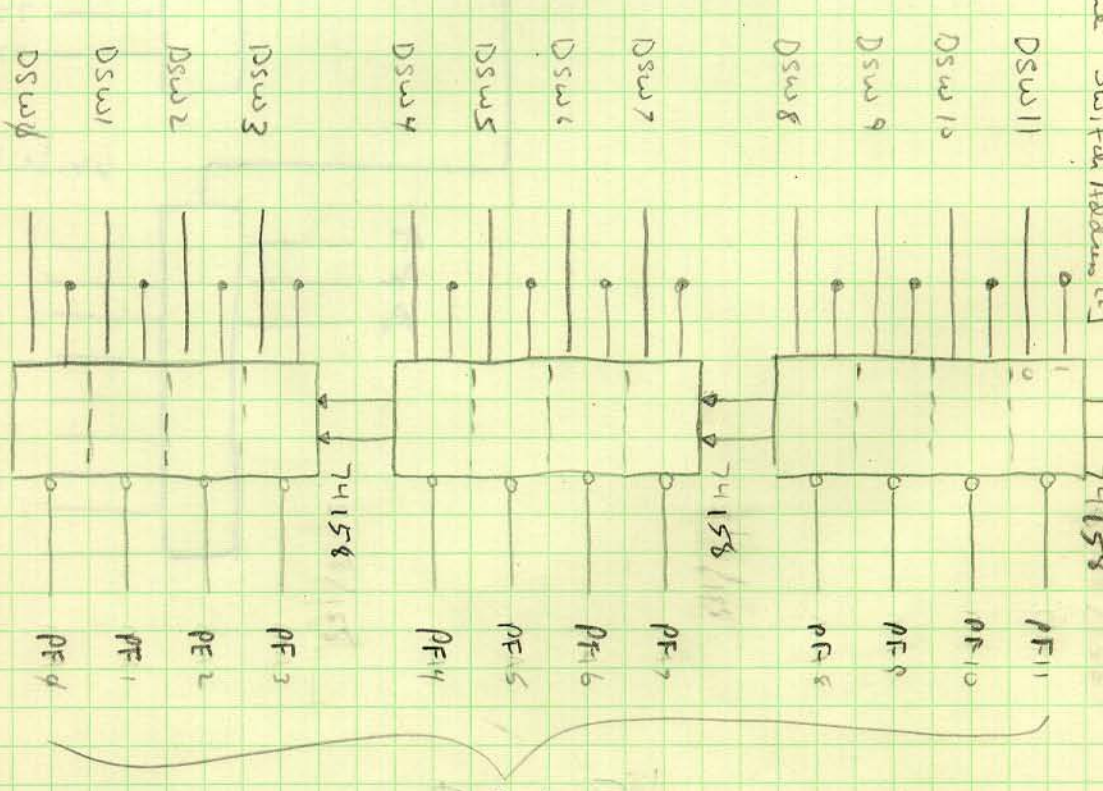


27 June 76
AGM

Modifications to the Panel logic to include the Multiplexor to the Microcode Address line & the Power Fail Restart address sequencing



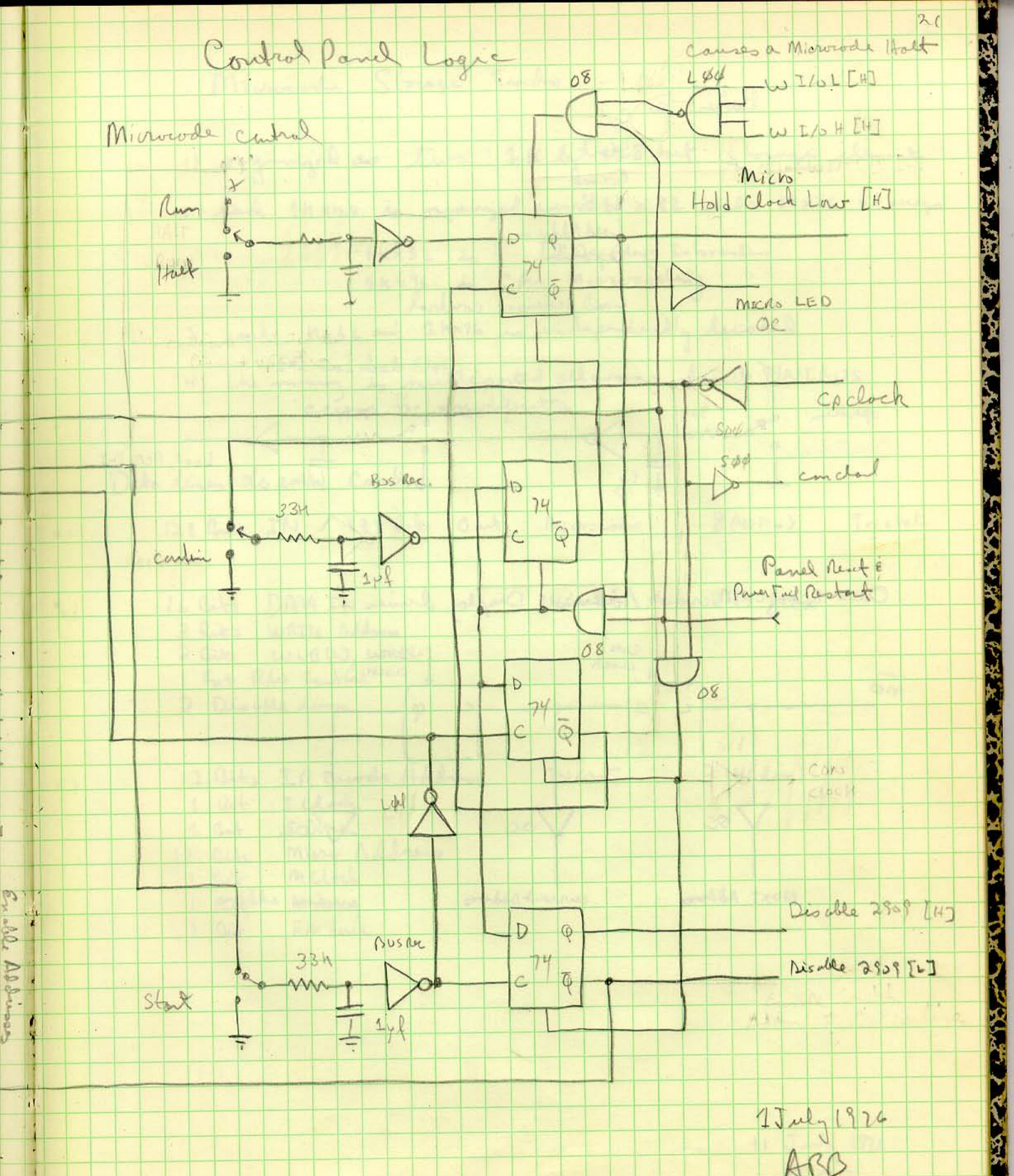
Console Panel Data Switches



On Controller Board

17 July 76
ABB

Control Panel Logic



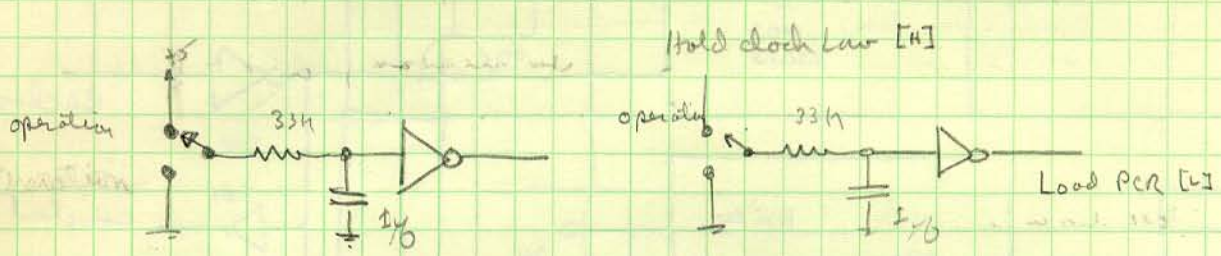
1 July 1976

ARD

Buffers for

Start
Exam
Continue
Load Address
Deposit

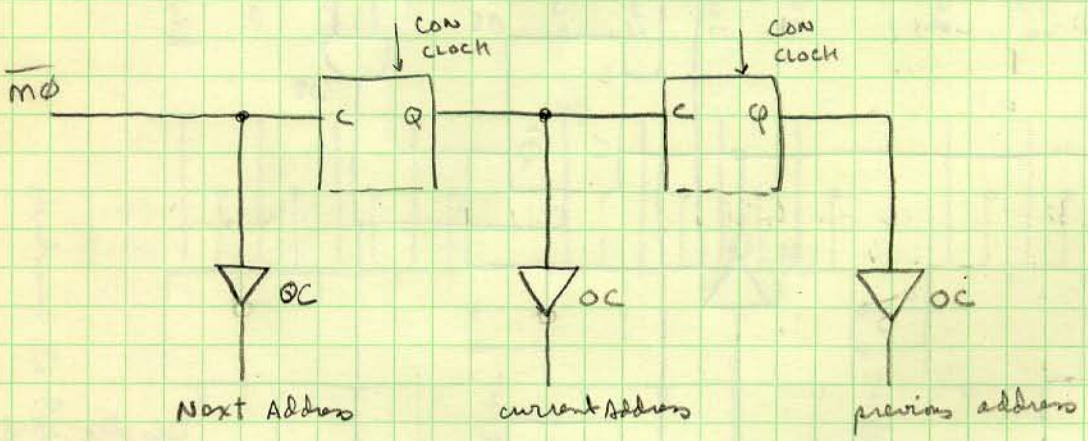
Load processor control



a)

ONE Bit of Microcode Address Display driver

b)



c)

Microcode Storage Cards -

1) organized as two 1K by 128 bit storage element

2) each 1K x128 is organized as a 1K x 32 and a 1K x 96 bit array

1K x 32 is IR Decoding Information
1K x 96 is CPU Microcoding

3) each 1K x 32 and 1K x 96 is independently decoded

4) the memory is multiported allowing direct UNIBUS access for modification

Data lines to each Card

a)	128 Bits IN / 128 Bits Out	Microcode	8 (40 Pin)	Tristate
b)	16 Bits DATA IN	IN/out	2 (40 Pin)	
	3 Bits WRITE Address			
	2 Bits WLB(L), WHB(L)			
	1 Ext RW Control			
	2 Disable lines			
c)	12 Bits IR Decode Address	IN/out	2 (40 Pin)	
	1 Bit I Clock			
	1 Bit I Done			
	12 Bits Micro Address			
	1 Bit M Clock			
	1 Bit M done			
	1 Bit EM done			

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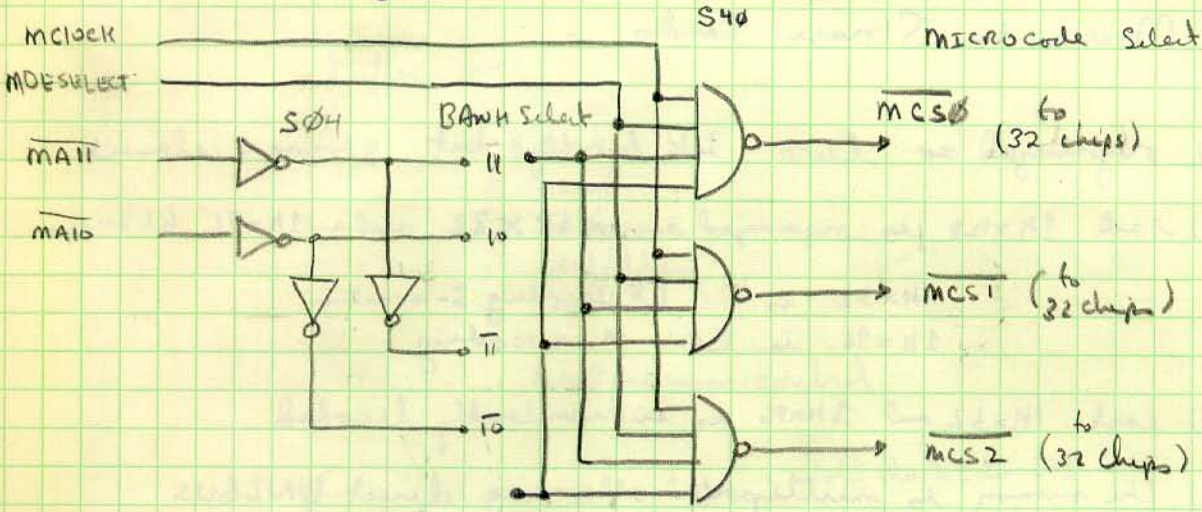
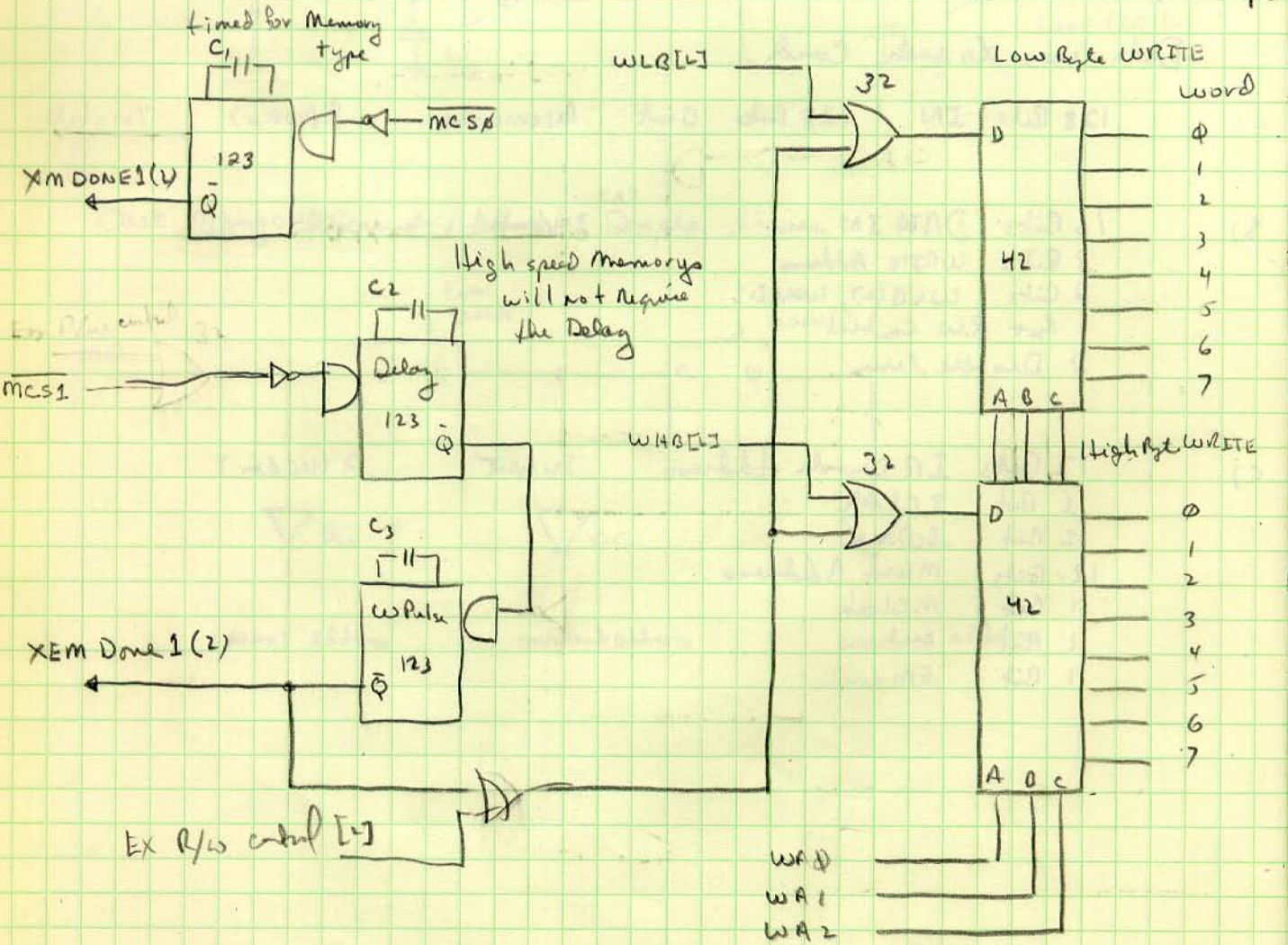
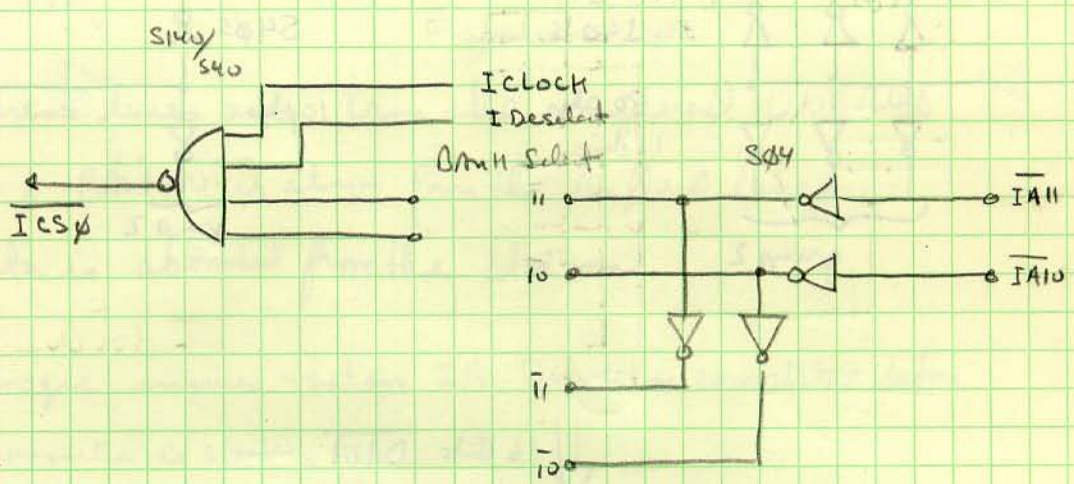
ARB

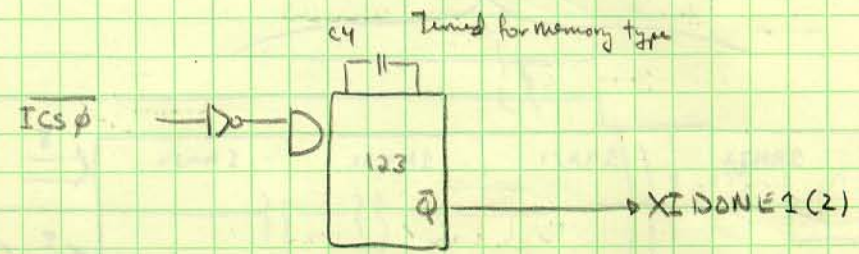
Board Decoding / for 1K×128

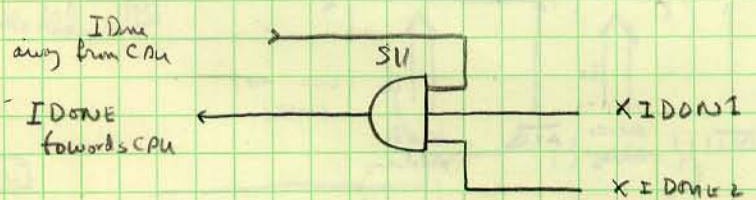
S140 / S40

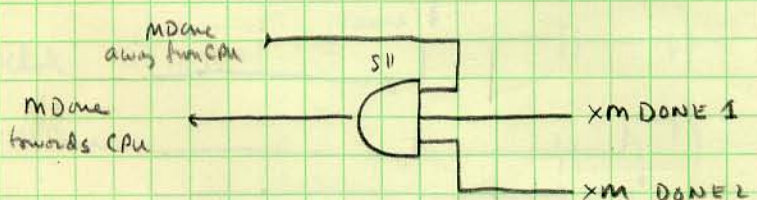


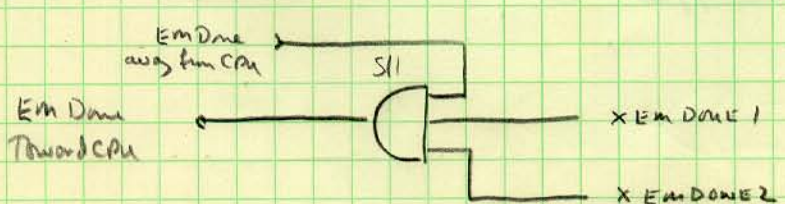




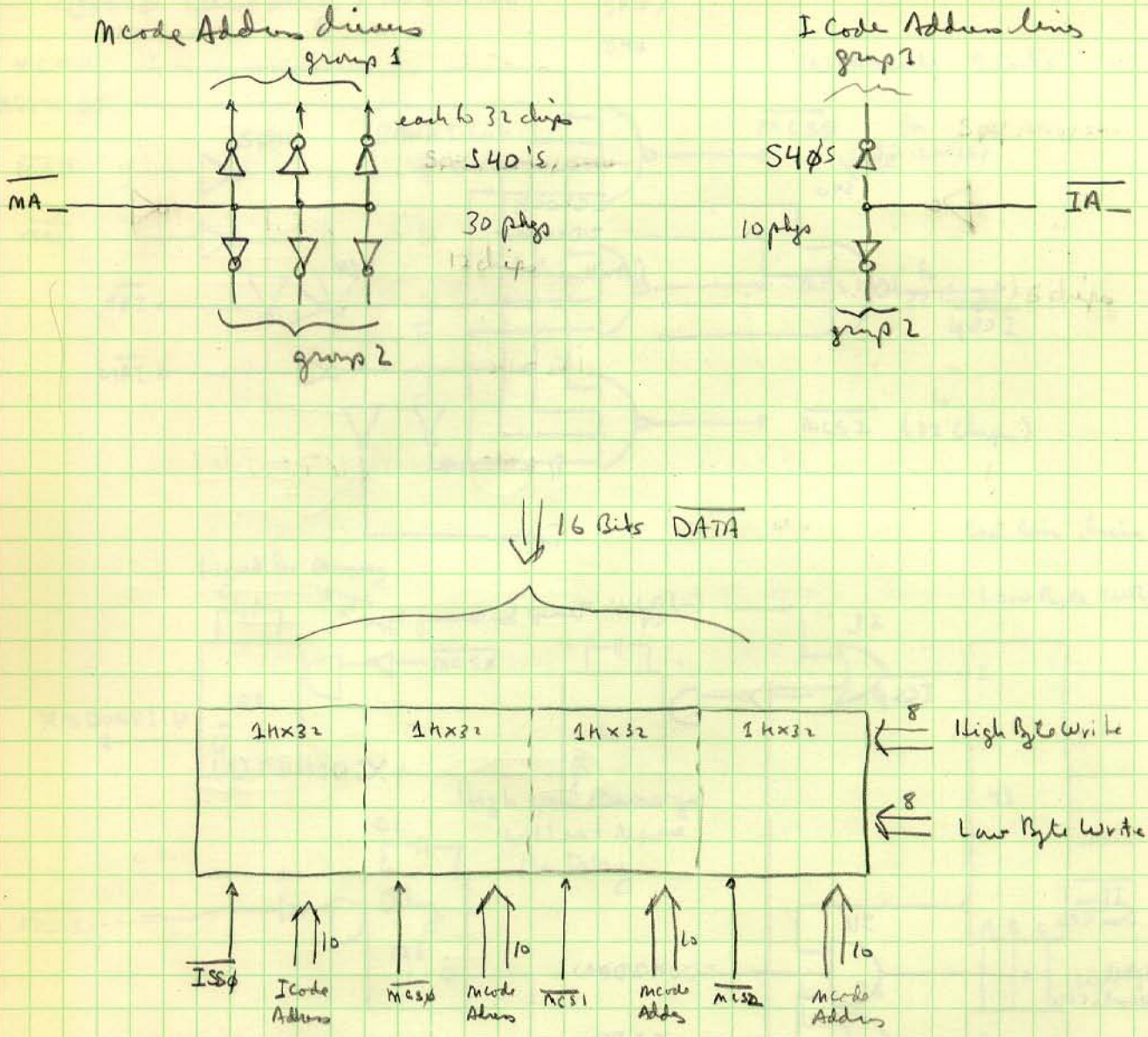








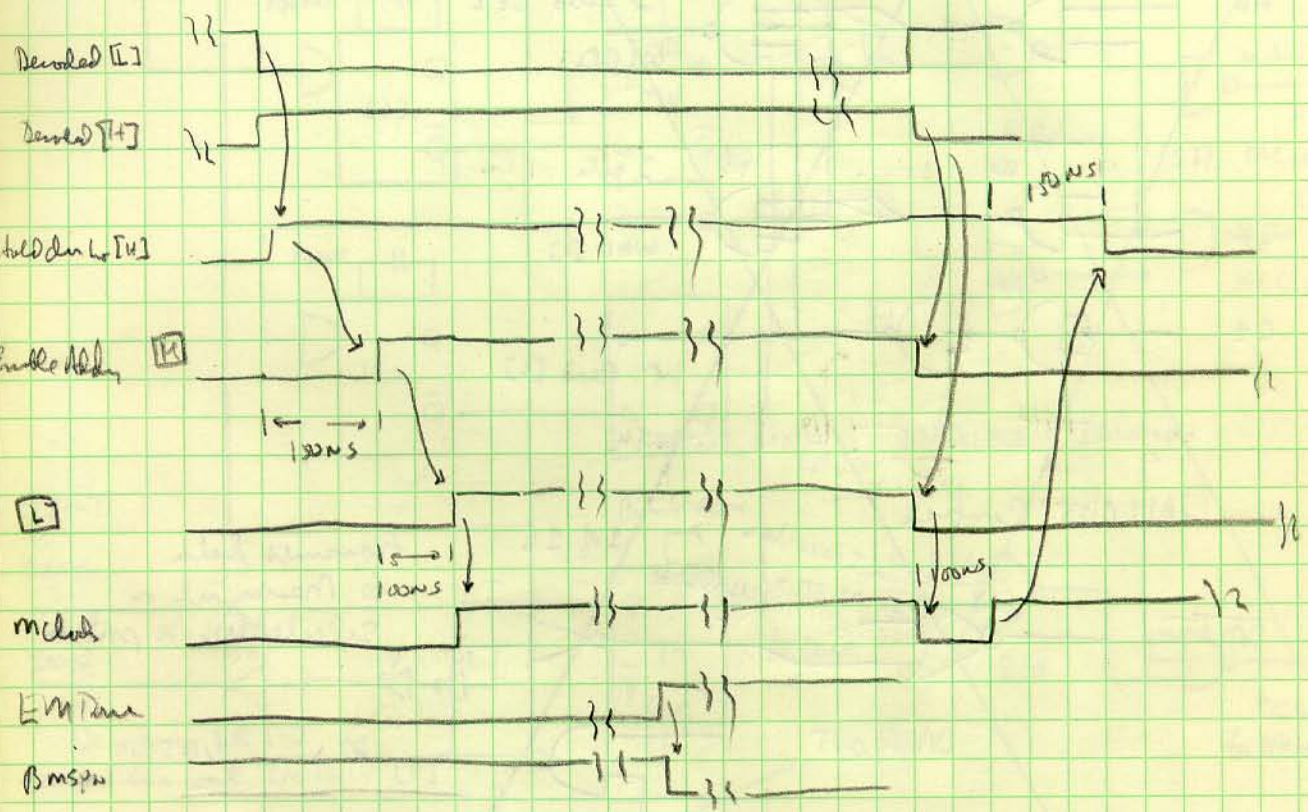
11 July 76
ARD


Mcode Address lines
group 1
each to 32 chips
S40's,
30 phys
MA
group 2
I Code Address lines
group 1
S40s
10 phys
IA
group 2
16 Bits DATA
1Mx32
1Mx32
1Mx32
1Mx32
8
High Byte Write
8
Low Byte Write
ISSØ
10
ICode Address
MCSØ
10
Mcode Address
MCS1
Mcode Address
MCS2
10
Mcode Address

Writable IR Decode/Microcode BUS Control

Address lines are from the buffered UNIBUS lines, BMSYN is also from the Buffered lines
All Data is obtained from the Unibus

Logic insures that an IR Decode is completed before a BUS Transaction is started



11 July 1976
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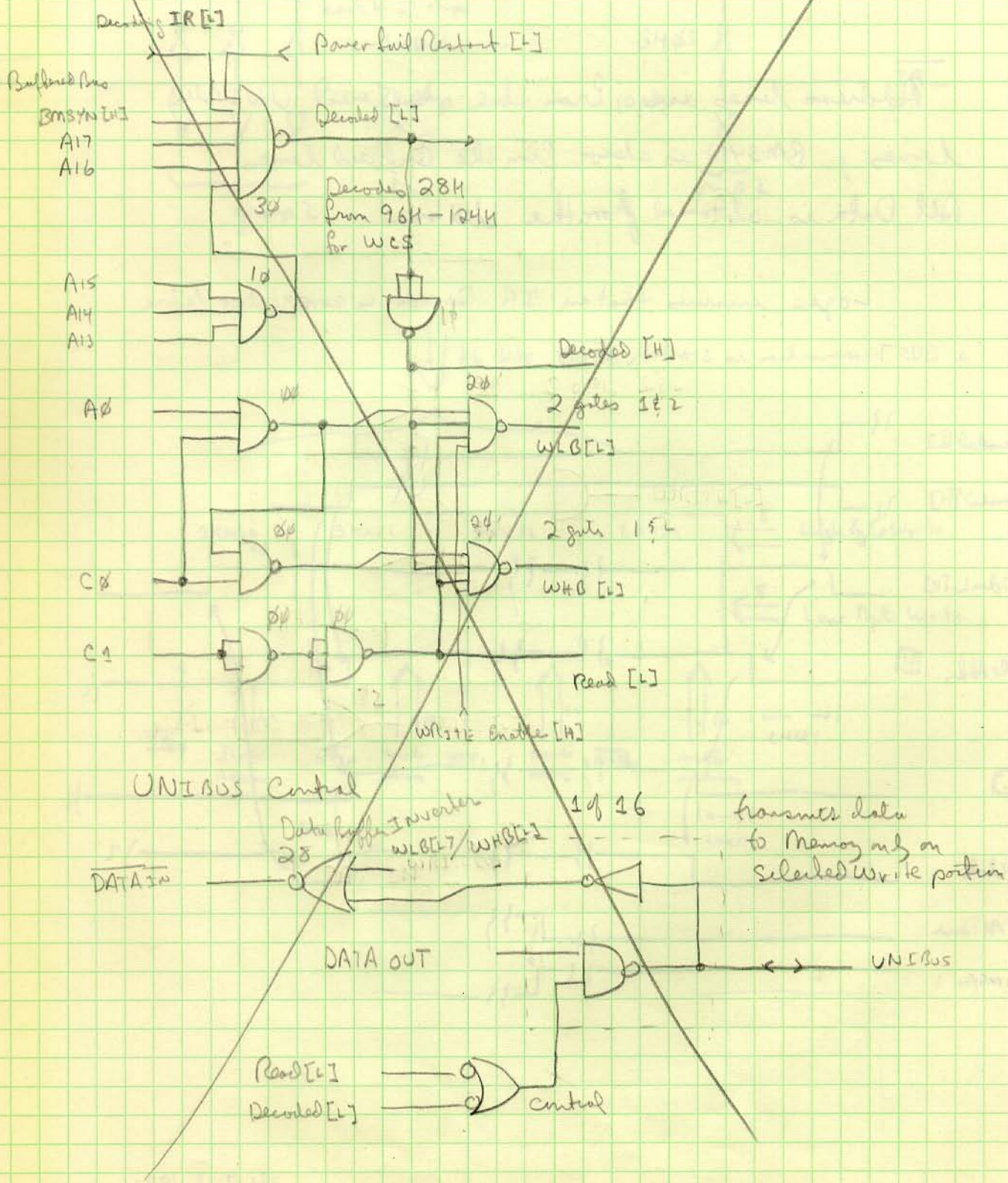
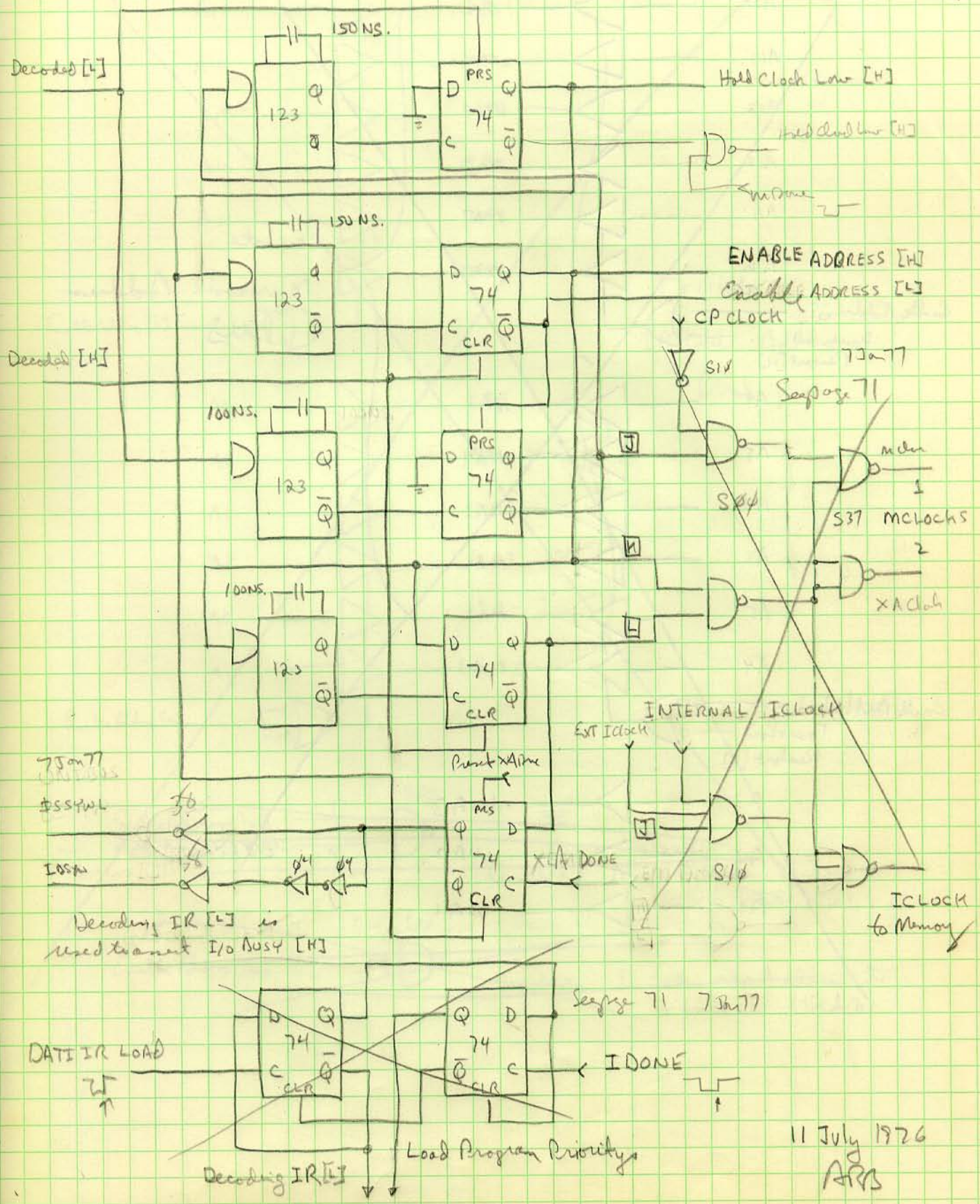
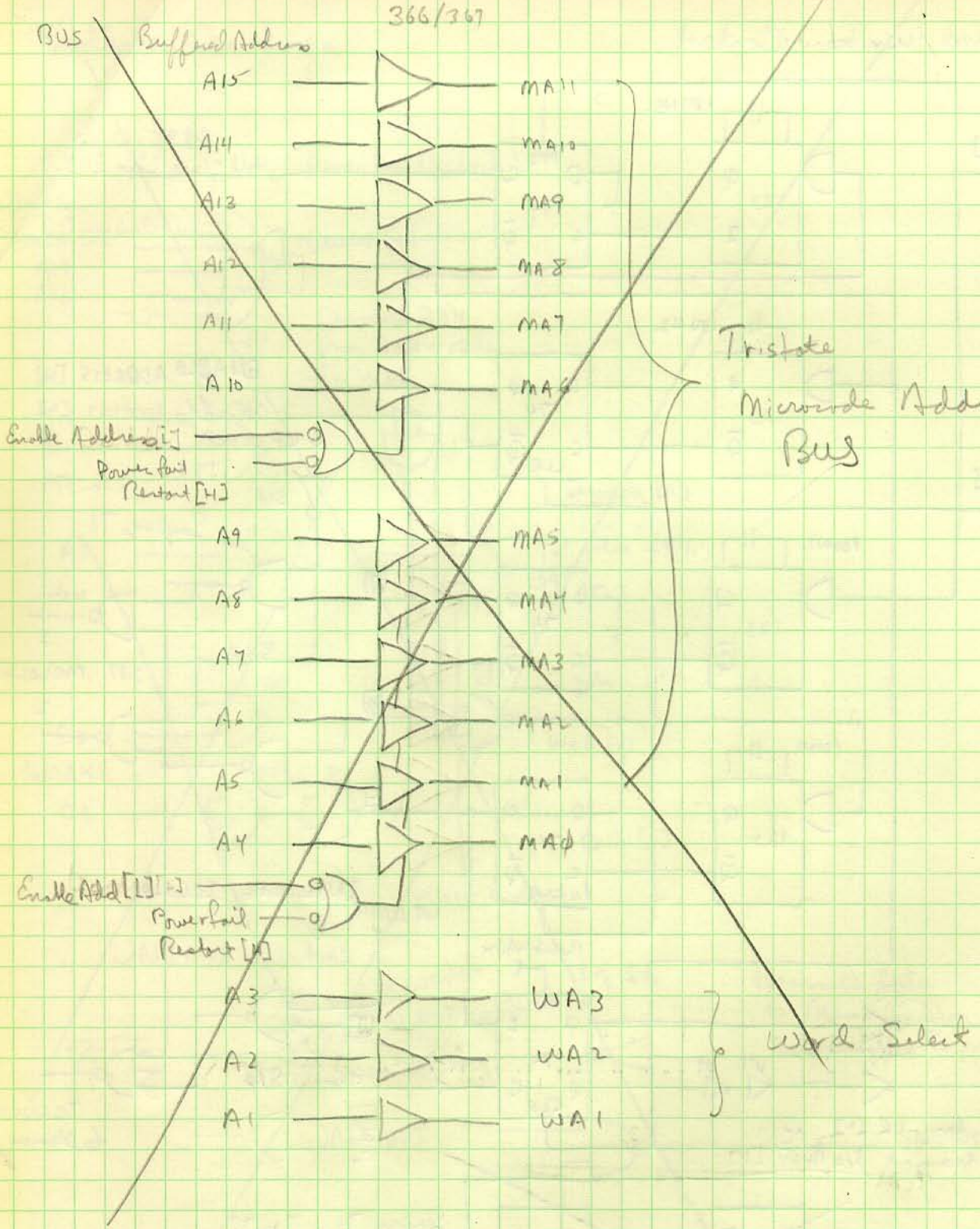
Address Decoding



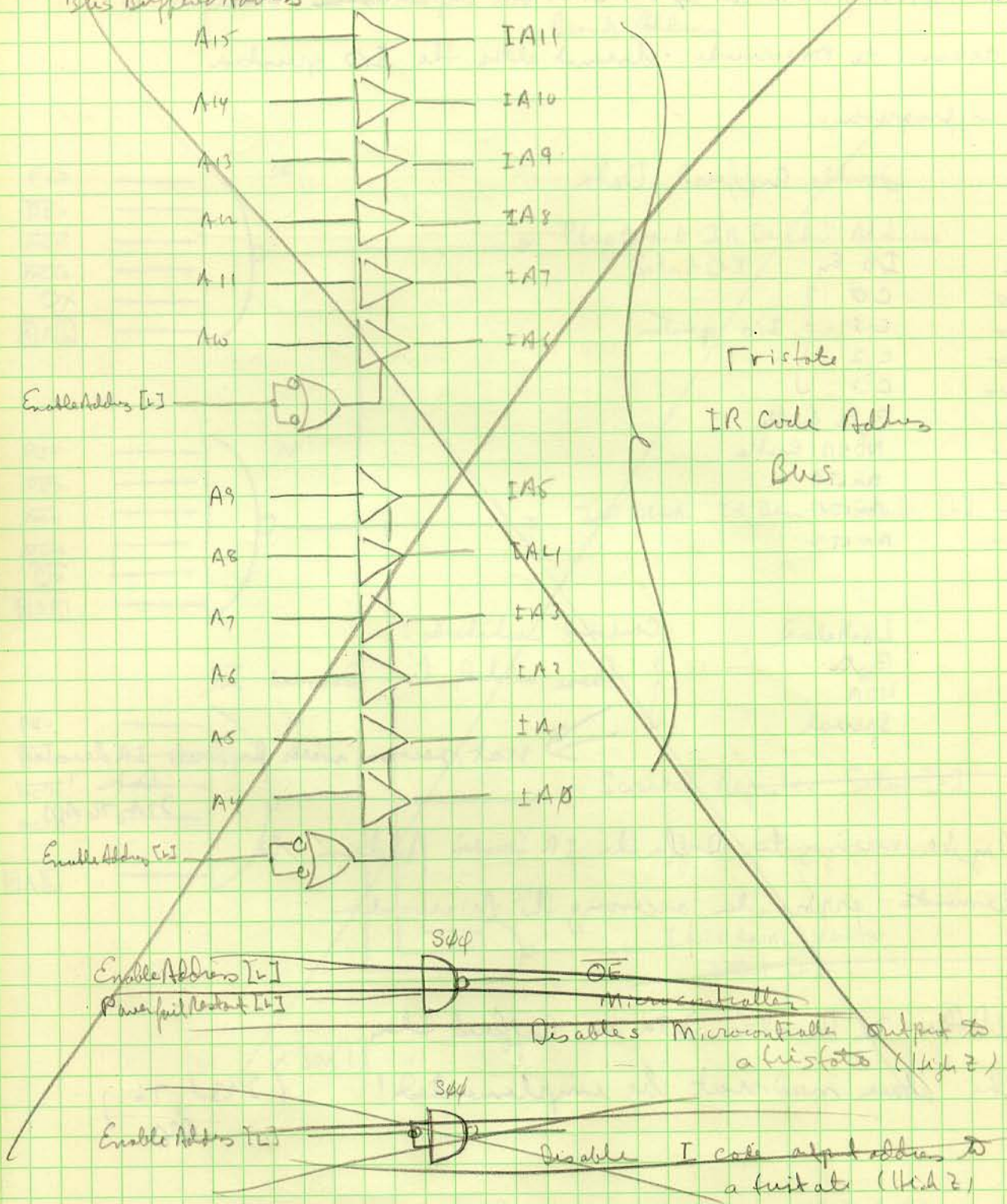
Read/Write Control




BUS
Buffered Address
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
MA11
MA10
MA9
MA8
MA7
MA6
MA5
MA4
MA3
MA2
MA1
MA0
WA3
WA2
WA1
Enable Address[1]
Powerfail Restart[H]
Enable Add[L]
Powerfail Restart[H]
Tristate Microcode Address BUS
Word Select

3661387

Bus Buffered Address



Tristate

IR Code Address Bus

Modification to I/O Control to insure that an access to microcode doesn't alter the I/O operation in progress.

Double Buffered Data

Micro	I/O En
Micro	C 0
Micro	C 1 } I/O operation
Micro	C 2
Micro	C 3
Micro	Byte Enable
Micro	NDSP Enable
Micro	MM BT 0
Micro	MM BT 1
Micro	MM BT 2

Lookahead
Byte
NOA
Special
} these added from Decoded IR

Combined Lookaheads!

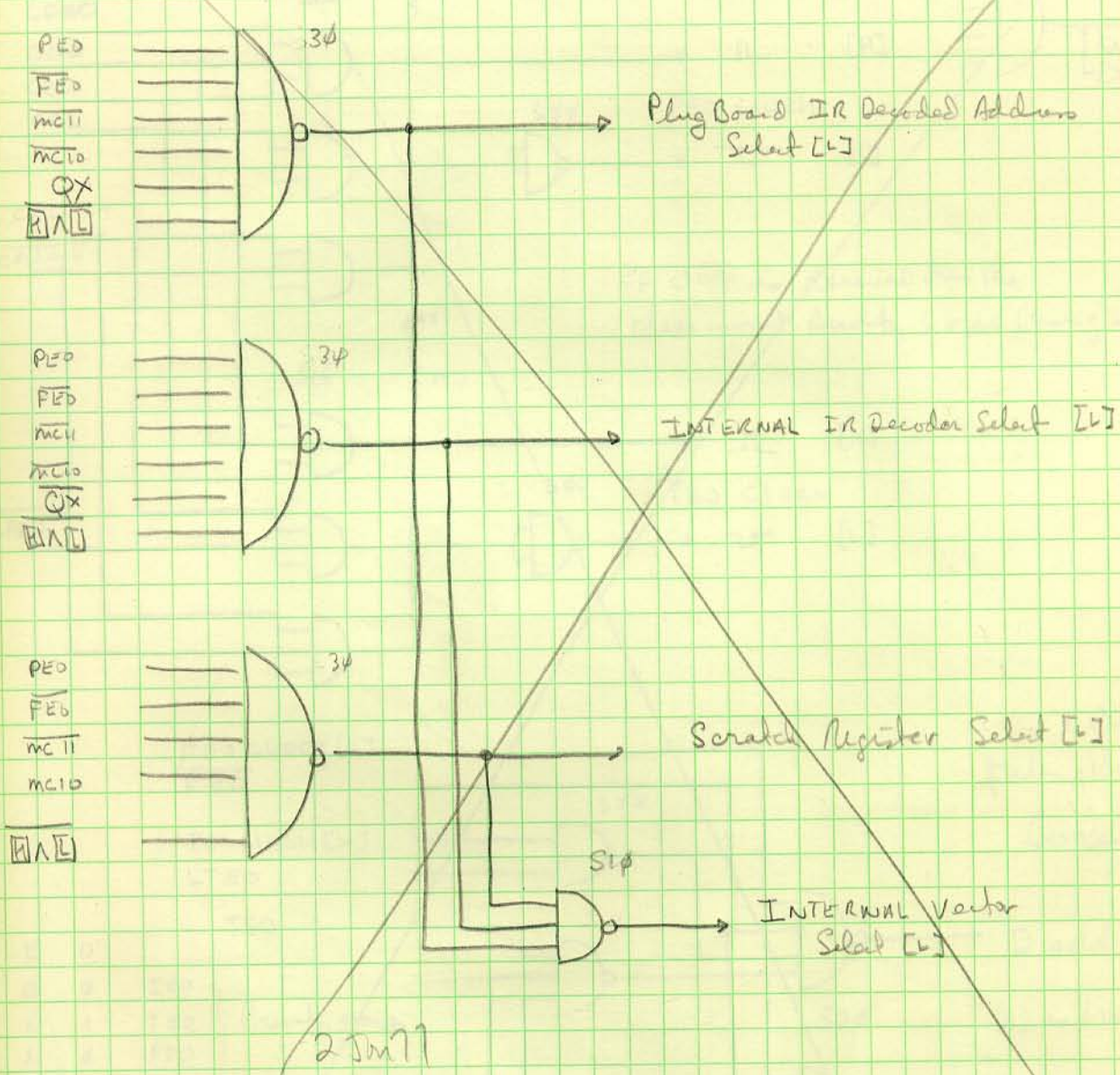
→ not necessary with Buffered IR decoded Data!
27 May 76 ARB

May be necessary to Buffer the IR Decoded Address to eliminate errors when accessing the Microcode

---

* If the IR Decoded Data is Buffered then the above need not be implemented! (24 Jun 76 ARB)

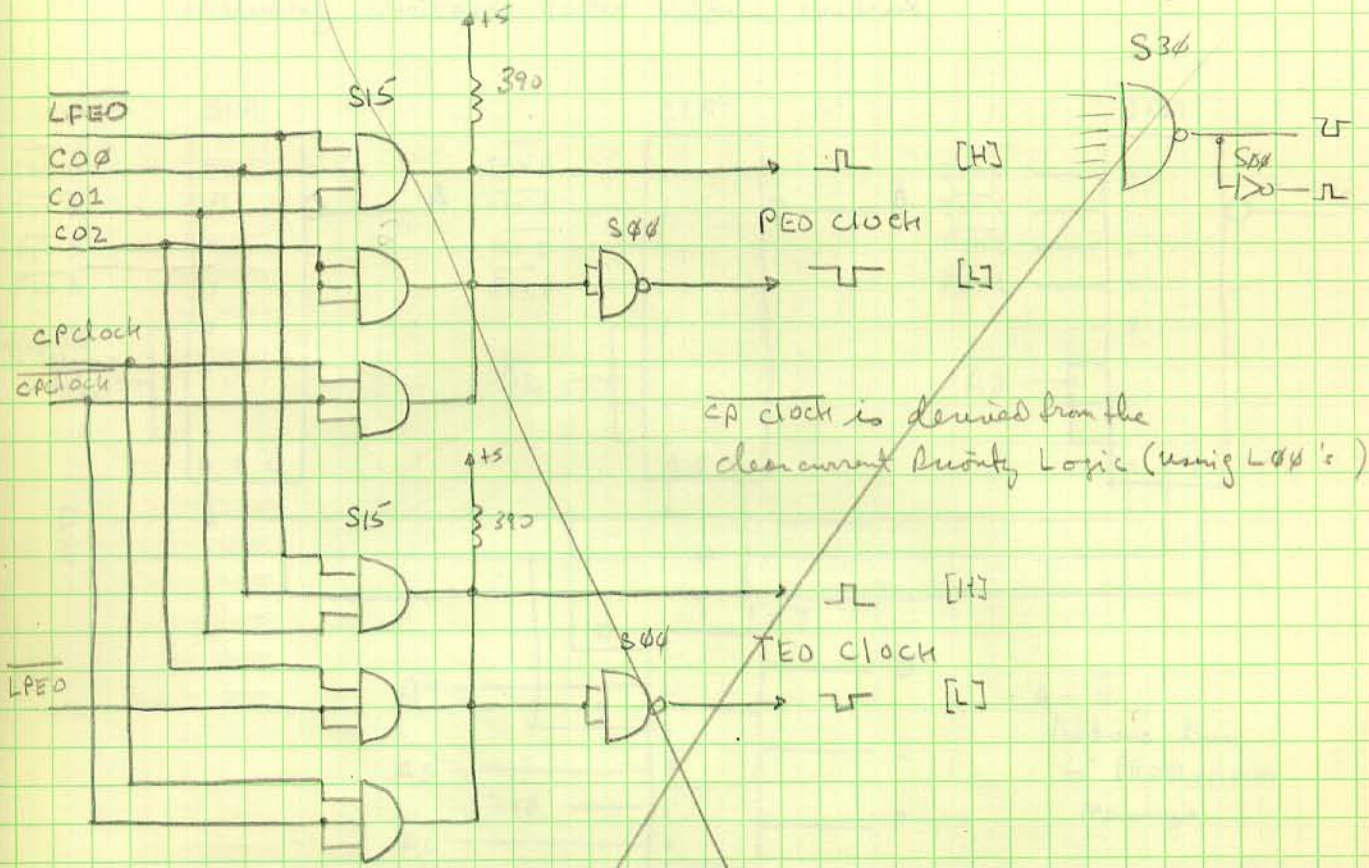
Modified Select logic for Scratch / Vector / and Programmed Branch Address

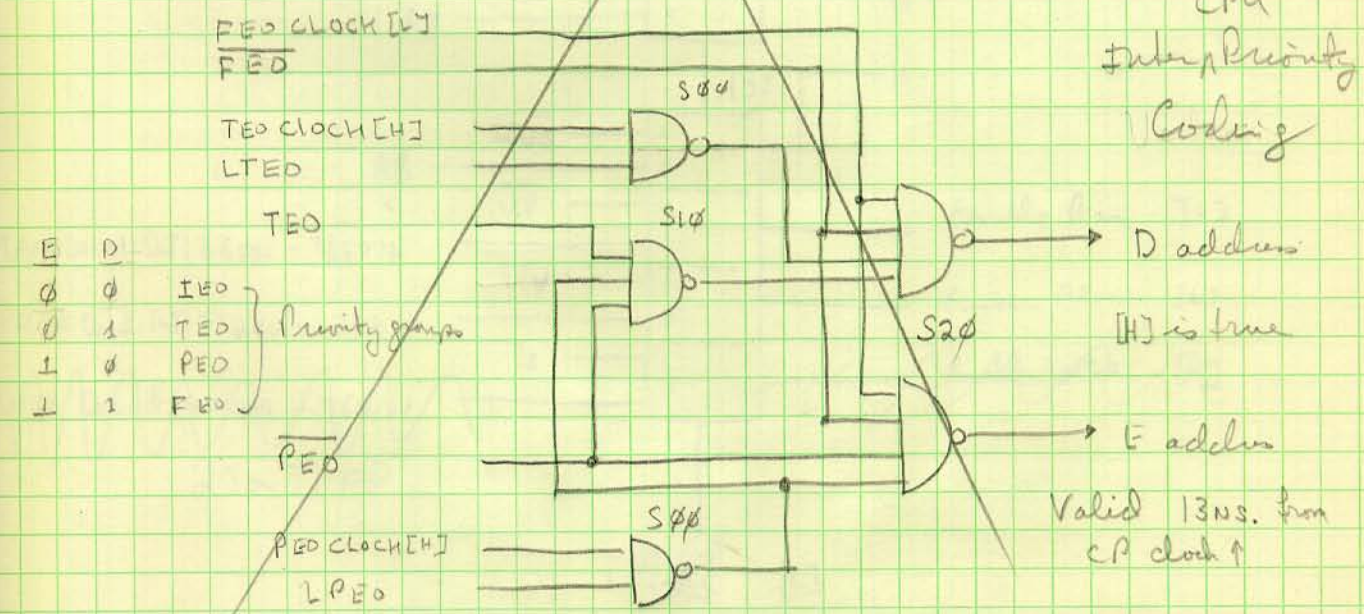


2 JAN 77

13 Jul 76
ARO

Redesign of Priority Clocks and Lookahead Addres. Coding 28
for the Vector/Programmed DR Icode Addressing





E	D	
0	0	IEO
0	1	TEO
1	0	PEO
1	1	FEO

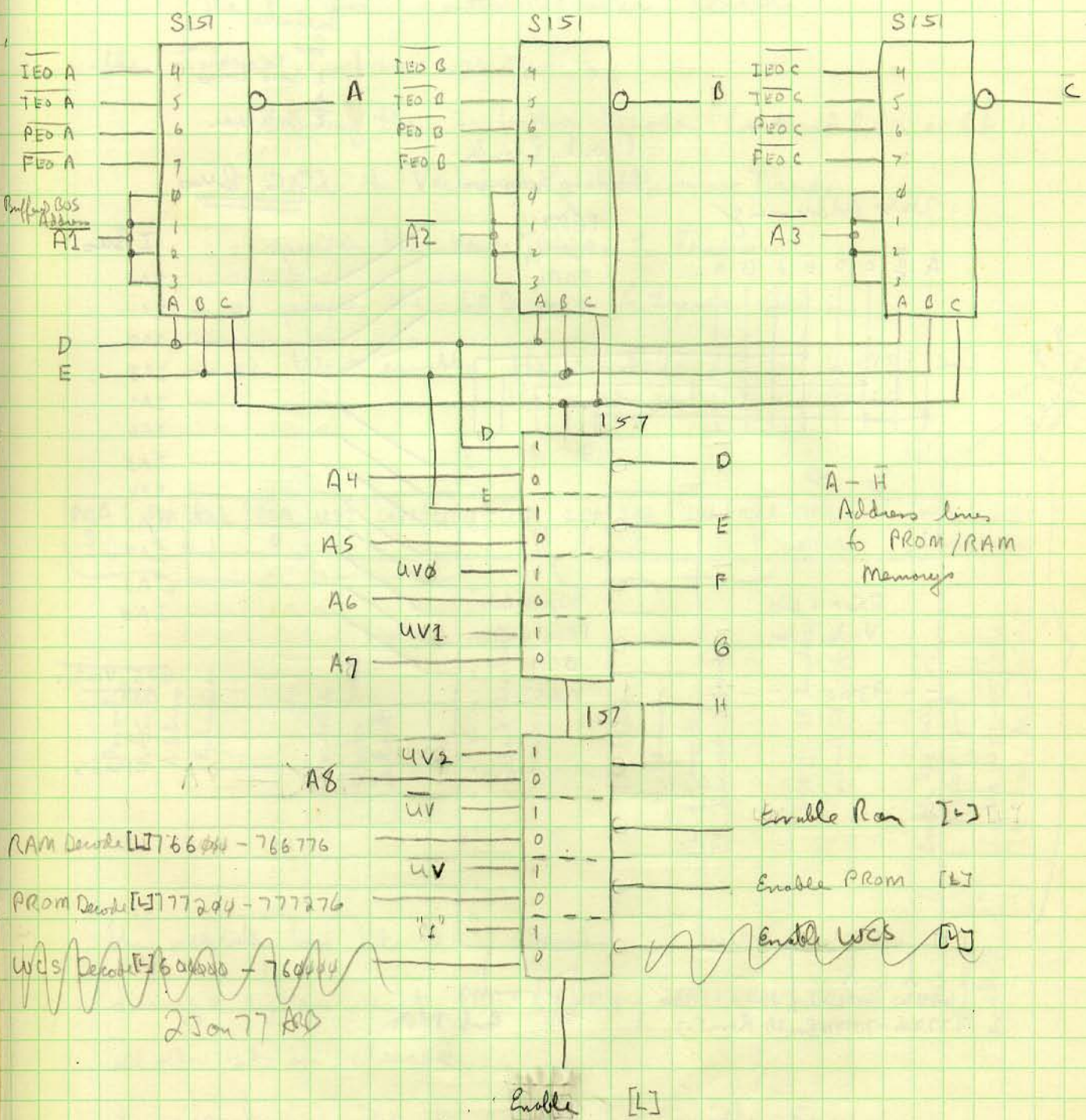
Priority groups

CPU Interrupt Priority Coding

14 July 1976
ARD

Redesign of Vector Address Selection Logic

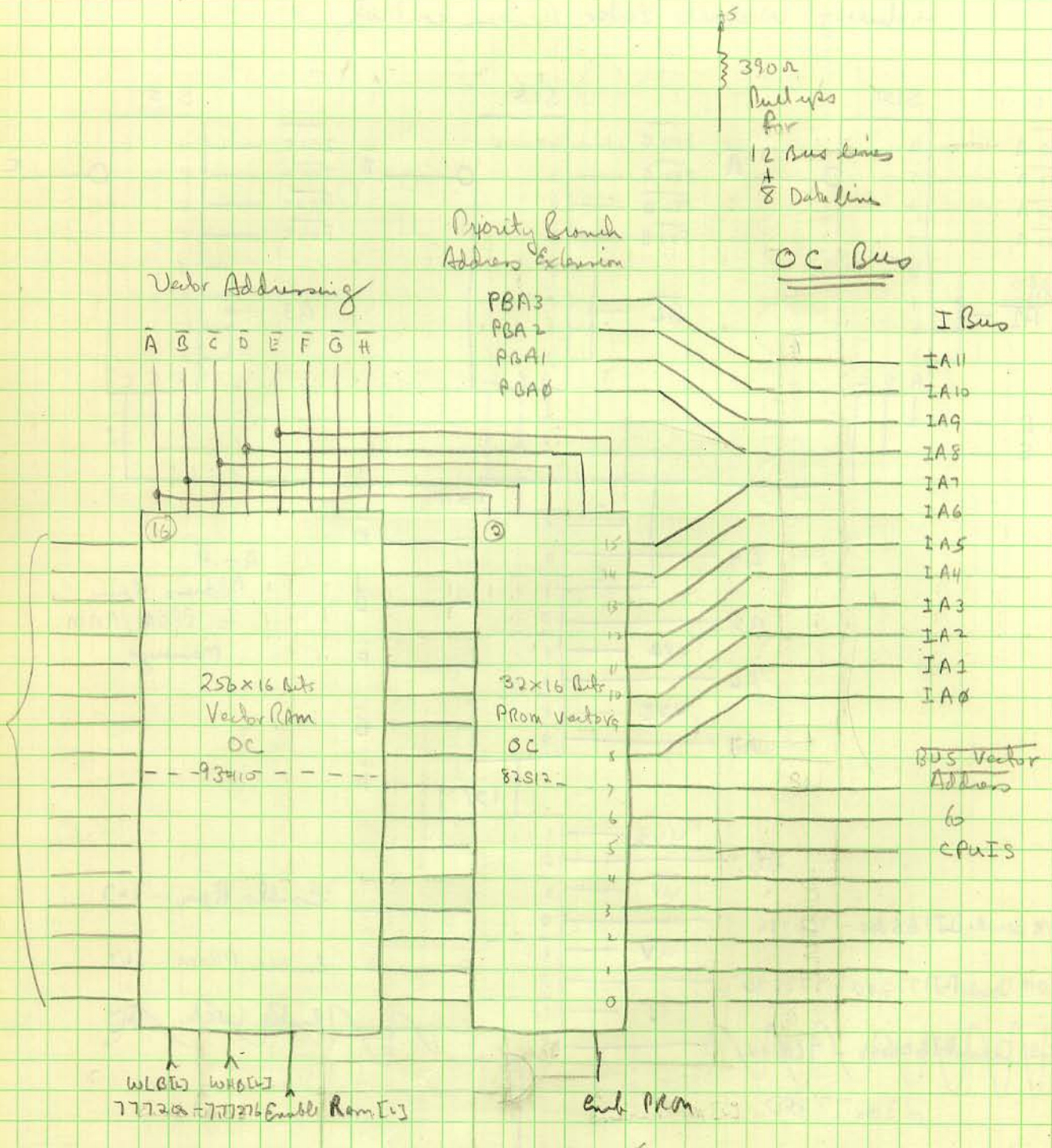
including Writable Vector Address control



14 July 1976

ARB

PRom / RAm Control



Processor Control Register · Logic

The Processor Control Register controls the Internal Processor operation by:

a) selecting the Instruction Decoder (internal PDP-11 or Ext.)

b) selects the Vector group for Processor Traps

c) specifies the Vector Broad Address Extension

d) specifies the IR Decoder Extension Address

e) Write enables the Writable Vector Store (WVS) and the Writable Control Store (WCS)

PSR Selected MMGT PAR/PDR

PGA 3	PGA 2	PGA 1	PGA 0	UV2	UV1	UV0	UV	IRA 3	IRA 2	IRA 1	IRA 0	PDP11/ OTHER		WVS Enable	WCS Enable
												0X			

Priority Branch Address Extension

Writable Vector Group Select

Select Writable Vectors [H]

IR Address Extension

Use selected IR decoder (unmapped)

PDP 11 IR Decoder / External IR Decoder

Enable Writing Vector group [H]

Enable writing WCS [H]

IR Flow / Microcode

Reads always enabled

this register has bits 0 & 1 cleared by an init

during a system reset, PBA3 & PBA2; IRA3 & IRA2 are set

all other bits are cleared

the register may be loaded from the console directly

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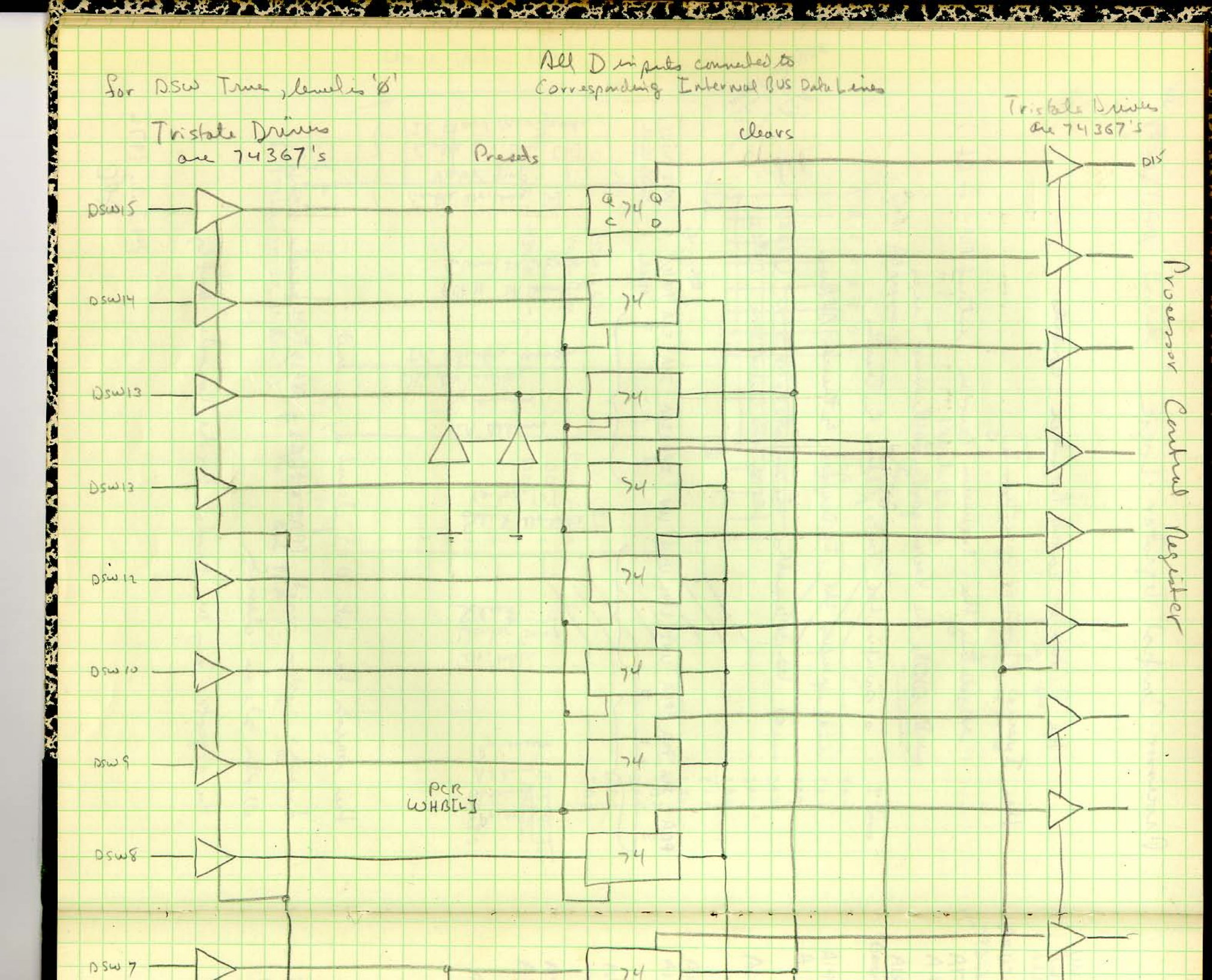
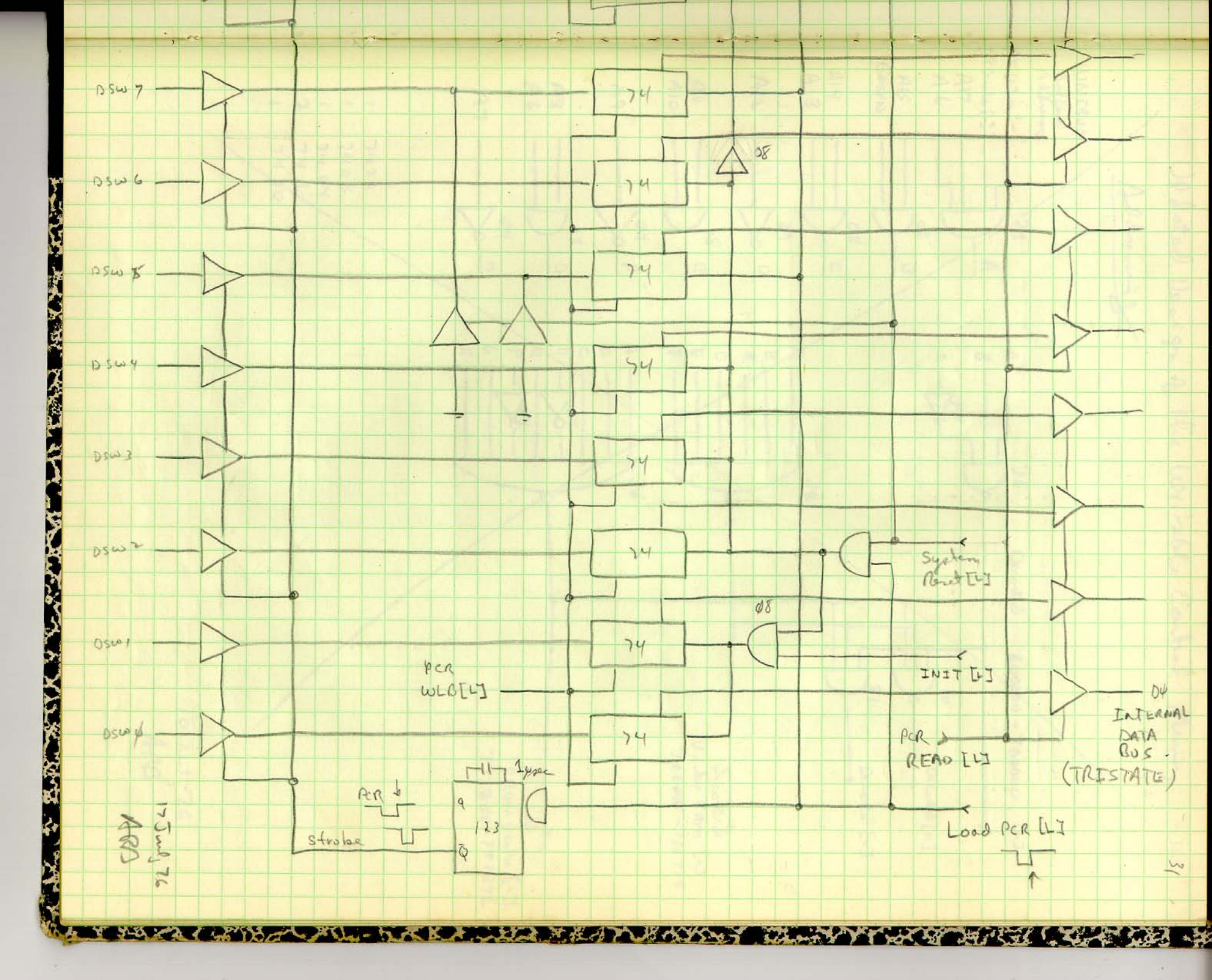
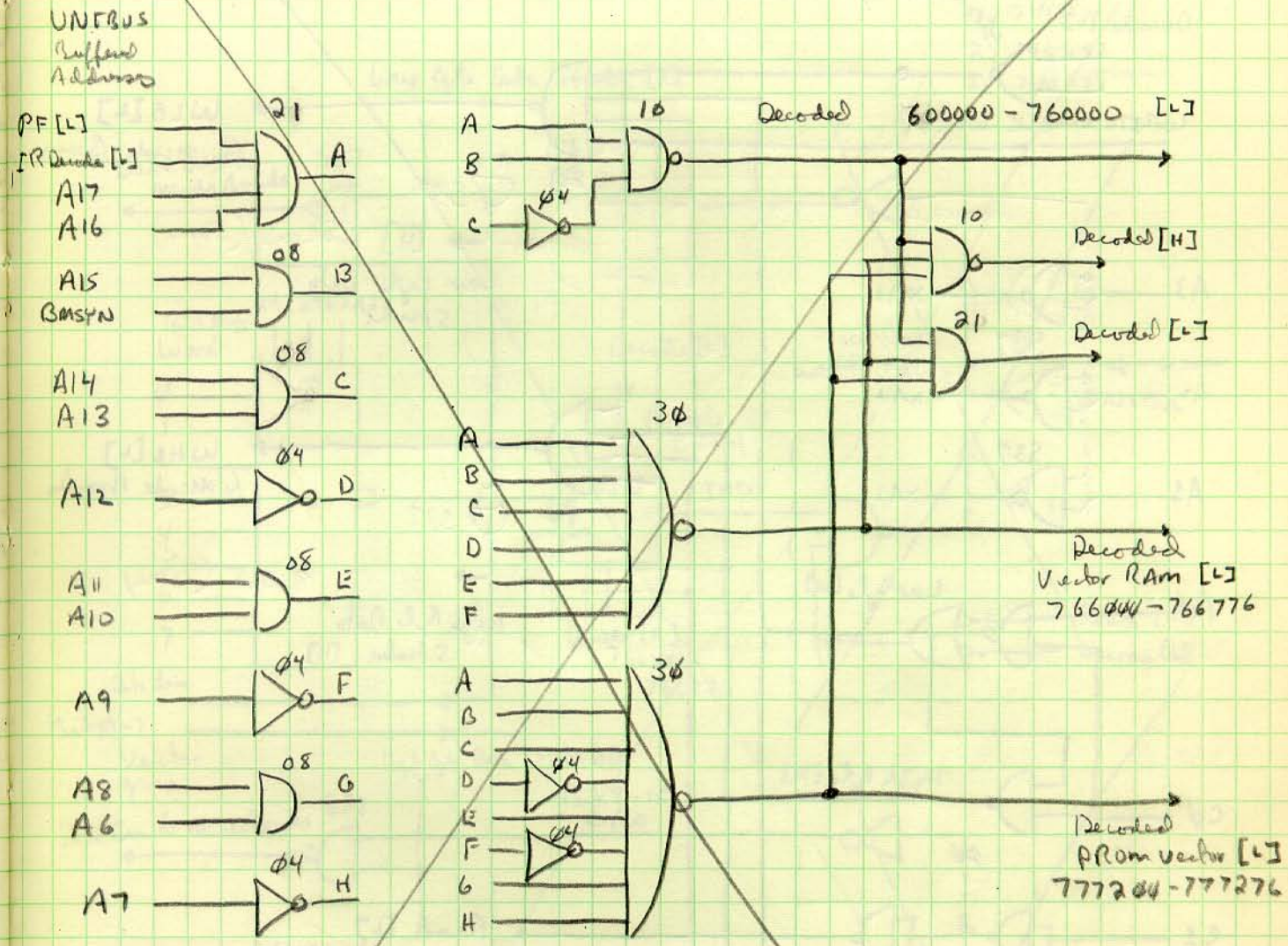
ARB


For DSW True, level is '0'
All D inputs connected to
Corresponding Internal BUS Data Lines
Tristate Drivers
are 74367's
Presets
Clears
Tristate Drivers
are 74367's
DSW15
DSW14
DSW13
DSW12
DSW11
DSW10
DSW9
DSW8
DSW7
74
PCR
WHBIL]
Processor Control Register


DSW 7
DSW 6
DSW 5
DSW 4
DSW 3
DSW 2
DSW 1
DSW 0
74
74
74
74
74
74
74
74
Ø8
Ø8
System Reset [L]
INIT [L]
PCR WLB [L]
PCR READ [L]
Load PCR [L]
Ø4 INTERNAL DATA BUS (TRISTATE)
PCR
strobe
1 sec
9
123
Q

Updated Design of the Writable Control Memory

Addressing

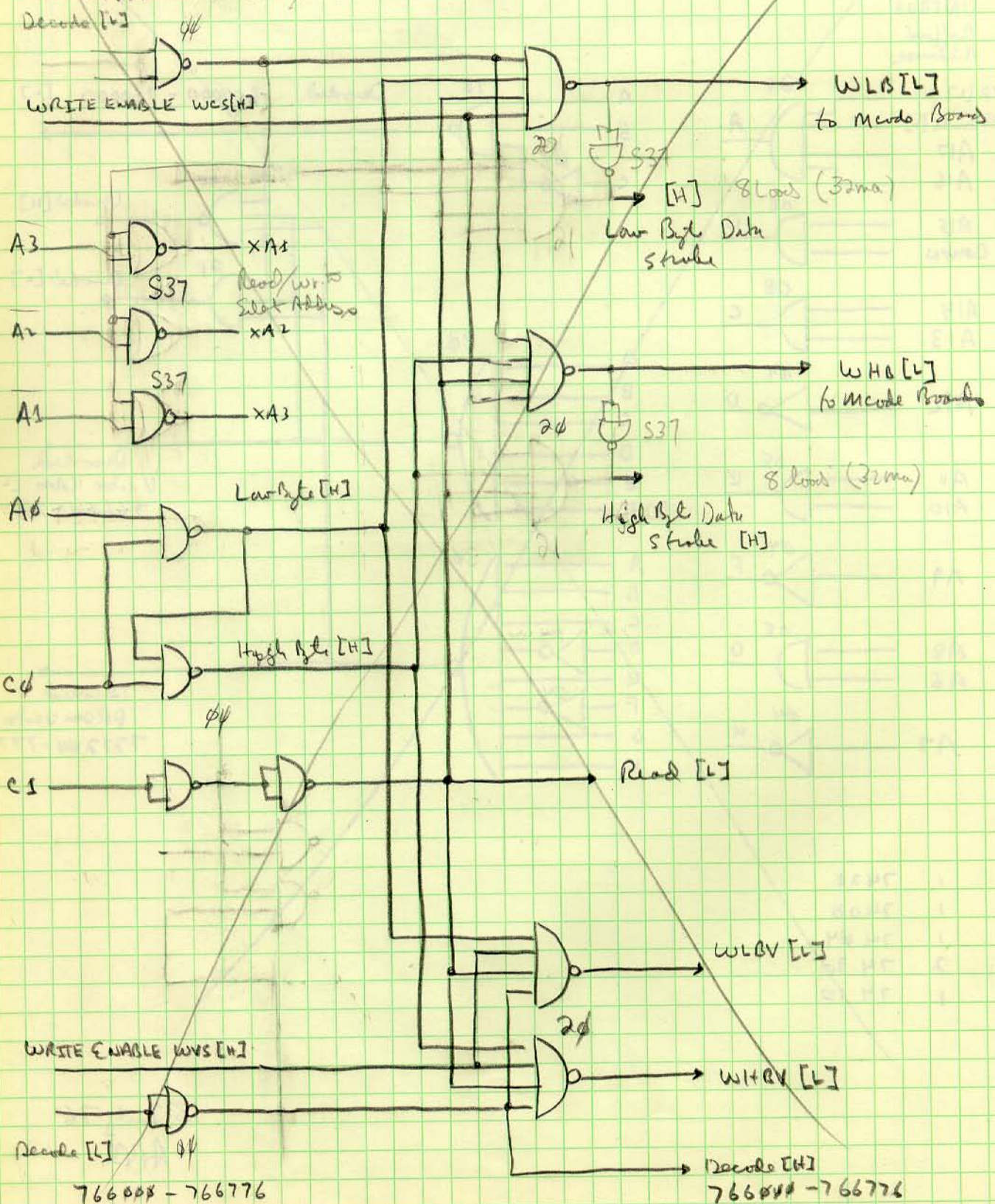


1	7421
1	7408
1	74Ø4
2	7430
1	7410

18 July 76
ARD

Write Control

600000 - 760000 / 76000 - 766777

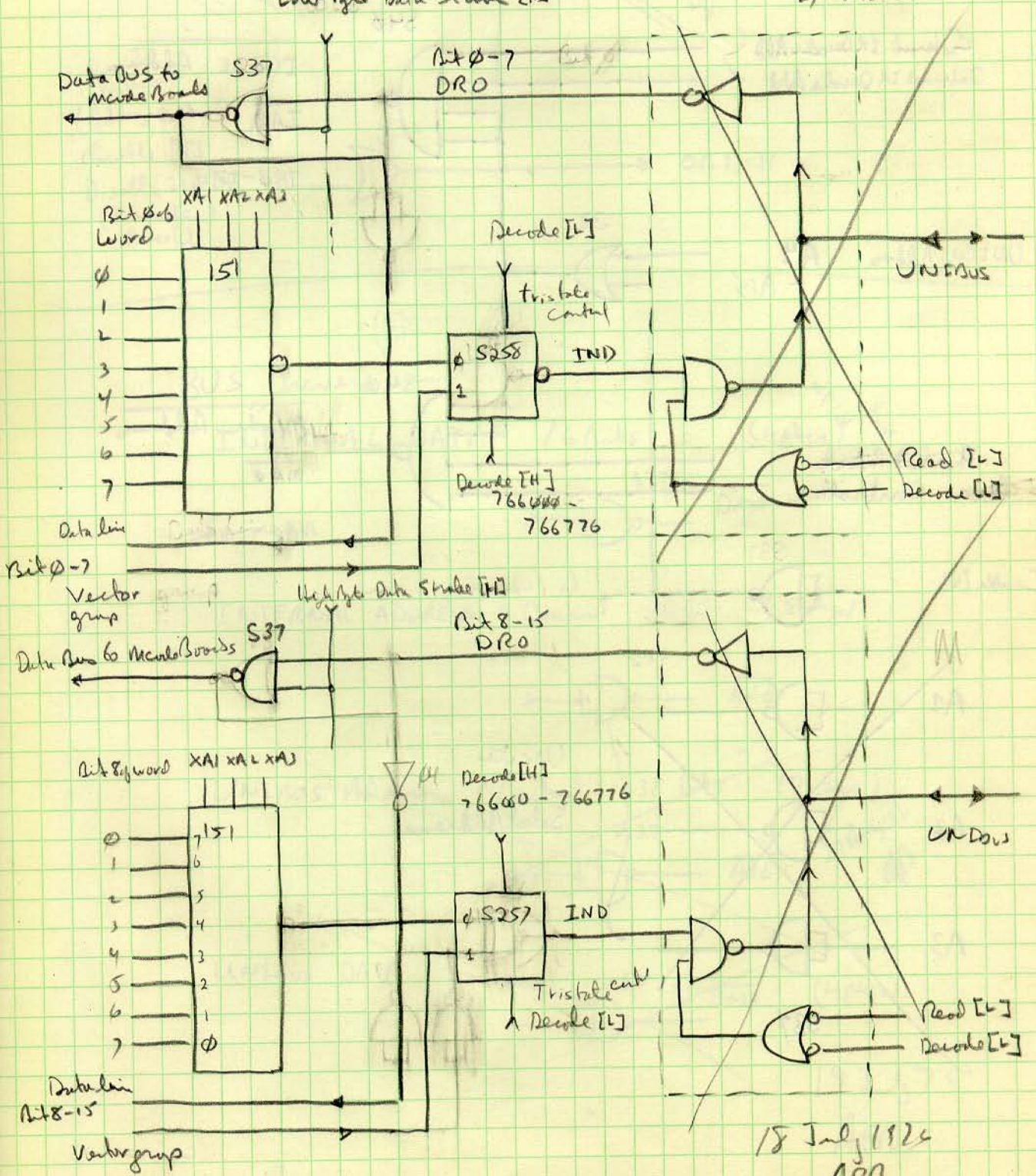


For 16 Bits

DAta Control

two bits of 16 shown

4) 74S37
16) 74151
2) 74S257
2) 74S258

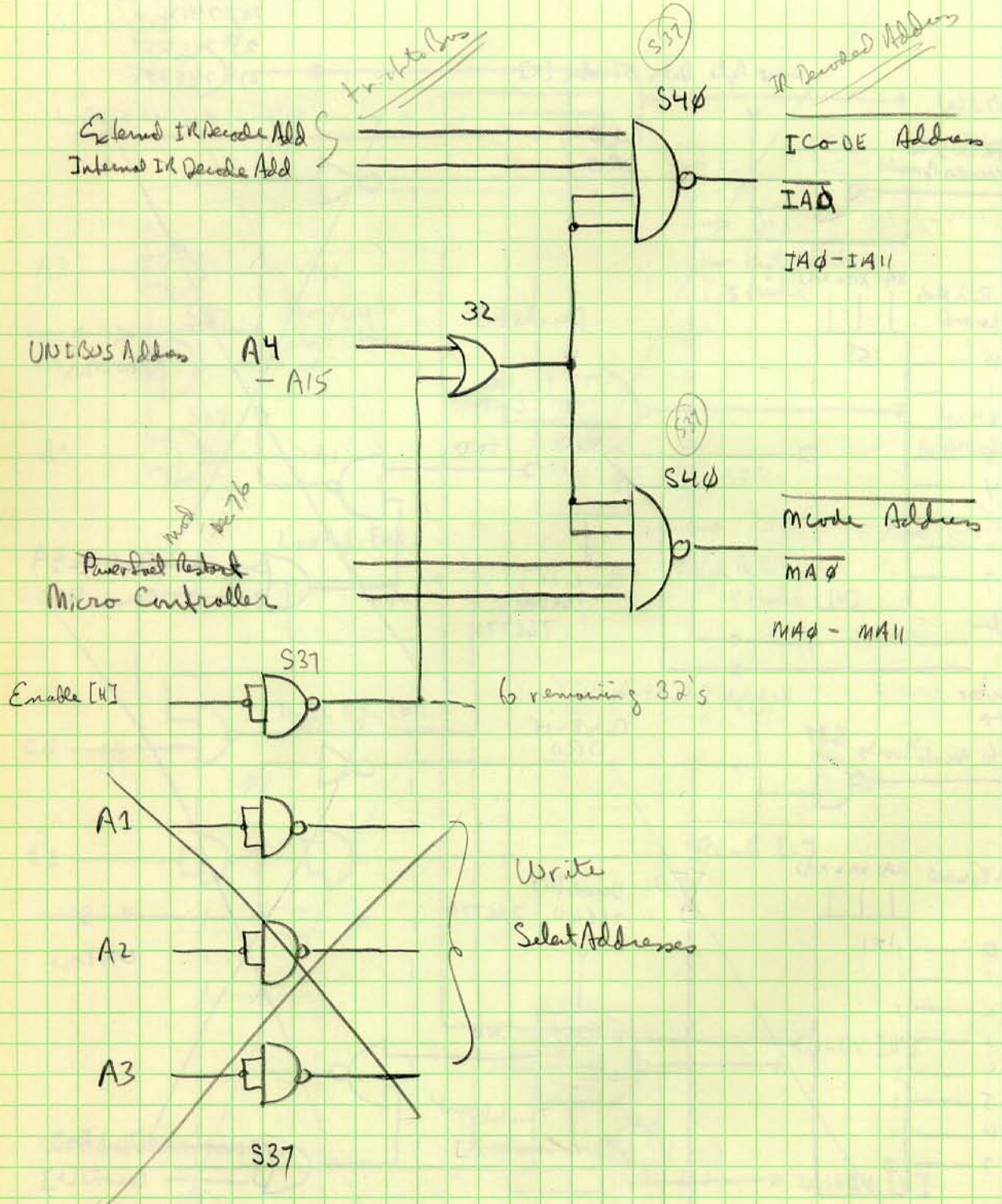


18 Jul 1924

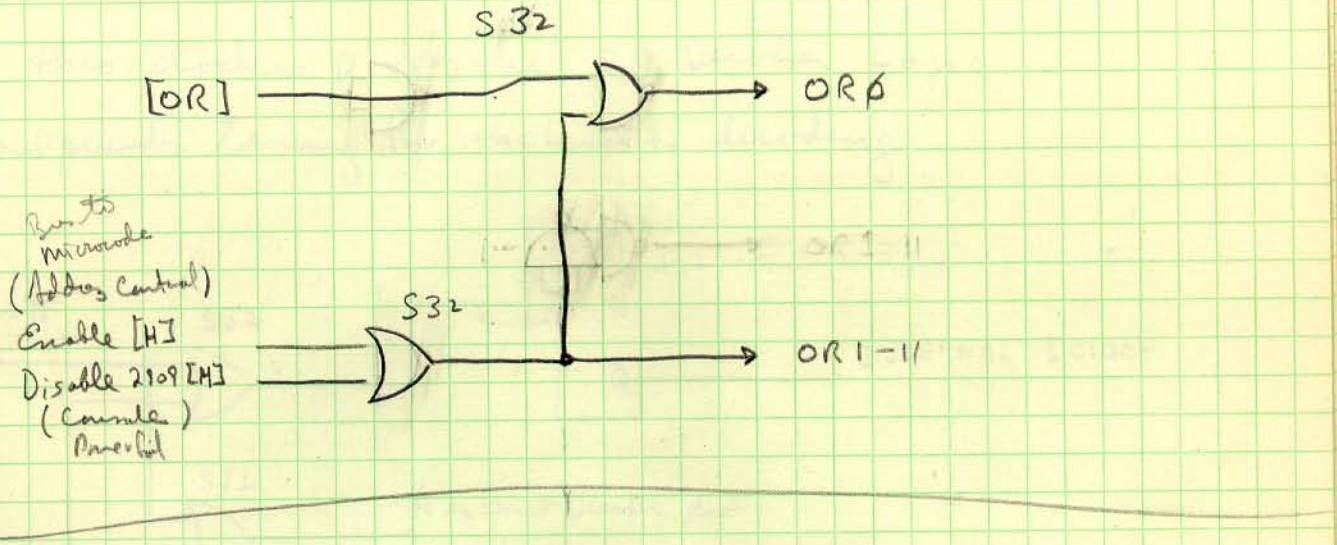
ARB

MCode / Icode Address Drivers

One bit of each shown

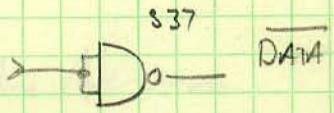


Modification to the Microcontrolla logic

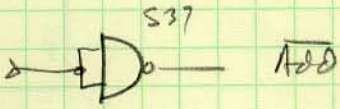


BUS Drivers —

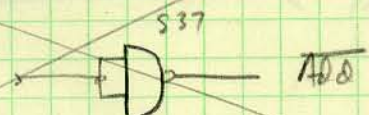
INTERNAL DATA 16 Bits (4 plgs)



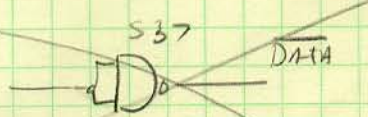
INTERNAL ADDRESS & Control 32 Bits (8 plgs)



UNIBUS Address & Control 32 Bits (8 plgs)



UNIBUS DATA

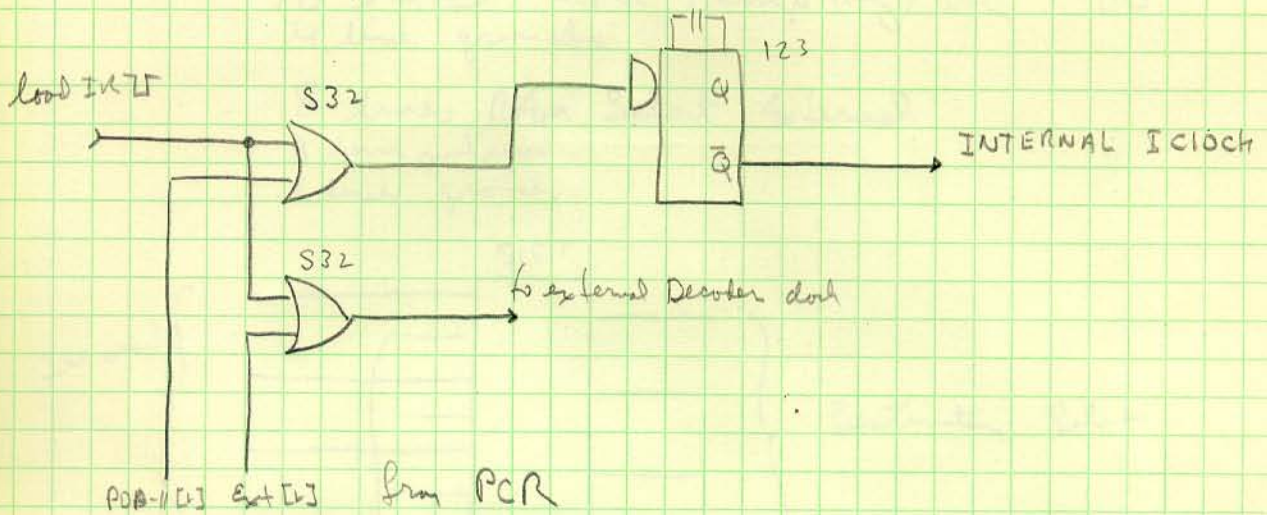


19 July 76

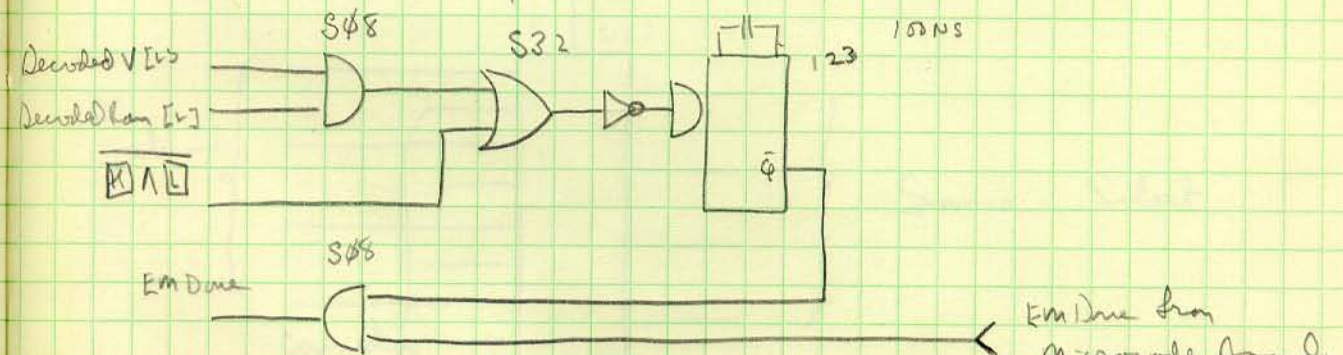
ABD

I Clock timing

This clock is part of the IR Decoder Logic and provides timing for instruction decoding



Vector Read Clock from Unibus Access



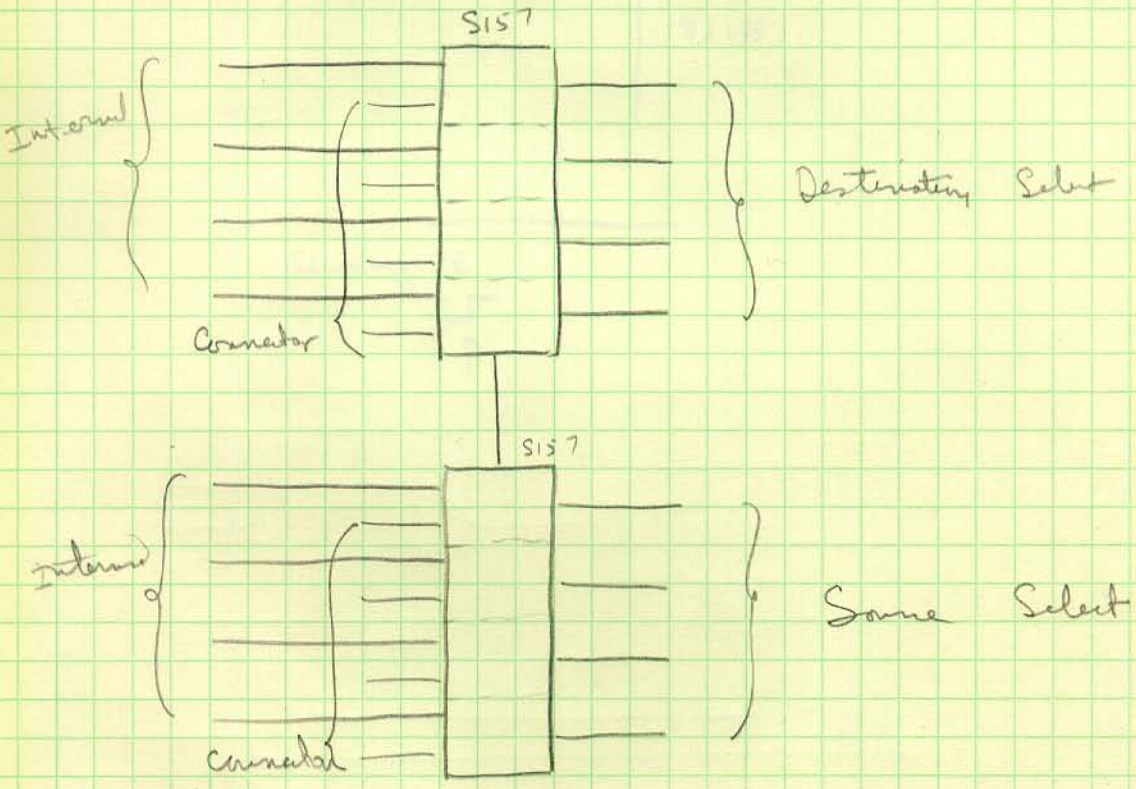
24 July 76
ARB

Modification of the Addressing Selation for Use with the External IR Decoder

1) 40 pin Connector

16 lines CPU Temp Reg/IR [I+J]
4 lines grounds

8 lines RAM Select External
8 lines not used
4 lines grounds



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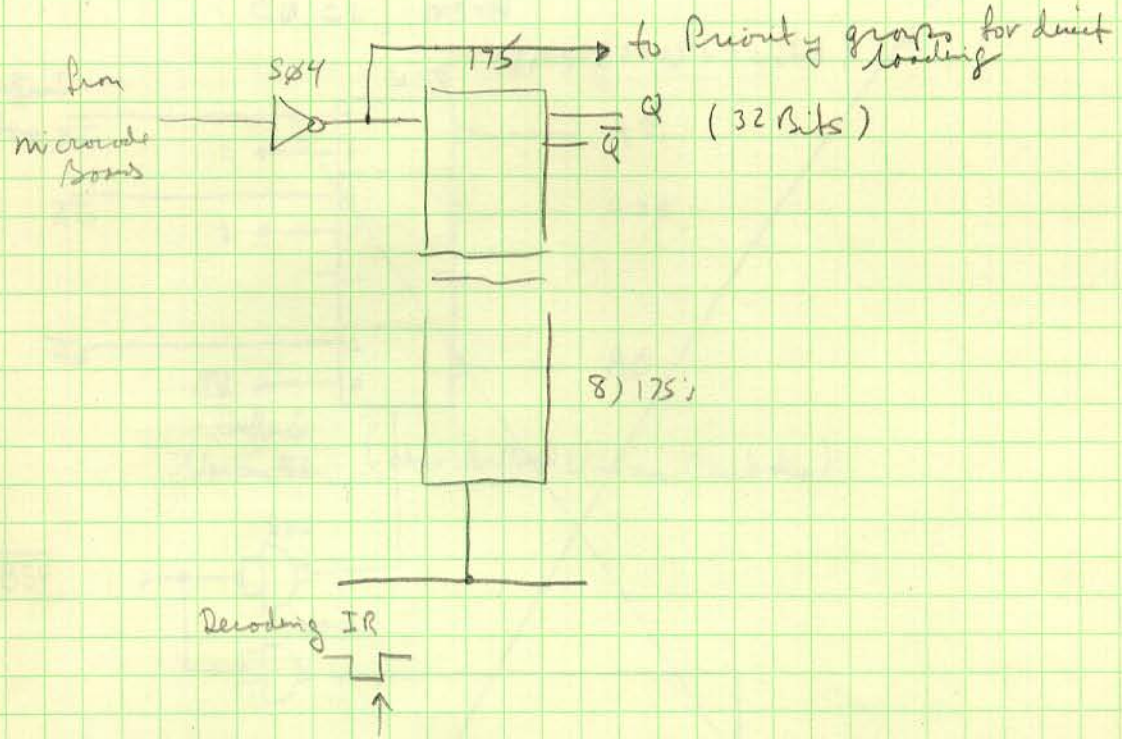
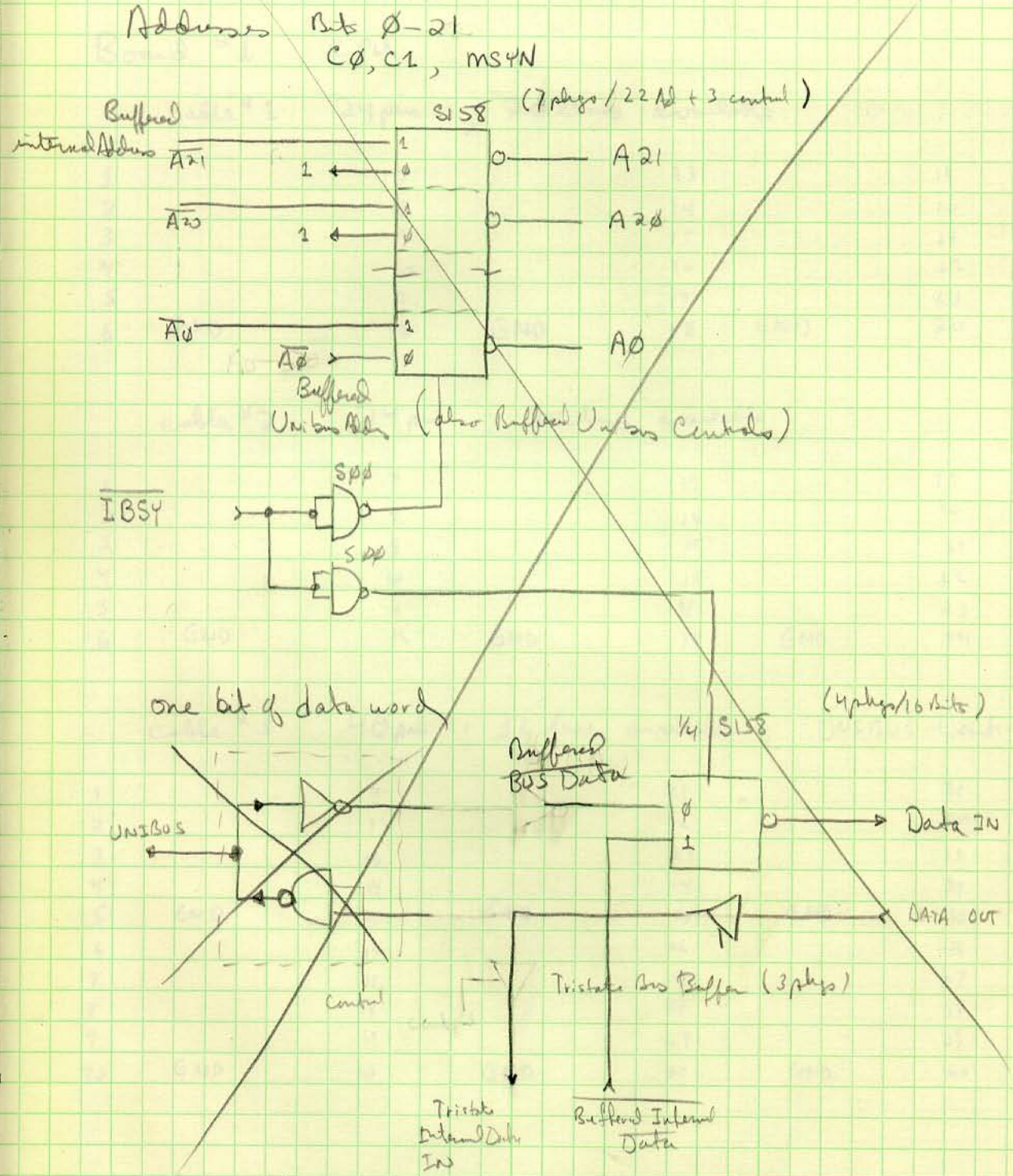
ABS

IR Decode Data Register 32 Bits

loaded at end of instruction load and decode sequence



Memory Control
Dual Port Data/Address/Control Selection



25 July 76
ARB

Current Cable Wiring List - CPU Board

Board #1 CPU

cable #1 24 pin ; 20 lines available ;

1		7		13		19	
2		8		14		20	
3		9		15		21	
4		10		16		22	
5		11		17		23	
6	GND	12	GND	18	GND	24	GND

cable #2 24 pin ; 20 lines available ;

1		7		13		19	
2		8		14		20	
3		9		15		21	
4		10		16		22	
5		11		17		23	
6	GND	12	GND	18	GND	24	GND

cable #3 40 pin ; 32 lines available ; UNIBUS Control

1		11		21		31	
2		12		22		32	
3		13		23		33	
4		14		24		34	
5	GND	15	GND	25	GND	35	GND
6		16		26		36	
7		17		27		37	
8		18		28		38	
9		19		29		39	
10	GND	20	GND	30	GND	40	GND

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AM

Board #2 CPU

Cable #4 40 pin ; 32 lines available ; UNIBUS DATA/ADD lines are Bidirectional OC

1	BD ØØ L	11	BD Ø8 L	21	BA ØØ L	31	BA Ø8 L
2	BD Ø1 L	12	BD Ø9 L	22	BA Ø1 L	32	BA Ø9 L
3	BD Ø2 L	13	BD ØA L	23	BA Ø2 L	33	BA Ø L
4	BD Ø3 L	14	BD 11 L	24	BA Ø3 L	34	BA 11 L
5	GND	15	GND	25	GND	35	GND
6	BD Ø4 L	16	BD 12 L	26	BA Ø4 L	26	BA 12 L
7	BD Ø5 L	17	BD 13 L	27	BA Ø5 L	37	BA 13 L
8	BD Ø6 L	18	BD 14 L	28	BA Ø6 L	38	BA 14 L
9	BD Ø7 L	19	BD 15 L	29	BA Ø7 L	39	BA 15 L
10	GND	20	GND	30	GND	40	GND

cable #7 40 pin ; 32 lines available ; Data Register out / IN DATA
DRO is a direct Bus ; IND is a Tristate Driven Bus

1	DRO Ø	11	DRO 8	21	IND Ø	31	IND 8
2	DRO 1	12	DRO 9	22	IND 1	32	IND 9
3	DRO 2	13	DRO 10	23	IND 2	33	IND 10
4	DRO 3	14	DRO 11	24	IND 3	34	IND 11
5	GND	15	GND	25	GND	35	GND
6	DRO 4	16	DRO 12	26	IND 4	36	IND 12
7	DRO 5	17	DRO 13	27	IND 5	37	IND 13
8	DRO 6	18	DRO 14	28	IND 6	38	IND 14
9	DRO 7	19	DRO 15	29	IND 7	39	IND 15
10	GND	20	GND	30	GND	40	GND

Cable #9 40 pin ; 32 lines available ; Data & PSR to Console

1	DRO Ø	11	DRO 8	21	PSR Ø	31	PSR 8
2	DRO 1	12	DRO 9	22	PSR 1	32	PSR 9
3	DRO 2	13	DRO 10	23	PSR 2	33	PSR 10
4	DRO 3	14	DRO 11	24	PSR 3	34	PSR 11
5	GND	15	GND	25	GND	35	GND
6	DRO 4	16	DRO 12	26	PSR 4	36	PSR 12
7	DRO 5	17	DRO 13	27	PSR 5	37	PSR 13
8	DRO 6	18	DRO 14	28	PSR 6	38	PSR 14
9	DRO 7	19	DRO 15	29	PSR 7	39	PSR 15
10	GND	20	GND	30	GND	40	GND

Board #2 CPU

cable #8 40 pin; 32 lines available; Data to Instruction Register
Data for I Register

1	IRS Ø	11	IRS 8	21	IR Ø	31	IR 8
2	IRS 1	12	IRS 9	22	IR 1	32	IR 9
3	IRS 2	13	IRS 10	23	IR 2	33	IR 10
4	IRS 3	14	IRS 11	24	IR 3	34	IR 11
5	GND	15	GND	25	GND	35	GND
6	IRS 4	16	IRS 12	26	IR 4	36	IR 12
7	IRS 5	17	IRS 13	27	IR 5	37	IR 13
8	IRS 6	18	IRS 14	28	IR 6	38	IR 14
9	IRS 7	19	IRS 15	29	IR 7	39	IR 15
10	GND	20	GND	30	GND	40	GND

cable #2 40 pin; 32 lines available; MMGT Control

1	MM Ø WLS	11	MM 2 WLS	21	RUA Ø	31	
2	MM Ø WHS	12	MM 2 WHS	22	RUA 1	32	
3	MM Ø Read	13	MM 2 Read	23	RUA 2	33	
4	RUB Ø	14		24	RUA 3	34	
5	GND	15	GND	25	GND	35	GND
6	MM 1 WLS	16	XL	26	RUA 4	36	
7	MM 1 WHS	17	XH	27	RUA 5	37	
8	MM 1 Read	18	XA	28	RUA 6	38	
9	RUB 2	19		29	RUA 7	39	
10	GND	20	GND	30	GND	40	GND

cable #3 40 pin; 32 lines available; Internal address Bus & Control
necessary Units Address & Controller

1	IA Ø	11	IA 8	21	IA 16	31	IBBSY
2	IA 1	12	IA 9	22	IA 17	32	IMSYN
3	IA 2	13	IA 10	23	IA 18	33	ISSYN
4	IA 3	14	IA 11	24	IA 19	34	DTOB (Data to Bus)
5	GND	15	GND	25	GND	35	GND
6	IA 4	16	IA 12	26	IA 20	36	RBMSYN
7	IA 5	17	IA 13	27	IA 21	37	RBSSYN
8	IA 6	18	IA 14	28		38	RUA 17
9	IA 7	19	IA 15	29		39	RUA 18
10	GND	20	GND	30	GND	40	GND

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ABM

Board #2 CPU

cable # 1 40 pin; 32 lines available; AD & ADX to Console
Virtual

1	AD Ø	11	AD 8	21	ADX Ø	31	
2	AD 1	12	AD 9	22	ADX 1	32	
3	AD 2	13	AD 10	23	ADX 2	33	
4	AD 3	14	AD 11	24	ADX 3	34	
5	GND	15	GND	25	GND	35	GND
6	AD 4	16	AD 12	26	ADX 4	36	
7	AD 5	17	AD 13	27	ADX 5	37	
8	AD 6	18	AD 14	28		38	
9	AD 7	19	AD 15	29		39	
10	GND	20	GND	30	GND	40	GND

cable # 5 40 pin; 32 lines available; AD & ADX to Console
Physical

1	GAD Ø	11	GAD 8	21	GAD 16	31	C'
2	GAD 1	12	GAD 9	22	GAD 17	32	V'
3	GAD 2	13	GAD 10	23	GAD 18	33	Z'
4	GAD 3	14	GAD 11	24	GAD 19	34	N'
5	GND	15	GND	25	GND	35	GND
6	GAD 4	16	GAD 12	26	GAD 20	36	
7	GAD 5	17	GAD 13	27	GAD 21	37	
8	GAD 6	18	GAD 14	28		38	
9	GAD 7	19	GAD 15	29		39	
10	GND	20	GND	30	GND	40	GND

cable # 6 40 pin; 32 lines available mm6T

1	AD Ø	11	AD 8	21	IA Ø	31	IA 8
2	AD 1	12	AD 9	22	IA 1	32	IA 9
3	AD 2	13	AD 10	23	IA 2	33	IA 10
4	AD 3	14	AD 11	24	IA 3	34	IA 11
5	GND	15	GND	25	GND	35	GND
6	AD 4	16	AD 12	26	IA 4	36	IA 12
7	AD 5	17	AD 13	27	IA 5	37	IA 13
8	AD 6	18	AD 14	28	IA 6	38	IA 14
9	AD 7	19	AD 15	29	IA 7	39	IA 15
10	GND	20	GND	30	GND	40	GND

Board # 1 CPU

Cable # 4 40 pin; 32 available; Control Data Misc

1		11		21		31	
2		12		22		32	
3		13		23		33	
4		14		24		34	
5	GND	15	GND	25	GND	35	GND
6		16		26		36	
7		17		27		37	
8		18		28		38	
9		19		29		39	
10	GND	20	GND	30	GND	40	GND

Cable # 5 40 pin; 32 available

Microcode to Console <63:32>
Buffered microcode

1	Bm 32	11	Bm 40	21	Bm 48	31	Bm 56
2	Bm 33	12	Bm 41	22	Bm 49	32	Bm 57
3	Bm 34	13	Bm 42	23	Bm 50	33	Bm 58
4	Bm 35	14	Bm 43	24	Bm 51	34	Bm 59
5	GND	15	GND	25	GND	35	GND
6	Bm 36	16	Bm 44	26	Bm 52	36	Bm 60
7	Bm 37	17	Bm 45	27	Bm 53	37	Bm 61
8	Bm 38	18	Bm 46	28	Bm 54	38	Bm 62
9	Bm 39	19	Bm 47	29	Bm 55	39	Bm 63
10	GND	20	GND	30	GND	40	GND

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Board #1 CPU

Cable # 6 40 pin; 32 available Microcode to console <31:0>

1	BM 0	11	BM 8	21	BM 16	31	BM 24
2	BM 1	12	BM 9	22	BM 17	32	BM 25
3	BM 2	13	BM 10	23	BM 18	33	BM 26
4	BM 3	14	BM 11	24	BM 19	34	BM 27
5	GND	15	GND	25	GND	35	GND
6	BM 4	16	BM 12	26	BM 20	36	BM 28
7	BM 5	17	BM 13	27	BM 21	37	BM 29
8	BM 6	18	BM 14	28	BM 22	38	BM 30
9	BM 7	19	BM 15	29	BM 23	39	BM 31
10	GND	20	GND	30	GND	40	GND

Cable # 7 40 pin; 32 available TRAP Vector IN & to Control Scratch Pg unit

1	TV 0	11		21	SCR 0	31	SCR 8
2	TV 1	12		22	SCR 1	32	SCR 9
3	TV 2	13		23	SCR 2	33	SCR 10
4	TV 3	14		24	SCR 3	34	SCR 11
5	GND	15	GND	25	GND	35	GND
6	TV 4	16	TBit	26	SCR 4	36	SCR Read Enable
7	TV 5	17		27	SCR 5	37	
8	TV 6	18		28	SCR 6	38	
9	TV 7	19		29	SCR 7	39	
10	GND	20	GND	30	GND	40	GND

SCR write enable decoded on CPU Board (74S138) (I/O Section)

24 Oct 76

Board #3 CPU

cable # 1 40 pin; 32 available Microcode in <95:64>
Direct microcode / Buffer Micro

1	Dm 64	11	Dm 72	21	Bm 80	31	Bm 88
2	Dm 65	12	Dm 73	22	Bm 81	32	Bm 89
3	Dm 66	13	Dm 74	23	Bm 82	33	Bm 90
4	Dm 67	14	Dm 75	24	Bm 83	34	Bm 91
5	GND	15	GND	25	GND	35	GND
6	Dm 68	16	Dm 76	26	Bm 84	36	Bm 92
7	Dm 69	17	Dm 77	27	Bm 85	37	Bm 93
8	Dm 70	18	Dm 78	28	Bm 86	38	Bm 94
9	Dm 71	19	Dm 79	29	Bm 87	39	Bm 95
10	GND	20	GND	30	GND	40	GND

Cable # 2 40 pin; 32 availabl Microcode In <63:32>
Dirct Microcode

1	Dm 32	11	Dm 40	21	Dm 48	31	Dm 56
2	Dm 33	12	Dm 41	22	Dm 49	32	Dm 57
3	Dm 34	13	Dm 42	23	Dm 50	33	Dm 58
4	Dm 35	14	Dm 43	24	Dm 51	34	Dm 59
5	GND	15	GND	25	GND	35	GND
6	Dm 36	16	Dm 44	26	Dm 52	36	Dm 60
7	Dm 37	17	Dm 45	27	Dm 53	37	Dm 61
8	Dm 38	18	Dm 46	28	Dm 54	38	Dm 62
9	Dm 39	19	Dm 47	29	Dm 55	39	Dm 63
10	GND	20	GND	30	GND	40	GND

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ARD

Board 3 CPU

Cable # 3 40 pin ; 32 available Microcode in <31:0>
Direct microcode

1	Dm 0	11	Dm 8	21	Dm 16	31	Dm 24
2	Dm 1	12	Dm 9	22	Dm 17	32	Dm 25
3	Dm 2	13	Dm 10	23	Dm 18	33	Dm 26
4	Dm 3	14	Dm 11	24	Dm 19	34	Dm 27
5	GND	15	GND	25	GND	35	GND
6	Dm 4	16	Dm 12	26	Dm 20	26	Dm 28
7	Dm 5	17	Dm 13	27	Dm 21	37	Dm 29
8	Dm 6	18	Dm 14	28	Dm 22	38	Dm 30
9	Dm 7	19	Dm 15	29	Dm 23	39	Dm 31
10	GND	20	GND	30	GND	40	GND

Cable # 4 40 pin; 32 available (IR Decoded Data / Select Data)

1	(000 IR (CPUD) (→)	11	XL	21	SRC 0	31	Byte
2	IRLD (→)	12	XH	22	SRC 1	32	Special
3	IRHD (→)	13	XA	23	SRC 2	33	NDA
4	Stall IR Decode (→)	14		24	SRC 3	34	C Lookahead
5	GND	15	GND	25	GND	35	GND
6	IR Decode (←)	16		26	DST 0	36	WLB Strobe
7	PCR WLB (→)	17		27	DST 1	37	WHB Strobe
8	PCR WHB (→)	18		28	DST 2	38	Read Strobe
9	PCR Read (→)	19		29	DST 3	39	
10	GND	20	GND	30	GND	40	GND

Board #4 CPU

Cable # 1 40 pin 32 available Data Switch / Control Switch from Console

1	DS Ø	11	DS 8	21	DS 16	31	CS Ø
2	DS 1	12	DS 9	22	DS 17	32	CS 1
3	DS 2	13	DS 10	23	DS 18	33	CS 2
4	DS 3	14	DS 11	24	DS 19	34	CS 3
5	GND	15	GND	25	GND	35	GND
6	DS 4	16	DS 12	26	DS 20	36	CS 4
7	DS 5	17	DS 13	27	DS 21	37	CS 5
8	DS 6	18	DS 14	28	~~—/—~~	38	CS 6
9	DS 7	19	DS 15	29	~~—/—~~	39	CS 7
10	GND	20	GND	30	GND	40	GND

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ABO

I/O Control

CPU BOARD #1 Layout

PRI	PRI	INT	INT	BG Rq W Pri4	BR Rq 8	I/O & Interrupt 1 Control	2	UNIBUS 3
S175	S04	X	33					

PRI	PRI	PRI	INT	INT	BUS Rec	Rq NPR NPG (3)	TMOT	TMOT Rqo INIT	BUSI/O	Rqo SACK IR SSYN ODSY	BUSI/O	Rqo ACLO DCLO INIT MSYN	X	X
S175	S11	S10	S04	S10	9837		8838		8838		8838			

PRI	PRI	PRI	INT	INT	NPR	BUSI/O	INIT	INIT	INIT	BUSY	BUSY	LOAD	LOAD	LOAD
S175	S11	S10	L04	S00	S20	7438	S24	121	00	S00	S10	S0	S02	A0

PRI	PRI	PRI	Int	Int	NPR					BUSY	BUSY	LOAD	LOAD	LOAD
S26	S04	148	00	S34	S24	S10	S175	S175	S175	S34	L00	L00	S34	S00

	PRI	PRI	CLI/O	CLI/O						FCLI/O	FCLI/O	LOAD	LOAD	LOAD
X	42	S00	S04	S11	S00	S32	S175	S175	S175	S30	S04	L00	L24	S00

X	X	X	X	mmGT Cnst	X	Control	ODDPC	CPCI Code	Control	control	mmGT 60	60H	INH DATIR	CLI/O
				153		00	20	00	00	10	S74	S74	S34	S30

Control Data 32 bits misc 4	microcode out (63:32) 5	microcode out (31:00) 6	Trap vector In SAC out 7

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CPU Board V3

Arithmetic Logic

CPU

UNIBUS 16 Data

4 Control ADR APX (Virtual)

MM 67 Control

Internal Address + Control

1

2

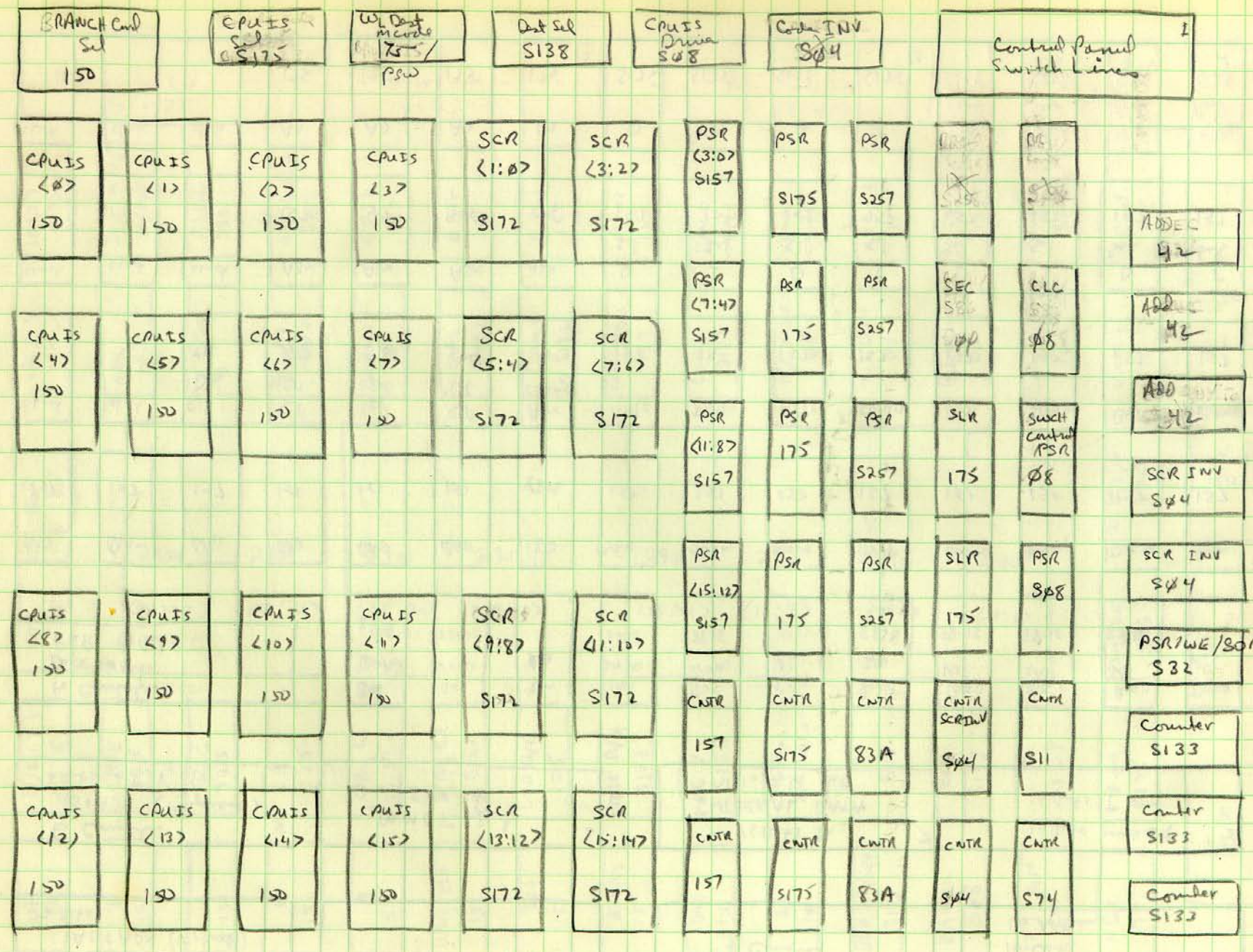
3

1	2	3	4
to Console AD & ADX (Virtual) 22 Bits	MMGT control	Internal Address + Control	UNIBUS 16 Data 16 Address
5	**6**	**7**	**8**
to Console AD & ADX (Physical) 22 Bits + C', V', Z', N'	MMGT Data In/out	16 Bits In INTERNAL DATA 16 Bits out	16 Bits → IR 16 Bits T ←

9															
to Console Data 16 Bits PSR 16 Bits	BUS I/O AD 8838	BUS I/O AD 8838	Tem Reg	BUS I/O AD 8838	BUS I/O AD 8838	Tem Reg	BUS I/O 8838	BUS I/O 8838	BUS I/O 8838	BUS I/O 8838	TERR Reg				
	DAD 157	DAD 157	DAD 157	DAD 157	BAD 157	BAD 157	I/O 8838	BUSM 157	BUSM 157	BUSM 157	BUSM 157	BUSM 157	BUSM 157	BUSM 157	BUSM 157
	clock	clock	Sel Drs S11	Sel IR S08	Sel IR S08	Sel IR S74	ADX coding S11	BYTE 157	ID/UD 157	BYTE 157	ID/UD 157	BYTE 157	ID/UD 157	BYTE 157	ID/UD 157
	clock	clock	clock	ADX 157	ADX 157	ADX 175	ADX 175	D Sel 157	I Sel 157	D Sel 157	I Sel 157	D Sel 157	I Sel 157	D Sel 157	I Sel 157
	clock	clock	clock	AD 175	AD 175	AD 175	AD 175	D S175	D S175	D S175	D S175	IR/SW Read S258	IR/SW Read S258	IR/SW Read S258	IR/SW Read S258

4 Aug 76 ARD

CPU Board 4 Select / PSR / SCR / Counter

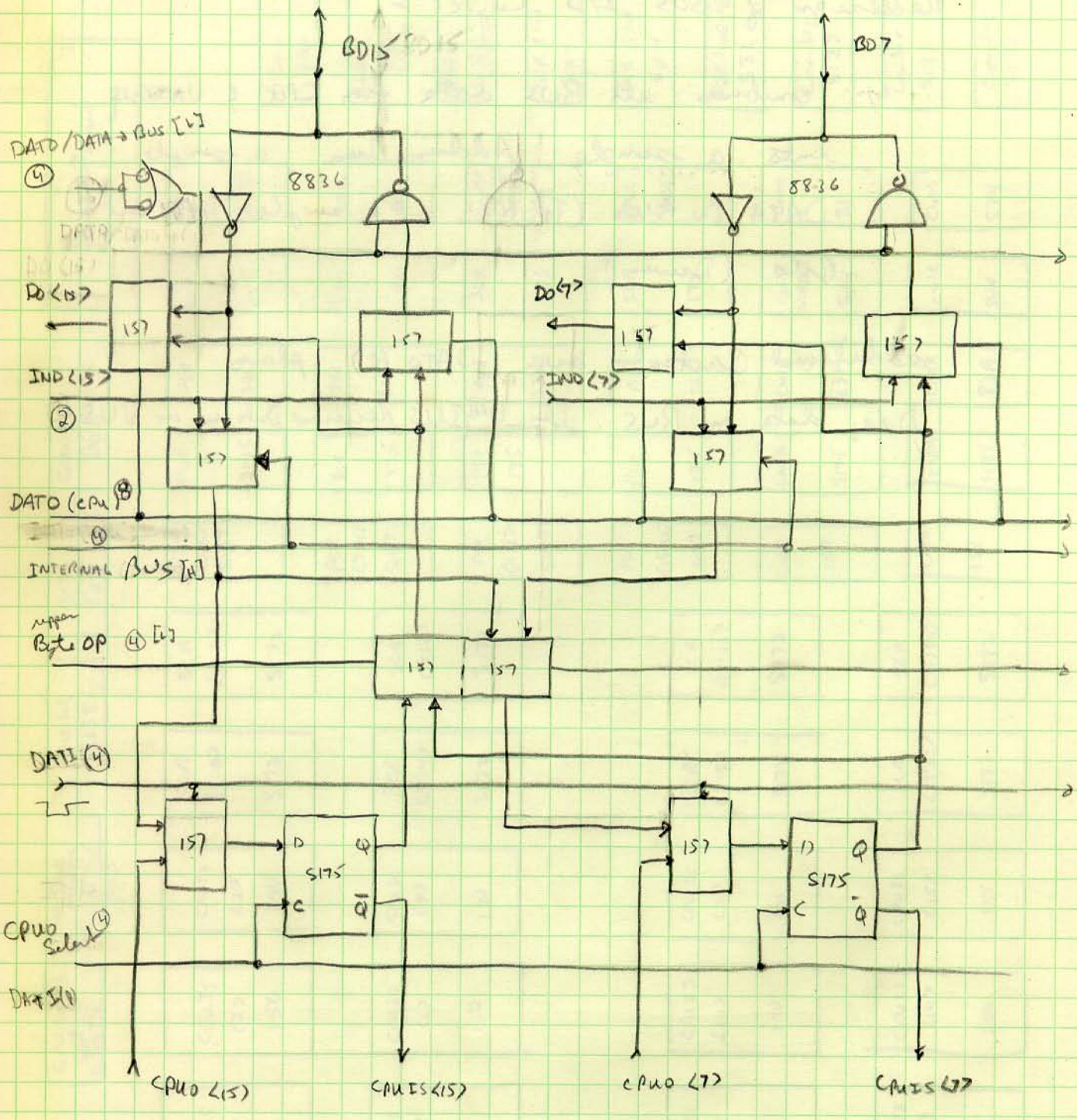


Redesign of BUS I/O Logic -

a) combines all BUS data from CPU & UNIBUS into a single Address Bus, a single DATA IN BUS (Tristate) and a single DATO out BUS (Driven)

additional Controls are DATO (B) places D Reg data on BUS else UNIBUS Received Data is on BUS

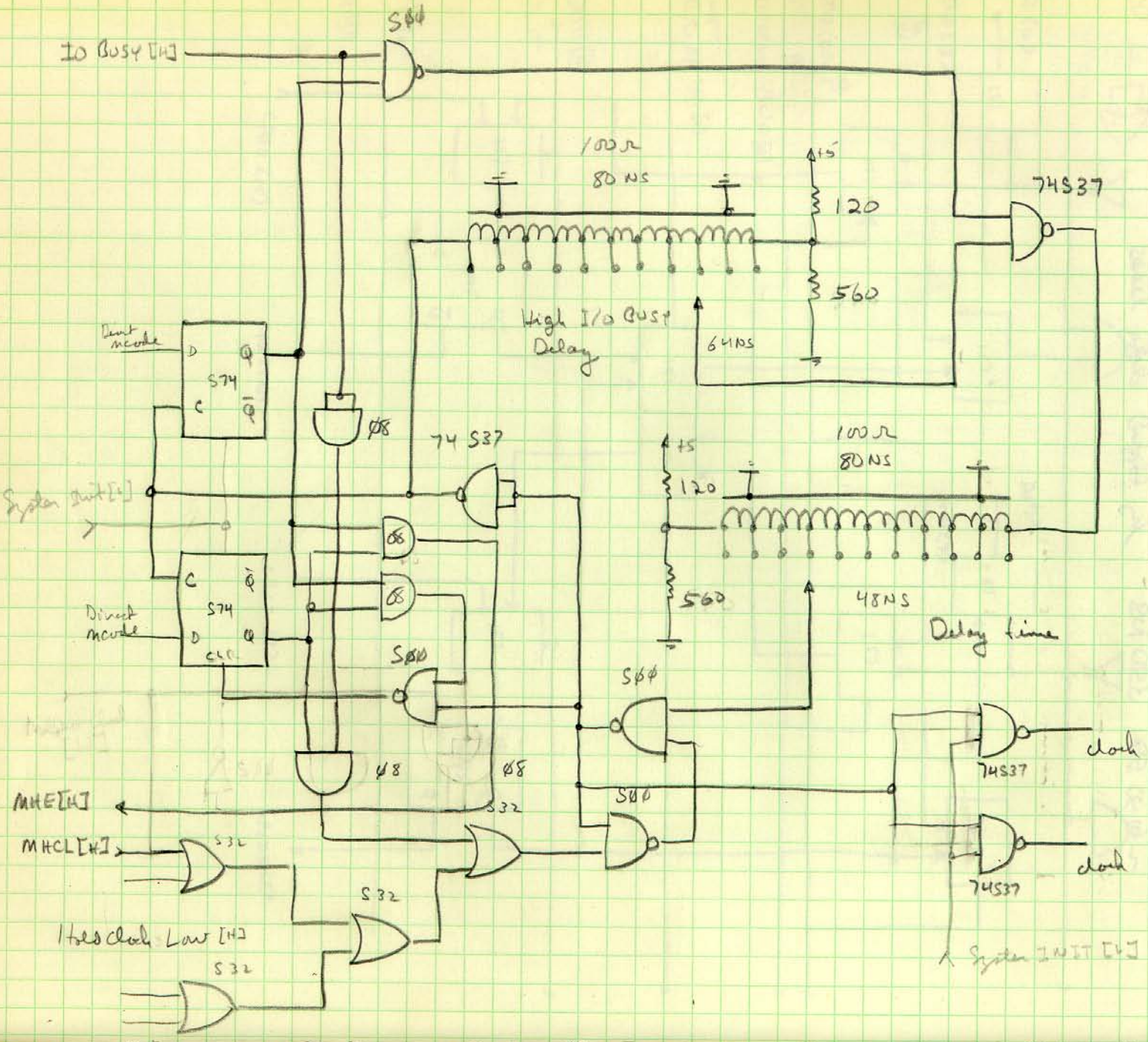
13 Aug 76
AFB


BD15
BD7
DATO/DATA → BUS [L]
8836
8836
DATA
DO<15>
DO<7>
157
157
157
157
157
157
IND<15>
IND<7>
DATO (CPU)
INTERNAL BUS [H]
upper Byte OP [L]
157
157
DATI
157
157
D
Q
S175
C
Q
D
Q
S175
C
Q
CPUO Select
DATI(H)
CPUO<15>
CPUIS<15>
CPUO<7>
CPUIS<7>

Redesign of CPU Clock

provides selectable clock rates in 16 NS intervals from

~ 150 to 350 NS by tapped delay line


IO Busy [H]
S04
100 Ω
80 NS
+5
120
560
74S37
High I/O Busy Delay
64NS
Inst mCode
D
Q
S74
C
Q̄
Ø8
74 S37
System Init [L]
Direct mCode
CLR
S00
S04
48NS
Delay time
clock
MHE [H]
MHCL [H]
S32
Holds clock Low [H]
System INIT [L]

Redesigning the IR Register logic

a) include CPU loading

b) memory addressing

c) IR loading

d) instruction decoding

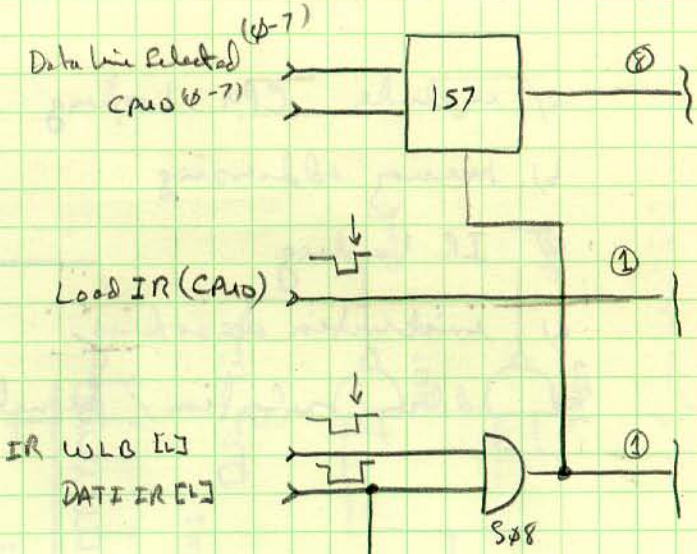
e) address selection / Branch coding

On CPU Board

① Operations

1) Load IR (CPU0)

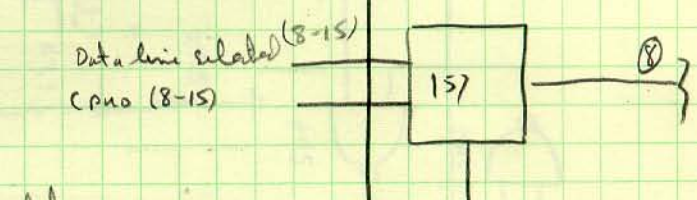
* No decoding
store data in
instruction Register
Banks 1 & 2
for Microcode
Address selection and
branch selection



2) DATI IR

* load 1st rank I register
by BUS Controller
set IR Loaded Flag

* initiate I reg decoding
when WI/O L or H is asserted
clear I/O Busy at time IR is decoded
and transfer 1st rank I reg into
2nd rank I Reg.

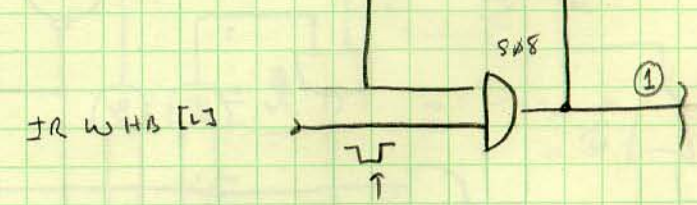


3) BUS addressed (WLB/WHB)

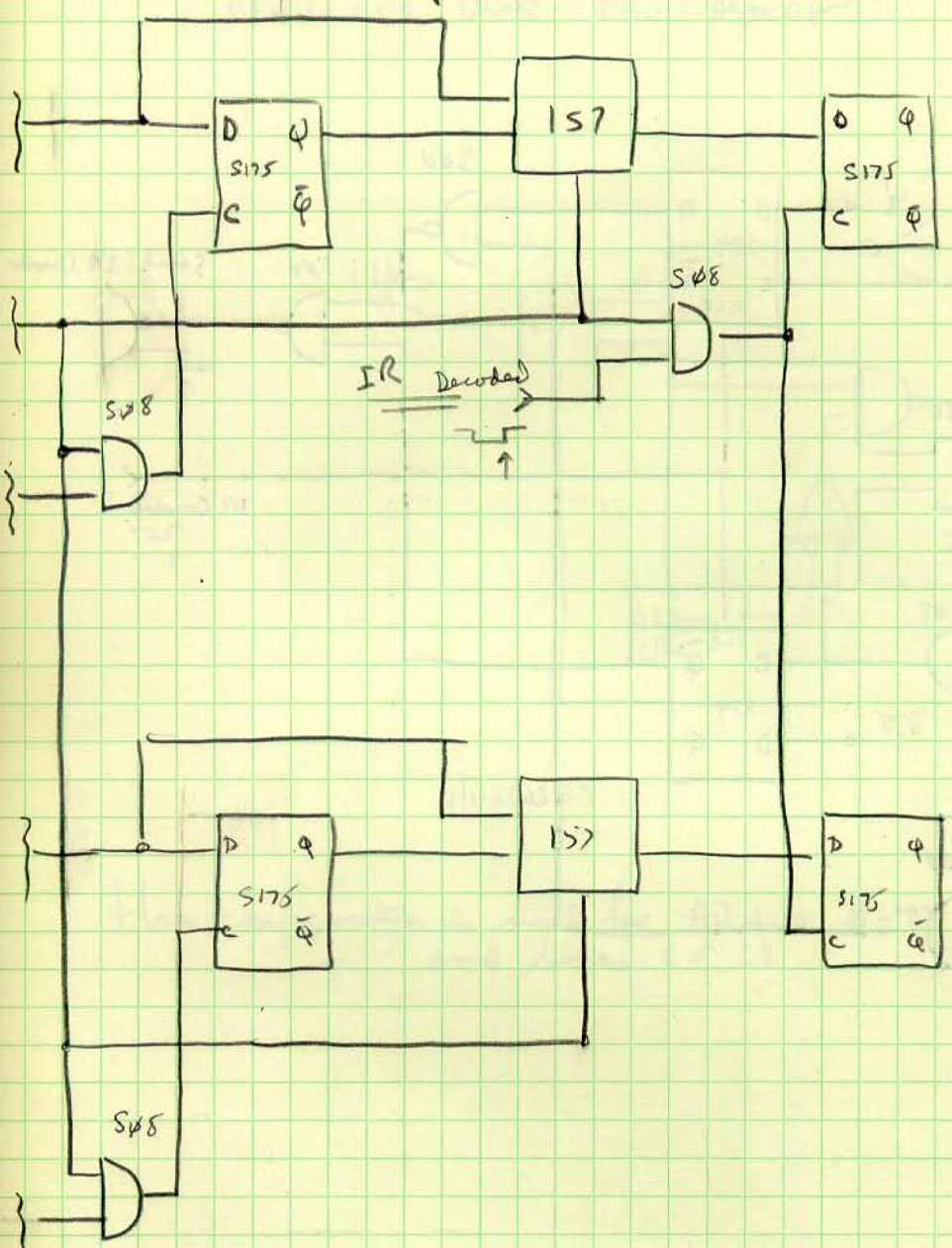
Load 1st rank I register
by Bus Control

* set IR flag, I/O Busy, decode IR

load 2nd rank I reg, clear I/O Busy

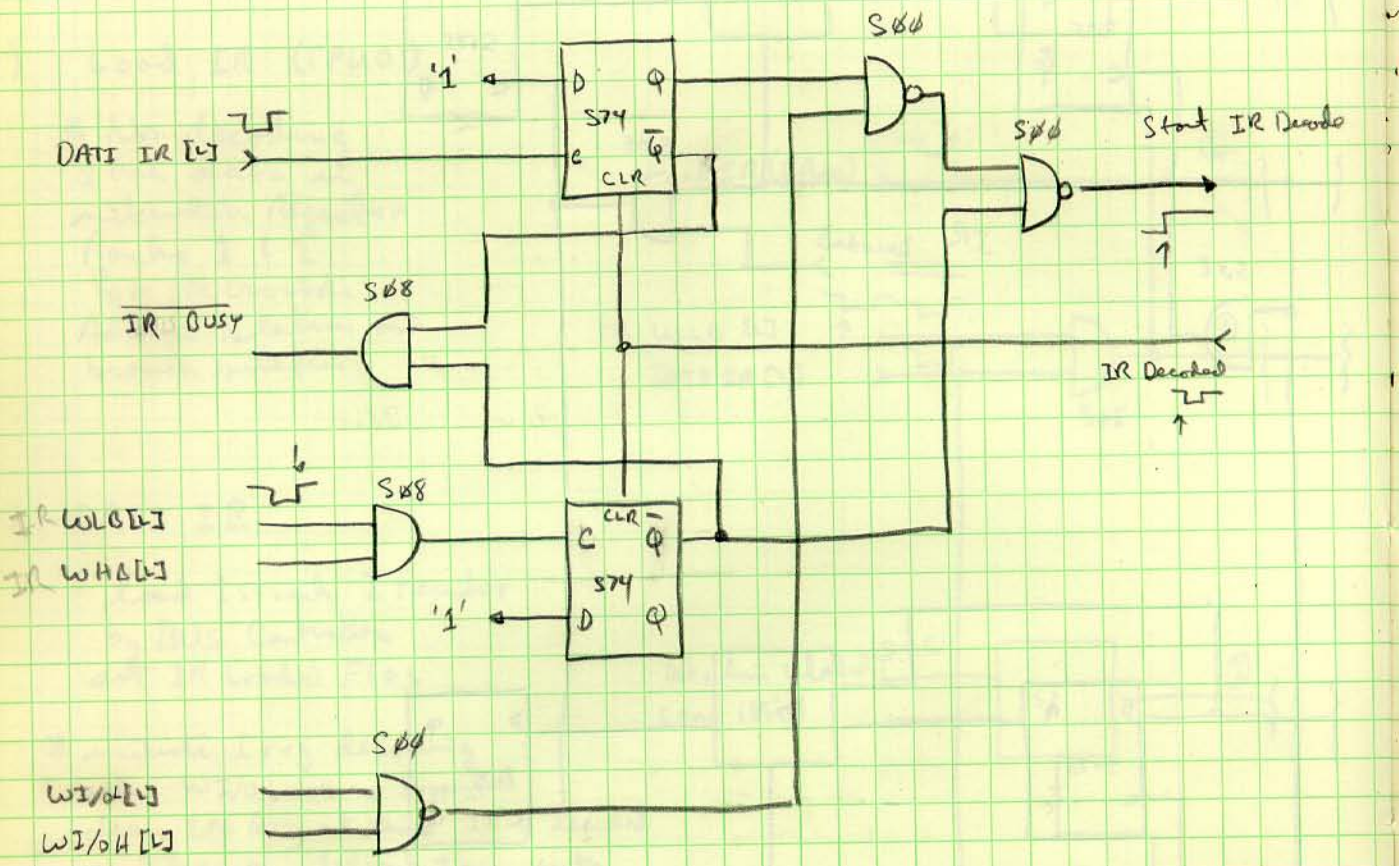


on Priority/Decoder Board

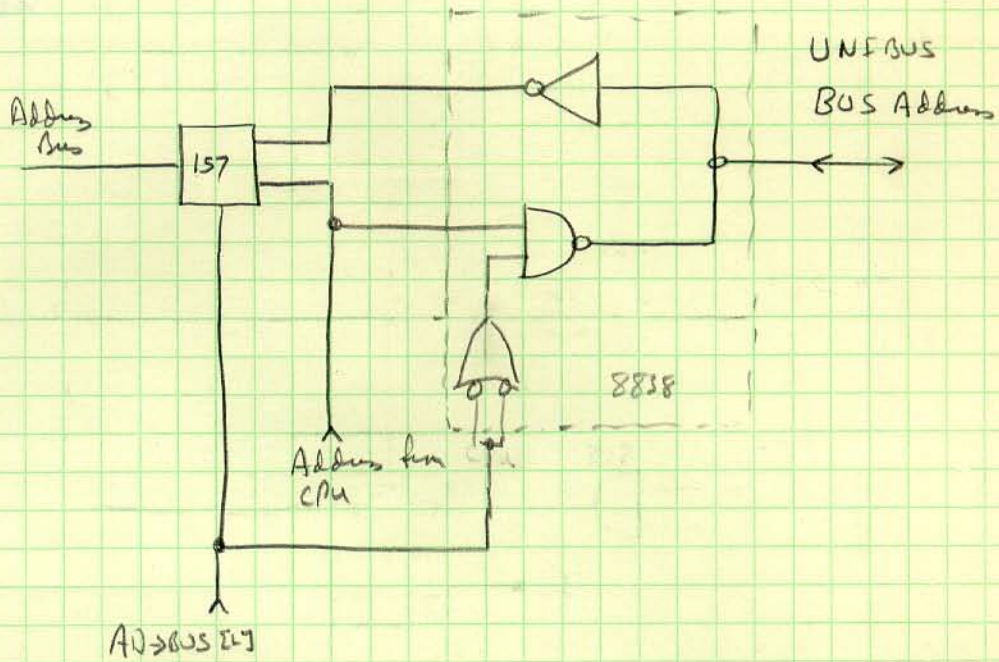


27 Aug 1976
ARB

IR Decode Control / on CPU Board



Address Bus Multiplexer

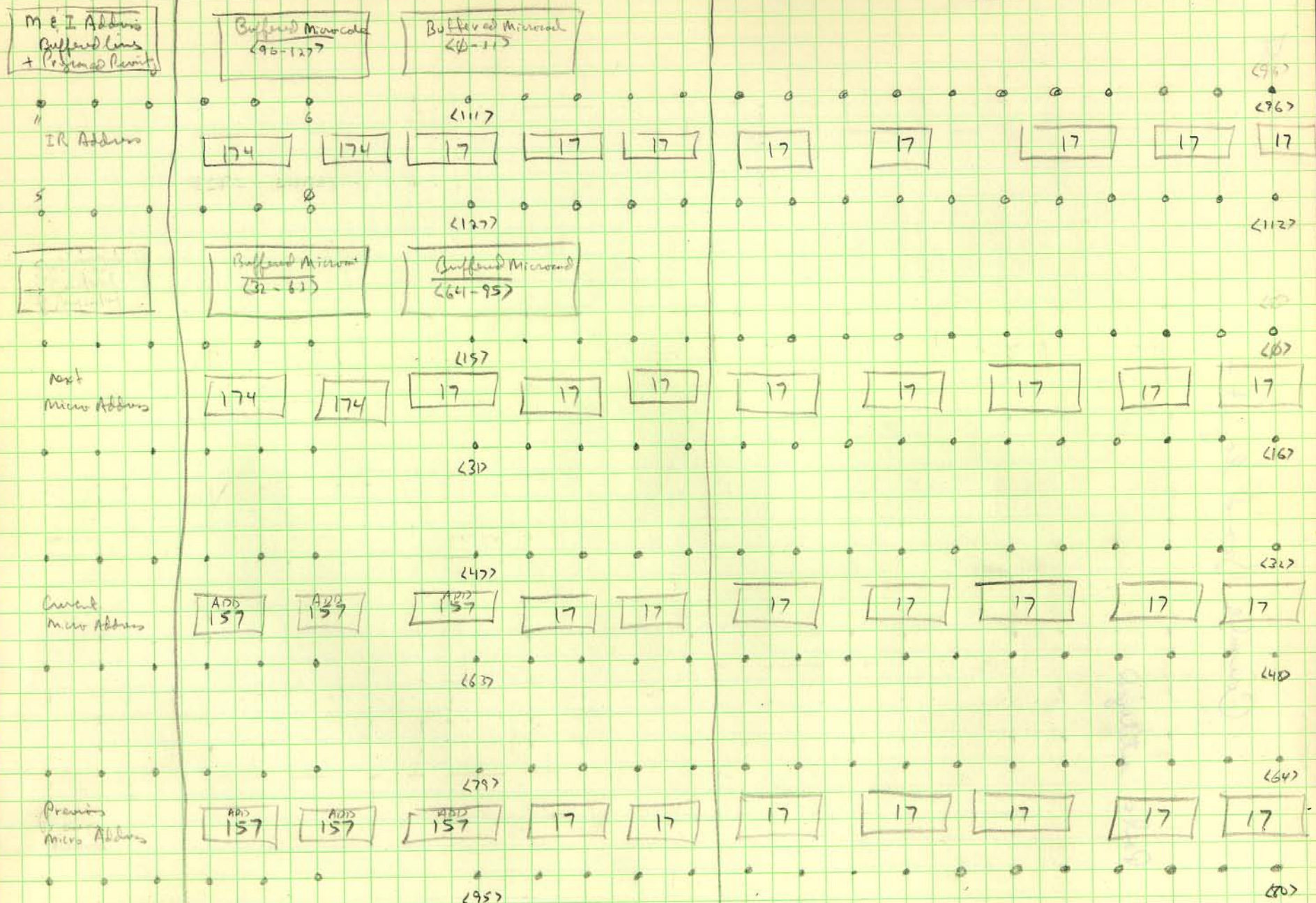


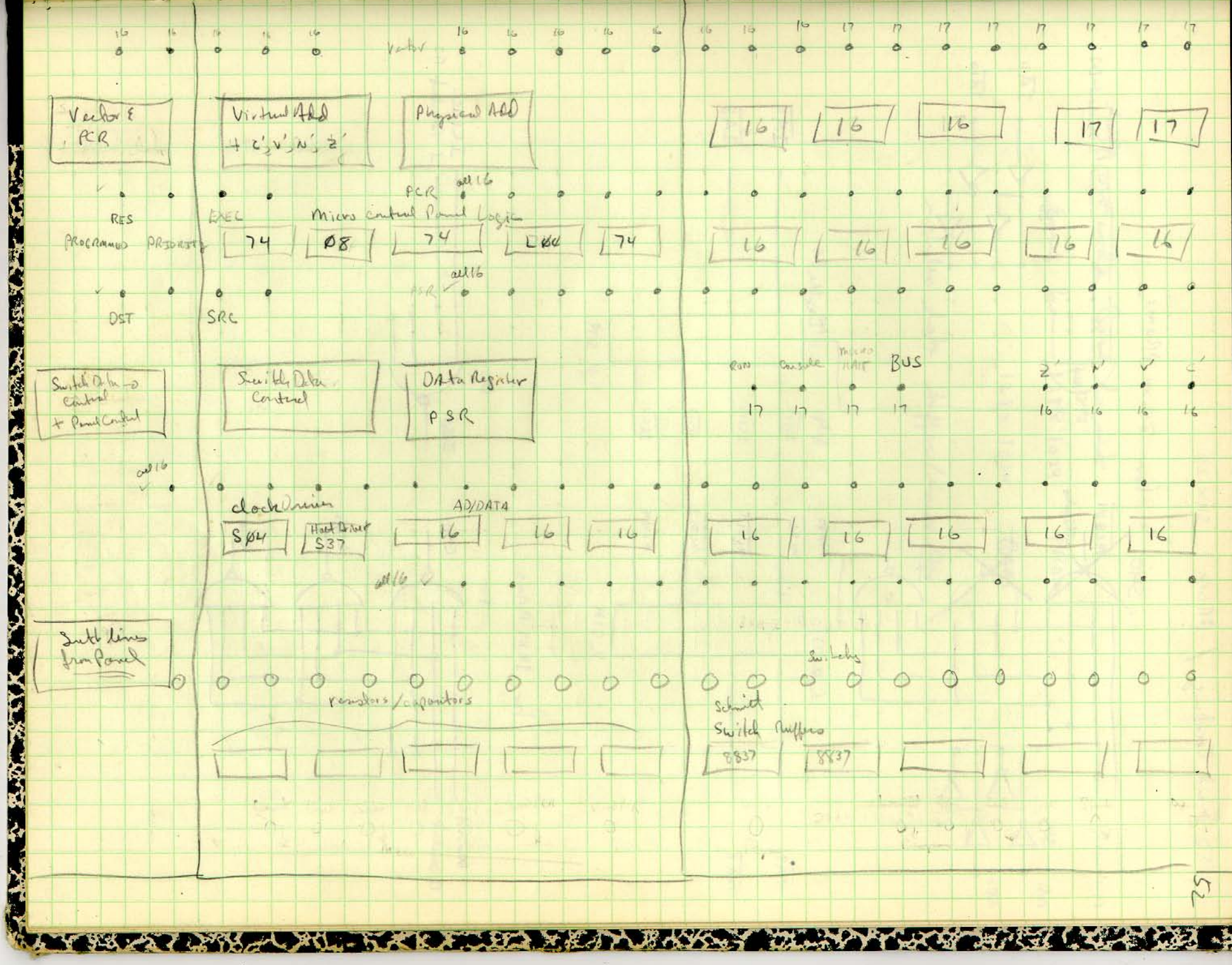
This configuration is used for AD bits Ø - 21 and lines CØ, C1

Console Board layout -

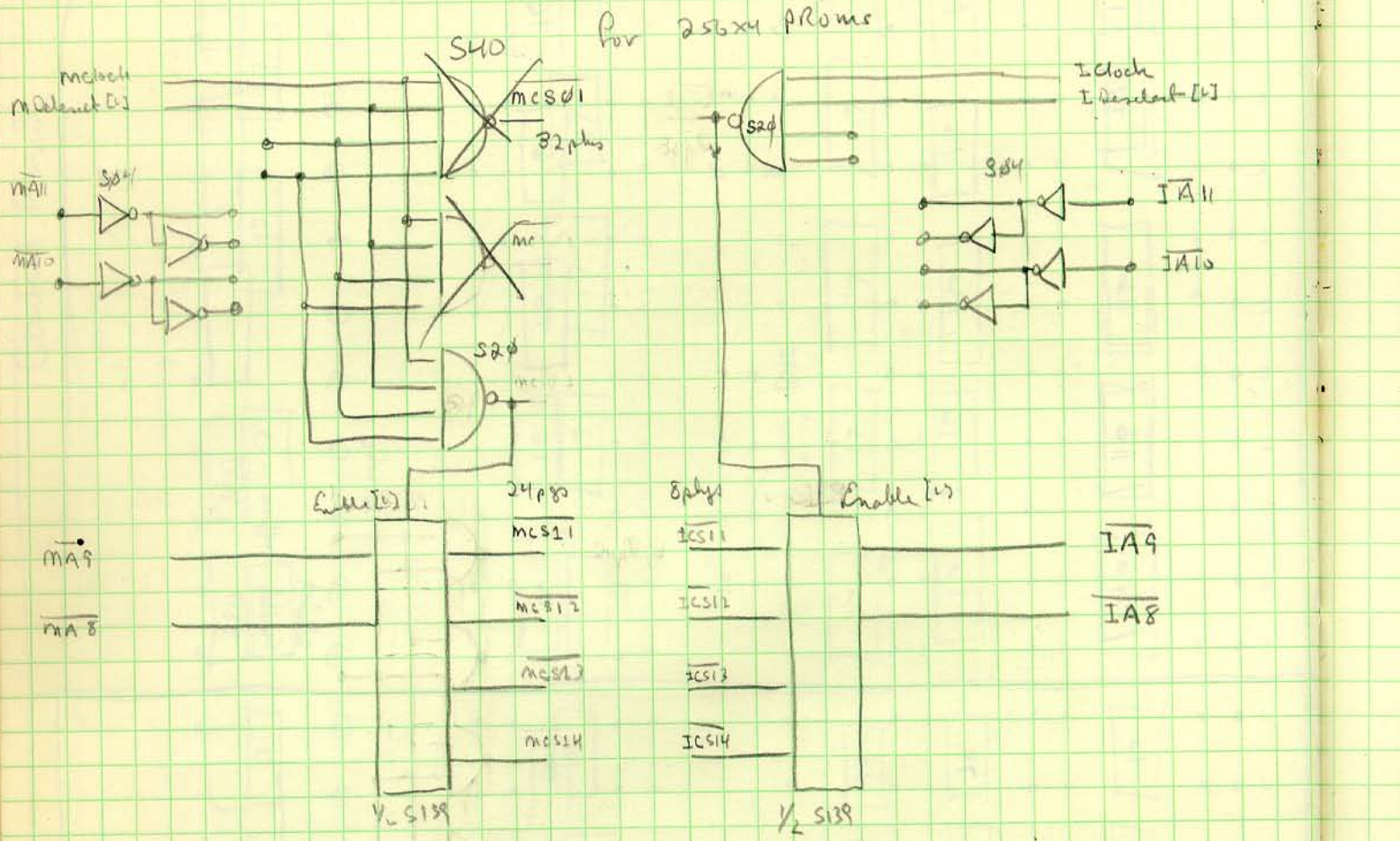
Parts utilized

Control Panel

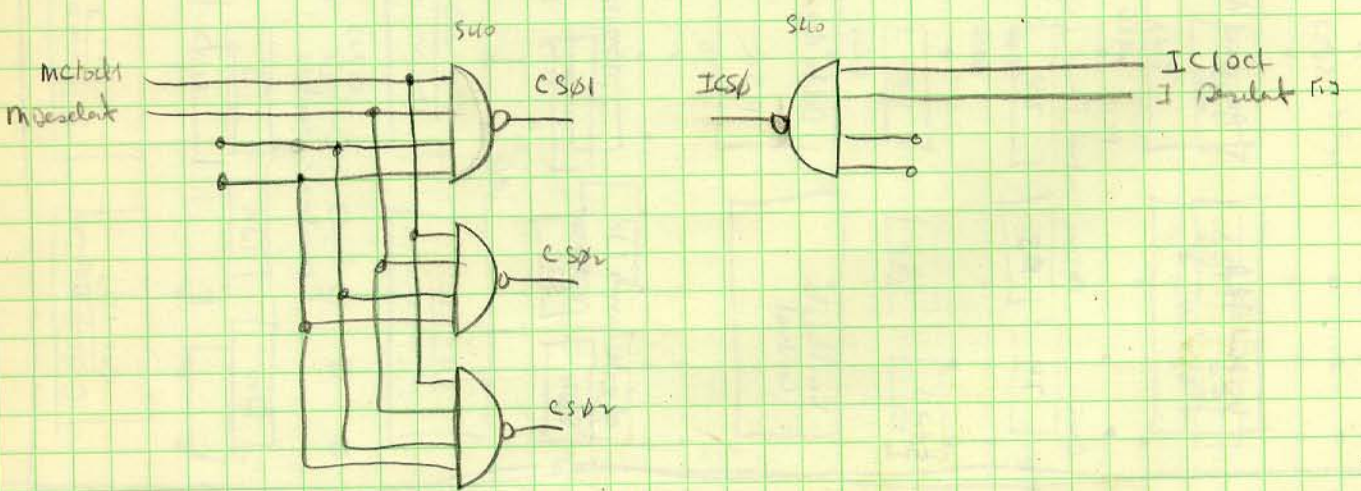



Vector & PCR
Virtual Add + c', v', n', z'
Physical Add
PCR
RES
PROGRAMMED
PRIORITY
EXEC
Micro control Panel Logic
74
08
74
74
DST
SRC
Switch Data Control + Panel Control
Switch Data Control
Data Register
PSR
clock Drive
AD/DATA
S64
Hex Driver S37
16
Switch lines from Panel
resistors / capacitors
Schmitt Switch Buffers
8837
8837
Sw. Locks
Bus
17
16

Board Decoding / PROM & 1M×128



For 1M×1 RAMs



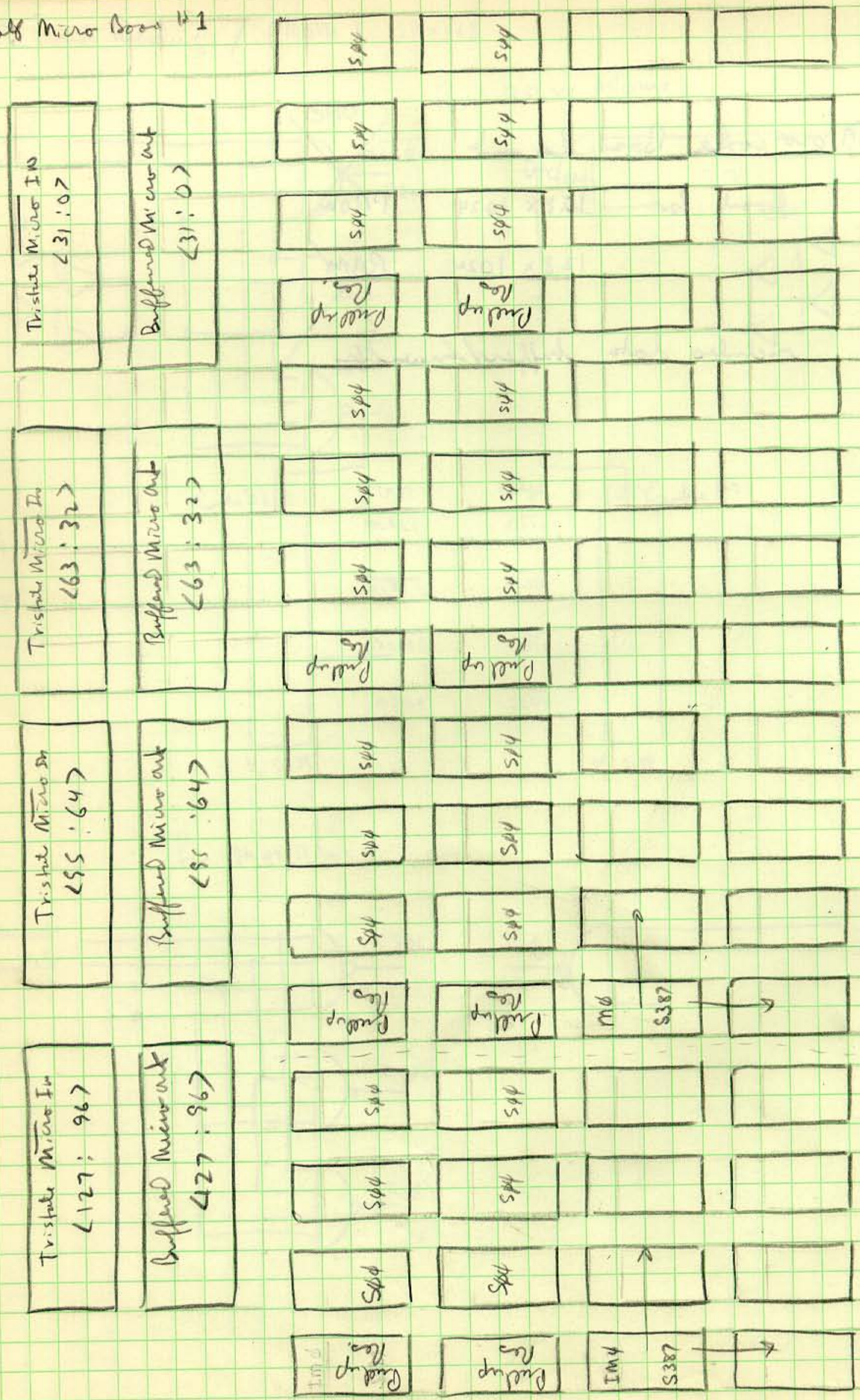
Micro-code Board layout

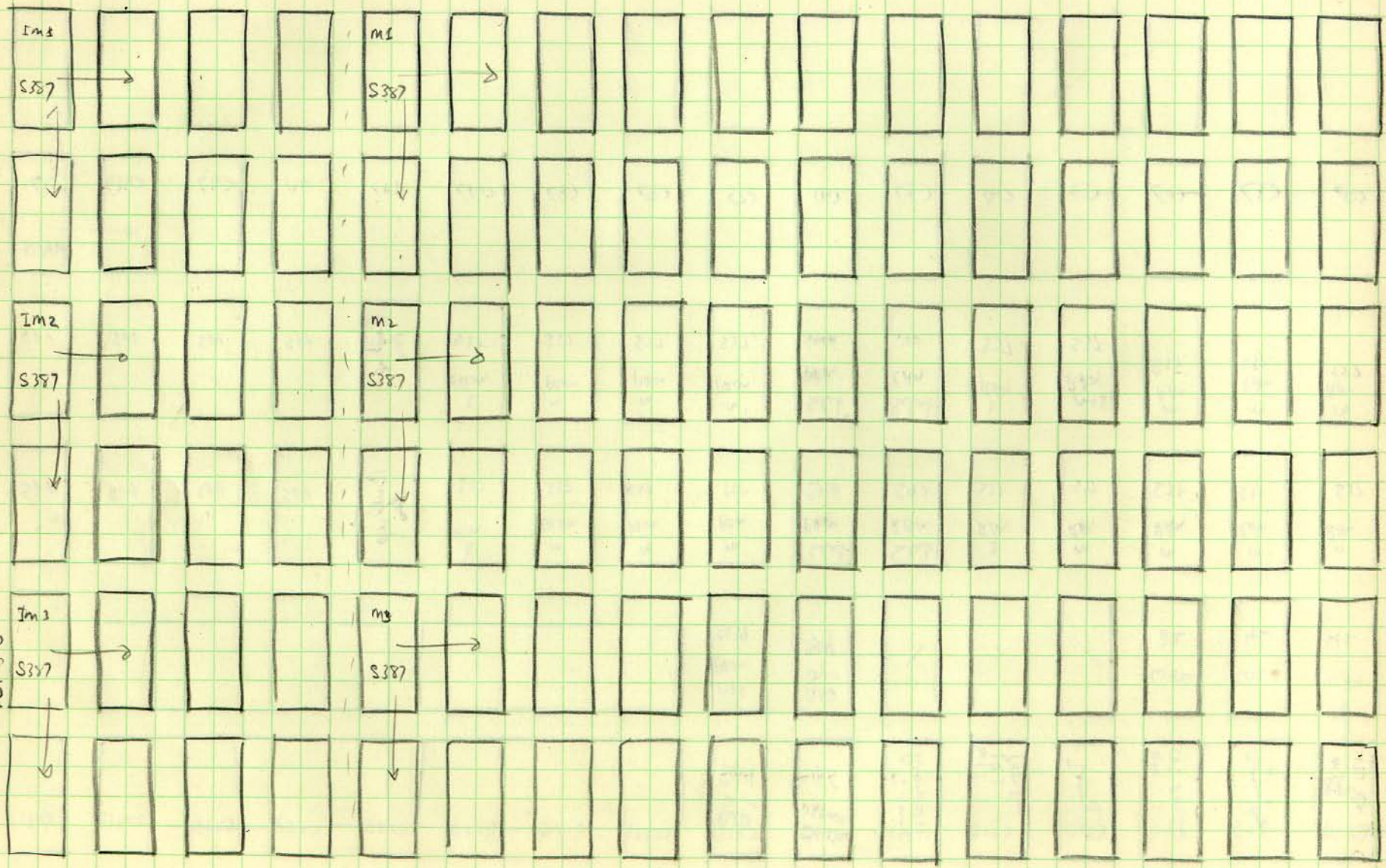
Board for 128 x 1024 PROM

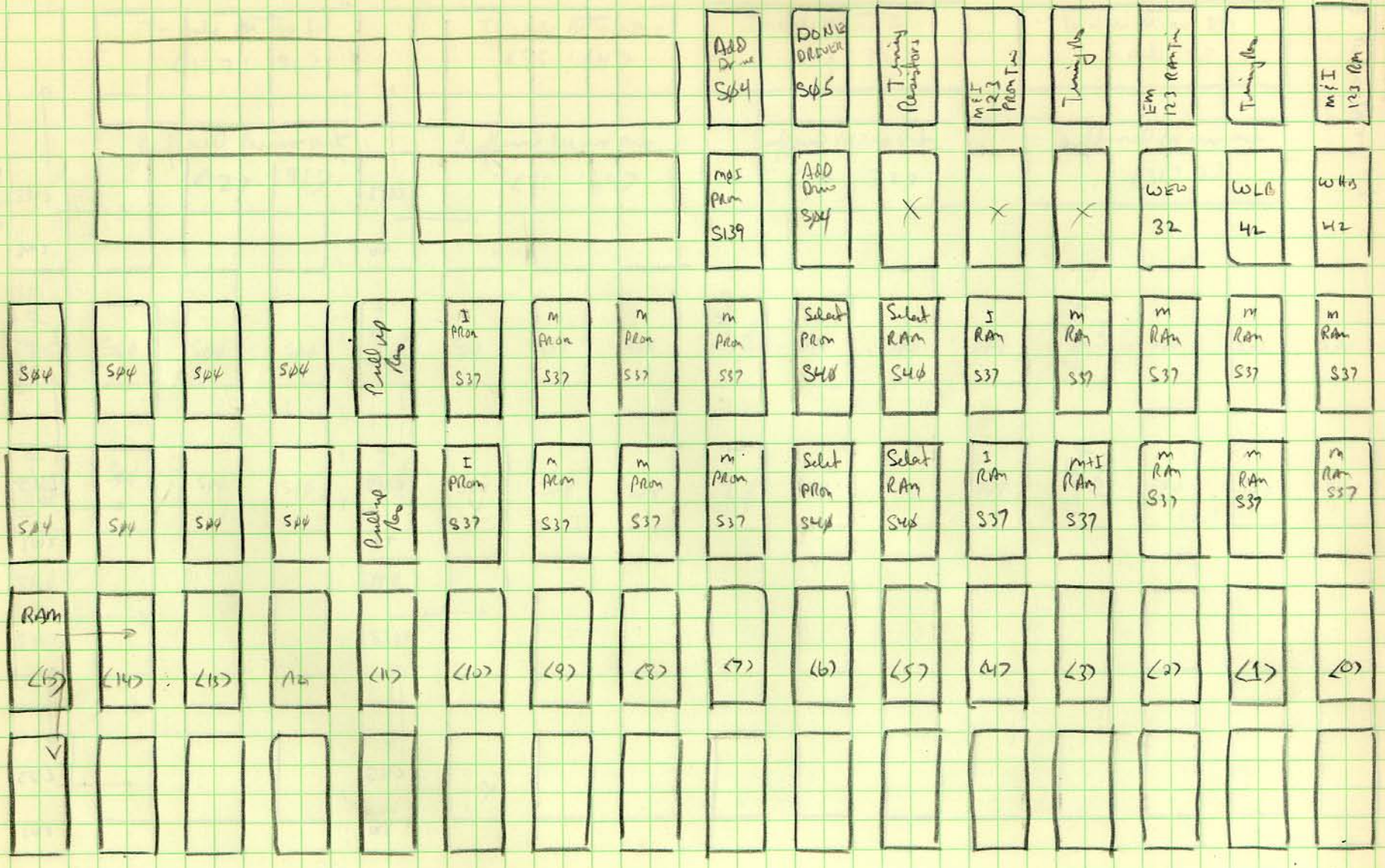
128 x 1024 RAM

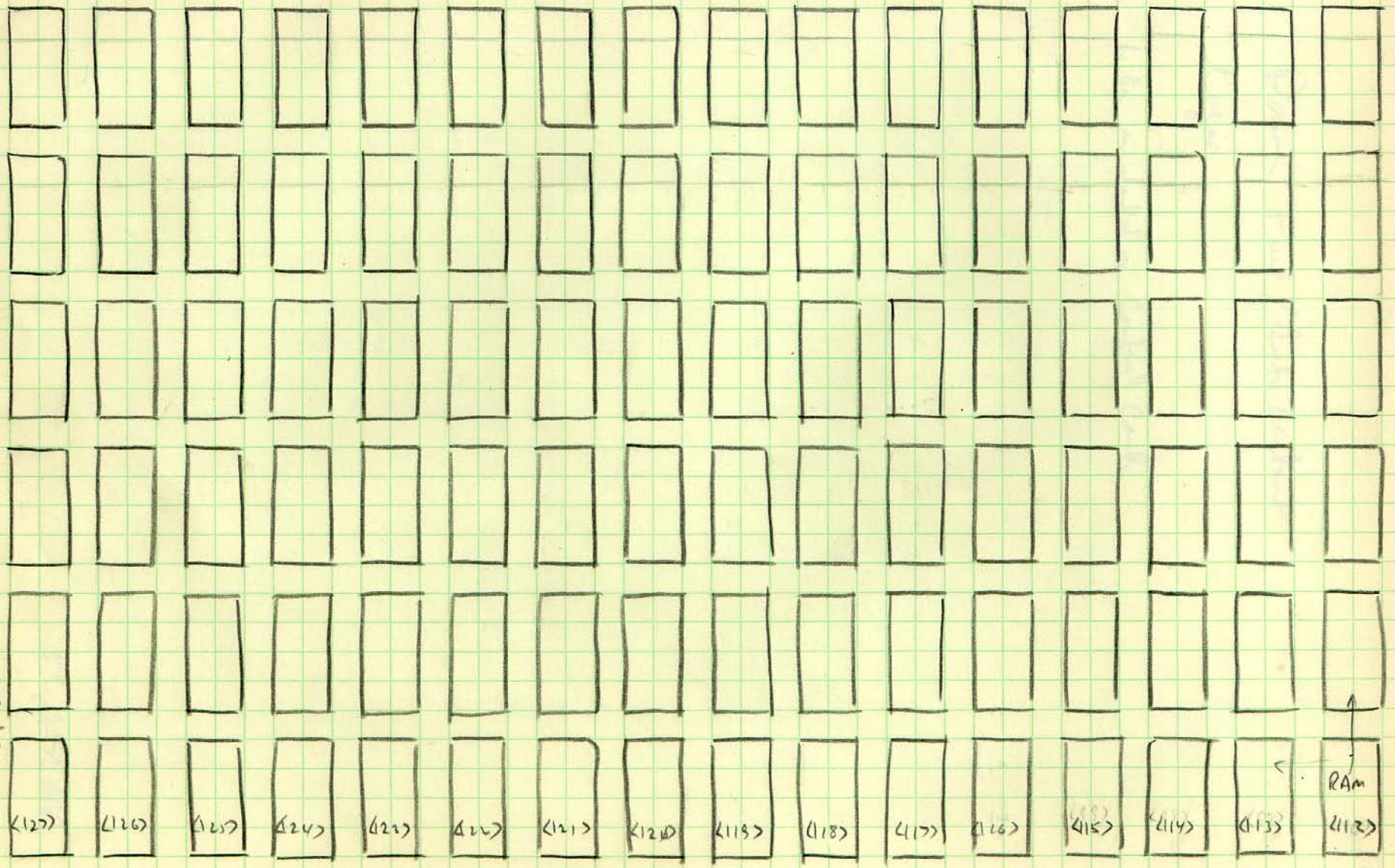
includes data buffer/inverters

Left Half Micro Board #1




Im1
S387
m1
S387
Im2
S387
m2
S387
Im3
S387
m3
S387
3 sets of ABD


Add Drive
S64
DONE DRIVER
S65
Trimming Resistors
M&I 123 PROM Trim
Trimming Logic
EM 123 RAM Trim
Trimming Logic
M&I 123 RAM
MSI PROM
S139
Add Drive
S64
WEN
32
WLB
42
WHB
42
S64
Pull up Logic
I PROM
S37
M PROM
S37
Select PROM
S48
Select RAM
S48
I RAM
S37
M RAM
S37
M+I RAM
S37
RAM
<15>
<14>
<13>
A6
<11>
<10>
<9>
<8>
<7>
<6>
<5>
<4>
<3>
<2>
<1>
<0>


ARG
<127>
<126>
<125>
<124>
<123>
<122>
<121>
<120>
<119>
<118>
<117>
<116>
<115>
<114>
<113>
<112>
RAm

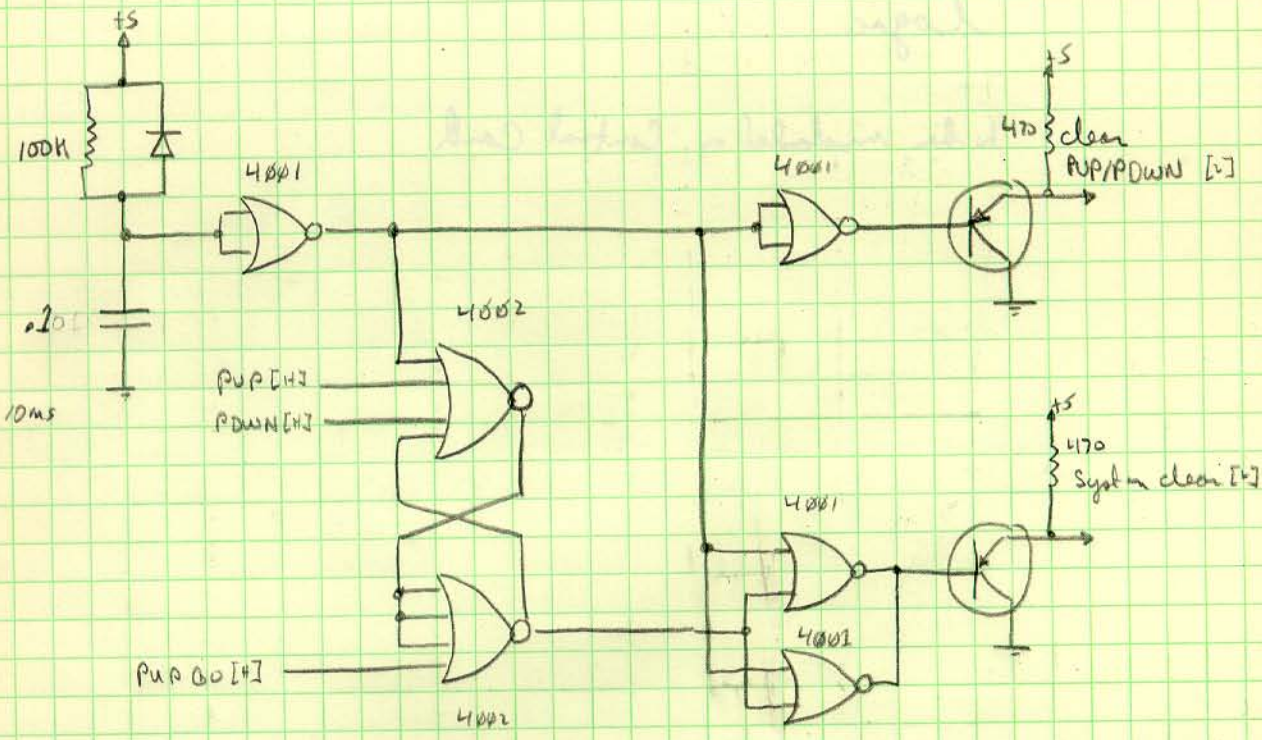
Power Fail / Auto Restart

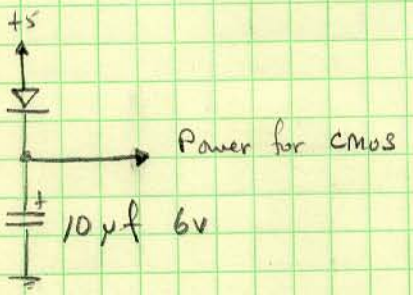
logic

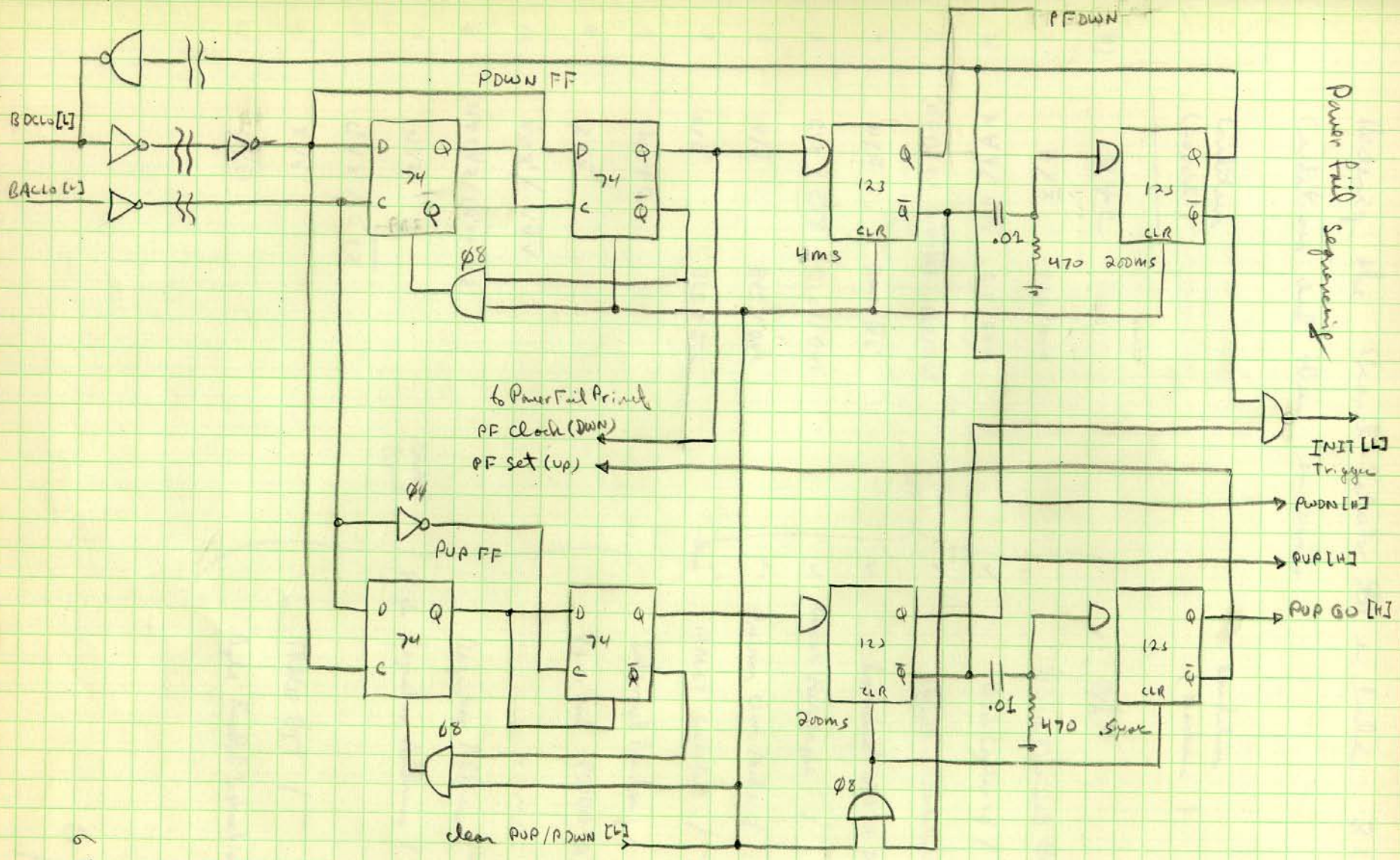
to be included in Control Card

5 Sept 76 AAA

CPU Power Monitor






PFDWN
PDWN FF
BDCLO [L]
BACLO [L]
74
123
CLR
4ms
.02
470
200ms
Power Fail Sequencing
to Power Fail Print
PF clock (DWN)
PF set (UP)
INIT [L]
Trigger
PWDN [H]
PUP [H]
PUP GO [H]
PUP FF
.01
clear PUP/PDWN [L]
6 sept 76
57

Redesign the Branch Selector to include 32 branch Conditions and their inverses

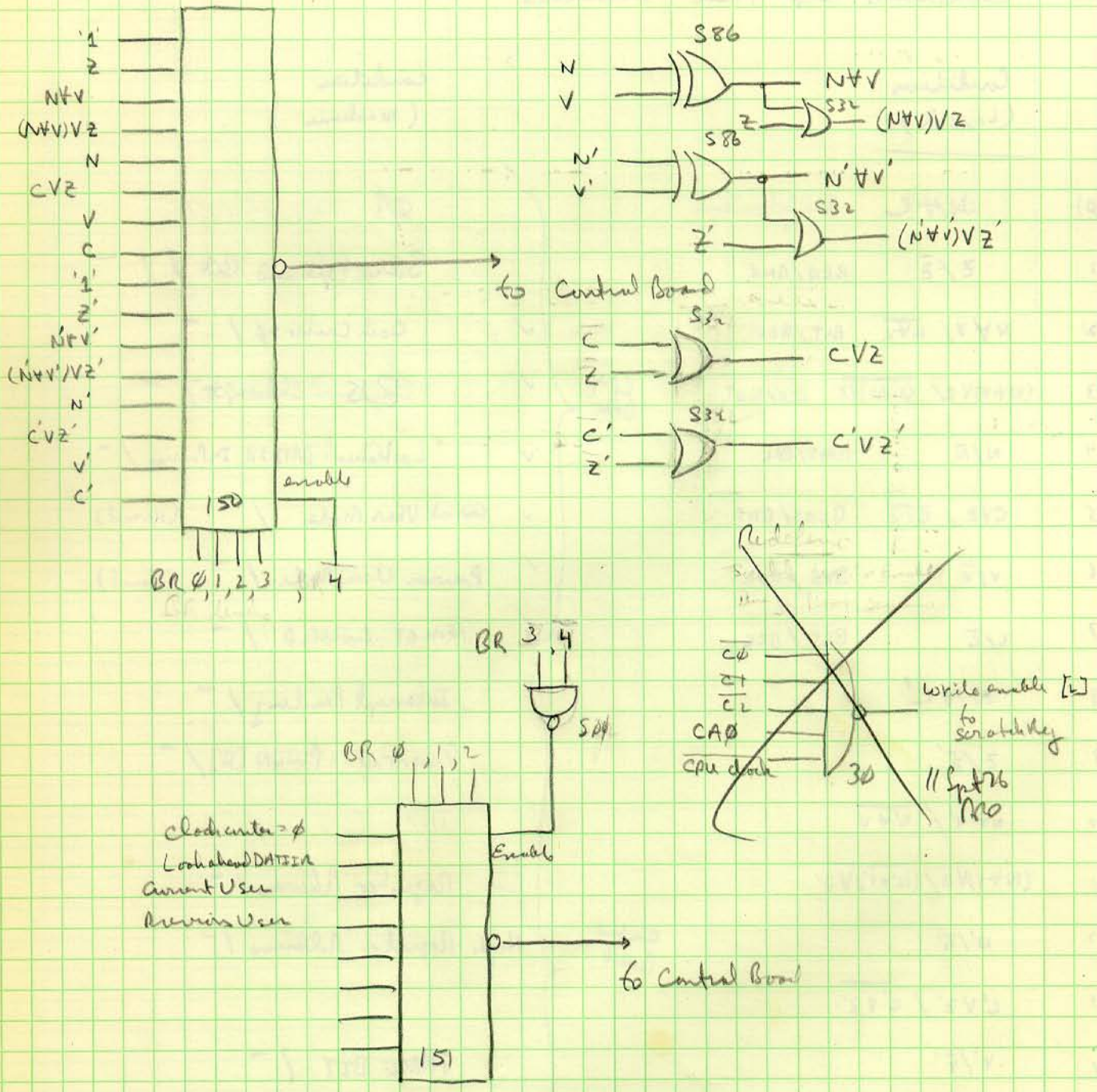
	Conditions (Logical)		Conditions (machine)	
0	$N \veebar C$			$\emptyset / \bar{1}$
1	$Z / \bar{Z}$	BEQ / BNE		Source Operand Bit $\emptyset$ / —
2	$N \veebar V / \overline{N \veebar V}$	BLT / BGE	✓	Clock Counter $\neq \emptyset$ / —
3	$(N \veebar V) \vee Z / \overline{(N \veebar V) \vee Z}$	BLE / BGT	✓	BUS Interrupt / —
4	$N / \bar{N}$	BMI / BPL	✓	Lookahead DATI IR In Progress / —
5	$CVZ / \overline{CVZ}$	BLOS / BHI	✓	Current User Mode / — (Kernel)
6	$V / \bar{V}$	BVS / BVC	✓	Previous User Mode / — (Kernel)
7	$C / \bar{C}$	BCS / BCC	✓	MMGT Enabled / —
8	$N' \veebar C'$			Interrupt Pending / —
9	$Z' / \bar{Z}'$			Power Fail PWDN [H] / —
10	$N' \veebar V' / \overline{N' \veebar V'}$			IRA (Ctl. Reg) / —
11	$(N' \veebar V') \vee Z' / \overline{(N' \veebar V') \vee Z'}$			Register Address / —
12	$N' / \bar{N}'$			High Register Address / —
13	$C' V Z' / \overline{C' V Z'}$			
14	$V' / \bar{V}'$			TRACE BIT / —
15	$C' / \bar{C}'$			Byte Enabled Instruction / —

CPU Board

Control Board

6 Sept 76
AFA

Coding Logic



Moved IR/SW Data Read Select ⊗ Control Board 6 Sept 76 ARO

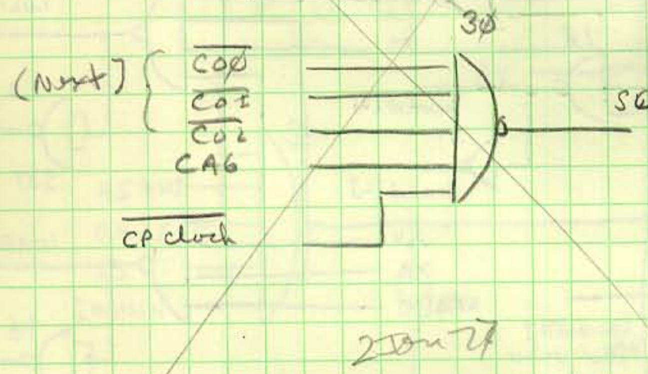
Moved Write Read Register ⊗ Control Board

Modify the Scratch Register Read/Write to be enabled only during a 'next instruction' code

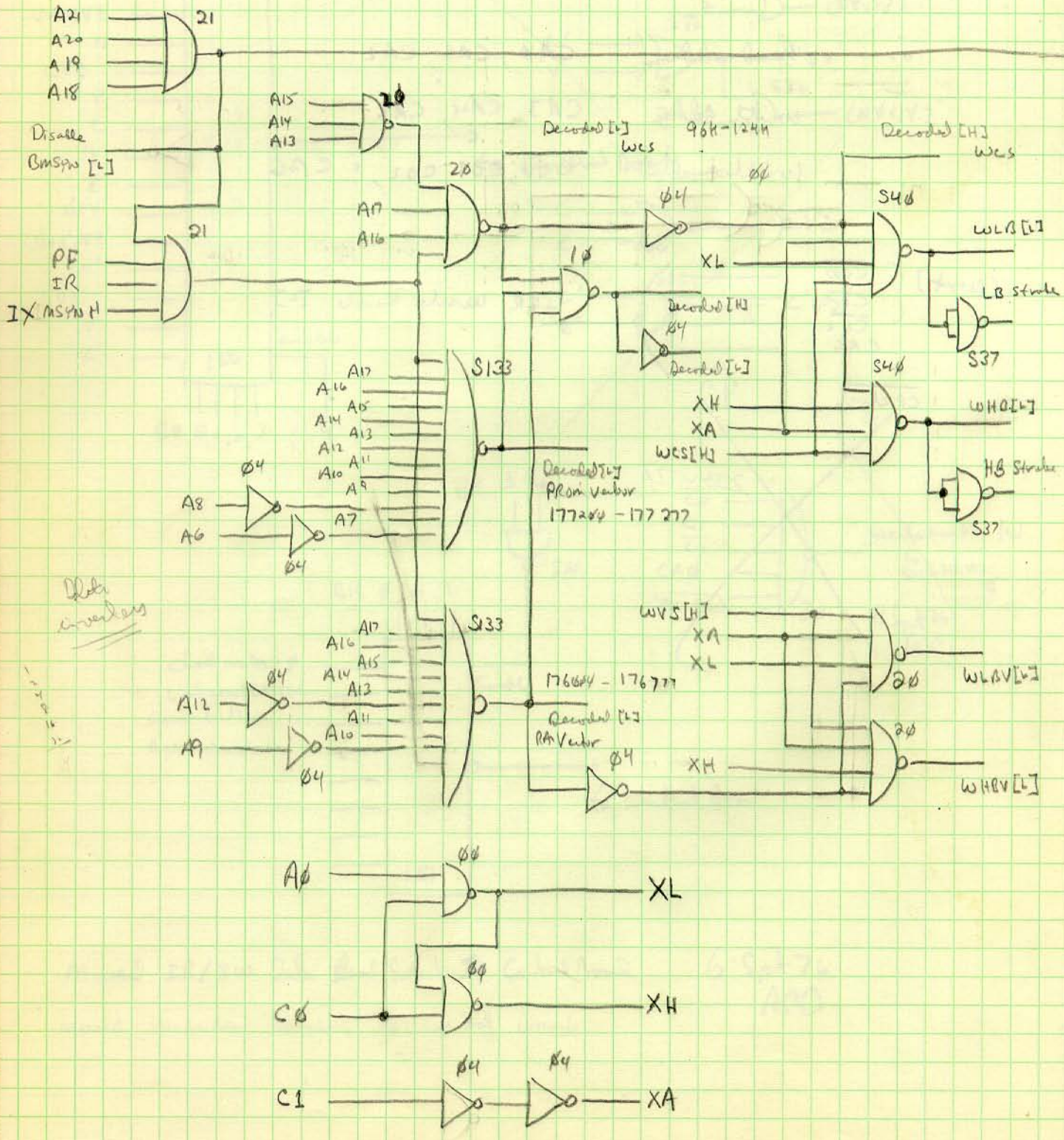
∴ Read address CA∅, CA1, CA2

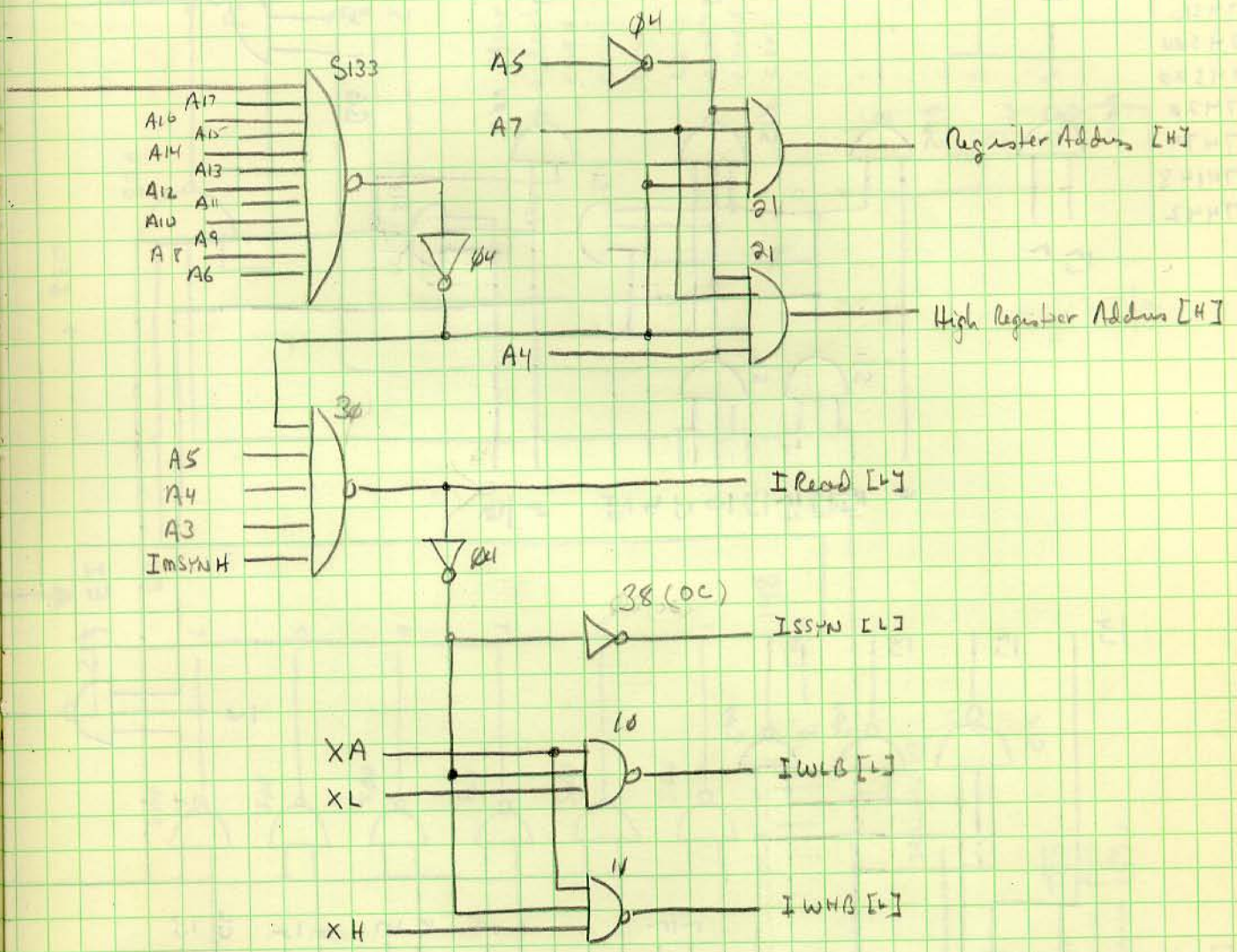
Write Address CA3, CA4, CA5

Write enabled CO∅, CO1, CO2, & CA6



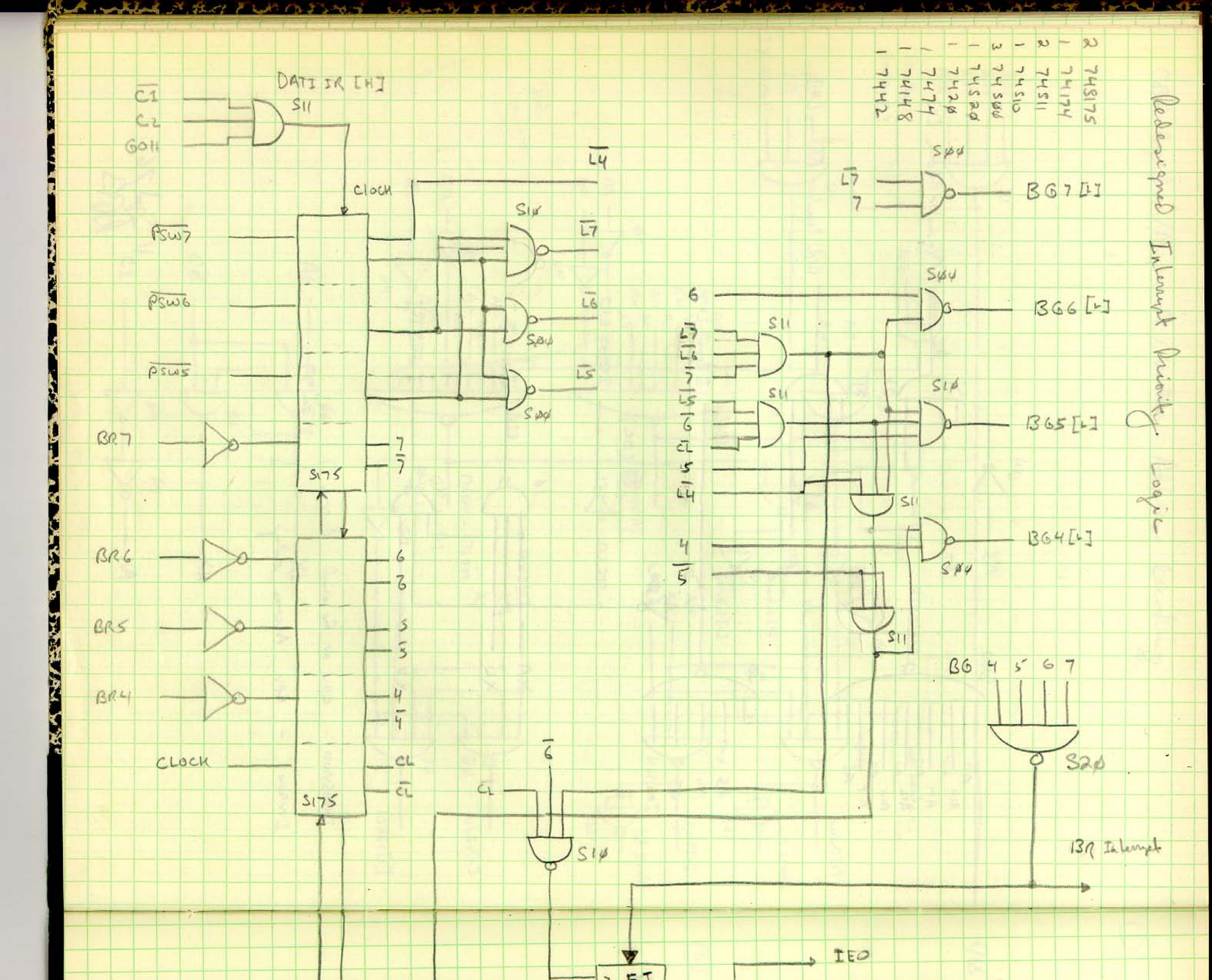
CPU Register / Microcode / Vector Address decoding

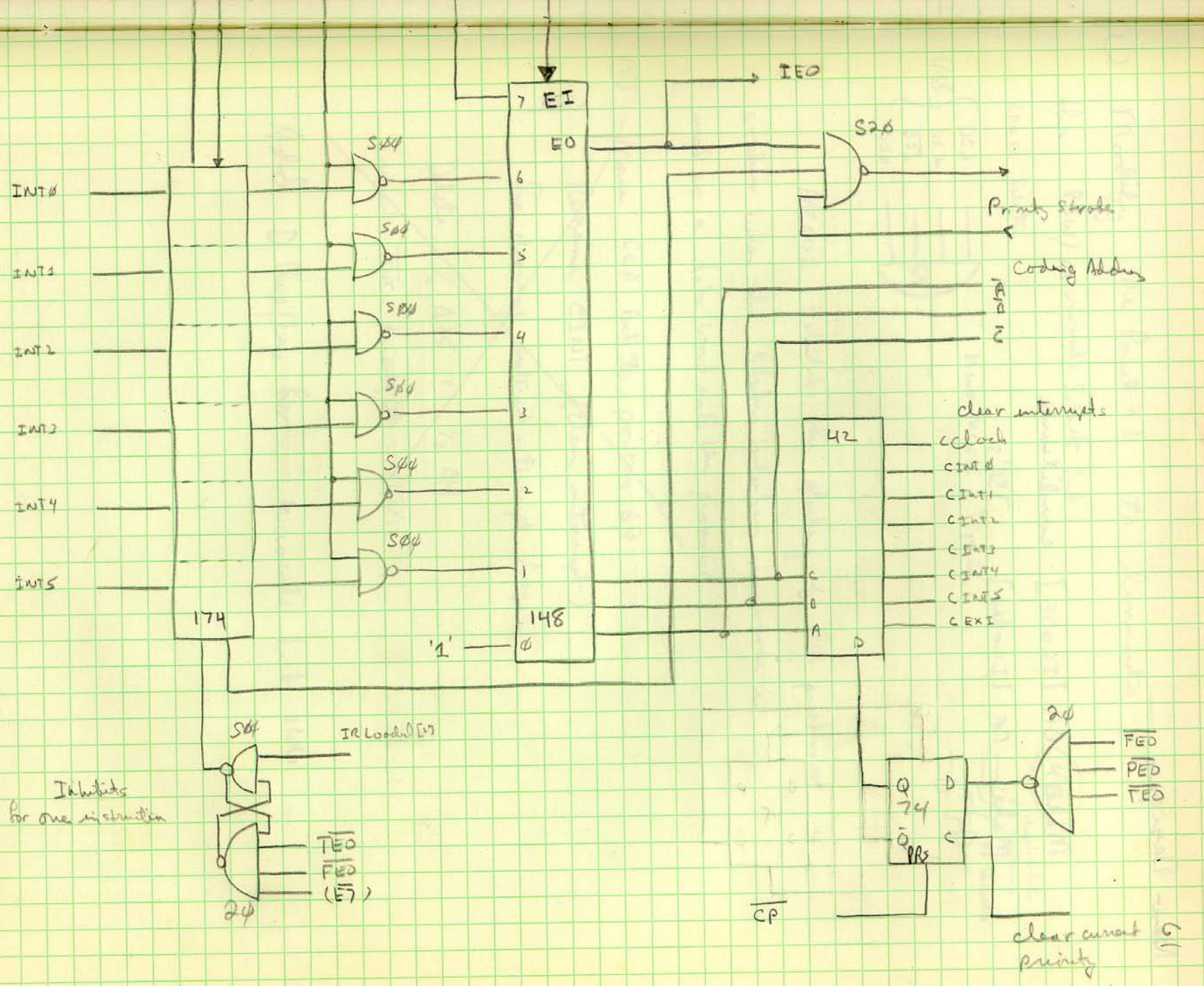




IXMSYNH - CPU or Extend Access
IMSYN - CPU Access only
} 8 Jan 77

11 Sept 76


Redesigned Interrupt Priority Logic
DATI IR [H]
C1
C2
GOH
S11
CLOCK
L4
PSW7
PSW6
PSW5
S10
L7
L6
L5
S00
BR7
BR6
BR5
BR4
CLOCK
S175
7
6
5
4
CL
BG7 [L]
BG6 [L]
BG5 [L]
BG4 [L]
BG 4 5 6 7
S20
IEO
IEI
IAK
IAK Interrupt
BR Interrupt
2 74S175
1 74174
2 74S11
1 74S10
3 74S00
1 74S20
1 74174
1 74148
1 7442


INT0
INT1
INT2
INT3
INT4
INT5
174
148
EI
EO
7
6
5
4
3
2
1
0
'1'
S0
IEO
S20
Priority Strobe
Coding Address
A
B
C
clear interrupts
42
clock
CINT0
CINT1
CINT2
CINT3
CINT4
CINT5
CEXI
IR Loaded [7]
Inhibits for one instruction
TEO
FED
(E7)
2φ
Q
D
74
PRS
CP
PED
clear current priority

New Designs —

Make BR [ICODE] conditional

Make BR [Icodes]]SR's

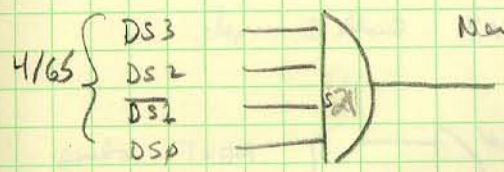
4/65

①

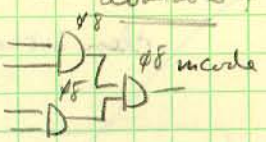
②

① Modify CPU Panel # 1 to eliminate the PSW/Microcode Select bit

CNTES Selection



4F1 ? available ?



MCODE Inhibits the clocking of the processor states when the States selection microcode is used as a data word into the processor

② Move CCP Bit to position 63

Rename CINT (clear interrupt)

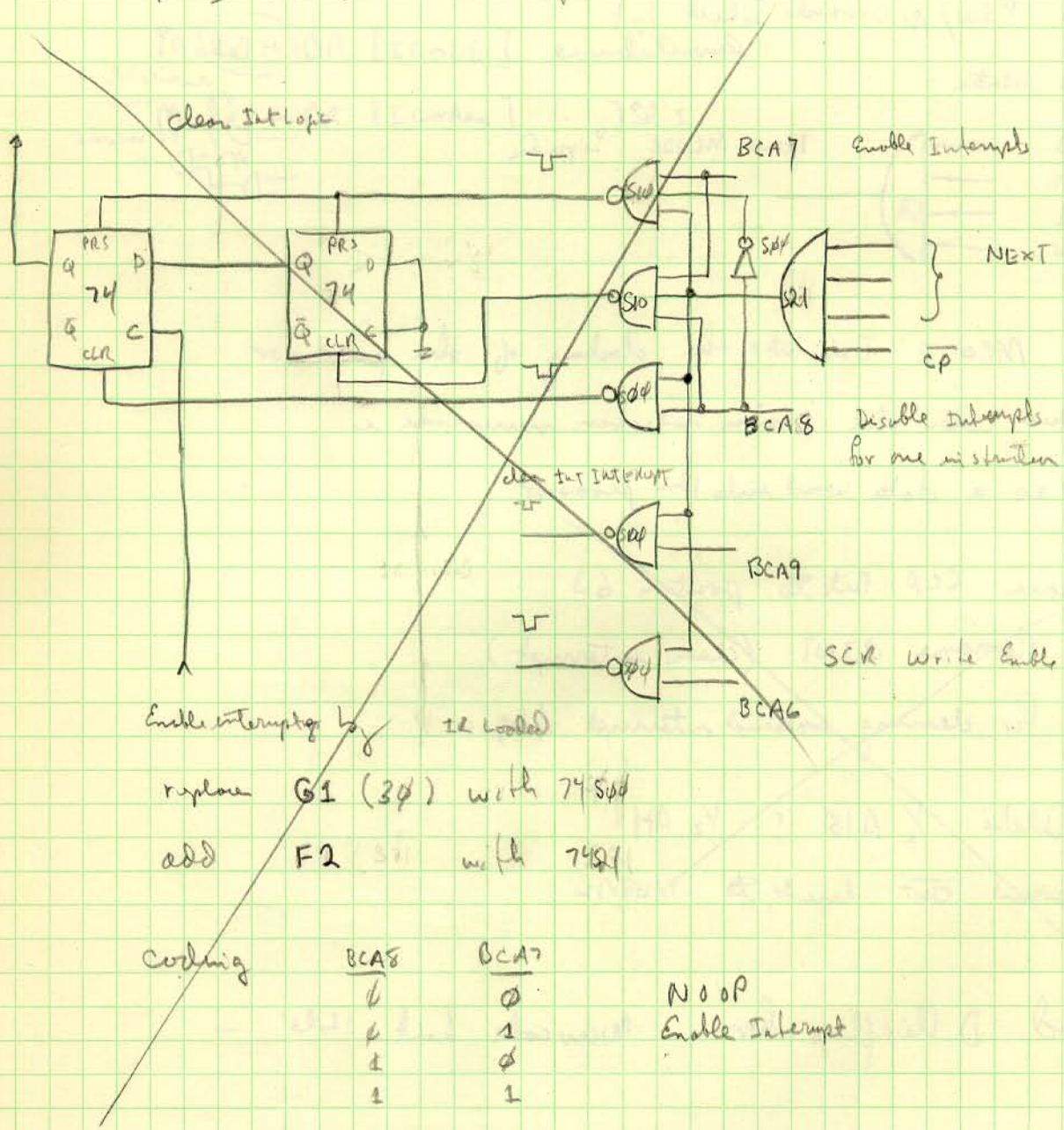
for clearing external interrupt logic

Delete ½ A15 ; ½ AH

signal $\overline{CINT}$ directly to XE8/12

Add D flipflop for Microcode halt state —

Interrupt Inhibit / Enable Logic



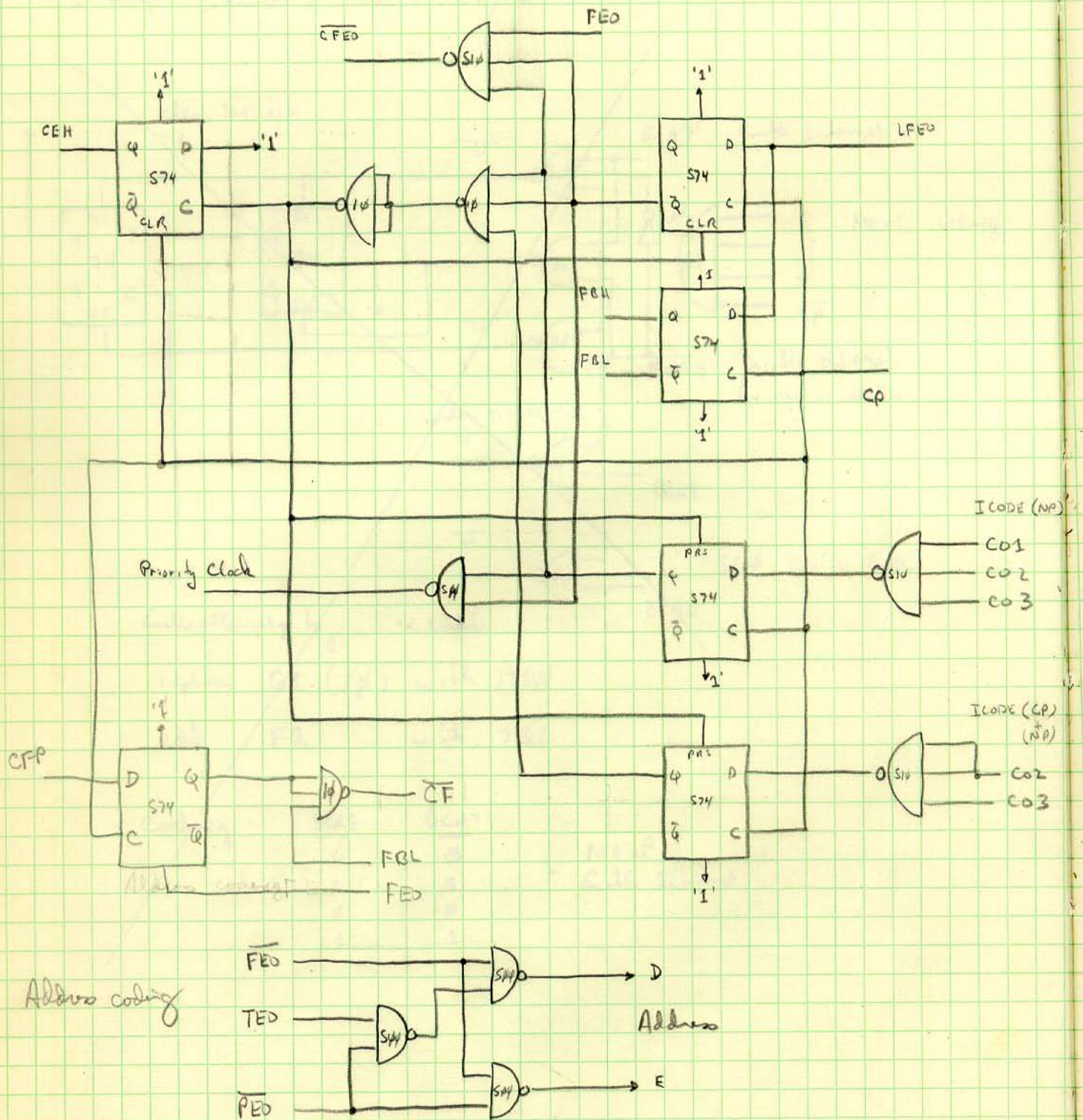
replace G1 (3ϕ) with 74S00

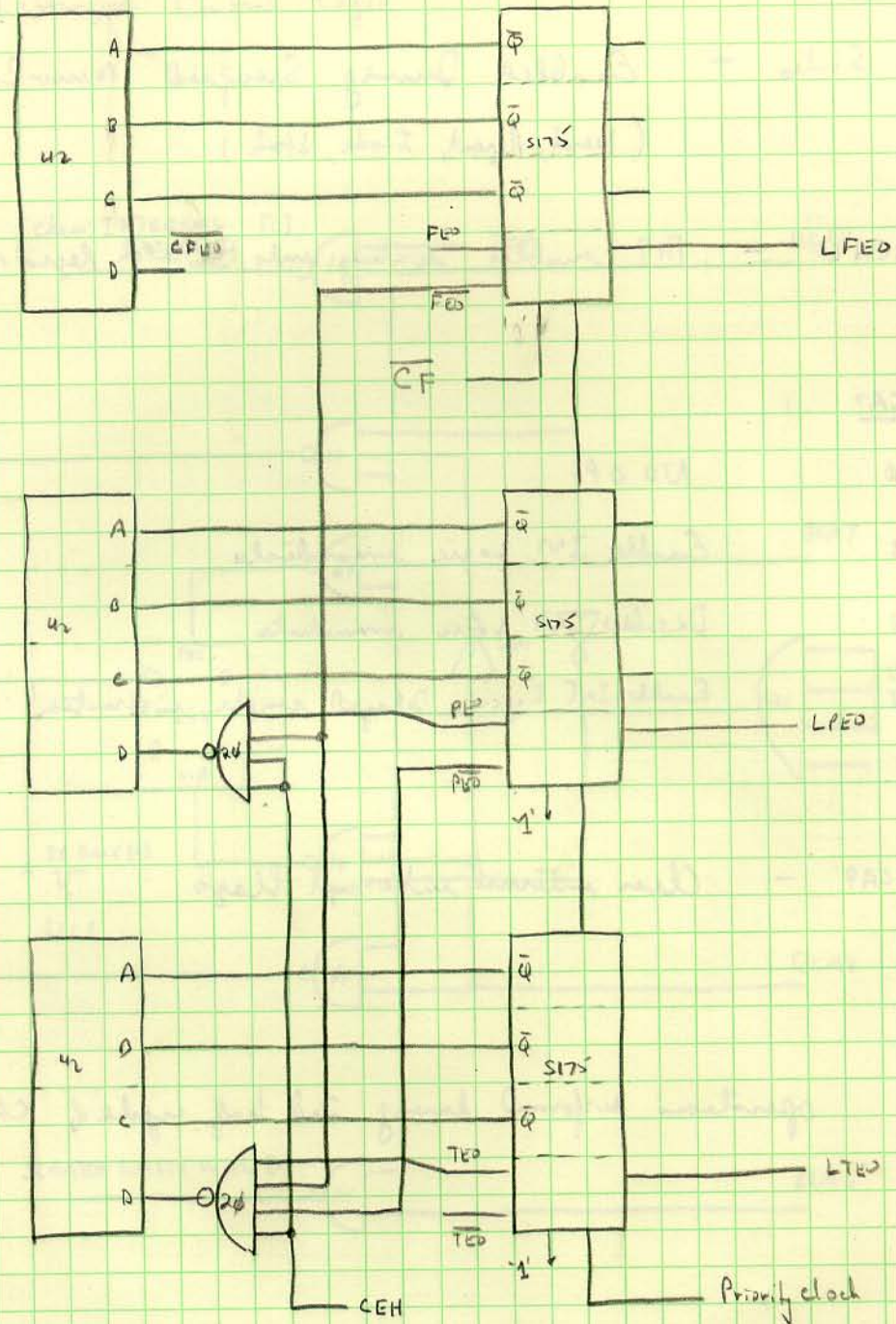
add F2 with 74S1

Coding

BCA8	BCA7	
0	0	NOOP
0	1	Enable Interrupt
1	0	
1	1	

CPU Priority Clocking Logic





29 Dec 1976

ARD

Control States – Enabled During Specified Micro Processor Cycles
(Next, Repeat, Icode, Stack)

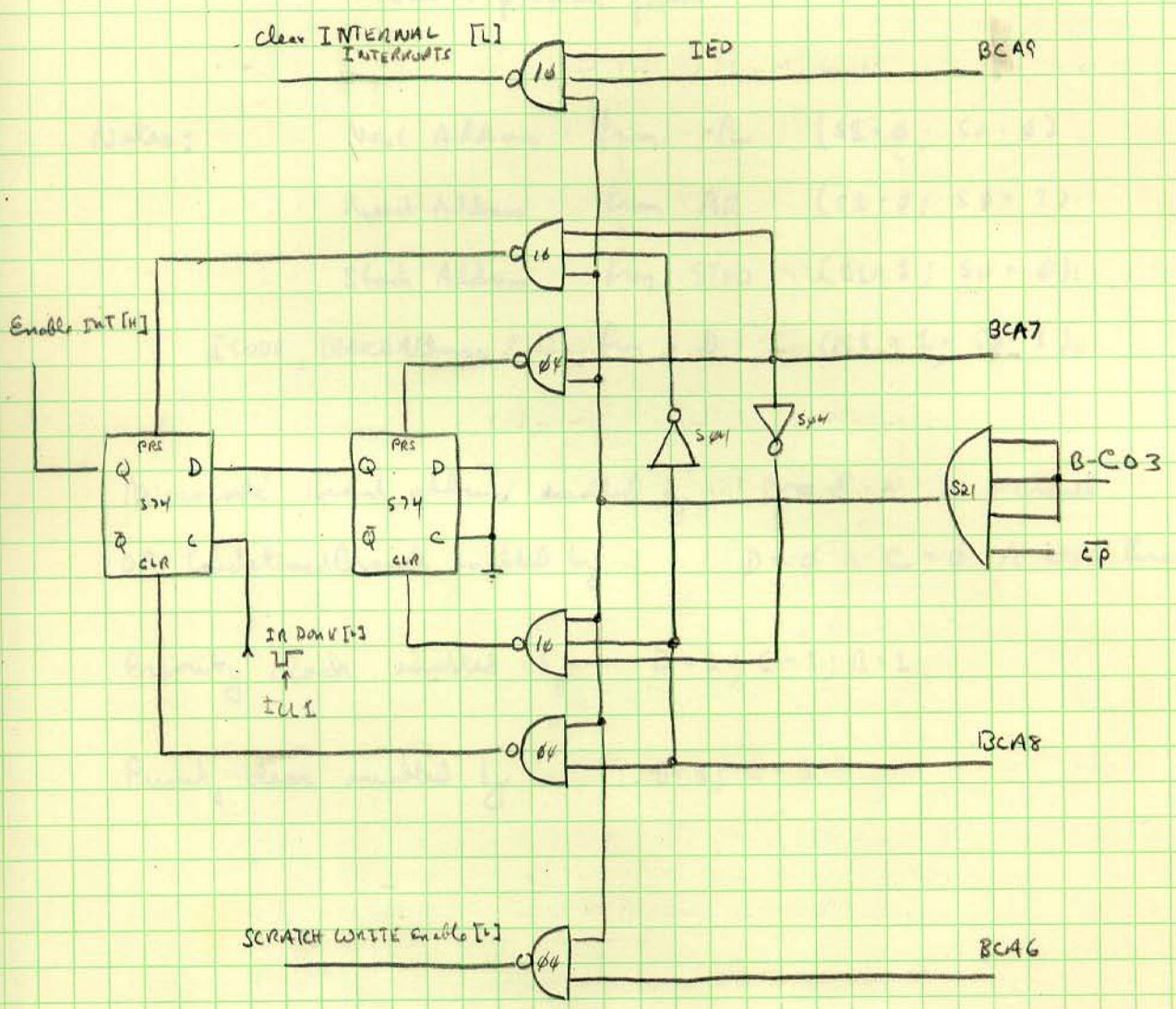
BCA6 – [H] enables writing into Scratch Registers

BCA8	BCA7	
0	0	NO OP
0	1	Enable INT Logic immediate
1	0	Disable INT Logic immediate
1	1	Enable INT Logic Delayed single instruction

BCA9 – Clear internal interrupt flags

operations performed during 2nd half cycle of CPU clock

Internal Interrupt Control Logic



29 Dec 1976

ARD

Microcontroller Branching Logic

a) 16 Conditional Branching operations to control program flow

Notes:

Next Address	from µPC	(S1 = Ø ; SØ = Ø)
Repeat Address	from AR	(S1 = Ø ; SØ = 1)
Stack Address	from STKD	(S1 = 1 ; SØ = Ø)
ICODE ; BRANCH Address	from D	(S1 = 1 ; SØ = 1)

Microcode Brand address enabled by $D = Ø \wedge$ No F Branch

OR Conditional Branch enabled by $D = Ø \wedge C = Ø \wedge$ No F Branch $\wedge$ [CN]

Priority clock enabled by D = 1 ; C = 1 ; B = 1

Priority clear enabled by D = 1 ; C = 1

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ARM

Current Status

D	C	B	A	Operation	Cond (ϕ, 1)	S1
ϕ	ϕ	ϕ	ϕ	Branch (Micro) V condition	[CN]	1
ϕ	ϕ	ϕ	1	Conditional Branch (Micro) V <C><N> ; Next	[CN]	[CN]
ϕ	ϕ	1	ϕ	Conditional Branch (Micro) V <V><Z> ; Next	[CN]	[CN]
ϕ	ϕ	1	1	Conditional Brand (Micro) V <C><V><Z><N> ; Next	[CN]	[CN]
ϕ	1	ϕ	ϕ	Conditional Branch ; Repeat	[CN]	[CN]
ϕ	1	ϕ	1	Conditional Branch ; Next	[CN]	[CN]
ϕ	1	1	ϕ	Conditional JSR ; Repeat	[CN]	[CN]
ϕ	1	1	1	Conditional JSR ; Next	[CN]	[CN]
1	ϕ	ϕ	ϕ	Conditional Next ; Repeat	[CN]	ϕ
1	ϕ	ϕ	1	Conditional Pop Stack ; Next	[CN]	ϕ
1	ϕ	1	ϕ	Conditional RTS ; Repeat	[CN]	[CN]
1	ϕ	1	1	Conditional RTS ; Next	[CN]	[CN]
1	1	ϕ	ϕ	Conditional Brand Icode (CP) ; Next	[CN]	[CN]
1	1	ϕ	1	Conditional JSR Icode (CP) ; Next	[CN]	[CN]
1	1	1	ϕ	Conditional Brand Icode (NP) ; Next	[CN]	[CN]
1	1	1	1	Conditional JSR Icode (NP) ; Next	[CN]	[CN]

Microcontroller Control Signals

S1	SØ	$\overline{FE}$	PUP	C_N	OR0	OR1	OR2	OR3
1	1	1	X	1	[CN]	Ø	Ø	Ø
[CN]	[CN]	1	X	1	Ø <C>	Ø <N>	Ø	Ø
[CN]	[CN]	1	X	1	Ø <V>	Ø <Z>	Ø	Ø
[CN]	[CN]	1	X	1	<C>	<V>	<Z>	<N>
[CN]	1	1	X	1	Ø	Ø	Ø	Ø
[CN]	[CN]	1	X	1	Ø	Ø	Ø	Ø
[CN]	1	$\overline{[CN]}$	X 1	1	Ø	Ø	Ø	Ø
[CN]	[CN]	$\overline{[CN]}$	X 1	1	Ø	Ø	Ø	Ø
Ø	$\overline{[CN]}$	1	X	1			Ø	
Ø	Ø	$\overline{[CN]}$	X Ø	1			Ø	
[CN]	$\overline{[CN]}$	$\overline{[CN]}$	X Ø	1			Ø	
[CN]	Ø	$\overline{[CN]}$	X Ø	1			Ø	
[CN]	[CN]	1	X	1			Ø	
[CN]	[CN]	$\overline{[CN]}$	X 1	1			Ø	
[CN]	[CN]	1	X	1			Ø	
[CN]	[CN]	$\overline{[CN]}$	X 1	1			Ø	

PUP is generated by SØ

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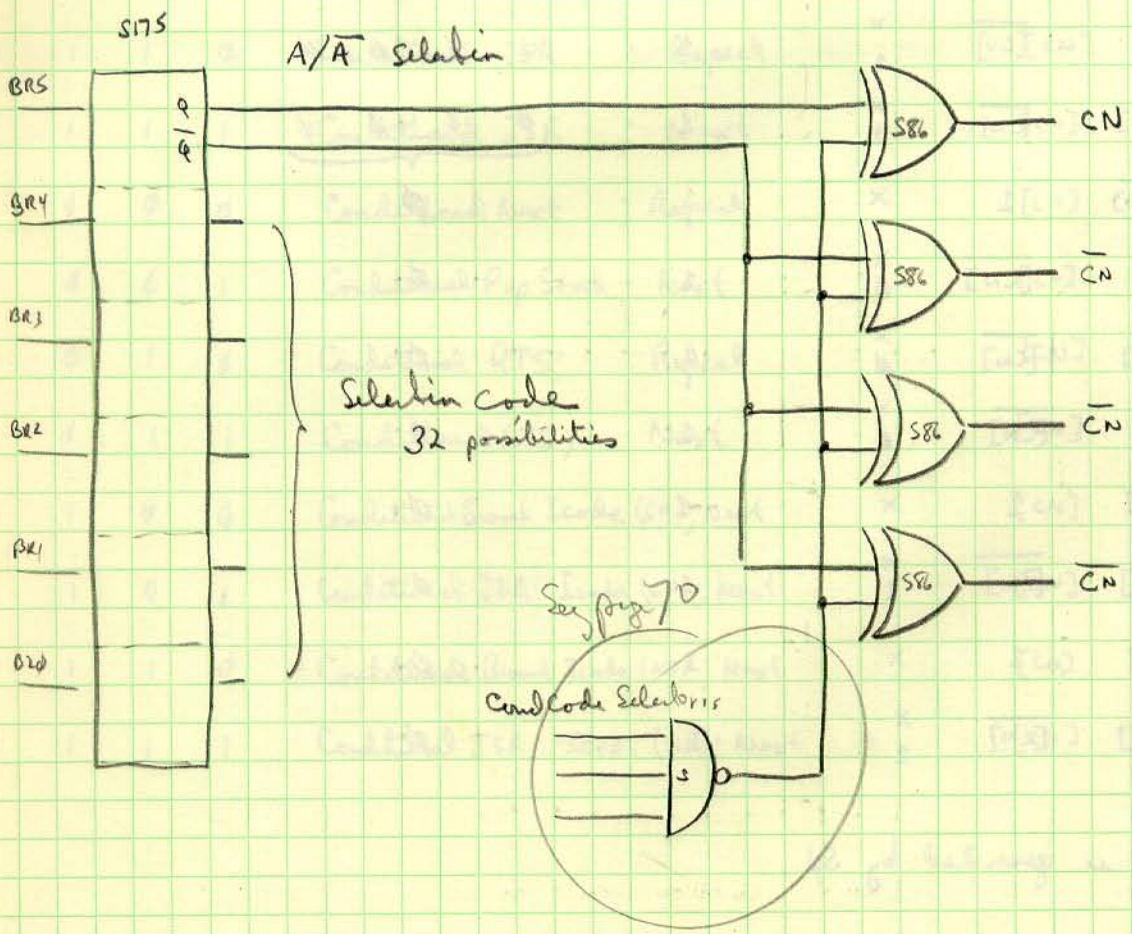
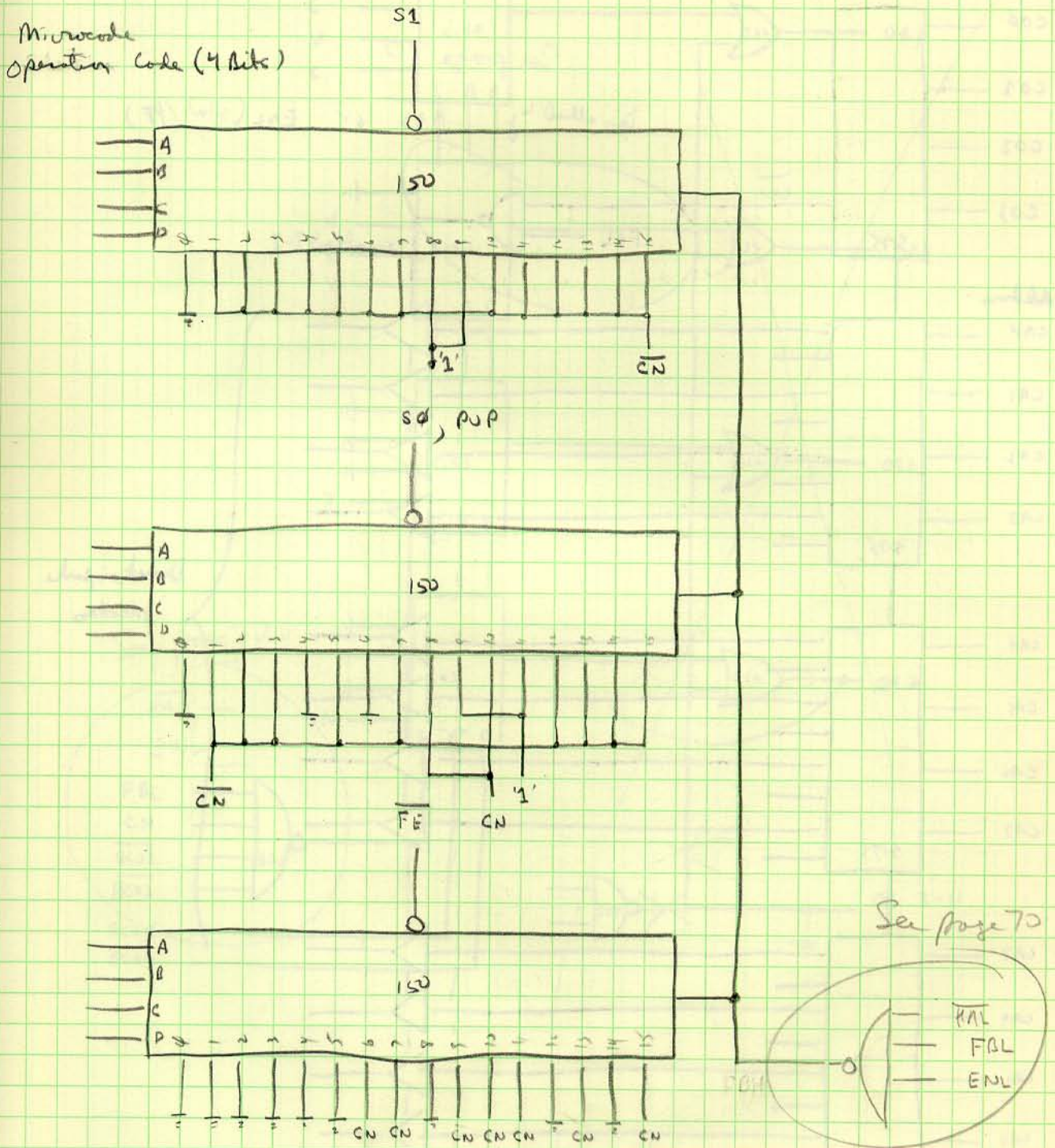
Special Conditions

a) Force Branch

1. Must Select the D input — S1 = 1, S4 = I
2. Must deselect any OR logic
3. must disable any push/pop stack — FE = 1





See page 70

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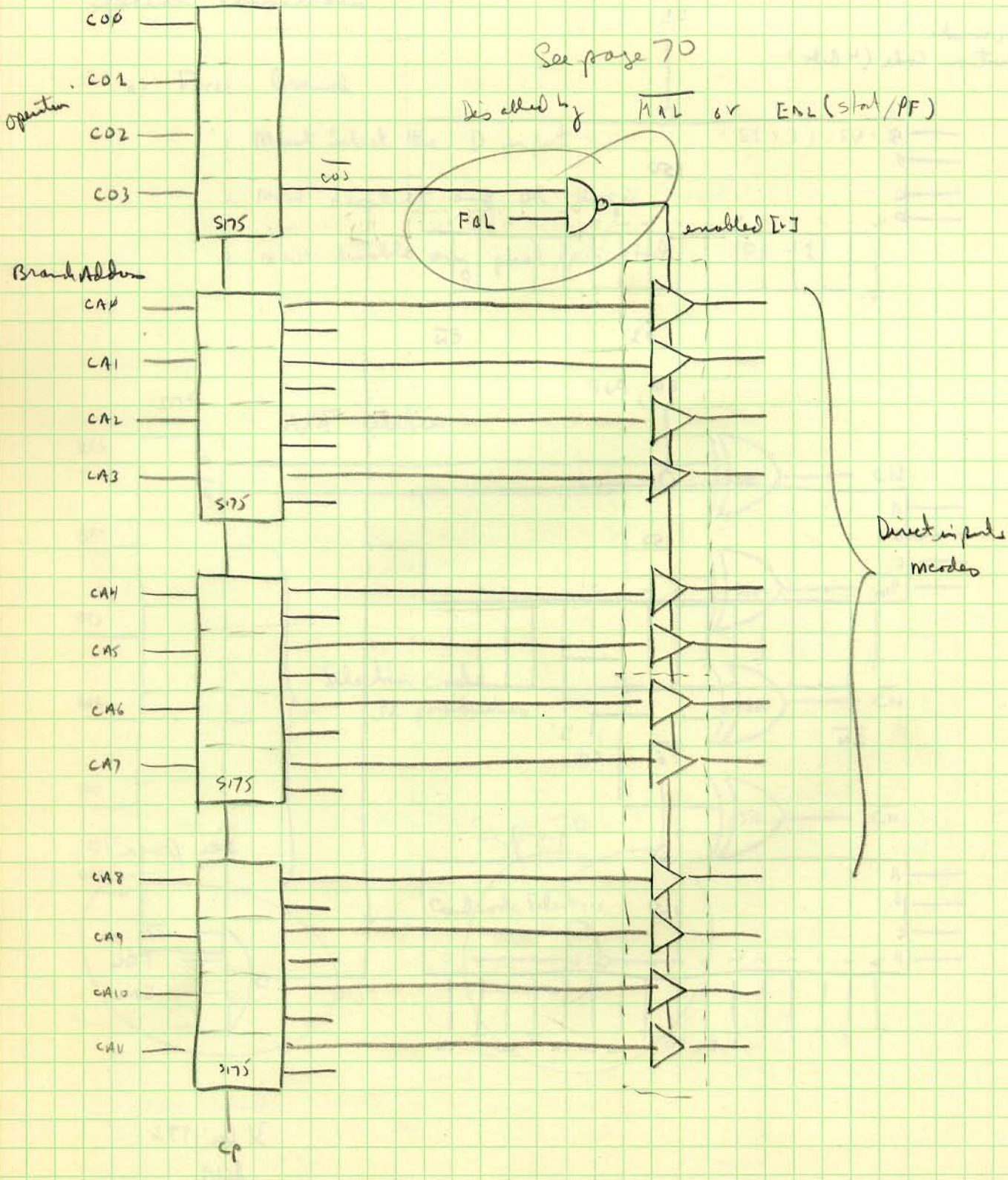
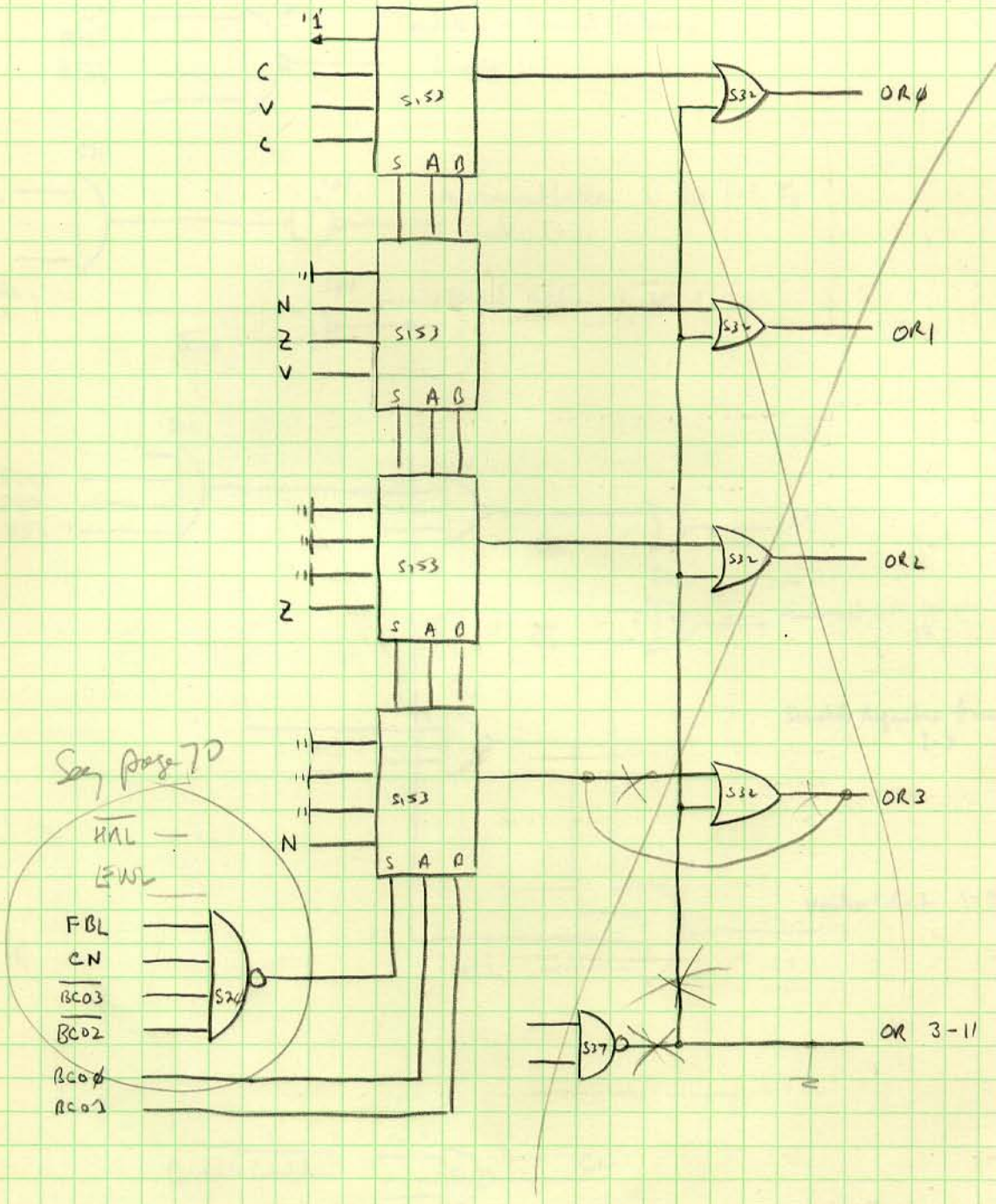
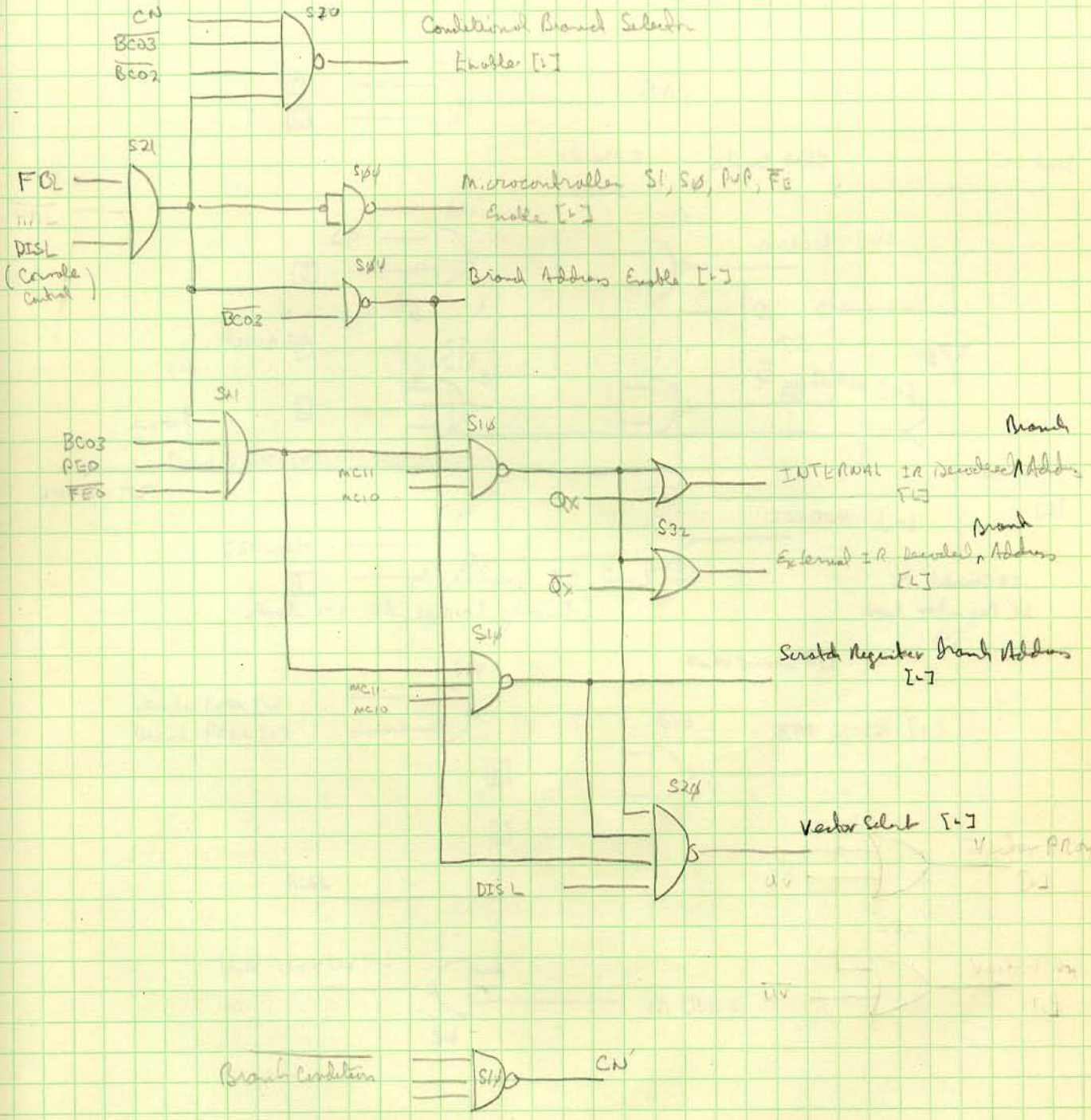
ARO


See page 70
Disabled by MAL or EAL (stat/PF)
Operation
CO0
CO1
CO2
CO3
S175
CO3
FAL
enabled [1]
Branch Address
CA0
CA1
CA2
CA3
S175
CA4
CA5
CA6
CA7
S175
CA8
CA9
CA10
CA11
S175
Cp
Direct inputs
microcode


'1'
C
V
C
S153
S A B
S32
OR0
N
Z
V
OR1
Z
OR2
N
OR3
See page 70
HAL
EWL
FBL
CN
BCO3
BCO2
S20
BCO0
BCO1
S37
OR 3-11

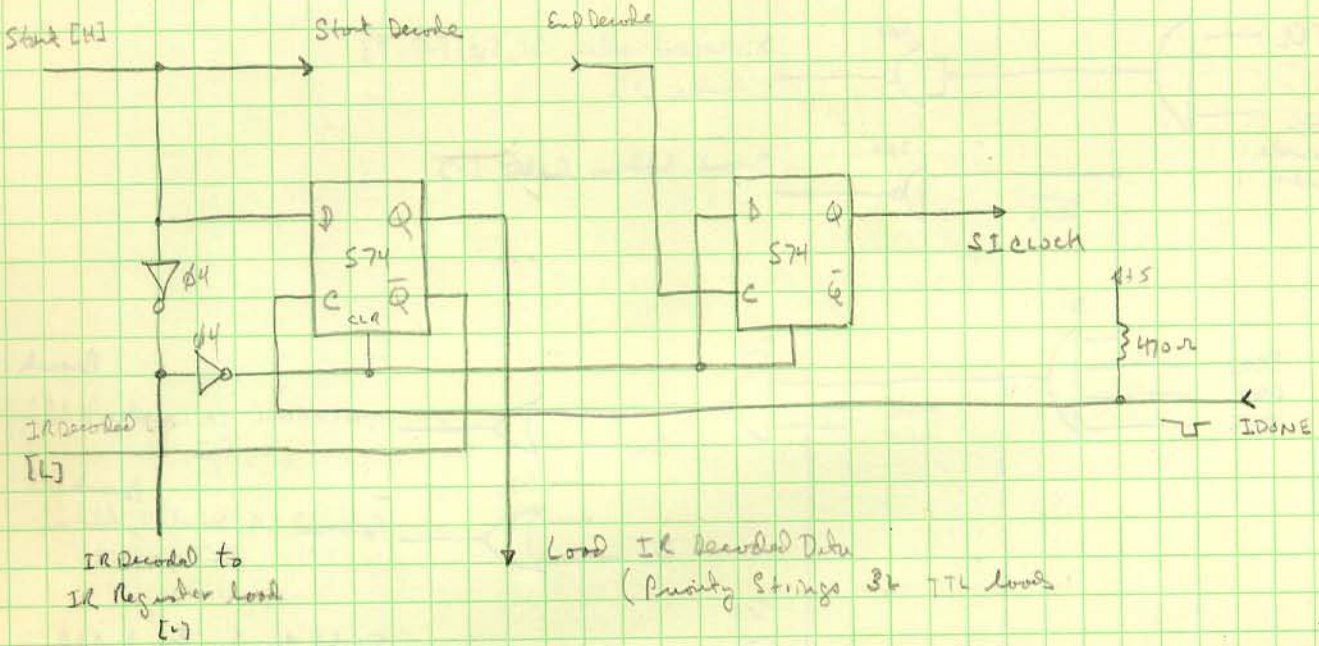
31 Jan 76
ABD

Microcontroller Data Bus Decoding

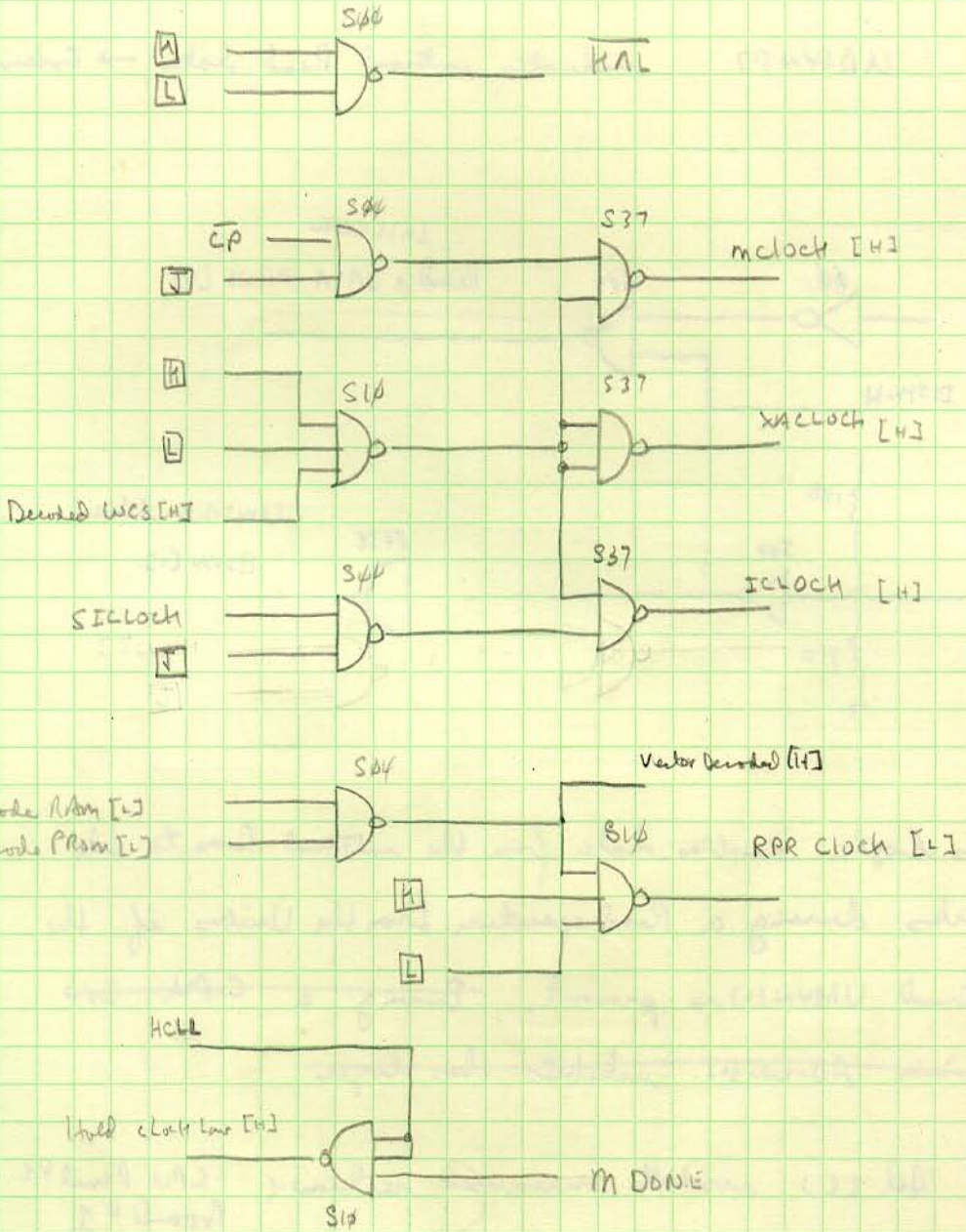


2 Jan 1977
ARG

IR Decoding Clock & Timing



Modifications to the BUS Control Access to Microcode RAMs

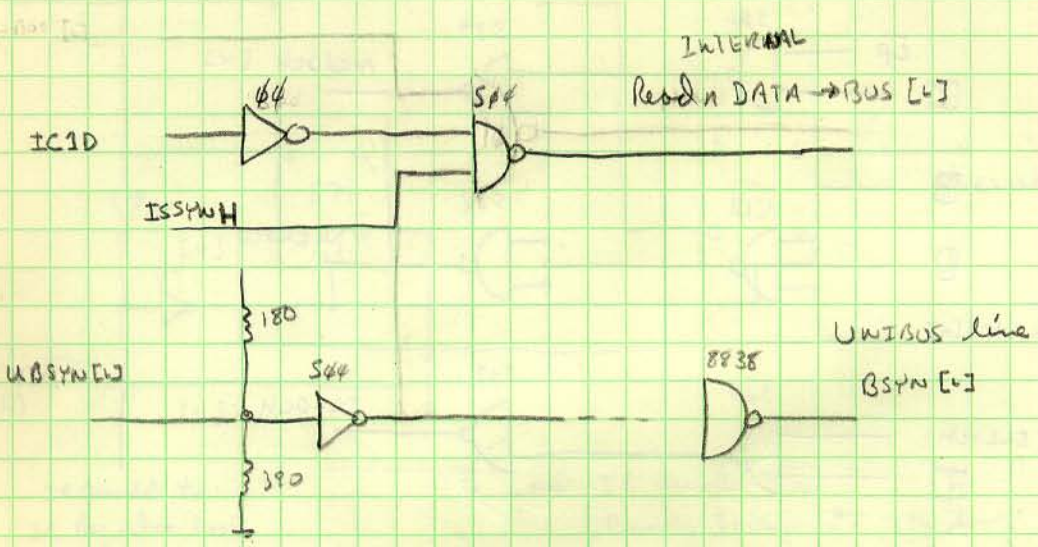


7Jan77
ARB

Modifications to CPU Panel #1

Delete DATA → BUS [L]

Add UBSYN [L] indicates internal Read data → External Unibus



this logic enables data from the internal Bus to the Unibus during a Read operation from the Unibus if the internal UBSYN [L] is present. ~~During a CPU I/O operation AD-BUS [L] inhibits this logic~~

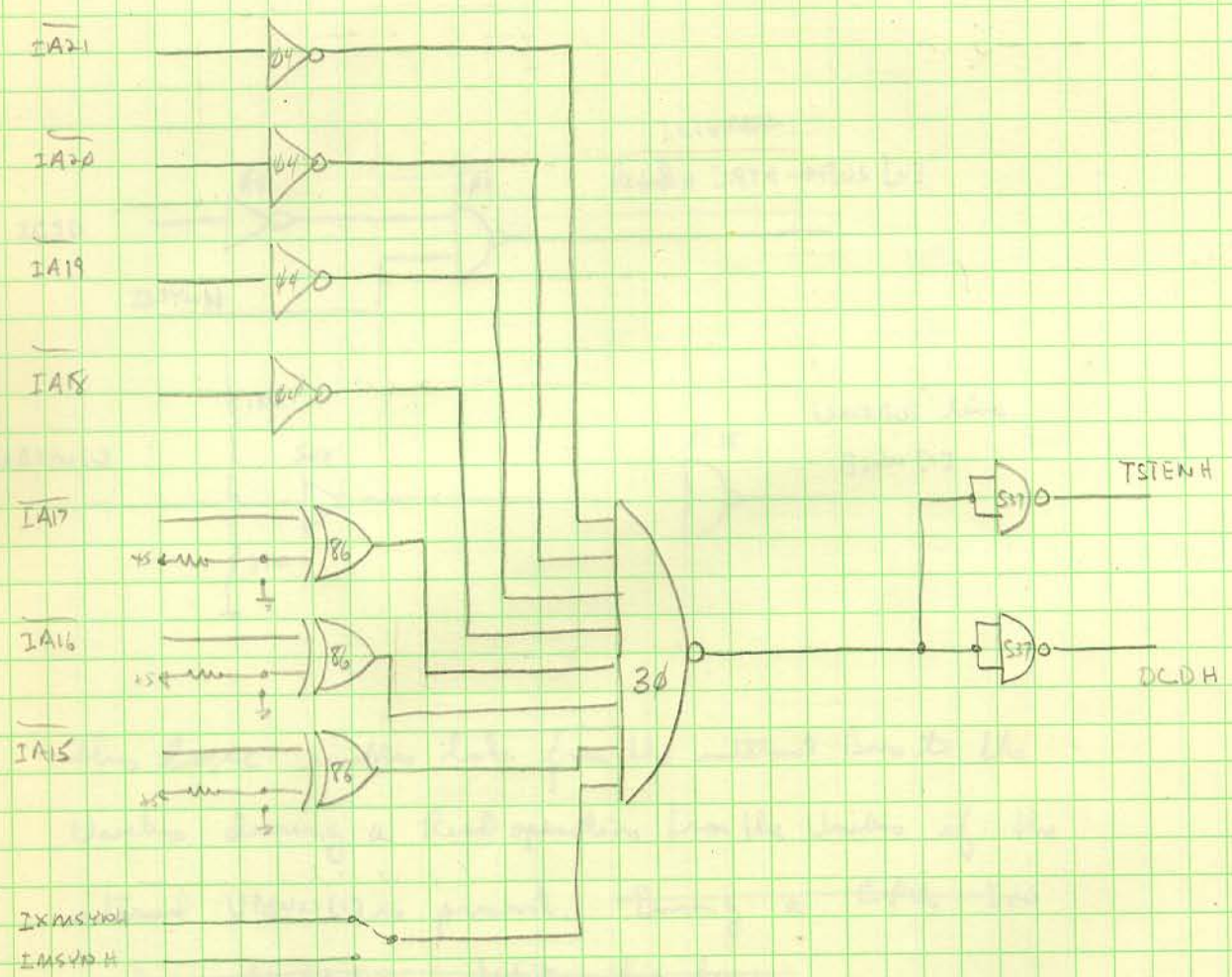
All IC's available in unused sections of CPU Panel #1 Board # 1

8 Jan 77

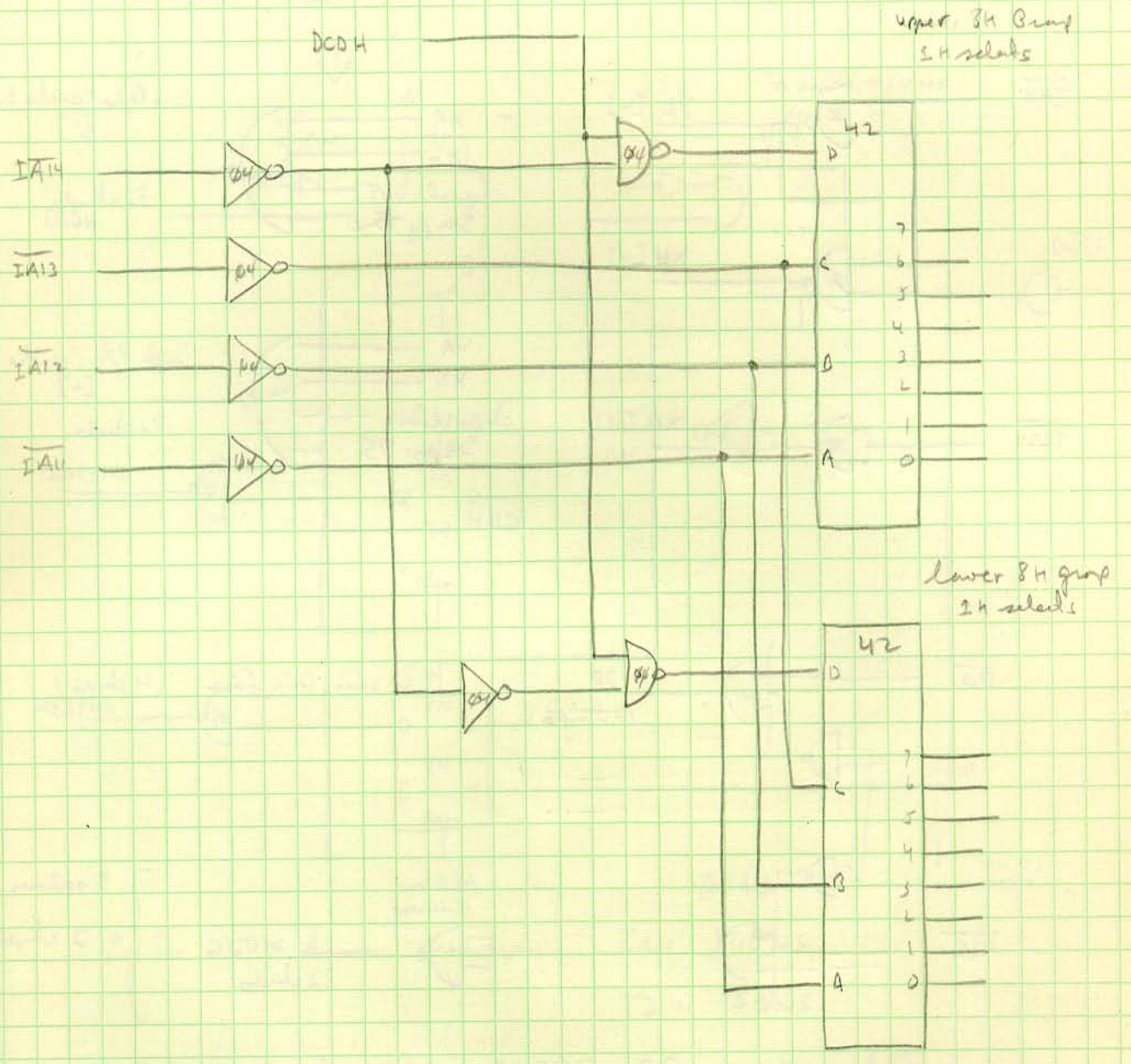
ARD

16K Read/write Memory Panel

Address Selector



Selectible for any 16K slot from Ø to 112K accessible by CPU only or CPU and Unibus


upper 8H Group
1H selects
DCDH
IA14
IA13
IA12
IA11
42
D
C
B
A
7
6
5
4
3
2
1
0
lower 8H group
1H selects
42
D
C
B
A
7
6
5
4
3
2
1
0

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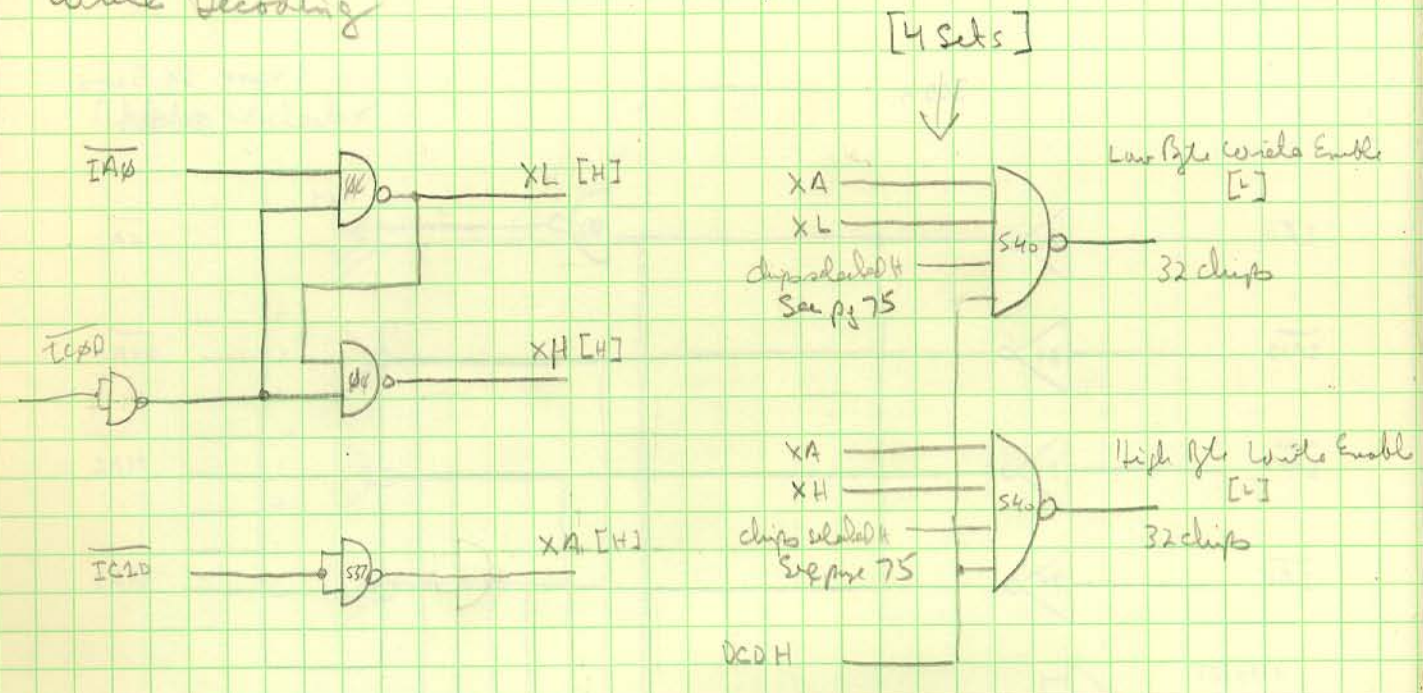
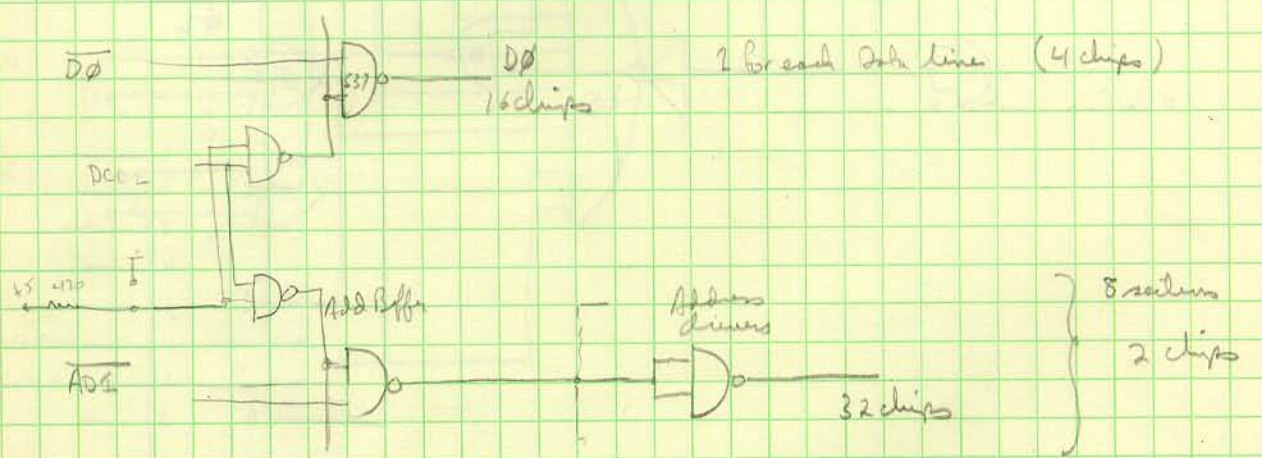
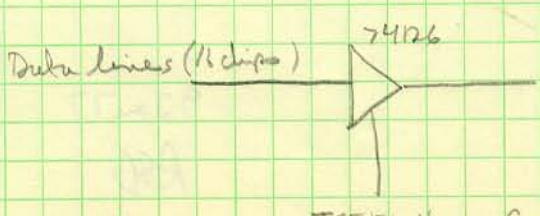
Write Decoding





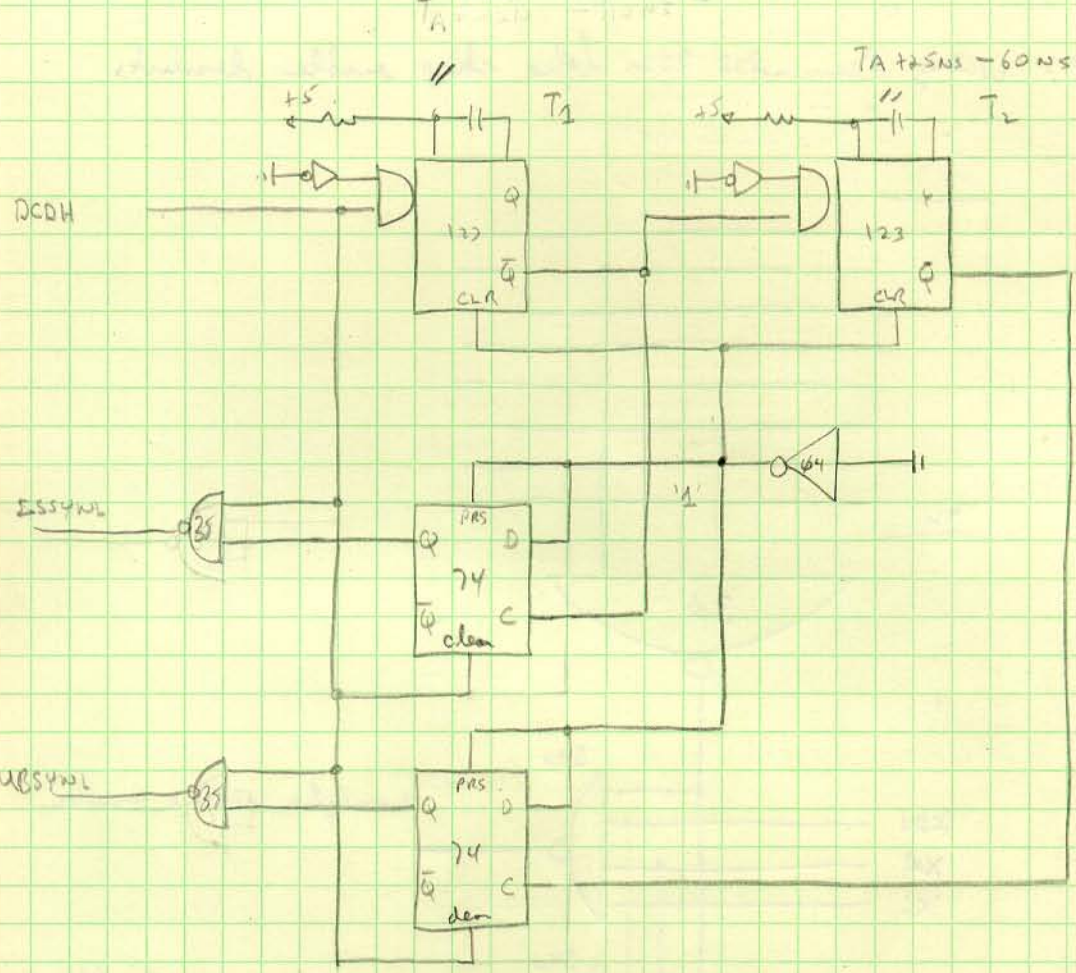
Add. regins 23 74S37 (20 drivers, 3 Buffers)

Tristate output gates



16 lines
[4 chips]

Access timing



∴ for 250NS Access memory T1 = 100NS

T2 = 50NS

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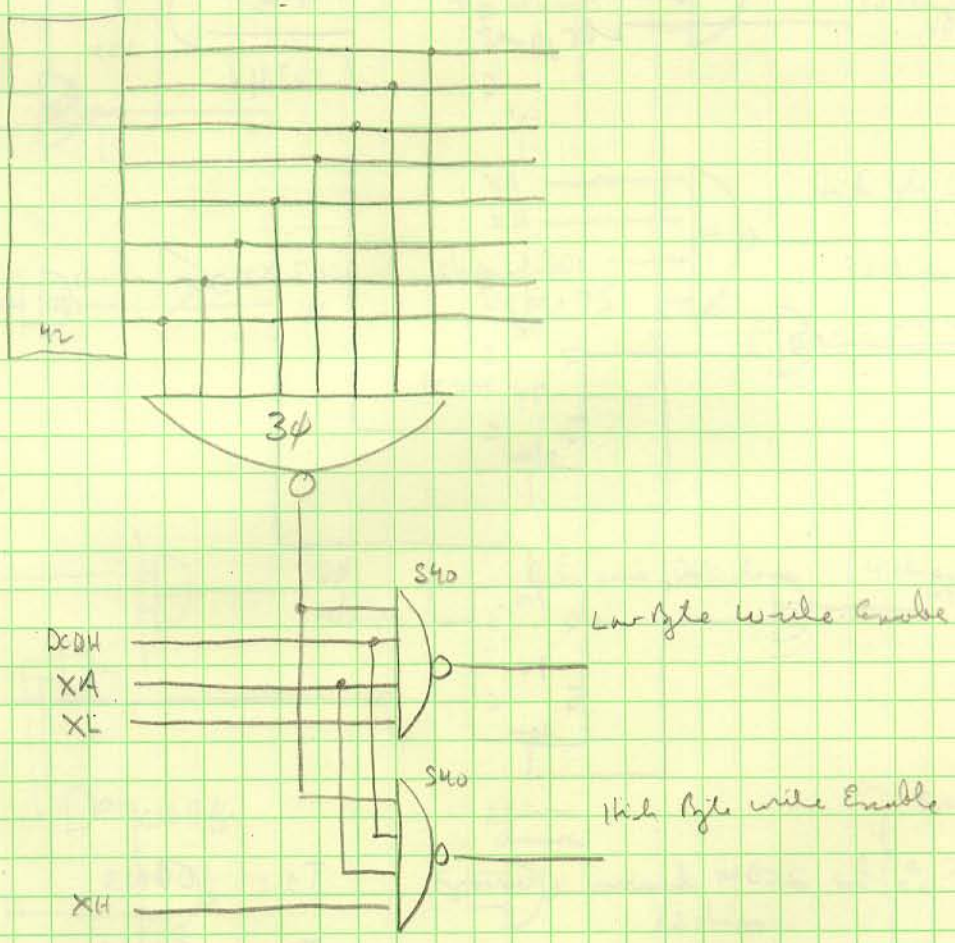
Modify Write enabling to

1) writing enabled 15ns after chip selected

2) writing terminated 25ns before chip enable deselects



(2 set of for each 8K half)

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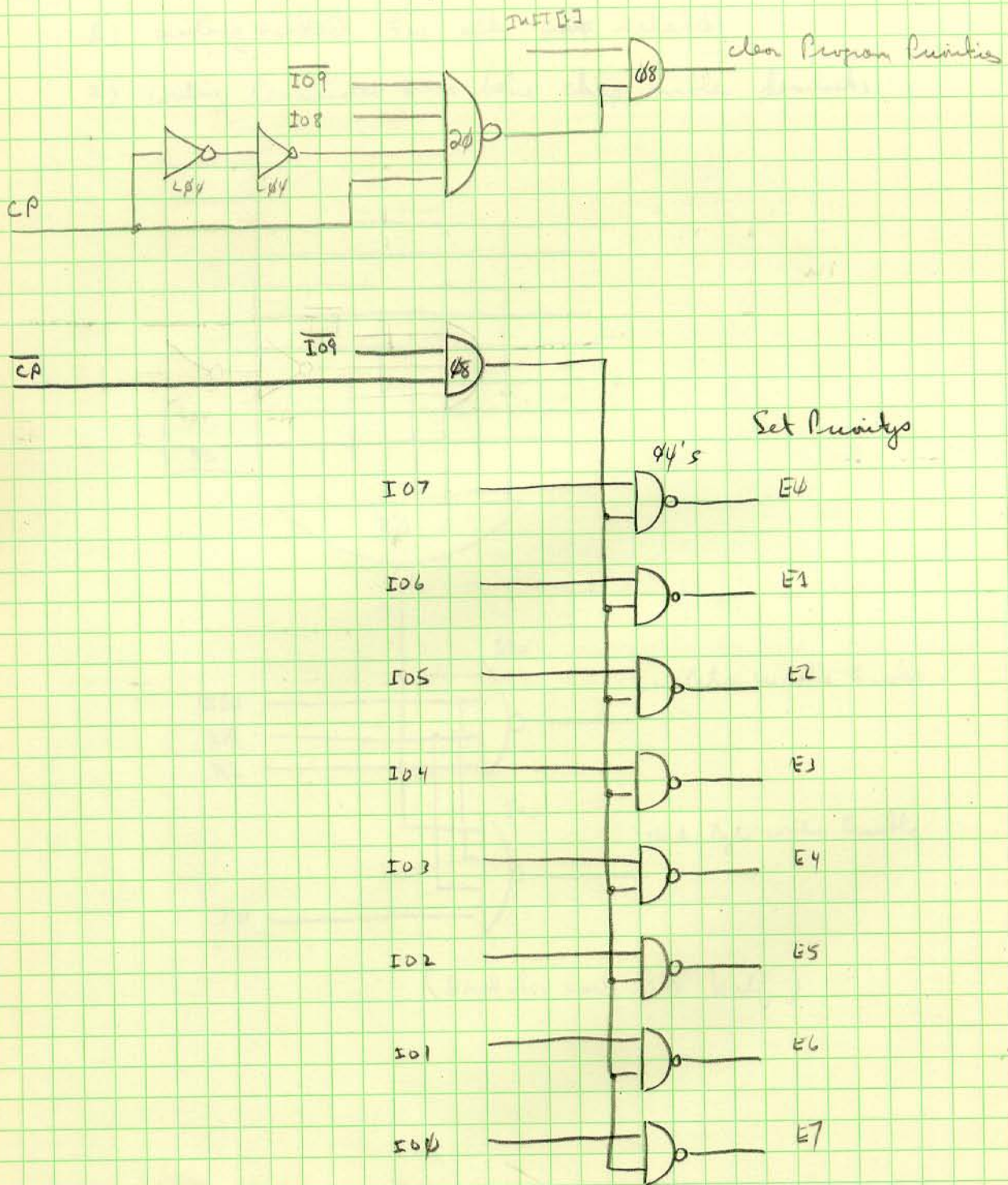
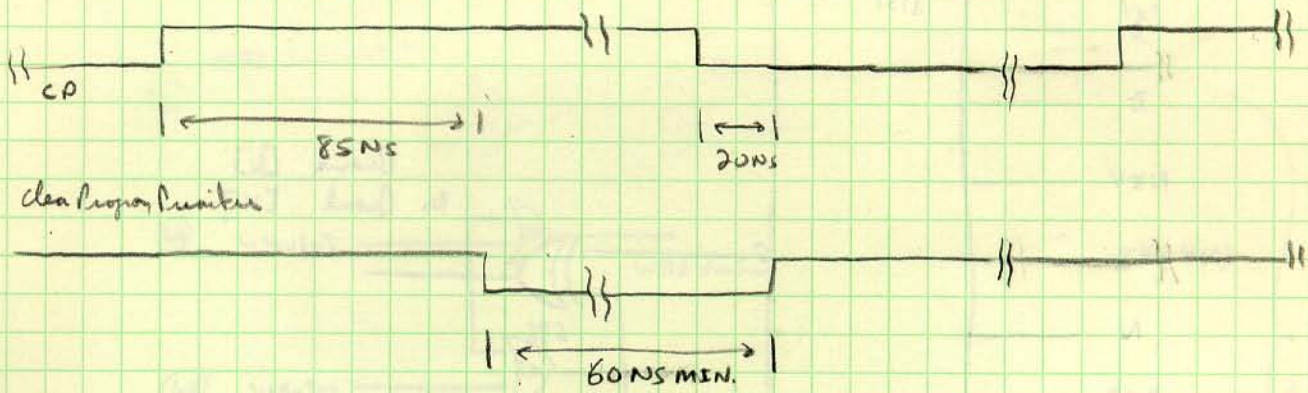
ARD

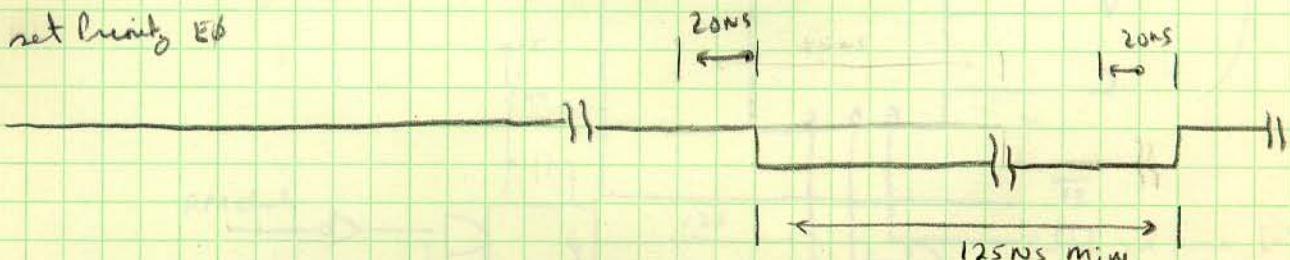
Programmed Priority clear & set



for $\overline{IO9}$ = H
IO8 = H



for IO7 = H



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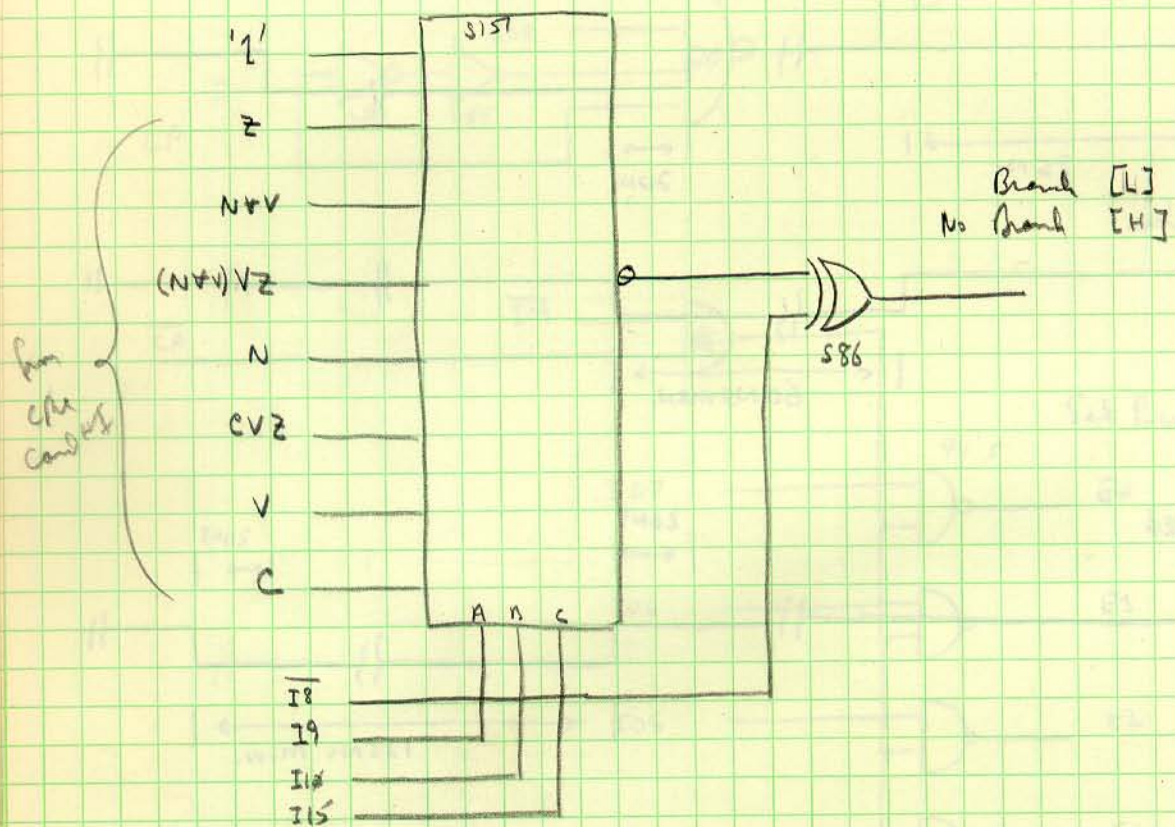
Conditional Branch Instruction Coding



Vector Ram/Prom Access timing / write timing

(see page 70, 64, 25, and 71)