

Memory Systems 1

Missouri '11
Prom/RAM

Missouri '12
RAM

Microcode Panel # 1 (Frame # 4)

4

a) contains 1K x 96 microcode PROM
1K x 32 INST Code PROM

b) 1K x 96 Microcode RAM
1K x 32 INST code RAM

Read/Write organization - RAM 16Kx16

\overline{MA} and \overline{IA} address lines must have
the same address specified

See page 86 for modification of this Panel

Microcode # 1 Prom/RAM

Microcode # 2 RAM

						16
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						2
						1

G

H

I

J

K

L

Microcoda '2 RAM

15 Dec 76
ARB

A	CMS Data	CMS Addressing	Res 123	Res 123	Res 123	Res 123	Res	123
	CMS Data	CMS Addressing	SOS	S44	S44	S40	S37	42
B	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470
	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470
C	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470
	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470
D	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470
	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470
E	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470
	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470
F	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470
	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470
G	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470
	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470	RES 470

All unnumbered are (K x I) RAMs
210L / 3542 Series

6	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
32																
48																
64																
80																
96																
112																
127																

15 Dec 76

ARRS

Microcassette #2
RAM

Connector Listings

CN1 - Tristate Microcode (inverted)

1	MC96	—	C1/1	40	GND			1
2		—	C1/4	39	MC112	—	D1/1	2
3		—	C1/15	38		—	D1/4	3
4		—	C1/12	37		—	D1/15	4
5	GND			36		—	D1/12	5
6		—	C2/1	35	GND			6
7		—	C2/4	34		—	D2/1	7
8		—	C2/15	33		—	D2/4	8
9		—	C2/12	32		—	D2/15	9
10	GND			31		—	D2/12	10
11		—	C3/1	30	GND			11
12		—	C3/4	29		—	D3/1	12
13		—	C3/15	28		—	D3/4	13
14		—	C3/12	27		—	D3/15	14
15	GND			26		—	D3/12	15
16		—	C4/1	25	GND			16
17		—	C4/4	24		—	D4/1	17
18		—	C4/15	23		—	D4/4	18
19	MC111	—	C4/12	22		—	D4/15	19
20	GND			21	MC127	—	D4/12	20

CN2 - Tristate Microcode (inverted)

1	MC64	—	C5/1	40	GND			1
2		—	C5/4	39	MC80	—	D5/1	2
3		—	C5/15	38		—	D5/4	3
4		—	C5/12	37		—	D5/15	4
5	GND			36		—	D5/12	5
6		—	C6/1	35	GND			6
7		—	C6/4	34		—	D6/1	7
8		—	C6/15	33		—	D6/4	8
9		—	C6/12	32		—	D6/15	9
10	GND			31		—	D6/12	10
11		—	C7/1	30	GND			11
12		—	C7/4	29		—	D7/1	12
13		—	C7/15	28		—	D7/4	13
14		—	C7/12	27		—	D7/15	14
15	GND			26		—	D7/12	15
16		—	C8/1	25	GND			16
17		—	C8/4	24		—	D8/1	17
18		—	C8/15	23		—	D8/4	18
19	MC79	—	C8/12	22		—	D8/15	19
20	GND			21	MC95	—	D8/12	20

Connector Listings CN3 - Tristate Microcode (inserted)

1	mc32	—	C9/1	40	GND		
2		—	C9/4	39	mc48	—	D9/1
3		—	C9/15	38		—	D9/4
4		—	C9/12	37		—	D9/15
5	GND			36		—	D9/12
6		—	C10/1	35	GND		
7		—	C10/4	34		—	D10/1
8		—	C10/15	33		—	D10/4
9		—	C10/12	32		—	D10/15
10	GND			31		—	D10/12
11		—	C11/1	30	GND		
12		—	C11/4	29		—	D11/1
13		—	C11/15	28		—	D11/4
14		—	C11/12	27		—	D11/15
15	GND			26		—	D11/12
16		—	C12/1	25	GND		
17		—	C12/4	24		—	D12/1
18		—	C12/15	23		—	D12/4
19	mc47	—	C12/15	22		—	D12/15
20	GND			21	mc63	—	D12/12

CN4 - Tristate Microcode (inserted)

1	mc6	—	C13/1	40	GND		
2		—	C13/4	39	mc16	—	D13/1
3		—	C13/15	38		—	D13/4
4		—	C13/12	37		—	D13/15
5	GND			36		—	D13/12
6		—	C14/1	35	GND		
7		—	C14/4	34		—	D14/1
8		—	C14/15	33		—	D14/4
9		—	C14/12	32		—	D14/15
10	GND			31		—	D14/12
11		—	C15/1	30	GND		
12		—	C15/4	29		—	D15/1
13		—	C15/15	28		—	D15/4
14		—	C15/12	27		—	D15/15
15	GND			26		—	D15/12
16		—	C16/1	25	GND		
17		—	C16/4	24		—	D16/1
18		—	C16/15	23		—	D16/4
19	mc15	—	C16/12	22		—	D16/15
20	GND			21	mc31	—	D16/12

Microcode #2
RAM

Connector Listings

CN7 - Buffered Micros

1	MC96	-	C1/3	40	GND			1
2		-	C1/6	39	MC112	-	D1/3	2
3		-	C1/13	38		-	D1/6	3
4		-	C1/10	37		-	D1/13	4
5	GND			36		-	D1/10	5
6		-	C2/3	35	GND			6
7		-	C2/6	34		-	D2/3	7
8		-	C2/13	33		-	D2/6	8
9		-	C2/10	32		-	D2/13	9
10	GND			31		-	D2/10	10
11		-	C3/3	30	GND			11
12		-	C3/6	29		-	D3/3	12
13		-	C3/13	28		-	D3/6	13
14		-	C3/10	27		-	D3/13	14
15	GND			26		-	D3/10	15
16		-	C4/3	25	GND			16
17		-	C4/6	24		-	D4/3	17
18		-	C4/13	23		-	D4/6	18
19	MC111	-	C4/10	22		-	D4/13	19
20	GND			21	MC127	-	D4/10	20

CN8 - Buffered Micros

1	MC64	-	C5/3	40	GND			1
2		-	C5/6	39	MC80	-	D5/3	2
3		-	C5/13	38		-	D5/6	3
4		-	C5/10	37		-	D5/13	4
5	GND			36		-	D5/10	5
6		-	C6/3	35	GND			6
7		-	C6/6	34		-	D6/3	7
8		-	C6/13	33		-	D6/6	8
9		-	C6/10	32		-	D6/13	9
10	GND			31		-	D6/10	10
11		-	C7/3	30	GND			11
12		-	C7/6	29		-	D7/3	12
13		-	C7/13	28		-	D7/6	13
14		-	C7/10	27		-	D7/13	14
15	GND			26		-	D7/10	15
16		-	C8/3	25	GND			16
17		-	C8/6	24		-	D8/3	17
18		-	C8/13	23		-	D8/6	18
19	MC79	-	C8/10	22		-	D8/13	19
20	GND			21	MC95	-	D8/10	20

CN9 - Buffered Microcode

1	mc32	-	C9/3	40	GND	
2		-	C9/6	39	mc48	- D9/3
3		-	C9/13	38		- D9/6
4		-	C9/10	37		- D9/13
5	GND			36		- D9/10
6		-	C10/3	35	GND	
7		-	C10/6	34		- D10/3
8		-	C10/13	33		- D10/6
9		-	C10/10	32		- D10/13
10	GND			31		- D10/10
11		-	C11/3	30	GND	
12		-	C11/6	29		- D11/3
13		-	C11/13	28		- D11/6
14		-	C11/10	27		- D11/13
15	GND			26		- D11/10
16		-	C12/3	25	GND	
17		-	C12/6	24		- D12/3
18		-	C12/10	23		- D12/6
19	mc47	-	C12/10	22		- D12/13
20	GND			21	mc63	- D12/10

CN10 - Buffered Microcode

1	mc φ	-	C13/3	40	GND	
2		-	C13/6	39	mc16	- D13/3
3		-	C13/13	38		- D13/6
4		-	C13/10	37		- D13/13
5	GND			36		- D13/10
6		-	C14/3	35	GND	
7		-	C14/6	34		- D14/3
8		-	C14/13	33		- D14/6
9		-	C14/10	32		- D14/13
10	GND			31		- D14/10
11		-	C15/3	30	GND	
12		-	C15/6	29		- D15/3
13		-	C15/13	28		- D15/6
14		-	C15/10	27		- D15/13
15	GND			26		- D15/10
16		-	C16/3	25	GND	
17		-	C16/6	24		- D16/3
18		-	C16/13	23		- D16/6
19	mc15	-	C16/10	22		- D16/13
20	GND			21	mc31	- D15/10

Microcode #2 RAM

Connector Listings

CN5/CN11 - Data

1	DA0	-	E32/11	40	GND		
2		-	E31/11	39	WLB[L]	-	B30/15
3		-	E30/11	38			
4		-	E29/11	37			
5	GND			36	WHB[L]	-	B30/12
6		-	E28/11	35	GND		
7		-	E27/11	34	WAW	-	B31/15
8		-	E26/11	33	WA1	-	B31/14
9		-	E25/11	32	WA2	-	B31/13
10	GND			31			
11		-	E24/11	30	GND		
12		-	E23/11	29	XACLOCK	-	B28/4
13		-	E22/11	28			
14		-	E21/11	27			
15	GND			26	XADONE	-	B25/6
16		-	E20/11	25	GND		C20/9
17		-	E19/11	24			
18		-	E18/11	23			
19	DA15	-	E17/11	22			
20	GND			21			

CN6/CN12 - Address

1	MA0	-	C23/1	40	GND		
2		-	C23/4	39	IA0	-	C22/1
3		-	D23/1	38		-	C22/4
4		-	D23/4	37		-	D22/1
5	GND			36		-	D22/4
6		-	C23/15	35	GND		
7		-	C23/12	34		-	C22/15
8		-	D23/15	33		-	C22/12
9		-	D23/12	32		-	D22/15
10	GND			31		-	D22/12
11		-	D32/4	30	GND		
12		-	D32/12	29		-	C32/1
13		-	B27/3	28		-	C32/15
14	MA11	-	B27/13	27		-	B26/13
15	GND			26	IA11	-	B26/13
16	MCLOCK	-	C26/12	25	GND		
17				24	ICLOCK	-	C26/4
18	MDONE [L]	-	B25/2	23			
19	MSL [L]	-	C26/11	22	IDONE [L]	-	B25/4
20	GND			21	IDSL [L]	-	C26/5

MC

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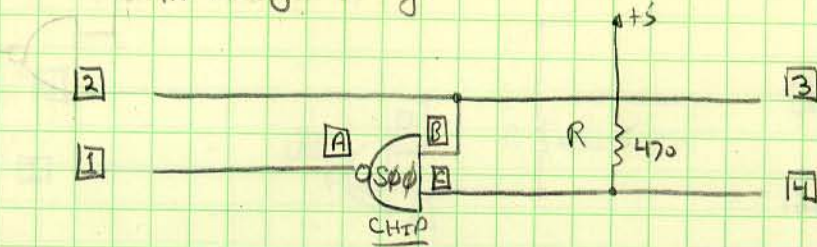
30

31

32

Buffering Logic

Changed



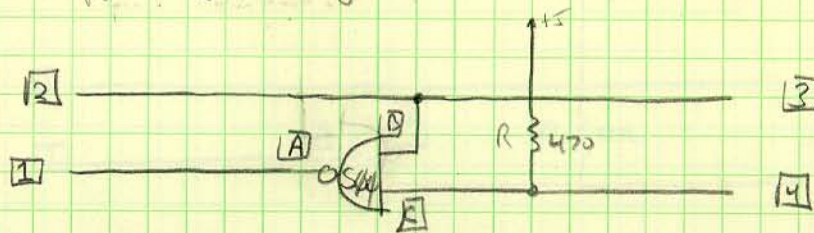
mc	1	A	B	2	3	4	C	R	R	CHIP
0	CN10/1	3	1	CN4/1	E32/12	E13/12	2	C18/2	C13	
1	CN10/2	6	4	CN4/2	E31/12	/ 11	5	C18/4		
2	CN10/3	13	15	CN4/3	E30/12	/ 10	14	C18/3		
3	CN10/4	10	12	CN4/4	E29/12	/ 9	11	C18/5		
4	CN10/6	3	1	CN4/6	E28/12	E14/12	2	C17/11	C14	
5	CN10/7	6	4	CN4/7	E27/12	/ 11	5	C17/10		
6	CN10/8	13	15	CN4/8	E26/12	/ 10	14	C17/6		
7	CN10/9	10	12	CN4/9	E25/12	/ 9	11	C17/7		
8	CN10/11	3	1	CN4/11	E24/12	E15/12	2	C17/15	C15	
9	CN10/12	6	4	CN4/12	E23/12	/ 11	5	C17/13		
10	CN10/13	13	15	CN4/13	E22/12	/ 10	14	C17/14		
11	CN10/14	10	12	CN4/14	E21/12	/ 9	11	C17/12		
12	CN10/16	3	1	CN4/16	E20/12	E16/12	2	C17/2	C16	
13	CN10/17	6	4	CN4/17	E19/12	/ 11	5	C17/4		
14	CN10/18	13	15	CN4/18	E18/12	/ 10	14	C17/3		
15	CN10/19	10	12	CN4/19	E17/12	/ 9	11	C17/5		
16	CN10/39	3	1	CN4/39	F32/12	F13/12	2	D18/2	D13	
17	CN10/38	6	4	CN4/38	F31/12	/ 11	5	D18/4		
18	CN10/37	13	15	CN4/37	F30/12	/ 10	14	D18/3		
19	CN10/36	10	12	CN4/36	F29/12	/ 9	11	D18/5		
20	CN10/34	3	1	CN4/34	F28/12	F14/12	2	D17/11	D14	
21	CN10/33	6	4	CN4/33	F27/12	/ 11	5	D17/10		
22	CN10/32	13	15	CN4/32	F26/12	/ 10	14	D17/6		
23	CN10/31	10	12	CN4/31	F25/12	/ 9	11	D17/7		
24	CN10/29	3	1	CN4/29	F24/12	F15/12	2	D17/15	D15	
25	CN10/28	6	4	CN4/28	F23/12	/ 11	5	D17/13		
26	CN10/27	13	15	CN4/27	F22/12	/ 10	14	D17/14		
27	CN10/26	10	12	CN4/26	F21/12	/ 9	11	D17/12		
28	CN10/24	3	1	CN4/24	F20/12	F16/12	2	D17/12	D16	
29	CN10/23	6	4	CN4/23	F19/12	/ 11	5	D17/4		
30	CN10/22	13	15	CN4/22	F18/12	/ 10	14	D17/3		
31	CN10/21	10	12	CN4/21	F17/12	/ 9	11	D17/5		

15 Dec 76
AGD

Microc. #2
RAM

Buffering Logic

Changed



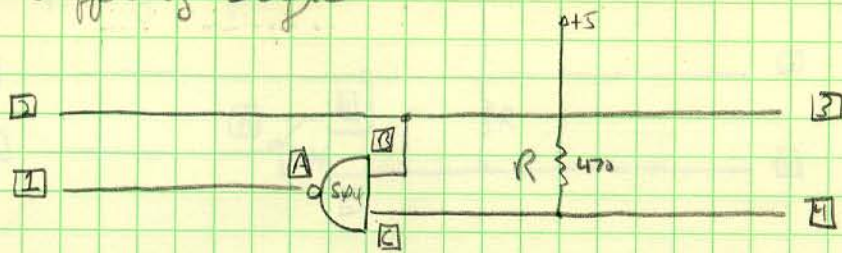
mc	1	A	B	2	3	4	5	R	CHIP
32	CN9/1	3	1	CN3/1	G32/12	E9/12	2	C19/15	C9
33	CN9/2	6	4	CN3/2	G31/12	11	5	C19/13	
34	CN9/3	13	15	CN3/3	G30/12	10	14	C19/14	
35	CN9/4	10	12	CN3/4	G29/12	9	11	C19/12	
36	CN9/6	3	1	CN3/6	G28/12	E10/12	2	C19/2	C10
37	CN9/7	6	4	CN3/7	G27/12	11	5	C19/4	
38	CN9/8	13	15	CN3/8	G26/12	10	14	C19/3	
39	CN9/9	10	12	CN3/9	G25/12	9	11	C19/5	
40	CN9/11	3	1	CN3/11	G24/12	E11/12	2	C18/11	C11
41	CN9/12	6	4	CN3/12	G23/12	11	5	C18/10	
42	CN9/13	13	15	CN3/13	G22/12	10	14	C18/6	
43	CN9/14	10	12	CN3/14	G21/12	9	11	C18/7	
44	CN9/16	3	1	CN3/16	G20/12	E12/12	2	C18/15	C12
45	CN9/17	6	4	CN3/17	G19/12	11	5	C18/13	
46	CN9/18	13	15	CN3/18	G18/12	10	14	C18/14	
47	CN9/19	10	12	CN3/19	G17/12	9	11	C18/12	
48	CN9/39	3	1	CN3/39	H32/12	F9/12	2	D19/15	D9
49	CN9/38	6	4	CN3/38	H31/12	11	5	D19/13	
50	CN9/37	13	15	CN3/37	H30/12	10	14	D19/14	
51	CN9/36	10	12	CN3/36	H29/12	9	11	D19/12	
52	CN9/34	3	1	CN3/34	H28/12	F10/12	2	D19/2	D10
53	CN9/33	6	4	CN3/33	H27/12	11	5	D19/4	
54	CN9/32	13	15	CN3/32	H26/12	10	14	D19/3	
55	CN9/31	10	12	CN3/31	H25/12	9	11	D19/5	
56	CN9/29	3	1	CN3/29	H24/12	F11/12	2	D18/11	D11
57	CN9/28	6	4	CN3/28	H23/12	11	5	D18/10	
58	CN9/27	13	15	CN3/27	H22/12	10	14	D18/6	
59	CN9/26	10	12	CN3/26	H21/12	9	11	D18/7	
60	CN9/24	3	1	CN3/24	H20/12	F12/12	2	D18/15	D12
61	CN9/23	6	4	CN3/23	H19/12	11	5	D18/13	
62	CN9/22	13	15	CN3/22	H18/12	10	14	D18/14	
63	CN9/21	10	12	CN3/21	H17/12	9	11	D18/12	

Microcode #2 RAM

16 Dec 1976
APD

Buffering Logic

changed



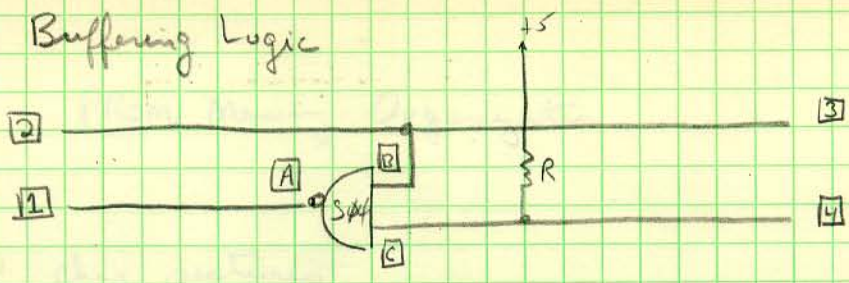
mc	[1]	[A]	[B]	[2]	[3]	[4]	[5]	R	CHIP
64	CN8/1	3	1	CN2/1	I32/12	E5/12	2	C20/11	C5
65	CN8/2	6	4	CN2/2	I31/12	11	5	C20/10	
66	CN8/3	13	15	CN2/3	I30/12	10	14	C20/6	
67	CN8/4	10	12	CN2/4	I29/12	9	11	C20/7	
68	CN8/6	3	1	CN2/6	I28/12	E6/12	2	C20/15	C6
69	CN8/7	6	4	CN2/7	I27/12	11	5	C20/13	
70	CN8/8	13	15	CN2/8	I26/12	10	14	C20/14	
71	CN8/9	10	12	CN2/9	I25/12	9	11	C20/12	
72	CN8/11	3	1	CN2/11	I24/12	E7/12	2	C20/2	C7
73	CN8/12	6	4	CN2/12	I23/12	11	5	C20/4	
74	CN8/13	13	15	CN2/13	I22/12	10	14	C20/3	
75	CN8/14	10	12	CN2/14	I21/12	9	11	C20/5	
76	CN8/16	3	1	CN2/16	I20/12	E8/12	2	C19/11	C8
77	CN8/17	6	4	CN2/17	I19/12	11	5	C19/10	
78	CN8/18	13	15	CN2/18	I18/12	10	14	C19/6	
79	CN8/19	10	12	CN2/19	I17/12	9	11	C19/7	
80	CN8/39	3	1	CN2/39	J32/12	F5/12	2	D20/11	D5
81	CN8/38	6	4	CN2/38	J31/12	11	5	D20/10	
82	CN8/37	13	15	CN2/37	J30/12	10	14	D20/6	
83	CN8/36	10	12	CN2/36	J29/12	9	11	D20/7	
84	CN8/34	3	1	CN2/34	J28/12	F6/12	2	D20/15	D6
85	CN8/33	6	4	CN2/33	J27/12	11	5	D20/13	
86	CN8/32	13	15	CN2/32	J26/12	10	14	D20/14	
87	CN8/31	10	12	CN2/31	J25/12	9	11	D20/12	
88	CN8/29	3	1	CN2/29	J24/12	F7/12	2	D20/8	D7
89	CN8/28	6	4	CN2/28	J23/12	11	5	D20/4	
90	CN8/27	13	15	CN2/27	J22/12	10	14	D20/3	
91	CN8/26	10	12	CN2/26	J21/12	9	11	D20/5	
92	CN8/24	3	1	CN2/24	J20/12	F8/12	2	D19/11	D8
93	CN8/23	6	4	CN2/23	J19/12	11	5	D19/10	
94	CN8/22	13	15	CN2/22	J18/12	10	14	D19/6	
95	CN8/21	10	12	CN2/21	J17/12	9	11	D19/7	

Microc 142 RAM

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ARB

Buffering Logic

Changed



MC -	1	A	B	2	3	4	C	R	CHIP
96	CN7/1	3	1	CN1/1	H32/12	E1/12	2	C19/1	C1
97	CN7/2	6	4	CN1/2	H31/12	11	5	C20/1	
98	CN7/3	13	15	CN1/3	H30/12	10	14	C17/1	
99	CN7/4	10	12	CN1/4	H29/12	9	11	C18/1	
100	CN7/6	3	1	CN1/6	H28/12	E2/12	2	C21/11	C2
101	CN7/7	6	4	CN1/7	H27/12	11	5	C21/10	
102	CN7/8	13	15	CN1/8	H26/12	10	14	C21/6	
103	CN7/9	10	12	CN1/9	H25/12	9	11	C21/7	
104	CN7/11	3	1	CN1/11	H24/12	E3/12	2	C21/15	C3
105	CN7/12	6	4	CN1/12	H23/12	11	5	C21/13	
106	CN7/13	13	15	CN1/13	H22/12	10	14	C21/14	
107	CN7/14	10	12	CN1/14	H21/12	9	11	C21/12	
108	CN7/16	3	1	CN1/16	H20/12	E4/12	2	C21/2	C4
109	CN7/17	6	4	CN1/17	H19/12	11	5	C21/4	
110	CN7/18	13	15	CN1/18	H18/12	10	14	C21/3	
111	CN7/19	10	12	CN1/19	H17/12	9	11	C21/5	
112	CN7/39	3	1	CN1/39	L32/12	F1/12	2	D19/1	D1
113	CN7/38	6	4	CN1/38	L31/12	11	5	D20/1	
114	CN7/37	13	15	CN1/37	L30/12	10	14	D17/1	
115	CN7/36	10	12	CN1/36	L29/12	9	11	D18/1	
116	CN7/34	3	1	CN1/34	L28/12	F2/12	2	D21/11	D2
117	CN7/33	6	4	CN1/33	L27/12	11	5	D21/10	
118	CN7/32	13	15	CN1/32	L26/12	10	14	D21/6	
119	CN7/31	10	12	CN1/31	L25/12	9	11	D21/7	
120	CN7/29	3	1	CN1/29	L24/12	F3/12	2	D21/15	D3
121	CN7/28	6	4	CN1/28	L23/12	11	5	D21/13	
122	CN7/27	13	15	CN1/27	L22/12	10	14	D21/14	
123	CN7/26	10	12	CN1/26	L21/12	9	11	D21/12	
124	CN7/24	3	1	CN1/24	L20/12	F4/12	2	D21/2	D4
125	CN7/23	6	4	CN1/23	L19/12	11	5	D21/4	
126	CN7/22	13	15	CN1/22	L18/12	10	14	D21/3	
127	CN7/21	10	12	CN1/21	L17/12	9	11	D21/5	

Microcords #2 RAM

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ARR

PROM Memory Organization

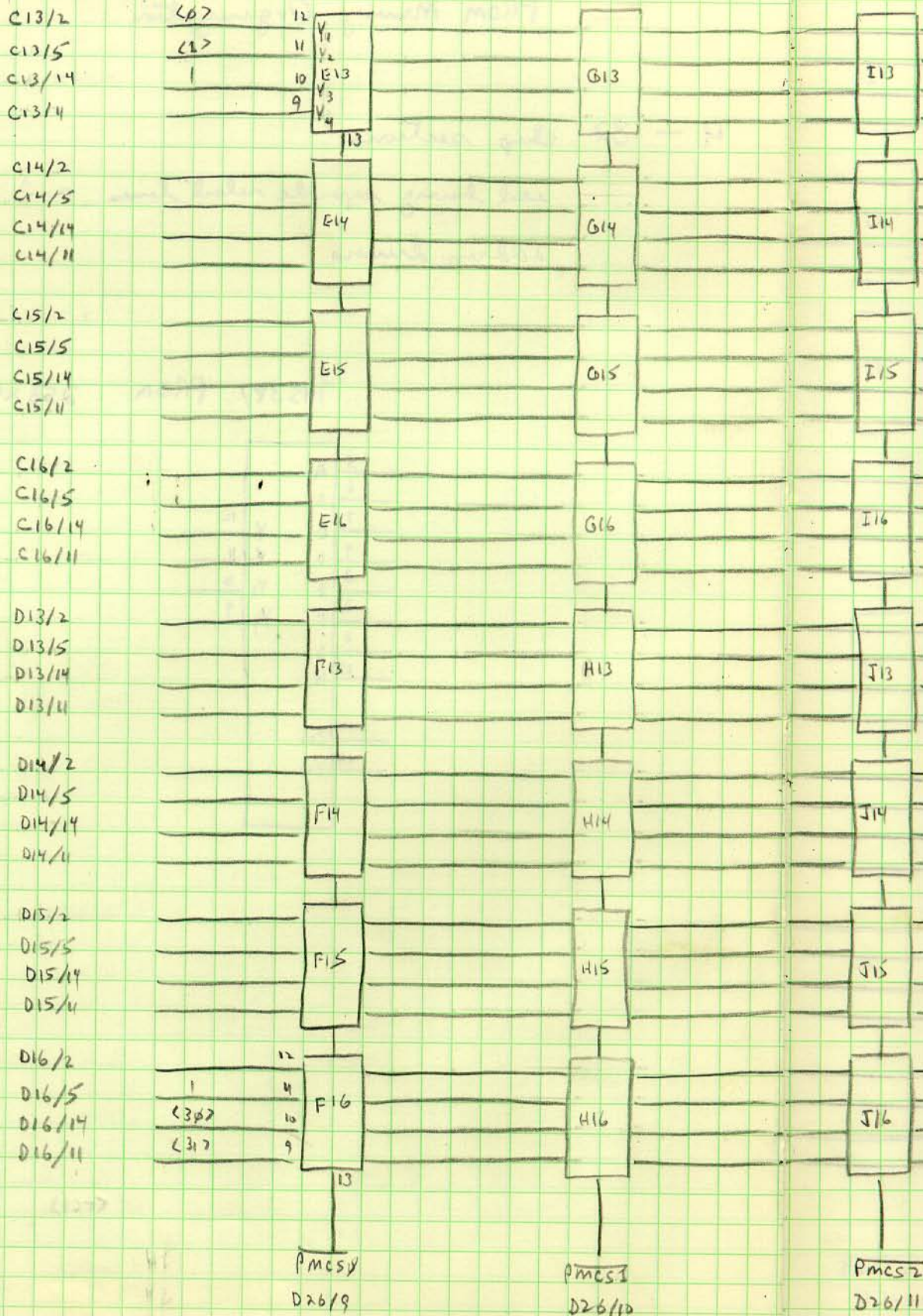
4 - 32 chip sections

each having separate select lines and address drivers

74S387 PROM 256x4

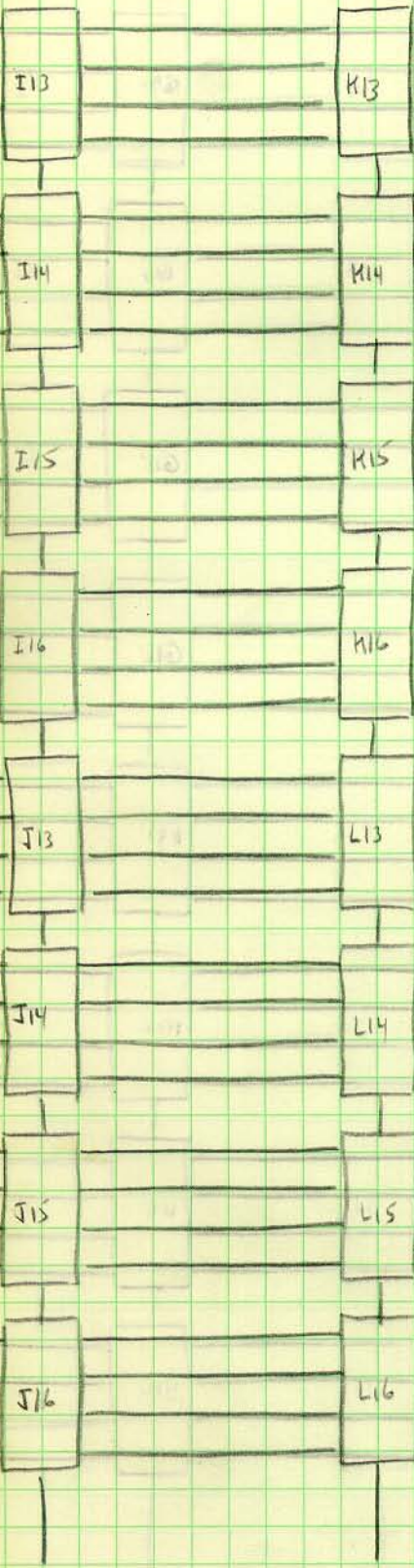


74S387 PROMS
1Kx32

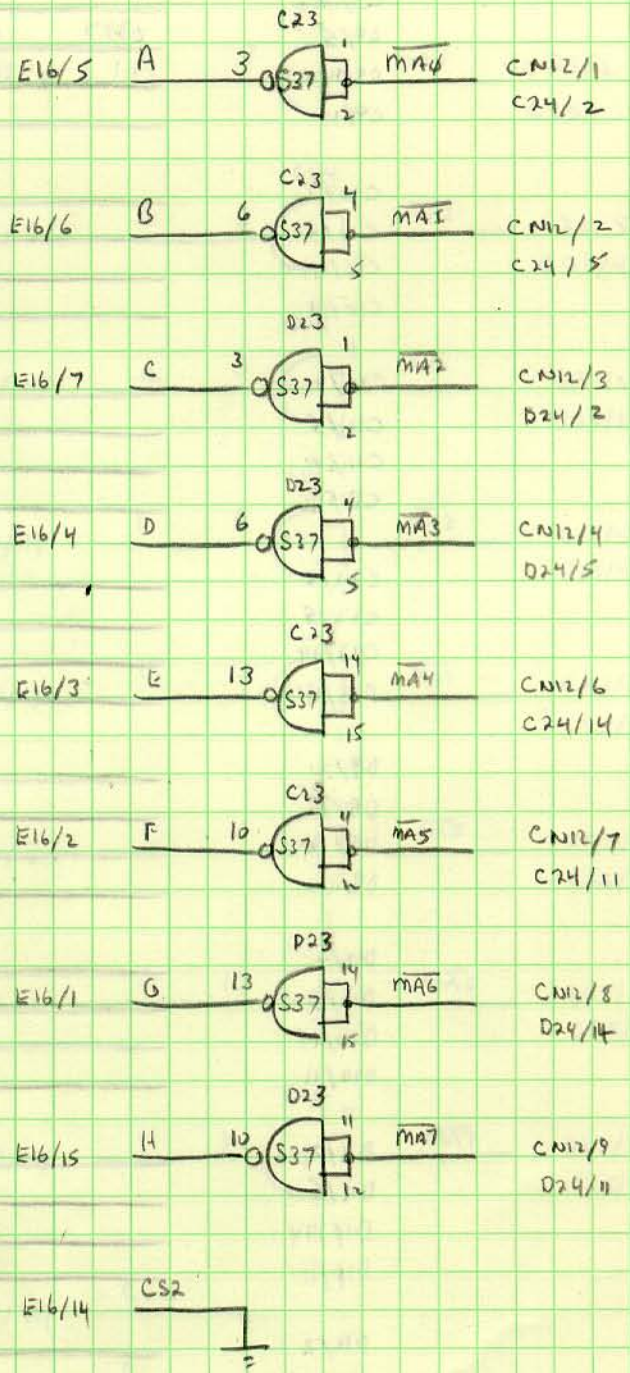


<31:667>
INSTRUCTION MICROCODE

Address lines
to all 32 chips

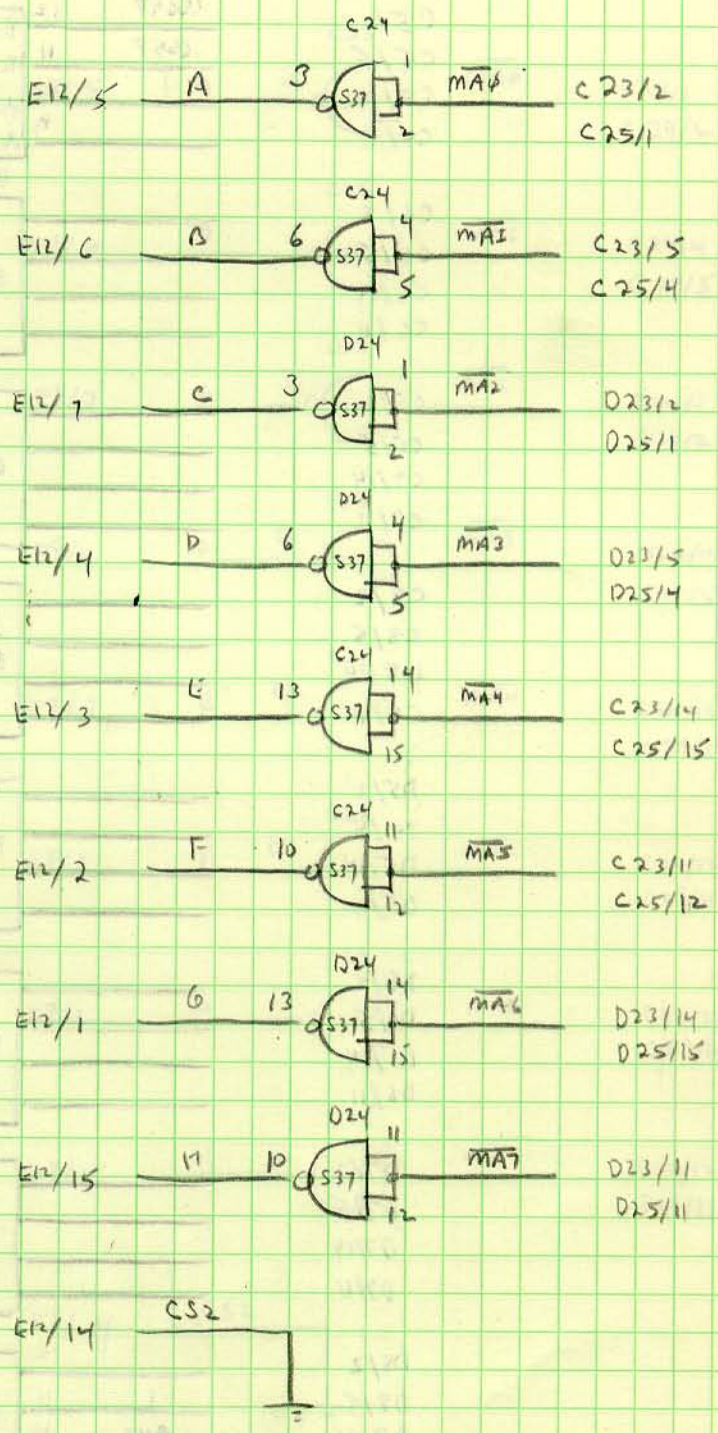
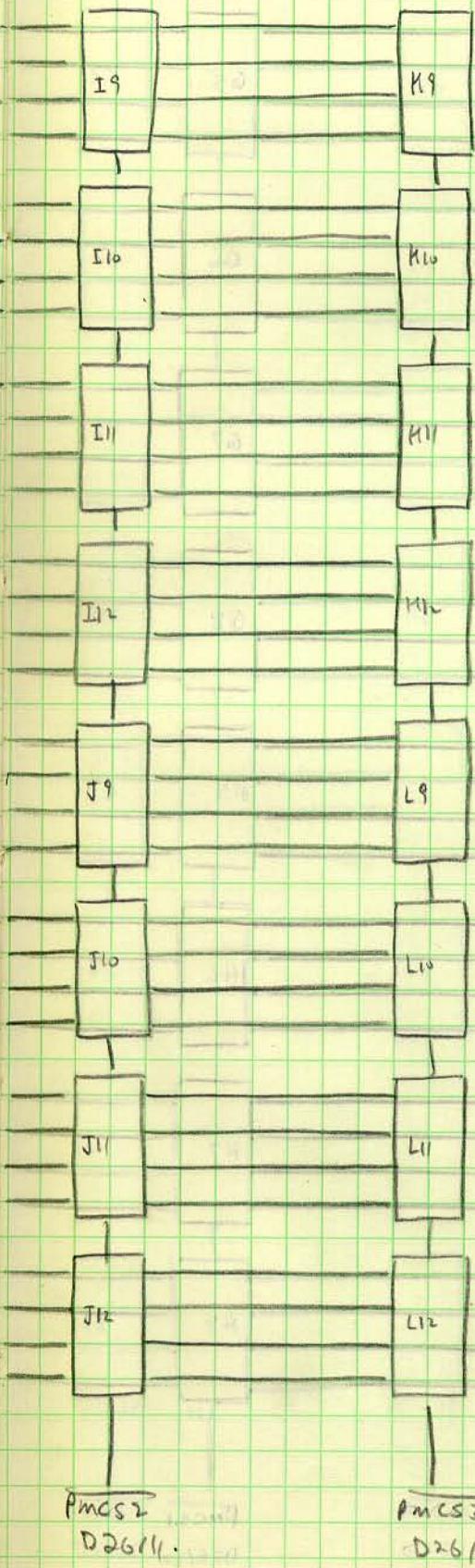


Pmcs2 D26/11 Pmcs3 D26/12



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Address lines to all 32 chips ✓



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74S387 PROMS
1Kx32

- C5/2
- C5/5
- C5/14
- C5/11

- C6/2
- C6/5
- C6/14
- C6/11

- C7/2
- C7/5
- C7/14
- C7/11

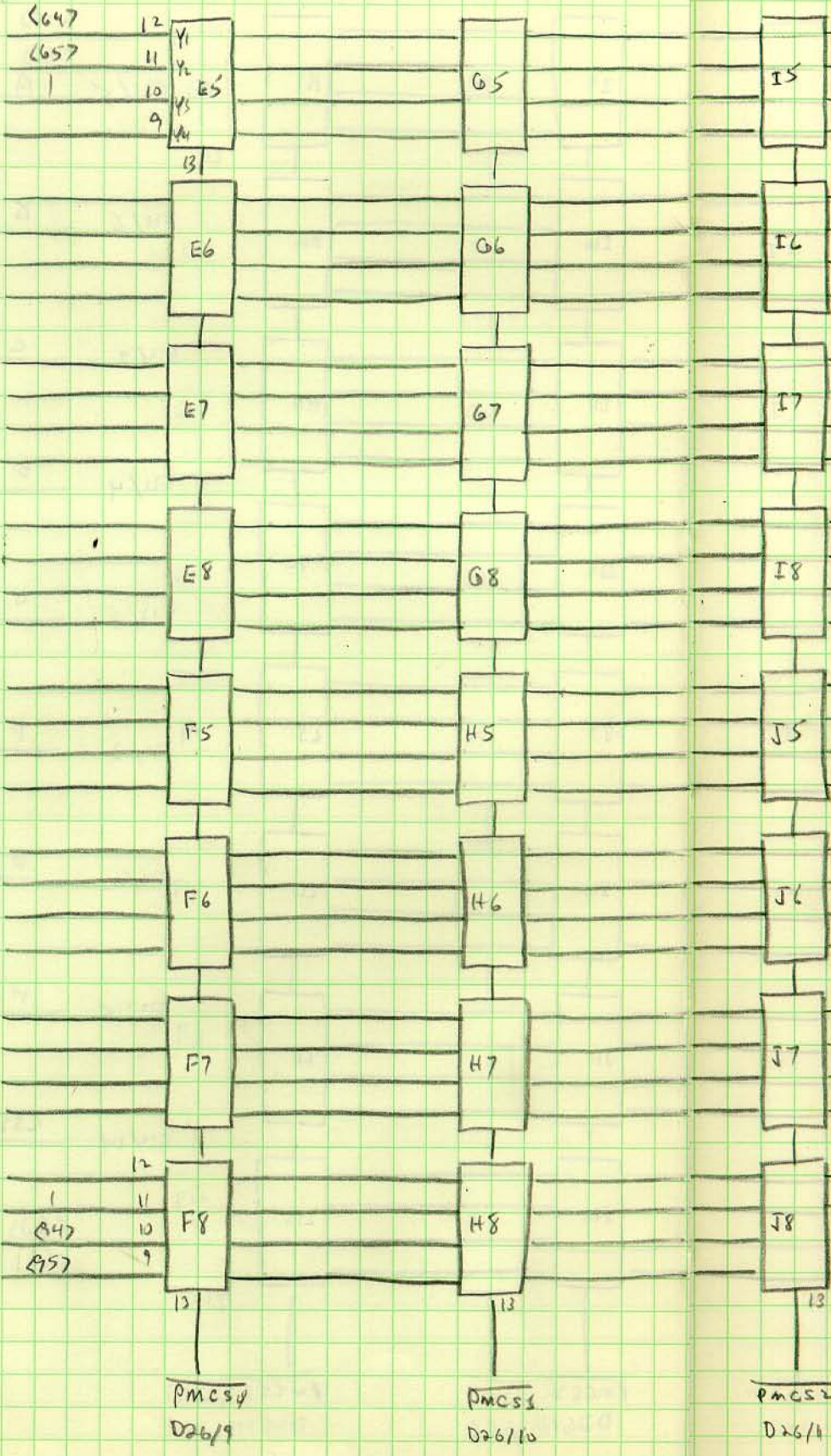
- C8/2
- C8/5
- C8/14
- C8/11

- D5/2
- D5/5
- D5/14
- D5/11

- D6/2
- D6/5
- D6/14
- D6/11

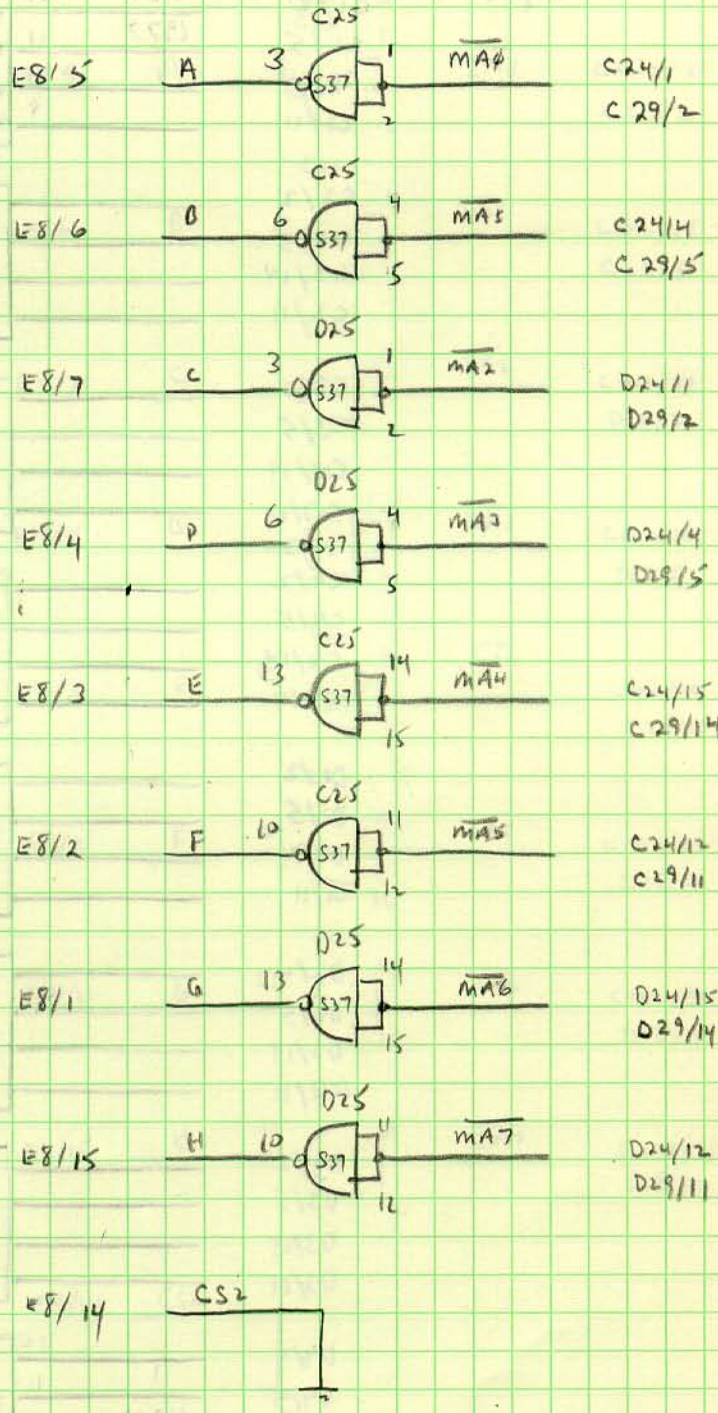
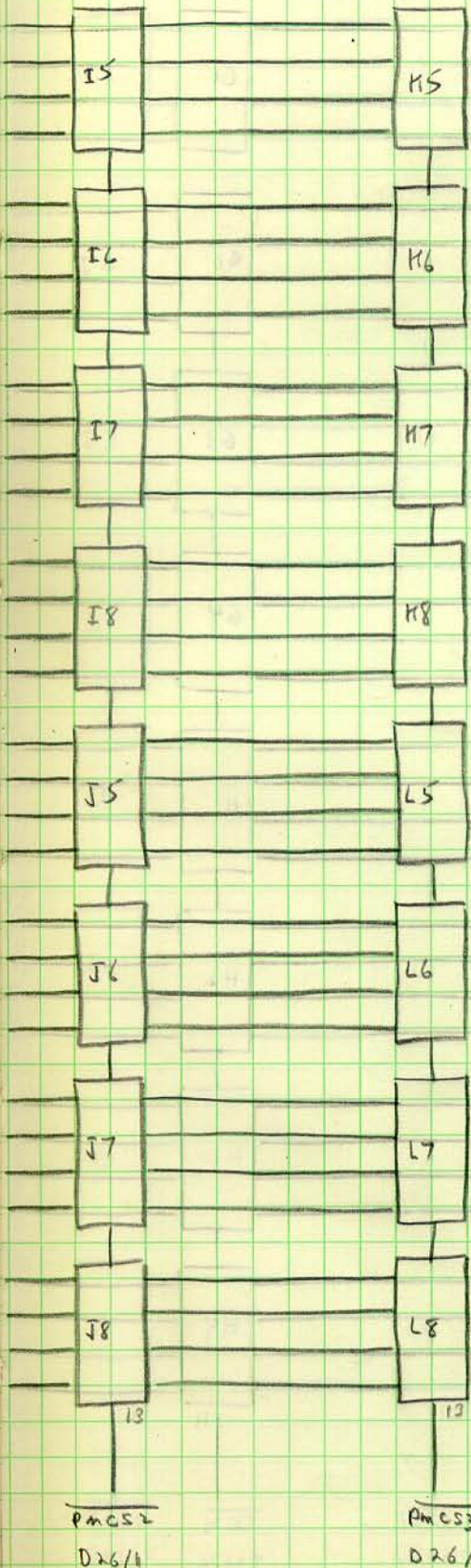
- D7/2
- D7/5
- D7/14
- D7/11

- D8/2
- D8/5
- D8/14
- D8/11



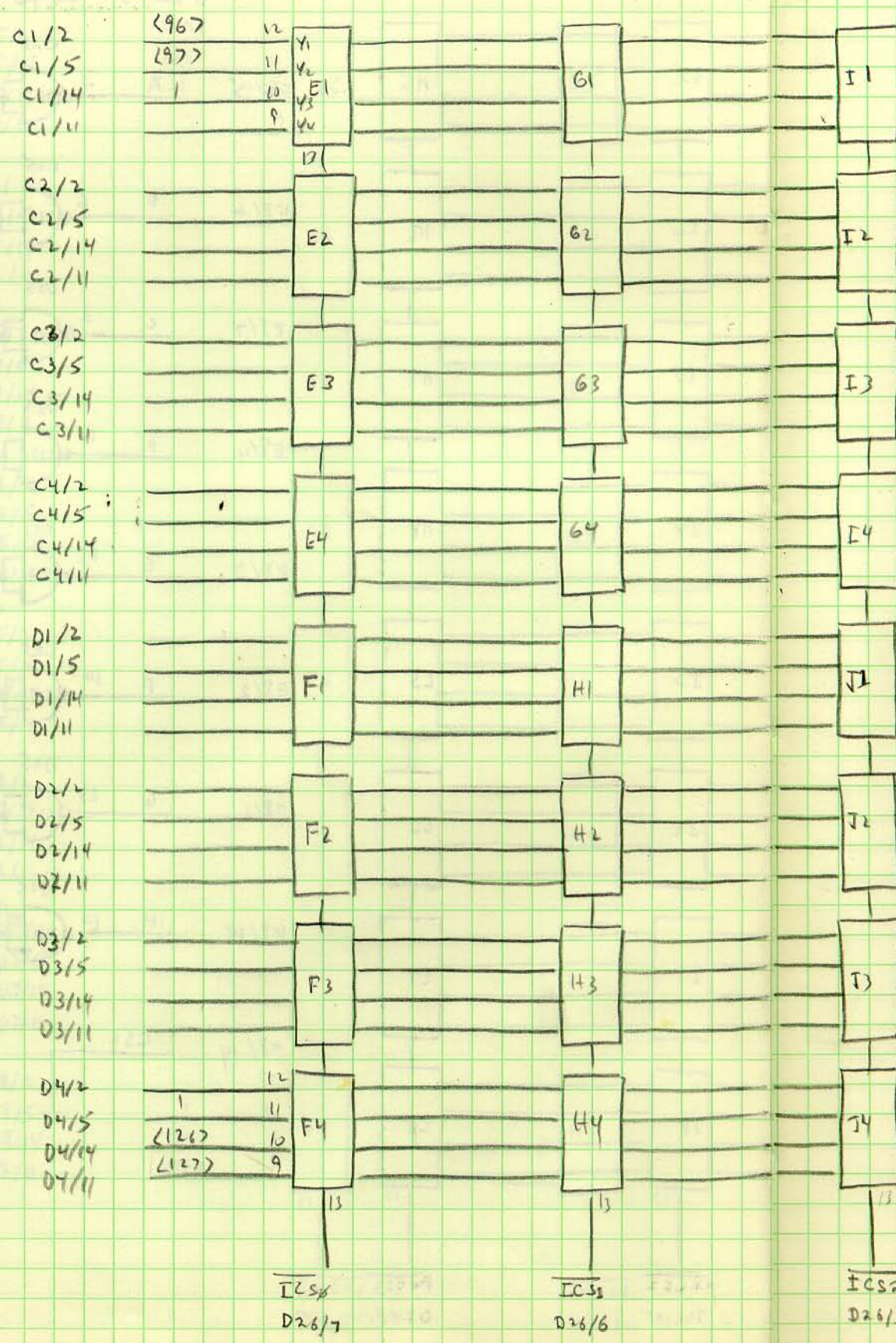
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INSTRUCTION MICROCODE

to All 32 chips ✓



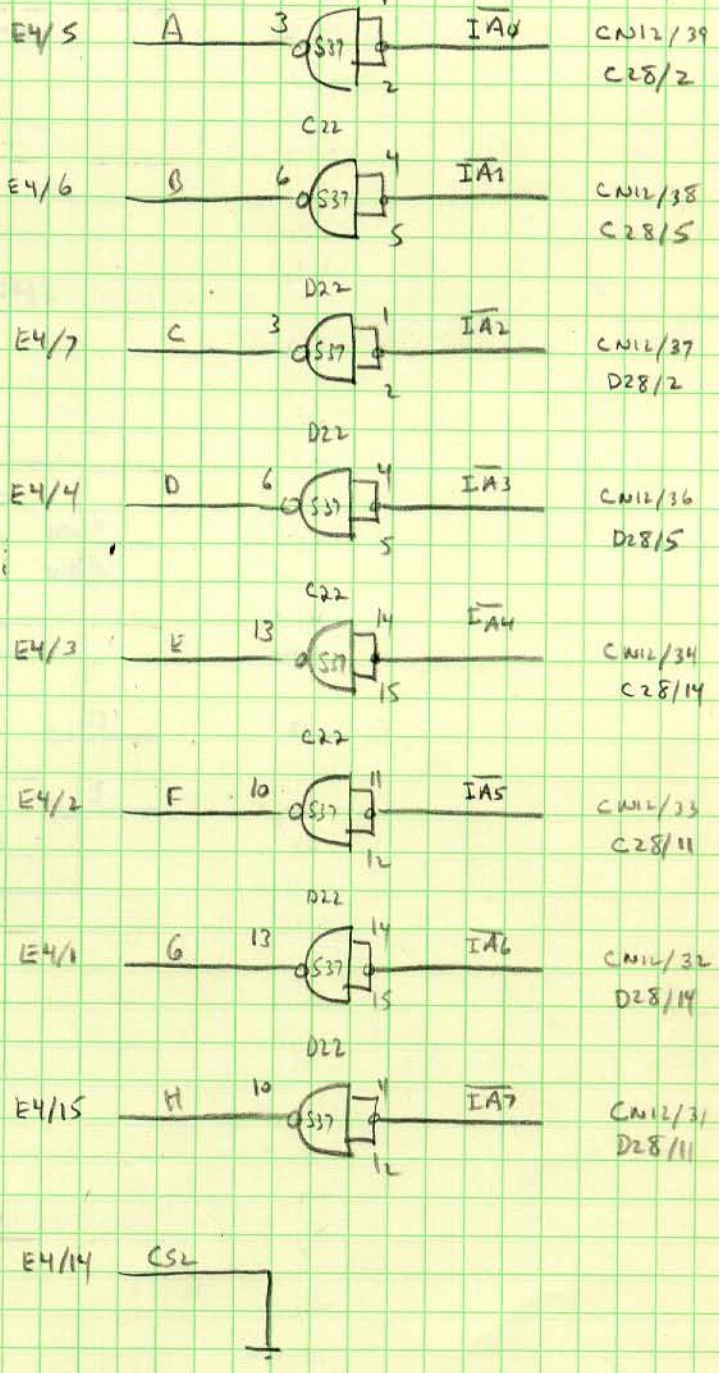
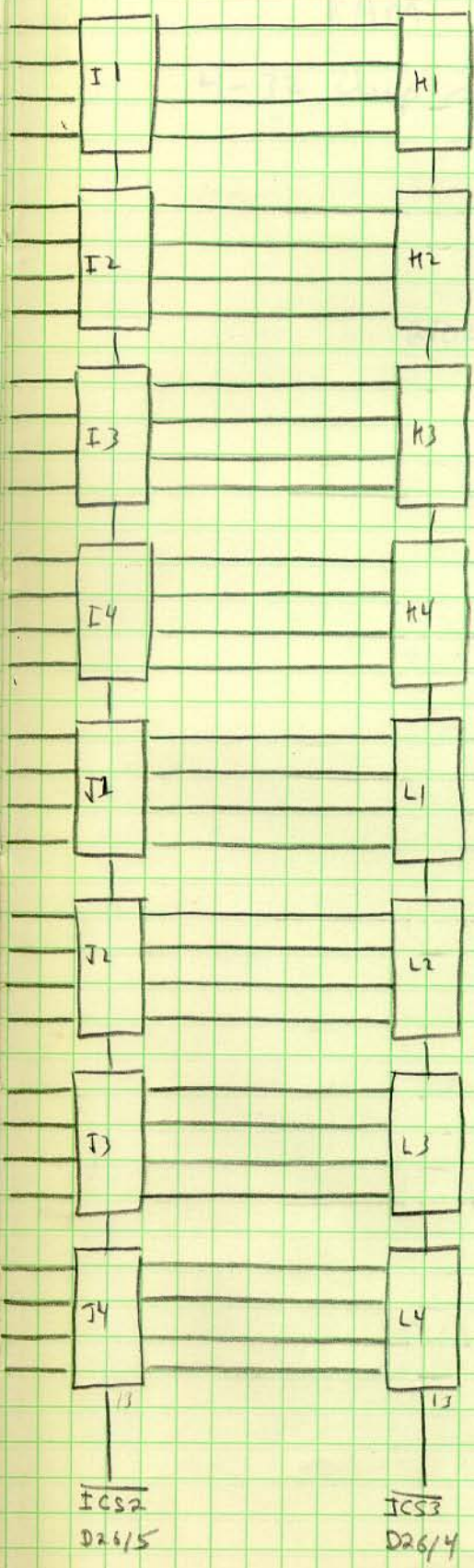
17 Dec 76
APB

74S387 PROMS
1Kx32



<96:127>
INSTRUCTION DECODE DATA

to All 32 chips



17 Dec 76
ARJ

Changed

RAM Microcode Memory Organization

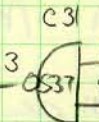
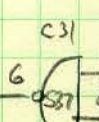
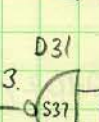
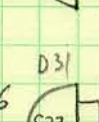
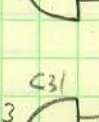
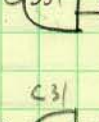
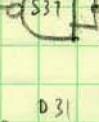
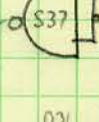
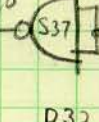
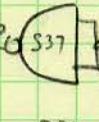
4-32 chip sections

2102 / 3542



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ARD

Address Lines

Bit	CHIP	DATA	DATA	DATA	DATA	DATA	DATA
0	E3L	C13/1	E32/8	A0		C30/2	32
1	E3I	C13/4					33
2	E3O	C13/15					34
3	E29	C13/12	E32/4	A1		C30/5	35
4	E28	C14/1					36
5	E27	C14/4					37
6	E26	C14/15	E32/5	A2		D30/2	38
7	E25	C14/12					39
8	E24	C15/1					40
9	E23	C15/4	E32/6	A3		D30/5	41
10	E22	C15/15					42
11	E21	C15/12					43
12	E20	C16/1	E32/7	A4		C30/14	44
13	E19	C16/4					45
14	E18	C16/15					46
15	E17	C16/12					47
16	F3L	D13/1	E32/2	A5		C30/11	48
17	F3I	D13/4					49
18	F3O	D13/15					50
19	F29	D13/12	E32/1	A6		D30/14	51
20	F28	D14/1					52
21	F27	D14/4					53
22	F26	D14/15	E32/16	A7		D30/11	54
23	F25	D14/12					55
24	F24	D15/1					56
25	F23	D15/4	E32/15	A8		D32/2	57
26	F22	D15/15					58
27	F21	D15/12					59
28	E20	D16/1	E32/14	A9		D32/14	60
29	F19	D16/4					61
30	F18	D16/15					62
31	F17	D16/12	E32/13		C5	C27/13	63

Address Drivers

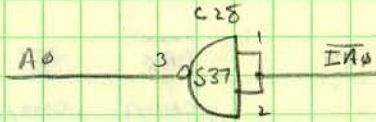
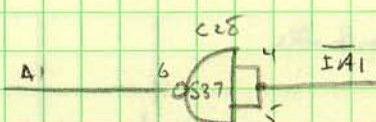
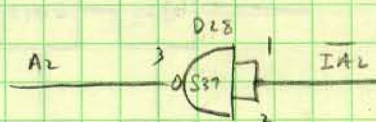
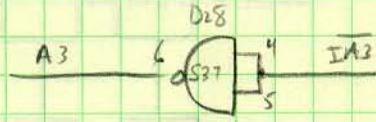
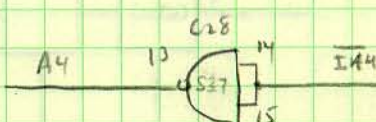
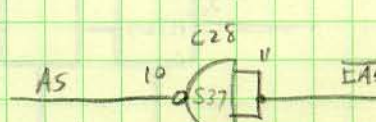
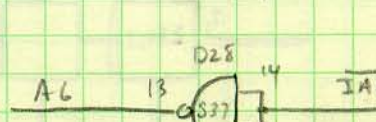
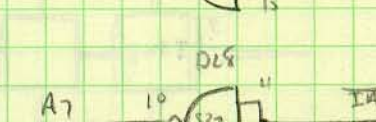
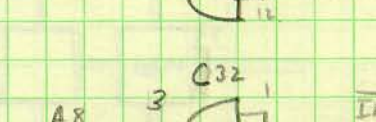
Changed ✓

Bit	CHIP	DMT (12) to			
32	G32	C9/11	G32/8	A0	C29/1 C31/2
33	G31	C9/14			
34	G34	C9/15			
35	G29	C9/12	G32/4	A1	C29/4 C31/5
36	G28	C10/11			
37	G27	C10/14			
38	G26	C10/15	G32/5	A2	D29/1 D31/2
39	G25	C10/12			
40	G24	C11/11			
41	G23	C11/14	G32/6	A3	D29/4 D31/5
42	G22	C11/15			
43	G21	C11/12			
44	G20	C12/11	G32/7	A4	C29/15 C31/14
45	G19	C12/14			
46	G18	C12/15			
47	G17	C12/12			
48	H32	D9/11	G32/2	A5	C29/12 C31/11
49	H31	D9/14			
50	H30	D9/15			
51	H29	D9/12	G32/11	A6	D29/15 D31/14
52	H28	D10/11			
53	H27	D10/14			
54	H26	D10/15	G32/16	A7	D29/12 D31/11
55	H25	D10/12			
56	H24	D11/11			
57	H23	D11/14	G32/15	A8	C32/5 D32/4
58	H22	D11/15			
59	H21	D11/12			
60	H20	D12/11	G32/14	A9	C32/11 D32/12
61	H19	D12/14			
62	H18	D12/15			
63	H17	D12/12	G32/13	CS	C27/10

17Da 76
APC

Address Drivers

RA	CHID	Port Crystal Pin	IC	Pin	IC Pin	Output	IC Pin	IC Pin	RA
64	I32	C5/1	I32/8	A0	3	$\overline{MA0}$	C29	C24/2 C30/1	96
65	I31	C5/4							97
66	I30	C5/15							98
67	I29	C5/12	I32/4	A1	6	$\overline{MA1}$	C29	C24/5 C30/4	99
68	I28	C6/1							100
69	I27	C6/4							101
70	I26	C6/15	I32/5	A2	3	$\overline{MA2}$	D29	D24/2 D30/1	102
71	I25	C6/12							103
72	I24	C7/1							104
73	I23	C7/4	I32/6	A3	6	$\overline{MA3}$	D29	D24/5 D30/4	105
74	I22	C7/15							106
75	I21	C7/12							107
76	I20	C8/1	I32/7	A4	13	$\overline{MA4}$	C29	C24/14 C30/15	108
77	I19	C8/4							109
78	I18	C8/15							110
79	I17	C8/12							111
80	I3-	D5/1	I32/2	A5	10	$\overline{MA5}$	C29	C24/11 C30/12	112
81	J31	D5/4							113
82	J30	D5/15							114
83	J29	D5/12	I32/1	A6	13	$\overline{MA6}$	D29	D24/14 D30/15	115
84	J28	D6/1							116
85	J27	D6/4							117
86	J26	D6/15	I32/16	A7	10	$\overline{MA7}$	D29	C24/11 D30/12	118
87	J25	D6/12							119
88	J24	D7/1							120
89	J23	D7/4	I32/15	A8	6	$\overline{MA8}$	C32	C32/11 D32/1	121
90	J22	D7/15							122
91	J21	D7/12							123
92	J20	D8/1	I32/14	A9	10	$\overline{MA9}$	C32	C32/12 D32/15	124
93	J19	D8/4							125
94	J18	D8/15							126
95	J17	D8/12	I32/13			$\overline{MC5}$		D27/10	127

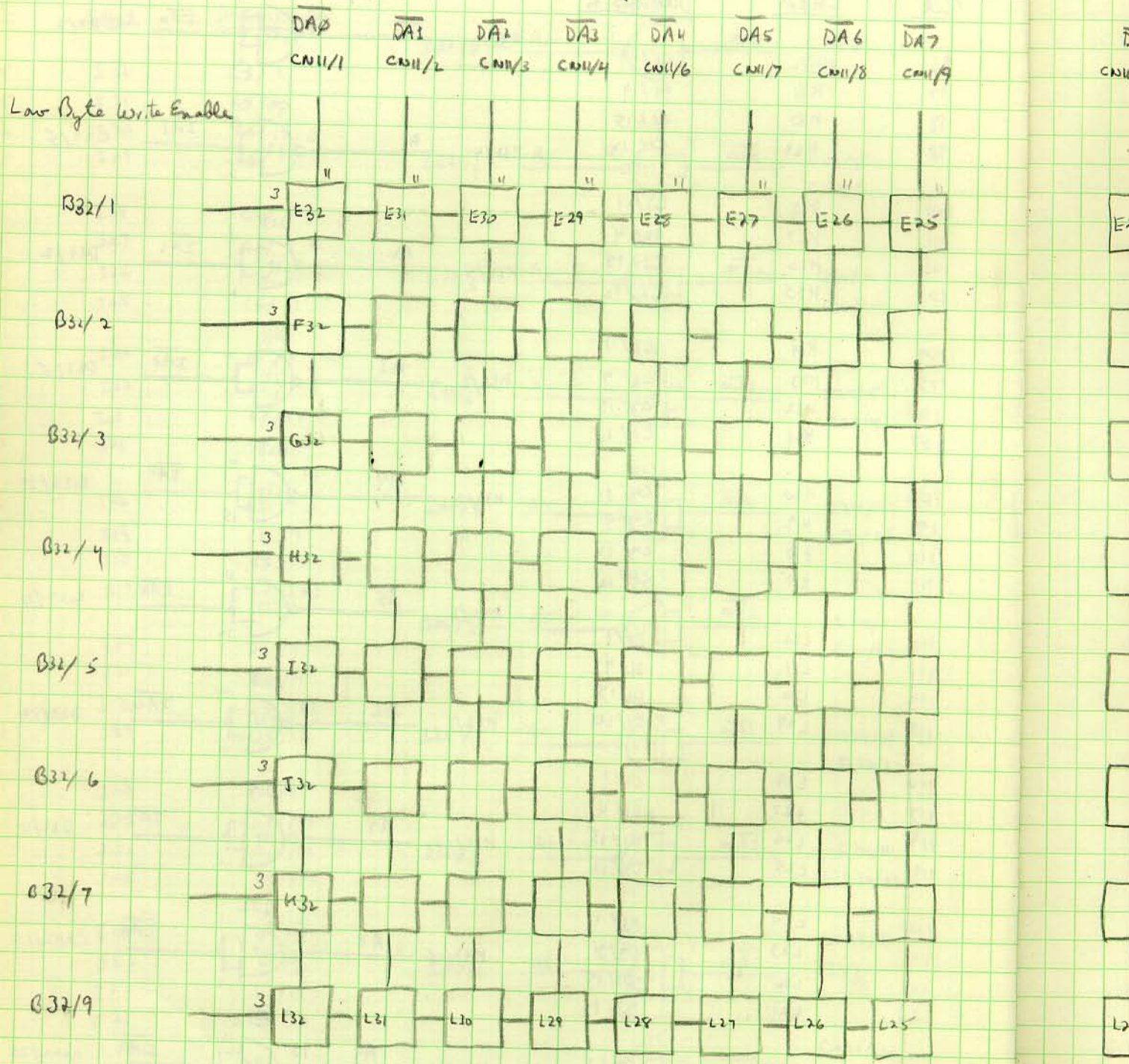
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97	K31	C1/4				
98	K30	C1/15				
99	K29	C1/12	K32/4	A1		C22/5
100	K28	C2/1				
101	K27	C2/4				
102	K26	C2/15				
103	K25	C2/12	K32/5	A2		D22/2
104	K24	C3/1				
105	K23	C3/4				
106	K22	C3/15				
107	K21	C3/12	K32/6	A3		D22/5
108	K20	C4/1				
109	K19	C4/4				
110	K18	C4/15				
111	K17	C4/12	K32/7	A4		C22/14
112	L32	D1/1				
113	L31	D1/4				
114	L30	D1/15				
115	L29	D1/12	K32/1	A5		C22/11
116	L28	D2/1				
117	L27	D2/4				
118	L26	D2/15				
119	L25	D2/12	K32/16	A7		D22/11
120	L24	D3/1				
121	L23	D3/4				
122	L22	D3/15				
123	L21	D3/12	K32/15	A8		CN12/29
124	L20	D4/1				
125	L19	D4/4				
126	L18	D4/15				
127	L17	D4/12	K32/14	A9		CN12/28
			K32/13	IC5		D22/6

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ARR

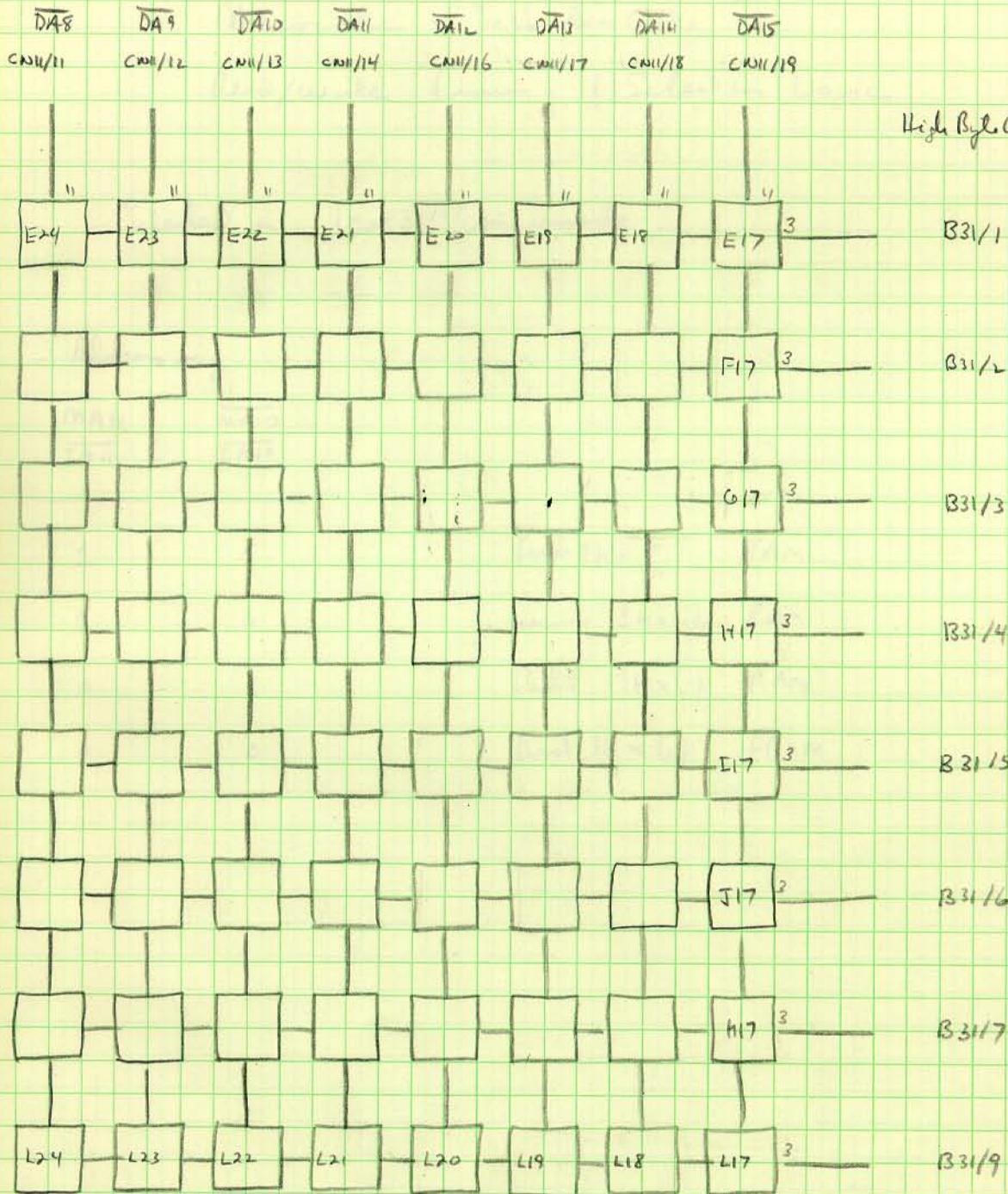
RAM Data & Write Selection for 1Kx128 RAM Section

Low Byte



High Byte

High Byte Write Enable



19 Dec 1976

ABC

Microcode & Instruction Code

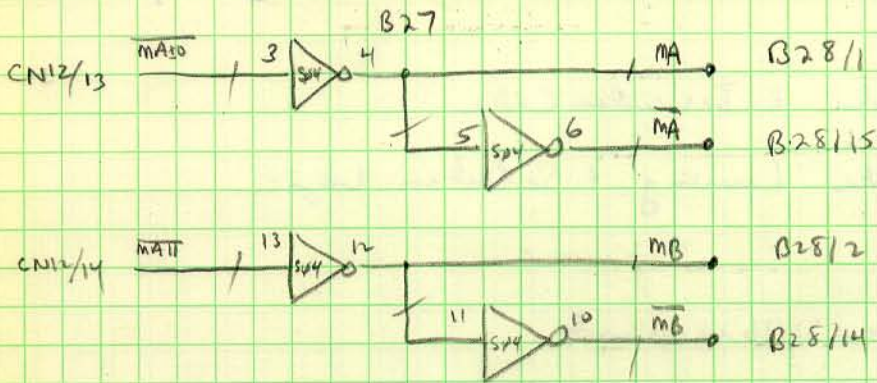
Read/write timing & Selection Logic

Selected in 1Kx 32/96 increments

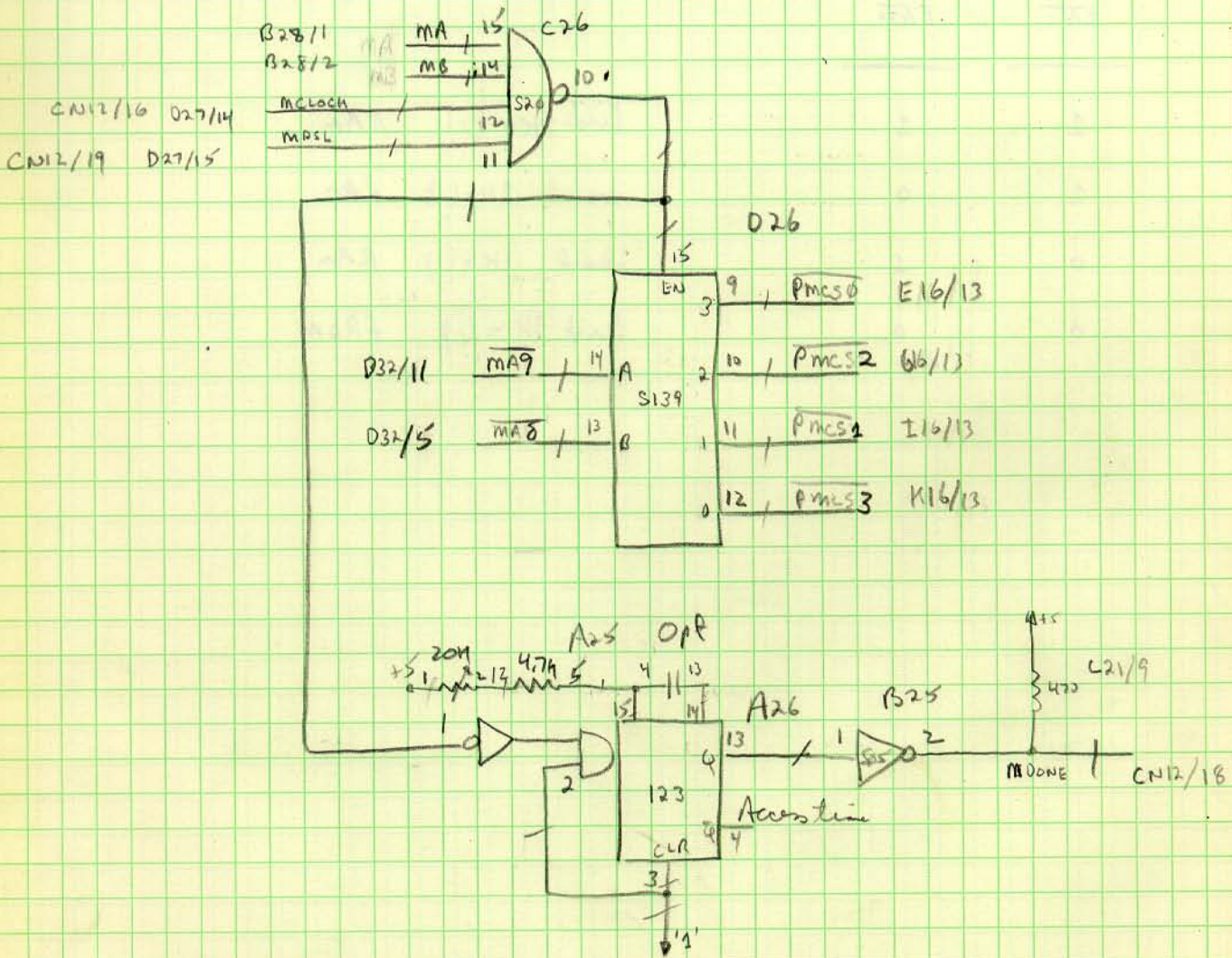
Addressing

$\overline{MA11}$	$\overline{MA10}$	
$\overline{IA11}$	$\overline{IA10}$	
1	1	first 1Kx (1) RAM
1	0	second 1Kx (1) RAM
0	1	third 1Kx (1) RAM
0	0	first 1Kx (1) PROM

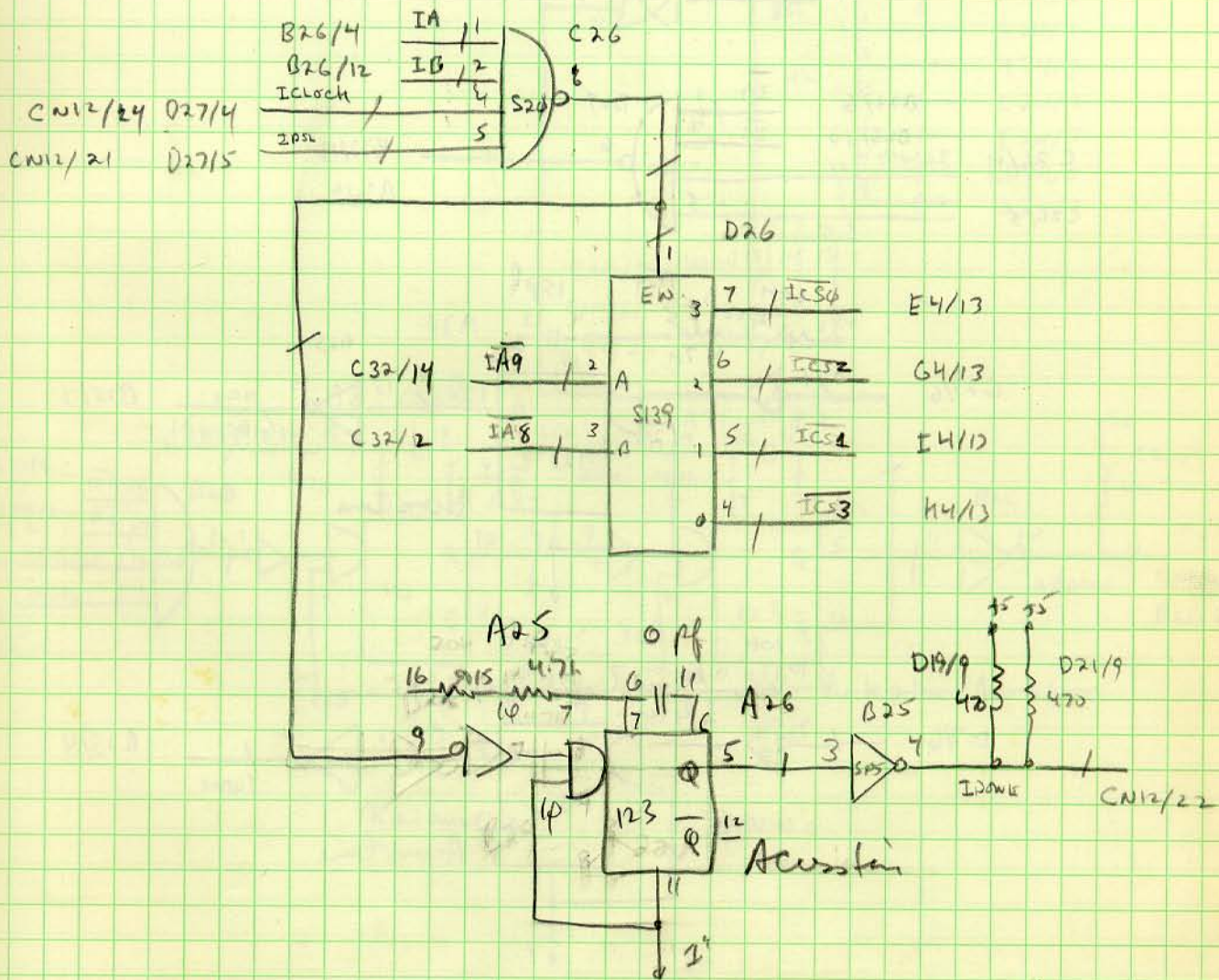
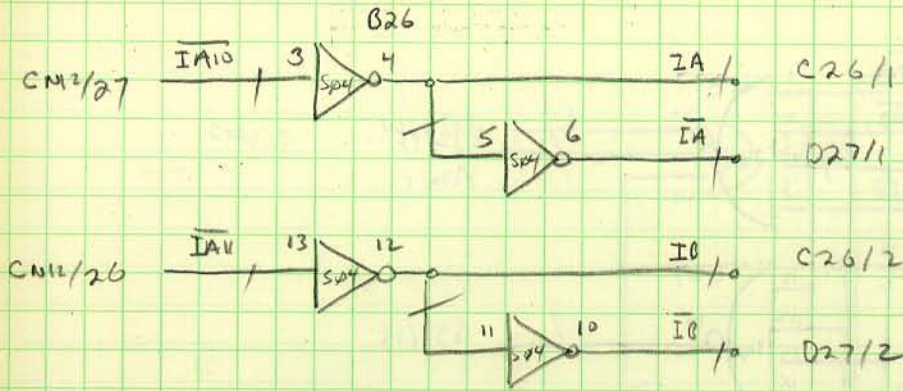
Microcode Selector Buffers



PROM Decoding

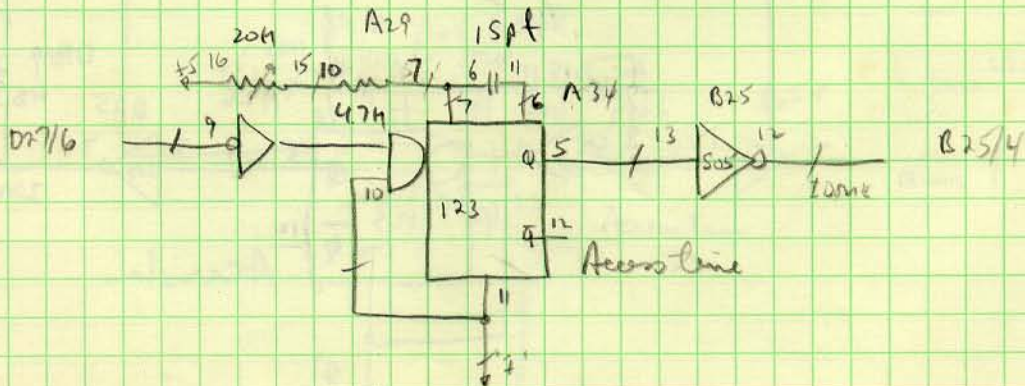
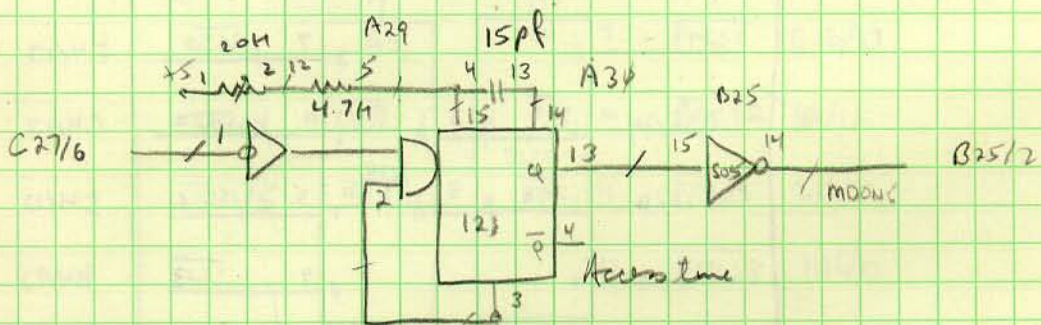
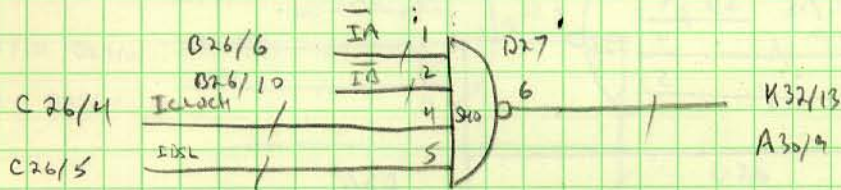
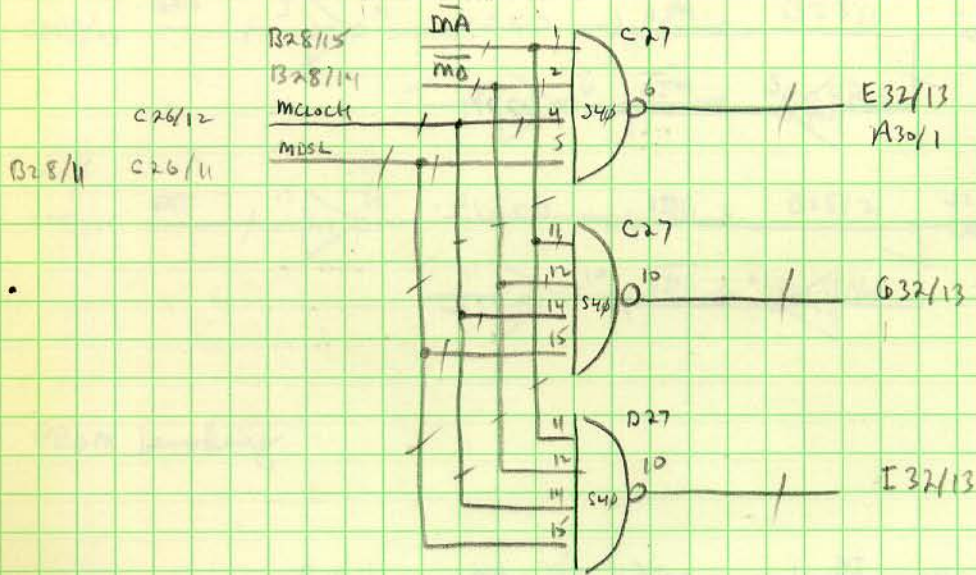


Changed



19 Dec 76
ARS

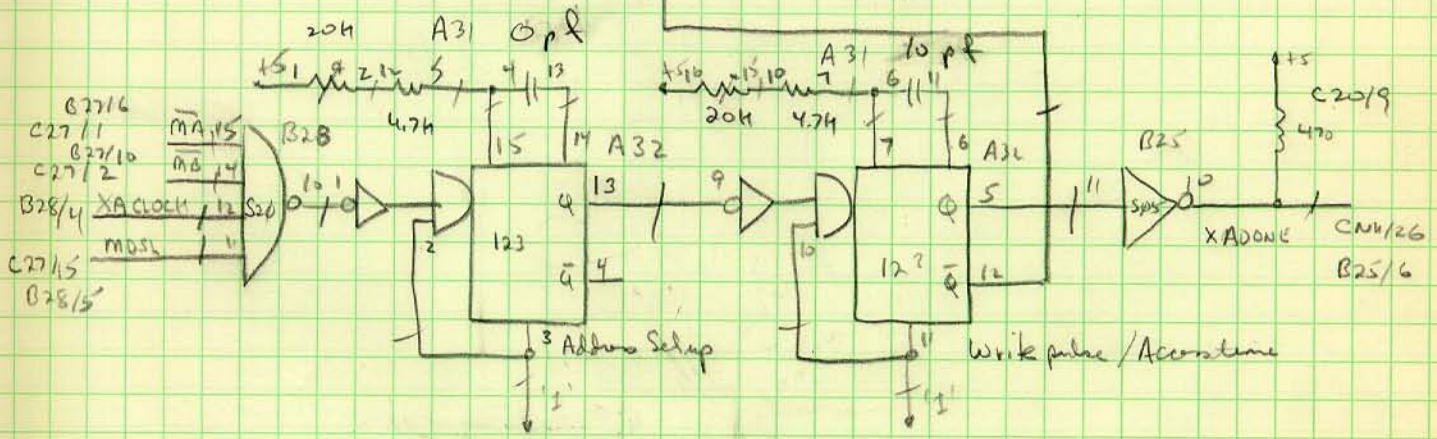
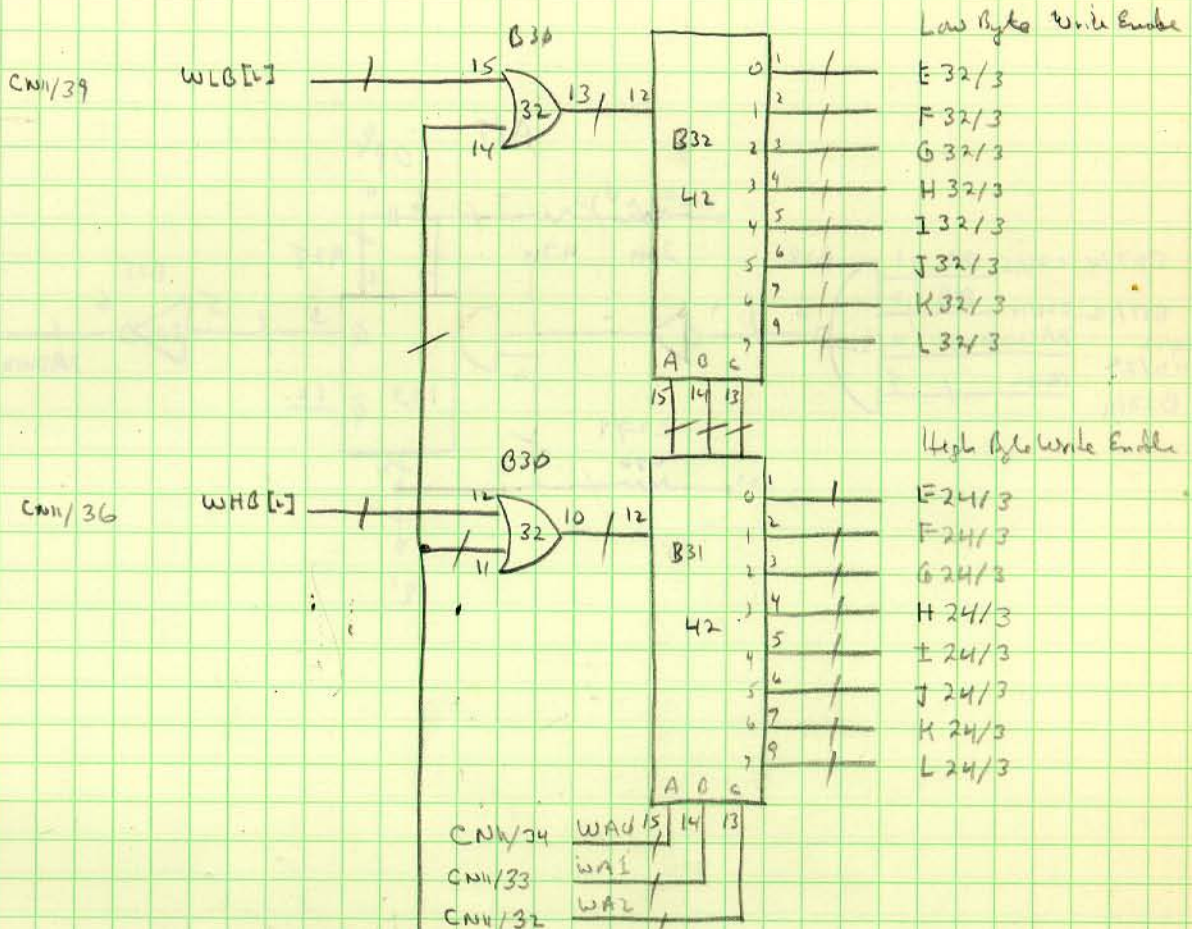
RAM Selects



B27/6
 C27/11
 B27/10
 C27/2
 B28/4
 C27/15
 B28/15

RAM Write Selection

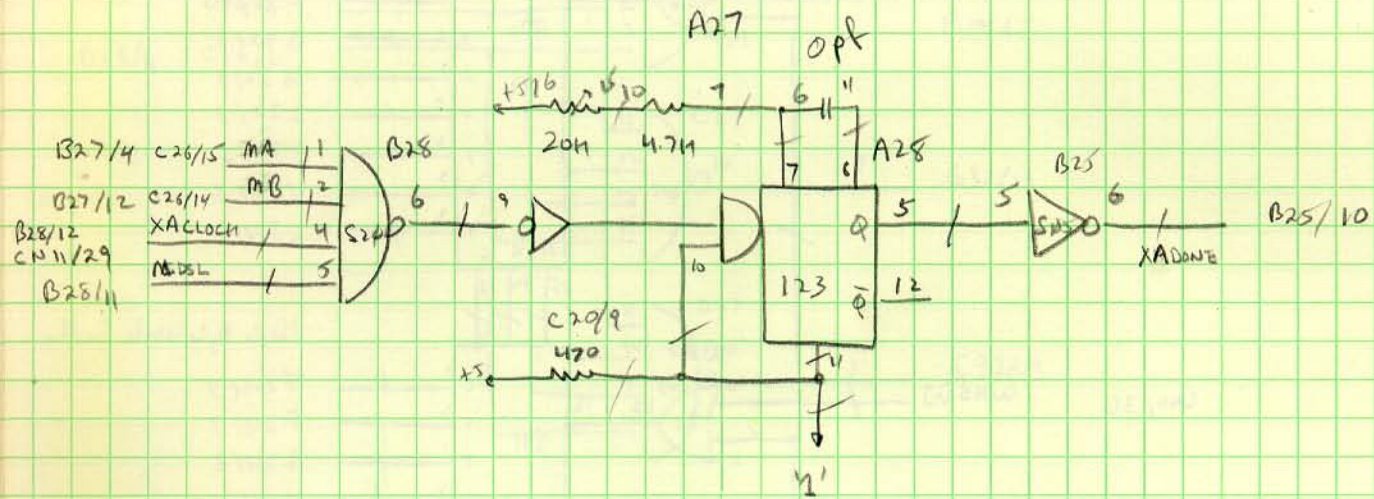
Changed



Minimum

200 ns

Prom Access



changed

25

16 K Memory Panel (Frame #7)

Read/Write organization 16Kx16

using 1Kx1 RAMs - AM 9102D 250 ns Max Access

Miscellaneous #2
RAM

28 Jan 77
ARB

Board #1

1/xx/xx

A B C

X	A1	A1	A2	A2	A3	A3	LB	HB	A4	A4	A5	A5	X	WEN	(11:147) CS
	S37	S87	S37	S37	S37	S37	S4A	S40	S37	S37	S37	S37		34	42
(0)	(1)	(2)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)	(13)	(14)	(15)	(16)

All unmarked IC's are 2102 type RAMs

Board #3

3/xx/xx

Board # 3

3/xx/xx

						1
						2
						3
						4
						5
						6
						7
						8
						9
						10
						11
						12
						13
						14
						15
						16

G

H

I

J

K

L

28 Jun 77
APD

Board #2
2/xx/xx

A	1	Address	2	Data	ADD <19:21> 86	ADD <19:21> 86	ADD <19:21> 86	ADD Selector	Cap 470	Write Timing	Mem Timing	one shots 123	X
B	3	Address	4	Data	ADD Puck <11:14> 04	ADD Puck <11:14> 04	Write Encoding 04	Select Decoding 34	DCDH Driver 537	one shots 123	Drivers 38	one shots 74	X
C		A <1:14> BUF 537		DO <6:15> 8797	DO <6:17> 8797	DO <12:19> 8797	DI <4:7> BUF 537	DI <8:11> BUF 537	DI <12:15> BUF 537	X	X	X	X
D		A <5:8> BUF 537		A6 537	A7 537	A7 537	A8 537	A8 537	A9 537	A9 537	A10 537	A10 537	X
E		A <1:14> CS 412		A6 537	A7 537	A7 537	A8 537	A8 537	A9 537	A9 537	A10 537	A10 537	X
F		A <1:14> CS 412		A6 537	A7 537	A7 537	A8 537	A8 537	A9 537	A9 537	A10 537	A10 537	X

all unmarked IC's are 2102 type RAMs

Board #4
4/xx/xx

Board #4
4/12/XX

						32
						31
						30
						29
						28
						27
						26
						25
						24
						23
						22
						21
						20
						19
						18
						17
G	H	I	J	K	L	

28Jan
ARD

Connector Wiring Board #2 (Frame #7)

#1 & #3 Internal Address Plus Control

1	$\overline{IA0}$	+	B26/15	40	GND	
2	$\overline{IA1}$	+	C17/1	39	$\overline{IA16}$	+ A25/4
3	$\overline{IA2}$	+	C17/4	38	$\overline{IA17}$	+ A25/15
4	$\overline{IA3}$	+	C17/15	37	$\overline{IA18}$	+ A25/12
5	GND			36	$\overline{IA19}$	+ A26/1
6		7	C17/12	35	GND	
7		+	C18/1	34	$\overline{IA20}$	+ A26/4
8		+	C18/4	33	$\overline{IA21}$	+ A26/15
9		+	C18/15	32	$\overline{IC0D}$	+ B28/1
10	GND			31	$\overline{IC1D}$	+ B28/15
11		+	C18/12	30	GND	
12		+	C19/1	29	IXMSYNH	+ B27/14
13		+	C19/4	28		
14		+	B25/1	27	ISSYNL	+ B30/3
15	GND			26	UBSYNL	+ B30/13
16	$\overline{IA12}$	+	B25/3	25	GND	
17	$\overline{IA13}$	+	B25/5	24	IMSYNH	-
18	$\overline{IA14}$	+	B25/15	23		
19	$\overline{IA15}$	+	A25/1	22		
20	GND			21	INIT CLEAR H	-

#2 & #4 DATA BUS

1	DI0	+	C21/3	40	GND	
2	DI1	+	C21/6	39	$\overline{DO0}$	+ C25/1
3		+	C21/13	38	$\overline{DO1}$	+ C25/4
4		+	C21/14	37		+ C25/15
5	GND			36		+ C25/12
6		+	C22/3	35	GND	
7		+	C22/6	34		+ C26/1
8		+	C22/13	33		+ C26/4
9		+	C22/14	32		+ C26/15
10	GND			31		+ C26/12
11		+	C23/3	30	GND	
12		+	C23/6	29		+ C27/1
13		+	C23/13	28		+ C27/4
14		+	C23/14	27		+ C27/15
15	GND			26		+ C27/12
16		+	C24/3	25	GND	
17		+	C24/6	24		+ C28/1
18		+	C24/13	23		+ C28/4
19	DI15	+	C24/14	22		+ C28/15
20	GND			21	$\overline{DO15}$	+ C28/12

Memory Address Selection

The seven (7) switch address selector may be used to locate the 16K memory panel at any 16K memory block in addressable memory. Memory addressing starts at address 0 to a 2 megawords. UNIBUS addresses are defined as the top most 128K words. Coding for each bit of the address is switch off for bit High and switch on for bit low

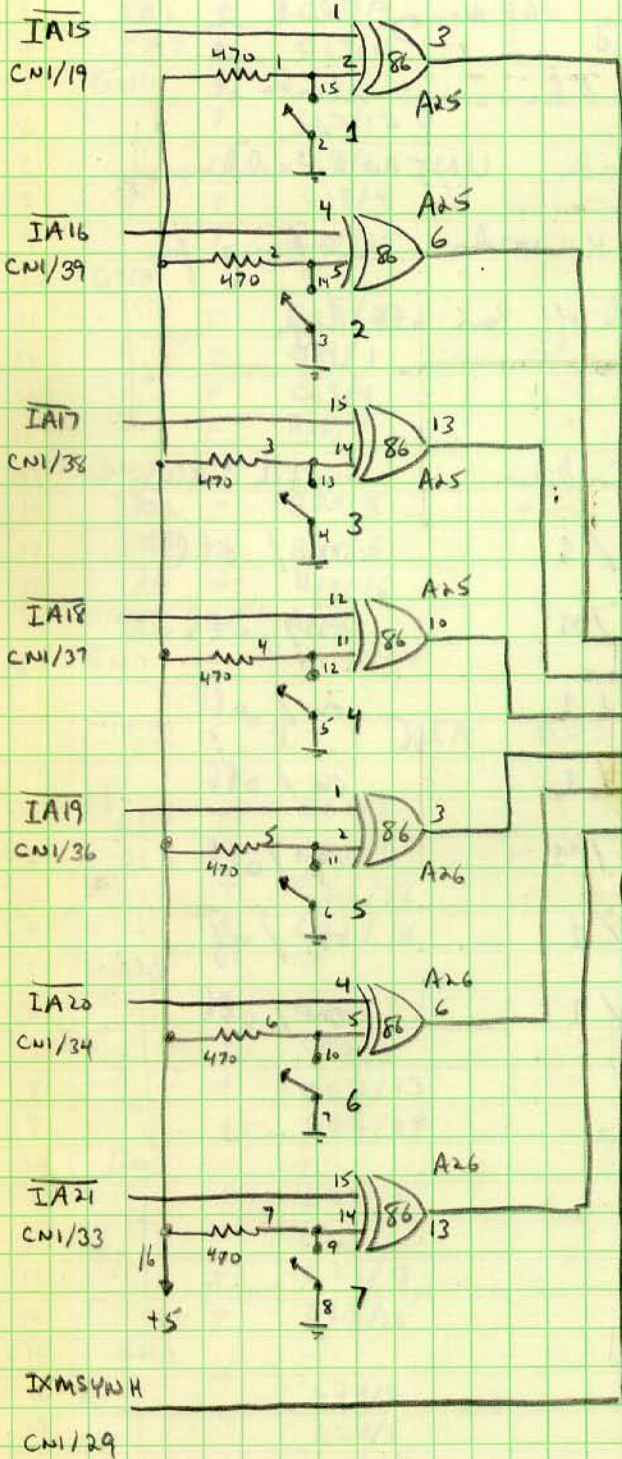
Switch	Bit Controlled	Bit Condition	Switch Setting
1	A15	0 / 1	ON / off
2	A16	0 / 1	ON / off
3	A17	0 / 1	on / off
4	A18	0 / 1	on / off
5	A19	0 / 1	on / off
6	A20	0 / 1	on / off
7	A21	0 / 1	on / off

For the first 16K of UNIBUS space

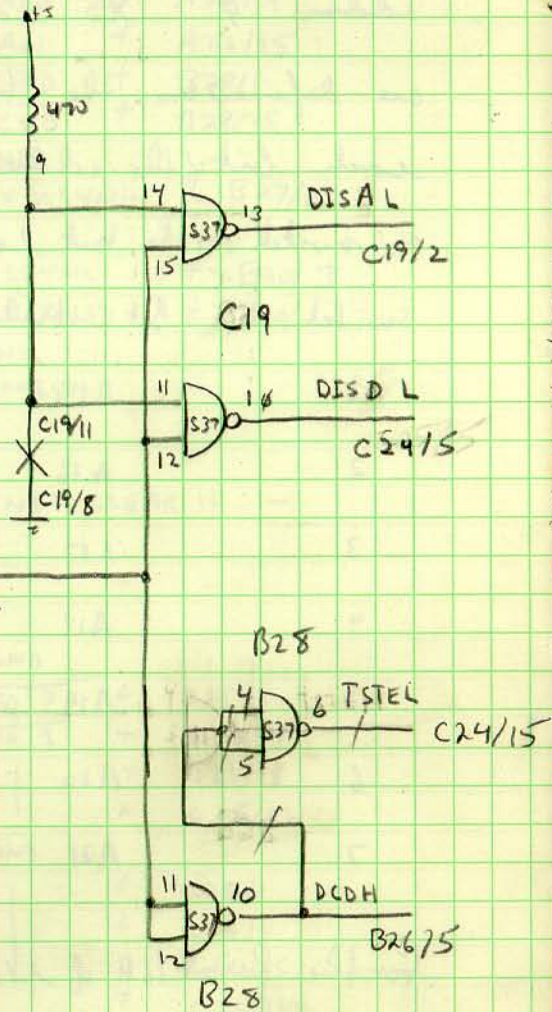
- 1 ON
- 2 ON
- 3 ON
- 4 ON
- 5 ON
- 6 ON
- 7 ON

28 Jan 77
APB

16K Read/Write Select Decoding



Remove jumper to disable Address & Data Buffers until board selection



Switches at A27

Resistors at A28

IA14

CN1/

IA13

CN1/

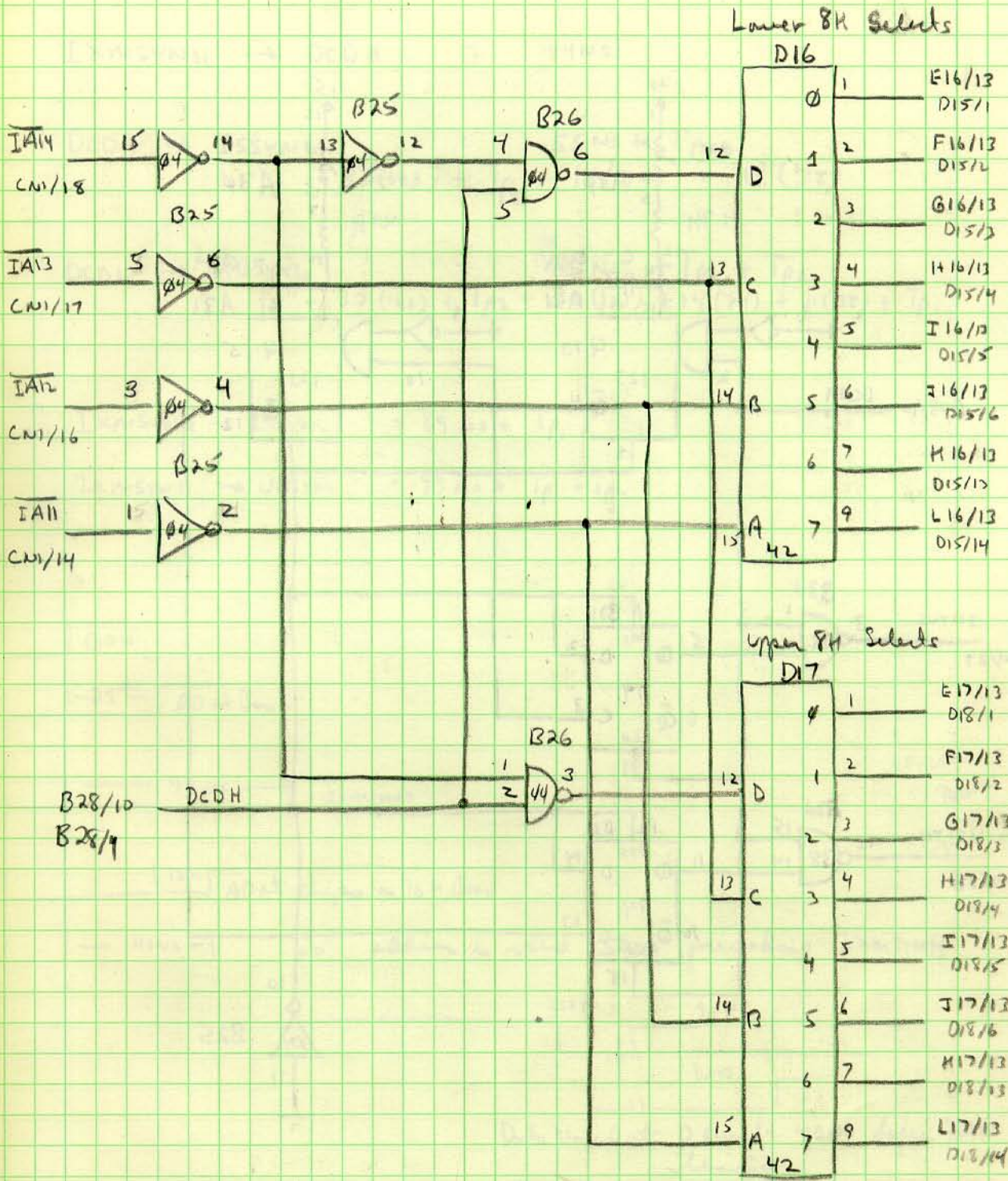
IA12

CN1/

IA11

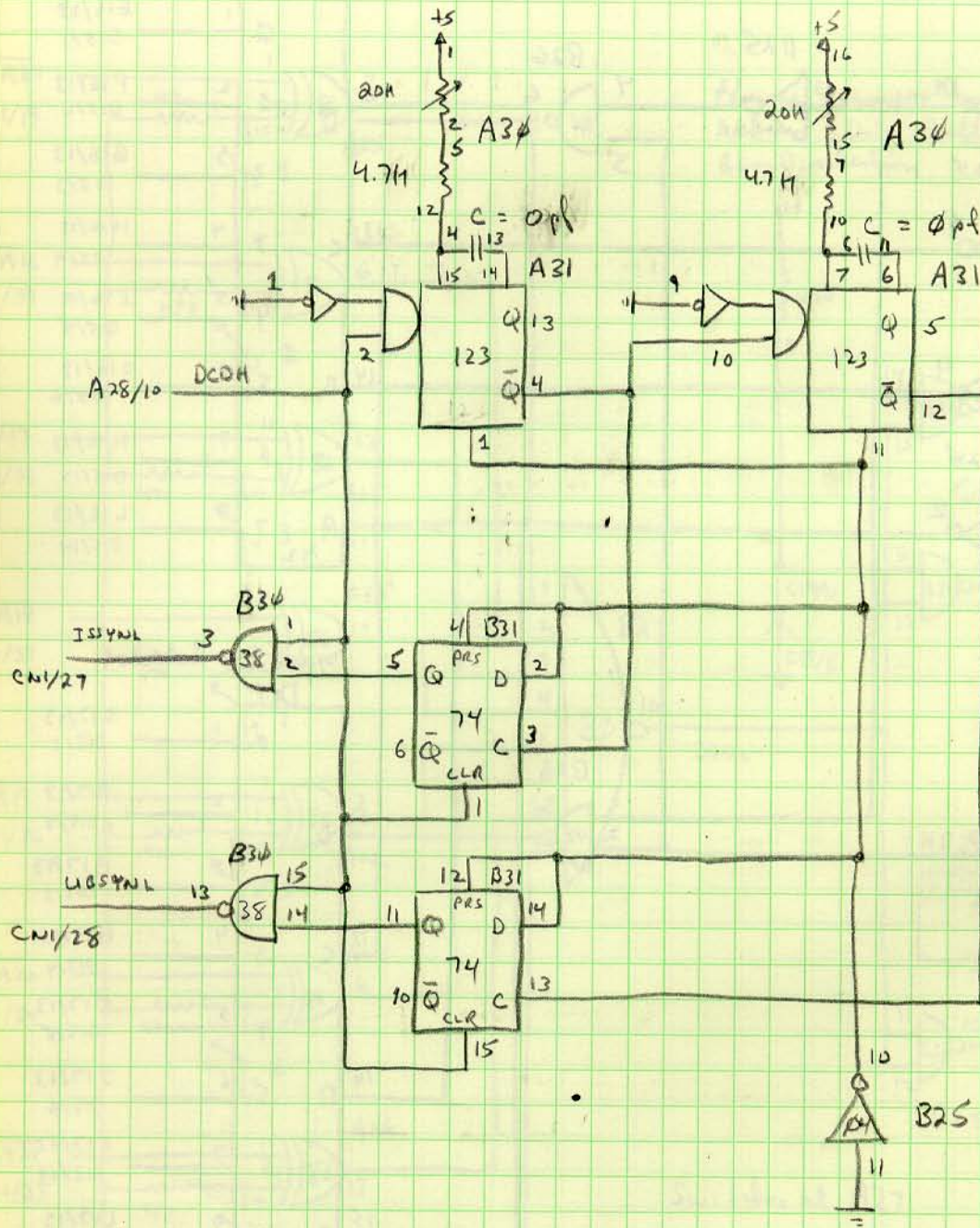
CN1/

1K Chip Select Decoder



28 Jan 77
ARR

Read/write Access Timing



Decoding timing

$$IXMSYNH \rightarrow DCDH = 14NS$$

$$DCDH \rightarrow ISSYNL = 55NS + T_p$$

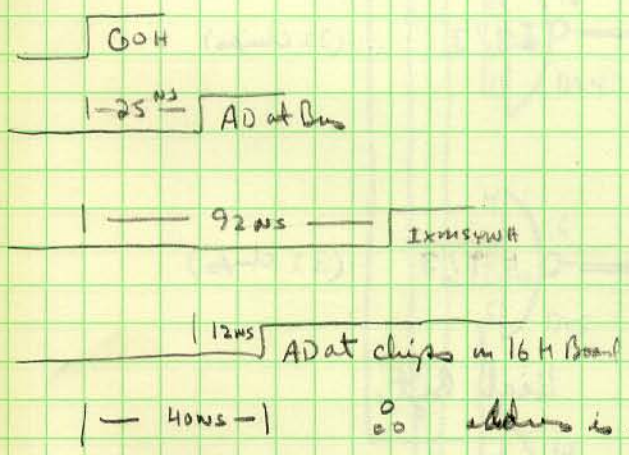
$$30(123) + T_{p1} + 14(74) + 11(38)$$

$$DCDH \rightarrow UBSYNL = 85NS + T_{p1} + T_{p2}$$

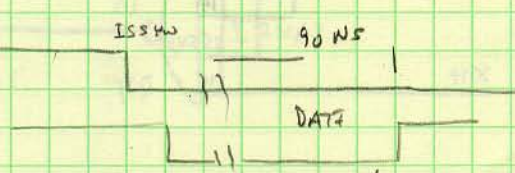
$$30(123) + T_{p1} + 30(123) + 14(74) + 11(38) + T_{p2}$$

$$\circ \circ IXMSYNH \rightarrow ISSYNL = 69NS + T_{p1}$$

$$IXMSYNH \rightarrow UBSYNL = 99NS + T_{p1} + T_{p2}$$



40+150 40+100
 300 data chips
 340
 2557 - 250



Data Valid at D output 40NS before DATA timing

allow 40NS

ISSYN should be set 40NS before memory time end

for ISSYN (Tacc = 250NS)

$$\circ \circ 250NS = 30NS + 40NS + 69 + T_{p1}$$

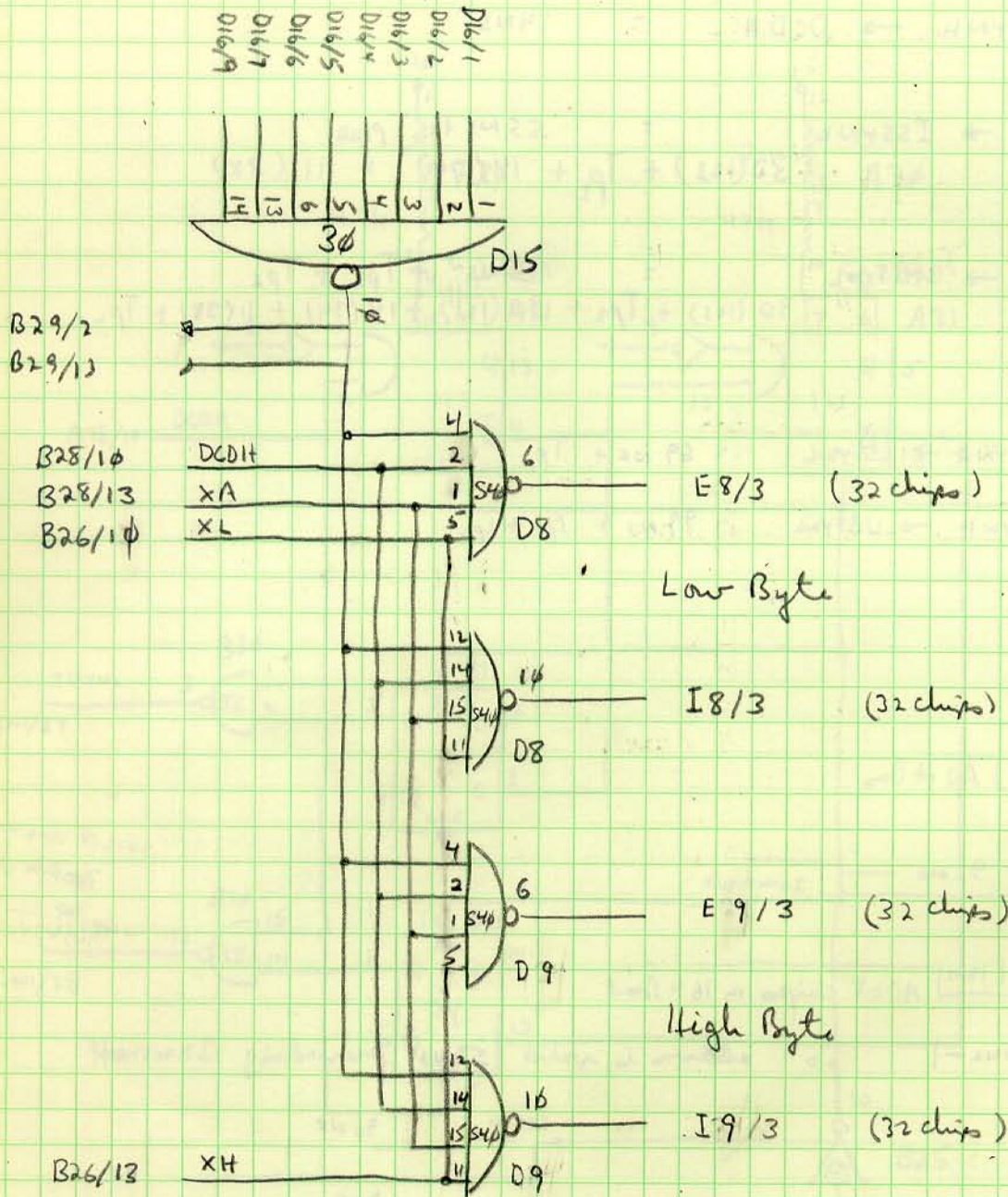
$$\circ \circ T_{p1} \approx 100NS$$

$$T_{p2} \approx 30NS$$

28 Jan 77
 ARB

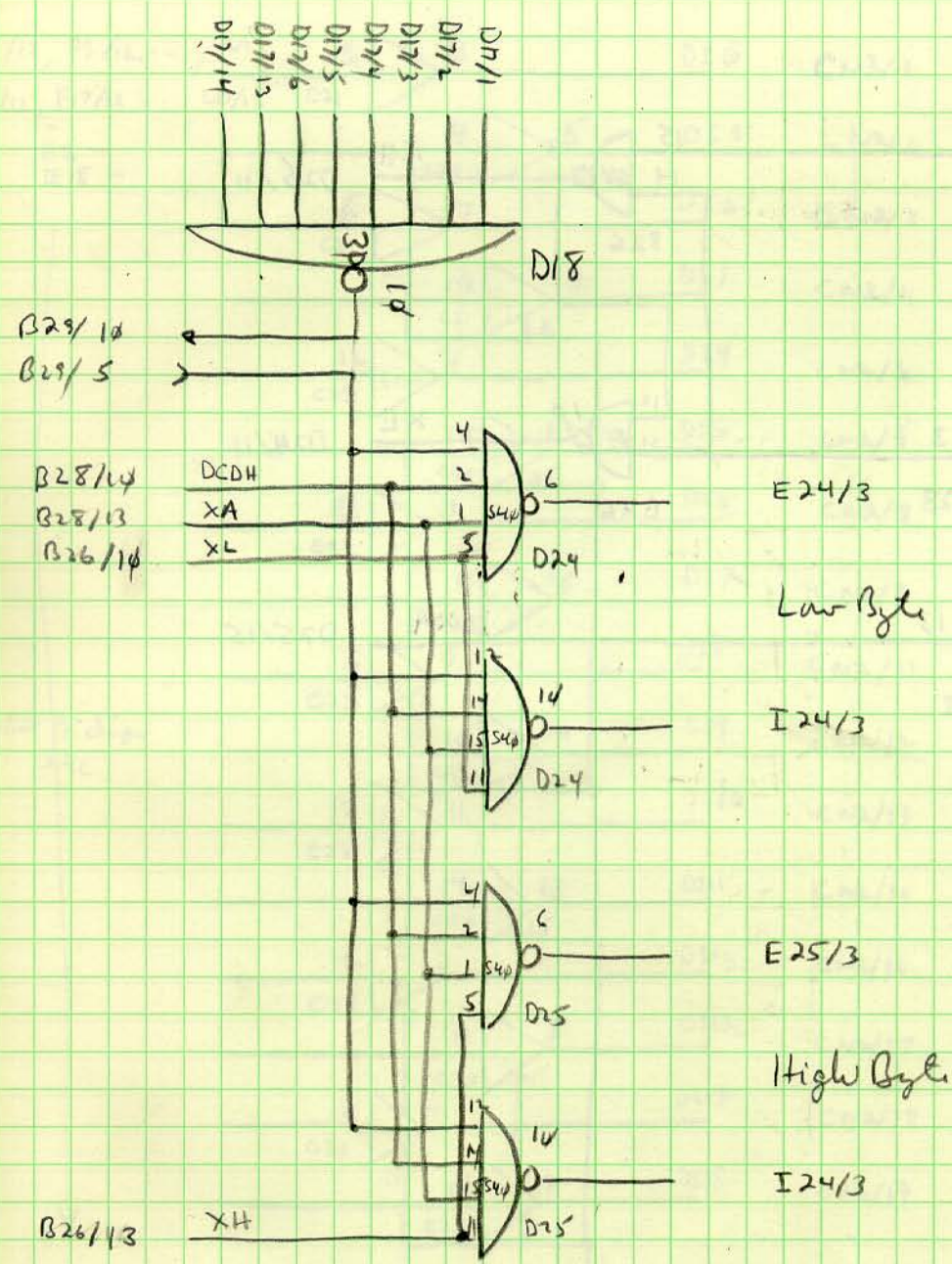
Read / Write Enable Logic

Low 8K



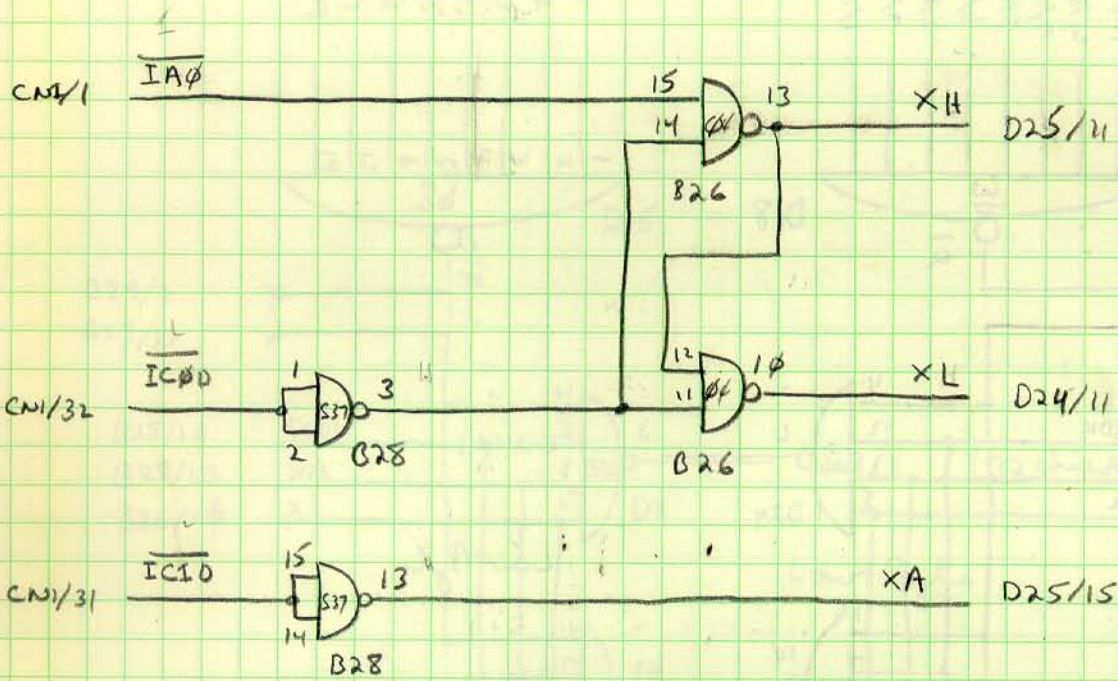
Read/Write Enable Logic

Upper 8M



28 Jan 77
ARB

Read/Write Decoding & Byte select



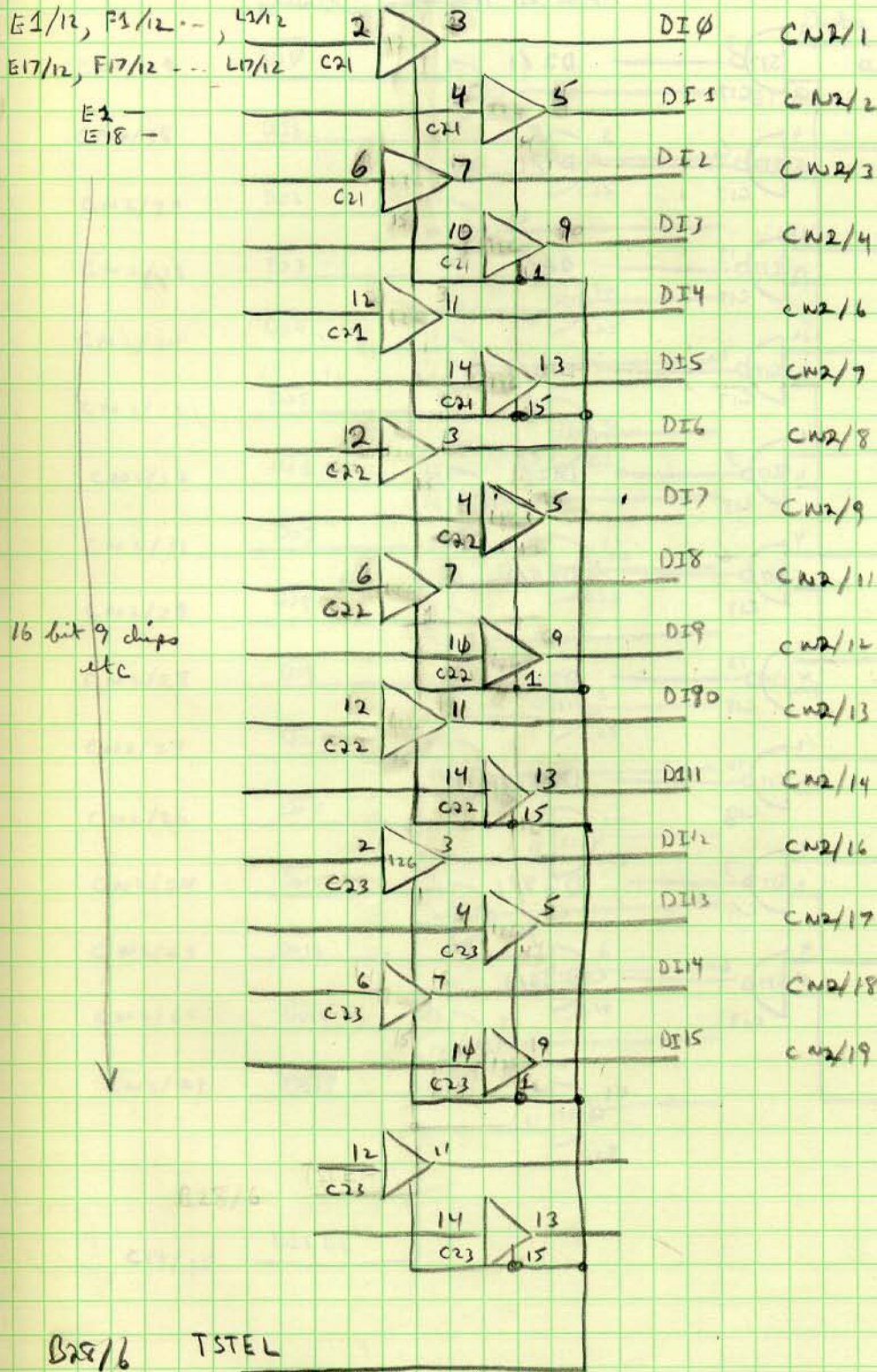
E1/12, F
E17/12, F
E2
E1

16 bit 9
at

B28/

Tristate Output Drivers

all 8T97B



16 bit data bus
etc

B28/6 TSTEL

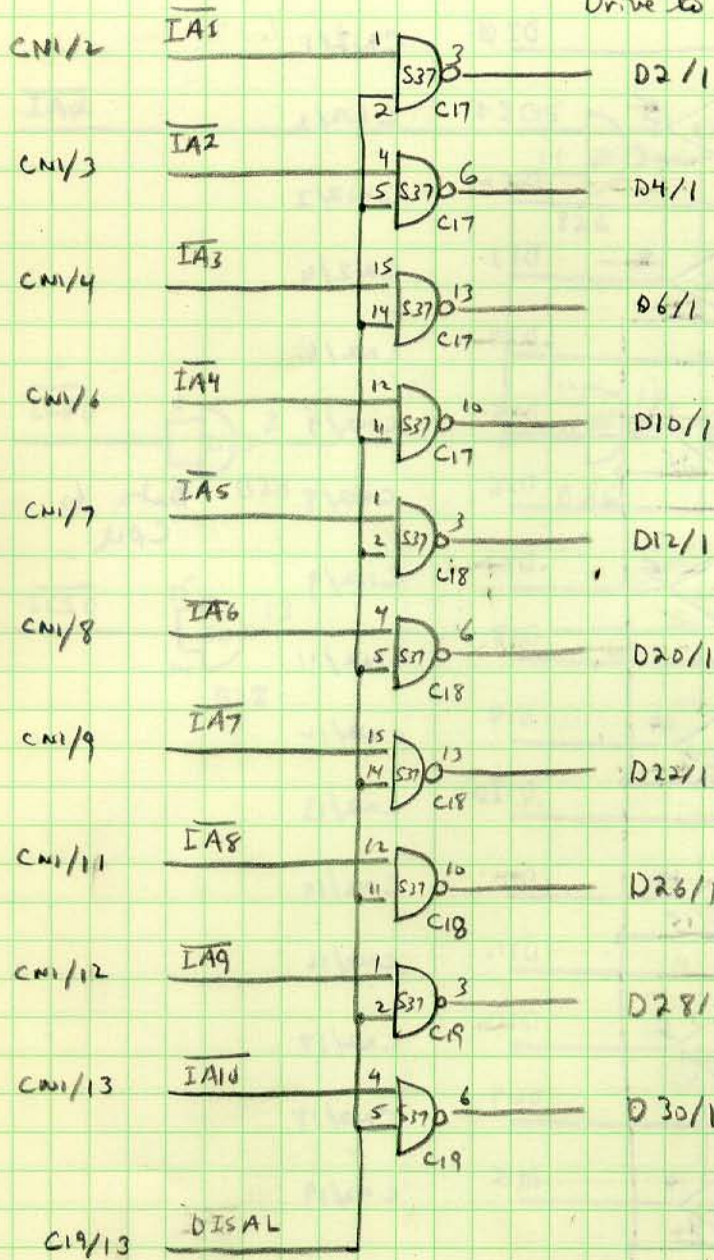
12 June 77

28 June 77

ARB

Address Buffers

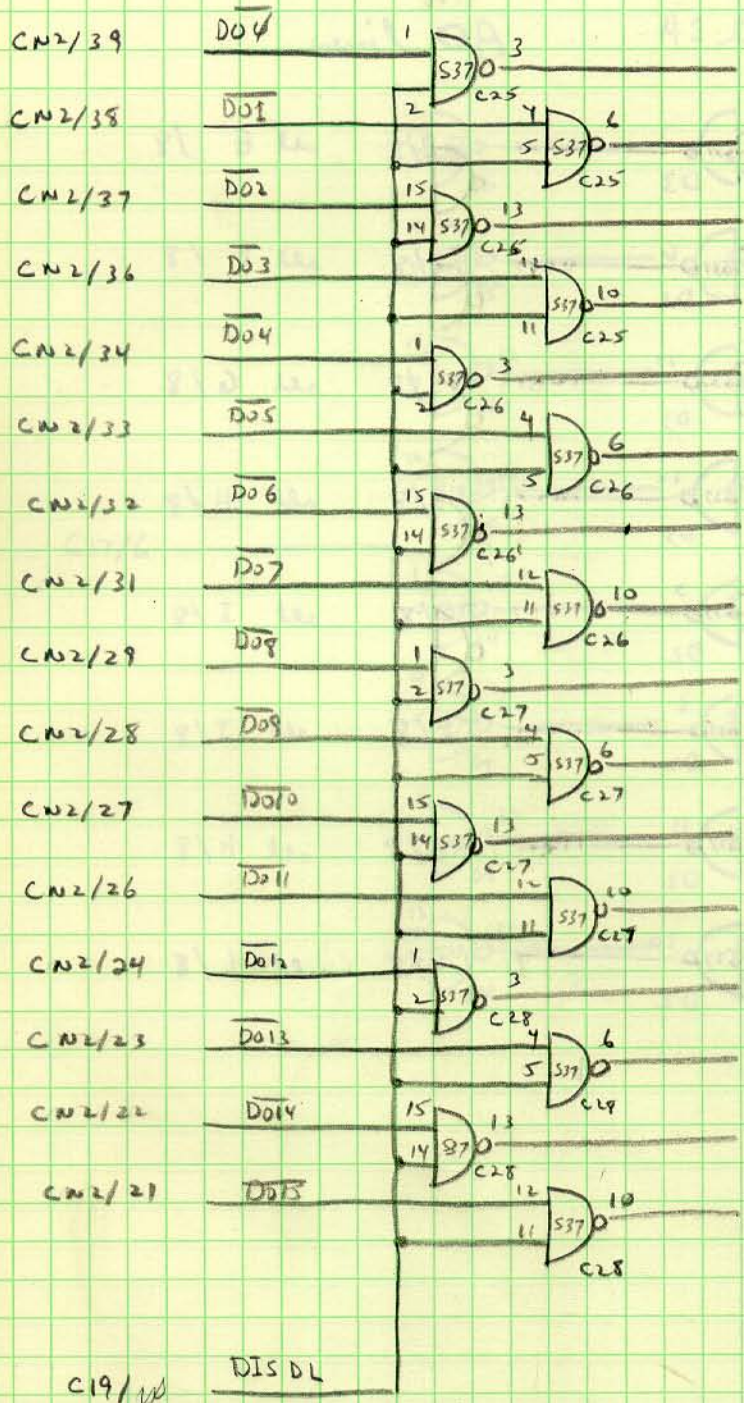
Drive to Address Drives



DATA Buffers & 16 H Frame



Data to Romo
all of each bit have
same driver

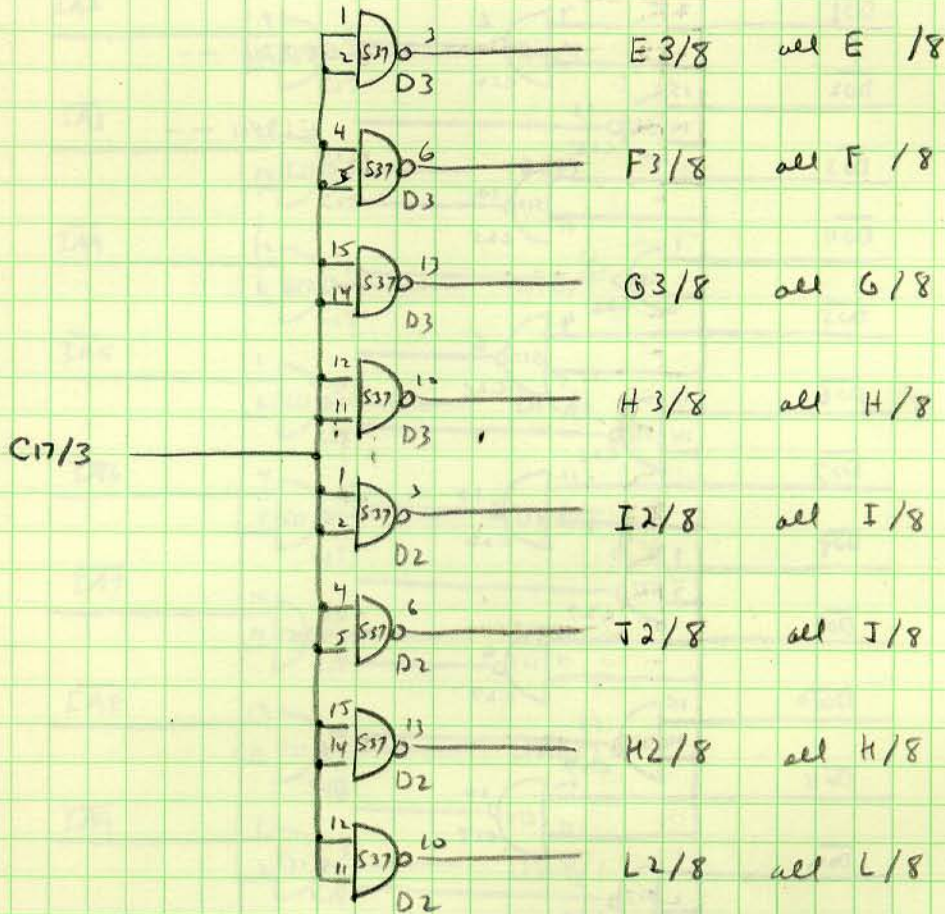


28J a 77
ARB

Address Drives - each gate lines 32 address lines

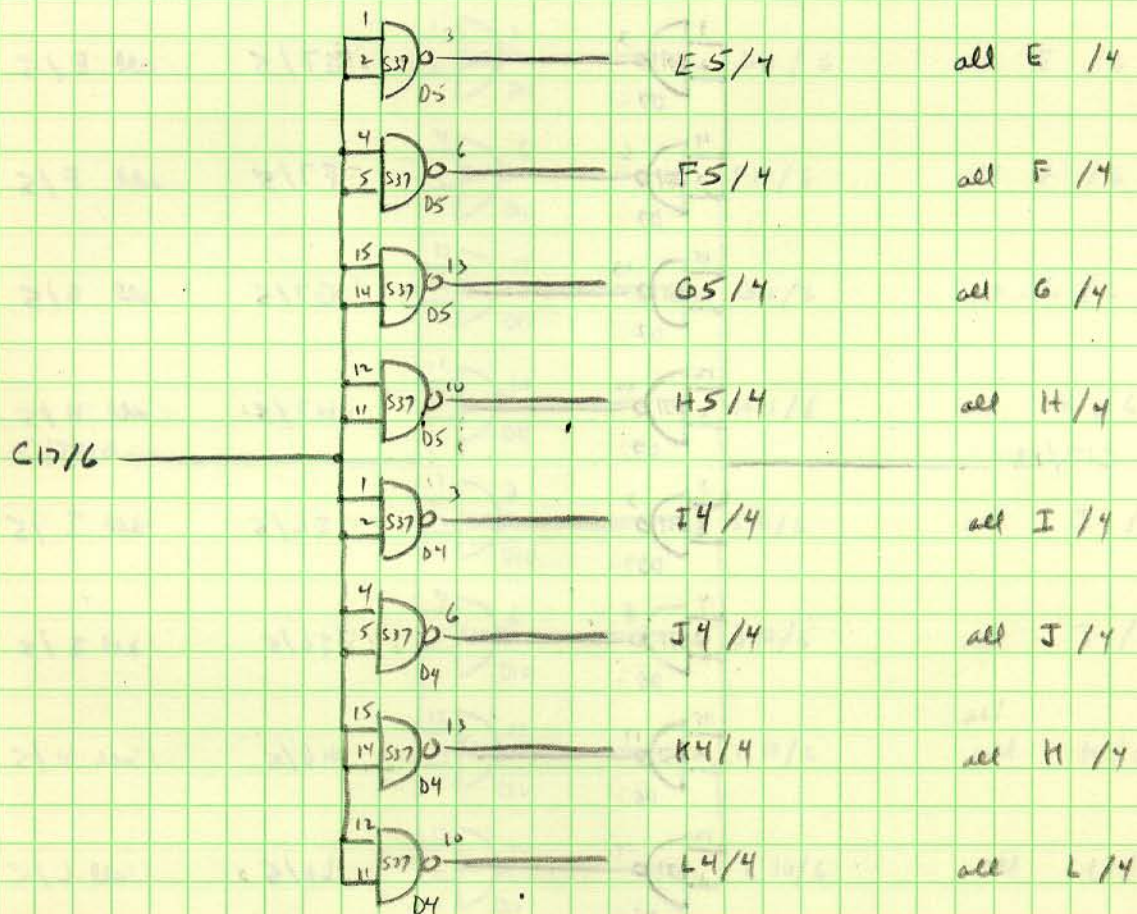
✓

AO lines





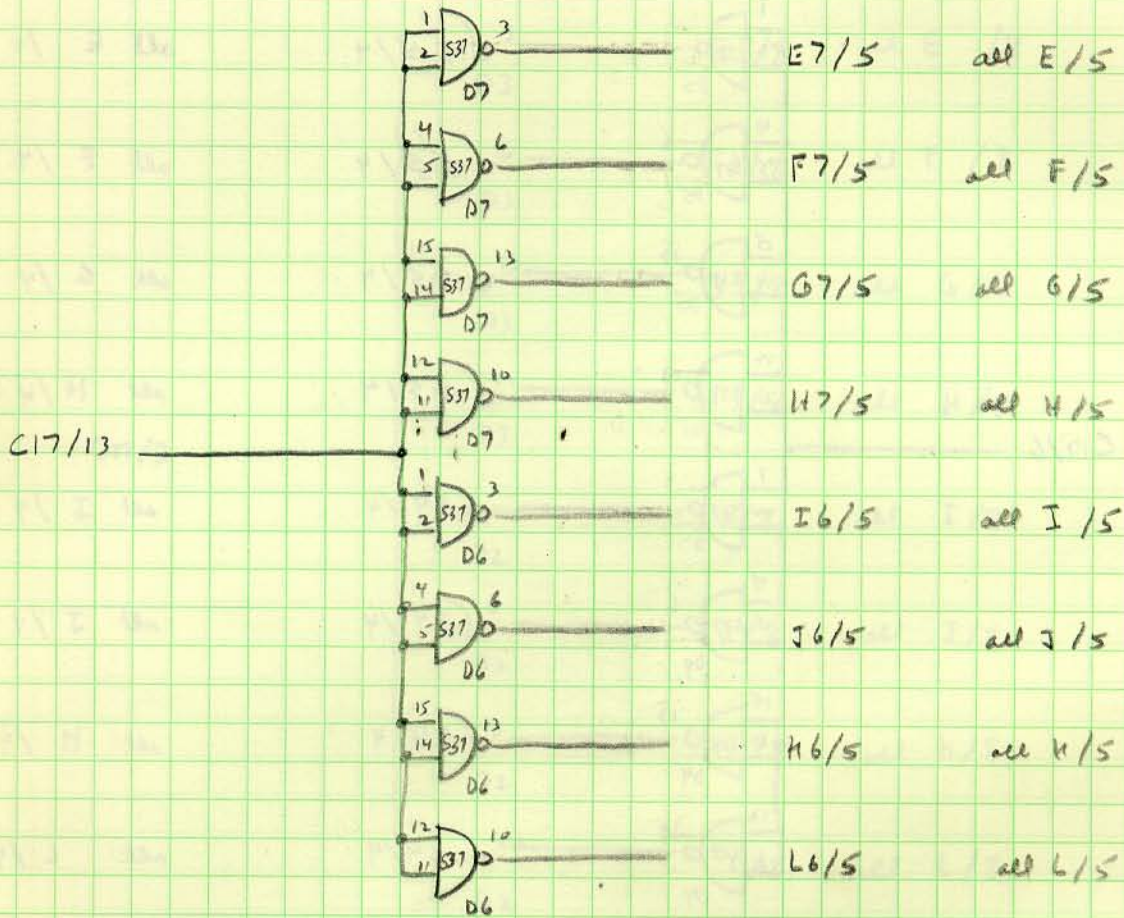
AI lines



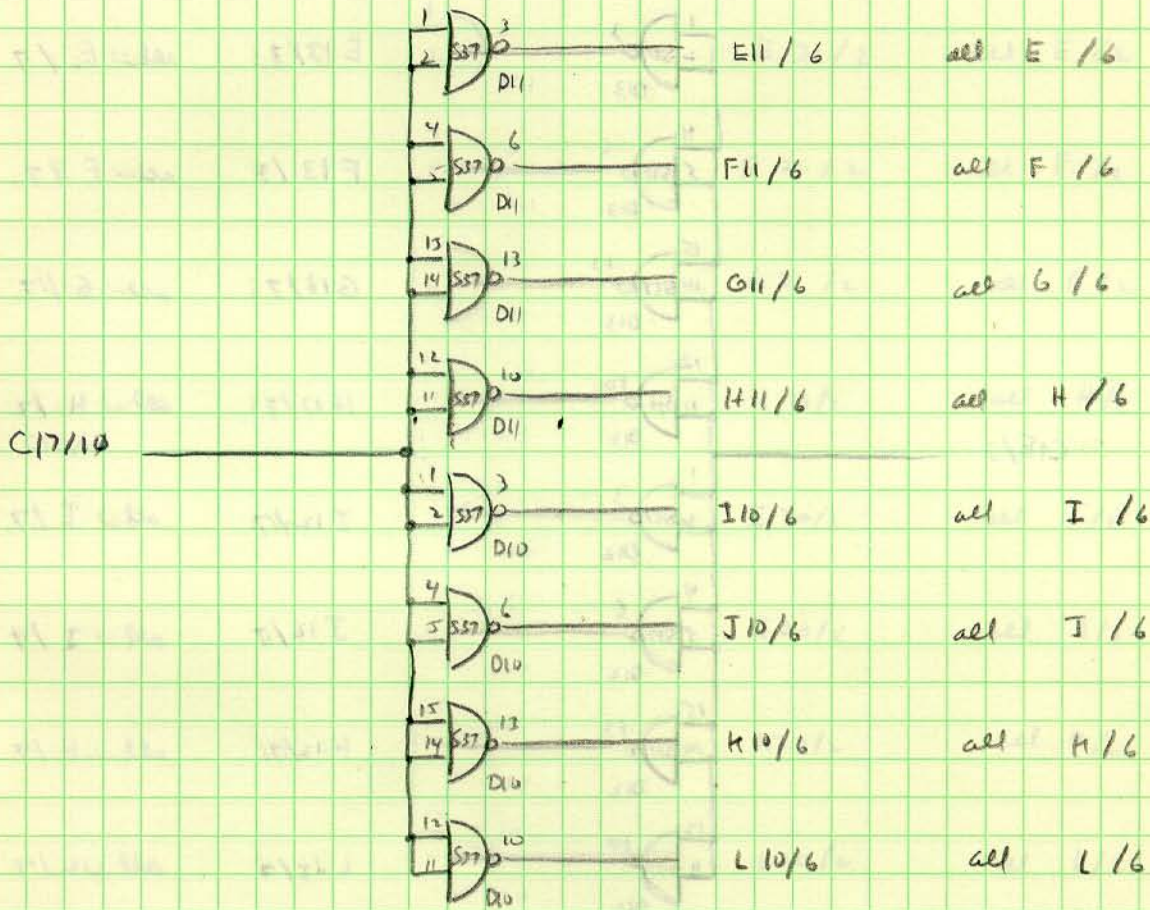
29.12.77

AR3

A2 lines ✓



A3 lines ✓

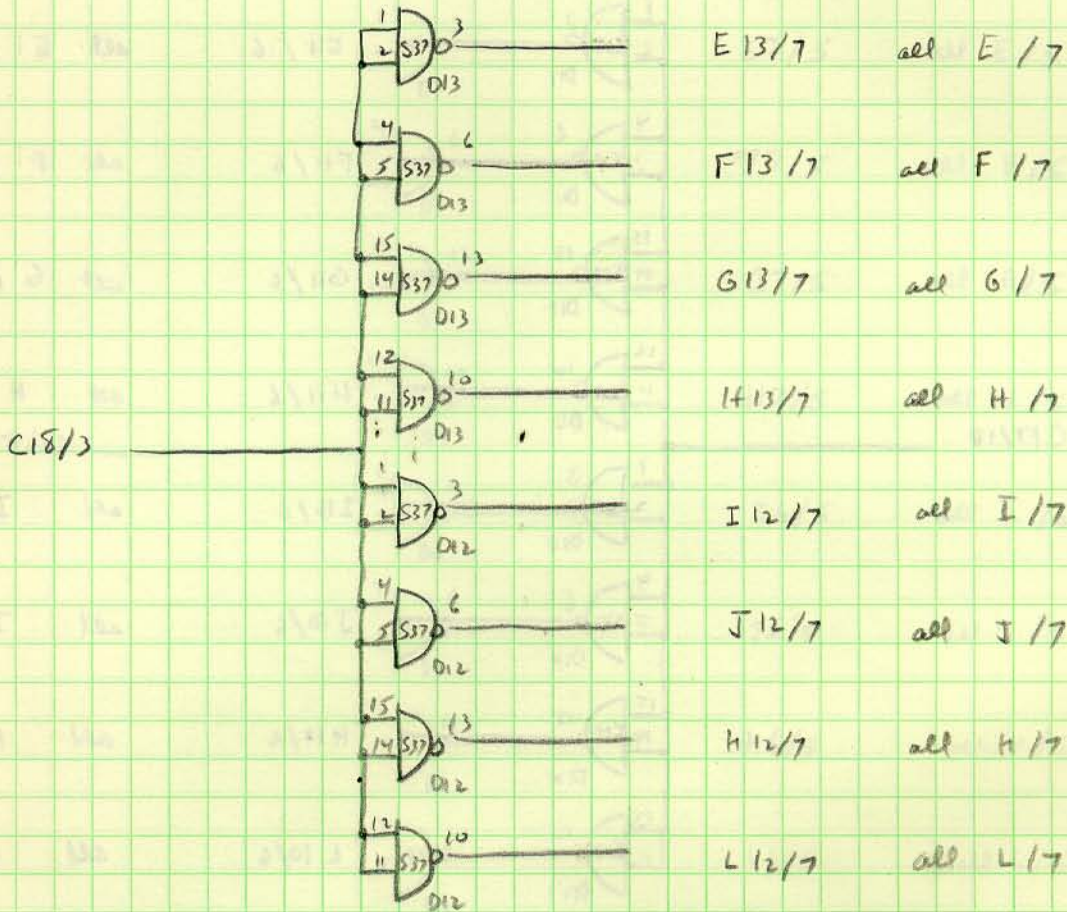


29 Ja 77

ARB

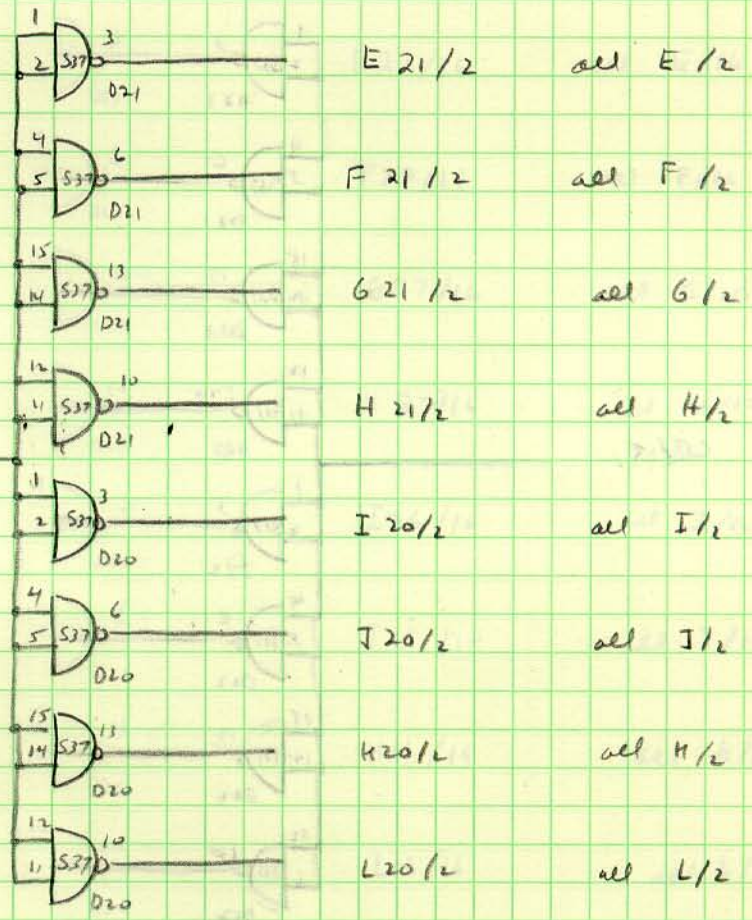
A4 lines

✓



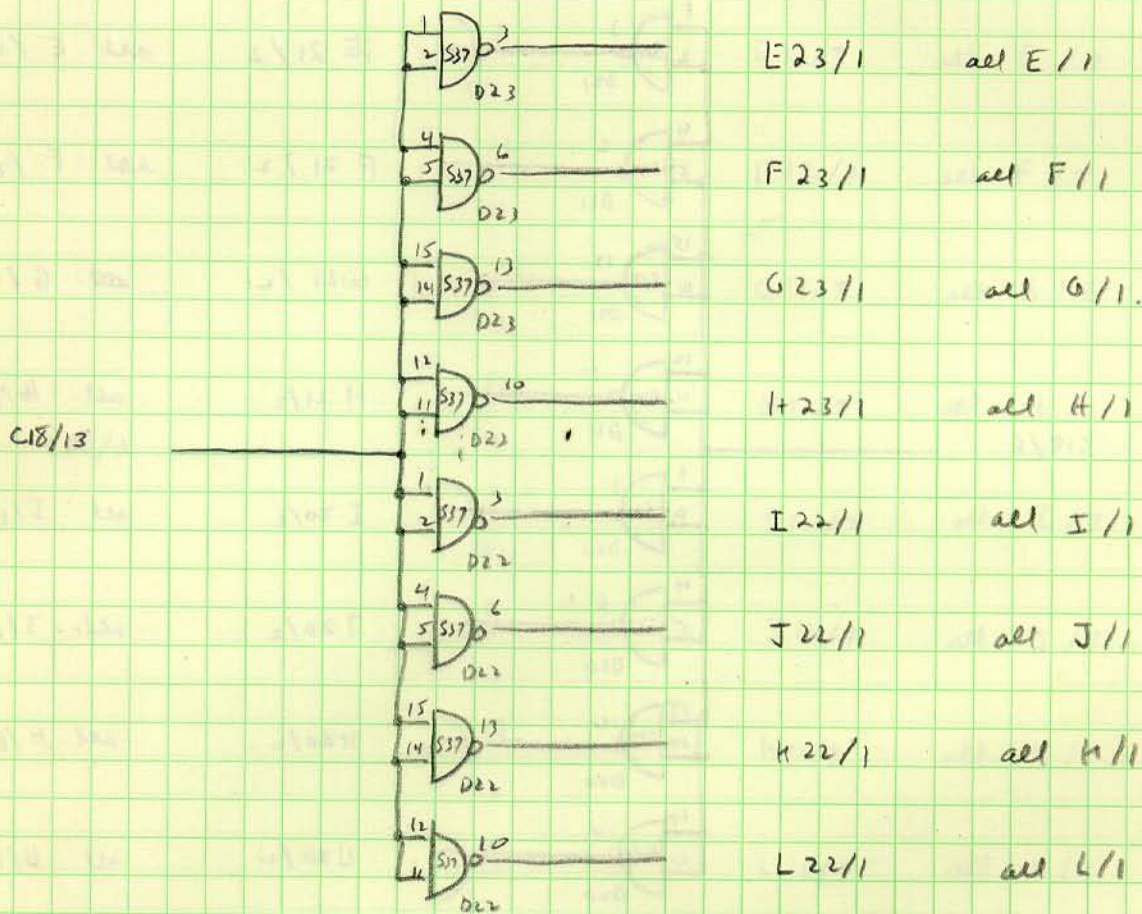
A 5 lines ✓

C18/6

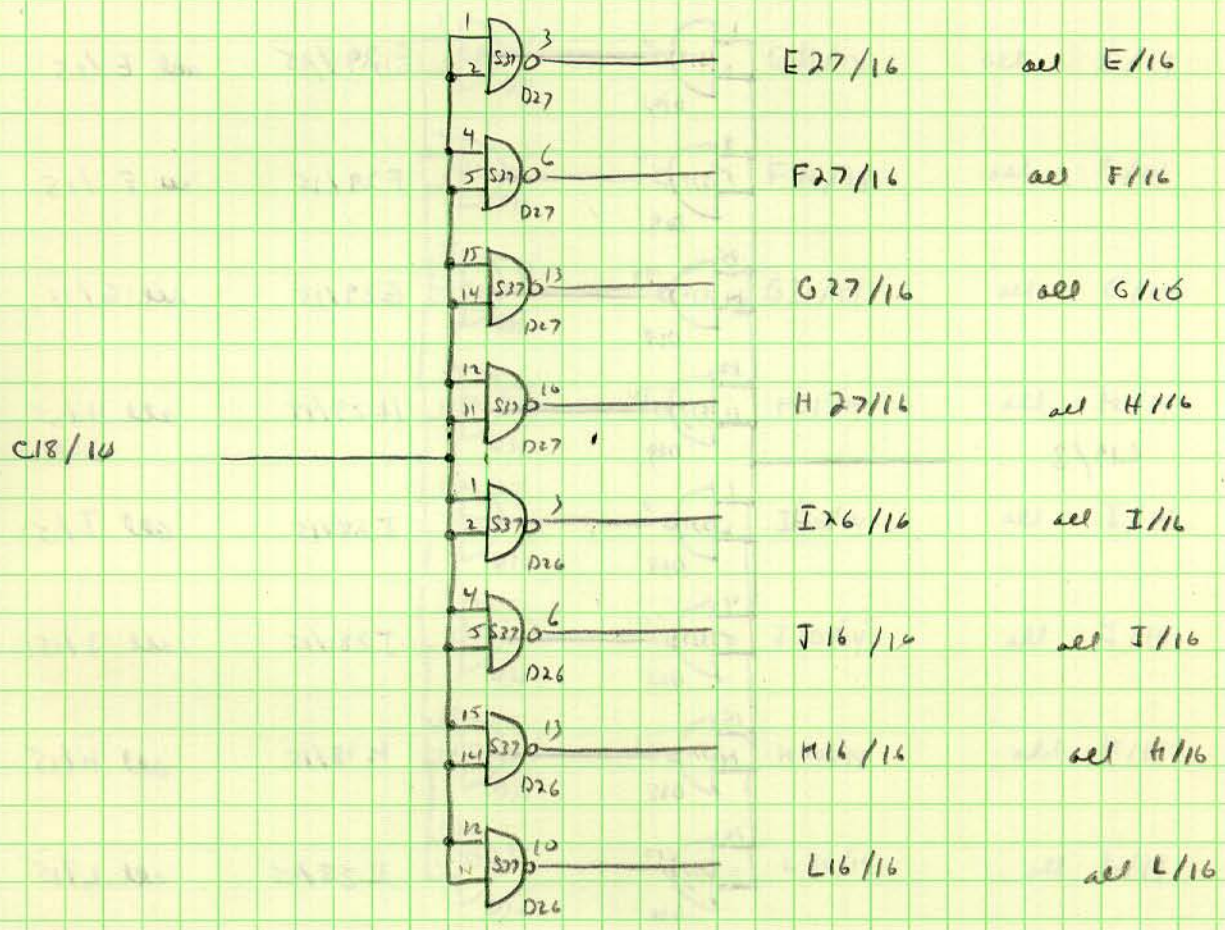


29 Jan 77
ARB

A6 lines ✓



A7 lines ✓



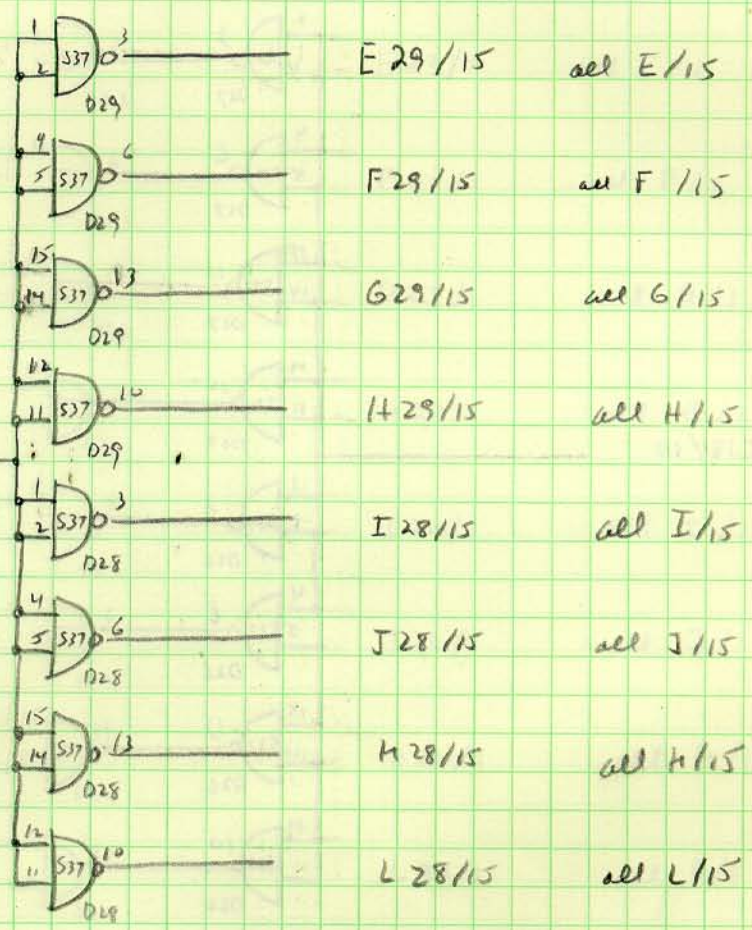
29 Jan 77

ARJ

A 8 lines

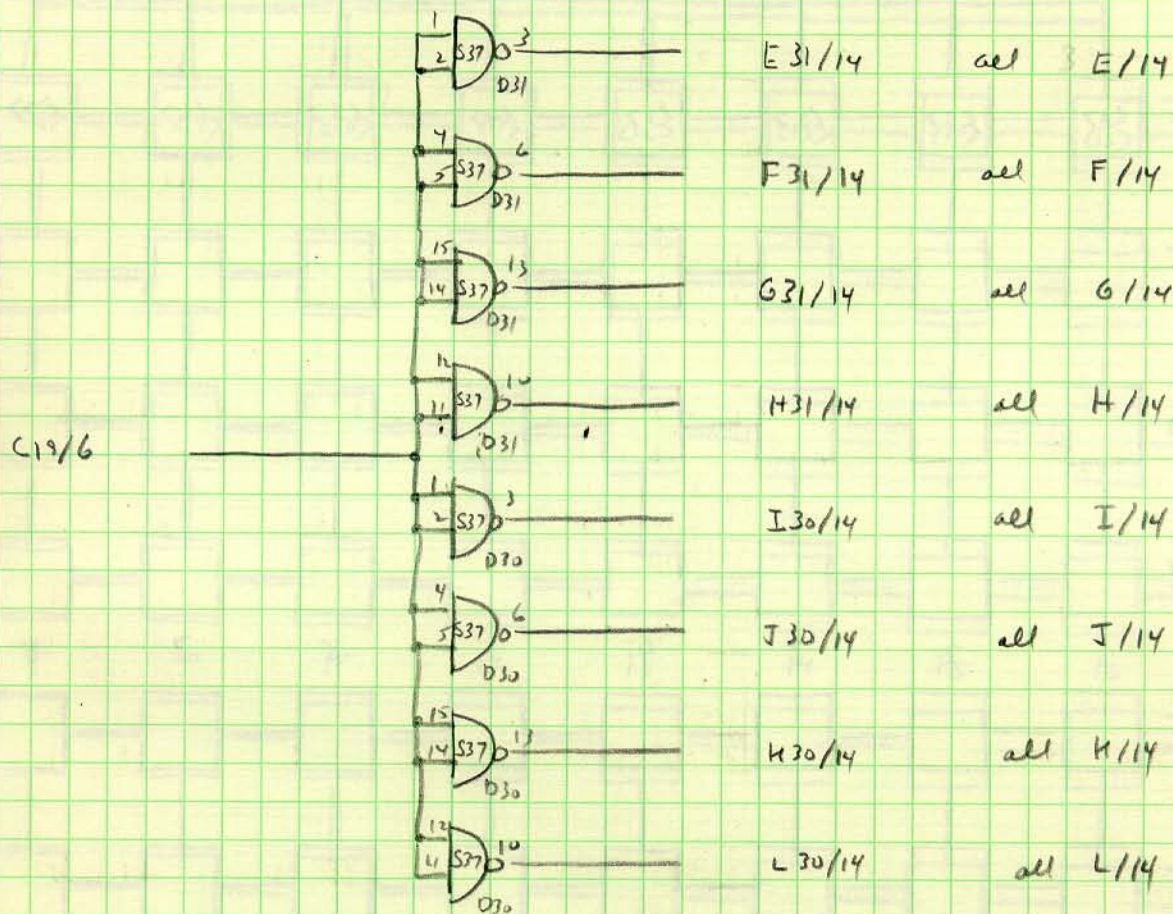


C19/3



A9 lines

✓



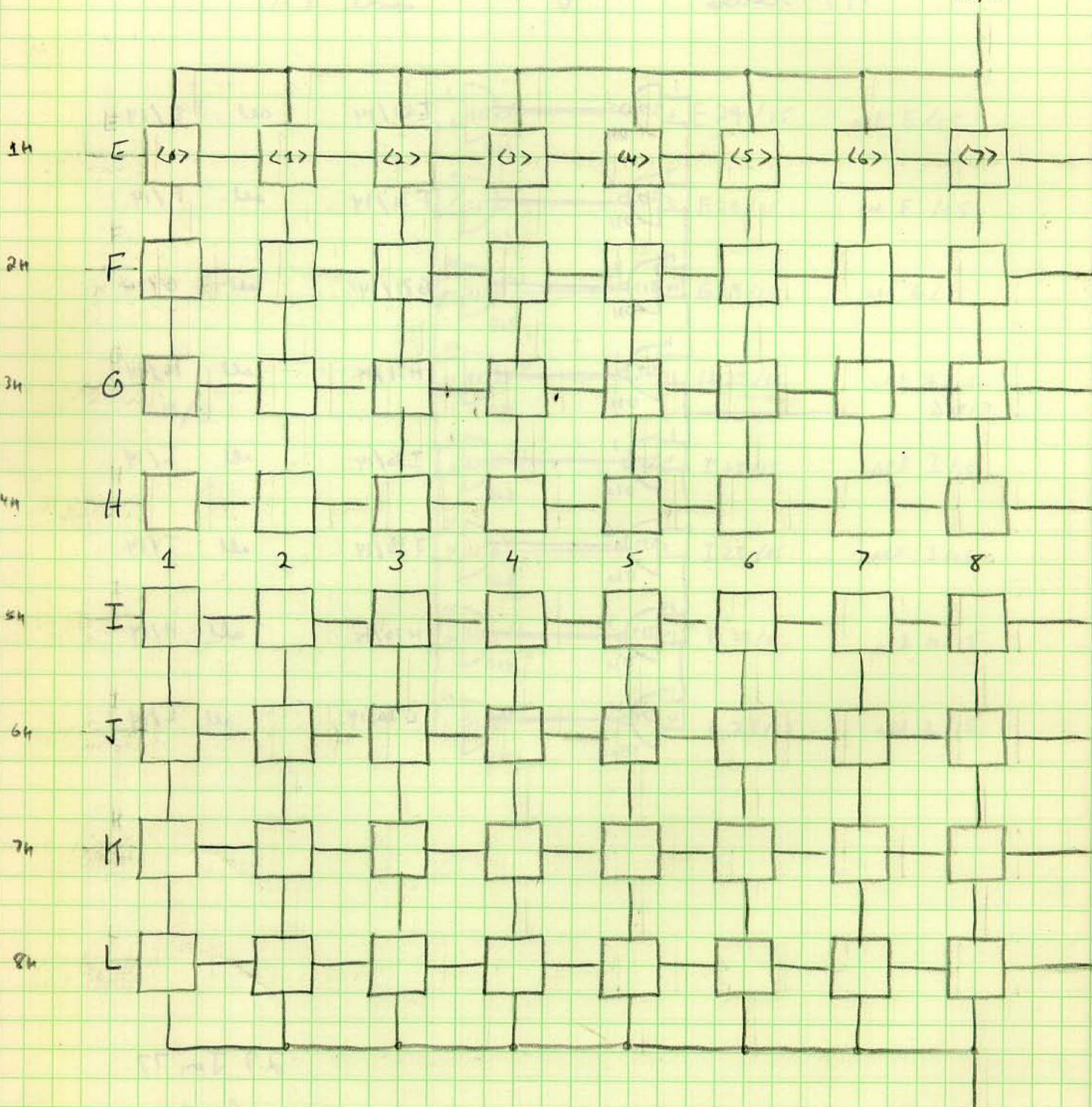
29 Jan 77

ARB

lower 8K chip select & Read/Write connections

Read/Write

D8/6

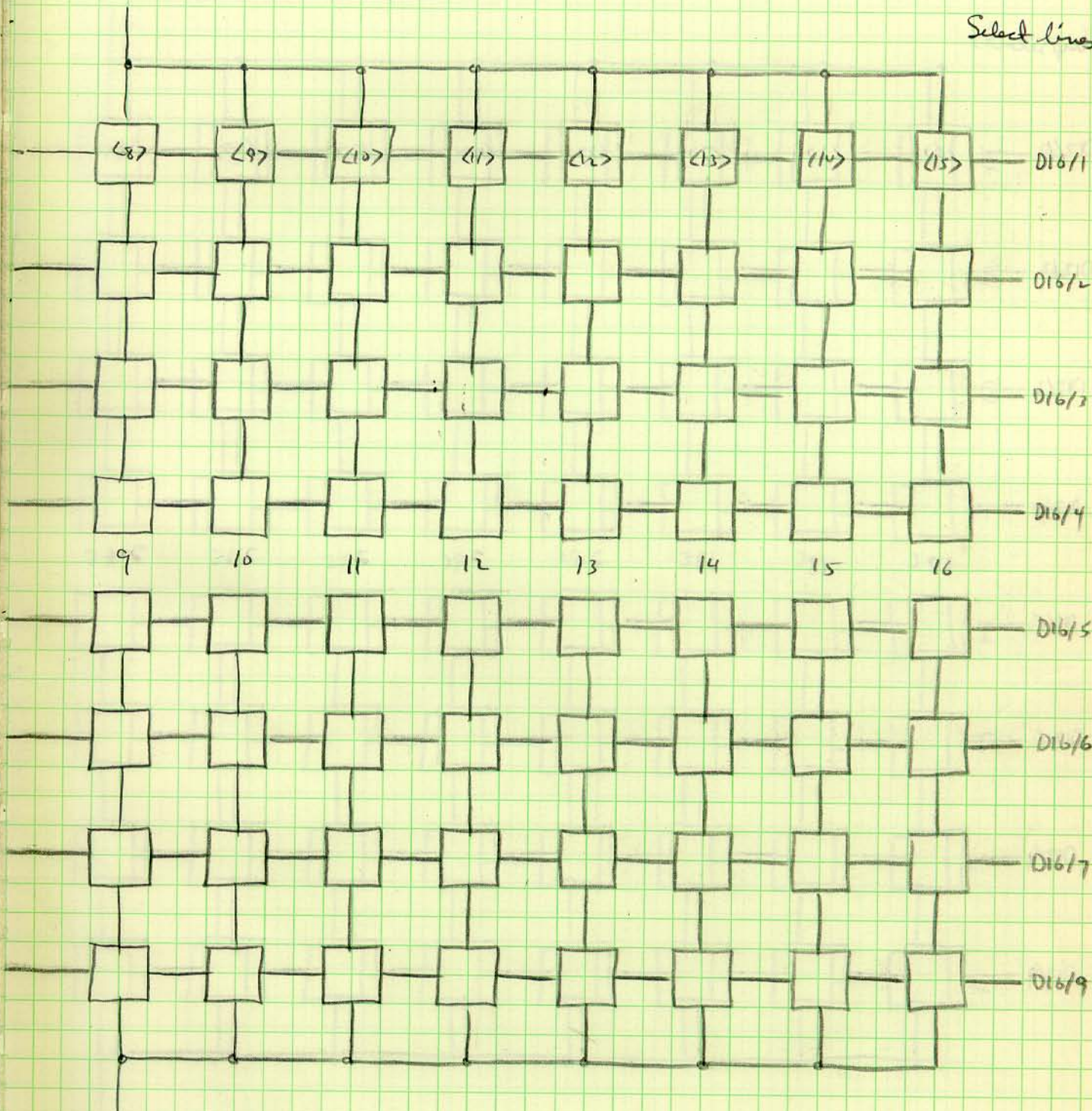


D8/14

Read/Write

D9/6

Select lines

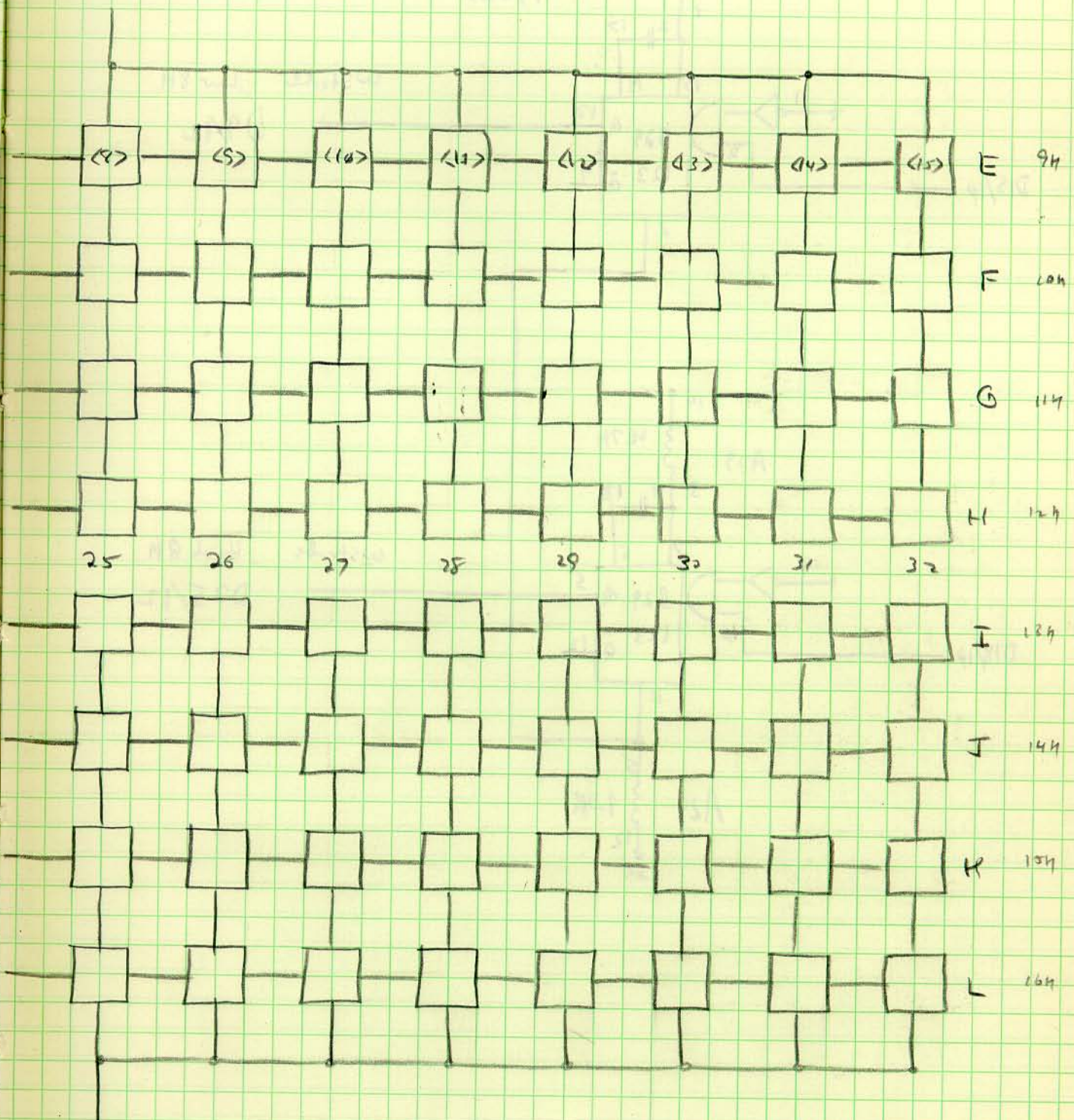


D9/14

29 Jan 77

ARS

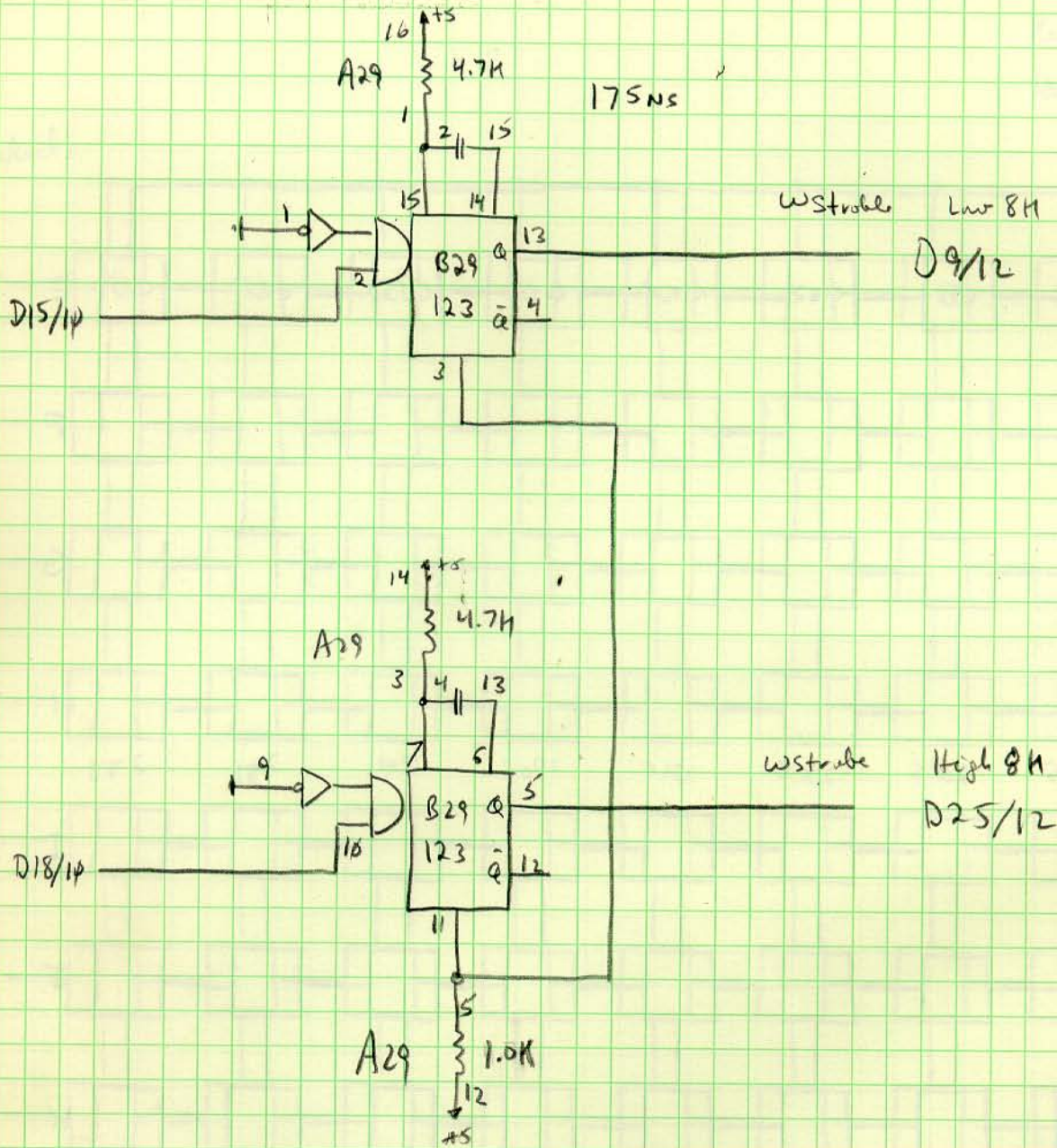
D25/6



D25/14

29 Jan 77
ABD

Write Strobe Logic



ABD 10 March 1979

Microcode Board # 2

16K x 16
2K x 128

Frame # 5

45

Contains

2K x 96 Bits of Microcode

2K x 32 Bits of Instruction Data

Data read as 2K x 128 Bits

Data written as 16K x 16 Bits

RAM Memories are 1K x 1 2102 Types

12 Feb 77
ARS

32	45	69	8	96	2	17
6	F	H	L	K	L	
						18
						19
						20
						21
						22
						23
						24
						25
						26
						27
						28
						29
						30
						31
						32

12 F. 477
A80

CN1 / CN7

<127: 967>

1	MC96	+	D1/11
2		+	D2/11
3		+	D3/11
4		+	D4/11
5	GND		
6		+	D5/11
7		-	D6/11
8		-	D7/11
9		-	D8/11
10	GND		
11		+	D9/11
12		+	D10/11
13		+	D11/11
14		-	D12/11
15	GND		
16		+	D13/11
17		+	D14/11
18		-	D15/11
19	MC111	-	D16/11
20	GND		

40	GND		
39	MC112	+	D1/13
38		+	D2/13
37		+	D3/13
36		+	D4/13
35	GND		
34		+	D5/13
33		+	D6/13
32		+	D7/13
31		+	D8/13
30	GND		
29		+	D9/13
28		-	D10/13
27		+	D11/13
26		-	D12/13
25	GND		
24		+	D13/13
23		+	D14/13
22		-	D15/13
21	MC127	+	D16/13

CN3

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20

CN2 / CN8

<95 - 63 >

1	MC64	+	C1/11
2		+	C2/11
3		-	C3/11
4		-	C4/11
5	GND		
6		+	C5/11
7		+	C6/11
8		-	C7/11
9		-	C8/11
10	GND		
11		+	C9/11
12		+	C10/11
13		+	C11/11
14		-	C12/11
15	GND		
16		+	C13/11
17		+	C14/11
18		-	C15/11
19	MC79	+	C16/11
20	GND		

40	GND		
39	MC80	+	C1/13
38		+	C2/13
37		+	C3/13
36		+	C4/13
35	GND		
34		+	C5/13
33		+	C6/13
32		+	C7/13
31		+	C8/13
30	GND		
29		+	C9/13
28		+	C10/13
27		+	C11/13
26		+	C12/13
25	GND		
24		+	C13/13
23		+	C14/13
22		+	C15/13
21	MC95	-	C16/13

CN4

1
2
3
4
5
6
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8
9
10
11
12
13
14
15
16
17
18
19
20

CN3/CN9

<63:32>

1	MC 32	+	C1/7
2		T	C2/7
3		T	C3/7
4		T	C4/7
5	GND		
6		+	C5/7
7		+	C6/7
8		+	C7/7
9		+	C8/7
10	GND		
11		+	C9/7
12		+	C10/7
13		T	C11/7
14		T	C12/7
15	GND		
16		+	C13/7
17		T	C14/7
18		+	C15/7
19	MC 47	+	C16/7
20	GND		

40	GND		
39	MC 48	+	C1/9
38		+	C2/9
37		T	C3/9
36		T	C4/9
35	GND		
34		T	C5/9
33		T	C6/9
32		T	C7/9
31		+	C8/9
30	GND		
29		+	C9/9
28		+	C10/9
27		+	C11/9
26		+	C12/9
25	GND		
24		T	C13/9
23		+	C14/9
22		+	C15/9
21	MC 63	+	C16/9

CN4/CN10

<31:4>

1	MC 4	+	C1/3
2		+	C2/3
3		+	C3/3
4		+	C4/3
5	GND		
6		T	C5/3
7		+	C6/3
8		+	C7/3
9		T	C8/3
10	GND		
11		T	C9/3
12		T	C10/3
13		T	C11/3
14		T	C12/3
15	GND		
16		+	C13/3
17		+	C14/3
18		+	C15/3
19	MC 15	+	C16/3
20	GND		

40	GND		
39	MC 16	+	C1/5
38		+	C2/5
37		+	C3/5
36		+	C4/5
35	GND		
34		+	C5/5
33		T	C6/5
32		+	C7/5
31		T	C8/5
30	GND		
29		T	C9/5
28		T	C10/5
27		+	C11/5
26		T	C12/5
25	GND		
24		+	C13/5
23		T	C14/5
22		+	C15/5
21	MC 31	+	C16/5

12 Feb 77
ARD

CN5/CN11

Data

1	DA4	+	E17/11
2		+	E18/11
3		+	E19/11
4		+	E20/11
5	GND		
6		+	E21/11
7		+	E22/11
8		+	E23/11
9		+	E24/11
10	GND		
11		+	E25/11
12		+	E26/11
13		+	E27/11
14		+	E28/11
15	GND		
16		+	E29/11
17		+	E30/11
18		+	E31/11
19	DA15	+	E32/11
20	GND		

40	GND		
39	WLB[LT]	-	C24/4
38			
37			
36	WHA[LT]	-	C24/12
35	GND		
34	WAp	-	D24/15
33	WA1	-	D24/14
32	WA2	-	D24/13
31			
30	GND		
29	xA clock [H]	+	B29/1
28			
27			
26	xA Dme	+	B25/6
25	GND		
24			
23			
22			
21			

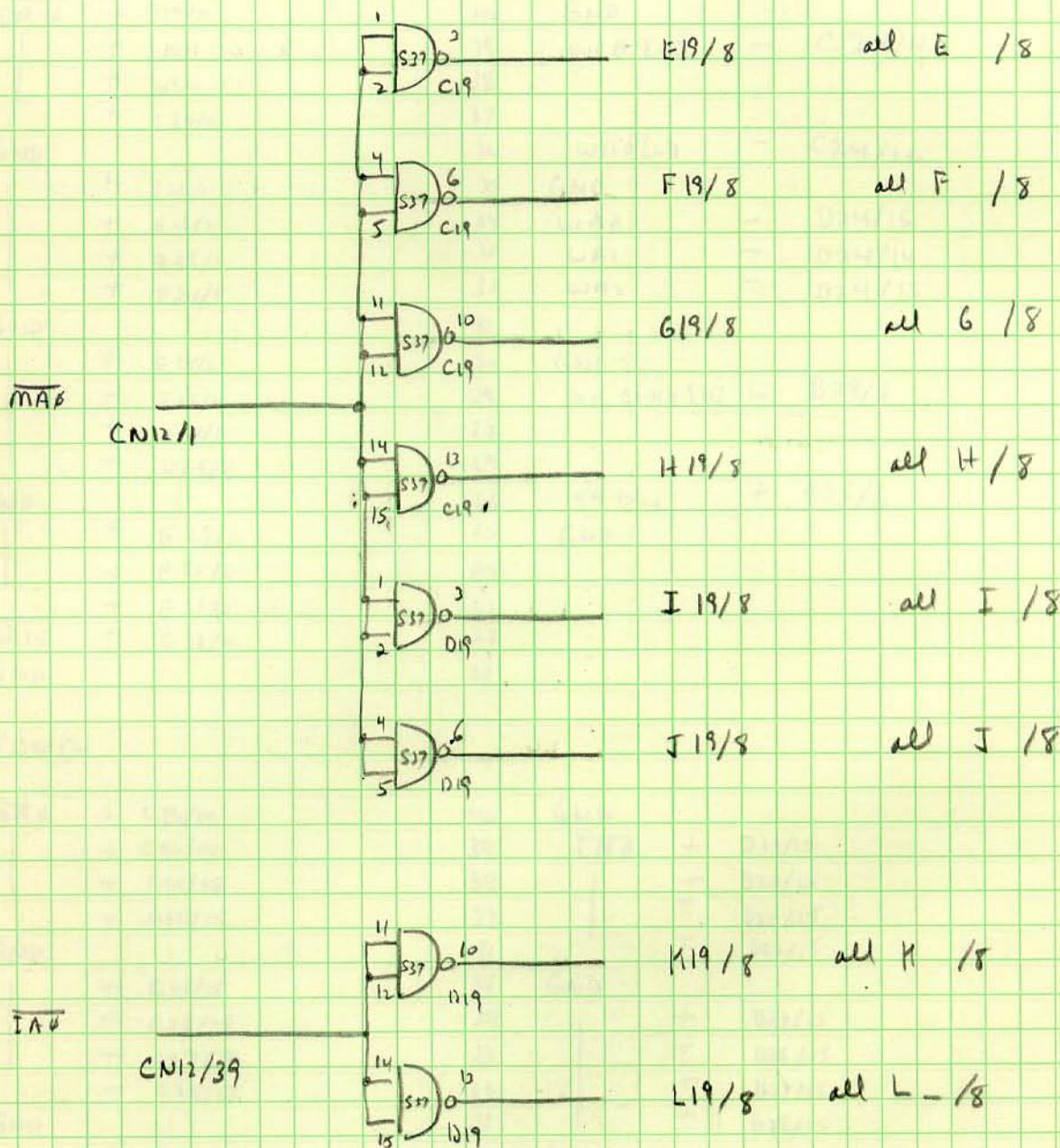
CN6/CN12

1	MA4	+	C19/15
2		+	C20/15
3		+	C21/15
4		+	C22/15
5	GND		
6		+	C23/15
7		+	C26/15
8		+	C27/15
9		+	C28/15
10	GND		
11		+	C29/15
12		+	C30/15
13		+	B26/1
14	MA13	+	B26/15
15	GND		
16	Mclock	+	C19/12
17			
18	mDme	+	B25/2
19	mPSL[LT]	+	C19/11 B28/4
20	GND		

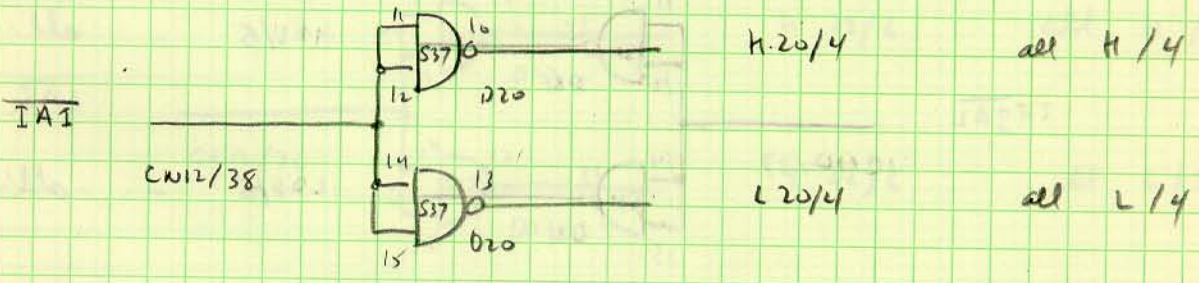
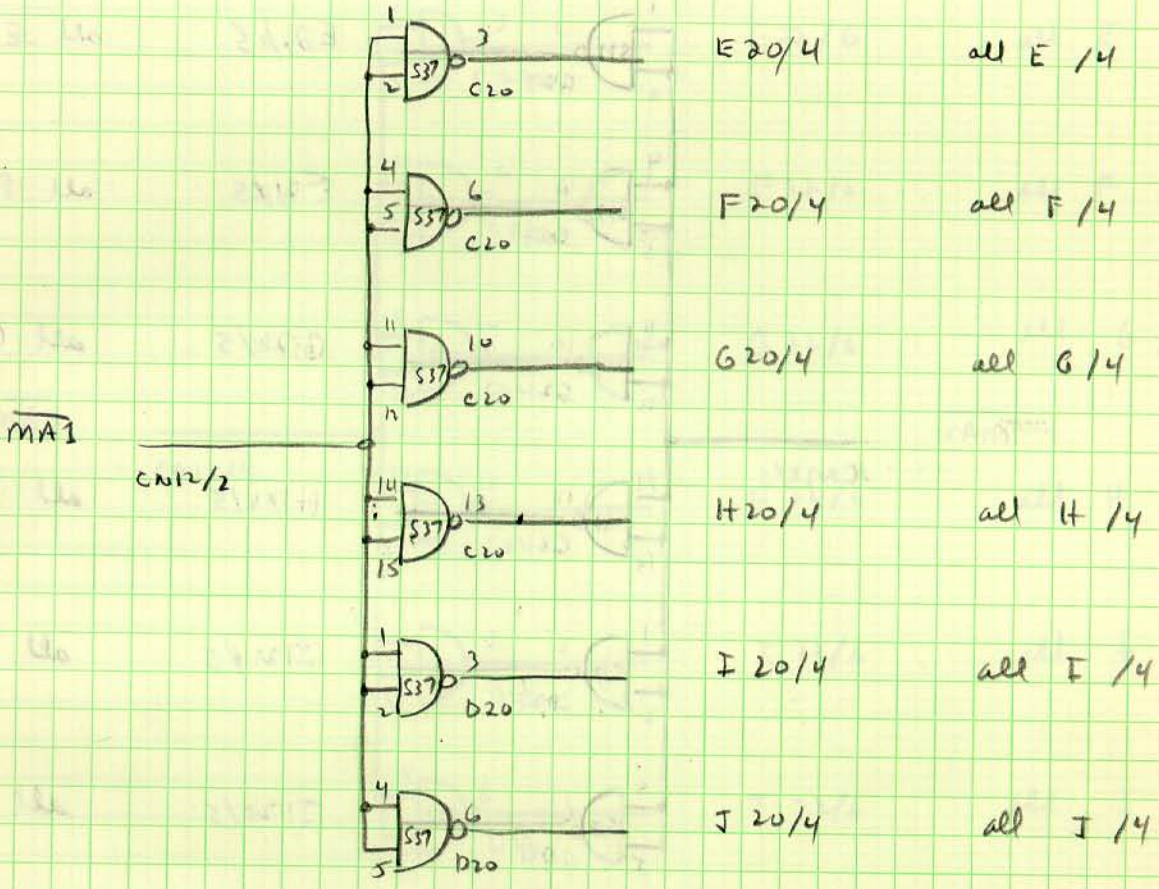
40	GND		
39	IA4	+	D19/15
38		+	D20/15
37		+	D21/15
36		+	D22/15
35	GND		
34		+	D23/15
33		+	D26/15
32		+	D27/15
31		+	D28/15
30	GND		
29		+	D29/15
28		+	D30/15
27		-	B27/1
26	IA11	-	B27/15
25	GND		
24	Iclock	+	D18/12
23			
22	IDme	+	B25/4
21	IDSL[LT]	+	D18/11

Address Drivers

AD Driver

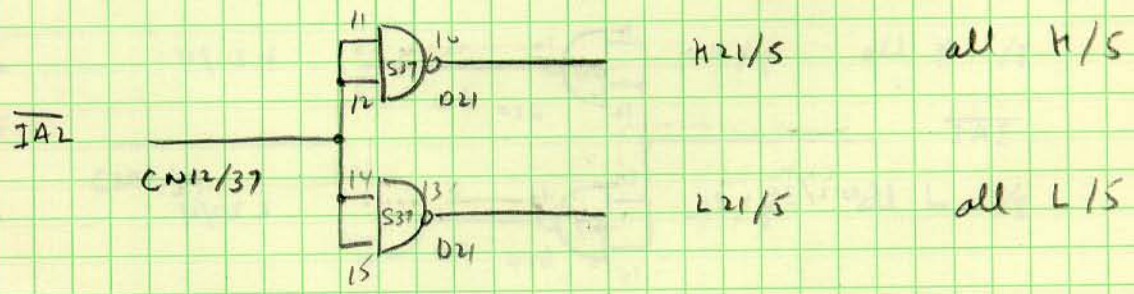
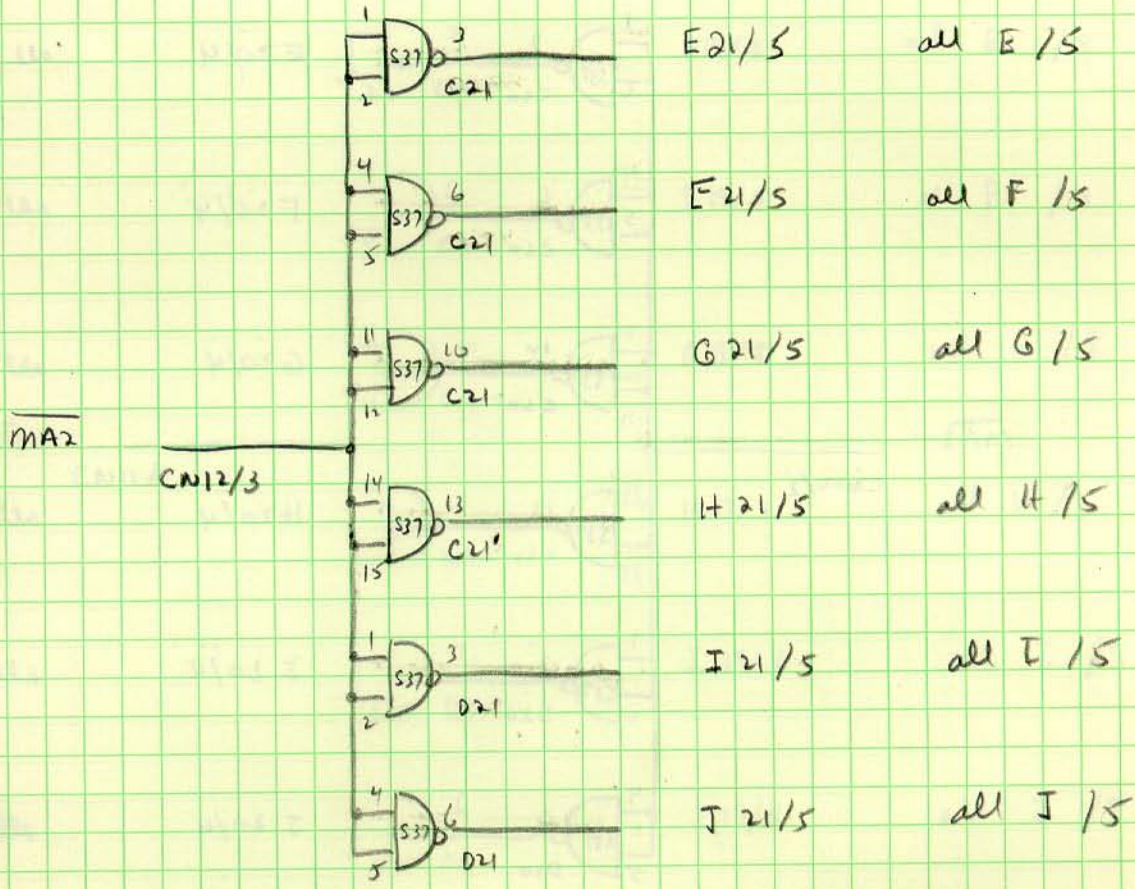


AI Driver ✓



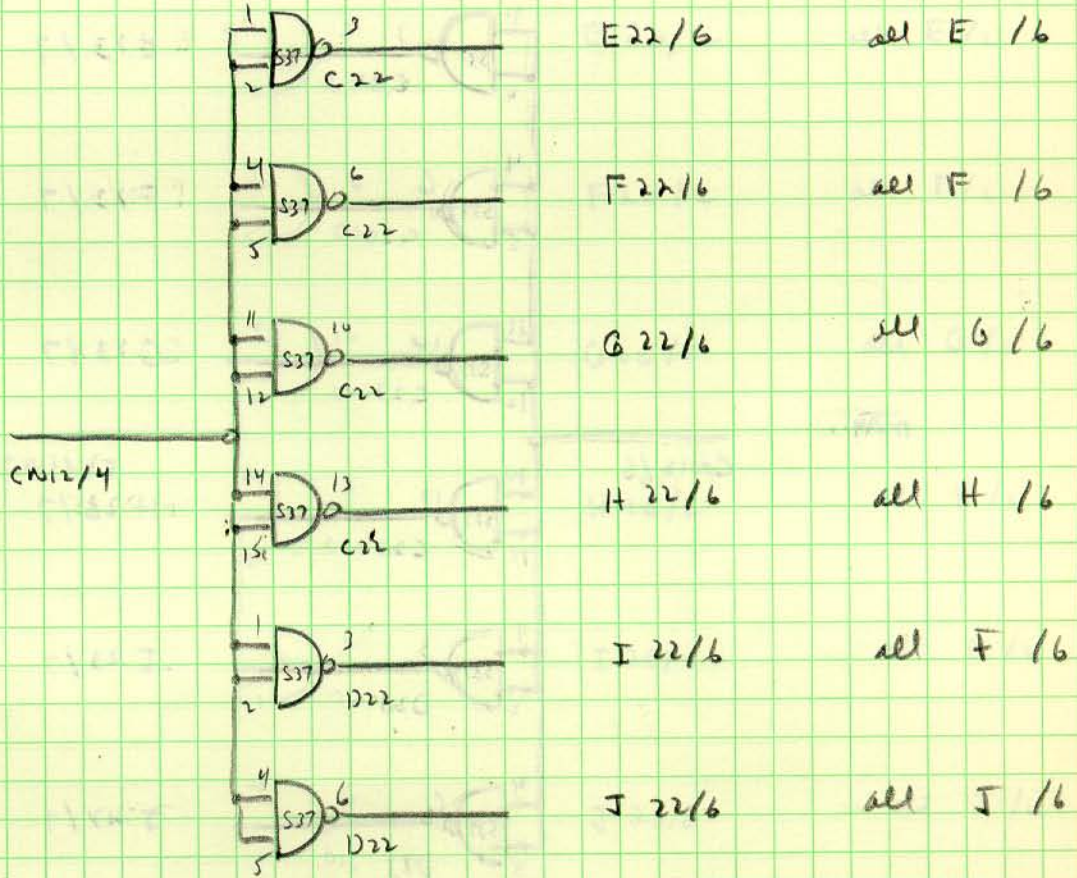
12 Feb 77
ARD

A2 Driver ✓

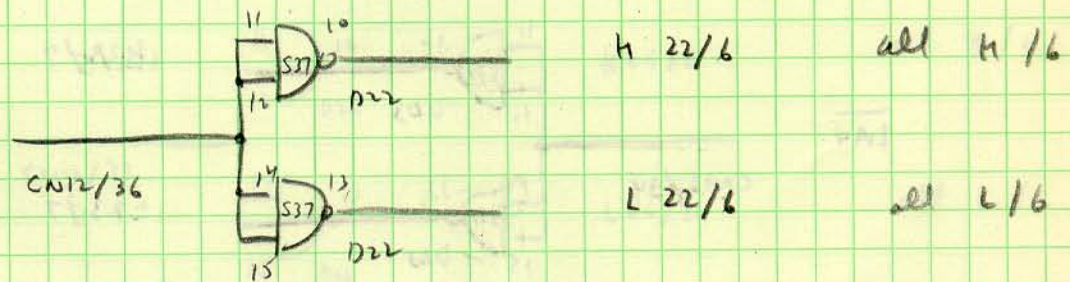


A3 Driver ✓

$\overline{MA3}$



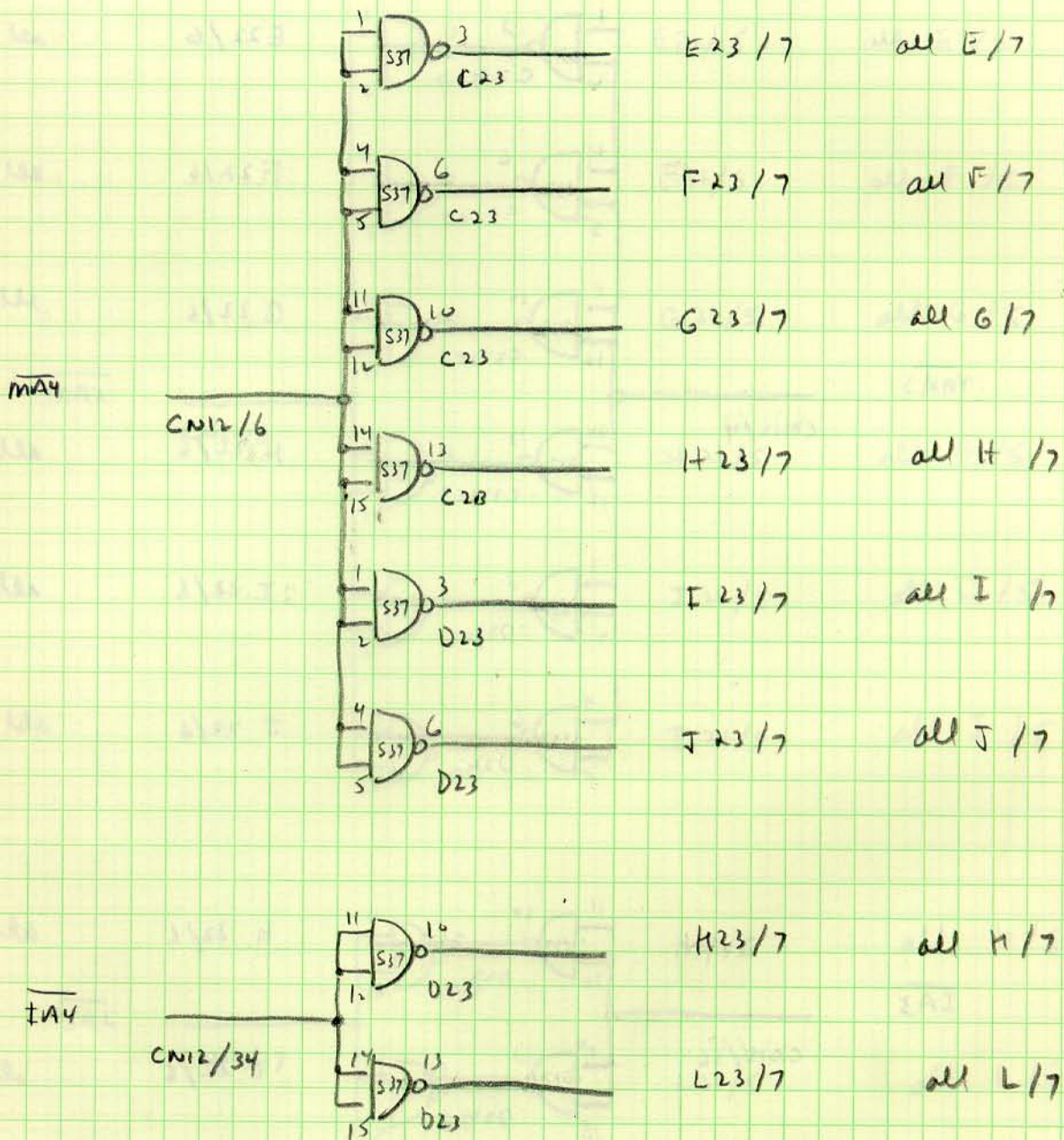
$\overline{IA3}$



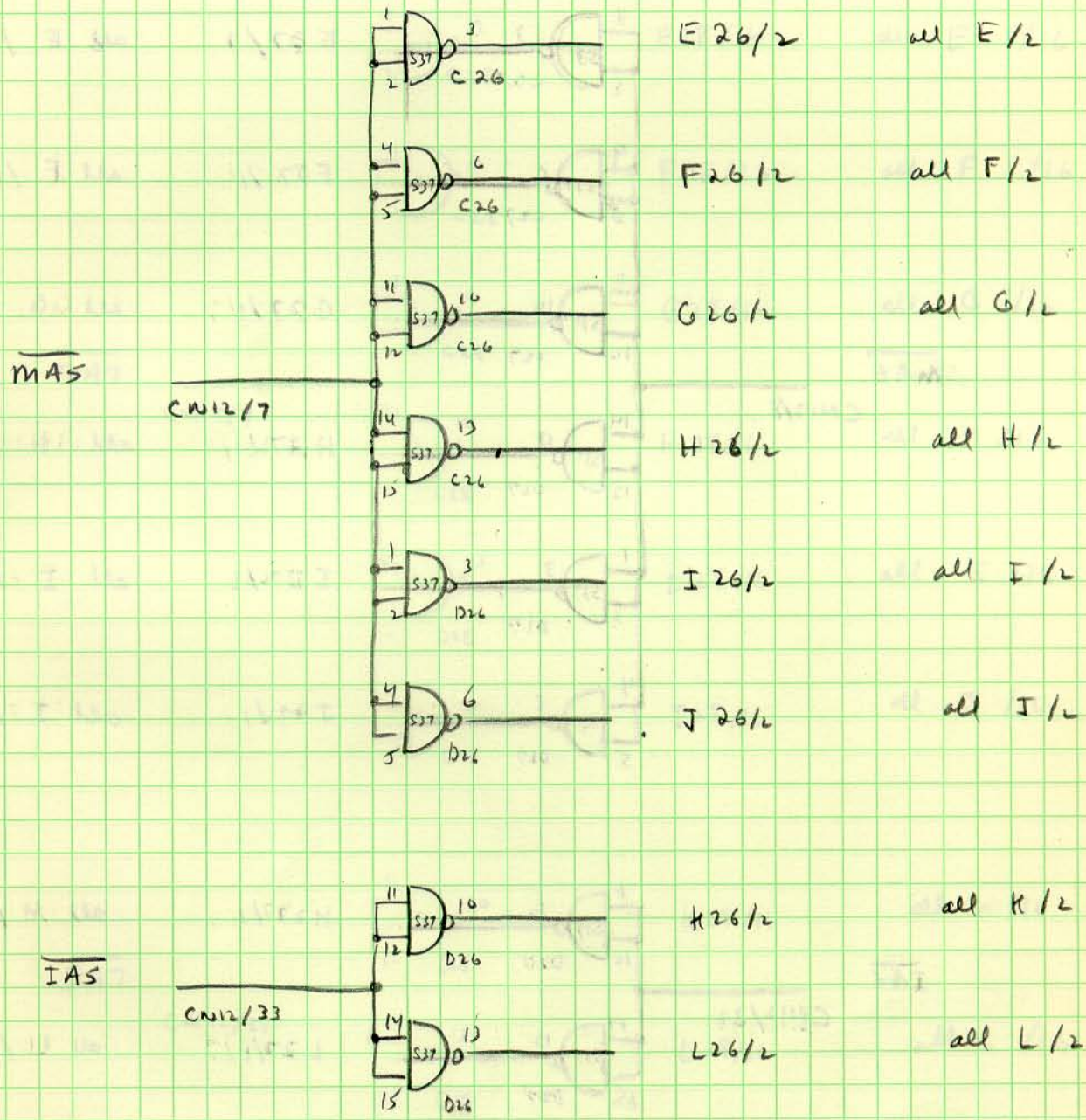
12 Feb 77

ARD

A4 Drives ✓

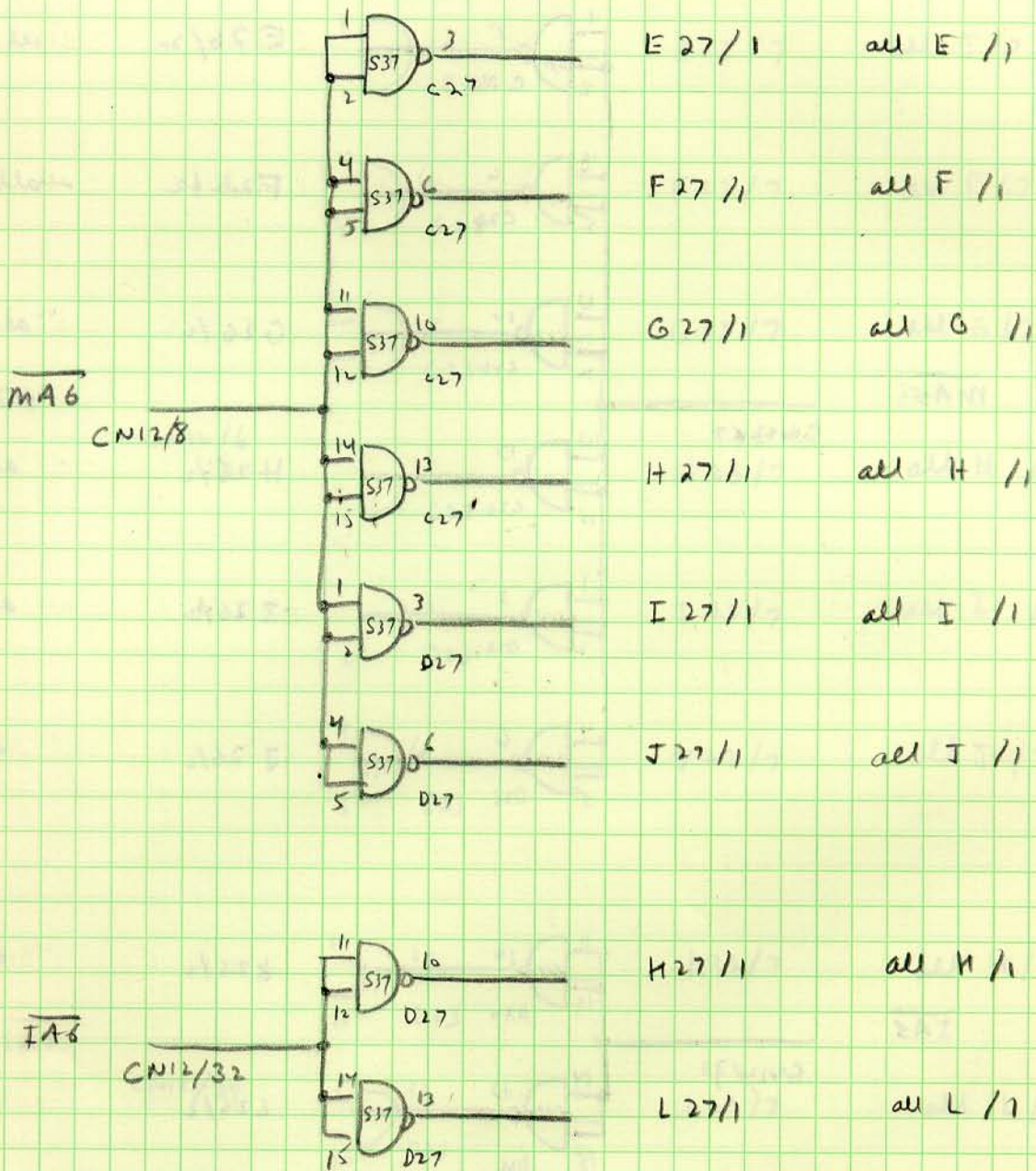


AS Drivers ✓

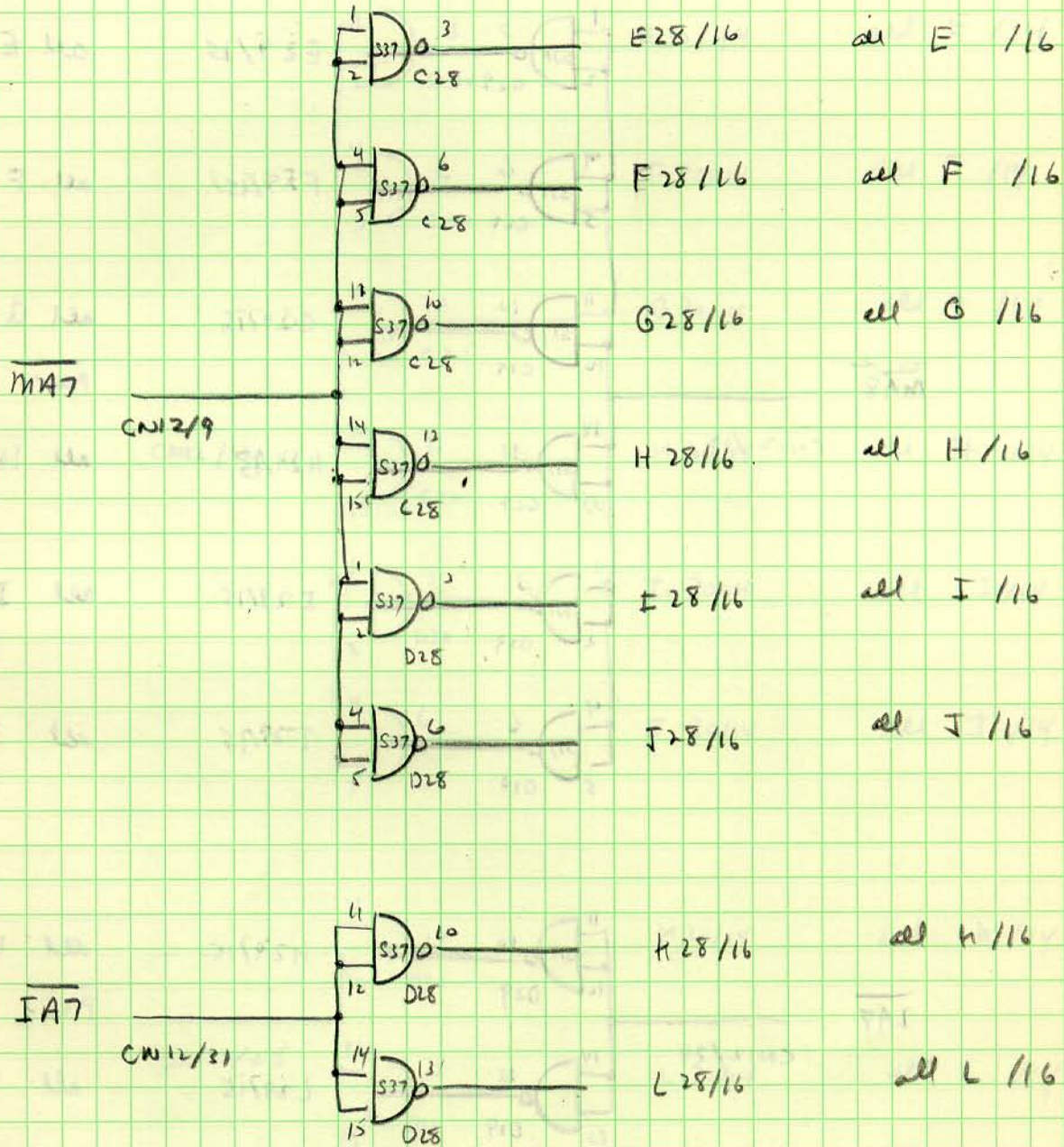


12 Feb 77
AFO

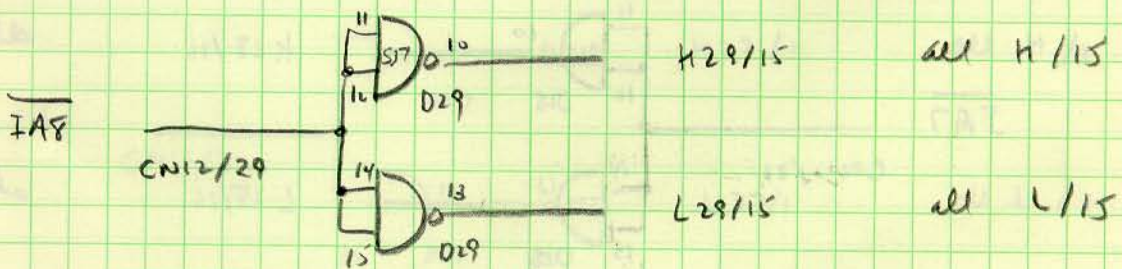
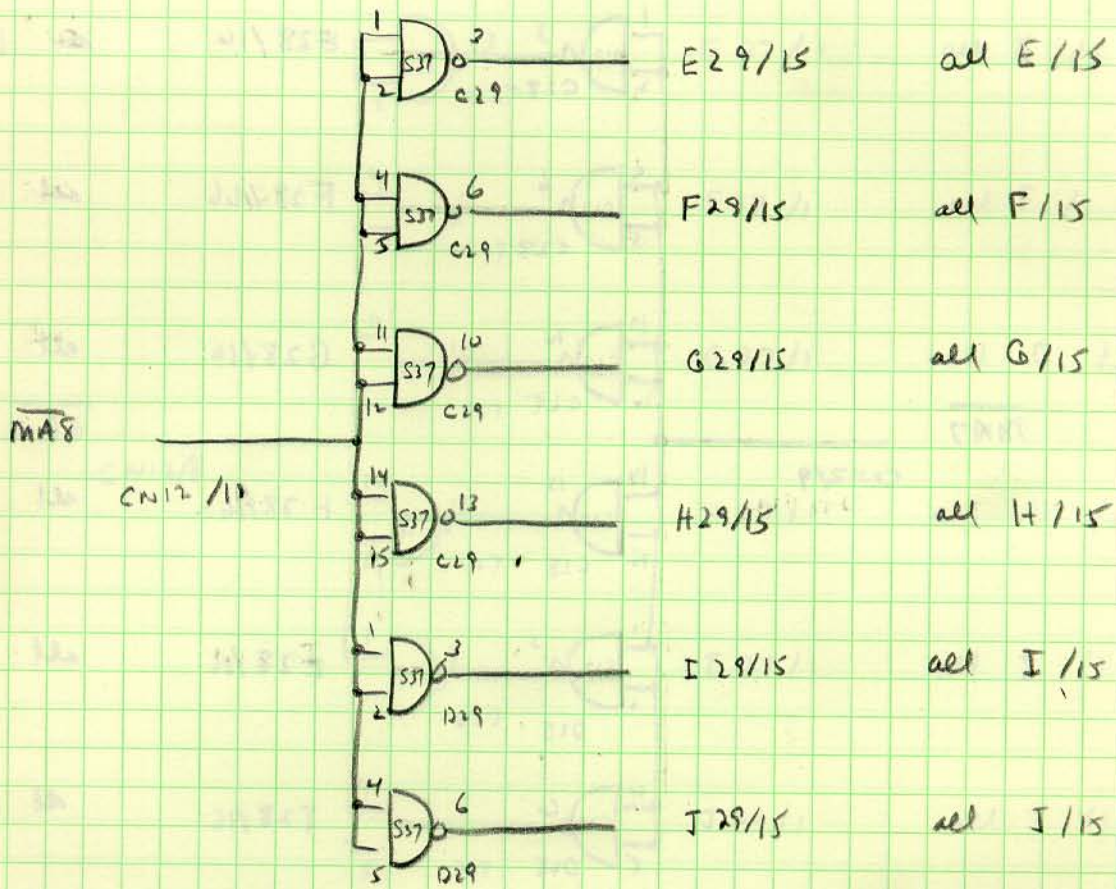
A6 Drivers ✓



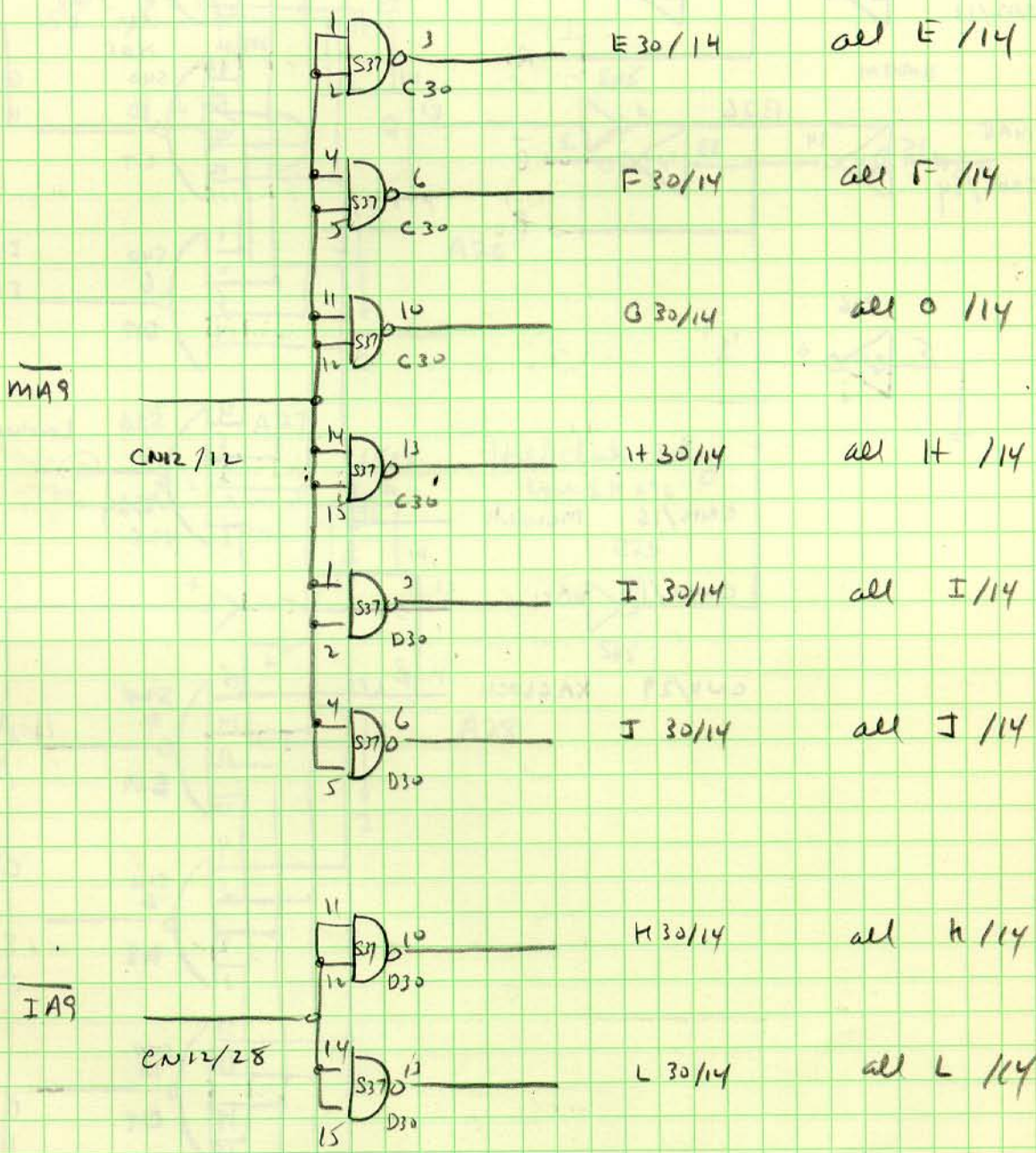
A7 Drivers ✓



A8 Drives ✓

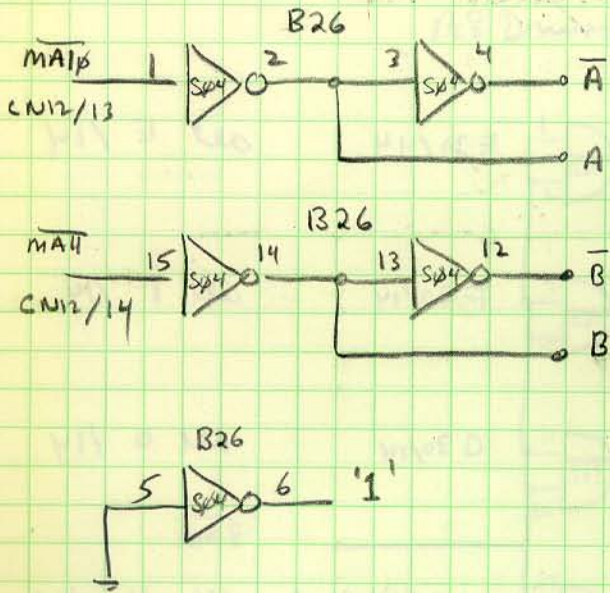


AP Drives ✓

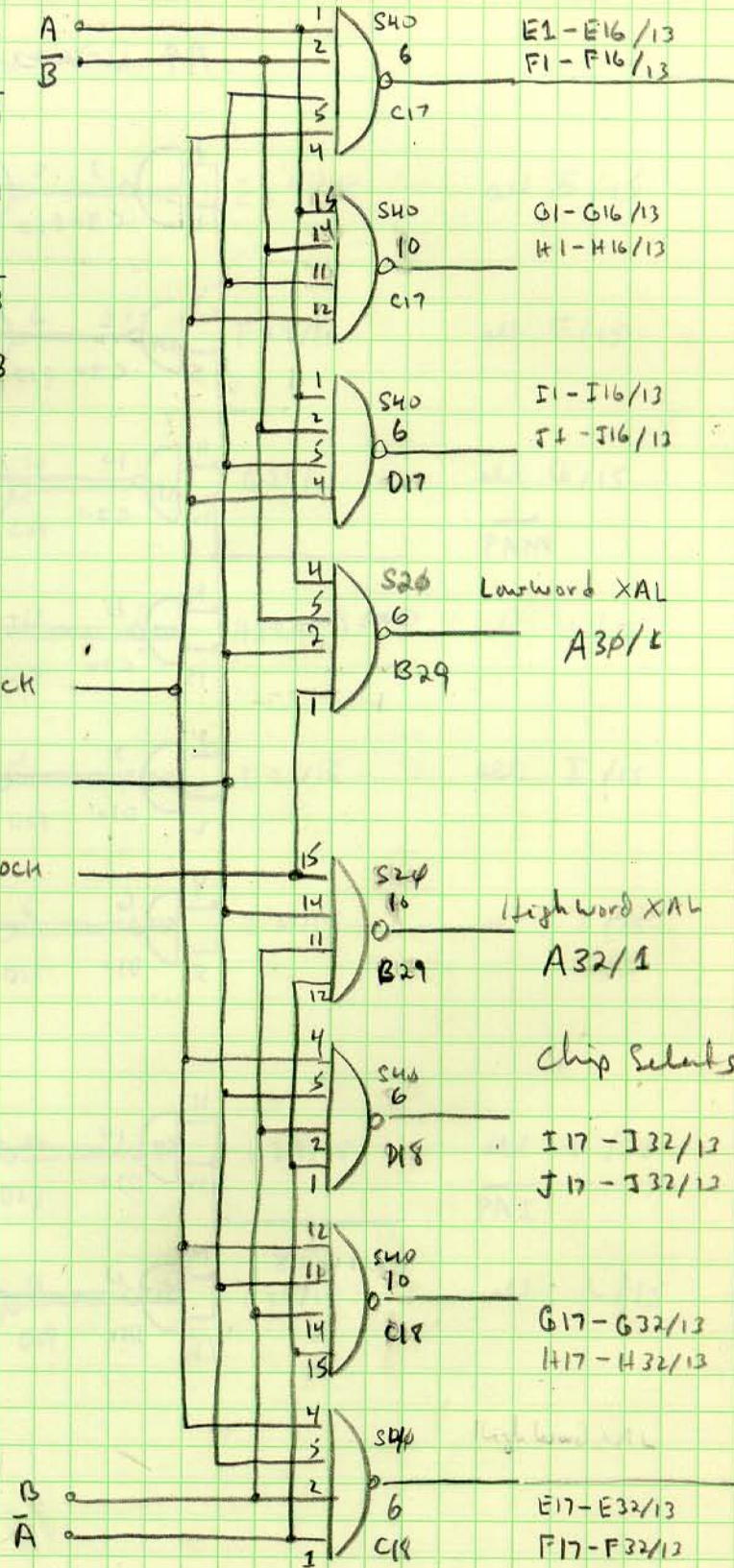


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ABD

Chip Select Logic (Meade)



CN11/16 meclock
 CN12/19 MIDSL
 CN11/29 XACLOCK



Chip Selects

E1-E16/13
F1-F16/13

G1-G16/13
H1-H16/13

I1-I16/13
J1-J16/13

Lowword XAL
A30/4

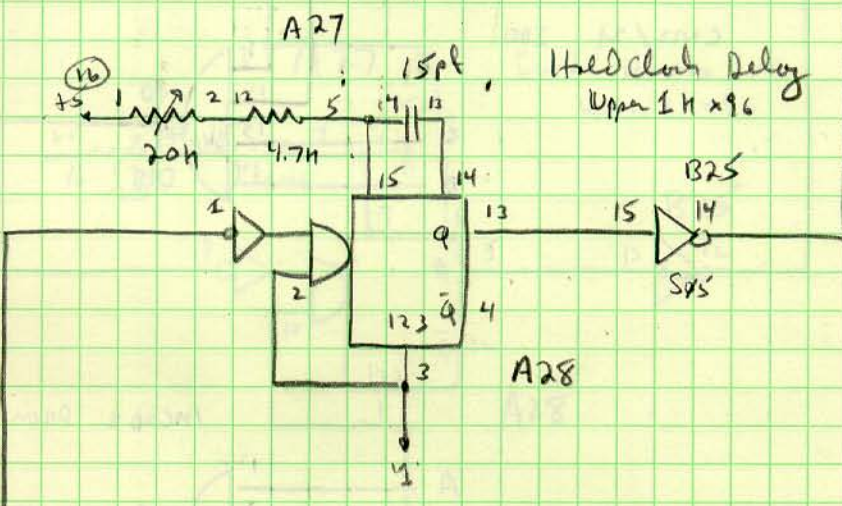
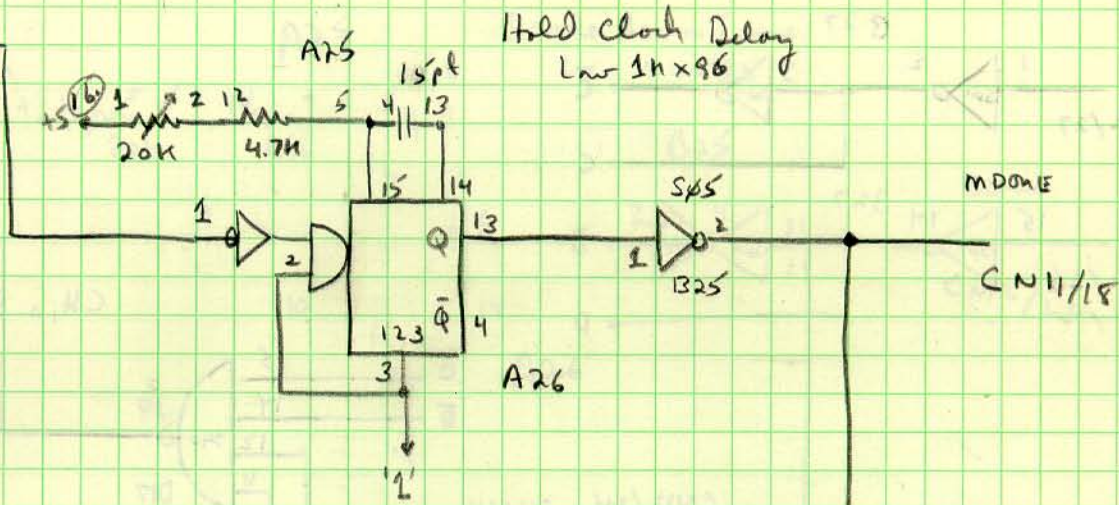
Highword XAL
A32/1

Chip Selects

I17-I32/13
J17-J32/13

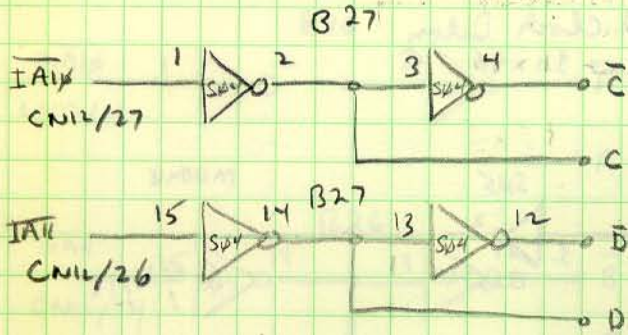
G17-G32/13
H17-H32/13

E17-E32/13
F17-F32/13

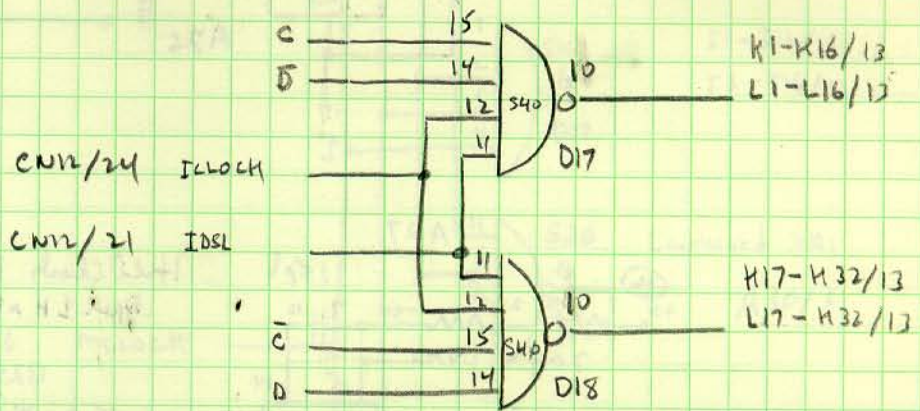


12 Feb 77
ARB

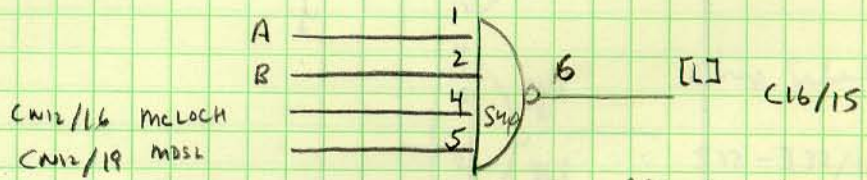
Chip Select Logic (Icode)



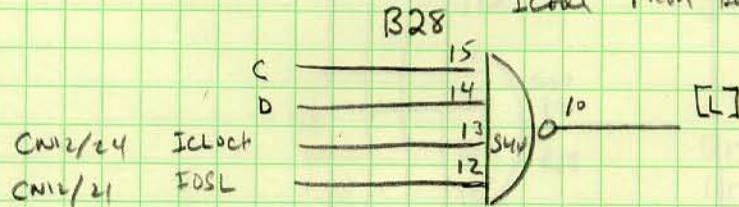
Chip Selects



MCODE PROM Decode

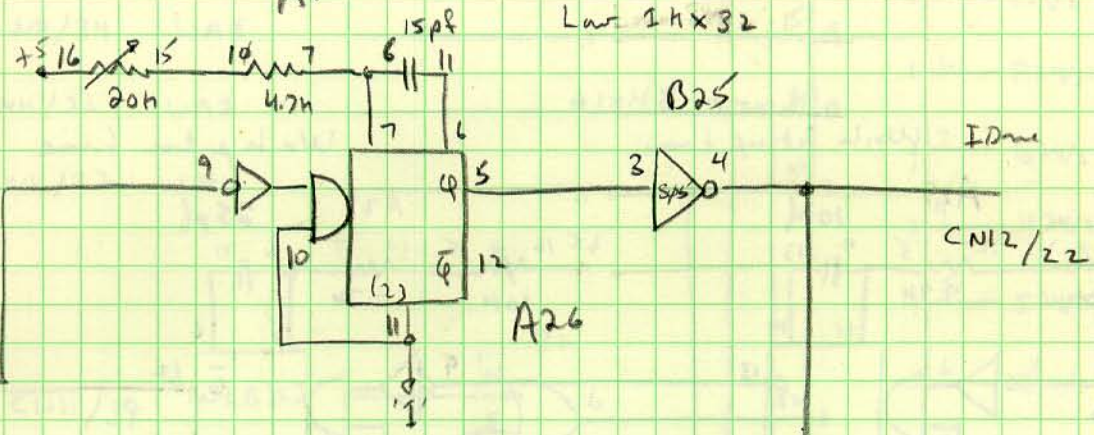


Icode PROM Decode



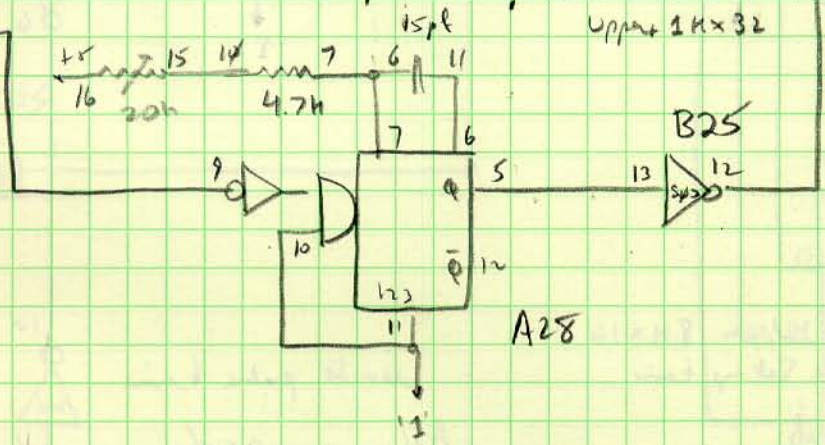
A25

Icode Access Time
Lower 1Kx32



A27

Icode Access Time
Upper 1Kx32



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ARB

Write Pulse Selection 57

C M11/34 WAP
 C N11/33 WA1
 C W11/32 WA2

C N11/39 WLB [L]

C N11/36 WHA [L]

Low Byte



0	1	E7-24/3	E1-24/3
1	2	F24/3	F17-F24/3
2	3	G24/3	G17-G24/3
3	4	H24/3	H17-H24/3
4	5	I24/3	I17-I24/3
5	6	J24/3	J17-J24/3
6	7	K24/3	K17-K24/3
7	8	L24/3	L17-L24/3
8	9		L18/3

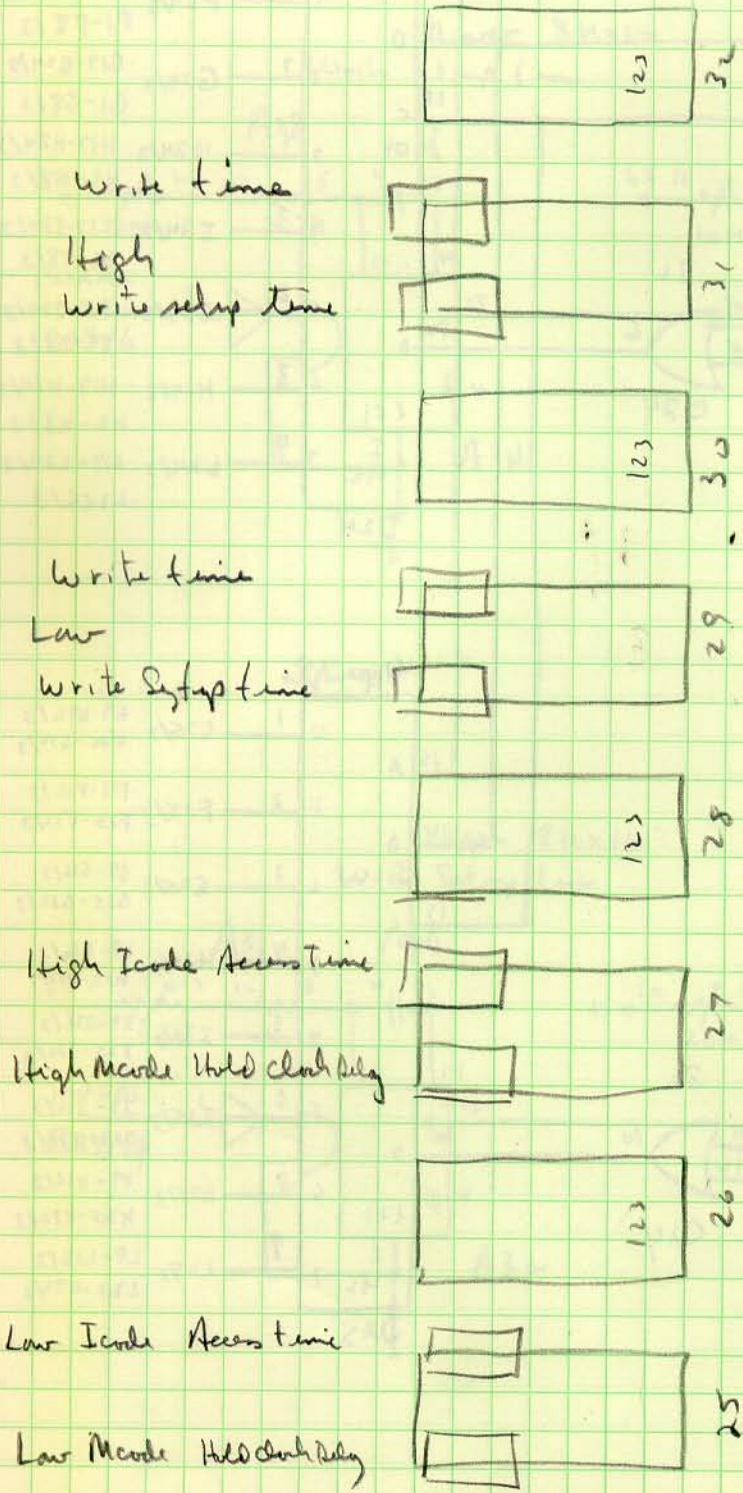
Upper Byte



0	1	E25/3	E17-E25/3
1	2	F25/3	F17-F25/3
2	3	G25/3	G17-G25/3
3	4	H25/3	H17-H25/3
4	5	I25/3	I17-I25/3
5	6	J25/3	J17-J25/3
6	7	K25/3	K17-K25/3
7	8	L25/3	L17-L25/3
8	9		L25-L32/3

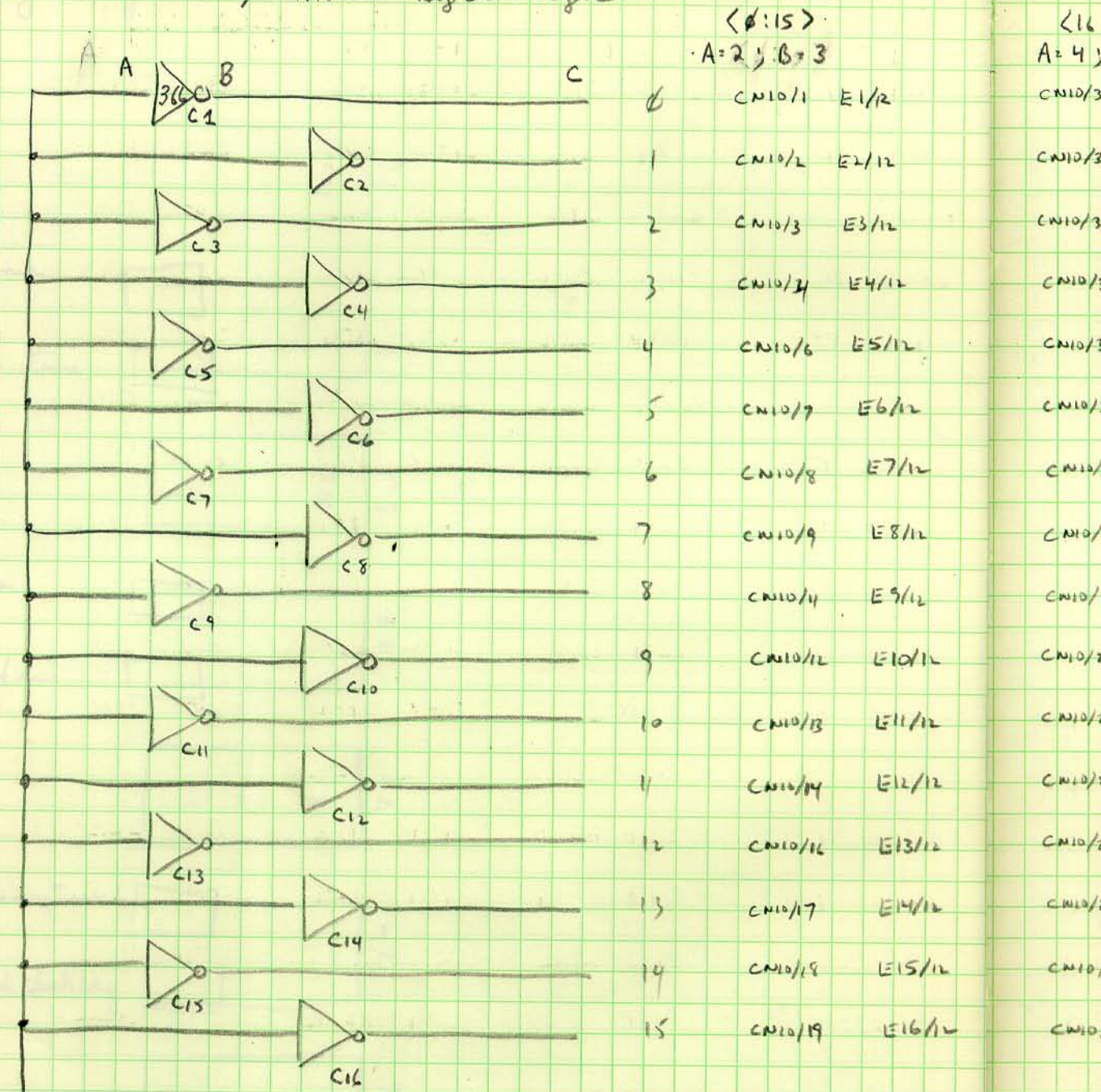
12 Feb 77
 ARJ

Timing Adjustment Locations



A

Microcode Connections / Tristate Highlevel Logic



Line	Component	Input	Output
0	CN10/1	E1/12	CN10/3
1	CN10/2	E2/12	CN10/3
2	CN10/3	E3/12	CN10/3
3	CN10/4	E4/12	CN10/3
4	CN10/6	E5/12	CN10/3
5	CN10/7	E6/12	CN10/3
6	CN10/8	E7/12	CN10/3
7	CN10/9	E8/12	CN10/3
8	CN10/11	E9/12	CN10/3
9	CN10/12	E10/12	CN10/2
10	CN10/13	E11/12	CN10/2
11	CN10/14	E12/12	CN10/2
12	CN10/16	E13/12	CN10/2
13	CN10/17	E14/12	CN10/2
14	CN10/18	E15/12	CN10/2
15	CN10/19	E16/12	CN10/2

Tristate enabled (For 366's)

B28/6

MCODE PRAM Decode

[L]

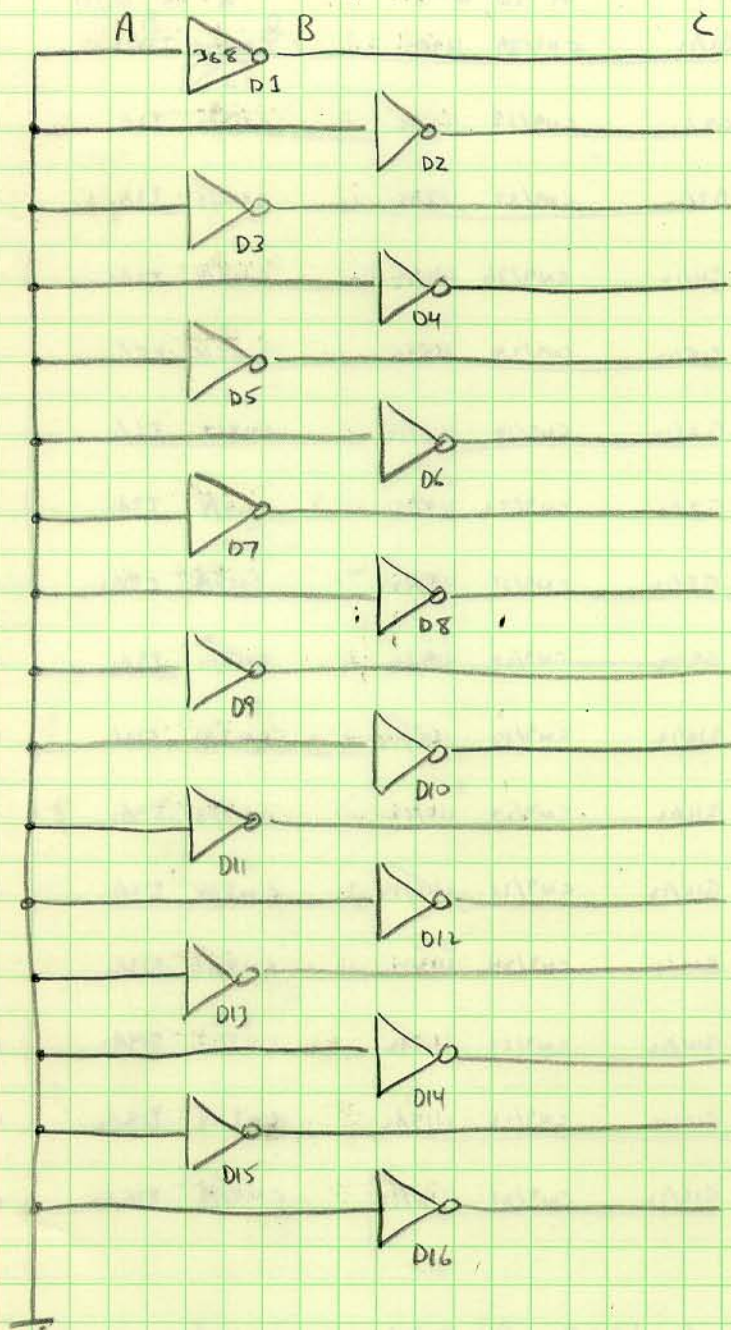
C16/15

all C1-C16/15

Connections for Micro Tri-stale

$\langle 16:31 \rangle$ A=4; B=5	$\langle 32:47 \rangle$ A=6; B=7	$\langle 48:63 \rangle$ A=10; B=9	$\langle 64:79 \rangle$ A=12; B=11	$\langle 80:95 \rangle$ A=14; B=13
CN10/39 F1/12	CN9/1 G1/12	CN9/39 H1/12	CN8/1 I1/12	CN8/39 J1/12
CN10/38 F2/12	CN9/2 G2/12	CN9/38 H2/12	CN8/2 I2/12	CN8/38 J2/12
CN10/37 F3/12	CN9/3 G3/12	CN9/37 H3/12	CN8/3 I3/12	CN8/37 J3/12
CN10/36 F4/12	CN9/4 G4/12	CN9/36 H4/12	CN8/4 I4/12	CN8/36 J4/12
CN10/34 F5/12	CN9/6 G5/12	CN9/34 H5/12	CN8/6 I5/12	CN8/34 J5/12
CN10/33 F6/12	CN9/7 G6/12	CN9/33 H6/12	CN8/7 I6/12	CN8/33 J6/12
CN10/32 F7/12	CN9/8 G7/12	CN9/32 H7/12	CN8/8 I7/12	CN8/32 J7/12
CN10/31 F8/12	CN9/9 G8/12	CN9/31 H8/12	CN8/9 I8/12	CN8/31 J8/12
CN10/29 F9/12	CN9/11 G9/12	CN9/29 H9/12	CN8/11 I9/12	CN8/29 J9/12
CN10/28 F10/12	CN9/12 G10/12	CN9/28 H10/12	CN8/12 I10/12	CN8/28 J10/12
CN10/27 F11/12	CN9/13 G11/12	CN9/27 H11/12	CN8/13 I11/12	CN8/27 J11/12
CN10/26 F12/12	CN9/14 G12/12	CN9/26 H12/12	CN8/14 I12/12	CN8/26 J12/12
CN10/24 F13/12	CN9/16 G13/12	CN9/24 H13/12	CN8/16 I13/12	CN8/24 J13/12
CN10/23 F14/12	CN9/17 G14/12	CN9/23 H14/12	CN8/17 I14/12	CN8/23 J14/12
CN10/22 F15/12	CN9/18 G15/12	CN9/22 H15/12	CN8/18 I15/12	CN8/22 J15/12
CN10/21 F16/12	CN9/19 G16/12	CN9/21 H16/12	CN8/19 I16/12	CN8/21 J16/12

Icode Connections / Tristate Negatable Logic



Icode PROM Decoder
[L]

B28/10

D16/15

Connections for Icode

<96:111>

A = 12; B = 11

CN7/1 H1/12

CN7/2 H2/12

CN7/3 H3/12

CN7/4 H4/12

CN7/6 H5/12

CN7/7 H6/12

CN7/8 H7/12

CN7/9 H8/12

CN7/10 H9/12

CN7/12 H10/12

CN7/13 H11/12

CN7/14 H12/12

CN7/16 H13/12

CN7/17 H14/12

CN7/18 H15/12

CN7/19 H16/12

<112:127>

A = 14; B = 13

CN7/39 L1/12

CN7/38 L2/12

CN7/37 L3/12

CN7/36 L4/12

CN7/34 L5/12

CN7/33 L6/12

CN7/32 L7/12

CN7/31 L8/12

CN7/29 L9/12

CN7/28 L10/12

CN7/27 L11/12

CN7/26 L12/12

CN7/24 L13/12

CN7/23 L14/12

CN7/22 L15/12

CN7/21 L16/12

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ARQ

ORGANIZATION

D24/1 LB4

D24/2 LB1

D24/3 LB2

D24/4 LB3

D24/5 LB4

D24/6 LB5

D24/7 LB6

D24/9 LB7

D24/9 LB7

D24/7 LB6

D24/6 LB5

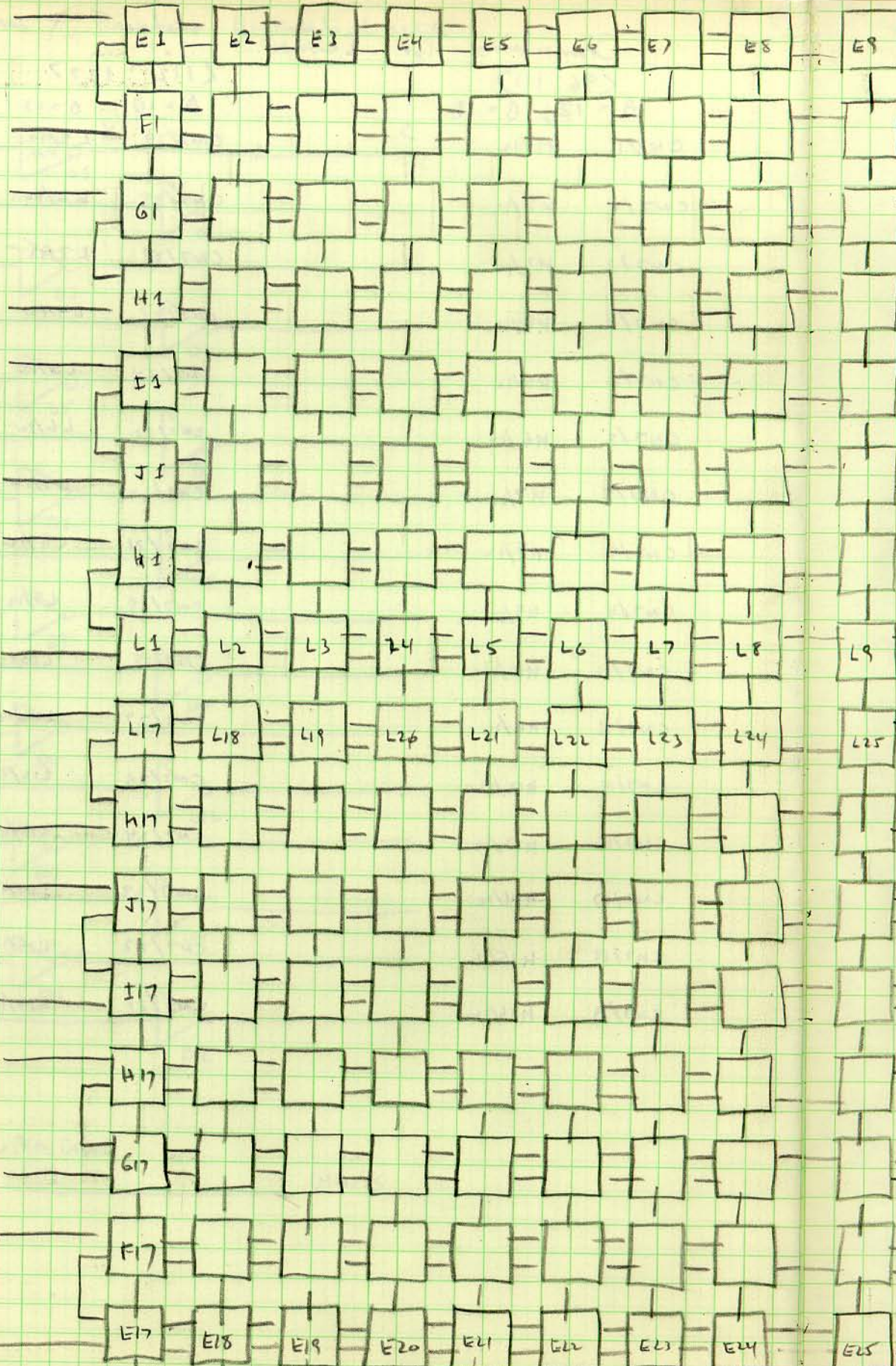
D24/5 LB4

D24/4 LB3

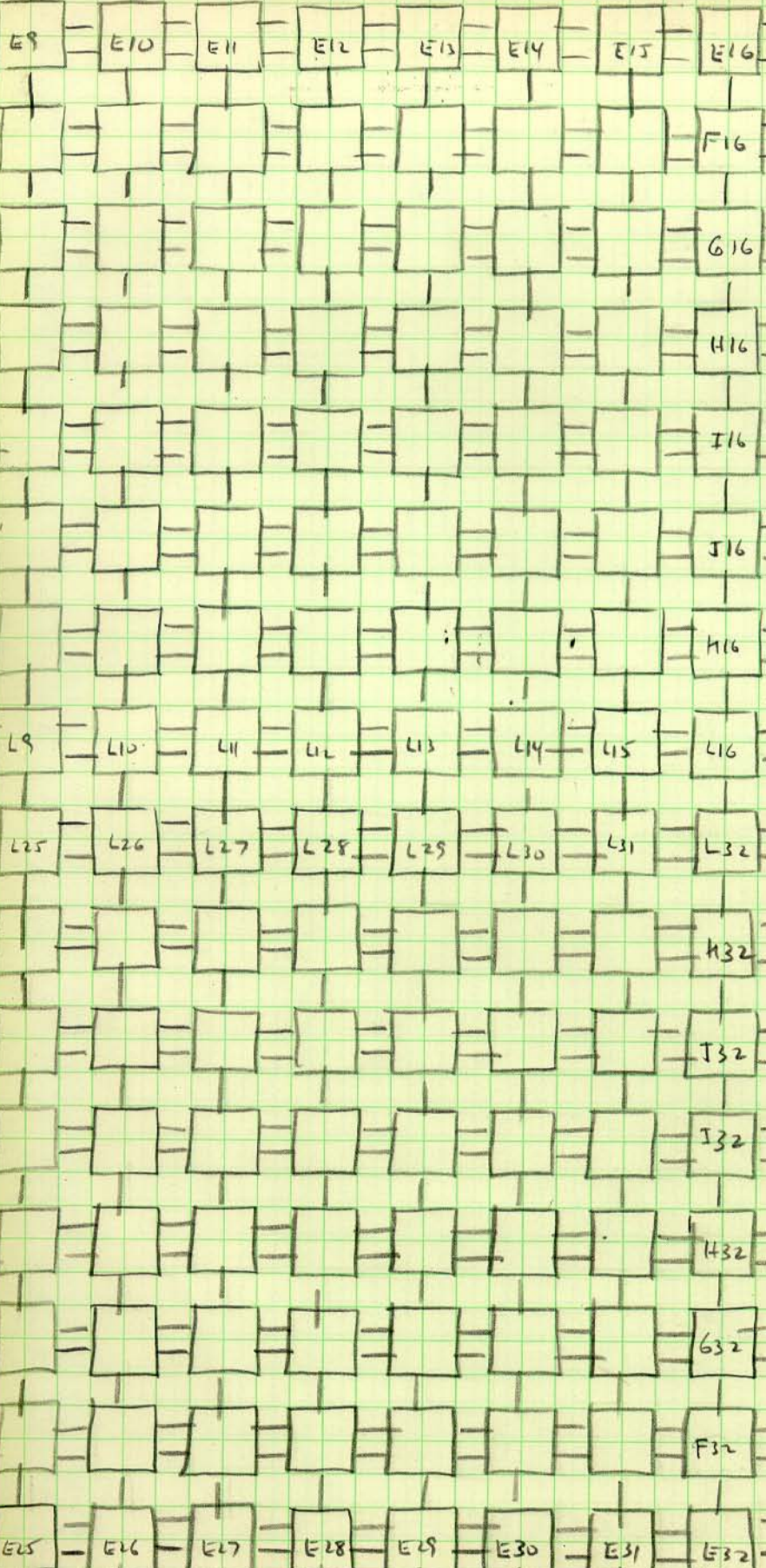
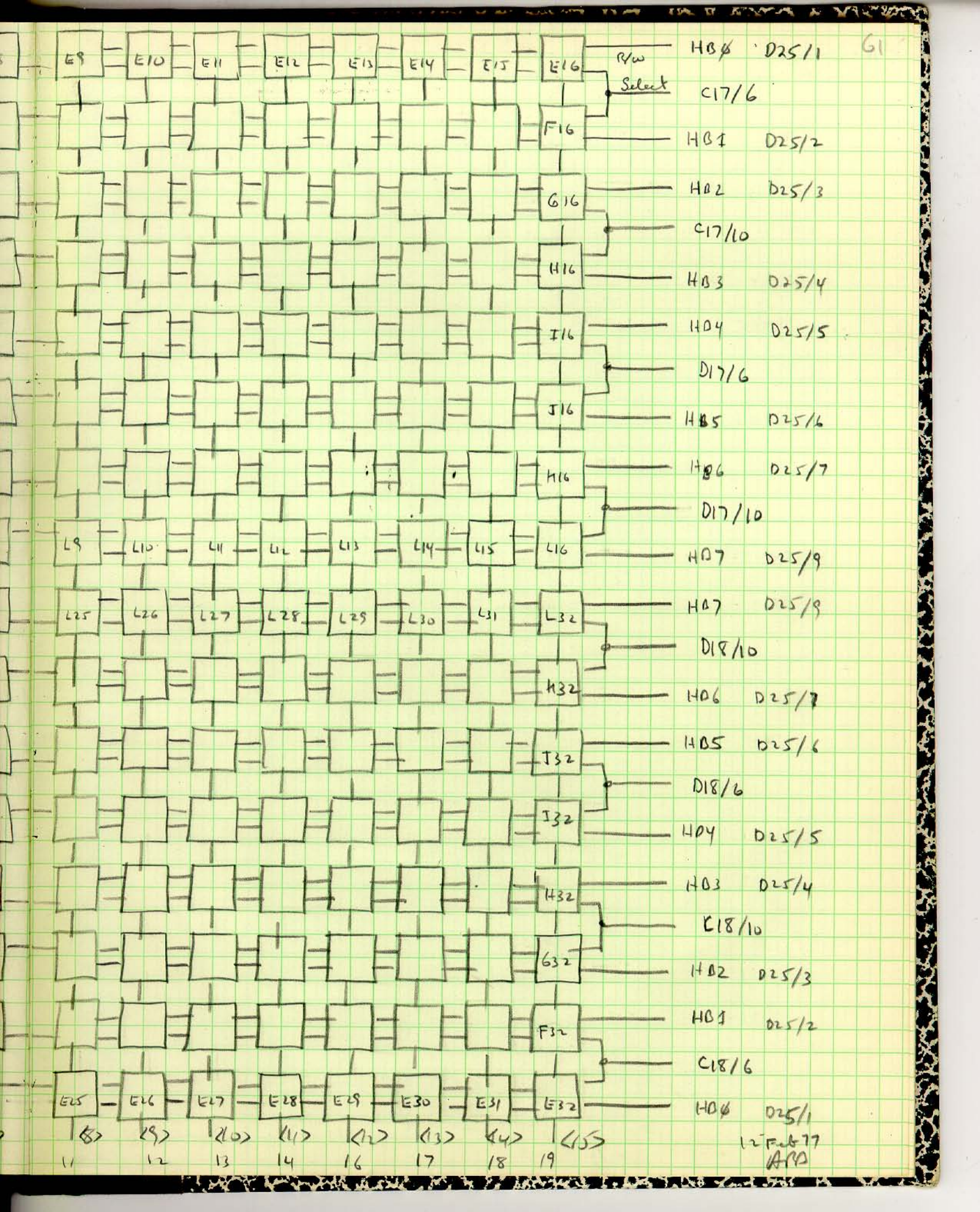
D24/3 LB2

D24/2 LB1

D24/1 LB4



CN11 1 2 3 4 6 7 8 9 11



Row Select
 H01 D25/1
 C17/6
 H02 D25/2
 H02 D25/3
 C17/10
 H03 D25/4
 H04 D25/5
 D17/6
 H05 D25/6
 H06 D25/7
 D17/10
 H07 D25/9
 H07 D25/9
 D18/10
 H06 D25/8
 H05 D25/6
 D18/6
 H04 D25/5
 H03 D25/4
 E18/10
 H02 D25/3
 H01 D25/2
 C18/6
 H06 D25/1

<8> <9> <10> <11> <12> <13> <14> <15>
 11 12 13 14 16 17 18 19

12 FEB 77
 APD

64K Dynamic Memory Board

63

two groups of 32K x 16 Bit RAM
using 4K x 1 dynamics

20 Nov 78
ABD

Connector Wiring Rev. Frame 4 9

CN1 & CN3

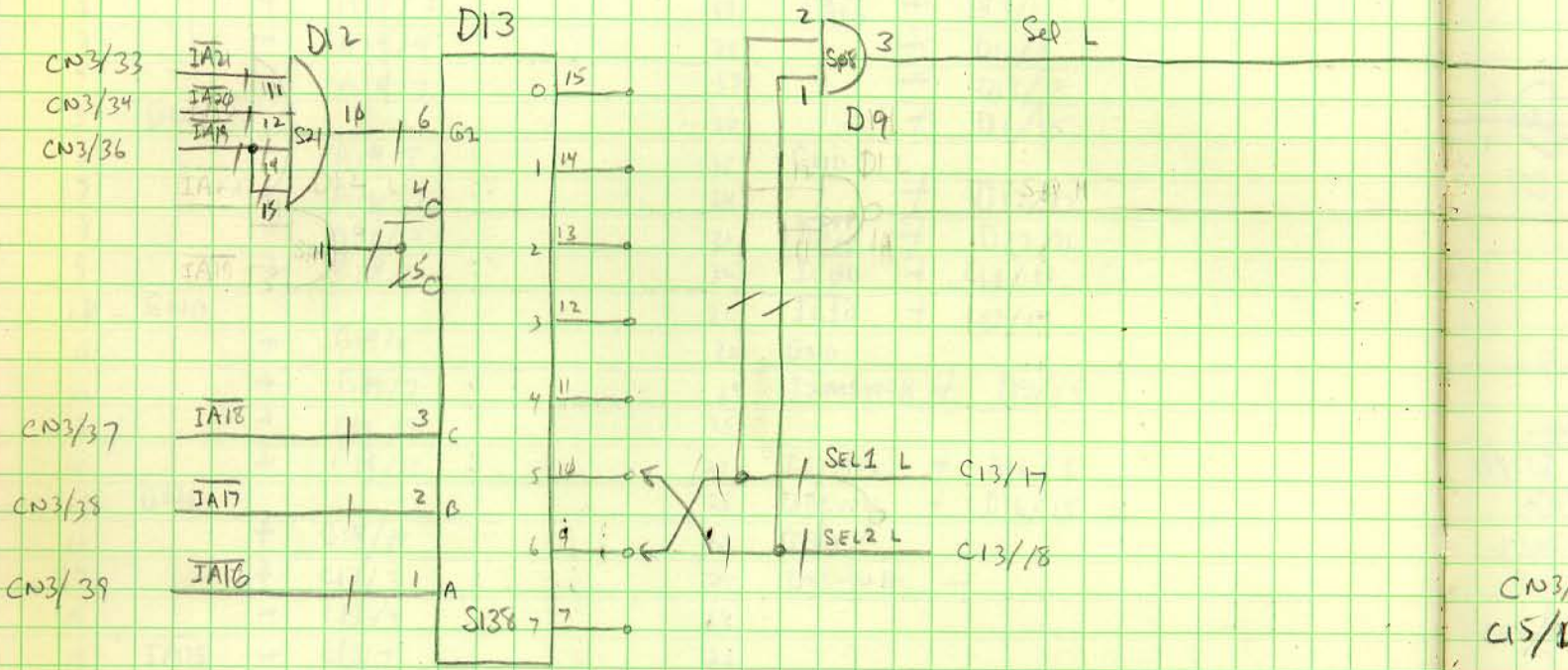
Internal Address Plus Control

1	IAD	+	C13/8	40	GND		
2		+	A14/3	39	IAT6	+	D13/1
3		+	A14/4	38		+	D13/2
4		+	A14/7	37		+	D13/3
5	GND			36		+	D2/15
6		+	A14/8	35	GND		
7		+	A14/13	34		+	D12/12
8		+	A14/14	33	IAR1	+	D12/11
9		+	B14/3	32	ICPD	+	C13/13
10	GND			31	IC1D	+	C13/14
11		+	B14/4	30	GND		
12		+	B14/7	29	IXMSYNH	+	D9/15
13		+	B14/8	28			
14		+	B14/13	27	ISSYNL	+	D16/1
15	GND			26	UBSYNL	+	D16/15
16		+	B14/14	25	GND		
17		+	C13/3	24	IMSYNH	-	
18		+	C13/4	23			
19	IAT5	+	C13/7	22			
20	GND			21	INIT CLR/ALH	-	

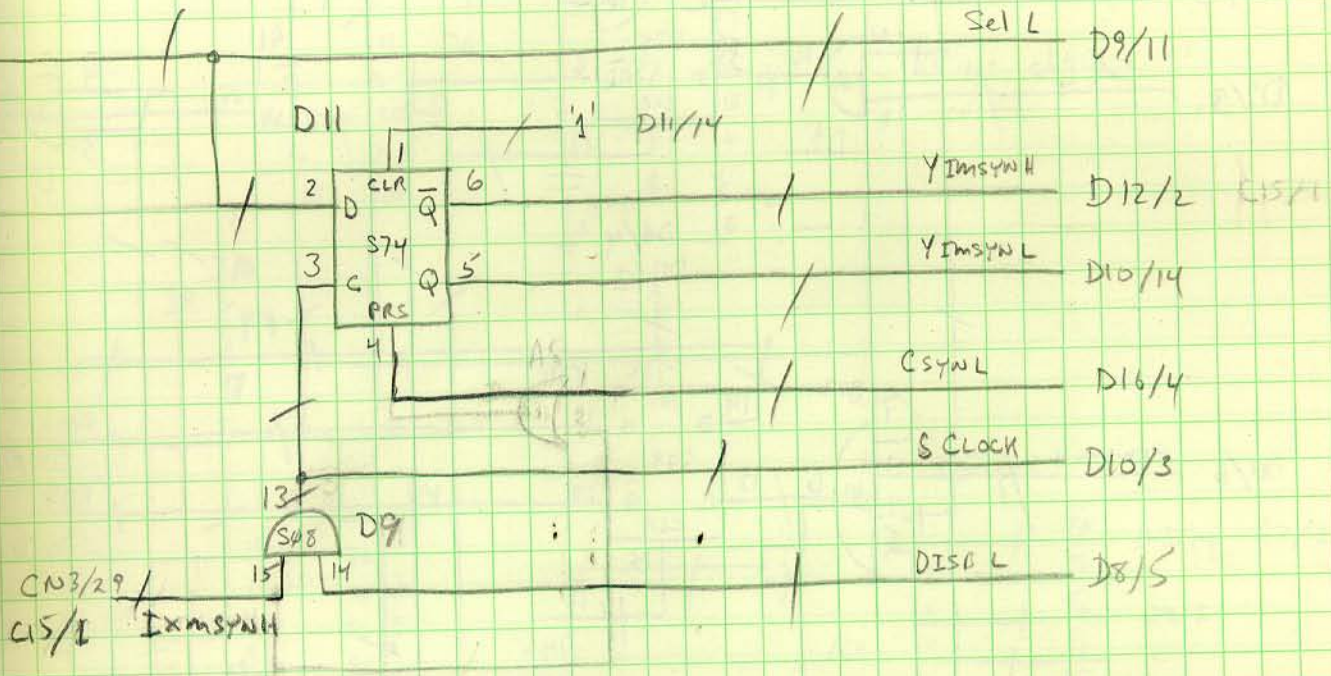
CN2 & CN4

1	DIP	+	A13/18	40	GND		
2		+	A13/16	39	DO1	+	A15/13
3		+	A13/14	38		+	A15/14
4		+	A13/12	37		+	A15/7
5	GND			36		+	A15/8
6		+	A13/9	35	GND		
7		+	A13/7	34		+	A15/13
8		+	A13/5	33		+	A15/14
9		+	A13/3	32		+	A15/17
10	GND			31		+	A15/18
11		+	B13/18	30	GND		
12		+	B13/16	29		+	B15/3
13		+	B13/14	28		+	B15/4
14		+	B13/12	27		+	B15/7
15	GND			26		+	B15/8
16		+	B13/9	25	GND		
17		+	B13/7	24		+	B15/13
18		+	B13/5	23		+	B15/14
19	DIS	+	B13/3	22		+	B15/17
20	GND			21	DOIS	+	B15/18

Address Select Logic

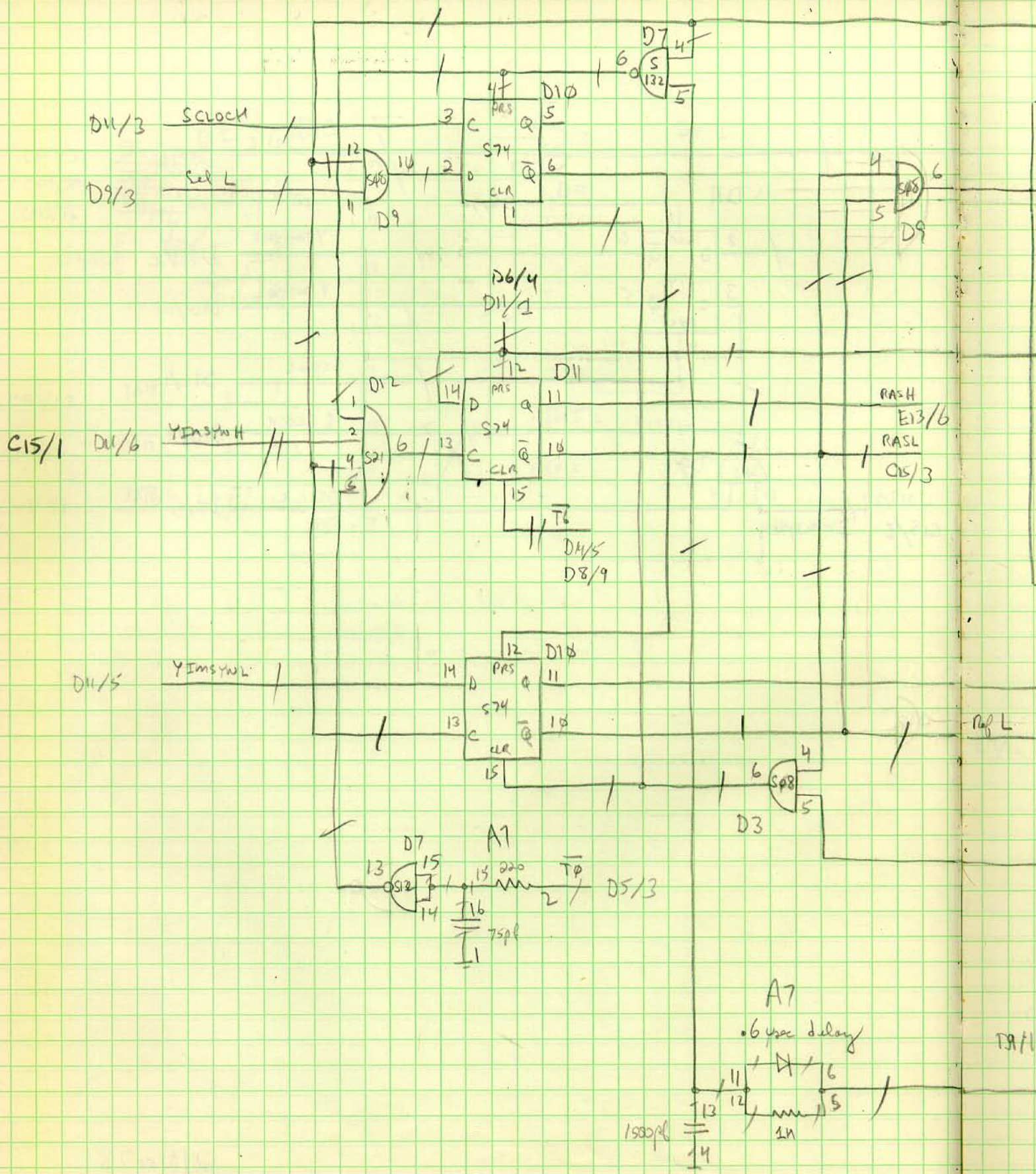


CN3/
C15/1

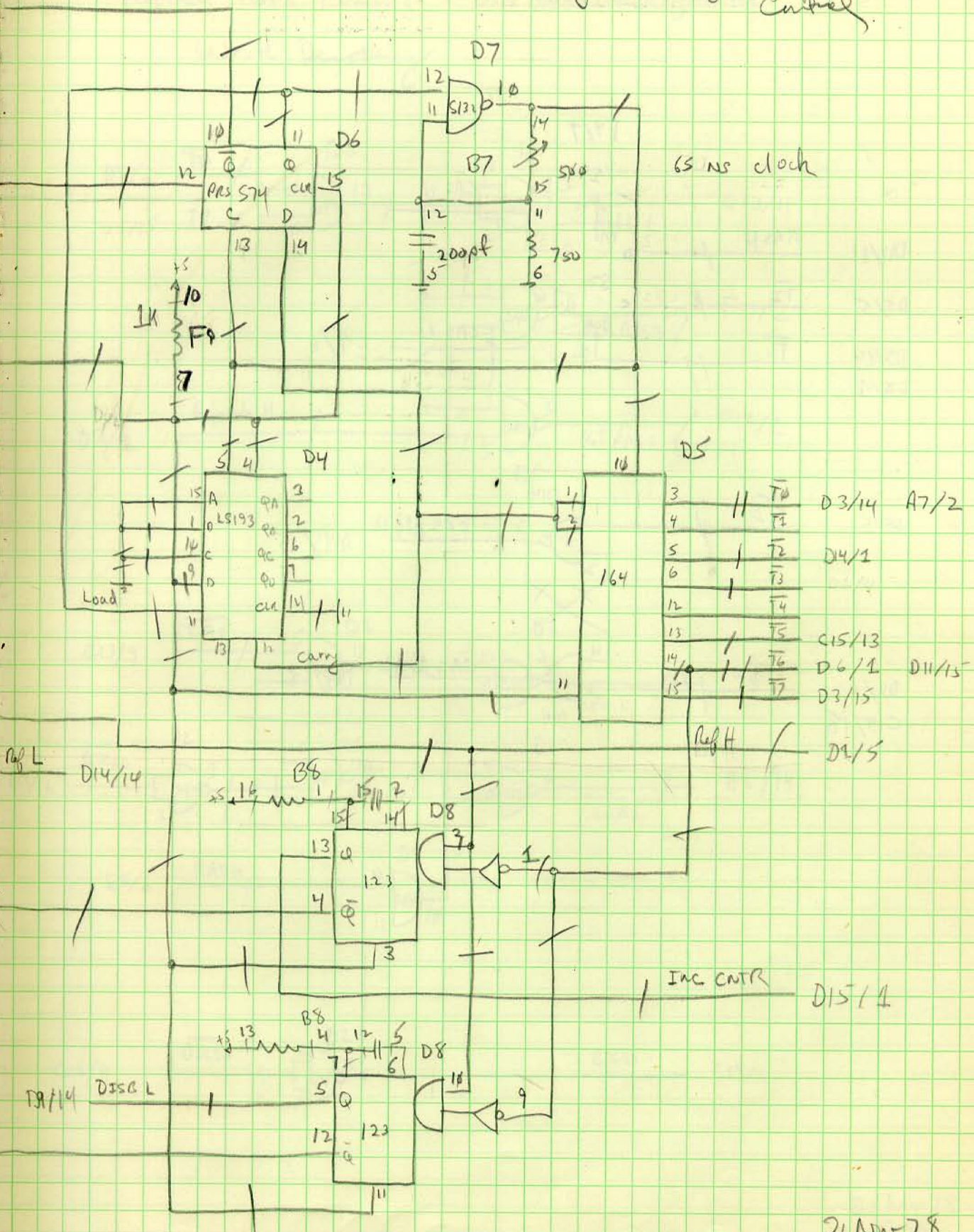


*Model...
...*

21 Nov 78
Apo

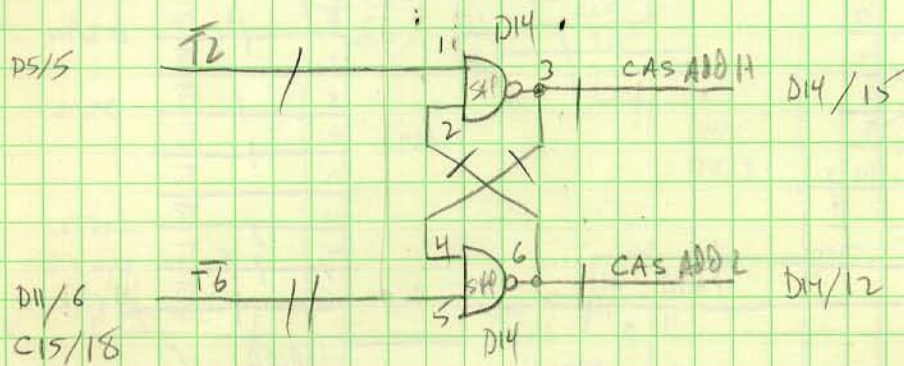
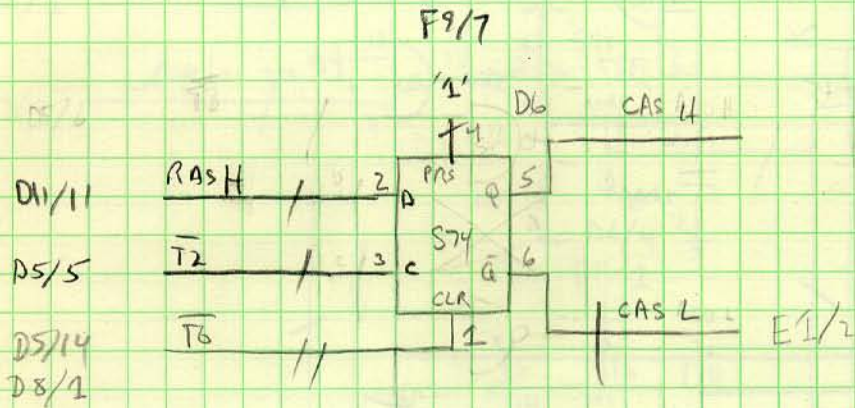


Memory Timing & Refresh Control

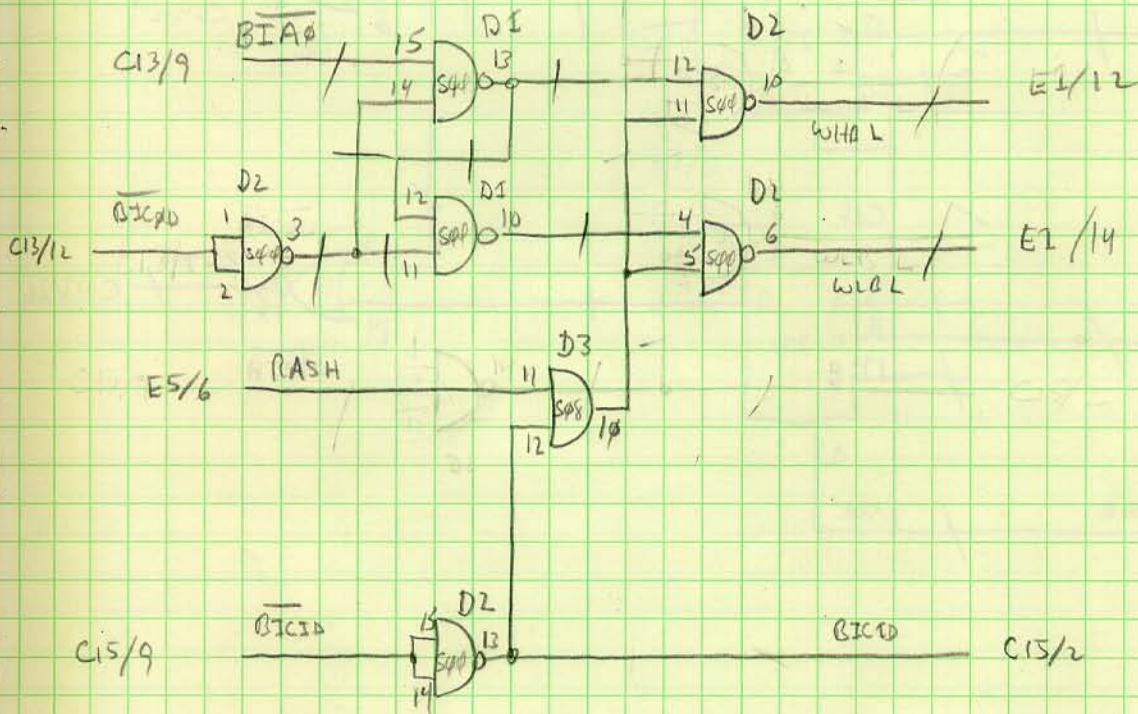
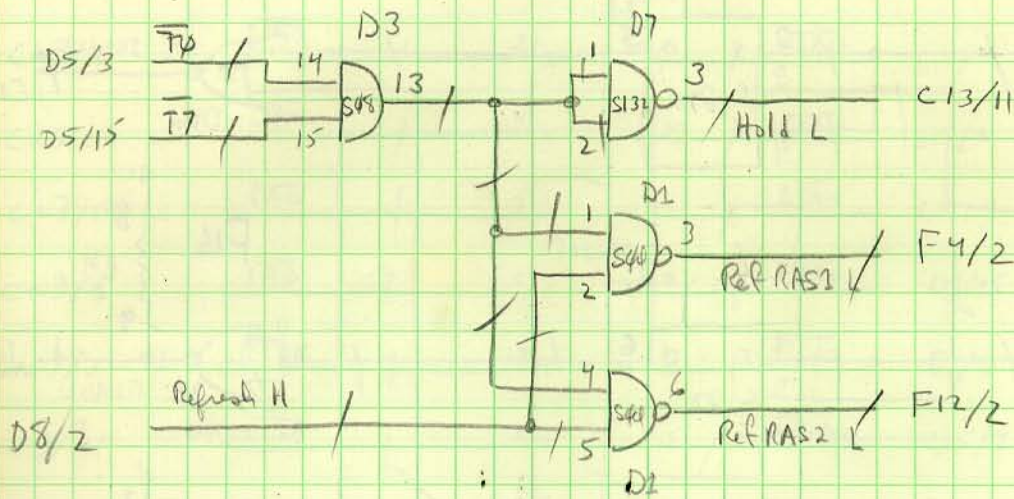


21 Nov 78
APP

CAS Timing Generator

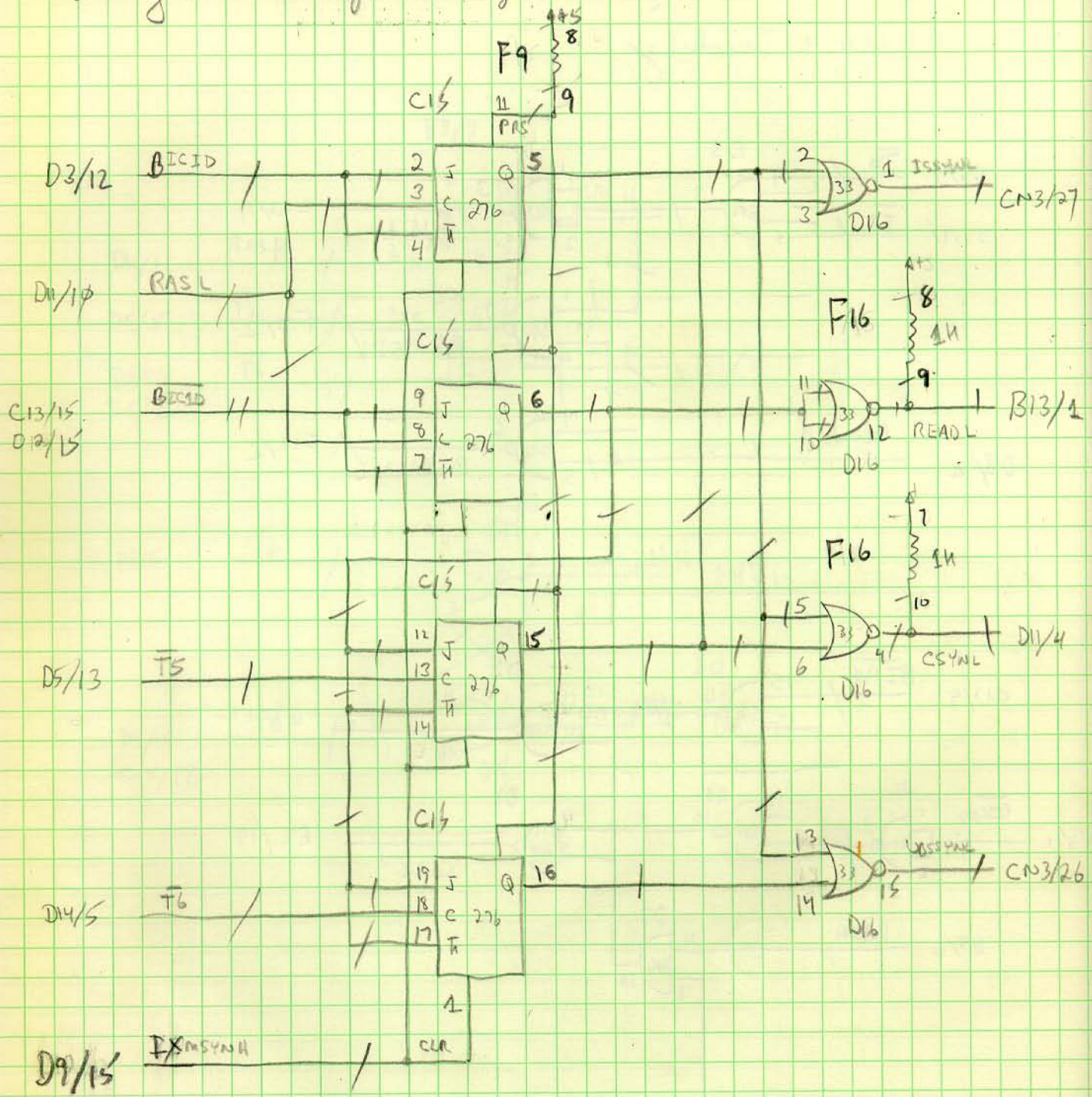


Refresh RAS Timing Data, Address Hold timing Write Decoding



21 Nov 78
RBB

Memory BUS Response Logic



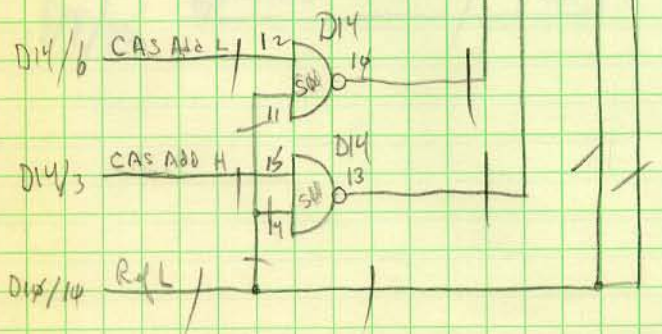
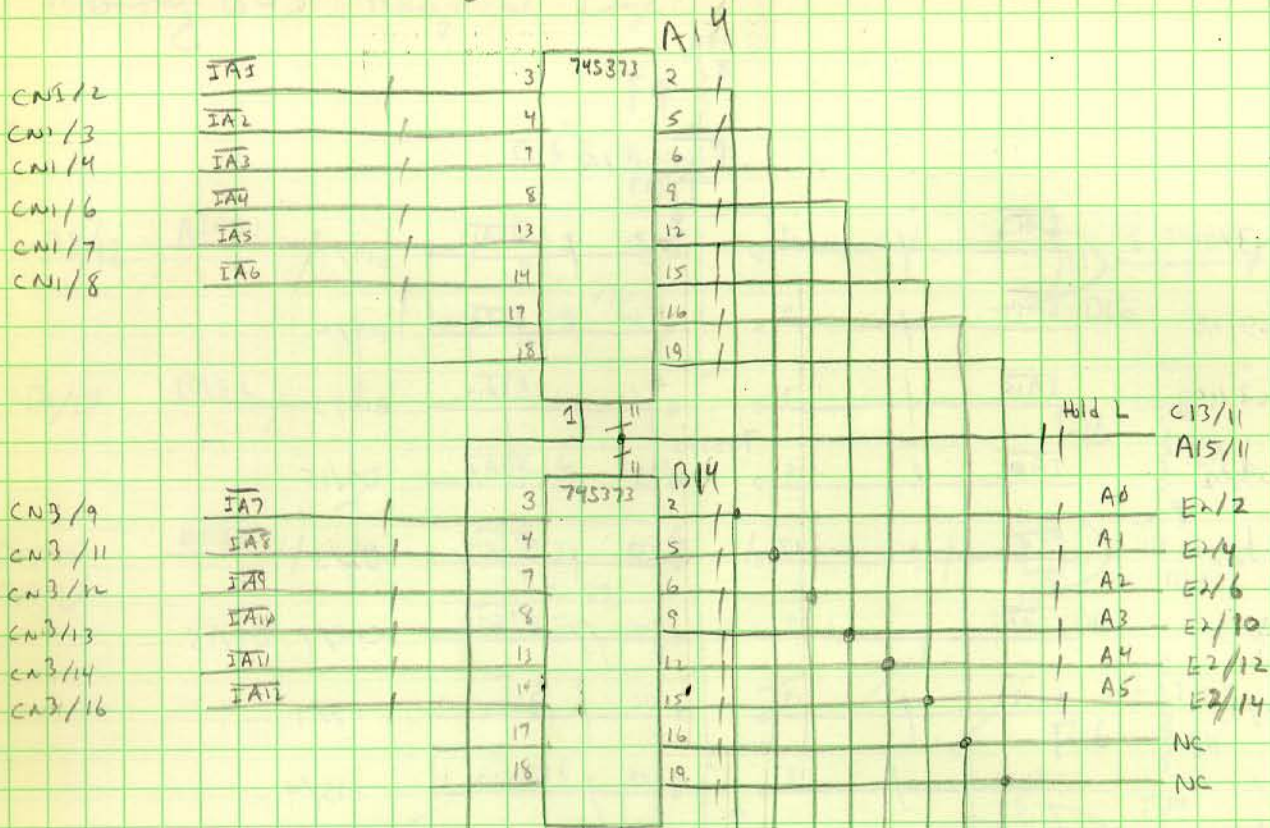
C13

CN3/17	$\overline{IA13}$	/	3	D	Q	2	/	$\overline{BIA13}$	E13/1
CN3/18	$\overline{IA14}$	/	4	D	Q	5	/	$\overline{BIA14}$	E13/2
CN3/19	$\overline{IA15}$	/	7	D	Q	6	/	$\overline{BIA15}$	E13/3
CN3/2	$\overline{IA\phi}$	/	8	D	Q	9	/	$\overline{BIA\phi}$	D2/15
CN3/32	$\overline{IC\phi D}$	/	13	D	Q	12	/	$\overline{BIC\phi D}$	D2/3
CN3/31	$\overline{IC10}$	/	14	D	Q	15	/	$\overline{BIC10}$	C15/7 D2/15
D9/2	SEL1 L	/	17	D	Q	16	/	BSEL1 L	E5/4
D9/1	SEL2 L	/	18	D	Q	19	/	BSEL2 L	E13/4

74S373
 Hold L
 D7/3
 B14/11

22 Nov 78
 ARB

Address multiplexing



A15

CN2/39	$\overline{D00}$	/	3	S373	2	/	$\overline{B00}$	G16/2
CN2/35	$\overline{D01}$	/	4		5	/	$\overline{B01}$	H16/2
CN2/37	$\overline{D02}$	/	7		6	/	$\overline{B02}$	I16/2
CN2/36	$\overline{D03}$	/	8		9	/	$\overline{B03}$	J16/2
CN2/34	$\overline{D04}$	/	13		12	/	$\overline{B04}$	K16/2
CN2/33	$\overline{D05}$	/	14		15	/	$\overline{B05}$	L16/2
CN2/32	$\overline{D06}$	/	17		16	/	$\overline{B06}$	M16/2
CN2/31	$\overline{D07}$	/	18		19	/	$\overline{B07}$	N16/2

11	1
----	---

B15

CN4/29	$\overline{D08}$	/	3	S373	2	/	$\overline{B08}$	O16/2
CN4/28	$\overline{D09}$	/	4		5	/	$\overline{B09}$	P16/2
CN4/27	$\overline{D10}$	/	7		6	/	$\overline{B10}$	Q16/2
CN4/26	$\overline{D11}$	/	8		9	/	$\overline{B11}$	R16/2
CN4/24	$\overline{D12}$	/	13		12	/	$\overline{B12}$	S16/2
CN4/23	$\overline{D13}$	/	14		15	/	$\overline{B13}$	T16/2
CN4/22	$\overline{D14}$	/	17		16	/	$\overline{B14}$	U16/2
CN4/21	$\overline{D15}$	/	18		19	/	$\overline{B15}$	V16/2

11	1
----	---

Hold L

Output Data BUS Drivers

A13

CN2/1	D10	/	18	S240	2	$\overline{RD8}$
CN2/2	D12	/	16		4	$\overline{RD1}$
CN2/3	D12	/	14		6	$\overline{RD2}$
CN2/4	D13	/	12		8	$\overline{RD3}$
CN2/6	D14	/	9		11	$\overline{RD4}$
CN2/7	D15	/	7		13	$\overline{RD5}$
CN2/8	D16	/	5		15	$\overline{RD6}$
CN2/9	D17	/	3		17	$\overline{RD7}$

1 | 19

B13

CN4/11	D18	/	18	S240	2	$\overline{RD8}$
CN4/12	D19	/	16		4	$\overline{RD9}$
CN4/13	D110	/	14		6	$\overline{RD10}$
CN4/14	D111	/	12		8	$\overline{RD11}$
CN4/16	D112	/	9		11	$\overline{RD12}$
CN4/17	D113	/	7		13	$\overline{RD13}$
CN4/18	D114	/	5		15	$\overline{RD14}$
CN4/19	D115	/	3		17	$\overline{RD15}$

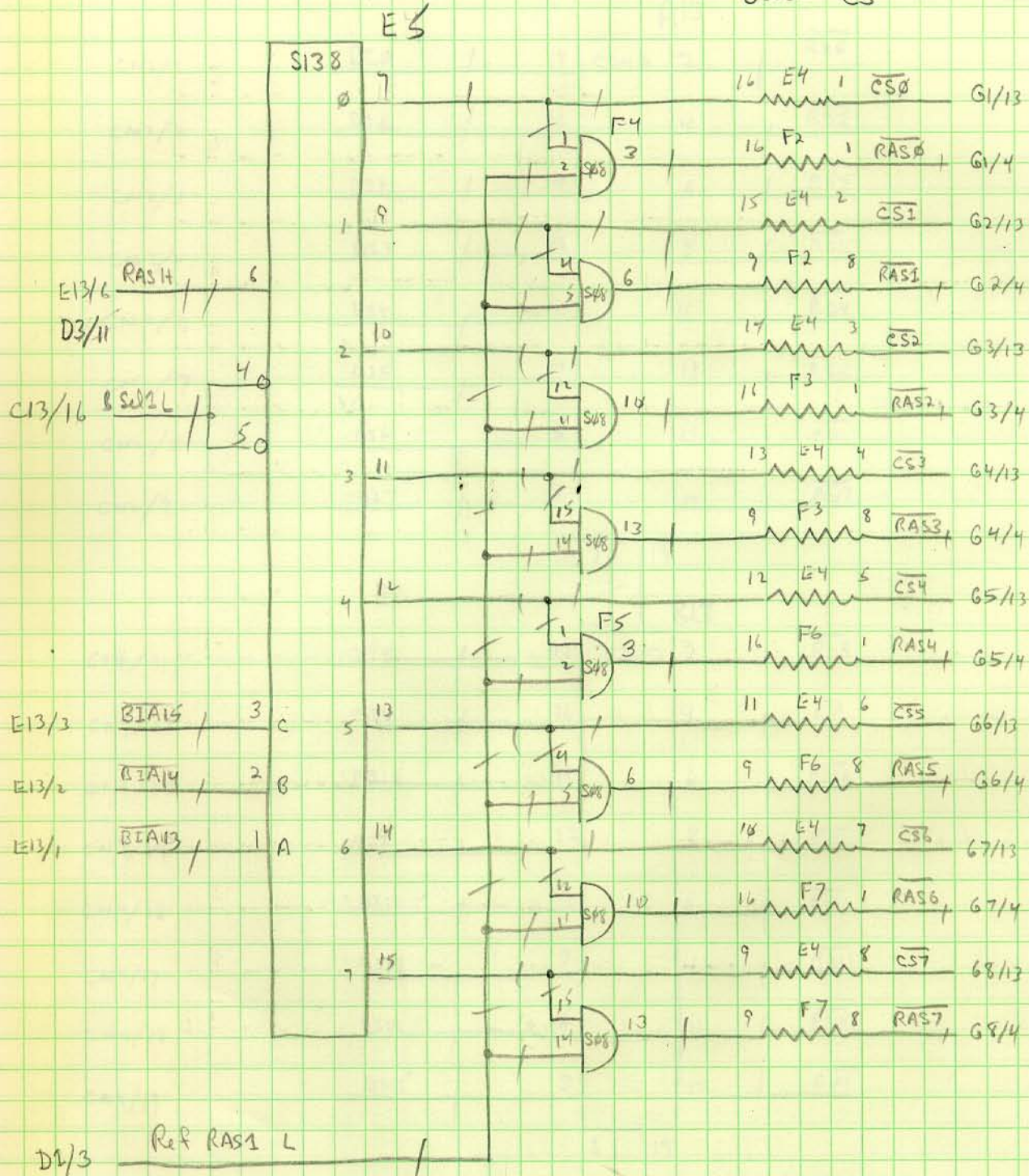
1 | 19

D16/12 Read L /

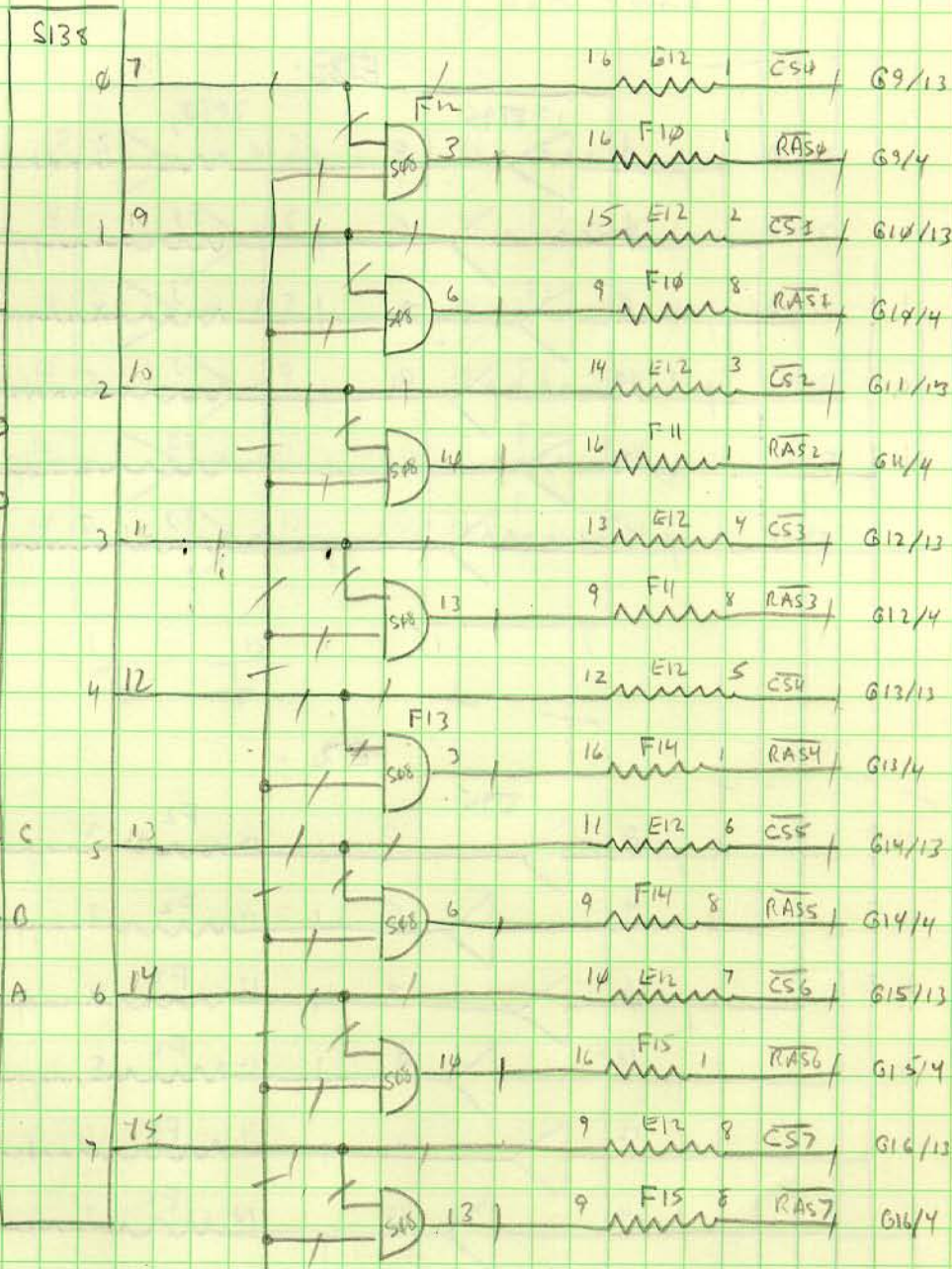
Memory RAS Select Decoding

BANK 1

562L - RAS
562L - CS



E13



ES/6 RASH // 6
DN/11

C13/19 BSEL2 L // 4
S0

C13/6 ES/3 BIAS // 3 C

C13/5 ES/2 BIAS // 2 D

C13/2 ES/1 BIAS // 1 A

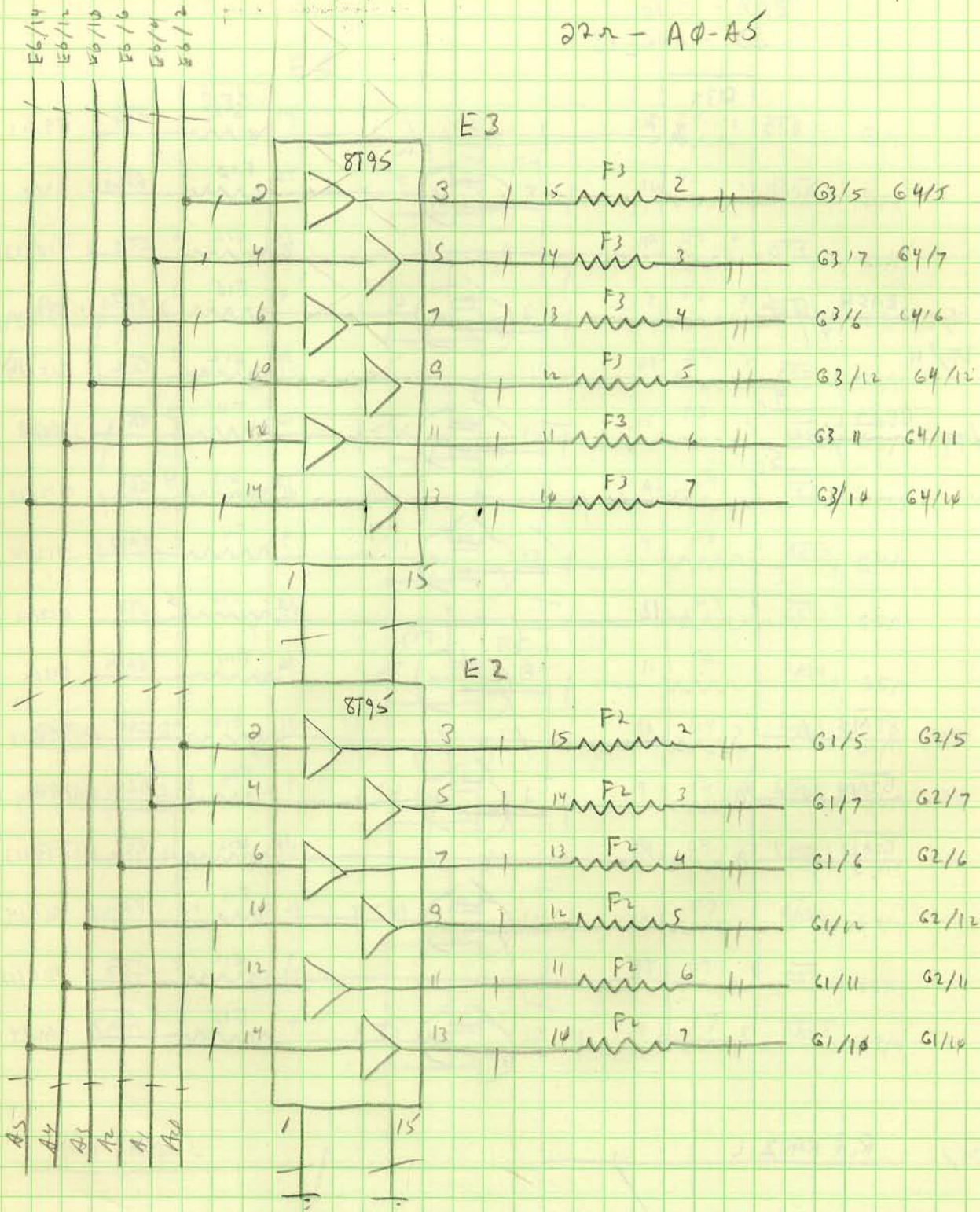
D1/6 R.F RAS2 L

23 Nov 78
ARD

16 K Block ϕ

Address Drivers

222 - A ϕ -A5



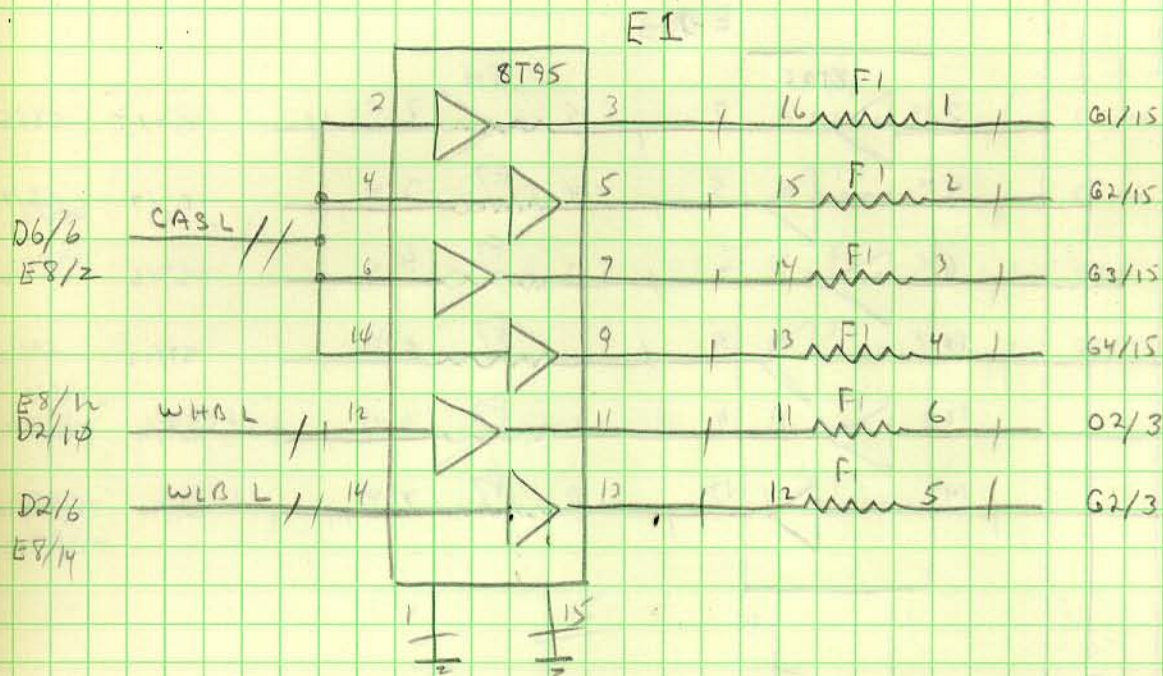
D6/6
E8/1

E8/1
D2/11

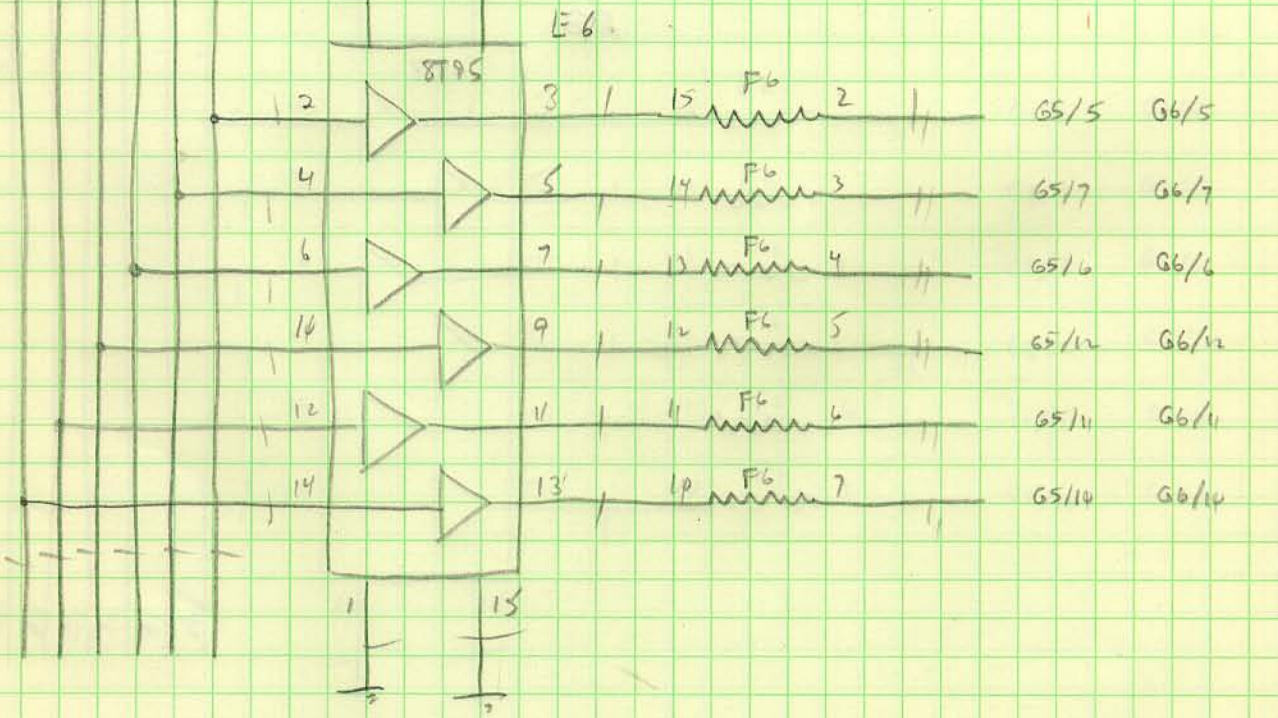
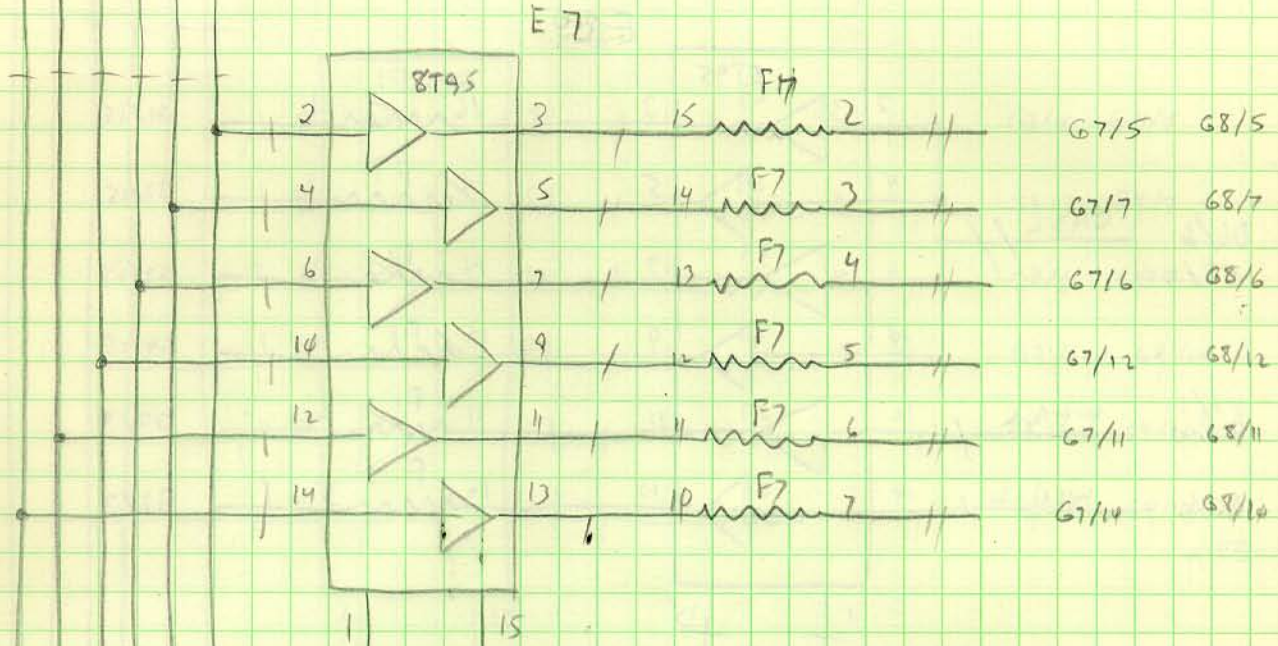
D2/6
E8/14

39Ω - CAS

22Ω - write



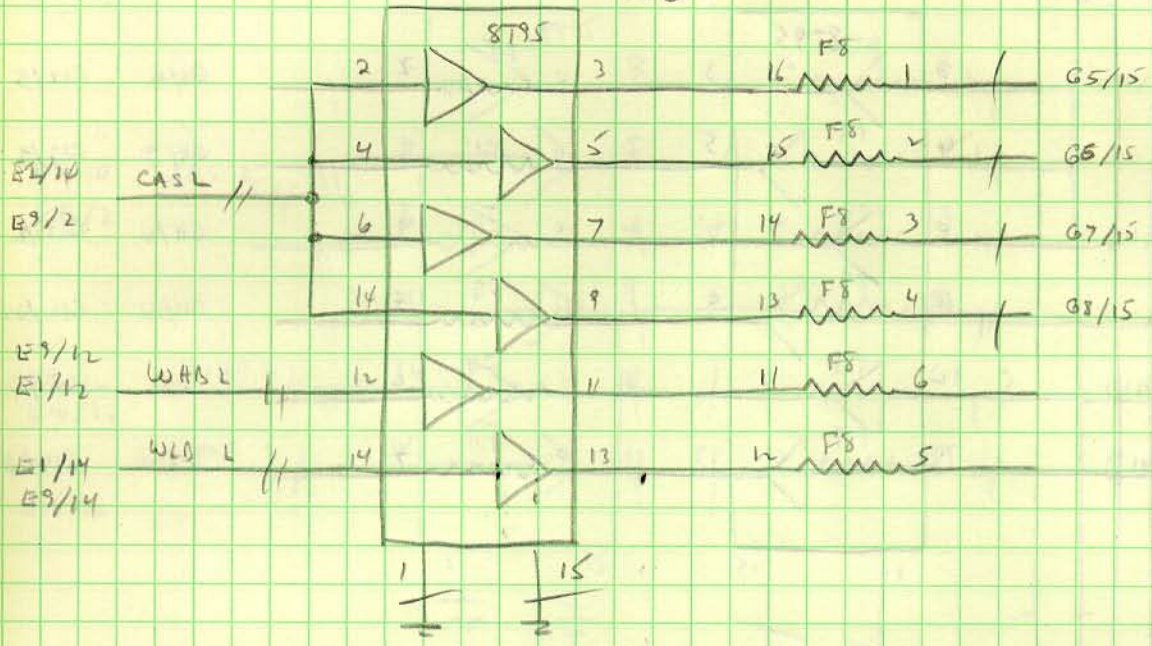
E14/14
E14/12
E14/10
E14/6
E14/4
E14/2



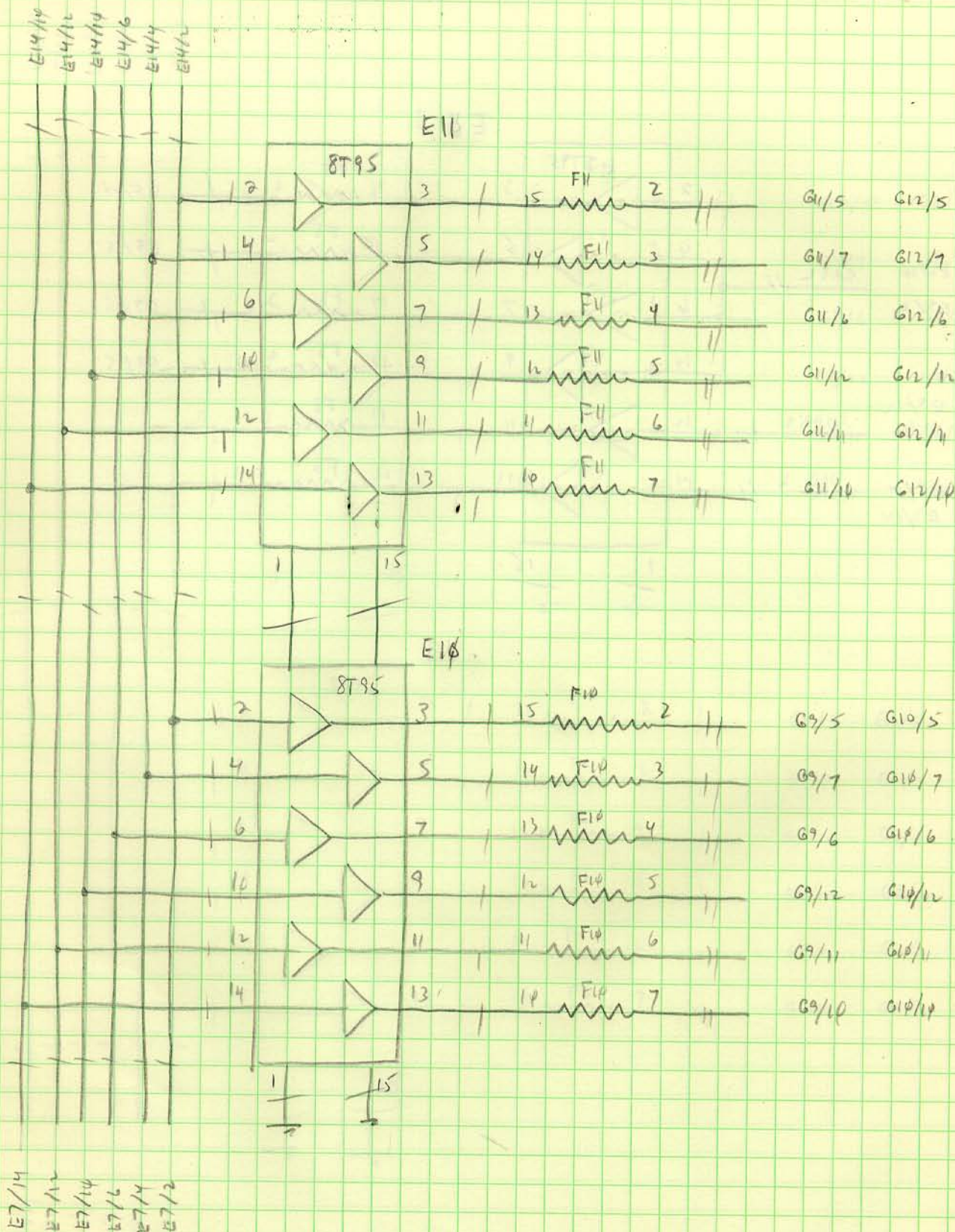
E3/14
E3/12
E3/10
E3/6
E3/4
E3/2

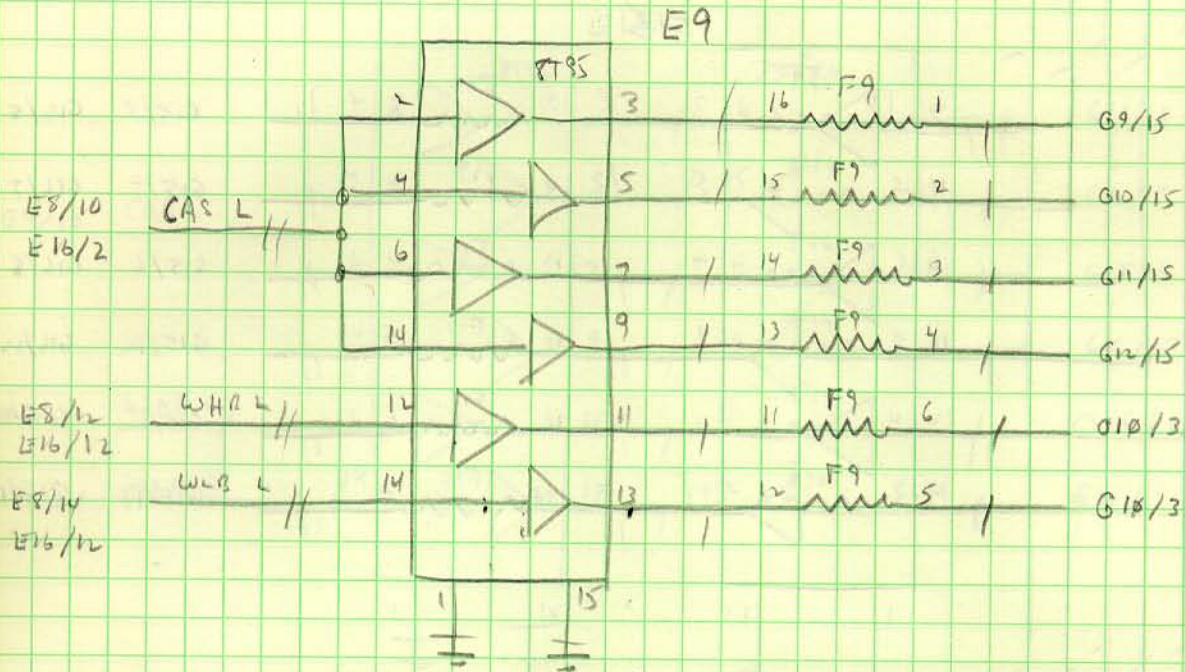
E1/14
E3/2
E3/11
E3/11
E3/14
E3/14

E8



23 Nov 78
APD

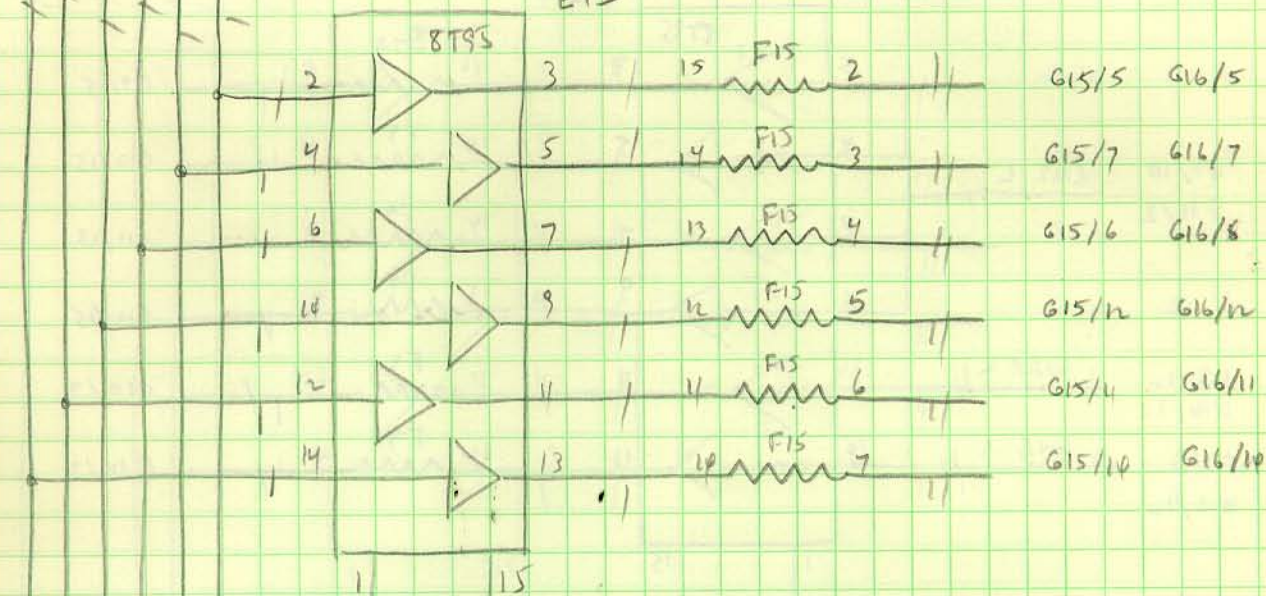




23 Nov 78
ARD

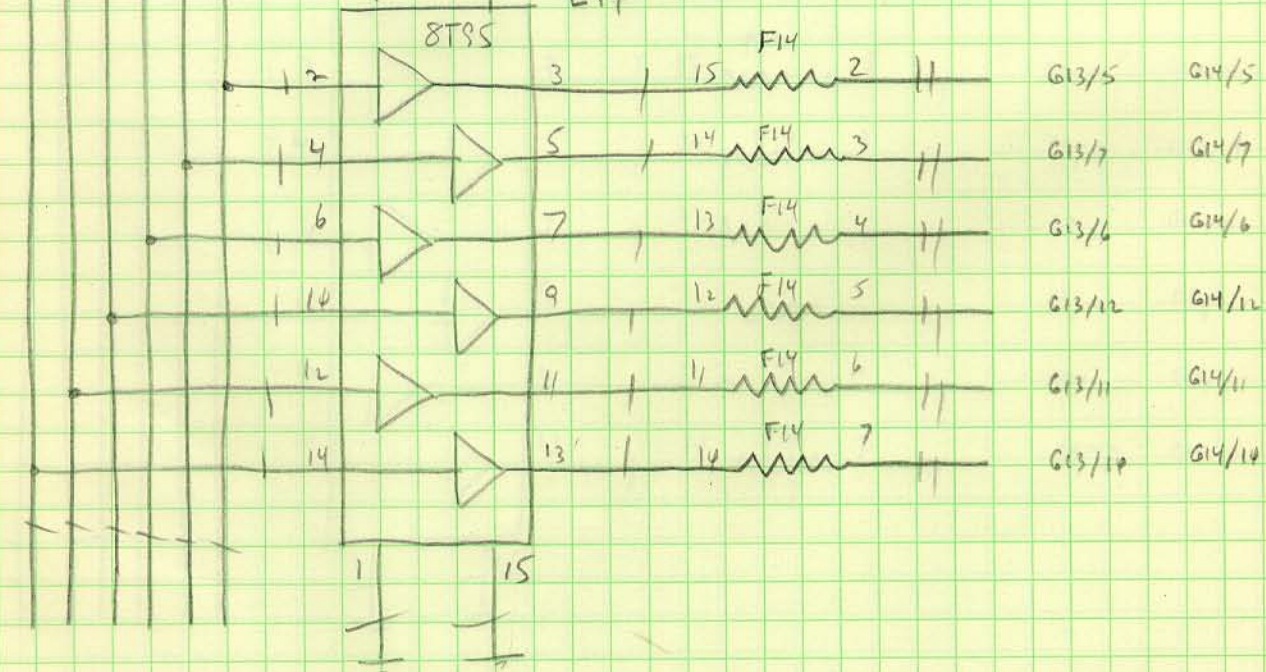
C14/14
C14/12
C14/9
C14/7
C14/5
C14/3

E15

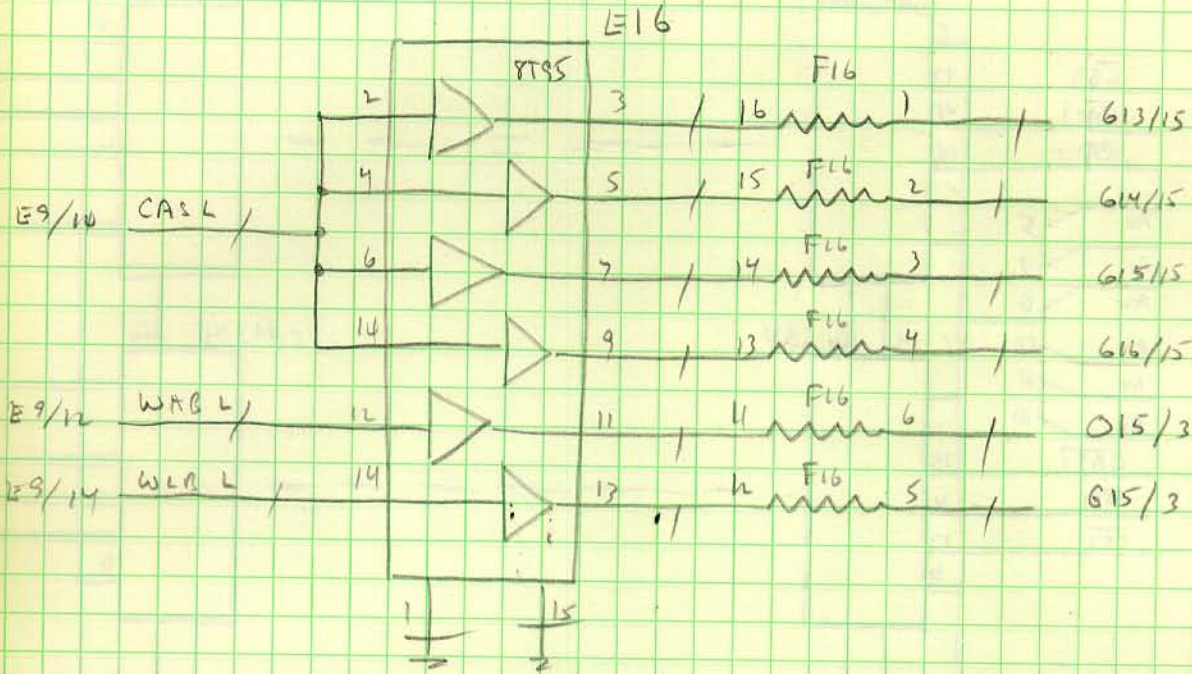


E9/1
E9/1
E9/1

E14

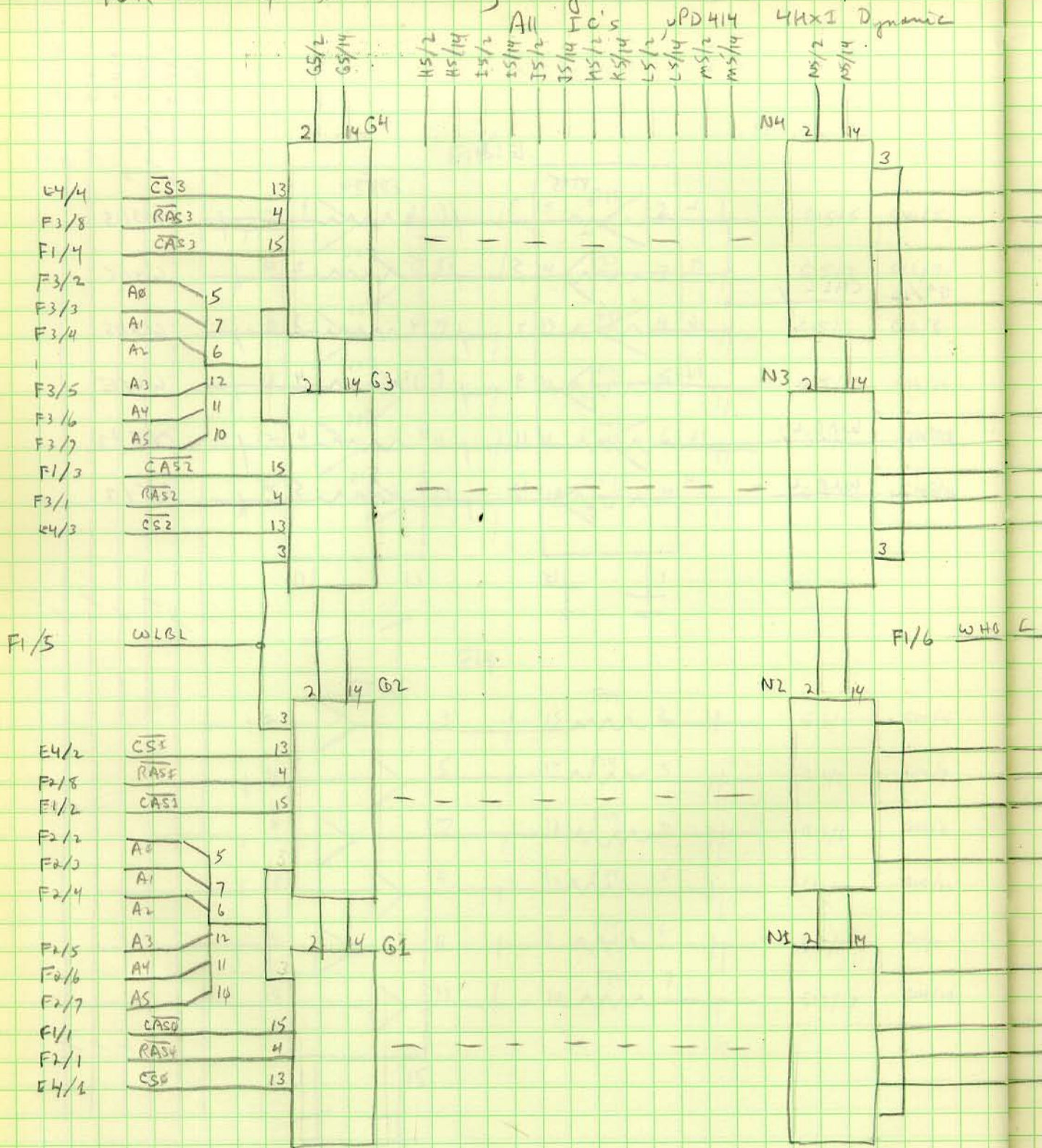


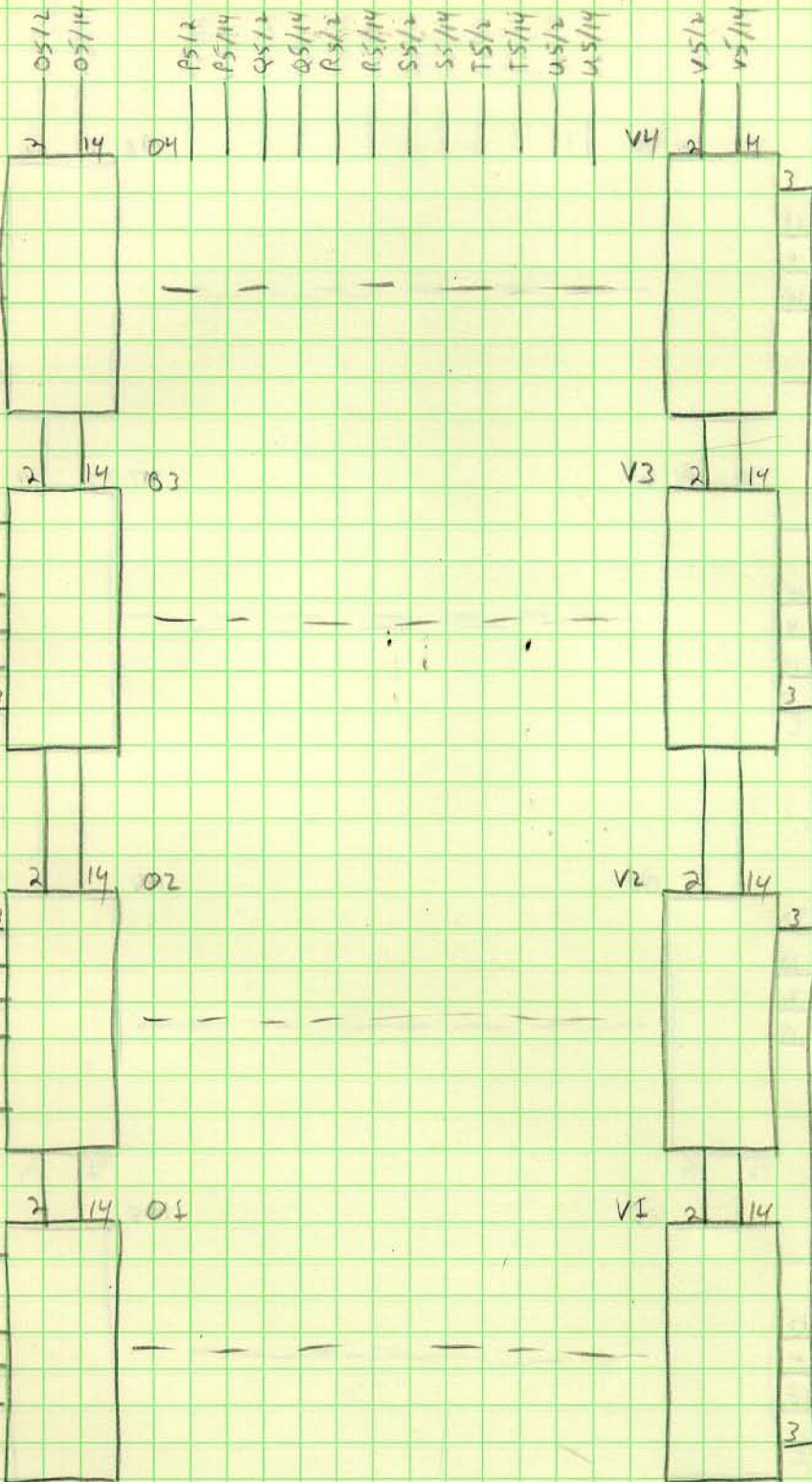
E11/14
E11/12
E11/10
E11/6
E11/4
E11/2



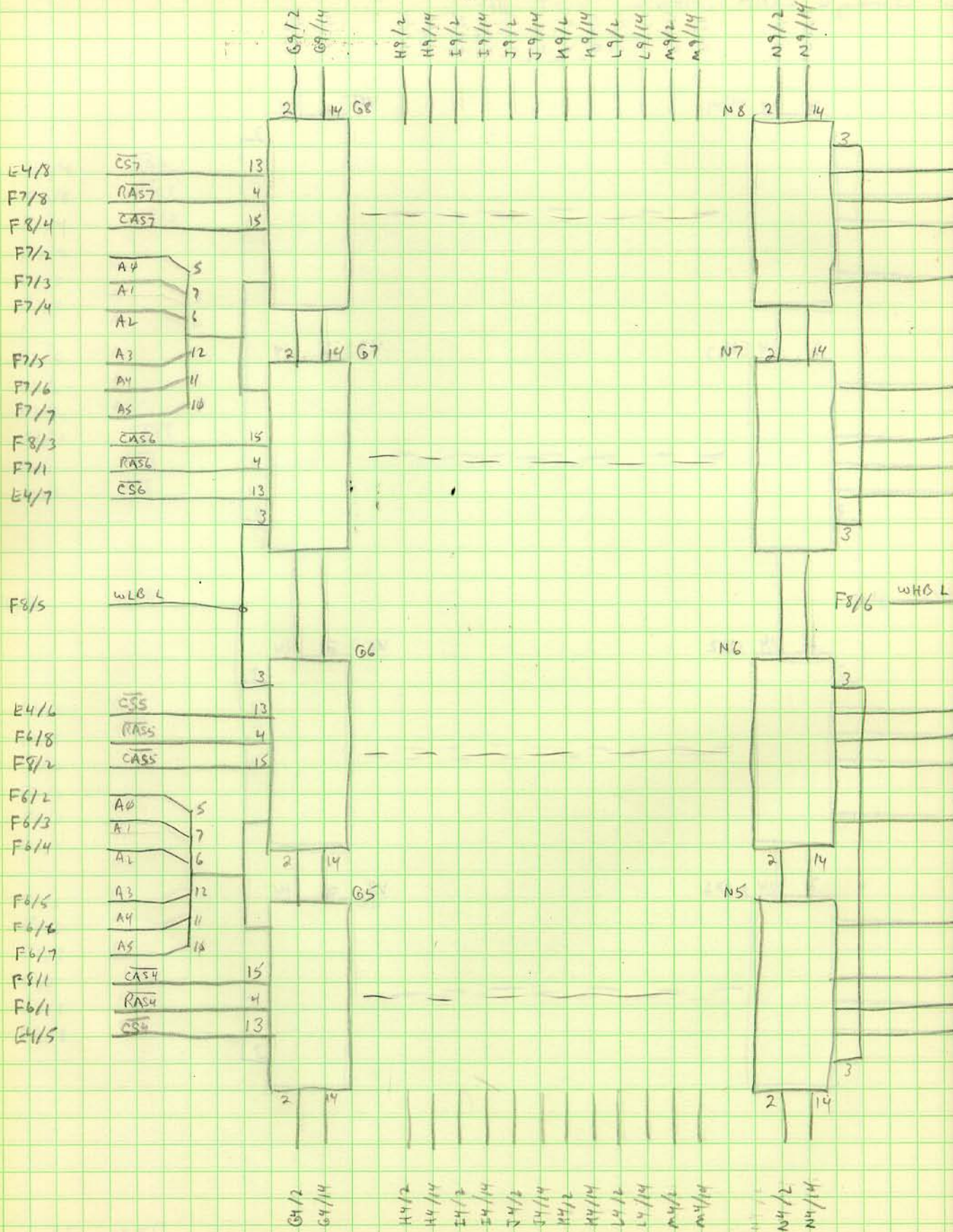
23 Nov 78
ARD

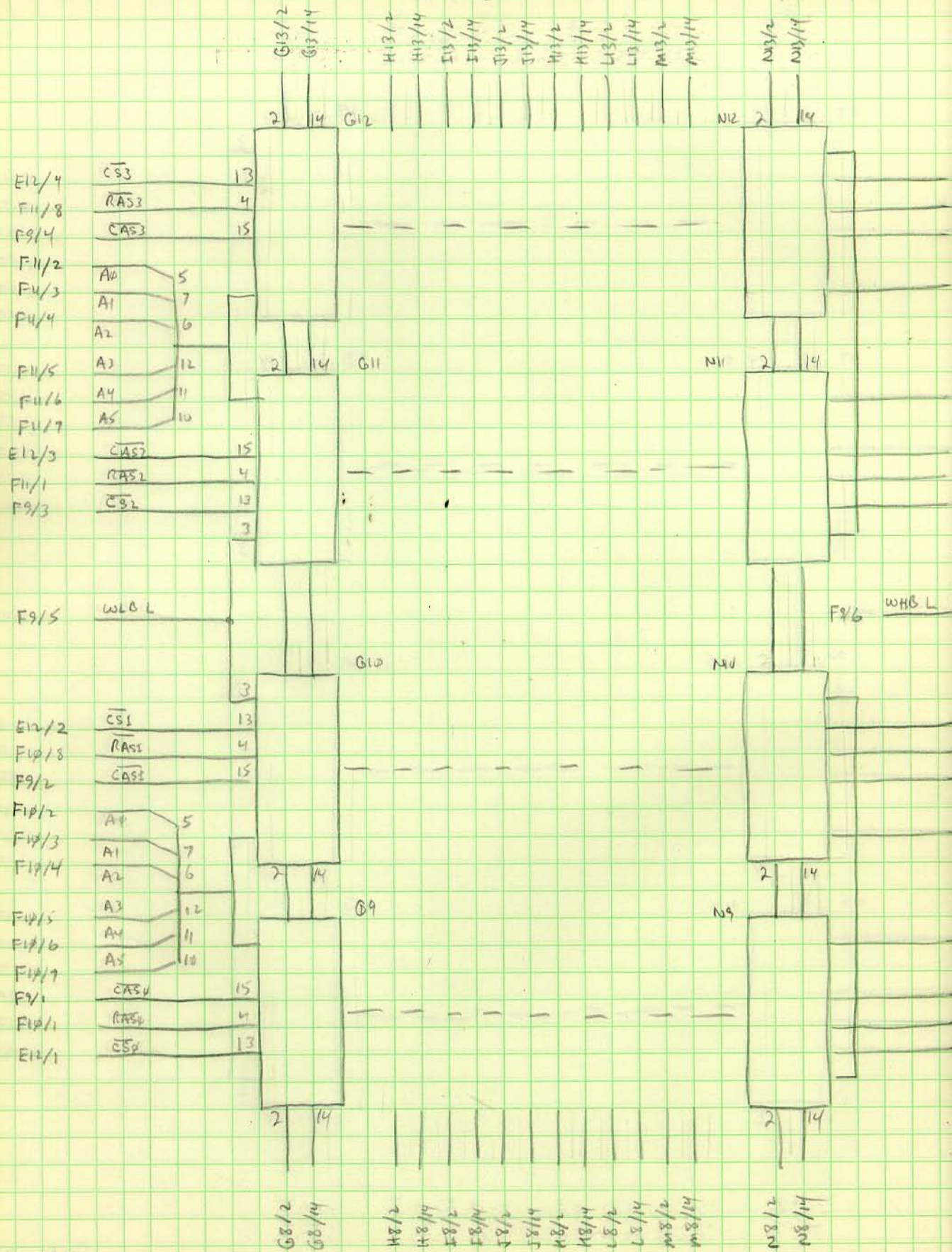
16K Block 4 Bank Memory Layout

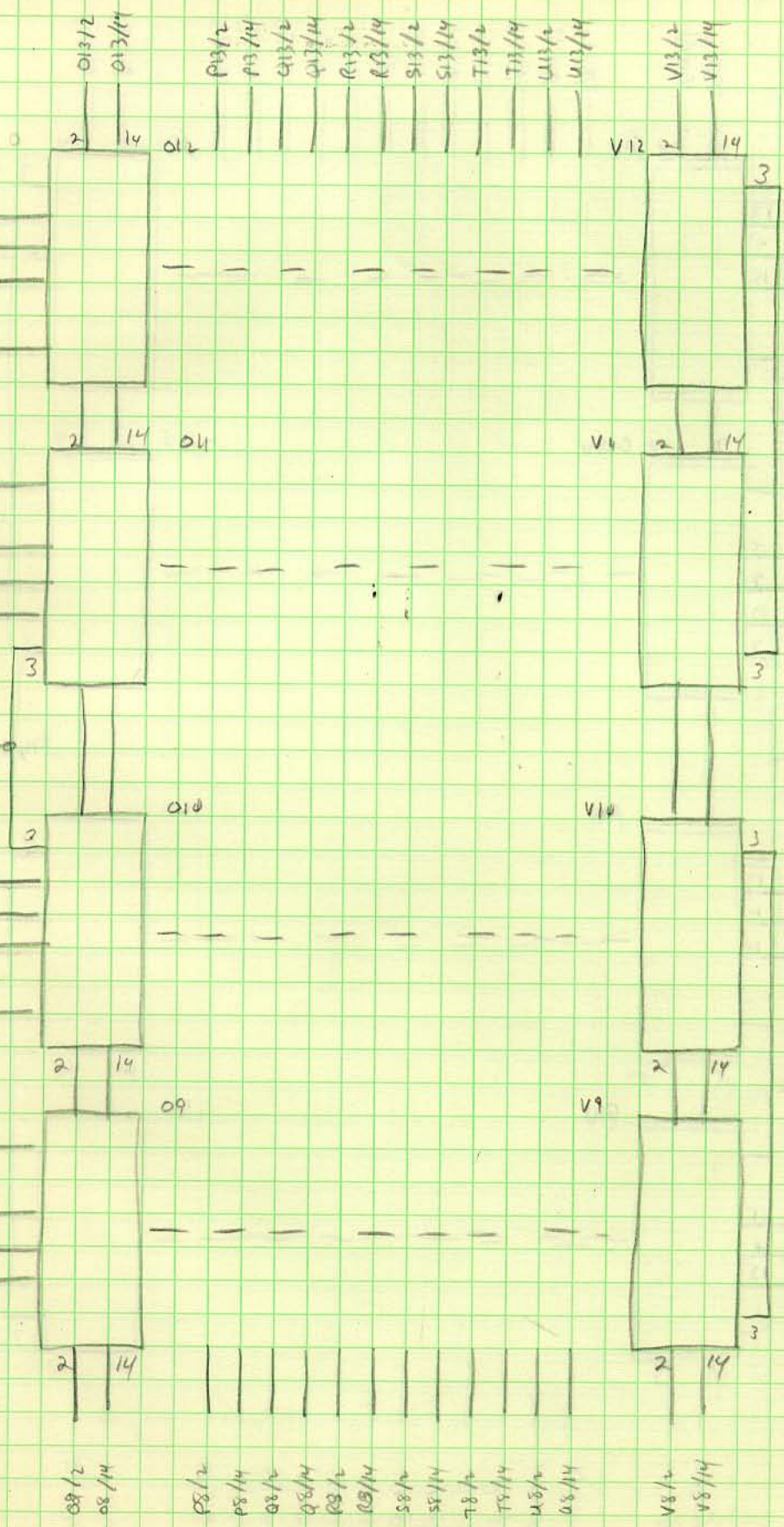




23 NW 78
ARB







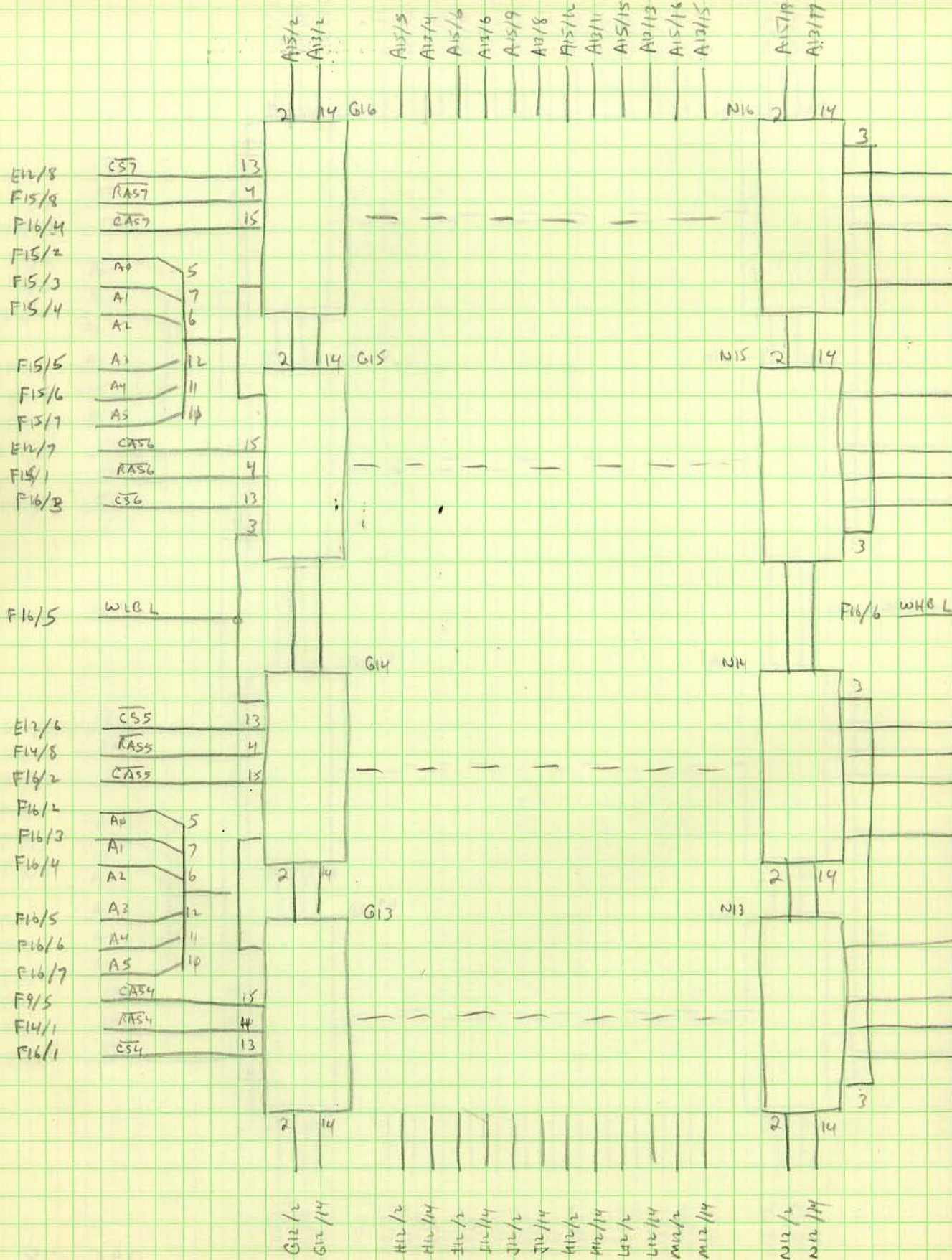
24 Nov 78
ARD

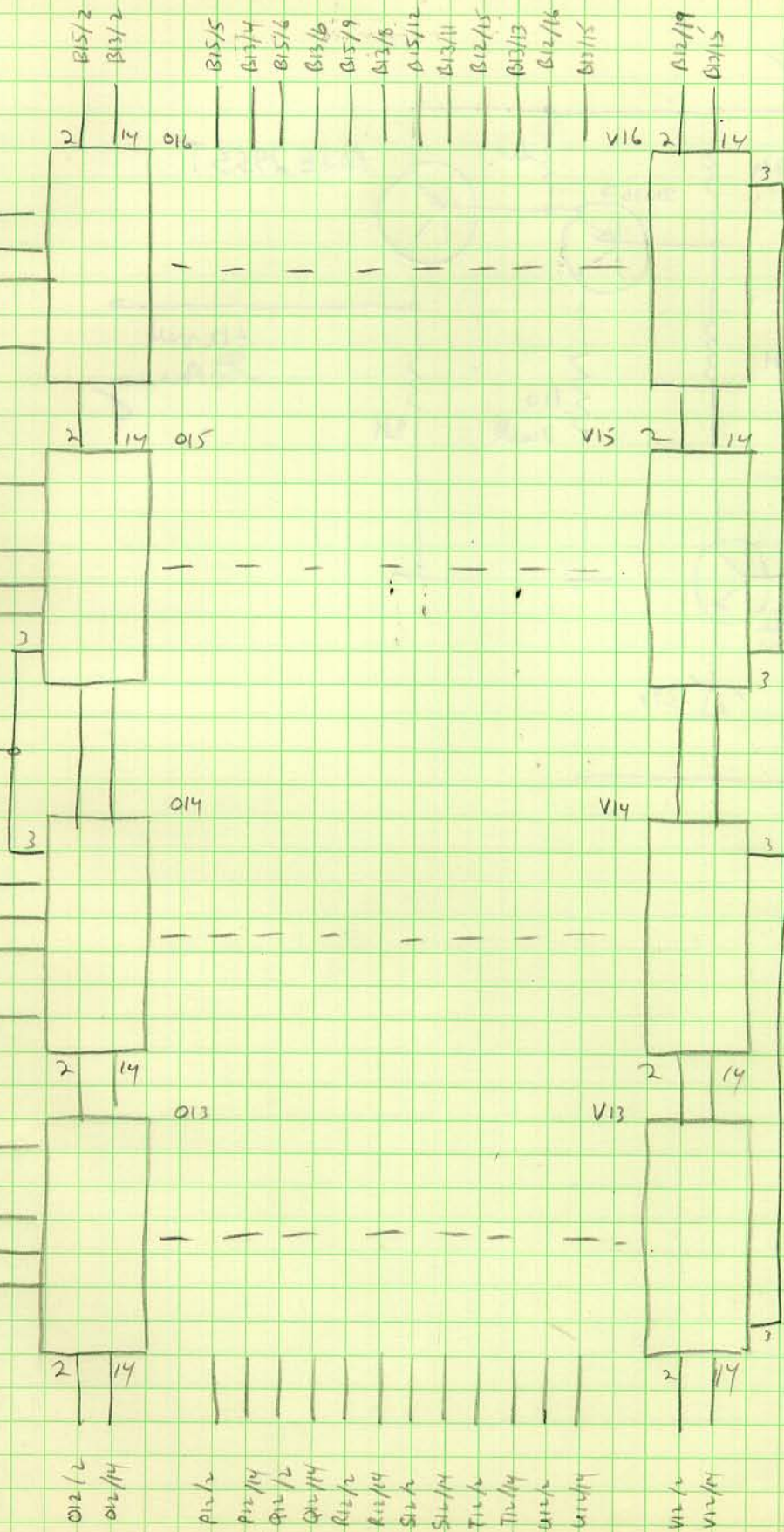
16K Block 3

Bank 2

Memory Layout

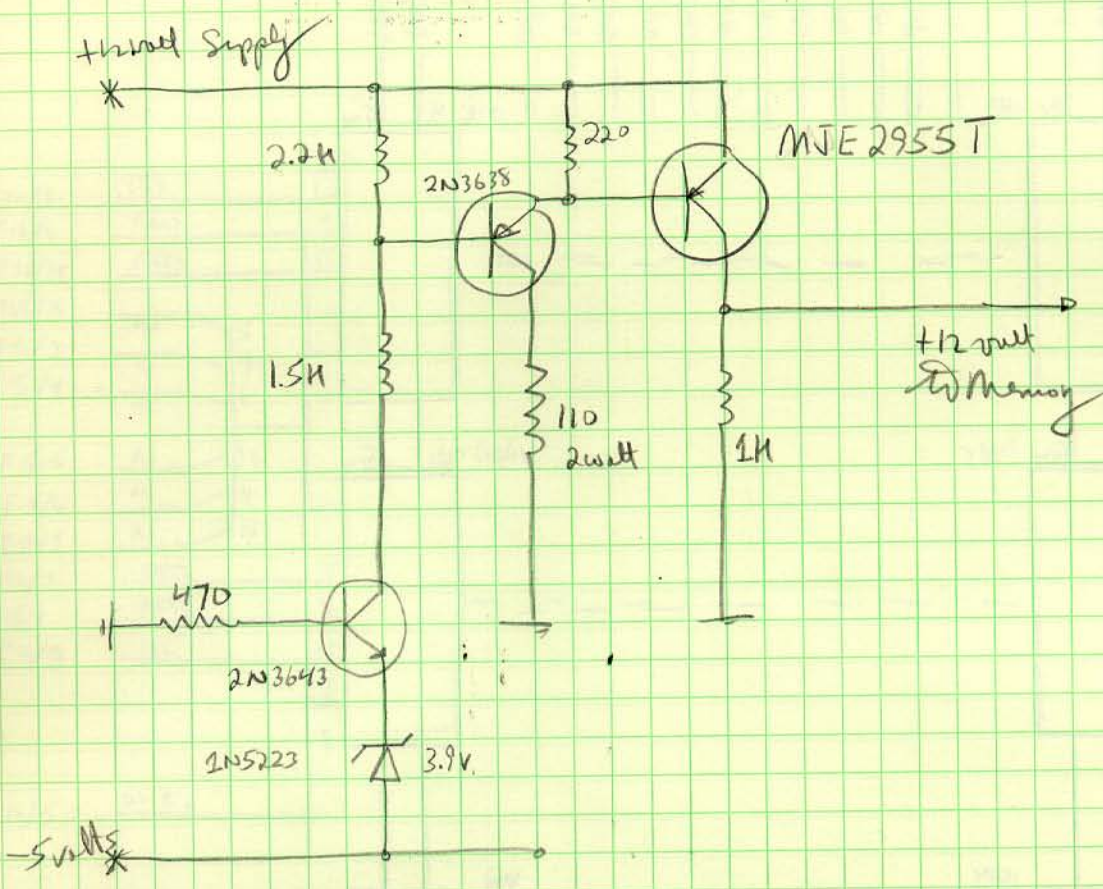
All DC's up 0414





24 Nov 78
ADD

+12 volt Control



Device Locations

A7 RES 68

A8 ~~RES~~ ~~68~~

A13 S240 72

A14 S373 71

A15 S373 71

B7 RES 68

B8 RES 68

B13 S240 72

B14 S373 71

B15 S373 71

C7

C8

C13 S373 74

C14 S240 71

C15 276 74

D1	S04	69
D2	S10	69
D3	S08 S8	68, 69
D4	LS193	68
D5	164	68
D6	S74	68, 69
D7	S132	68, 69
D8	123	68
D9	S08	67, 68
D10	S74	68
D11	S74	67, 68
D12	S21	67
D13	S138	67
D14	S04	69, 71
D15	LS393	71
D16	33	70

Dewie Locoties

E1	8T9S	74
E2	8T9S	74
E3	8T9S	74
A13 E4	RES	73
A14 E5	RES	73
A15 E6	8T9S	75
E7	8T9S	75
E8	8T9S	75
E9	8T9S	76
E10	8T9S	76
E11	8T9S	76
E12	RES	73
E13	RES	73
C1 E14	8T9S	77
C2 E15	8T9S	77
C3 E16	8T9S	77

F1	RES		74
F2	RES	73	74
F3	RES	73	74
F4	S48	73	
F5	S48	73	
F6	RES	73	75
F7	RES	73	75
F8	RES		75
F9	RES	68, 70,	76
F10	RES	73	76
F11	RES	73	76
F12	S48	73	
F13	S48	73	
F14	RES	73	77
F15	RES	73	77
F16	RES	70	77

3 Dec 78

Modification of Microcode Panel # I (Frame #4)

1K x 96	Microcode	PROM
1K x 32	Instruction Code	PROM
3K x 96	Microcode	2116 RAM
3K x 32	Instruction code	2116 RAM

Only Changes are recorded here —

Modified MDone, IDone, XDone logic

11 June 82

L6 #0

G 245 <96:103> <112:119> <104:111> <100:107>

245 245 245 245

I 245 <64:71> <80:87> <72:79> <88:95>

245 245 245 245

J 245 <32:39> <48:55> <40:47> <56:63>

245 245 245 245

K 245 <4:7> <16:23> <8:15> <24:31>

245 245 245 245

<96:103> 2116 L

<64:71> 2116 L

<32:39> 2116 L

<4:7> 2116 L

<96:103> 2116 H

<64:71> 2116 H

<32:39> 2116 H

<4:7> 2116 H

<112:119> 2116 L

<80:87> 2116 L

<48:55> 2116 L

<16:23> 2116 L

<112:119> 2116 H

<80:87> 2116 H

<48:55> 2116 H

<16:23> 2116 H

<104:111> 2116 L

<72:79> 2116 L

<40:47> 2116 L

<8:15> 2116 L

<104:111> 2116 H

<72:79> 2116 H

<40:47> 2116 H

<8:15> 2116 H

<120:127> 2116 L

<88:95> 2116 L

<56:63> 2116 L

<24:31> 2116 L

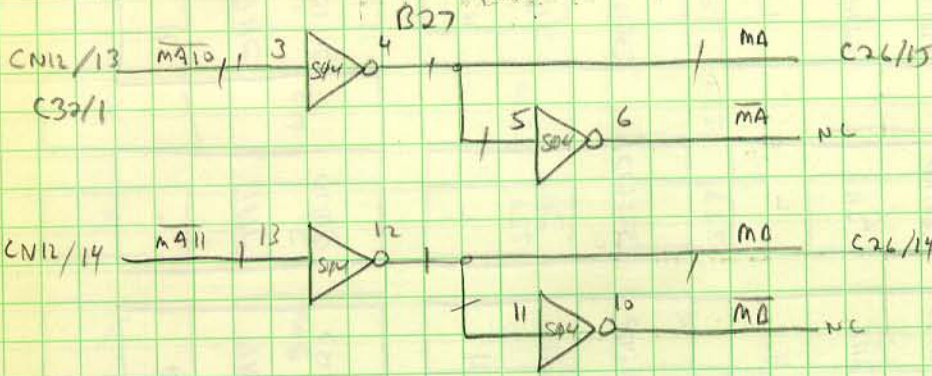
<120:127> 2116 H

<88:95> 2116 H

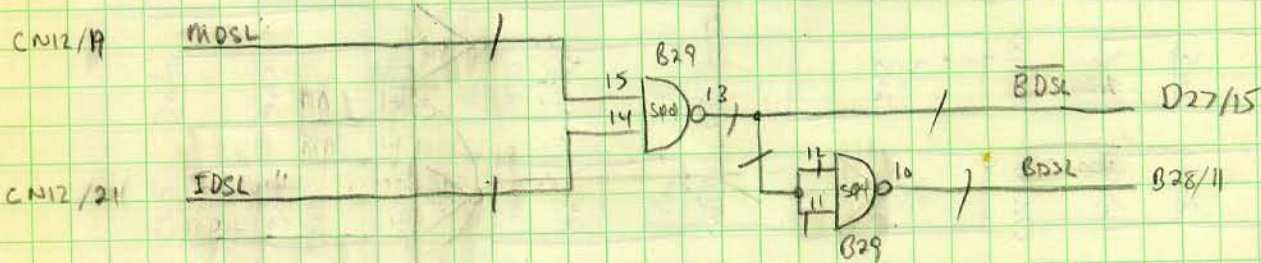
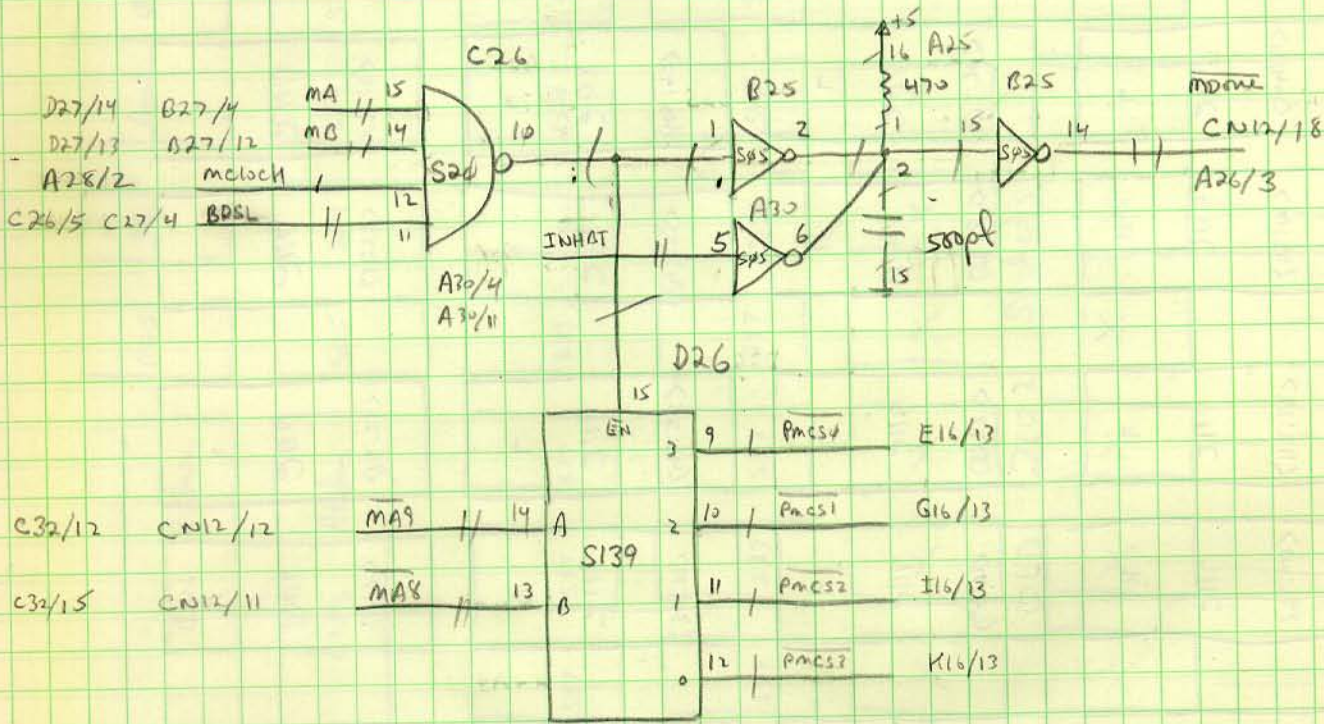
<56:63> 2116 H

<24:31> 2116 H

Microcode Selector Buffers

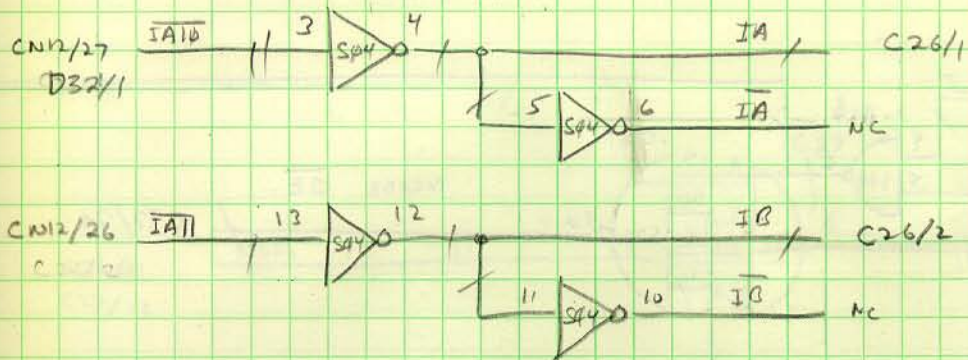


MCODE PROM Decoder

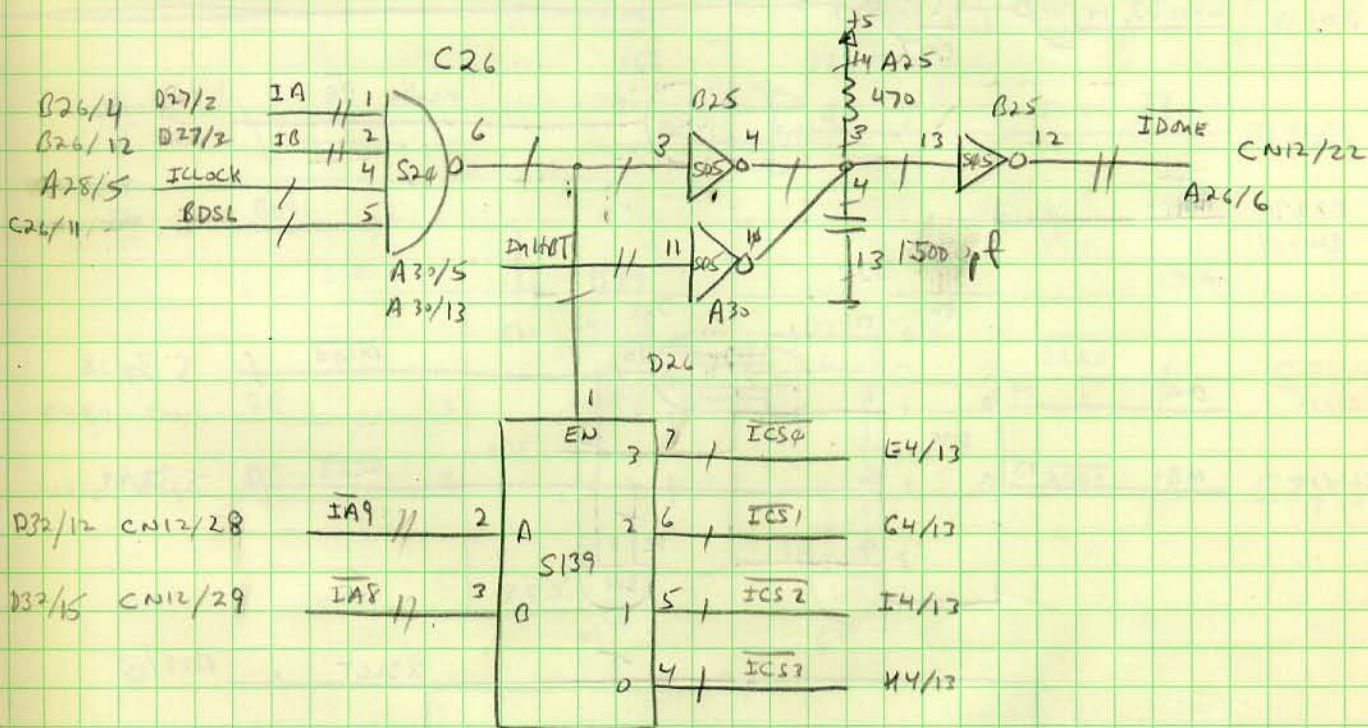


ICode Selector Buffers

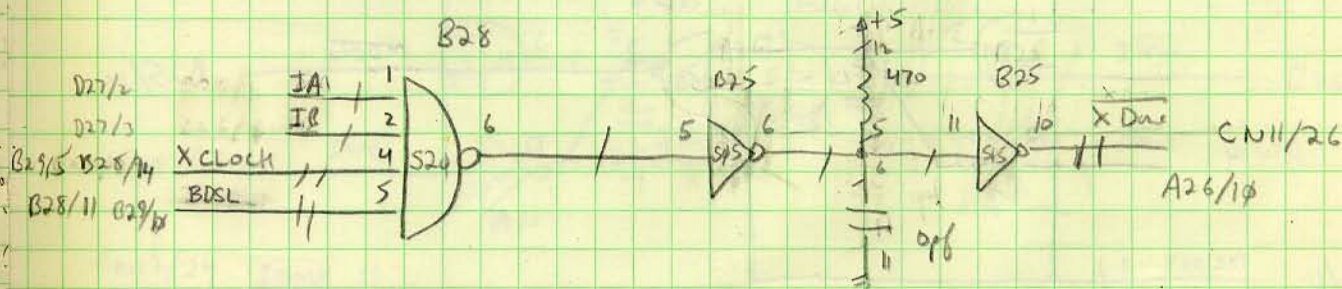
B26



ICode Prom Decoder

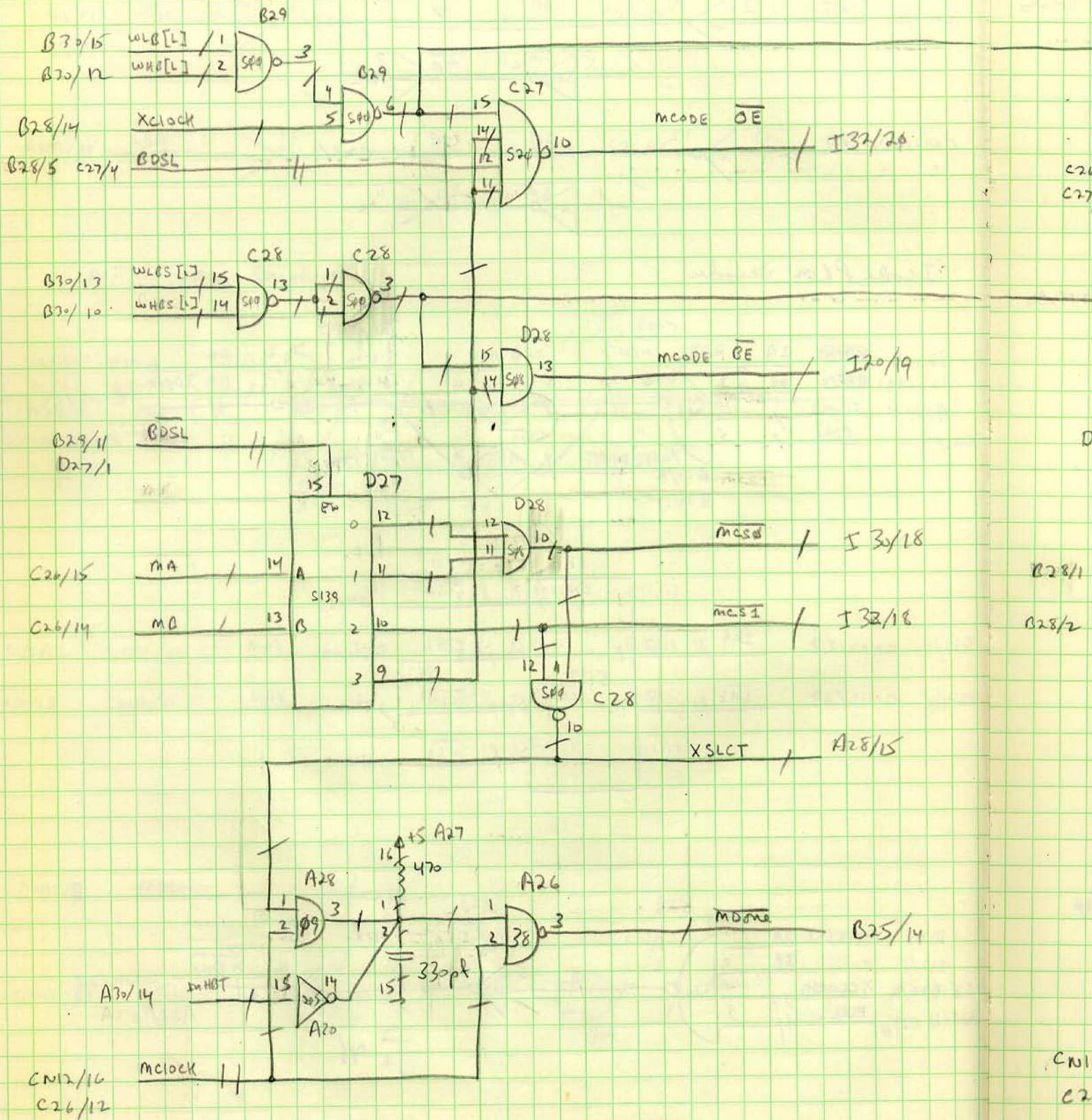


B28

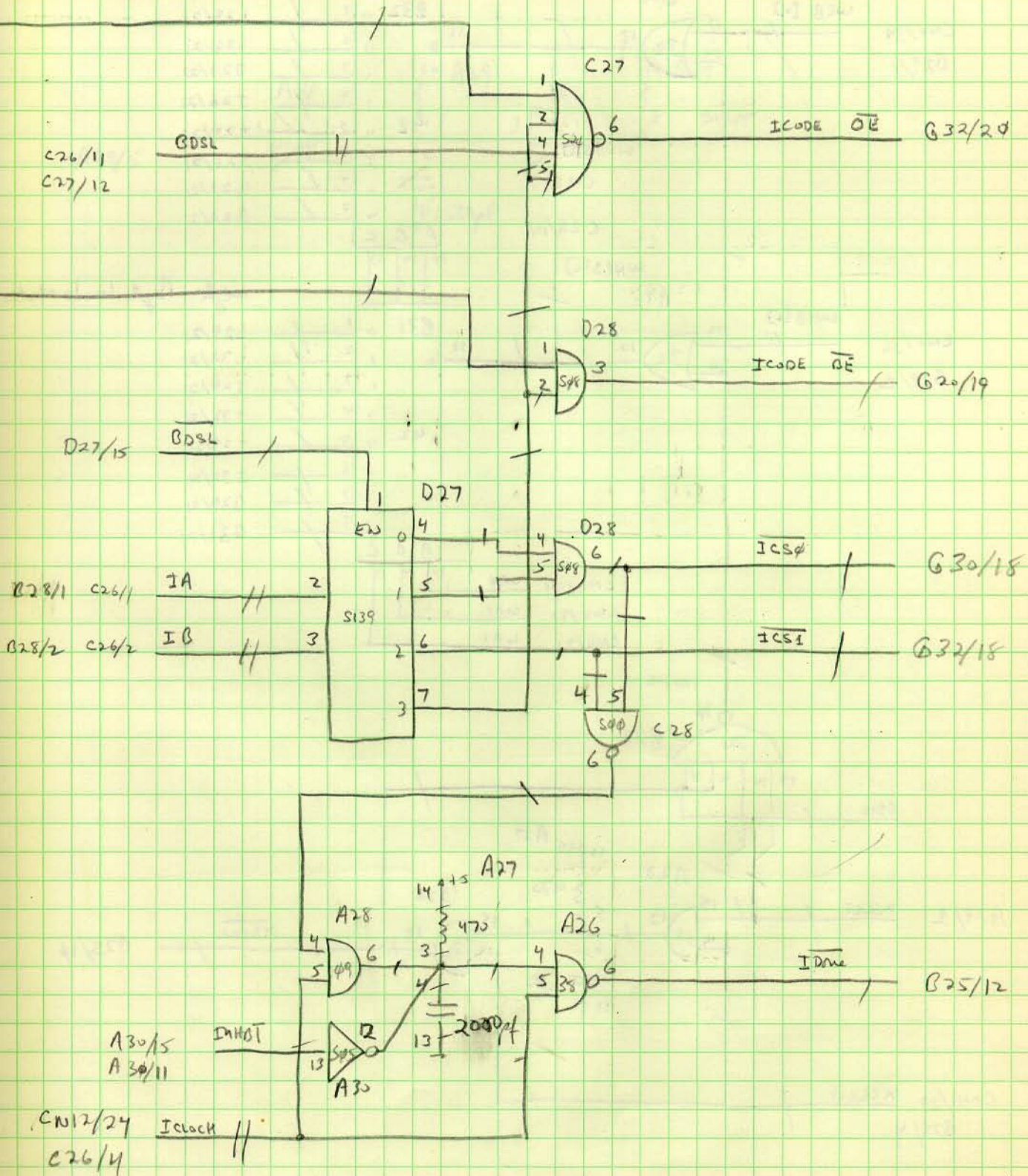


11 June 82
A003

MCODE RAM Decoder



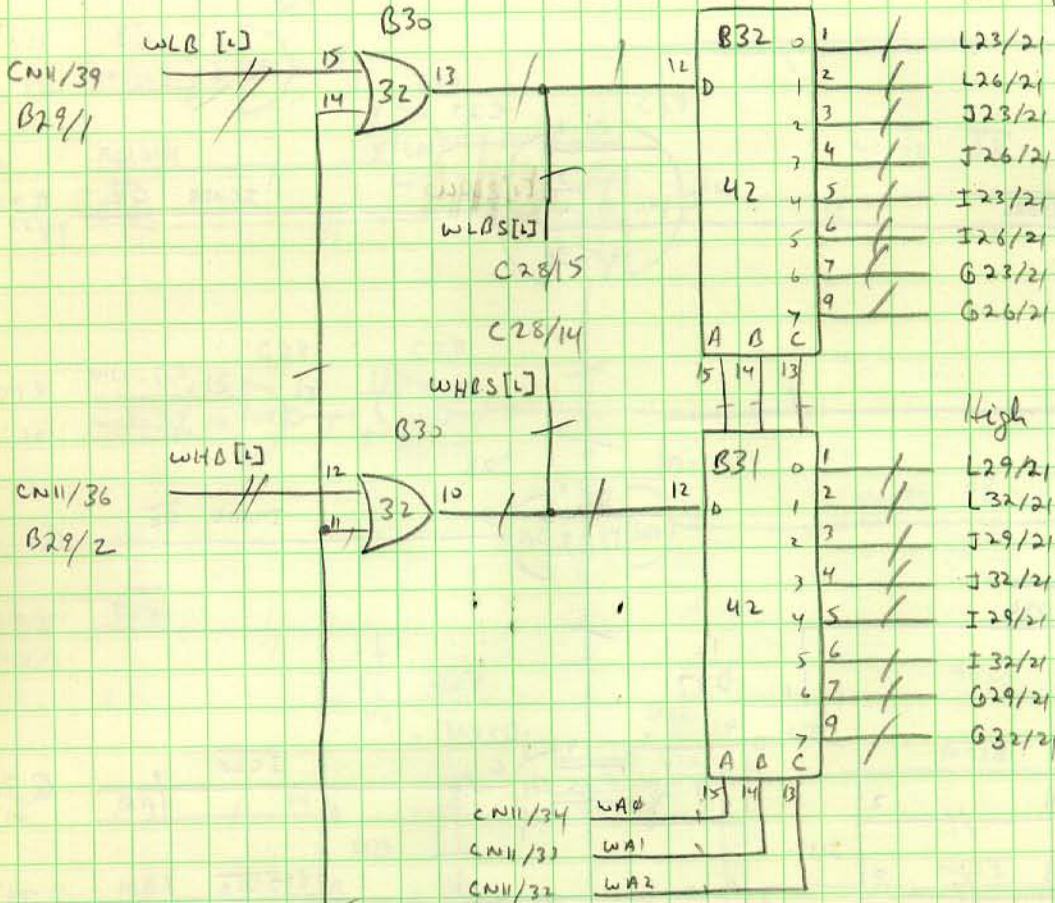
ICODE RAM Decoder



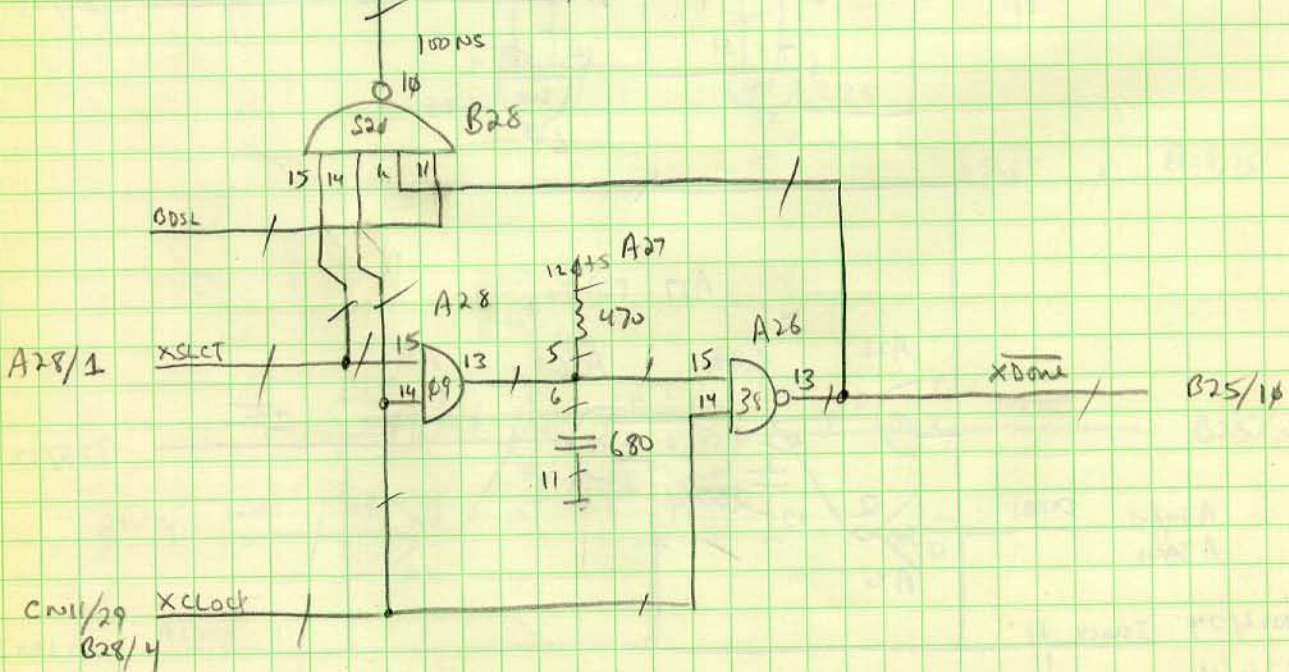
12 June 82
APD

MCODE/ICODE WRITE Selection

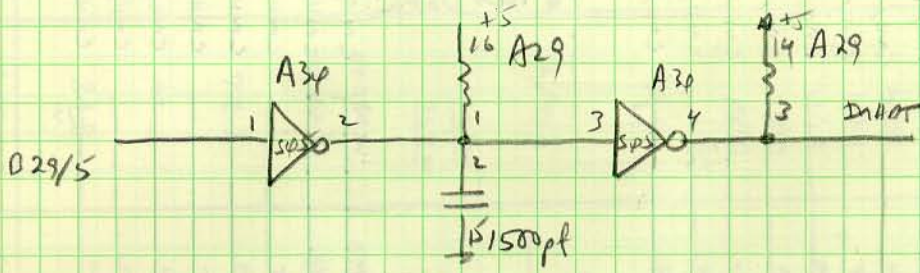
Low Byte Write strobe



High Byte Write strobe

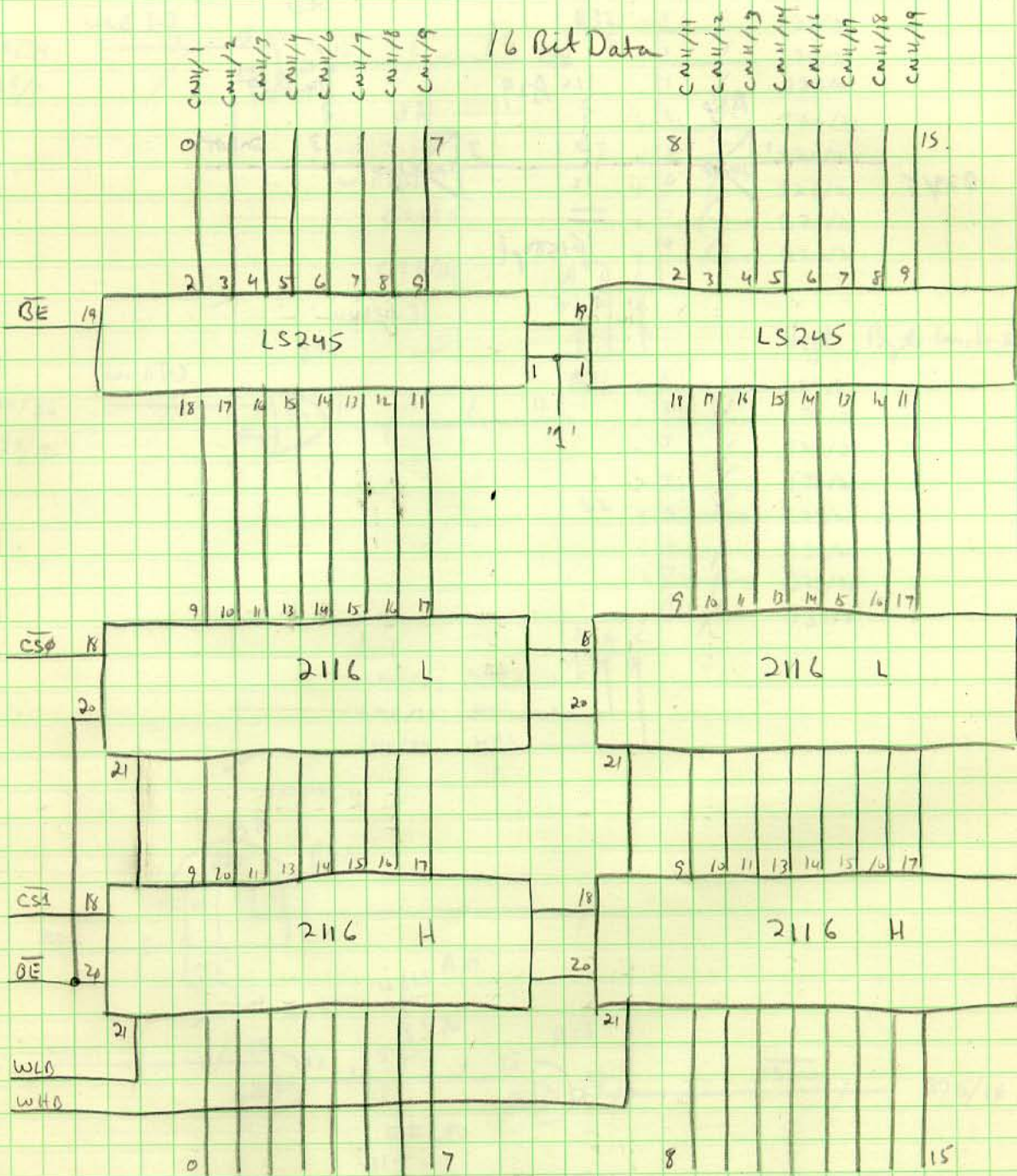


XA Access Inhibit



I code Rans
M code Rans

Word organized



<56:627>
 <48:557>
 <40:47>
 <32:397>
 <24:317>
 <16:237>
 <8:157>
 <0:7>

	<0:17>	<8:15>	<16:23>	<24:31>	<32:39>	<40:47>	<48:55>	<56:63>
LS245	L17	L19	L18	L20	J17	J19	J18	J20
	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE
2116 L	L21	L27	L24	L30	J21	J27	J24	J30
	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE
2116 H	L23	L29	L26	L32	J23	J29	J26	J32
	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE	M CODE OE M CODE OE
BE								
OE								
CSP								
CSI								
WLD								
WHD								
0/8	C13/1	C15/1	D13/1	D15/1	C9/1	C11/1	D9/1	D11/1
1/9	C13/4	C15/4	D13/4	D15/4	C9/4	C11/4	D9/4	D11/4
2/10	C13/15	C15/15	D13/15	D15/15	C9/15	C11/15	D9/15	D11/15
3/11	C13/12	C15/12	D13/12	D15/12	C9/12	C11/12	D9/12	D11/12
4/12	C14/1	C16/1	D14/1	D16/1	C10/1	C12/1	D10/1	D12/1
5/13	C14/4	C16/4	D14/4	D16/4	C10/4	C12/4	D10/4	D12/4
6/14	C14/15	C16/15	D14/15	D16/15	C10/15	C12/15	D10/15	D12/15
7/15	C14/12	C16/12	D14/12	D16/12	C10/12	C12/12	D10/12	D12/12
	B32/1	B31/1	B32/2	B31/2	B32/3	B31/3	B32/4	B31/4

12 June 82
APD

	<64:717	<72:797	<80:877	<88:957	<96:1037	<104:1117	<112:1197	<120:1277
LS245	I17	I19	I18	I20	G17	G19	G18	G20
2116 L	I21	I27	I24	I30	G21	G27	G24	G30
2116 H	I28	I29	I26	I32	G23	G29	G26	G32
BE	MCODE BE	MCODE BE	MCODE BE	MCODE BE	ICODE BE	ICODE BE	ICODE BE	ICODE BE
OE	MCODE OE	MCODE OE	MCODE OE	MCODE OE	ICODE OE	ICODE OE	ICODE OE	ICODE OE
CS0	MCS0	MCS0	MCS0	MCS0	ICSP	ICSP	ICSP	ICSP
CS2	MCS2	MCS2	MCS2	MCS2	ICSE	ICSE	ICSE	ICSE
W40	B32/5	B31/5	B32/6	B31/6	B32/7	B31/7	B32/9	B31/9
W40								
0/8	C5/1	C7/1	D5/1	D7/1	C1/1	C3/1	D1/1	D3/1
1/9	C5/4	C7/4	D5/4	D7/4	C1/4	C3/4	D1/4	D3/4
2/10	C5/15	C7/15	D5/15	D7/15	C1/15	C3/15	D1/15	D3/15
3/11	C5/12	C7/12	D5/12	D7/12	C1/12	C3/12	D1/12	D3/12
4/12	C6/1	C8/1	D6/1	D8/1	C2/1	C4/1	D2/1	D4/1
5/13	C6/4	C8/4	D6/4	D8/4	C2/4	C4/4	D2/4	D4/4
6/14	C6/15	C8/15	D6/15	D8/15	C2/15	C4/15	D2/15	D4/15
7/15	C6/12	C8/12	D6/12	D8/12	C2/12	C4/12	D2/12	D4/12

ICODE Buffers

mc

