Keyboard/Video Terminal
Interface

NATIONAL

53-110

Made in U.S.A.

Keyboard / Video Terminal Interface

includes the following

a) PDP11 BUS I/O FOR TERMINAL I/O

b) PDP11 BUS I/O FOR GRAPHICS PROCESSOR

c) PDP11 BUS NPR LOGIC FOR BOOT LOADING OF MICROPROGRAM

d) optical paper tape reader interface

e) Full Ascii Keyboard I/O

f) Full Ascii video display / half screen graphics

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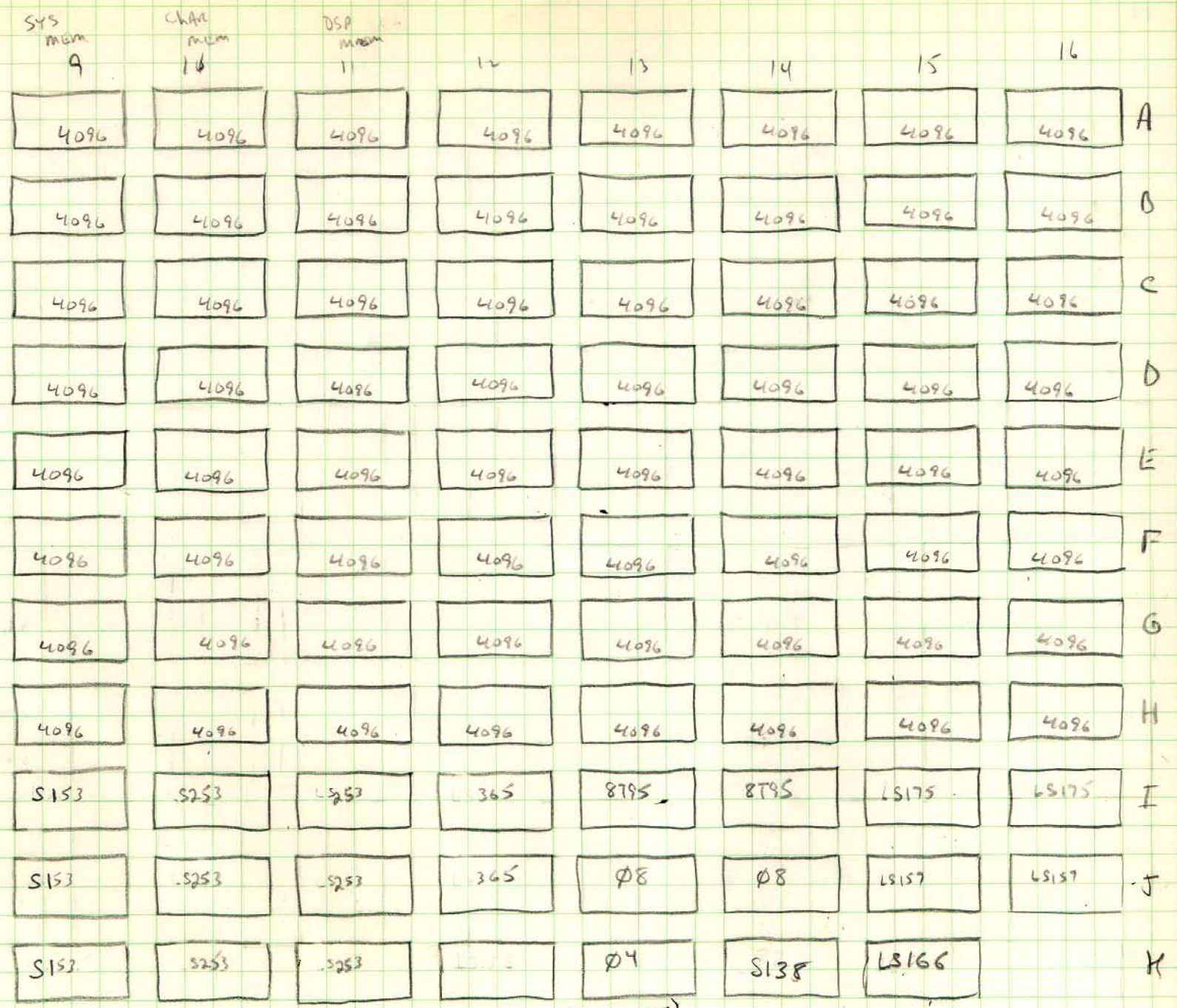
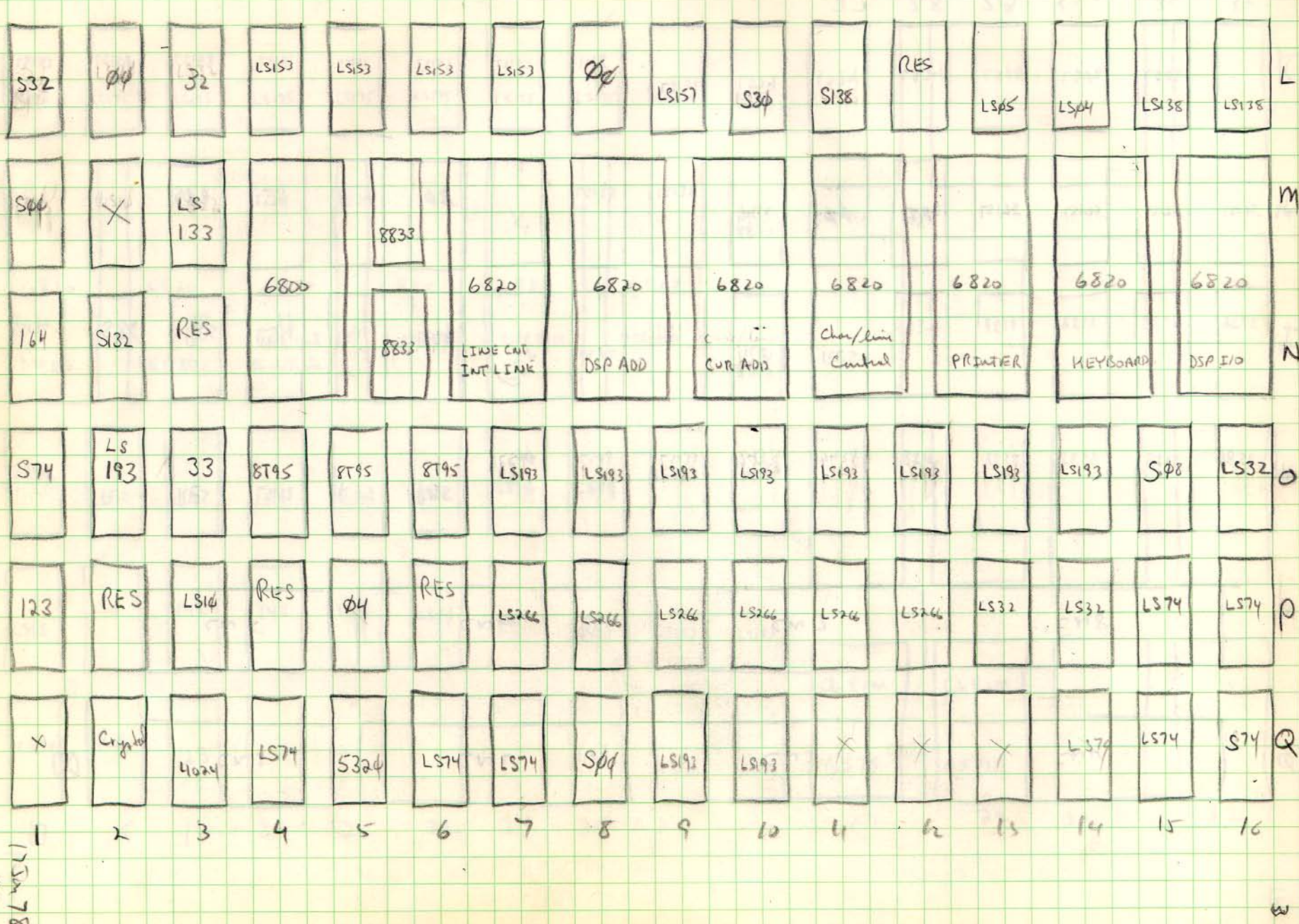
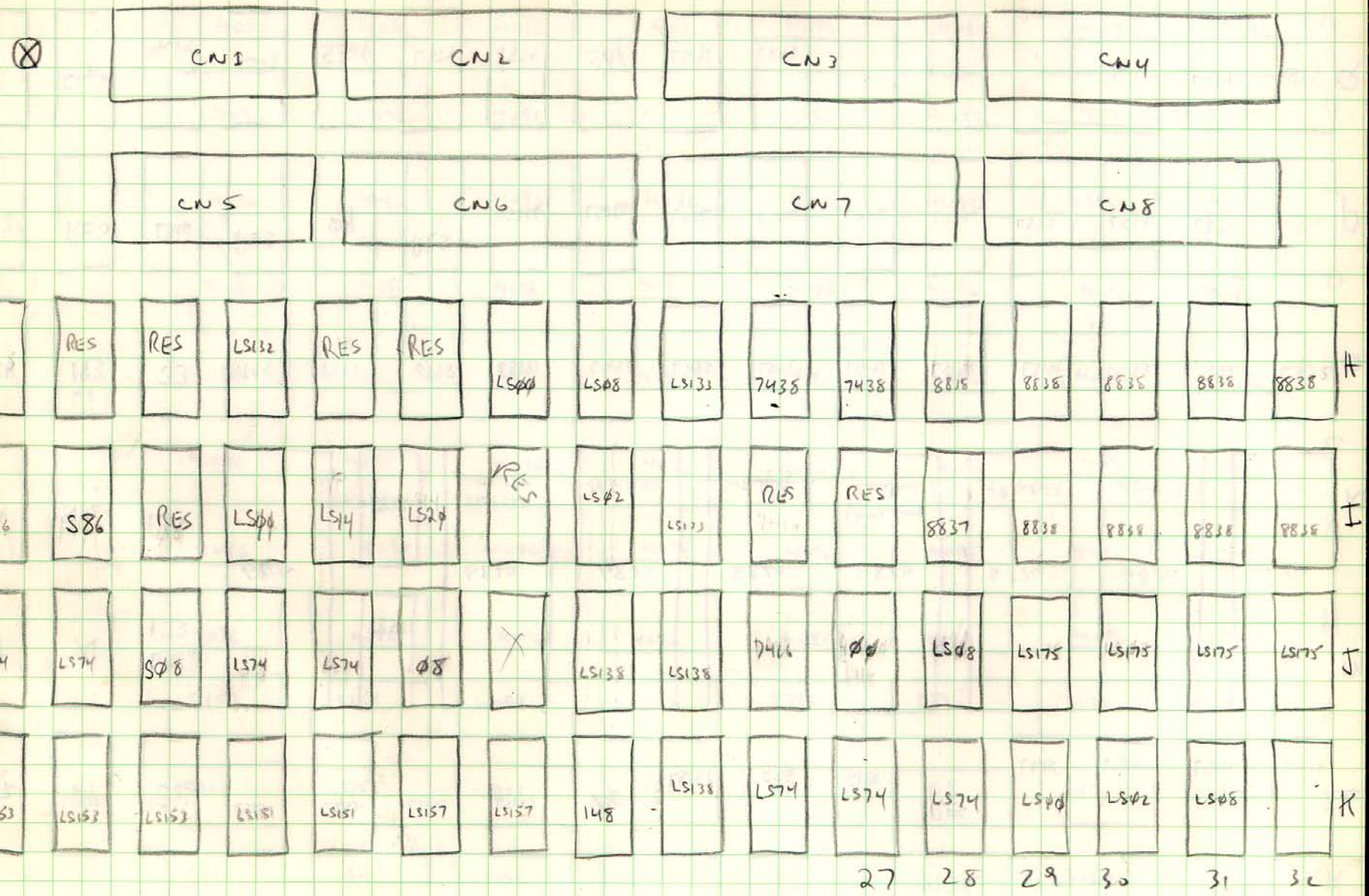

SYS MEM
CHAR MEM
DSP MEM
9
10
11
12
13
14
15
16
A
B
C
D
E
F
G
H
I
J
K
4096
S153
S253
365
8T95
8T97
LS175
LS157
LS166
Ø8
Ø4
S138


S32
Ø4
32
LS153
LS153
LS153
LS153
Ø4
LS157
S30
S138
RES
LS05
LS04
LS138
LS138
L
S04
X
LS 133
8833
6800
6820
6820
6820
6820
6820
6820
M
164
S132
RES
8833
LINE CNT INT LINE
DSP ADD
CUR ADD
Char/Line Control
PRINTER
KEYBOARD
DSP I/O
N
S74
LS 193
33
8T95
8T95
8T95
LS193
LS193
LS193
LS193
LS193
LS193
LS193
LS193
S08
LS32
O
123
RES
LS10
RES
Ø4
RES
LS266
LS266
LS266
LS266
LS266
LS266
LS32
LS32
LS74
LS74
P
X
Crystal
4024
LS74
5324
LS74
LS74
S04
LS193
LS193
X
X
X
LS74
LS74
S74
Q
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16


CN1
CN2
CN3
CN4
CN5
CN6
CN7
CN8
RES
RES
LS132
RES
RES
LSØØ
LSØ8
LS133
7438
7438
8838
8838
8838
8838
8838
A
LS136
S86
RES
LSØ1
LS14
LS2Ø
RES
LSØ2
LS173
RES
RES
8837
8838
8838
8838
8838
I
LS74
LS74
SØ8
LS74
LS74
Ø8
X
LS138
LS138
7416
ØØ
LSØ8
LS175
LS175
LS175
LS175
J
LS153
LS153
LS153
LS151
LS151
LS157
LS157
148
LS138
LS74
LS74
LS74
LSØ1
LSØ2
LSØ8
K
27
28
29
30
31
32


LS175
LS175
LS175
LS175
LS175
LS175
LS175
LS175
LS175
LS175
6820
DSP I/O
6820
KEY I/O
6820
NPR Cnt
Photocode
6820
NPR DATA
6820
NPR DATA
6820
NPR ADD
8833
8833
8T95
LS174
LS174
LS174
LS174
LSØ2
LS1Ø
LSØ4
LS153
LS153
LSØ8
LS11
148
148
148
LSØ4
LS11
RES
LS153
LS153
LS74
Res
123
RES
LS138
LS138
ch Rom
6575
ch Rom
6571A
27
29
30
32
17
18
19
20
21
22
23
24
25
26
L
M
N
O
P
Q
R

CN1

1		24	GND
2		23	
3		22	
4		21	
5		20	
6	GND	19	
7		18	GND
8		17	
9		16	
10		15	
11		14	
12	GND	13	

CN2 Keyboard / Phototreader

1	K0	-	L17/4	40	GND		
2	K1	-	L17/5	39	P0	—	L21/4
3	K2	-	L17/12	38	P1	—	L21/5
4	K3	-	L17/13	37	P2	—	L21/12
5	GND			36	P3	—	L21/13
6	K4	—	L18/4	35	GND		
7	K5	-	L18/5	34	P4	—	L22/4
8	K6	—	L18/12	33	P5	-	L22/5
9	—			32	P6	-	L22/12
10	GND			31	P7	-	L22/13
11	KSTROB	—	L17/9	30	GND		
12	Clock	—	MN16/40	29	PSTROBE	—	L22/9
13	Repeat	—		28	SPKR+	+	I23/1
14	Break	—		27	SPKR-	+	I23/2
15	GND			26	-12V	+	Q5/1
16	Paper	-		25	GND		
17	Here Is	-		24	+5V	+	H10/16
18	Tape →	-		23	+5V	+	H9/16
19	Tape ←	-		22	+5V	+	H8/16
20	GND			21	+5V	+	H7/16

CN3

1	
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17	
18	
19	
20	

CN4

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16	
17	
18	
19	
20	

CN3 UNIBUS OUT CONTROL

1	BR4 L	+	CN7/1
2	BR5 L	+	
3	BR6 L	+	
4	BR7 L	+	
5	GND		
6	NPR L	+	
7			
8			
9	INIT L	+	
10	GND		
11	ACLO	+	
12	DCLO	+	
13	PwrFail L	−	
14	BSSYN	+	
15	GND		
16	BMSYN	+	
17			
18			
19	BBSY	+	
20	GND		CN7/24

40	GND		
39	BG4	+	CN7/39
38	BG5	+	
37	BG6	+	
36	BG7	+	CN7/36
35	GND		
34	NPGO	−	I27/3
33			
32	60HZ INT H	+	CN7/32
31			
30	GND		
29	INTR	+	
28	SACK	+	
27	PBØ	+	
26	PB1	+	
25	GND		
24	CØ L	+	
23	C1 L	+	
22	BA16	+	
21	BA17	+	CN7/21

CN4 UNIBUS OUT DATA/ADDRESS

1	BDØ L	+	CN8/1
2		+	
3		+	
4		+	
5	GND		
6		+	
7		+	
8		+	
9		+	
10	GND		
11		+	
12		+	
13		+	
14		+	
15	GND		
16		+	
17		+	
18		+	
19	BDISL	+	CN8/19
20	GND		

40	GND		
39	BAØ L	+	CN8/39
38		+	
37		+	
36		+	
35	GND		
34		+	
33		+	
32		+	
31		+	
30	GND		
29		+	
28		+	
27		+	
26		+	
25	GND		
24		+	
23		+	
22		+	
21	BAISL	+	CN8/21

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CN5 INTERNAL INTERRUPT LINES

1	Clock	—	24	GND	
2	INT0	—	23	C Clock	—
3	|	—	22	C INT0	—
4	|	—	21	|	—
5	|	—	20	|	—
6	GND		19		—
7	|	—	18	GND	
8	INT5	—	17	|	—
9	EX-ILINE	—	16	C INT5	—
10			15	C EX ILINE	—
11			14		
12	GND		13		

PRINTER DATA/Control

CN6

1	PD0	—	MN13/16	40	GND		
2	PD1	—	MD13/17	39	PCB1	—	MN13/18
3	PD2	—	MN13/12	38	PCB2	—	MN13/19
4	PD3	—	MN13/13	37			
5	GND			36			
6	PD4	—	MN13/14	35	GND		
7	PD5	—	MN13/15	34	PCA1	—	MN13/40
8	PD6	—	MN13/16	33	PCA2	—	MN13/39
9	PD7	—	MN15/17	32			
10	GND			31			
11	PC0	—	MN13/2	30	GND		
12	PC1	—	MN13/3	29			
13	PC2	—	MN13/4	28			
14	PC3	—	MN13/5	27	-12V		
15	GND			26	-12V		
16	PC4	—	MN13/6	25	GND		
17	PC5	—	MN13/7	24	+12V		
18	PC6	—	MN13/8	23	+12V.		
19	PC7	—	MN13/9	22	+5V.		
20	GND			21	+5V		

CN7 UNIBUS IN CONTROL

1	BR4	−	CN3/1				
2	BR5	−					
3	BR6	−					
4	BR7	−					
5	GND						
6	NPR L	−		H27/13			
7							
8							
9	INIT	−		−	I28/13		
10	GND						
11	ACLO	−					
12	DCLO	−					
13	Power Fail L	+		H19/6			
14	BSSYN	−		−	H26/6		
15	GND						
16	BMSYN	−		−	H27/10		
17							
18							
19	BBSY	−	CN3/19	−	H27/3		
20	GND						

40	GND						
39	B64	−	CN3/39				
38	B65	−					
37	B66	−					
36	B67	−	CN3/36				
35	GND						
34	NPG I						I27/4
33	60 H Clock	+	CN3/33			+	L8115
32	60 Hz INT	−	CN3/32				
31	Clock INT clear L	+	CN3/31				
30	GND						
29	INTR	−					
28	SACK	−				−	H27/6
27	PB0	−					
26	PB1	−					
25	GND						
24	C0 1	+				+	H28/12
23	C1 L	+				+	H28/15
22	BA16 L	+				+	H28/1
21	BA17 L	+	CN3/21			+	H28/4

CN8 UNIBUS DATA/Address IN

1	BD0 L	+	CN4/1	+	I29/15			
2		+		+	I29/12			
3		+		+	I29/4			
4		+		+	I29/1			
5	GND							
6		+		+	I36/15			
7		+		+	I30/12			
8		+		+	I30/4			
9		+		+	I36/1			
10	GND							
11		+		+	I31/15			
12		+		+	I31/12			
13		+		+	I31/4			
14		+		+	I31/1			
15	GND							
16		+		+	I32/15			
17		+		+	I32/12			
18		+		+	I32/4			
19	BD15 L	+	CN4/19	+	I32/1			
20	GND							

40	GND							
39	BA0 L	+	CN4/40			+	H29/1	
38		+				+	H29/4	
37		+				+	H29/12	
36		+				+	H29/15	
35	GND							
34		+				+	H30/1	
33		+				+	H30/4	
32		+				+	H30/12	
31		+				+	H30/15	
30	GND							
29		+				+	H31/1	
28		+				+	H31/4	
27		+				+	H31/12	
26		+				+	H31/15	
25	GND							
24		+				+	H32/1	
23		+				+	H32/4	
22		+				+	H32/12	
21	BA15 L	+	CN4/21			+	H32/15	

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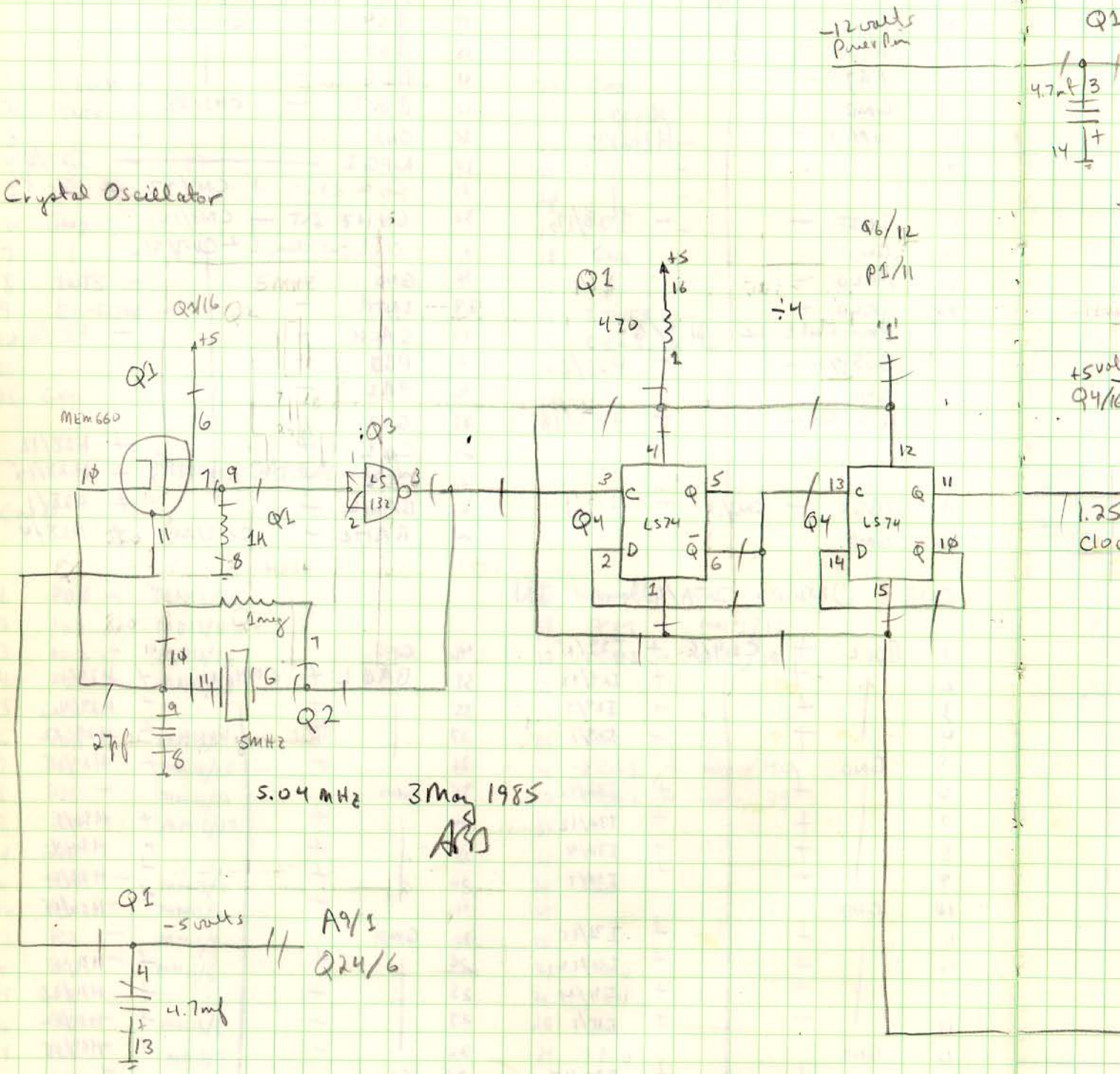
ABD

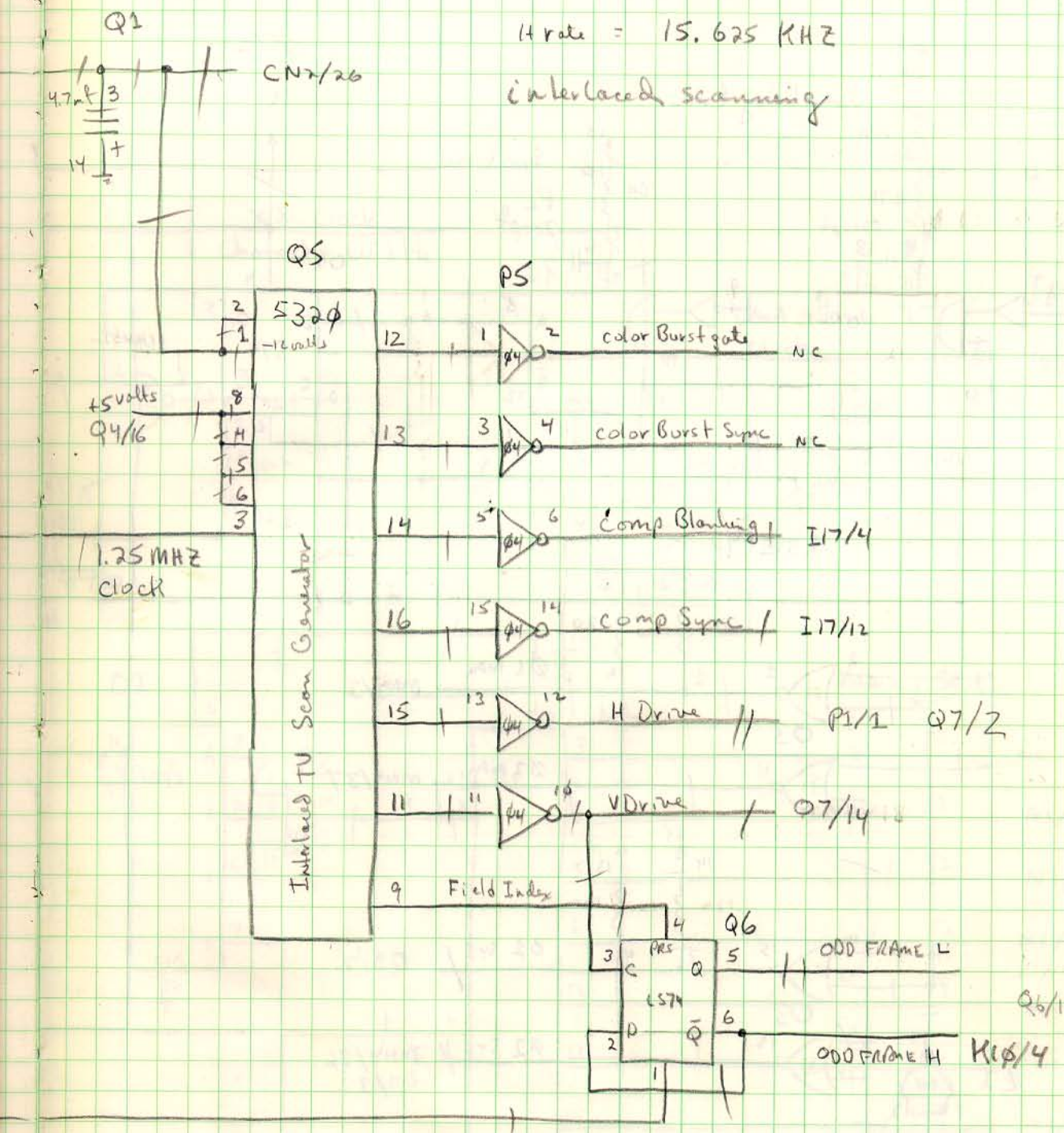
Video Sync Clock/Generator



Vrate = 59.5238 HZ

Hrate = 15.625 KHZ

interlaced scanning



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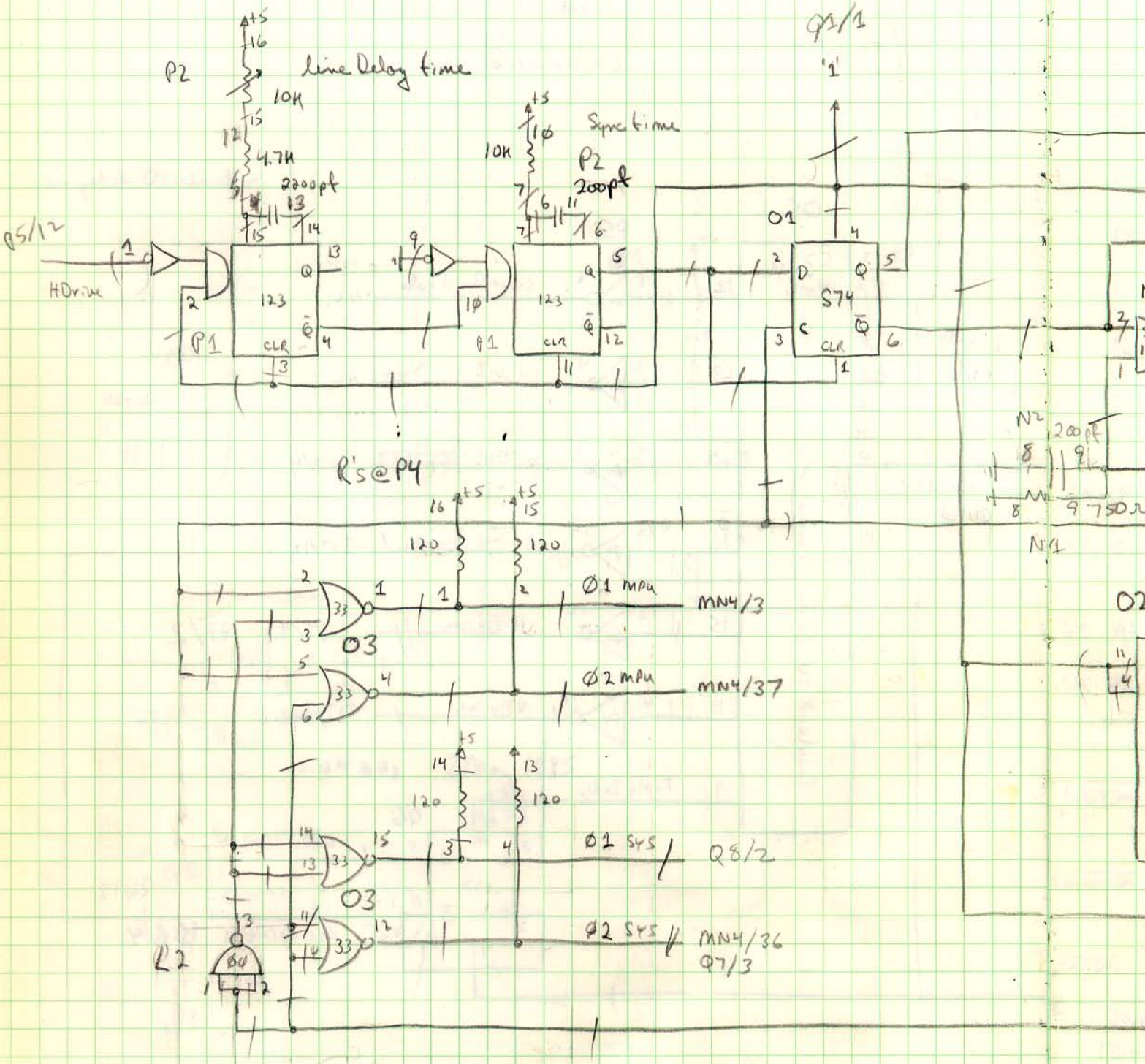
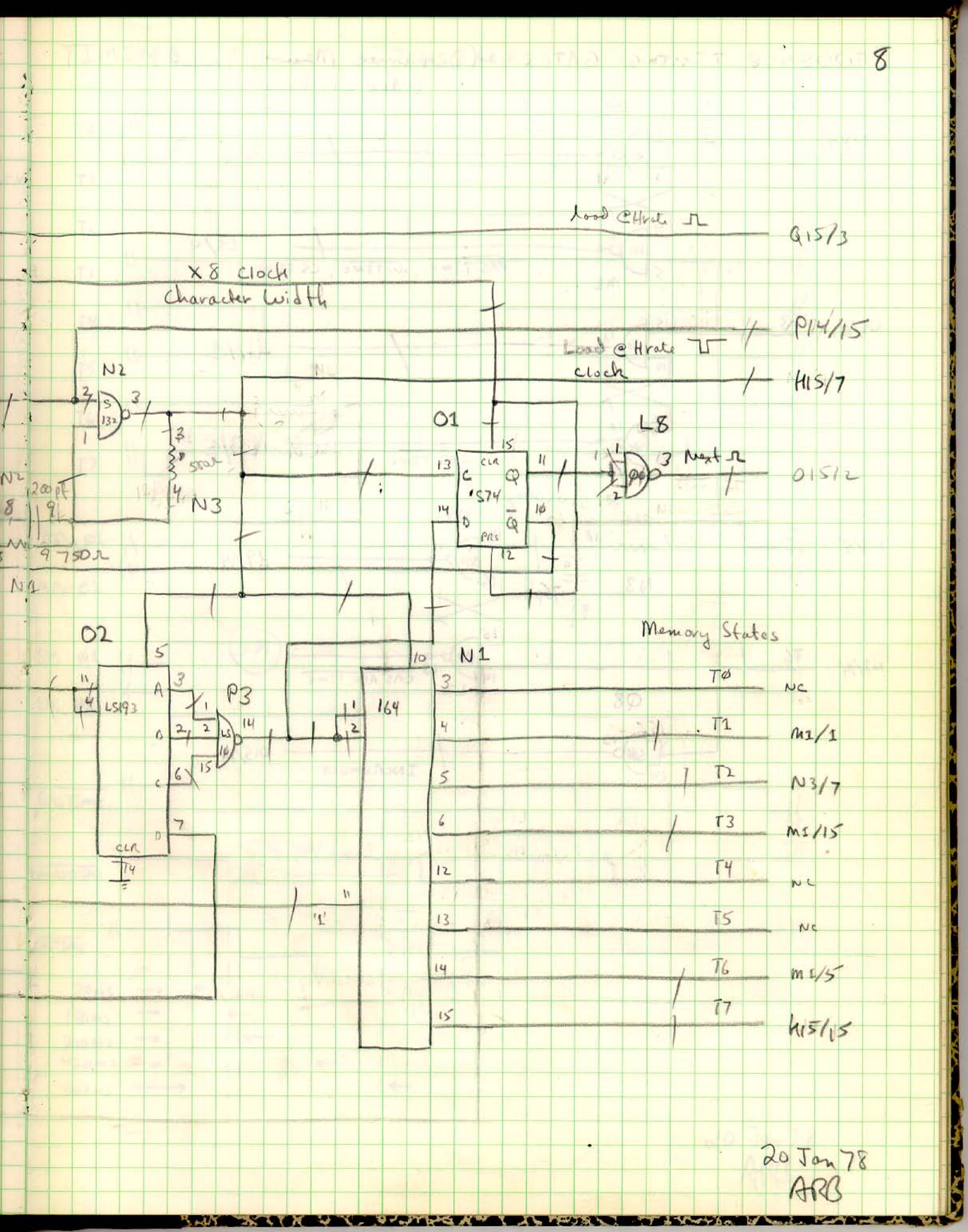
AMD

MPU Clock Generator & Scan Synchronization




load @Hrate
Q15/3
X8 clock
Character width
P14/15
Load @ Hrate
clock
H15/7
N2
01
L8
Next
01512
200pf
9.1k
9750Ω
N3
N1
02
LS193
P3
164
Memory States
T0
NC
T1
M1/1
T2
N3/7
T3
M5/15
T4
NC
T5
NC
T6
M5/5
T7
H15/15

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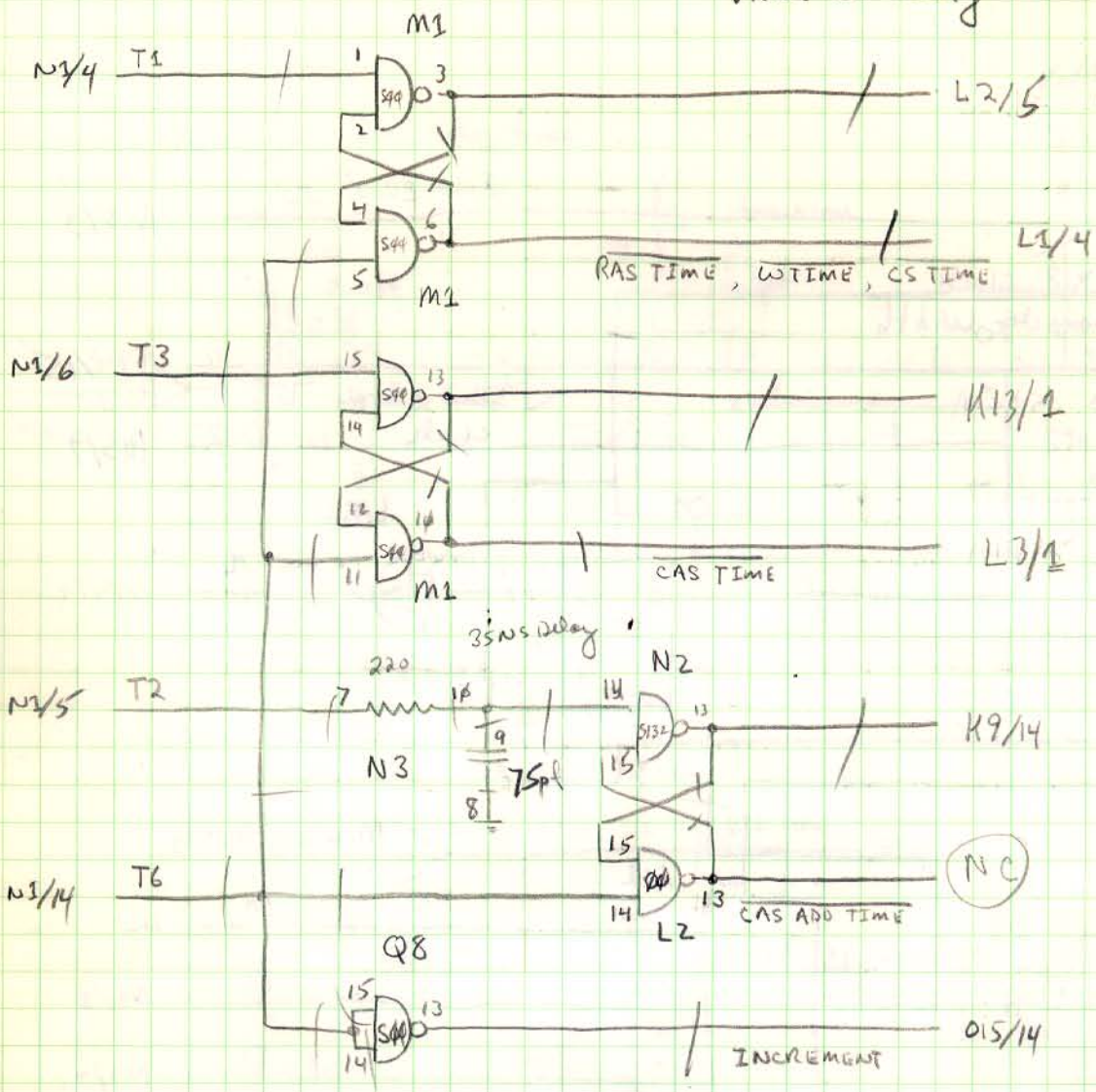
SEQUENCE TIMING GATES (Dynamic Memory Times) Video Clocking



TIM

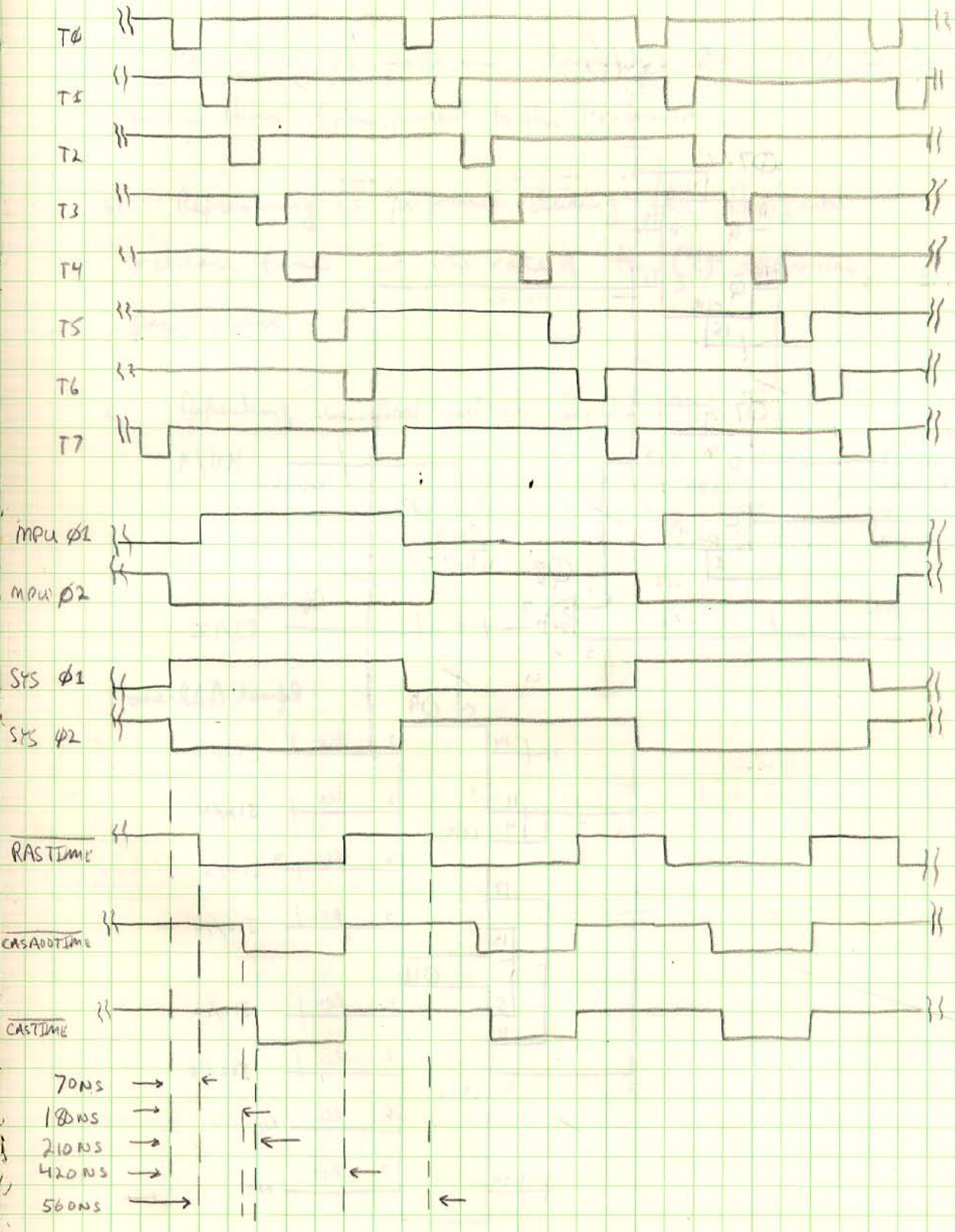
T0
T1
T2
T3
T4
T5
T6
T7

MPU Φ1
MPU Φ2
SYS Φ1
SYS Φ2

RASTIME
CASADDTIME
CASTIME

70NS
180NS
210NS
420N
560NS

TIMING ~ 70NS/div



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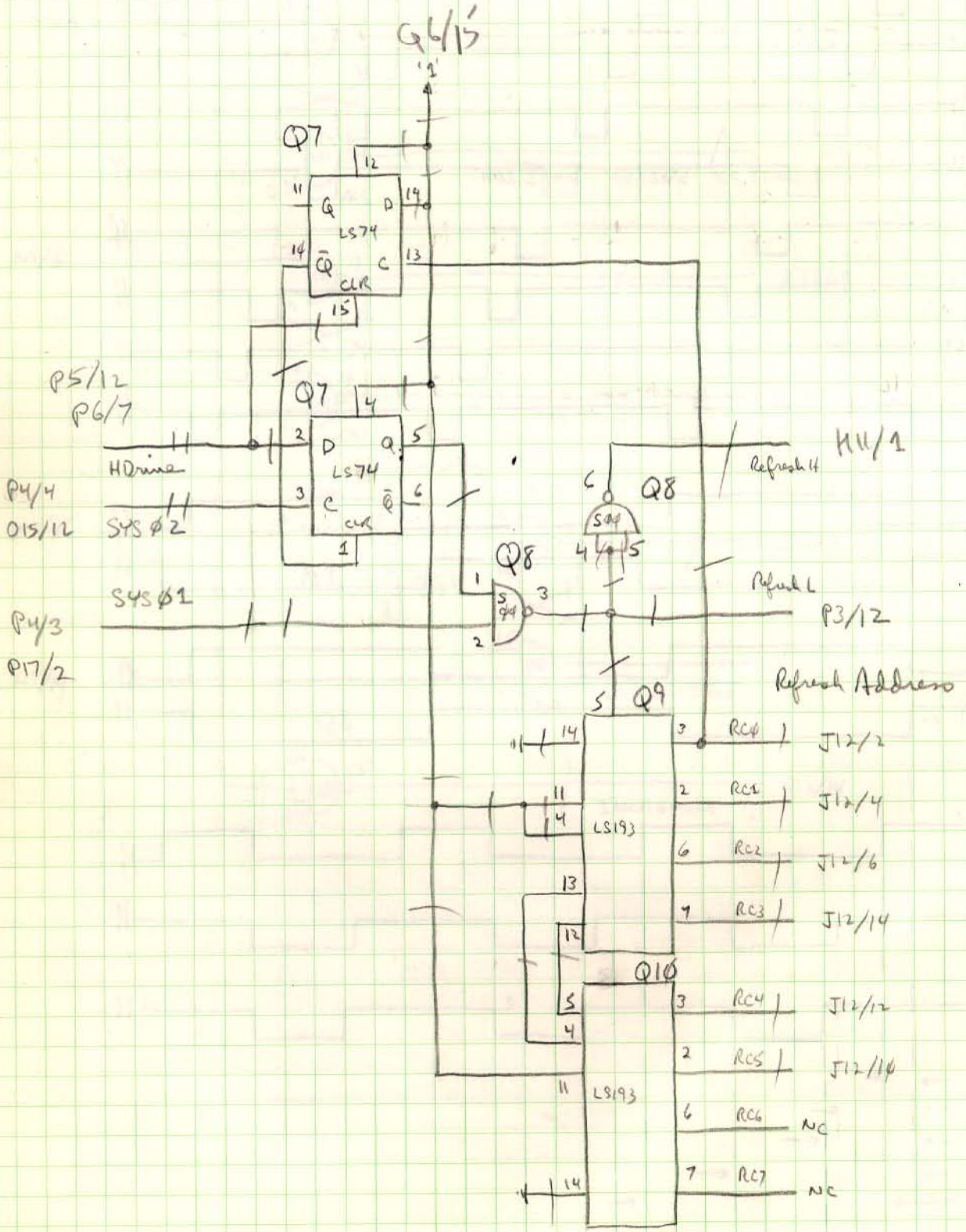
Refresh Timing and Counter



Notes:

a) Refreshing is performed during Ø1 MPU cycle and is thus transparent to the Processor

b) Refreshing is performed during the Horizontal retrace time at the rate of two (2) addresses per scan

c) Refreshing is performed in 2.03 MS.

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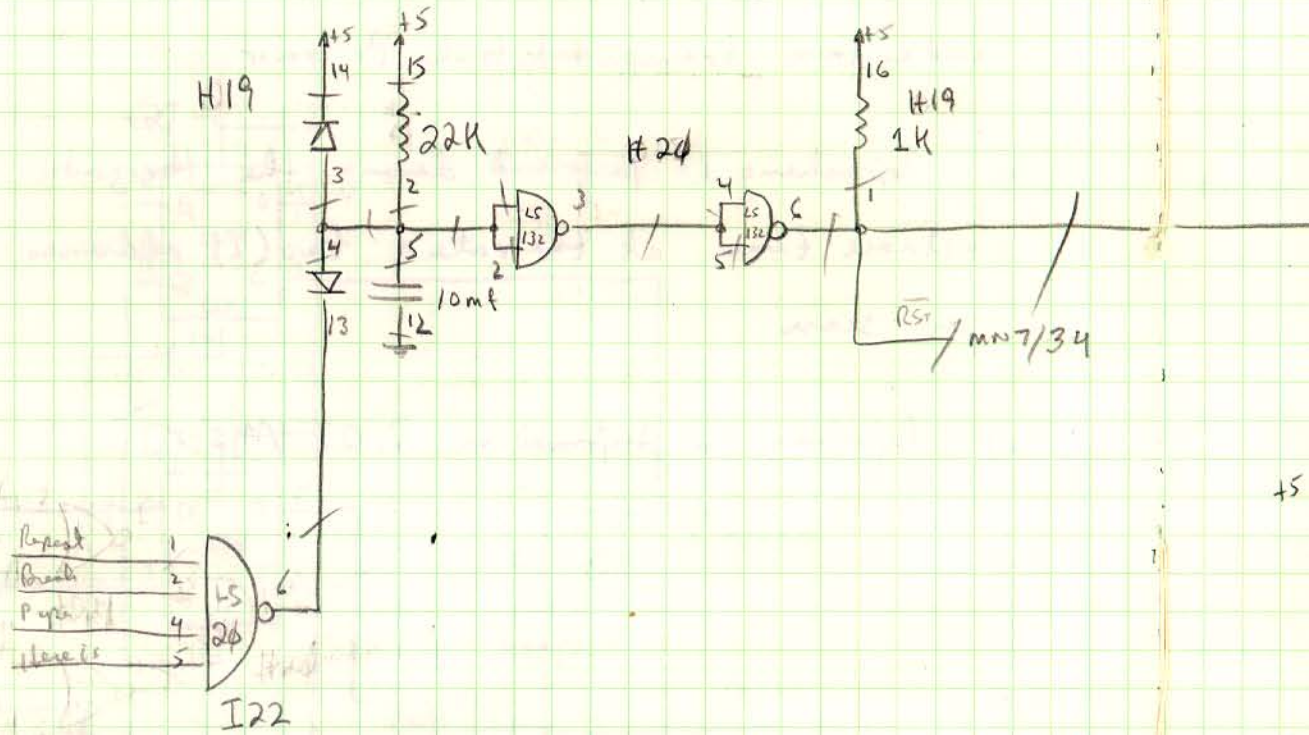
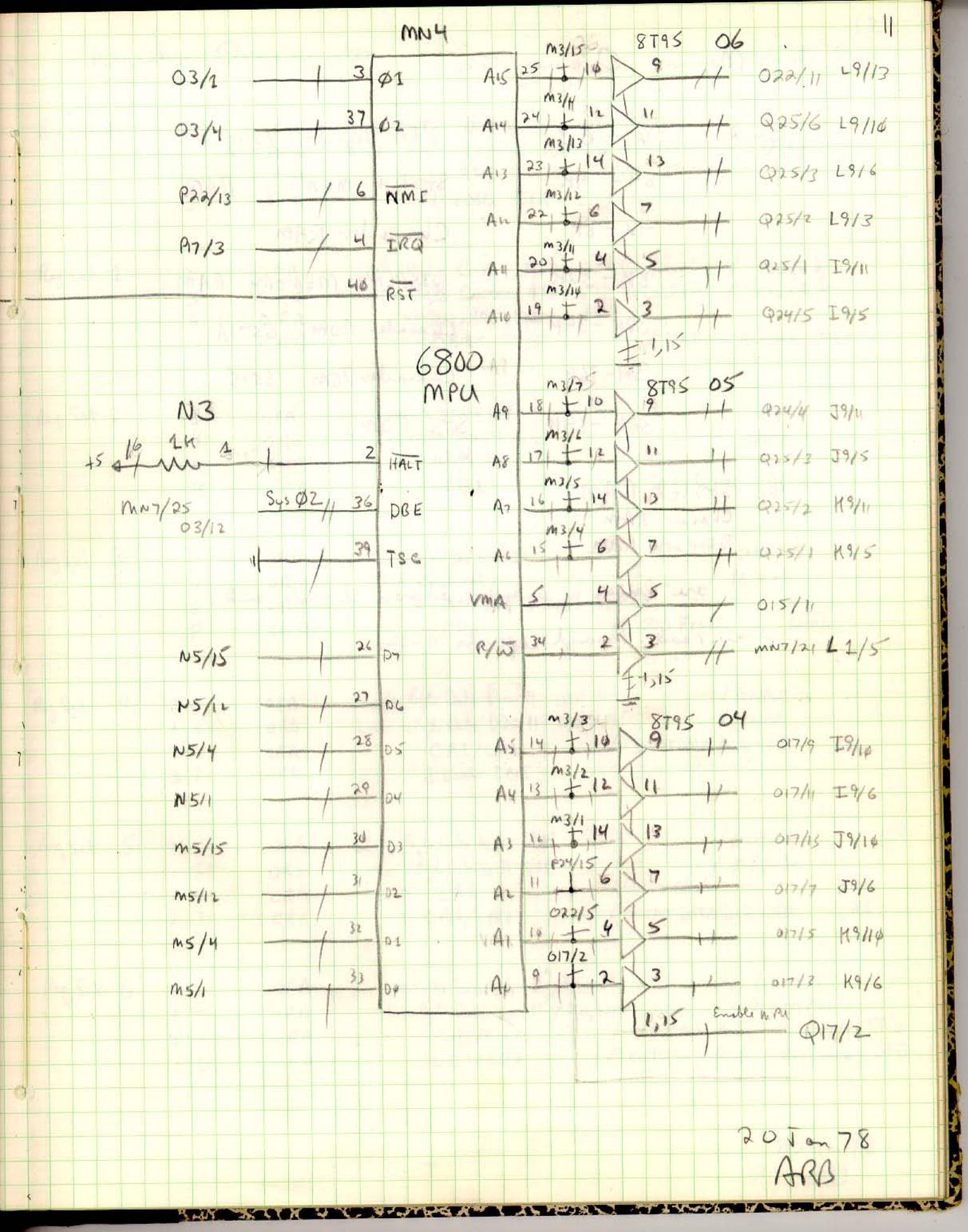
Motorola 6800 8 Bit Processor / Reset Logic



Reset by power turn on or simultaneous depression of Here Is, Paper, Break, and Repeat Buttons.


MN4
6800 MPU
8T95 06
8T95 05
8T95 04
N3
+5
1K
1/6
1
MN7/25
03/12
Sys Ø2
03/1
03/4
P22/13
A7/3
N5/15
N5/12
N5/4
N5/1
M5/15
M5/12
M5/4
M5/1
Ø1
Ø2
NMI
IRQ
RST
HALT
DBE
TSC
D7
D6
D5
D4
D3
D2
D1
D0
VMA
R/W
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
M3/15
M3/14
M3/13
M3/12
M3/11
M3/10
M3/7
M3/6
M3/5
M3/4
M3/3
M3/2
M3/1
P24/15
022/5
017/2
1,15
022/11 L9/13
Q25/6 L9/10
Q25/3 L9/6
Q25/2 L9/3
Q25/1 I9/11
Q24/5 I9/5
Q24/4 J9/11
Q25/3 J9/5
Q25/2 K9/11
Q25/1 K9/5
015/11
MN7/21 L1/5
017/9 I9/10
017/11 I9/6
017/15 J9/10
017/7 J9/6
017/5 K9/10
017/3 K9/6
Enable to PIA
Q17/2

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System Memory Organization

Basic:	Ø – 63	PIA Registers / Registers
6	64 – 4K	SYSTEM MEMORY RAM
	4K – 8K	Character RAM
	8K – 32K	DISPLAY MEMORY RAM
	32K – 34K	Character ROM 6571A
	34 – 36K	Character ROM 6575
	36K – 64K	SYS ROM's

the SYSTEM RAM
Character RAM
DISPLAY RAM

are driven by independ address lines and are read through seperate BUSES.

Reg Set

Reg Set

Reg Set

Reg Set

Reg Set

Reg Set

Reg Set

Register Organization

Reg Set Ø	Ø	ORA	High Byte Display Address Register	/ Output	
	1	ORB	Low Byte Display Address Register	/ Output	
	2	CRA	CA1	/INIT	/ IRQ
	3	CRB	disable INT		
Reg Set 1	4	ORA	High Byte Cursor Address Register	/ Output	
	5	ORB	Low Byte Cursor Address Register	/ Output	
	6	CRA	disable INT		
	7	CRB	CB1	/ Vertical Retrace	NMI
Reg Set 2	8	ORA	Current Scan Line	/ Input	
	9	ORB	Interrupt Scan Line	/ Output	
	A	CRA	disable Int		
	B	CRB	CB1	/ Scan Line	NMI
Reg Set 3	C	ORA	Character per Line	/ Output	
	D	ORB	DSP Control	/ Mixed	
	E	CRA	disable Int / NMI STROBE		USED
	F	CRB	CB1	/ ODD Frame	NMI
Reg Set 4	10	ORA	High Byte Data from 11 DSP	/ INPUT	
	11	ORB	Low Byte Data from 11 DSP	/ INPUT	
	12	CRA	CA1/CA2	/ INPUT DATA Ready DSP	IRQ
	13	CRB	disable INT		
Reg Set 5	14	ORA	High Byte Data to 11 DSP	/ Output	
	15	ORB	Low Byte Data to 11 DSP	/ output	
	16	CRA	CB1	/ 60Hz clock	IRQ
	17	CRB	CB1/CB2	/ OUTPUT DATA Read DSP	IRQ
Reg Set 6	18	ORA	Low Byte Data from 11 / Punch	/ INPUT	
	19	ORB	Low Byte Data to 11 / Keyboard	/ OUTPUT	
	1A	CRA	CA1/CA2	/ INPUT Data Ready Punch	IRQ
	1B	CRB	CB1/CB2	/ OUTPUT Data Read Keyboard	IRQ

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Reg Set 7	1C	ORA	Keyboard ASCII		/ INPUT	
	1D	ORB	Keyboard Control Keys		/ INPUT	
	1E	CRA	CA1	/ Data Ready		IRQ
	1F	CRB	disable INT	/ BELL Control		USED
Reg Set 8	20	ORA	PRINTER Control		/ Mixed	
	21	ORB	PRINTER Character		/ output	
	22	CRA	CA1/CA2	} IRQ's tied together		
	23	CRB	CB1/CB2	} / Printer finished		IRQ
Reg Set 9	24	ORA	Photoreader		/ INPUT	
	25	ORB	NPR Control		/ MIXED	
	26	CRA	CA1/CA2	/ Data Ready Photoreader		IRQ
	27	CRB	CB1/CB2	/ Transfer finished NPR		IRQ
Reg Set 10	28	ORA	High Byte NPR Address		/ OUTPUT	
	29	ORB	Low Byte NPR Address		/ OUTPUT	
	2A	CRA	disable INT or	Key Tape ←		IRQ
	2B	CRB	disable INT or	Key Tape →		IRQ
Reg Set 11	2C	ORA	High Byte Data to 11		/ OUTPut	
	2D	ORB	Low Byte Data to 11		/ OUTput	
	2E	CRA	disable INT or	Key Home Is		IRQ
	2F	CRB	disable INT or	Key Paper		IRQ
Reg Set 12	30	ORA	High Byte from 11		/ INPUT	
	31	ORB	Low Byte from 11		/ INPUT	
	32	CRA	disable INT or	Key Break		IRQ
	33	CRB	disable INT or	Key Repeat		IRQ
Reg Set 13			Not Used			

Reg Set 14 Not Used

Reg Set 15 Not Used

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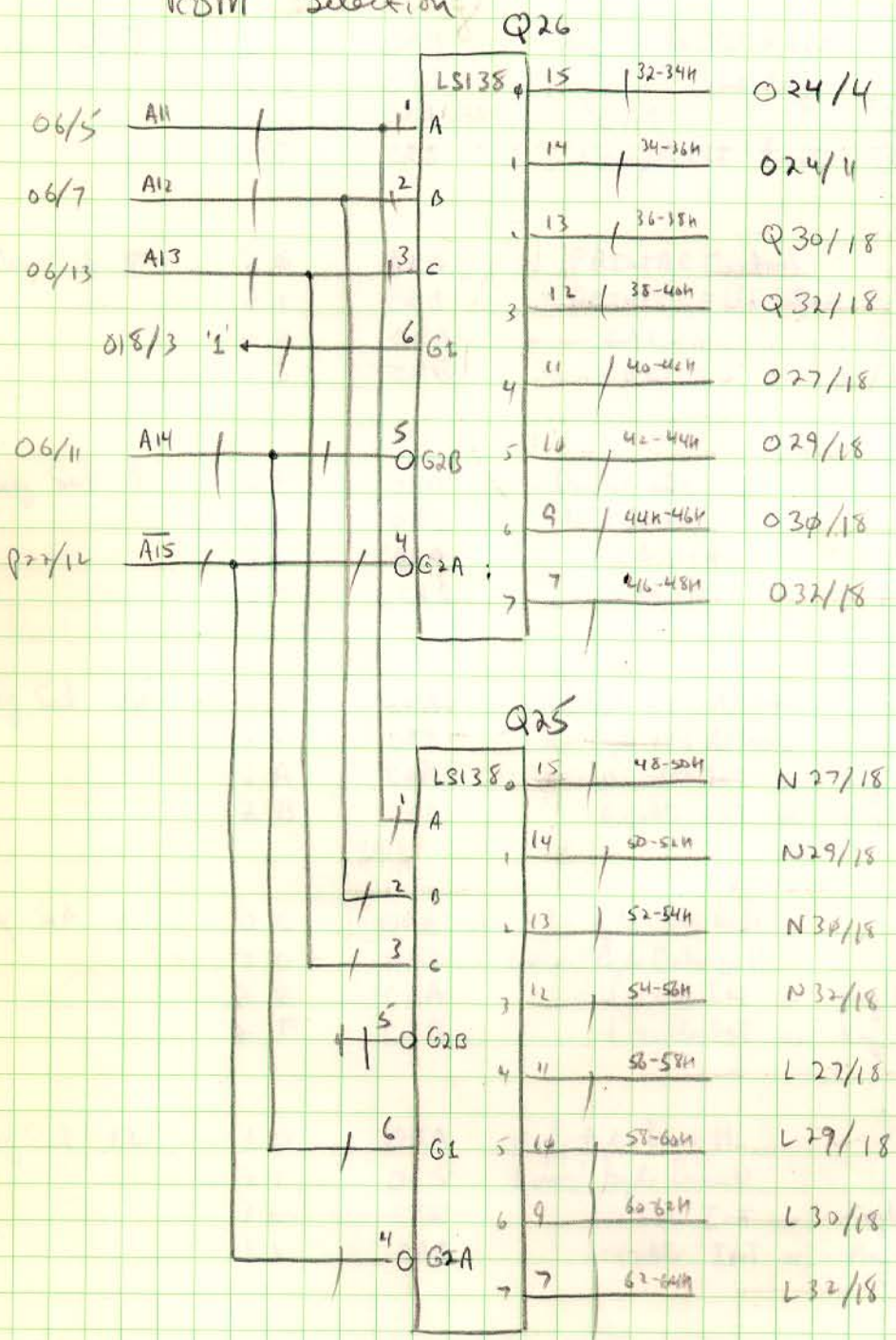
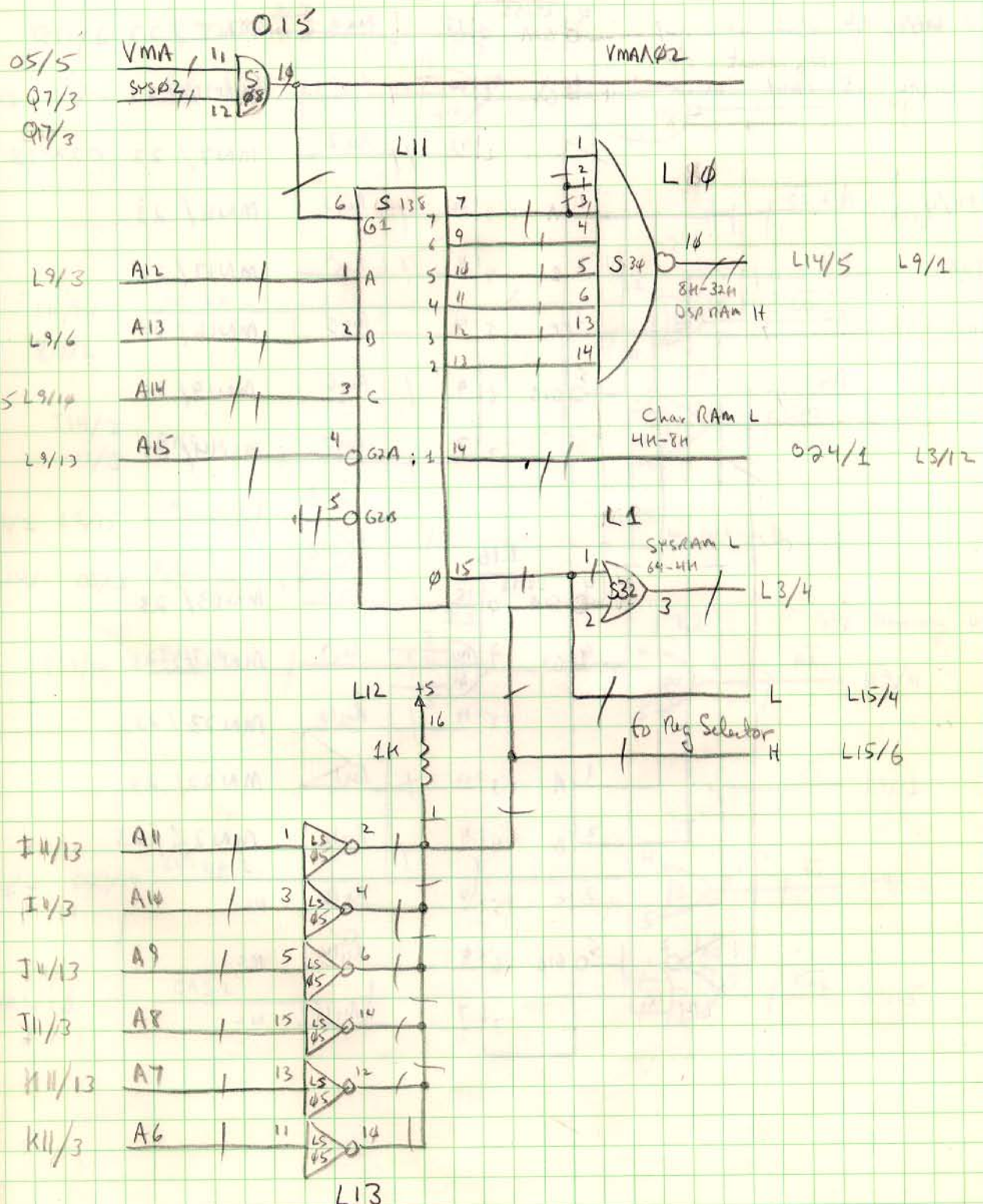
MPU Memory Address Decoding

ROM Selection



RAM Selection



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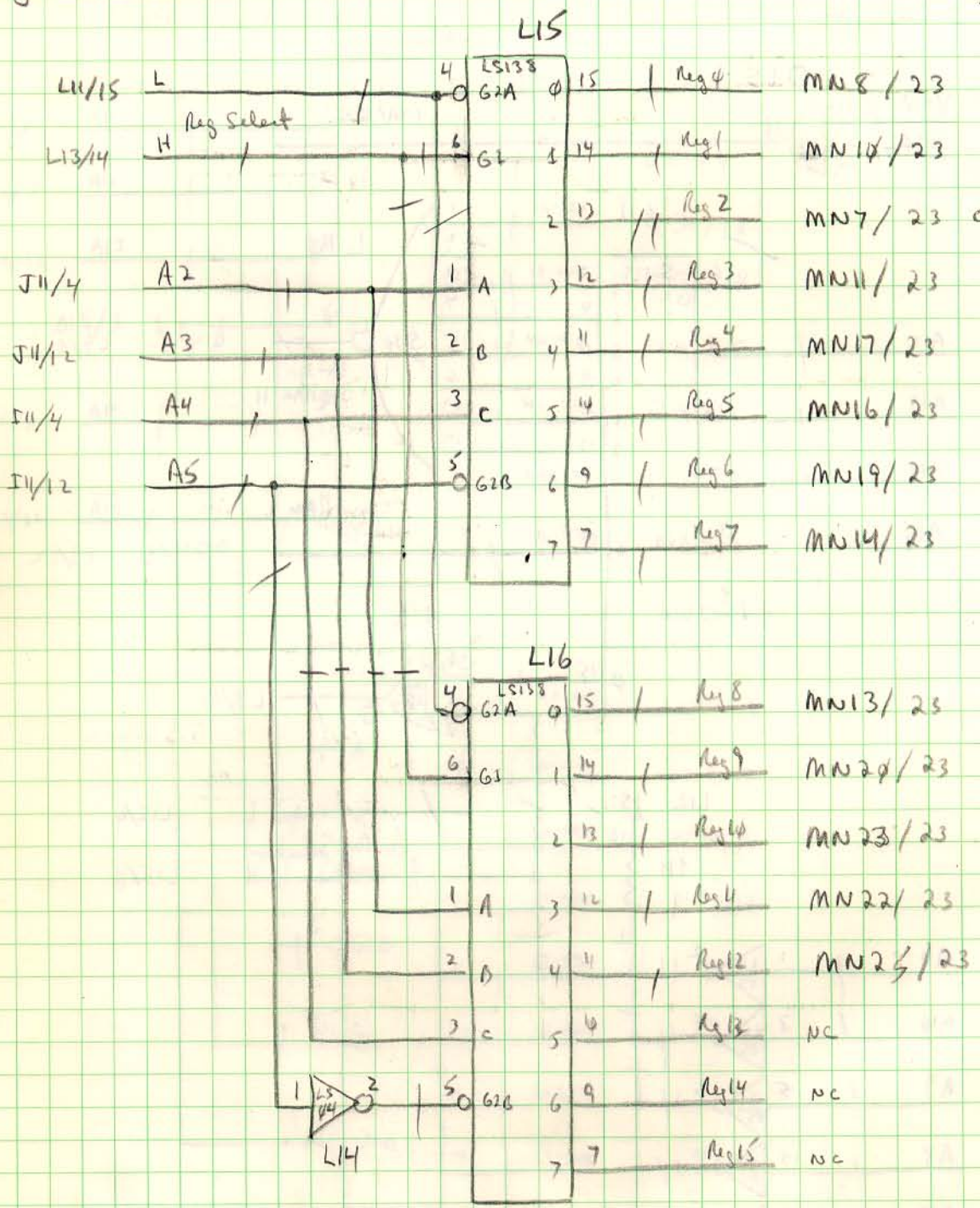
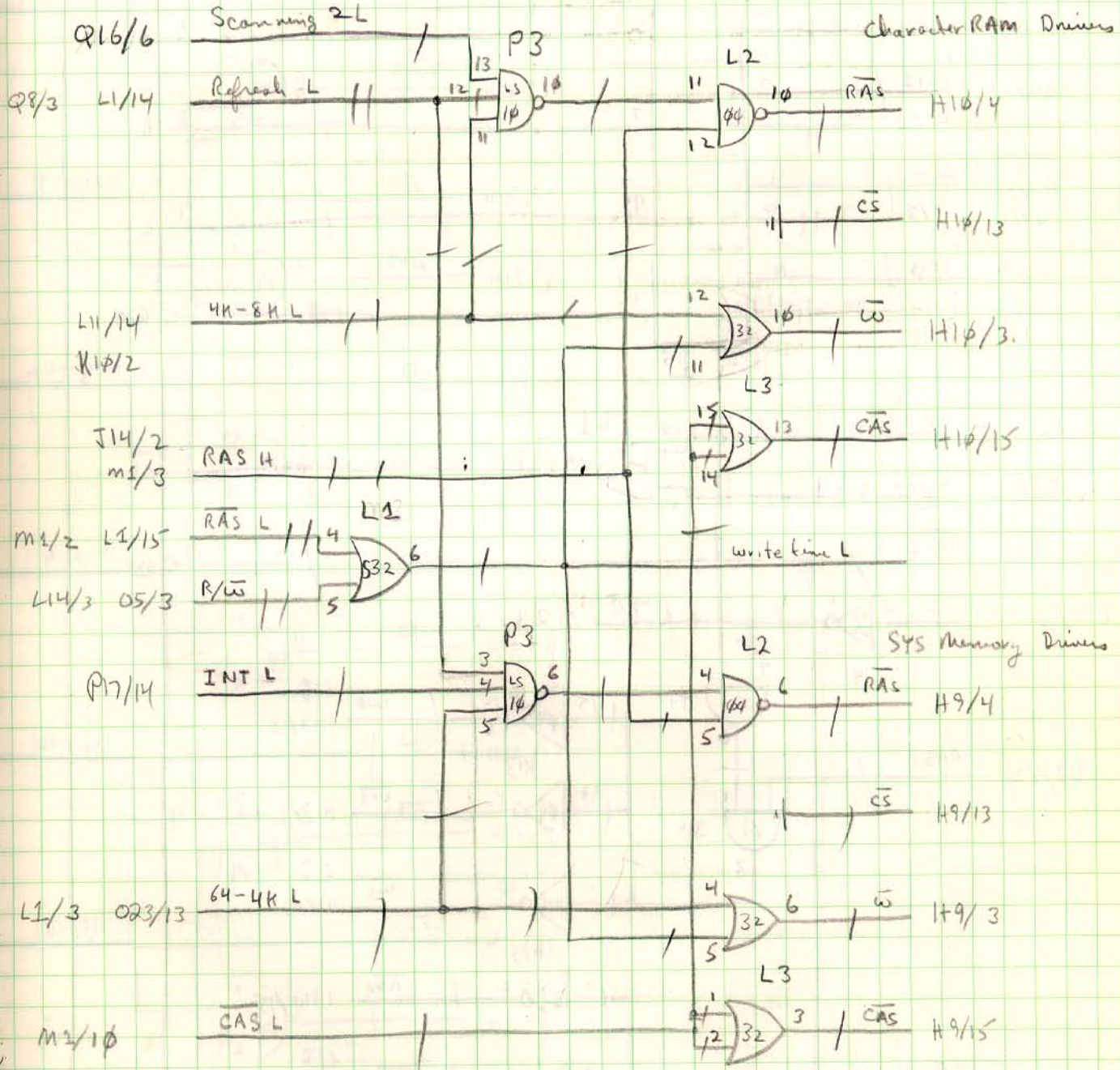
APB

Reg/PIA Selects



Character RAM / SYSTEM RAM Read/write Control Logic



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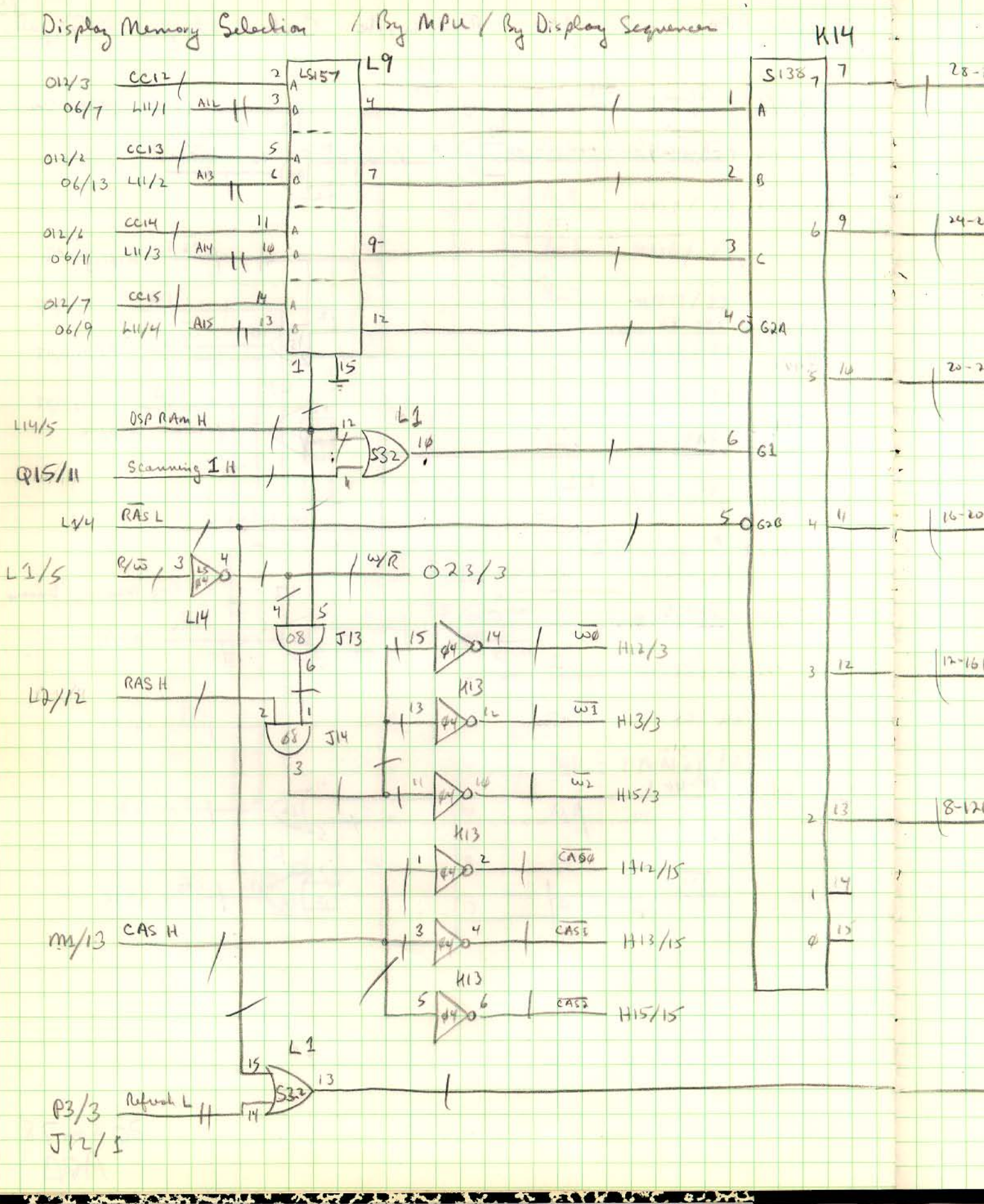
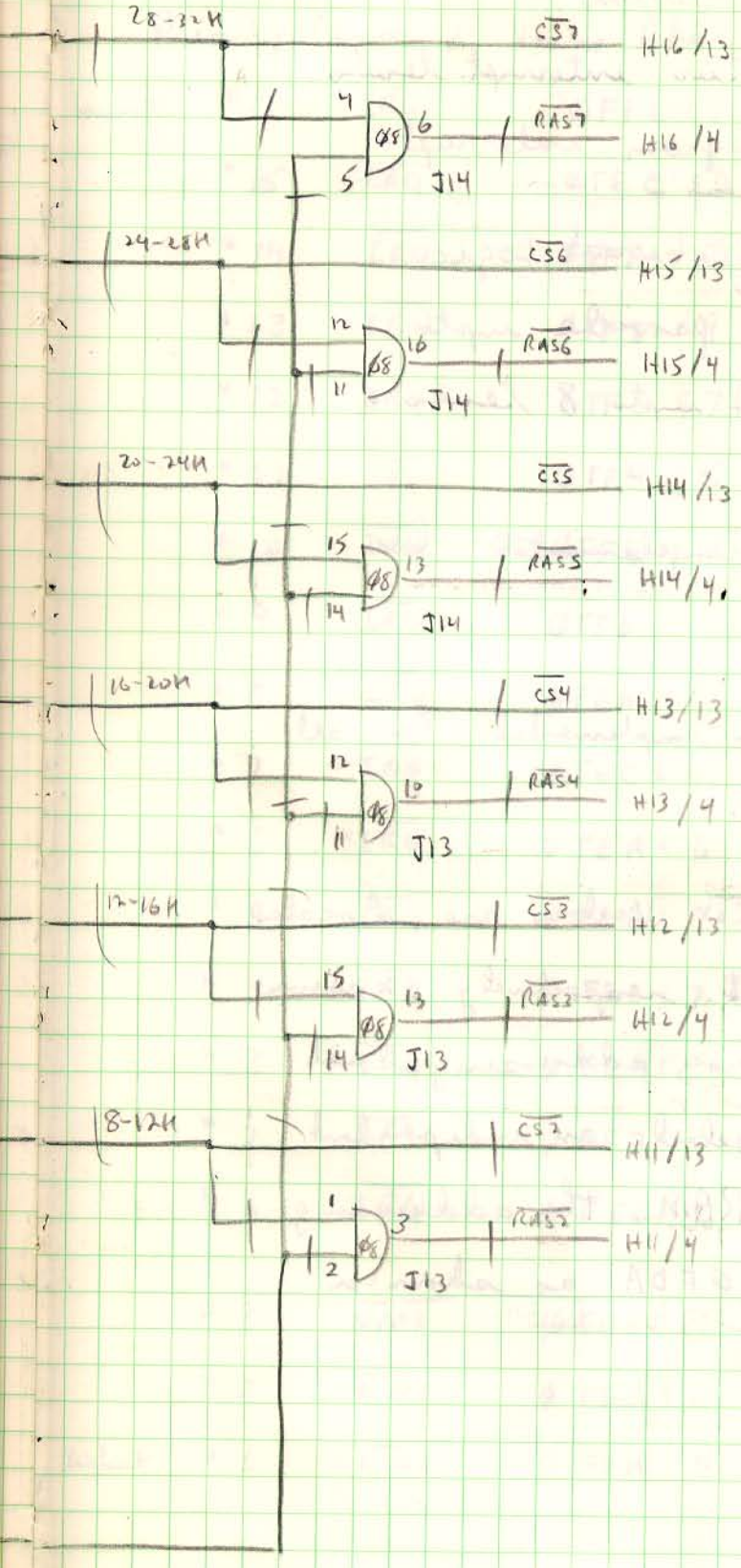
ARB

Display Memory Selection / By MPU / By Display Sequencer




28-32K
CS7
H16/13
4
5
Ø8
6
RAS7
H16/4
J14
24-28K
CS6
H15/13
12
11
Ø8
10
RAS6
H15/4
J14
20-24K
CS5
H14/13
15
14
Ø8
13
RAS5
H14/4
J14
16-20K
CS4
H13/13
12
11
Ø8
10
RAS4
H13/4
J13
12-16K
CS3
H12/13
15
14
Ø8
13
RAS3
H12/4
J13
8-12K
CS2
H11/13
1
2
Ø8
3
RAS2
H11/4
J13

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ARO

Special Notes on the Interrupt Logic

The 6800 has only two interrupt levels for externally triggered program interrupts.

A multilevel Vectored interrupt Logic system has been added to provide upto 16 levels for $\overline{IRQ}$'s and upto 8 levels of $\overline{NMI}$'s.

Three $\overline{NMI}$ levels are implemented for the CRT Display Control.

System $\overline{IRQ}$ levels are implemented for all remaining Control functions.

The Normal $\overline{NMI}$ and $\overline{IRQ}$ Vectors are located at FFFD/FFFC and FFF9/FFF8 respectively, however the Logic modifies the Memory addressing such that each interrupt level selects an independent vector from the System RAM. The addressing selects locations ØFFF to ØFDA as shown on the next page.

Priority levels		& Fleetline Vector Addresses	Function
Lowest	H 16 IRQ	ØFFE & F	Key Repeat
	H 15 IRQ	ØFFC & D	Key Break
	H 14 IRQ	ØFFA & B	Key Paper
	H 13 IRQ	ØFF8 & 9	Key Here Is
	H 12 IRQ	ØFF6 & 7	Key Tape →
	H 11 IRQ	ØFF4 & 5	Key Tape ←
	H 10 IRQ	ØFF2 & 3	NPR TRANS
	H 9 IRQ	ØFF0 & 1	DSP OUTPUT DATA
	H 8 IRQ	ØFEE & F	DSP INPUT DATA
	H 7 IRQ	ØFEC & D	Data OUT to PDP11
	H 6 IRQ	ØFEA & B	Data IN fm PDP11
	H 5 IRQ	ØFE8 & 9	Keyboard
	H 4 IRQ	ØFE6 & 7	PRINTER
	H 3 IRQ	ØFE4 & 5	Photoreader
	H 2 IRQ	ØFE2 & 3	60 HZ Clock
	H 1 IRQ	ØFE0 & 1	BUS INIT (CPU)
	H 3 NMI	ØFDE & F	LINE SCAN
	H 2 NMI	ØFDC & D	VERTICAL BLANK
Highest	H 1 NMI	ØFDA & B	ODD FRAME

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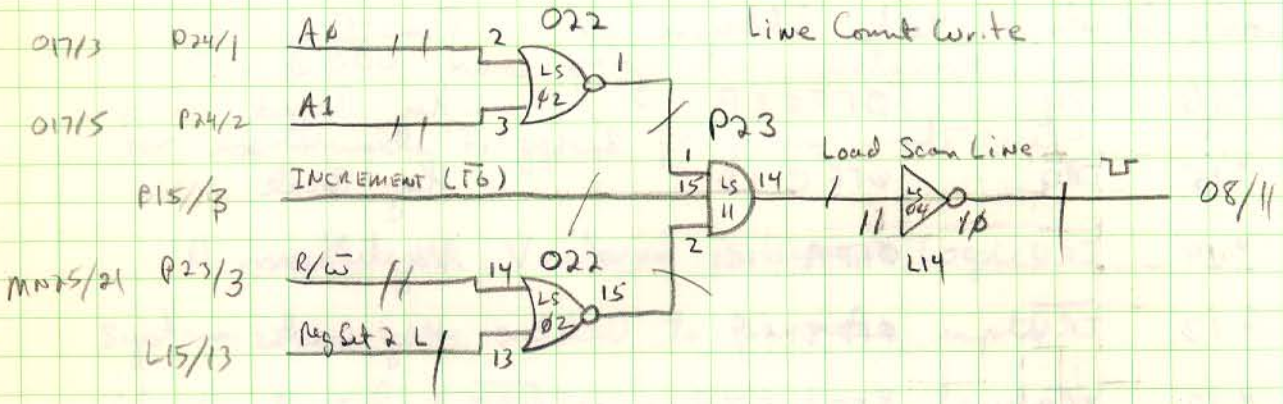
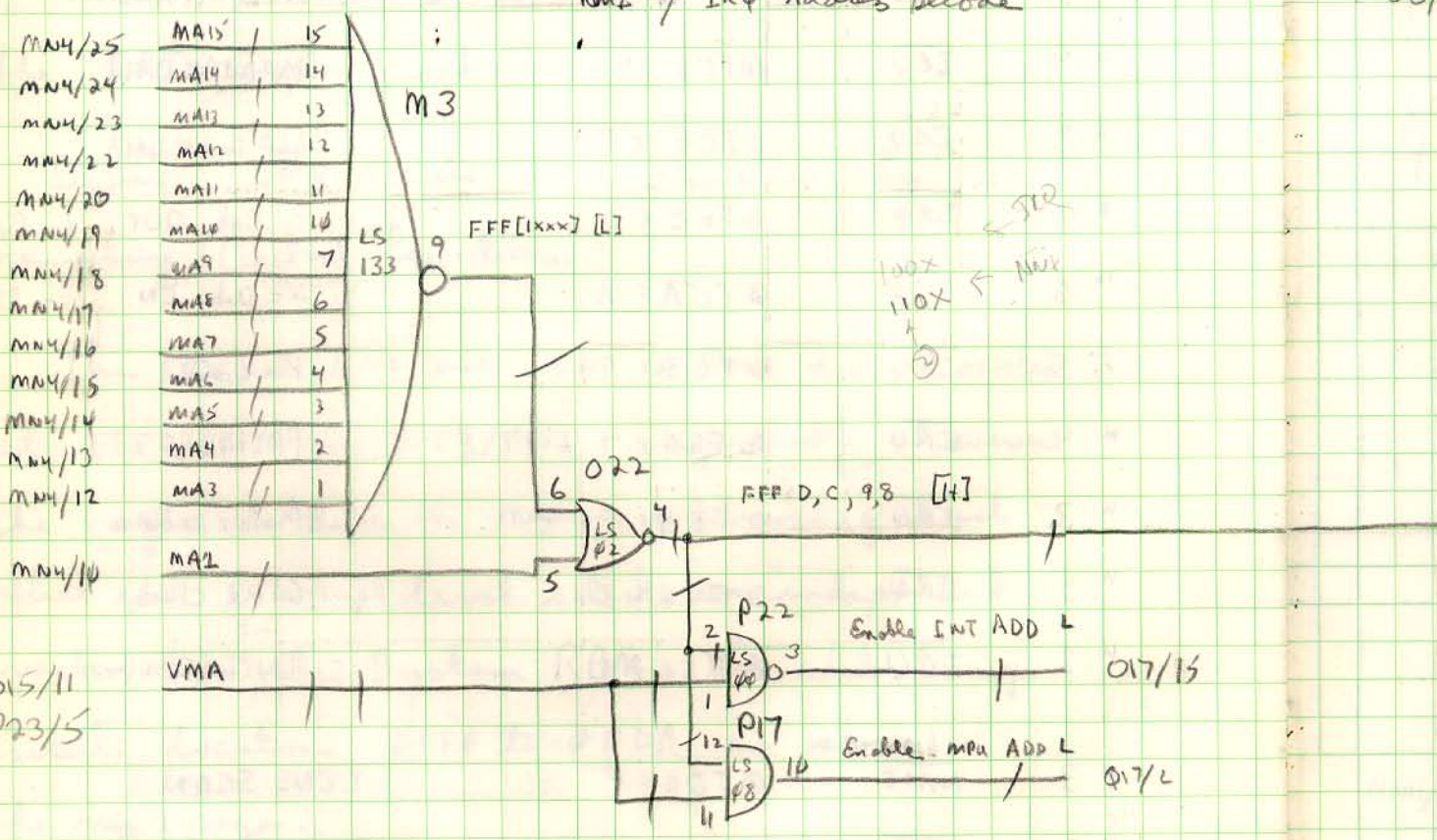
ARD

Line Counter Write Logic / MPU Bus Control Logic





$\overline{NMI}$ or $\overline{IRQ}$ Access Control

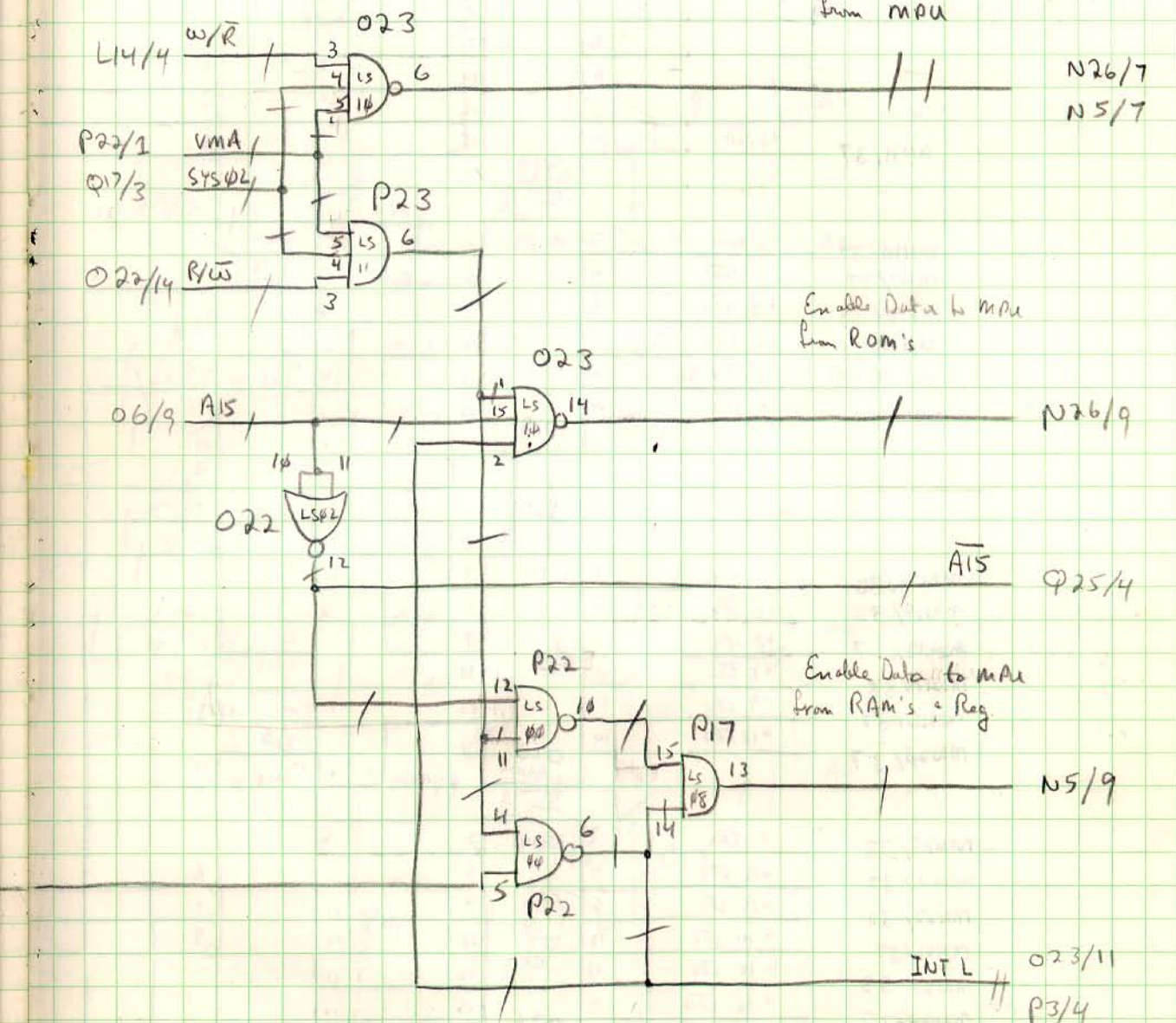


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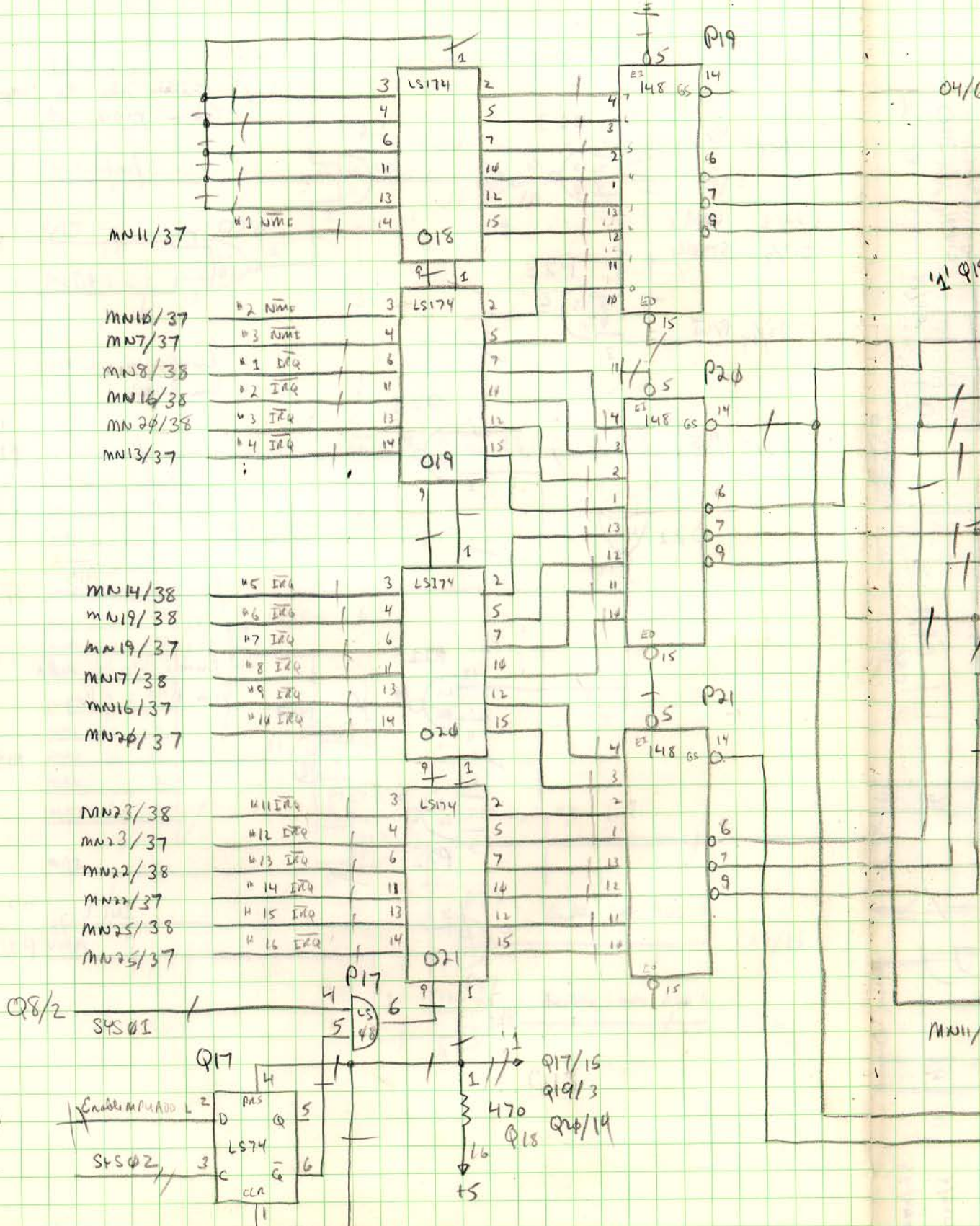
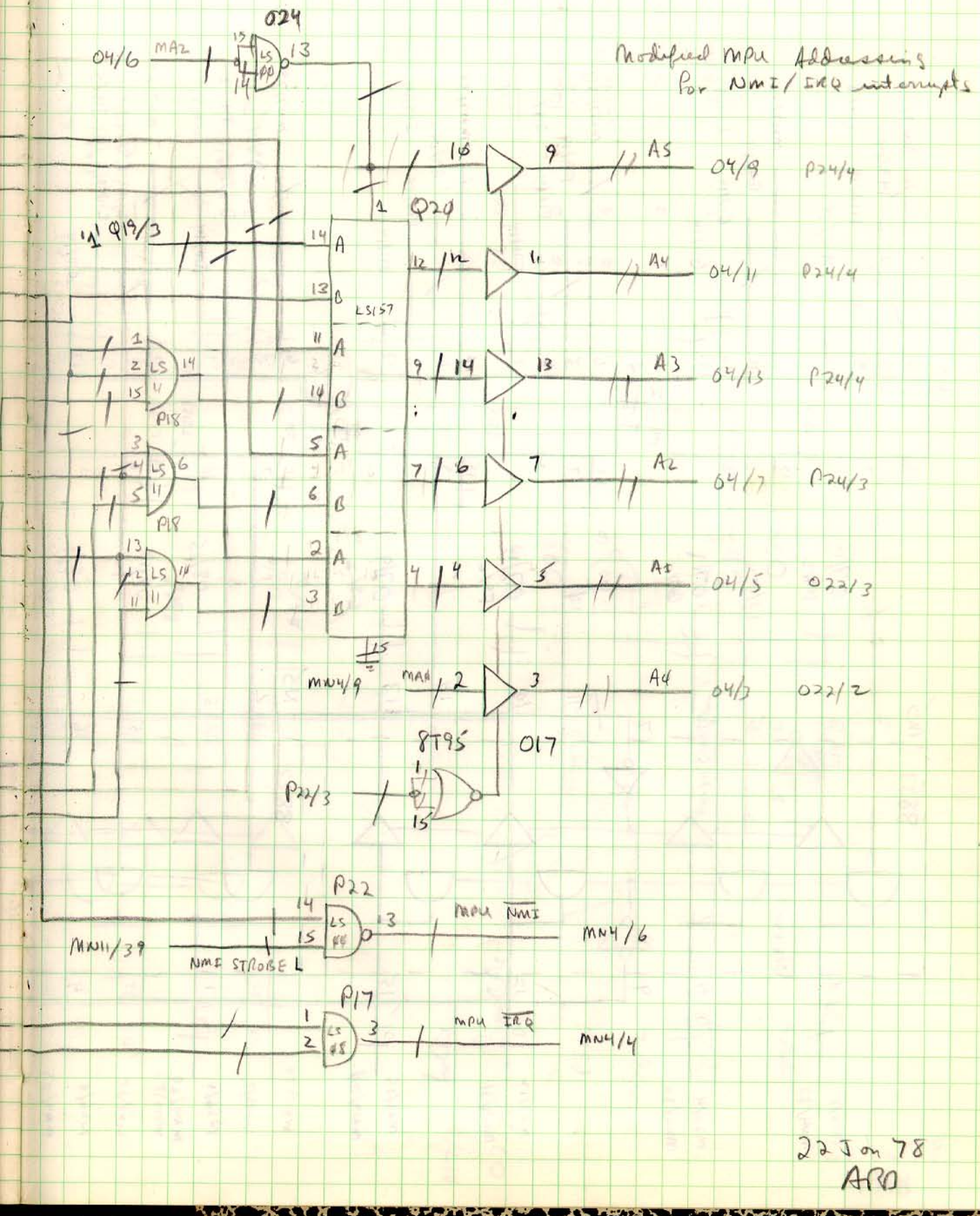
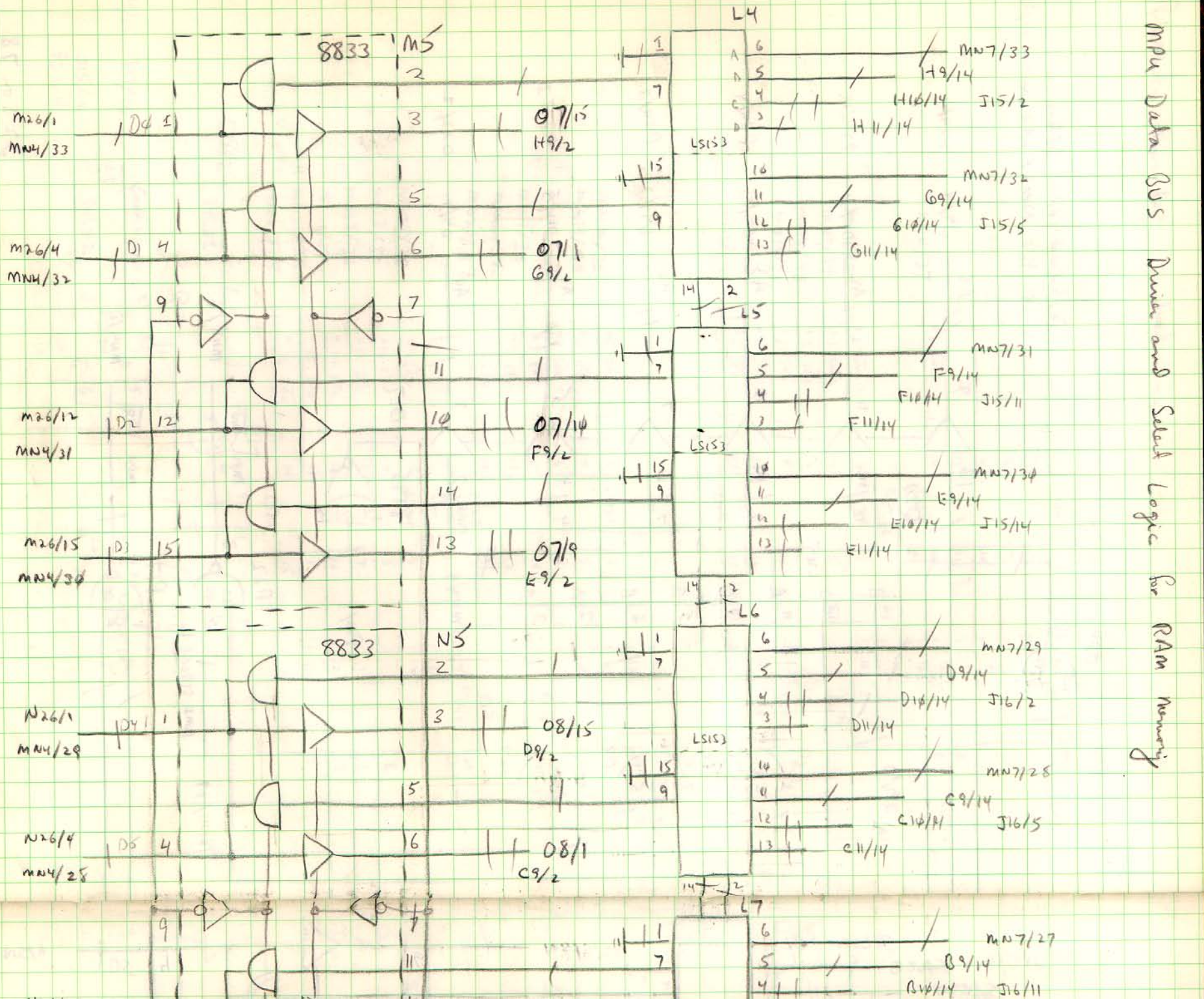
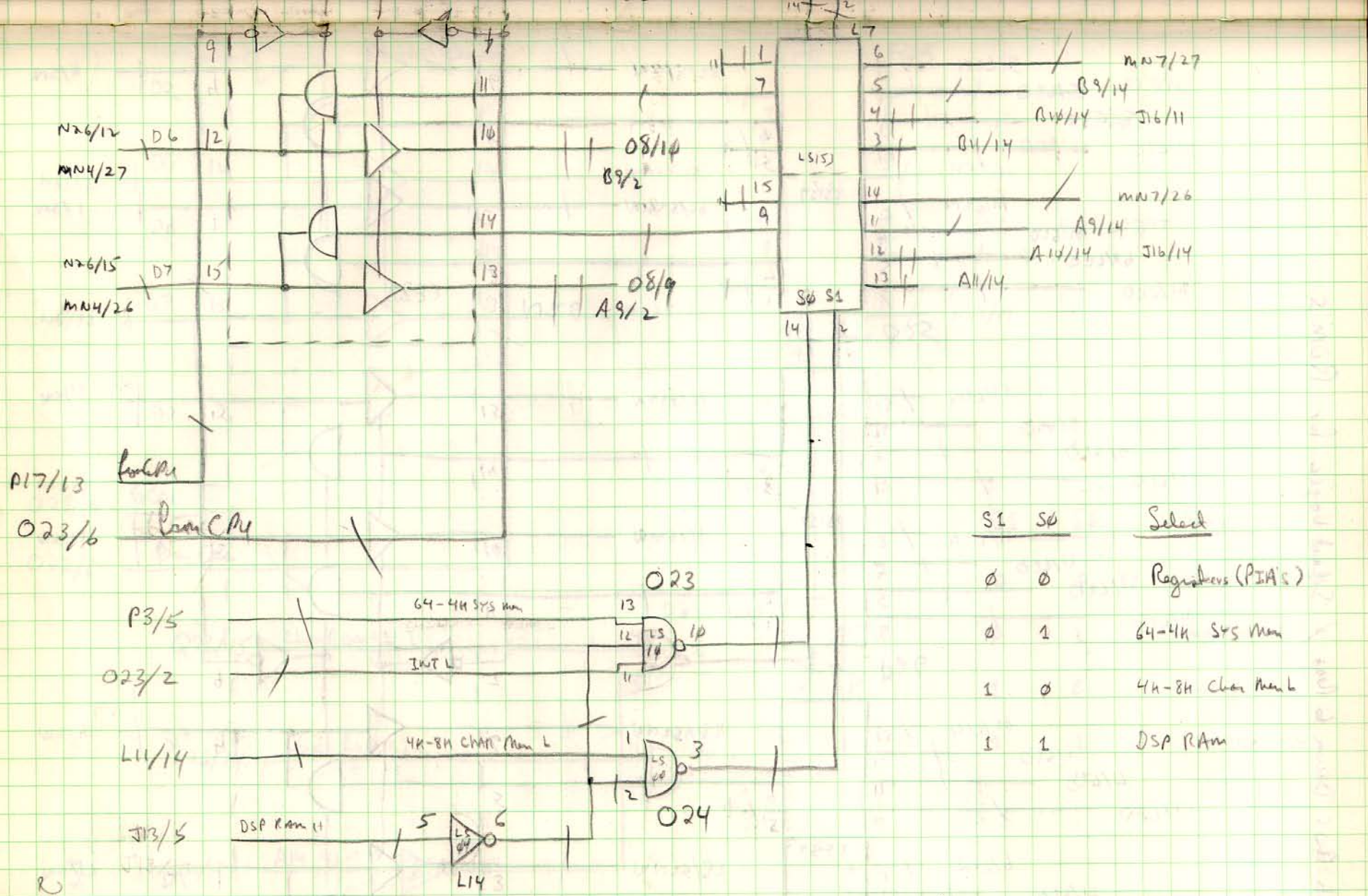
ABB

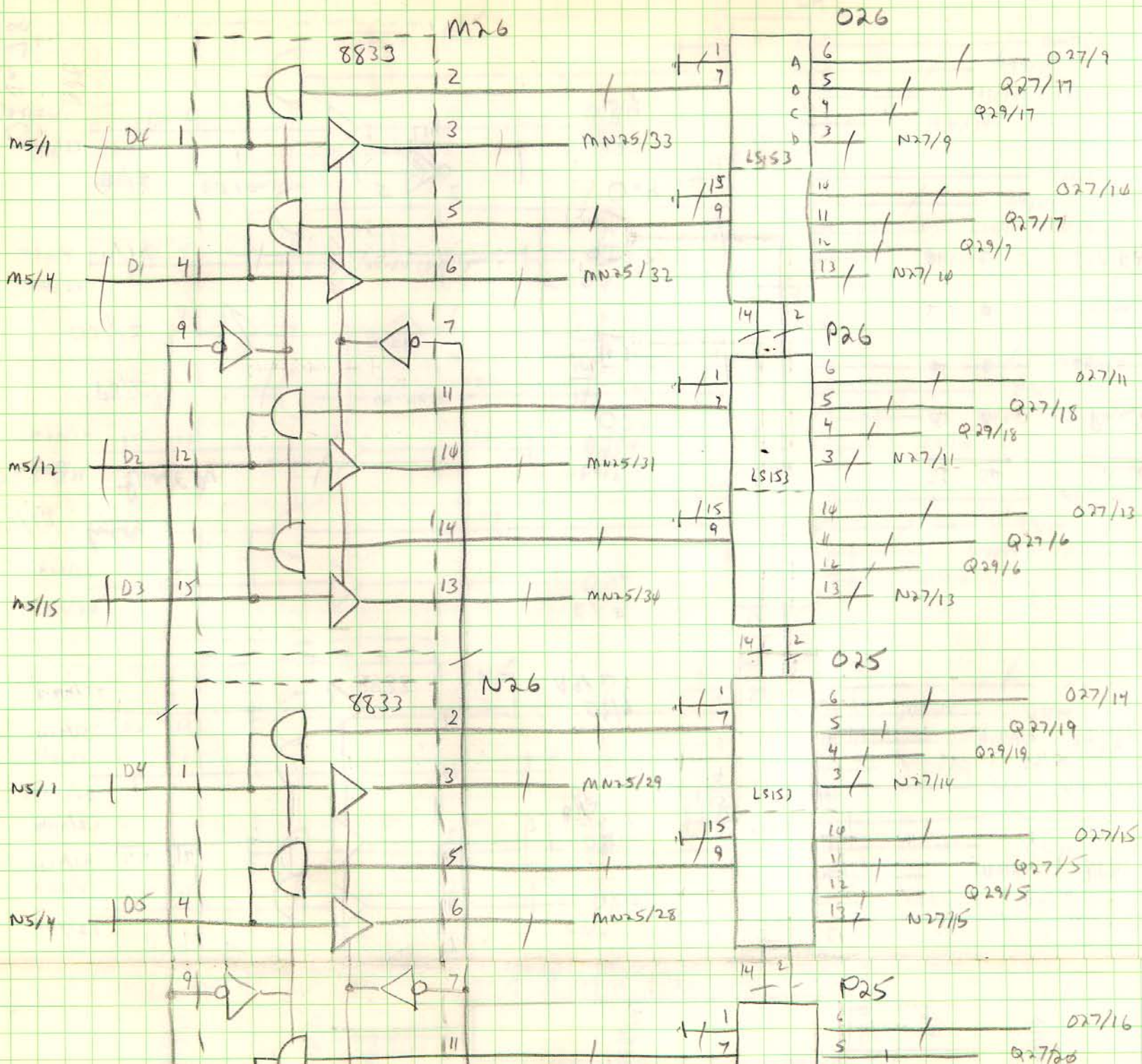
Priority Encoder & Control Logic



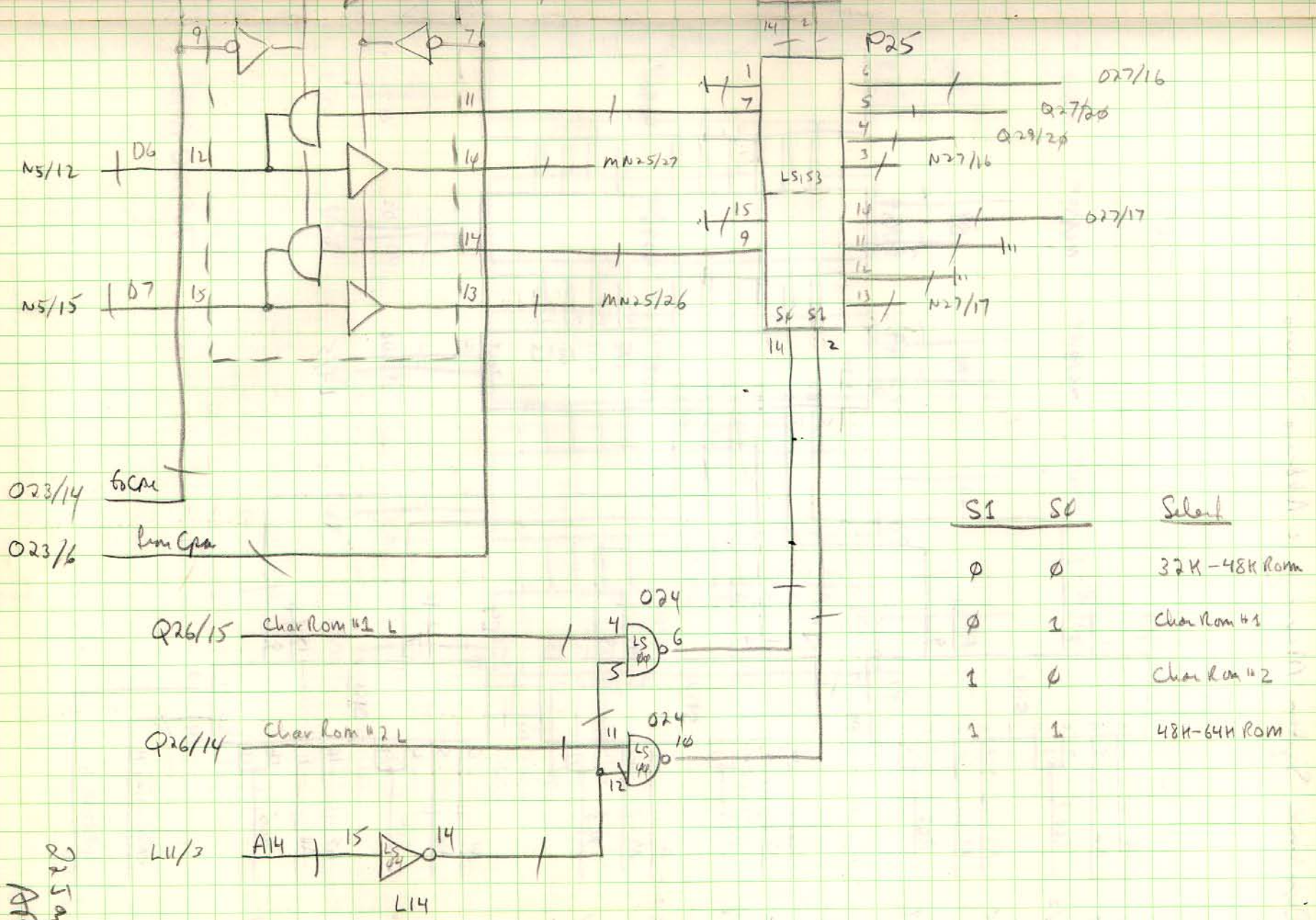

Modified MPU Addressing
For NMI/IRQ interrupts
O24
04/6
MA2
LS 00
Q20
LS157
'1' Q19/3
P18
P18
A5
04/9
P24/4
A4
04/11
P24/4
A3
04/13
P24/4
A2
04/7
P24/3
A1
04/5
022/3
MN4/9
MA4
A4
04/3
022/2
8T95
017
P22/3
P22
LS 00
MPU NMI
MN11/39
NMI STROBE L
MN4/6
P17
LS 08
MPU IRQ
MN4/4


MPU Data BUS Driver and Select Logic for RAM Memory
8833
M5
M26/1
MN4/33
D4
07/15
H9/2
M26/4
MN4/32
D1
07/1
G9/2
M26/12
MN4/31
D2
07/10
F9/2
M26/15
MN4/30
D3
07/9
E9/2
8833
N5
N26/1
MN4/29
D4
08/15
D9/2
N26/4
MN4/28
D6
08/1
C9/2
L4
LS153
MN7/33
H9/14
H16/14
J15/2
H11/14
MN7/32
G9/14
G10/14
J15/5
G11/14
L5
MN7/31
F9/14
F10/14
J15/11
F11/14
MN7/30
E9/14
E10/14
J15/14
E11/14
L6
MN7/29
D9/14
D10/14
J16/2
D11/14
MN7/28
C9/14
C10/14
J16/5
C11/14
L7
MN7/27
B9/14
B10/14
J16/11


N26/12
D6
MN4/27
08/14
B9/2
N26/15
D7
MN4/26
08/9
A9/2
LS153
MN7/27
B9/14
B10/14
J16/11
B11/14
MN7/26
A9/14
A10/14
J16/14
A11/14
S0 S1
P17/13
from CPU
023/6
from CPU
023
P3/5
64-4H SYS Mem
INT L
023/2
L11/14
4H-8H CHAR Mem L
J13/5
DSP RAM H
LS08
LS00
L14
024
S1 S0 Select
0 0 Registers (PIA's)
0 1 64-4H SYS Mem
1 0 4H-8H Char Mem L
1 1 DSP RAm

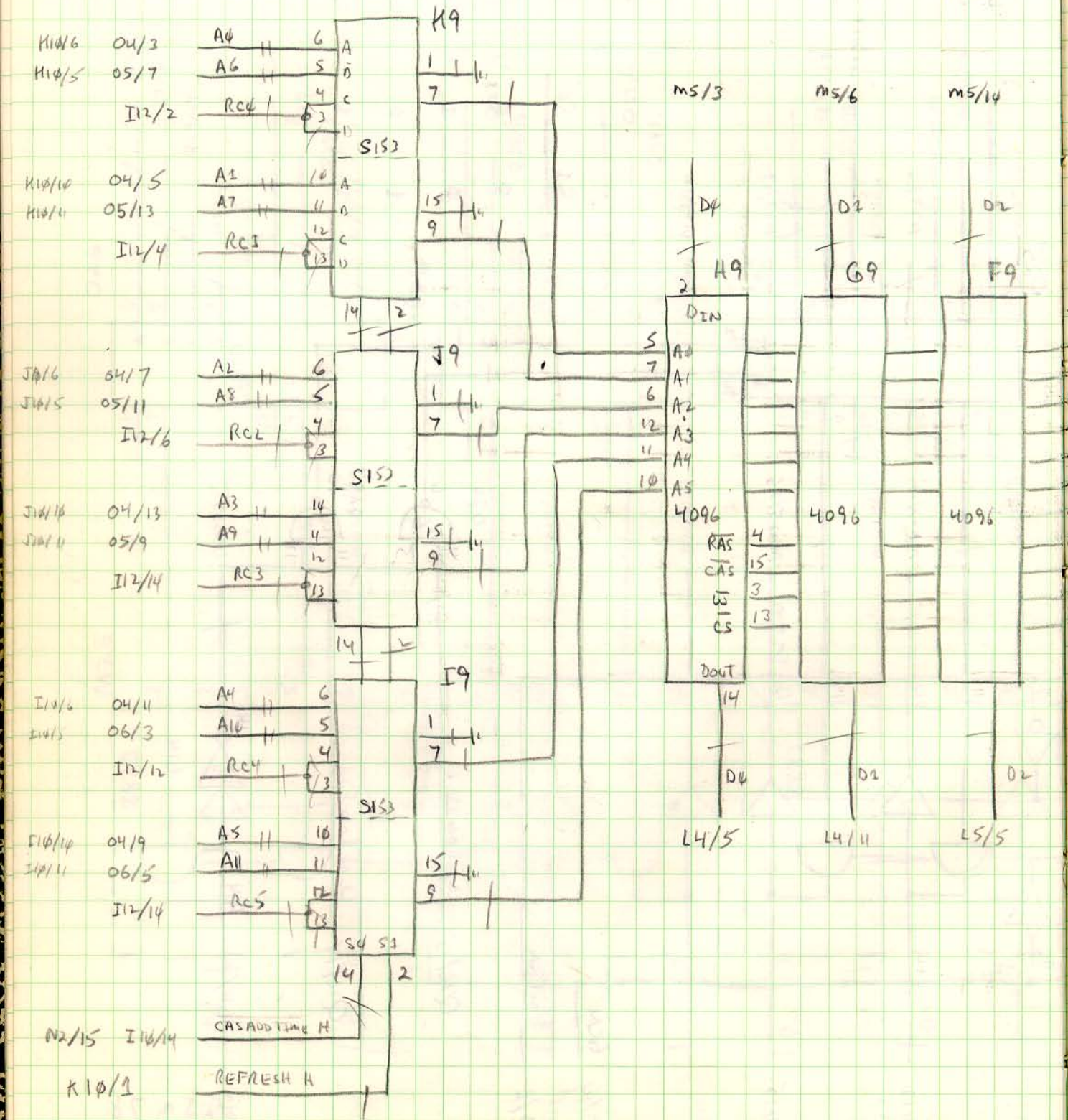


MPU Data Bus Drivers / Select Logic for ROM's

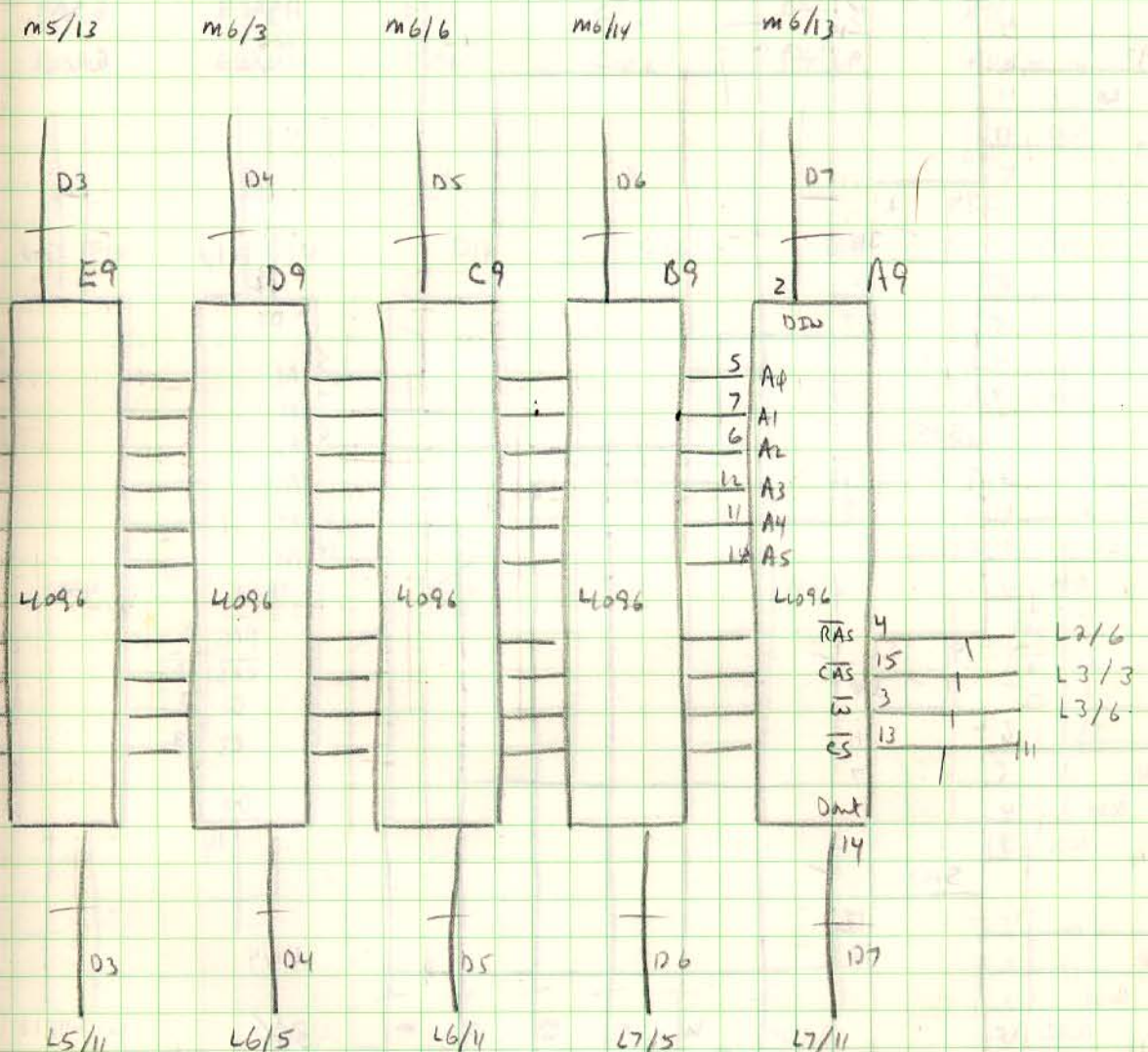


S1	S0	Select
0	0	32K-48K Rom
0	1	Char Rom #1
1	0	Char Rom #2
1	1	48K-64K Rom

4K Dynamic System Memory & Address Drivers



DATA INPUT



DATA OUTPUT

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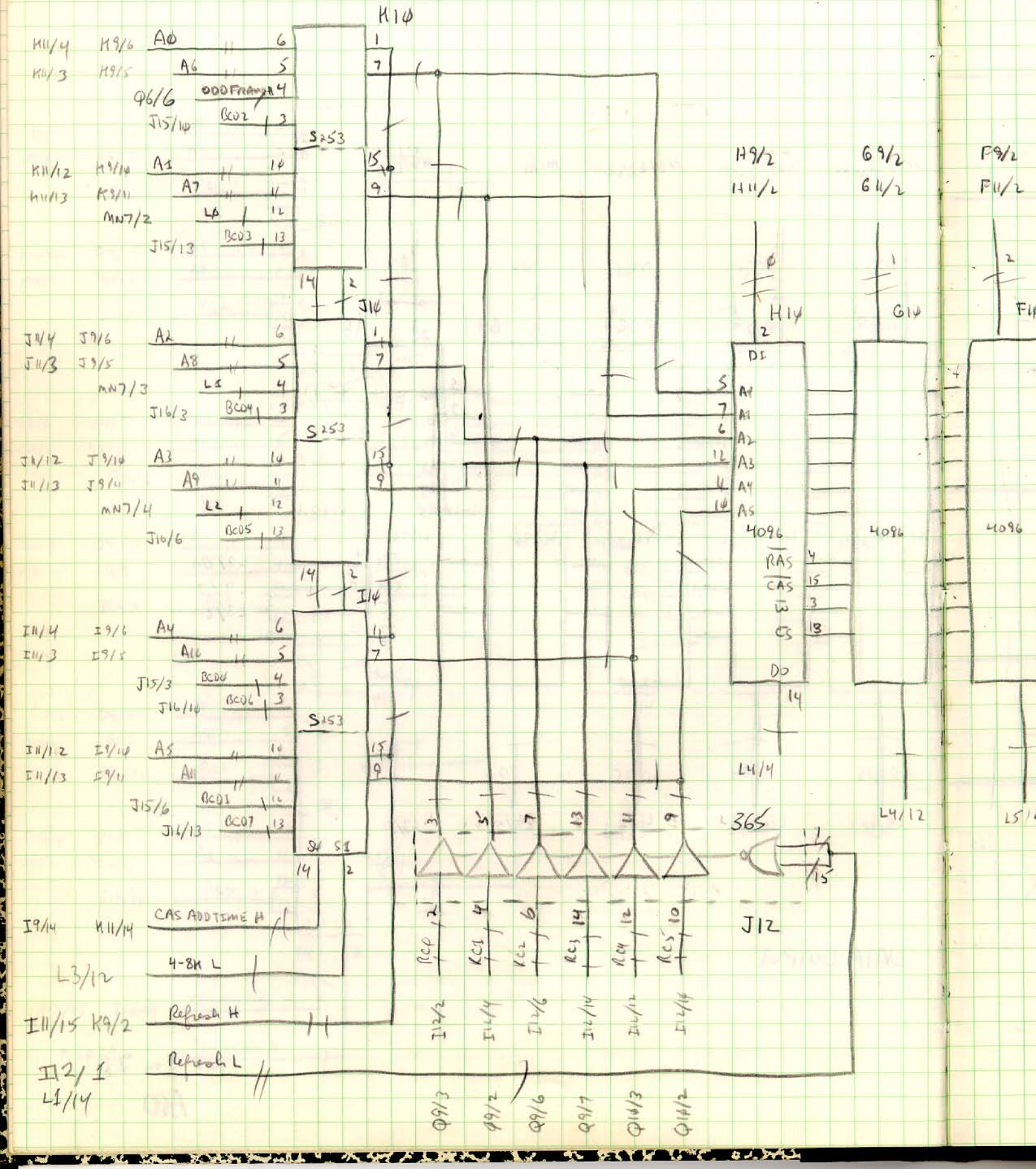
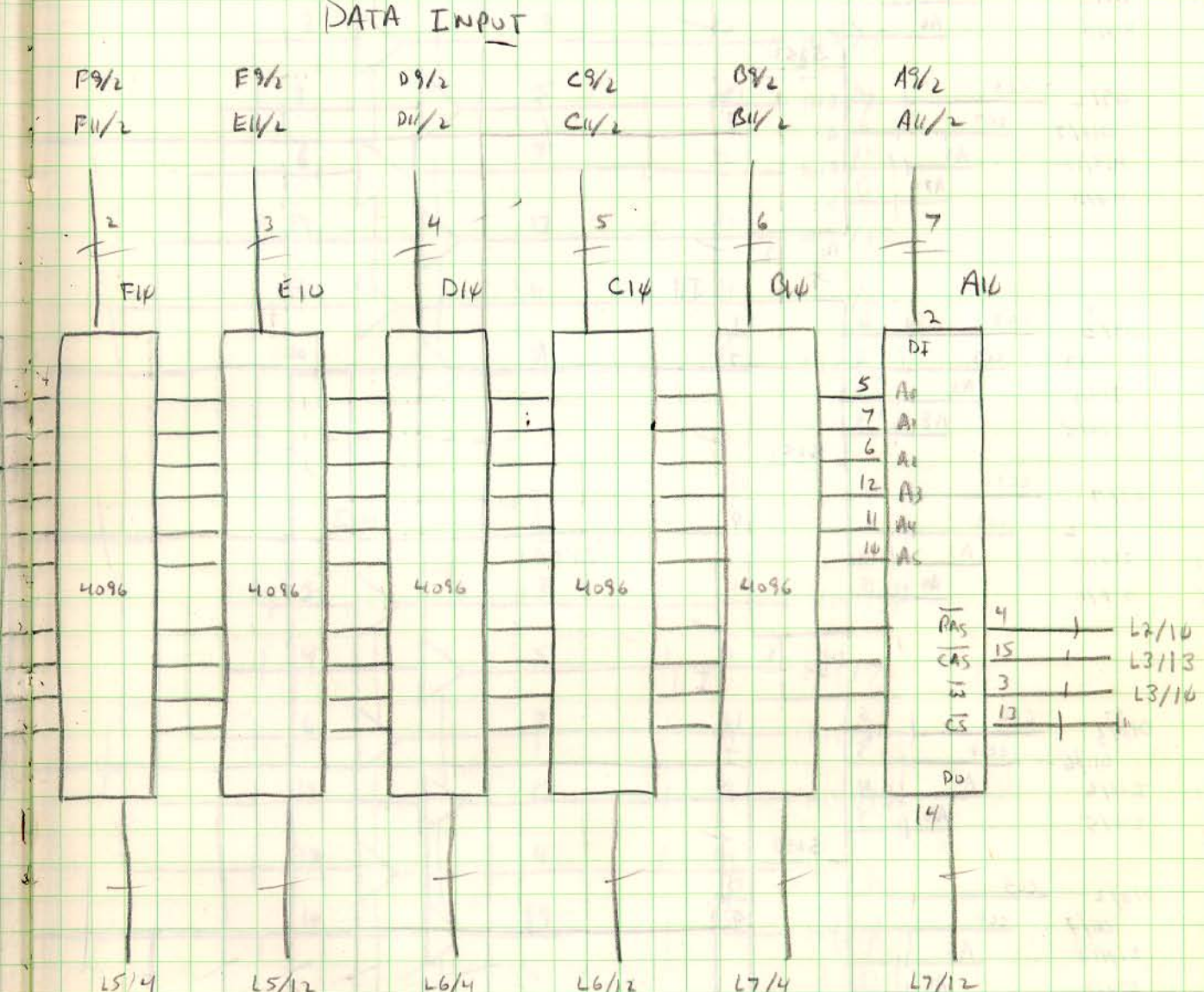
ADD

4K Dynamic Character Memory : Addressing Drives




DATA INPUT
F9/2
F11/2
E9/2
E11/2
D9/2
D11/2
C9/2
C11/2
B9/2
B11/2
A9/2
A11/2
2
3
4
5
6
7
F1Ø
E1Ø
D1Ø
C1Ø
B1Ø
A1Ø
4096
4096
4096
4096
4096
DI
DO
5
7
6
12
11
10
4
15
3
13
14
L7/10
L3/13
L3/10
L5/4
L5/12
L6/4
L6/12
L7/4
L7/12
DATA OUTPUT

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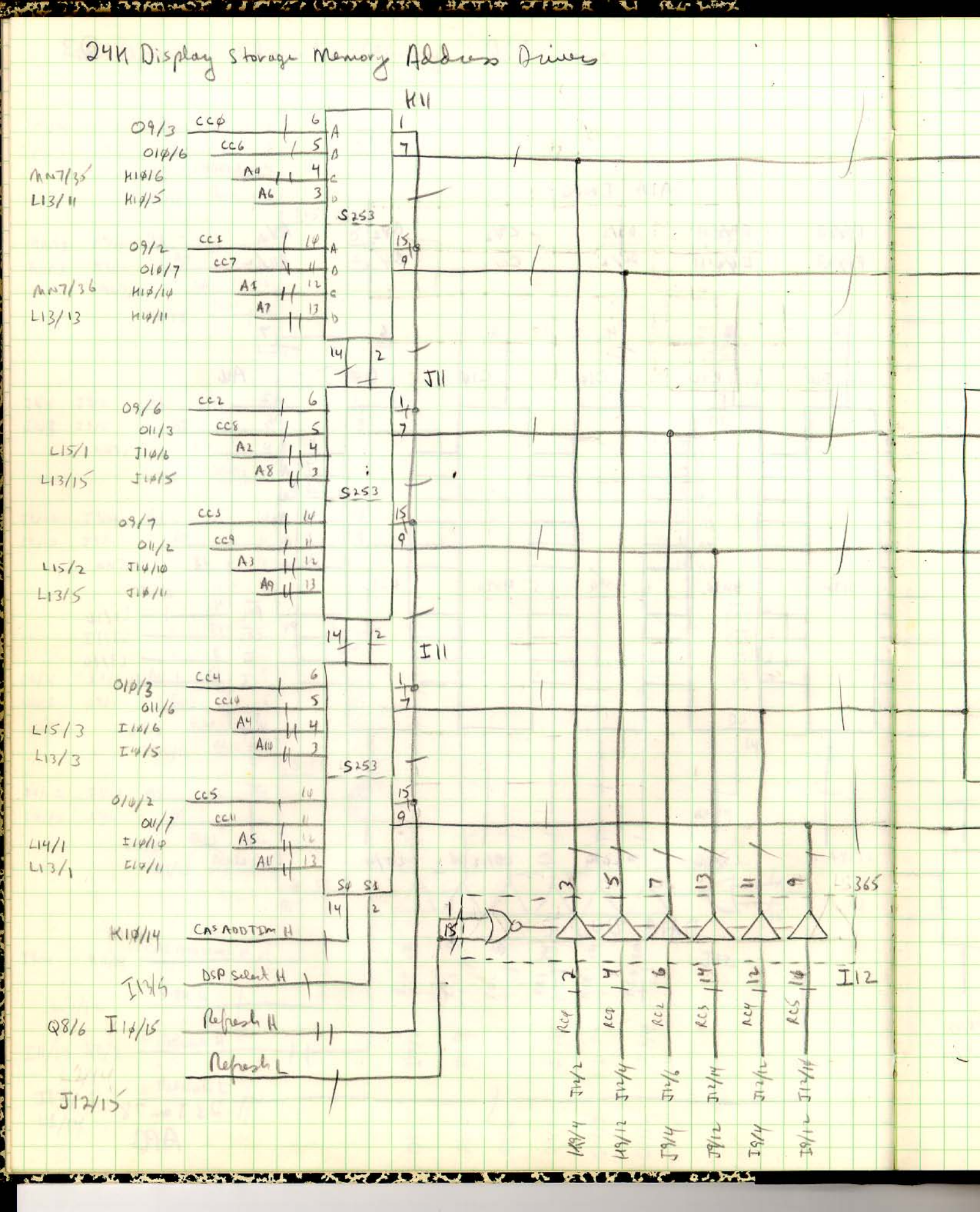
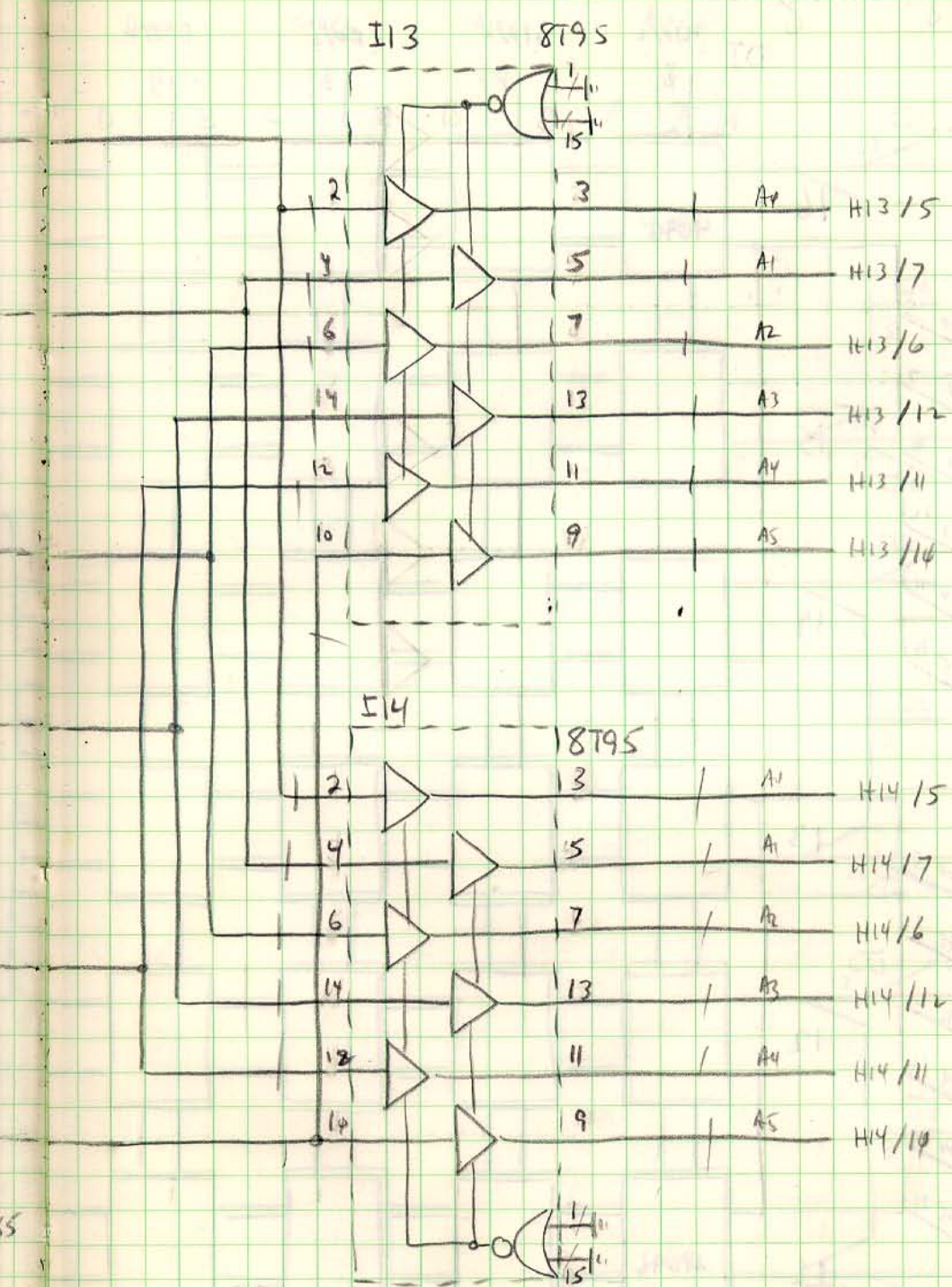
ARB

24K Display Storage Memory Address Drivers




I13
8T95
1
15
2
3
A1
H13/5
4
5
A1
H13/7
6
7
A2
H13/6
14
13
A3
H13/12
12
11
A4
H13/11
10
9
A5
H13/10
I14
8T95
2
3
A1
H14/5
4
5
A1
H14/7
6
7
A2
H14/6
14
13
A3
H14/12
12
11
A4
H14/11
10
9
A5
H14/10
1
15

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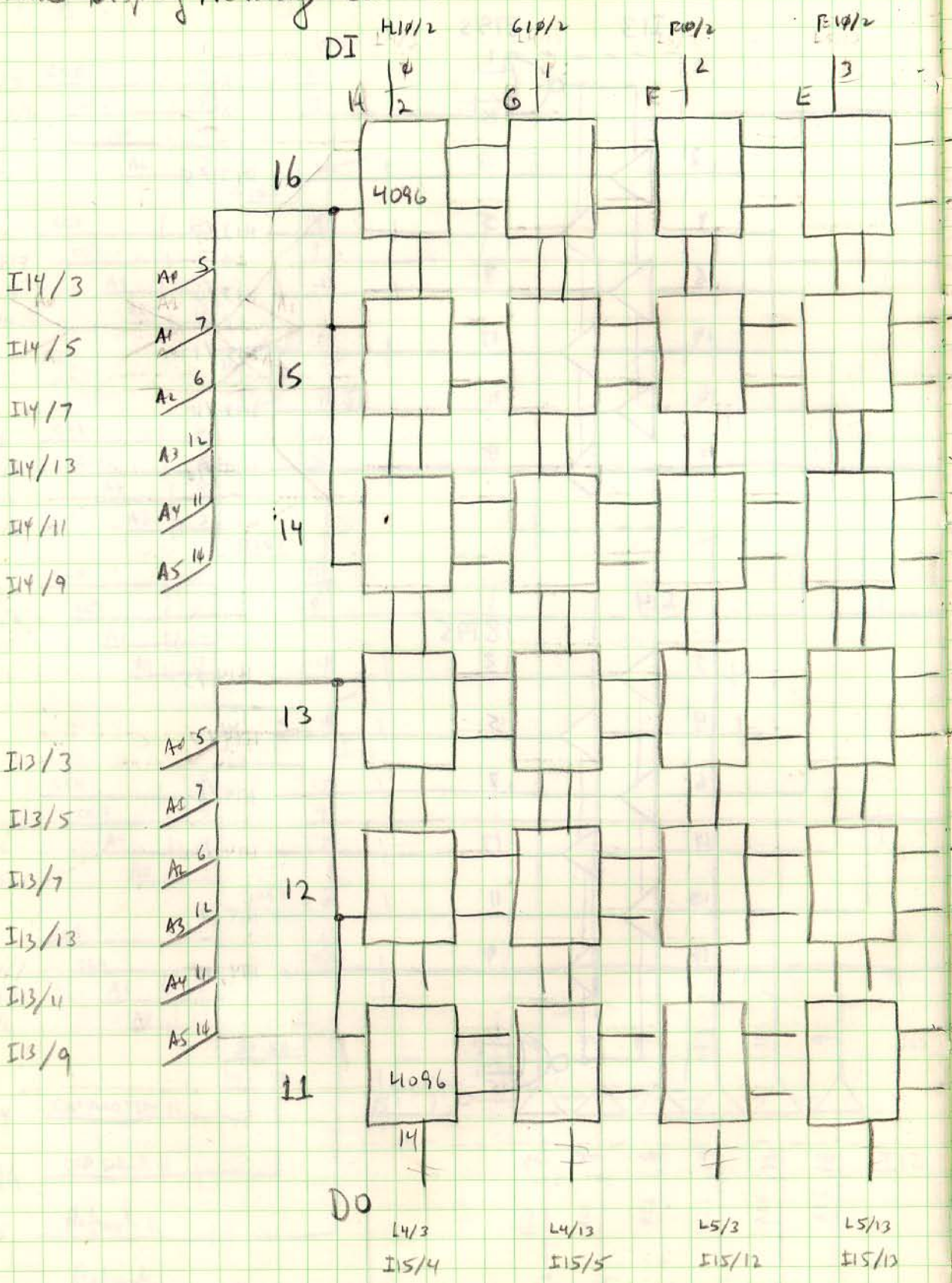
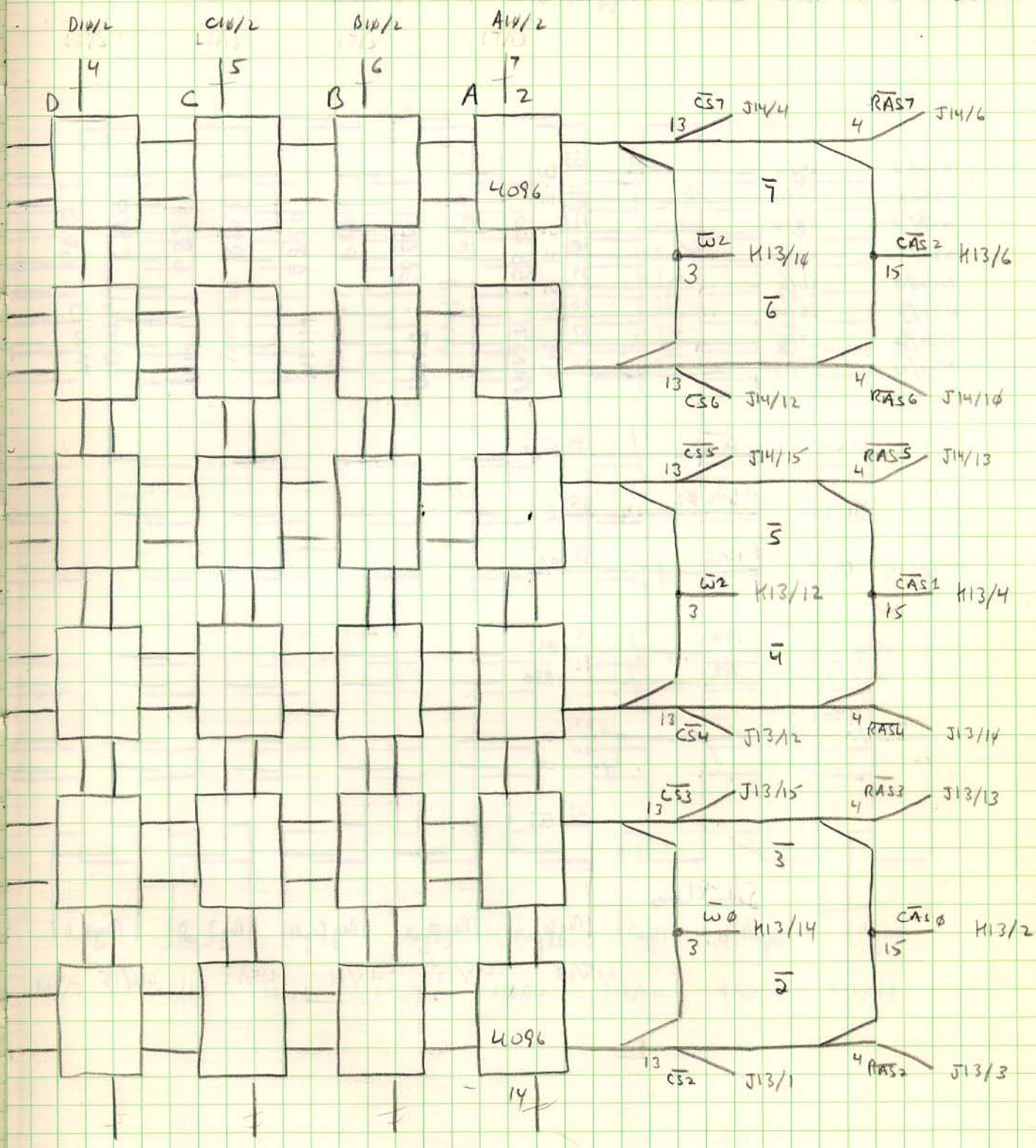
ARB

24K Dynamic Display Memory Connections




D10/2
C10/2
B10/2
A10/2
4
5
6
7
D
C
B
A
2
4096
4096
14
CS7 J14/4
13
RAS7 J14/6
4
7
W2 H13/14
3
CAS2 H13/6
15
6
13 CS6 J14/12
4 RAS6 J14/10
CS5 J14/15
13
RAS5 J14/13
4
5
W2 H13/12
3
CAS1 H13/4
15
4
13 CS4 J13/12
4 RAS4 J13/14
CS3 J13/15
13
RAS3 J13/13
4
3
W0 H13/14
3
CAS0 H13/2
15
2
13 CS2 J13/1
4 RAS2 J13/3
L6/3
I16/4
L6/13
I16/5
L7/3
I16/12
L7/13
I16/13

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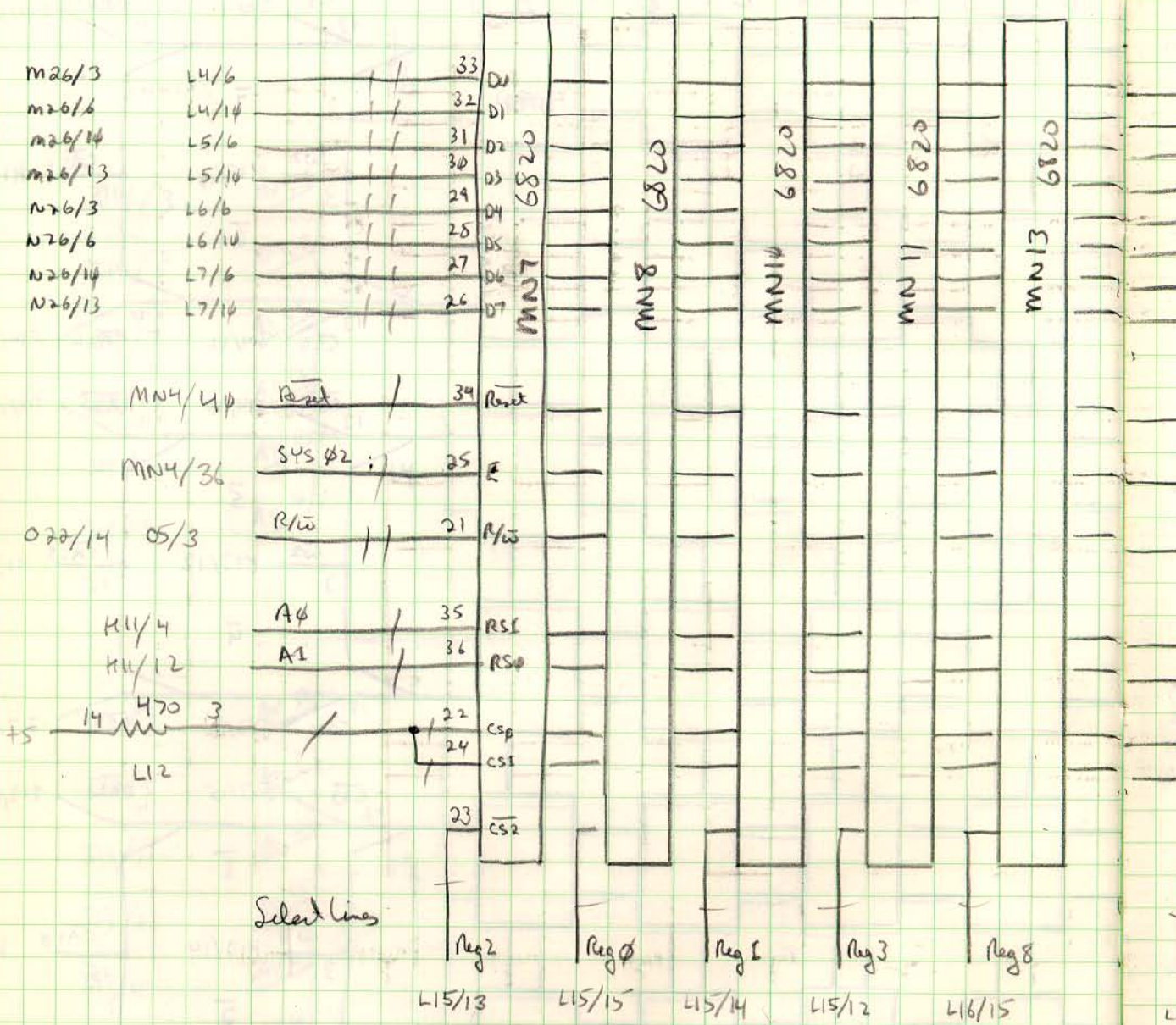
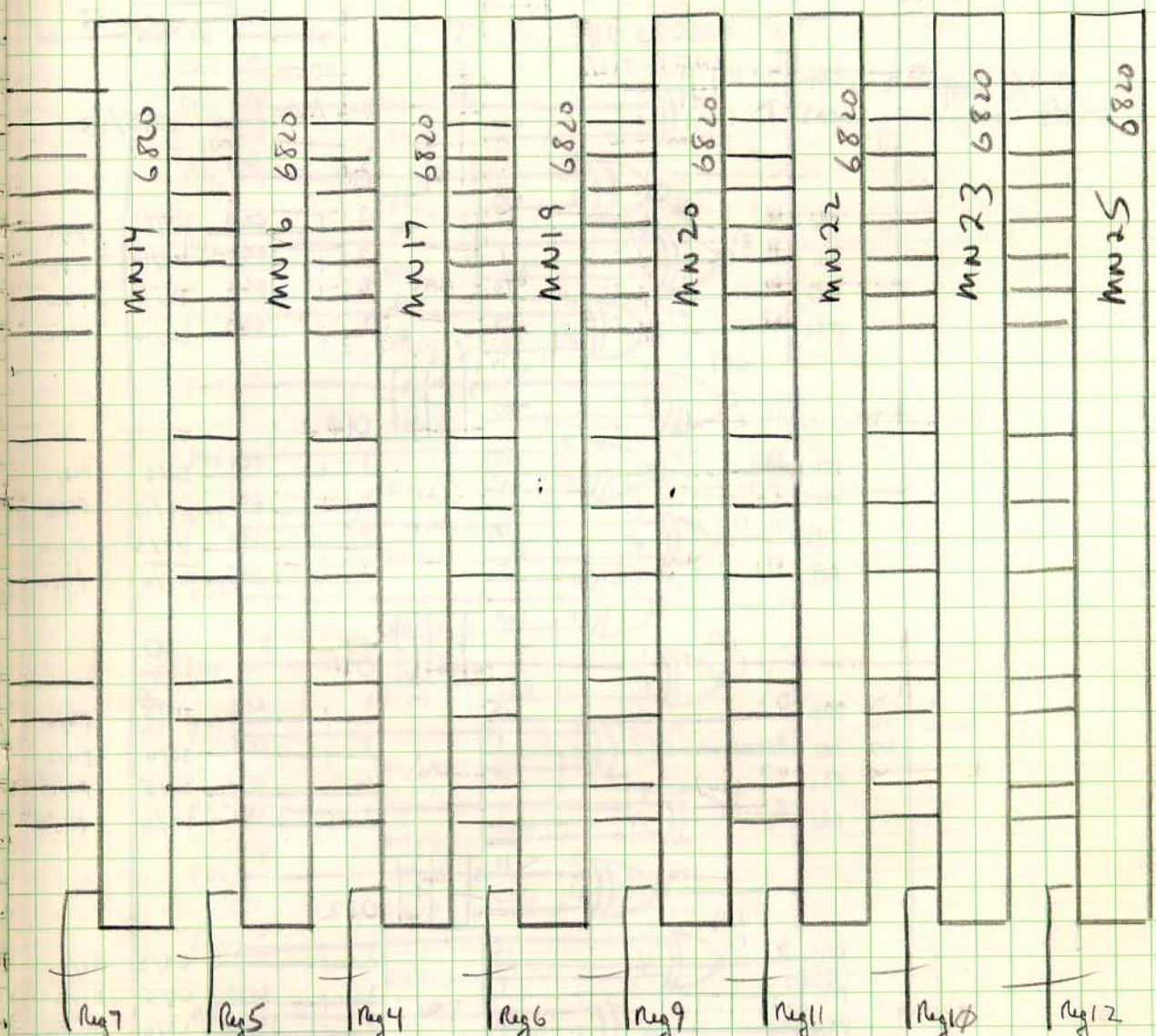
ADB

Data and Data Control signals to the PIA's




MN14 6820
MN16 6820
MN17 6820
MN19 6820
MN20 6820
MN22 6820
MN23 6820
MN25 6820
Reg7
Reg5
Reg4
Reg6
Reg9
Reg11
Reg10
Reg12
L15/7
L15/14
L15/11
L15/9
L16/14
L16/12
L16/13
L16/18

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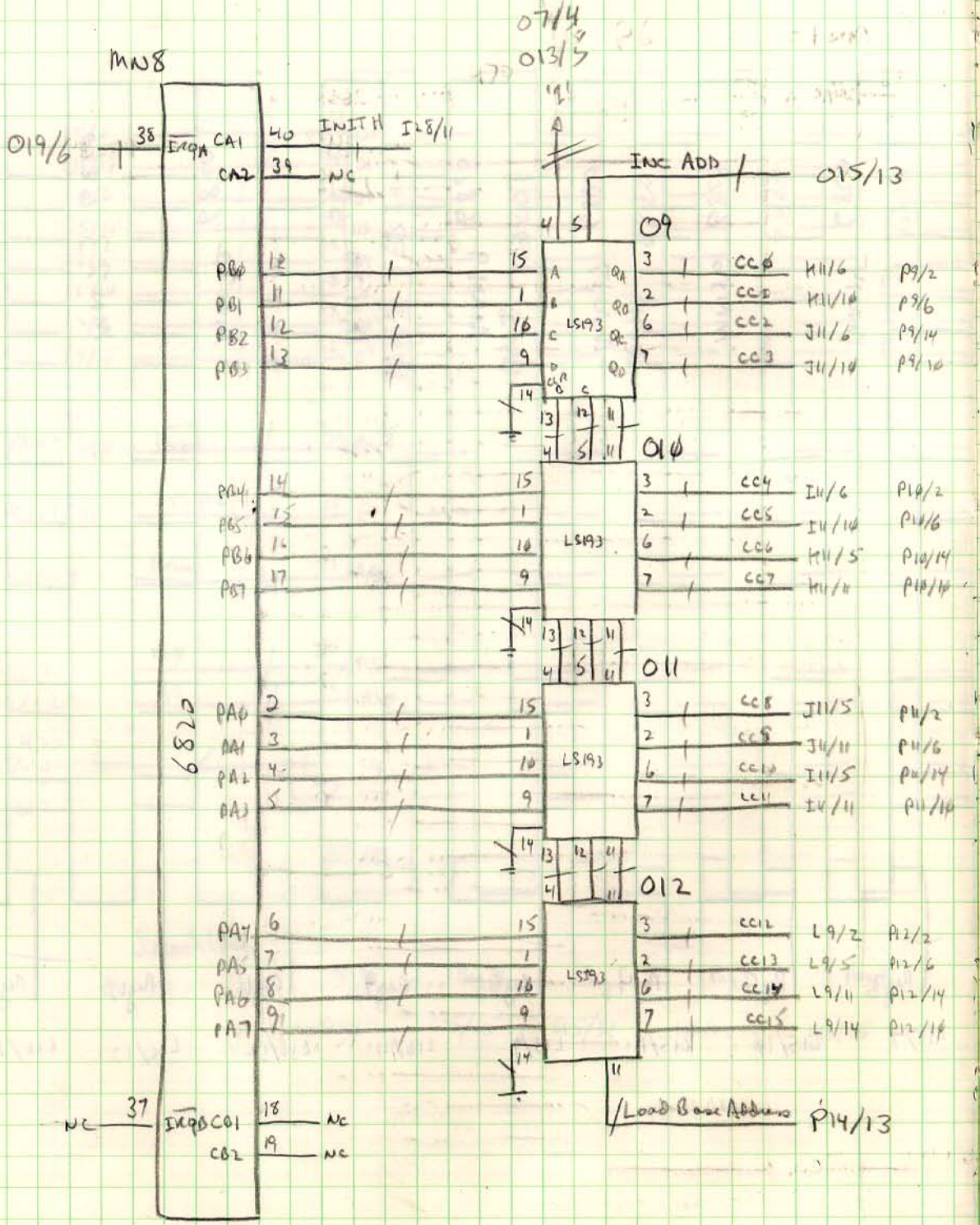
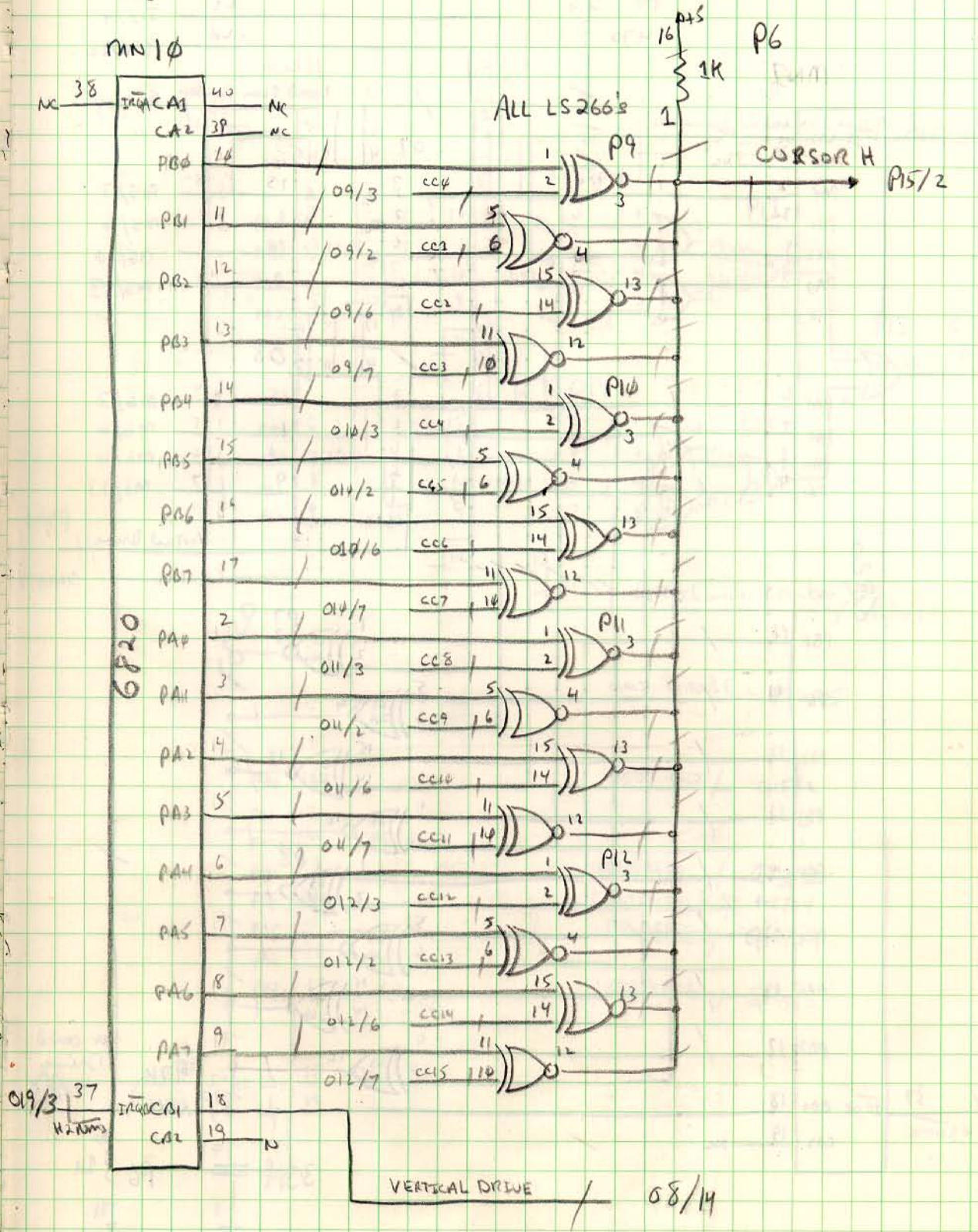
ARB

Reg Set Ø Display Base Address & Current Address Register



Reg Set 1 CURSOR ADDRESS & Address Comparator



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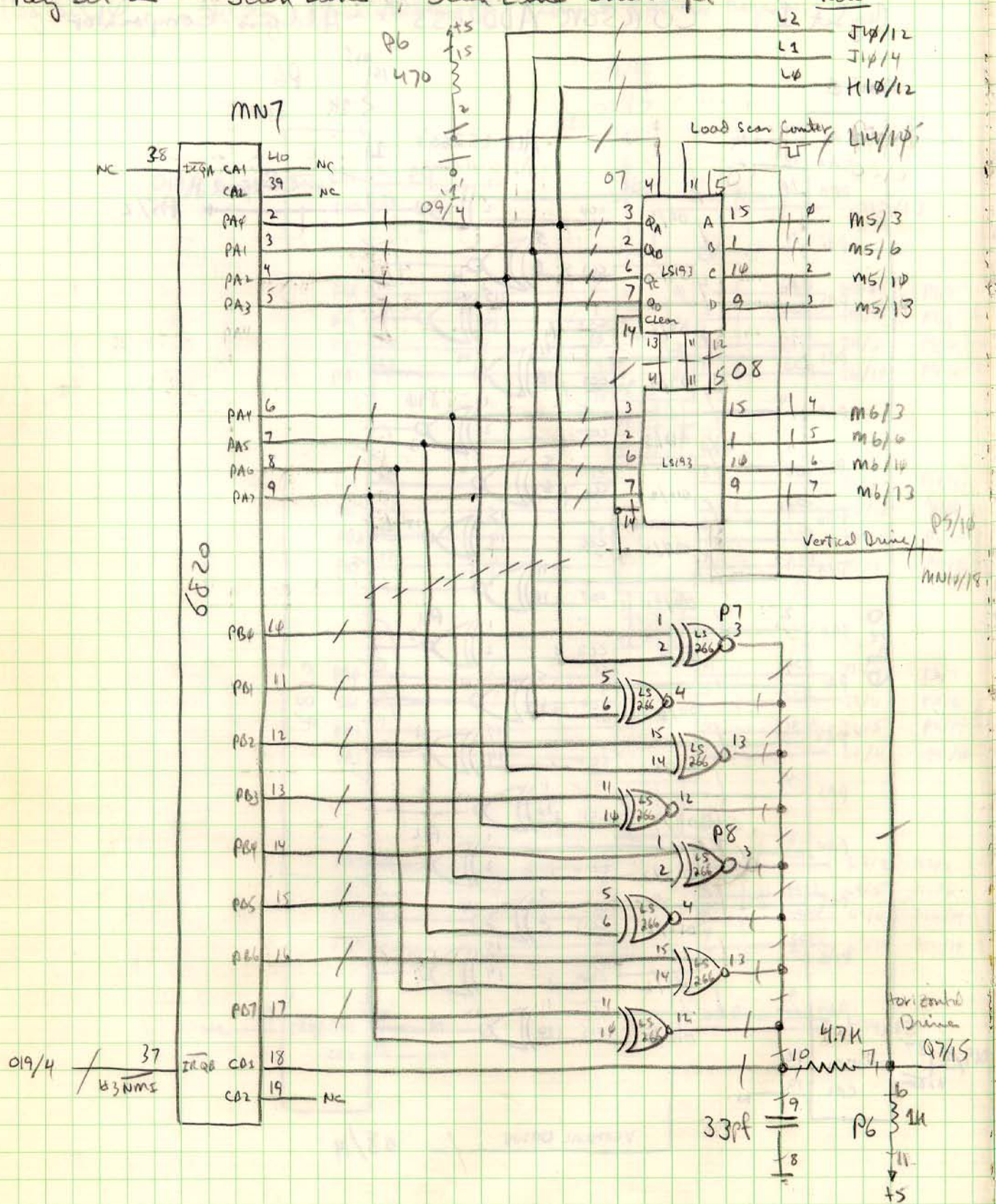
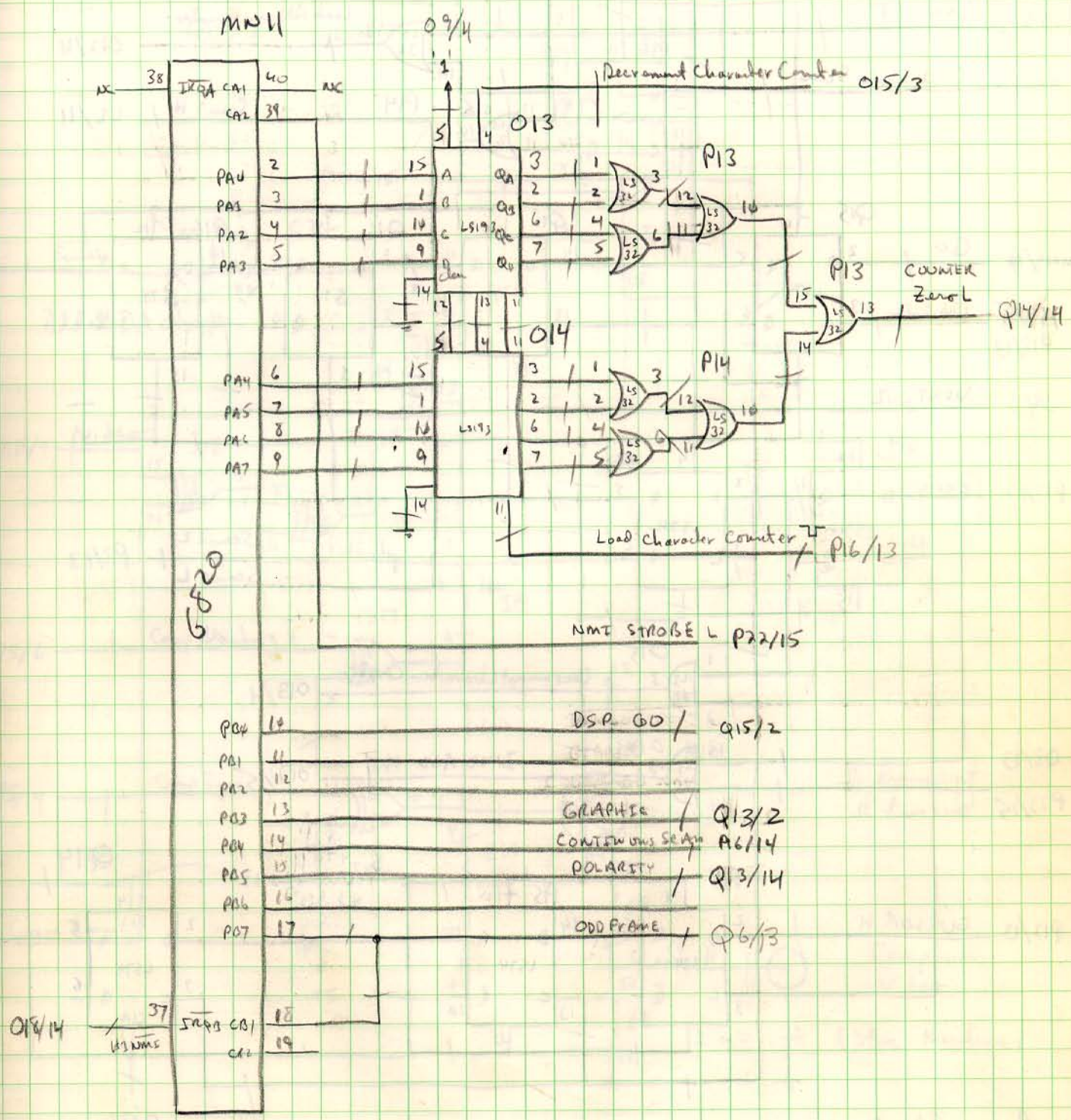
ARB

Reg Set 2 Scan Line & Scan Line Interrupt



Reg Set 3 Characters/line & Display Control



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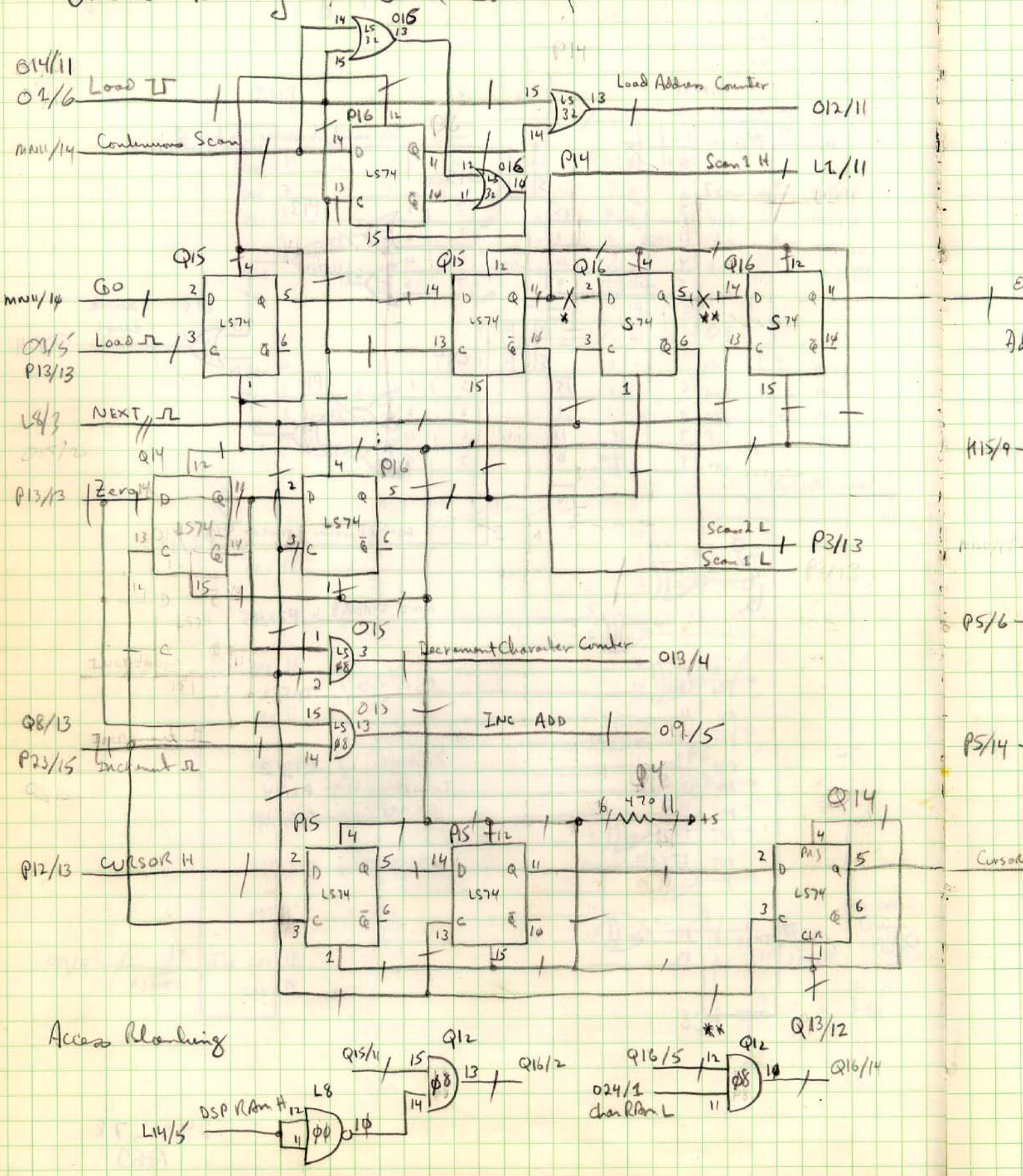
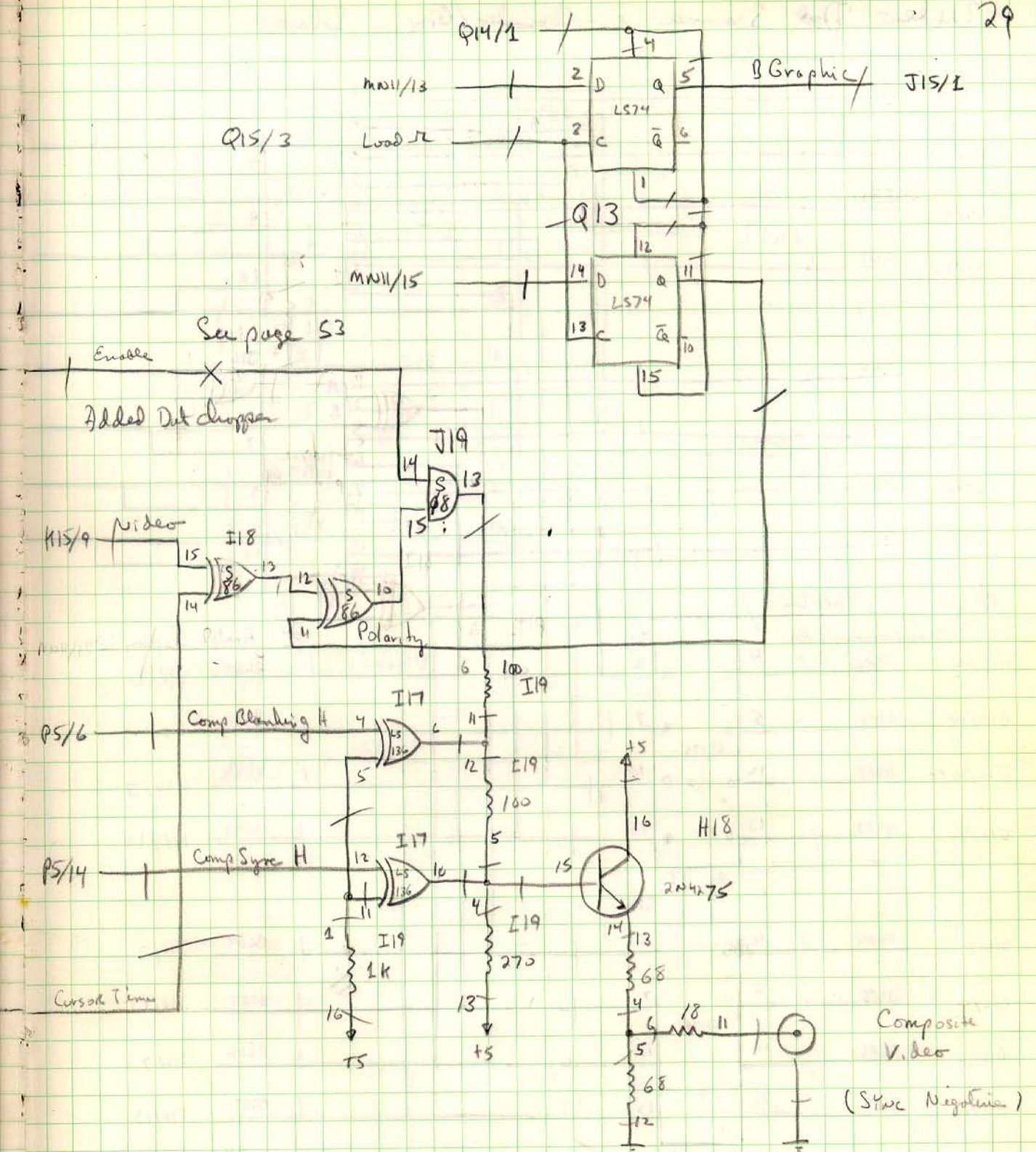
ARB

Video Timing & Scan Control




Q14/1
MN11/13
Q15/3
Load
B Graphic/
J15/1
LS74
Q13
MN11/15
See page 53
Enable
Added Dot dropper
J19
H15/9
Video
I18
Polarity
I19
I17
P5/6
Comp Blanking H
P5/14
Comp Sync H
100
270
1K
Cursor Timing
+5
H18
2N4275
68
18
Composite Video
(Sync Negative)

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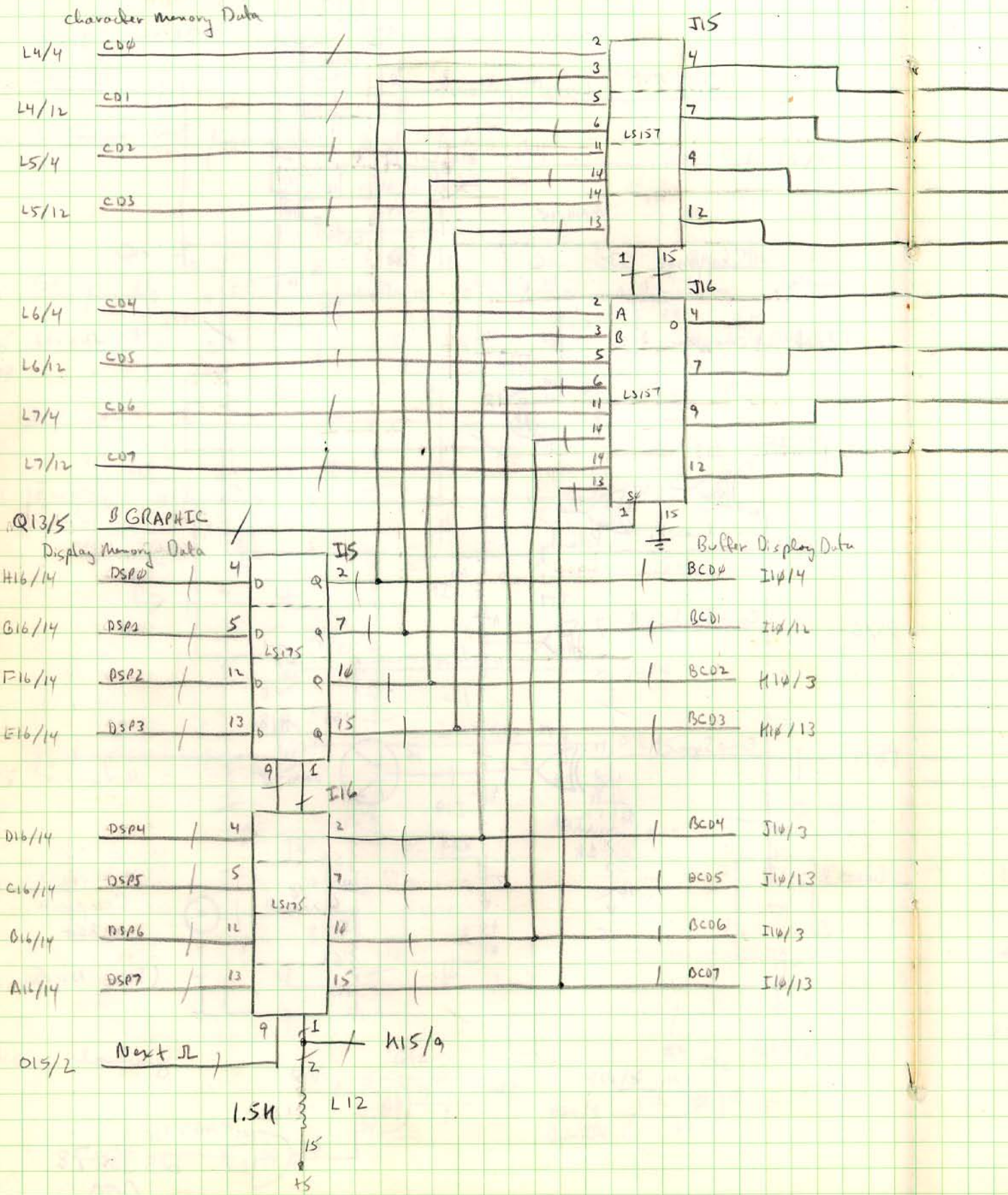
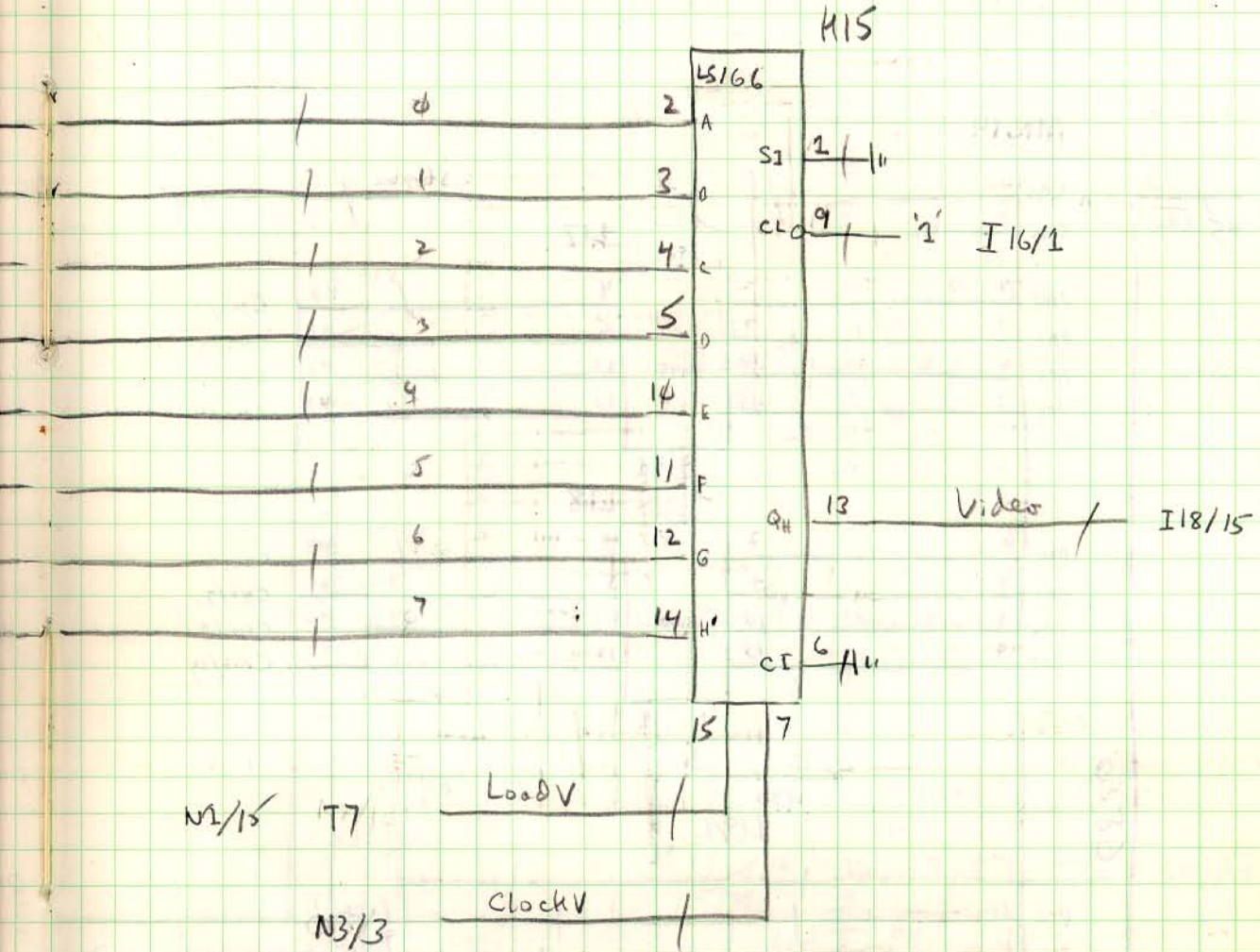
ASD

Video Dot Scanner & Character/Graphic Selector




H15
LS166
2
A
3
B
4
C
5
D
10
E
11
F
12
G
14
H'
S1
1
11
CLO
9
'1'
I16/1
QH
13
Video
I18/15
CI
6
A11
15
7
LoadV
N1/15 T7
ClockV
N3/3

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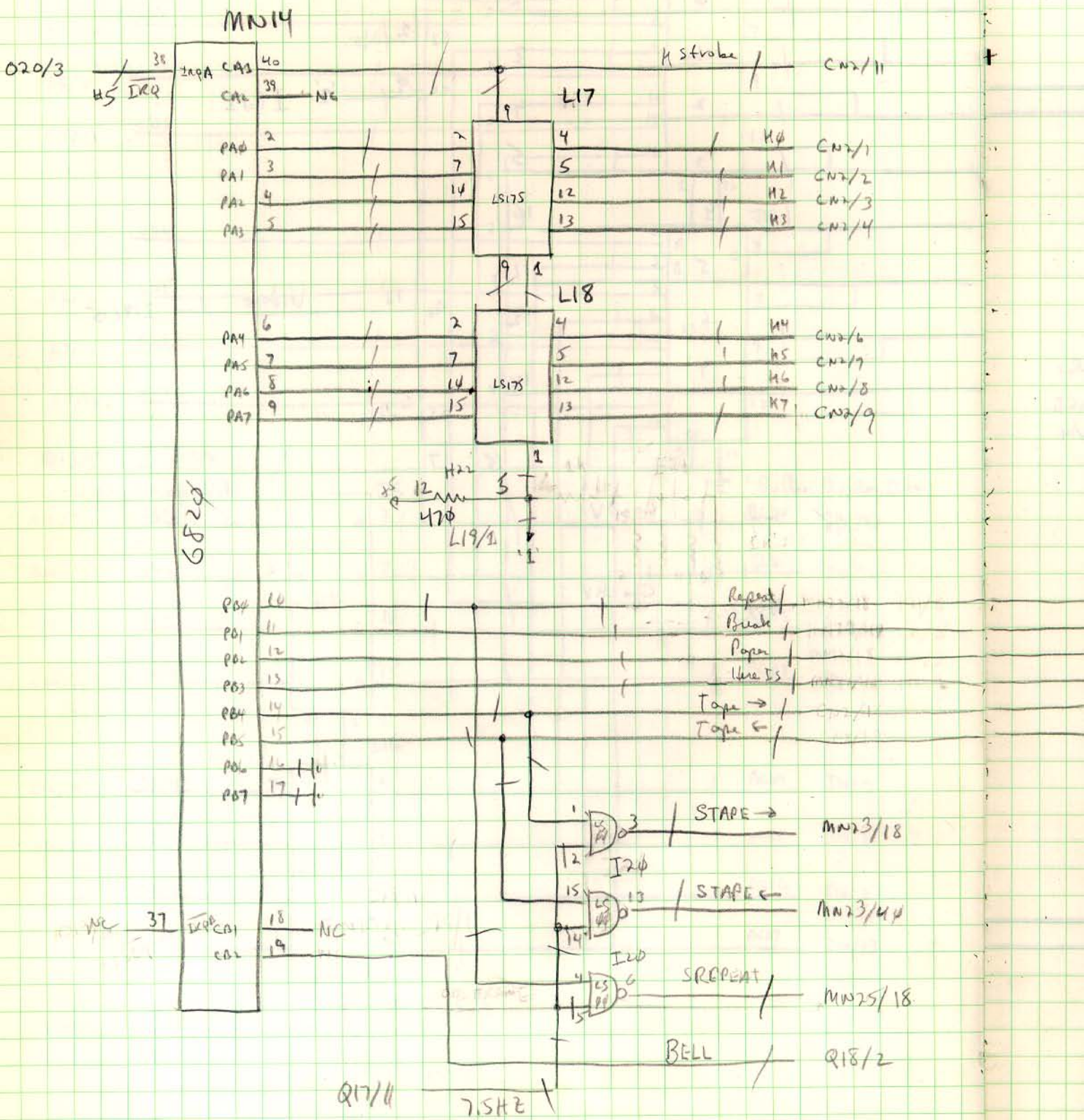
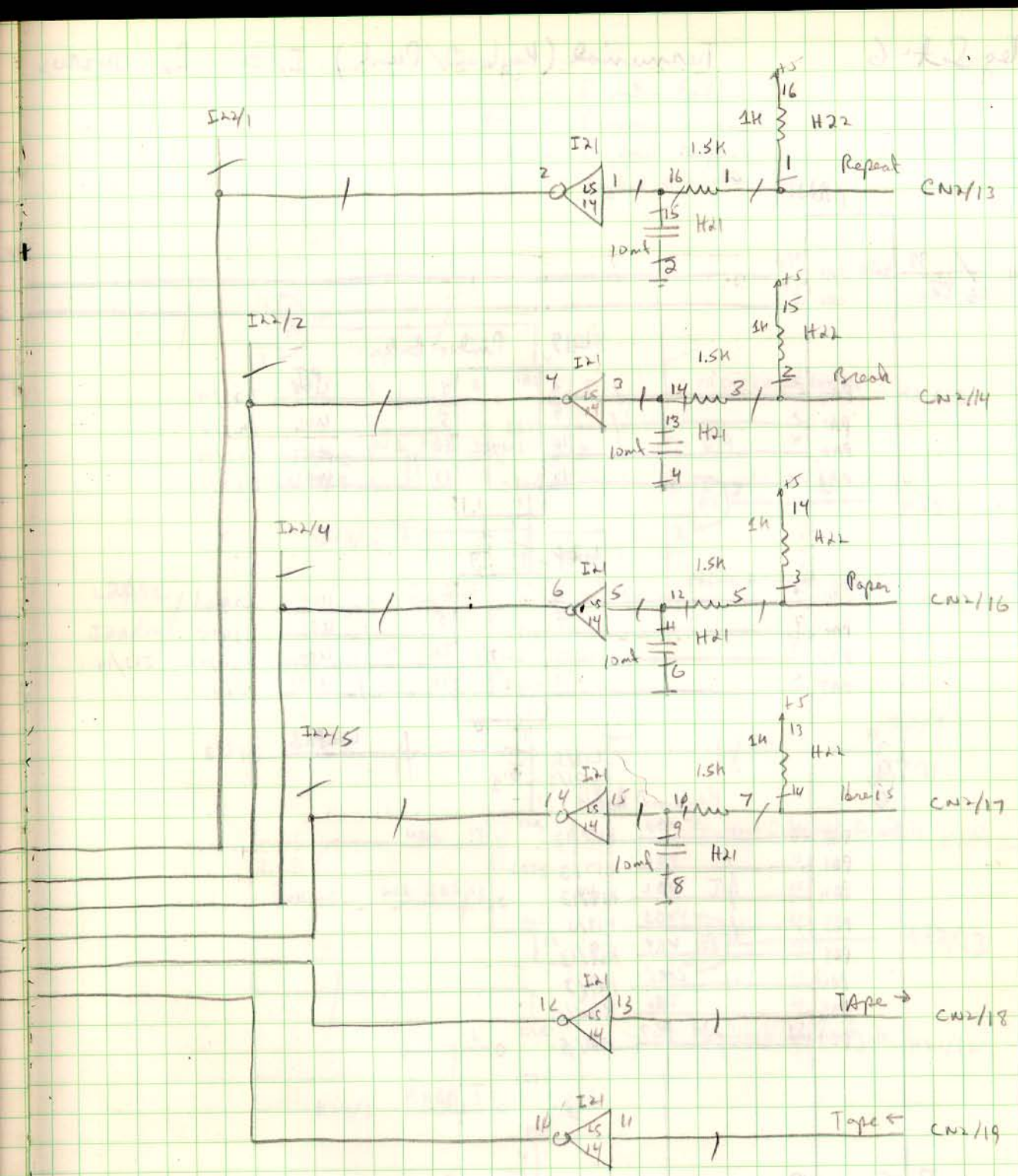
ARD

Reg Set 7 ASCII Keyboard Input




IA2/1
I21
1.5K
+5
16
1K
H22
Repeat
CN2/13
10mf
H21
IA2/2
Breath
CN2/14
IA2/4
Paper
CN2/16
IA2/5
Ribbons
CN2/17
TApe →
CN2/18
Tape ←
CN2/19

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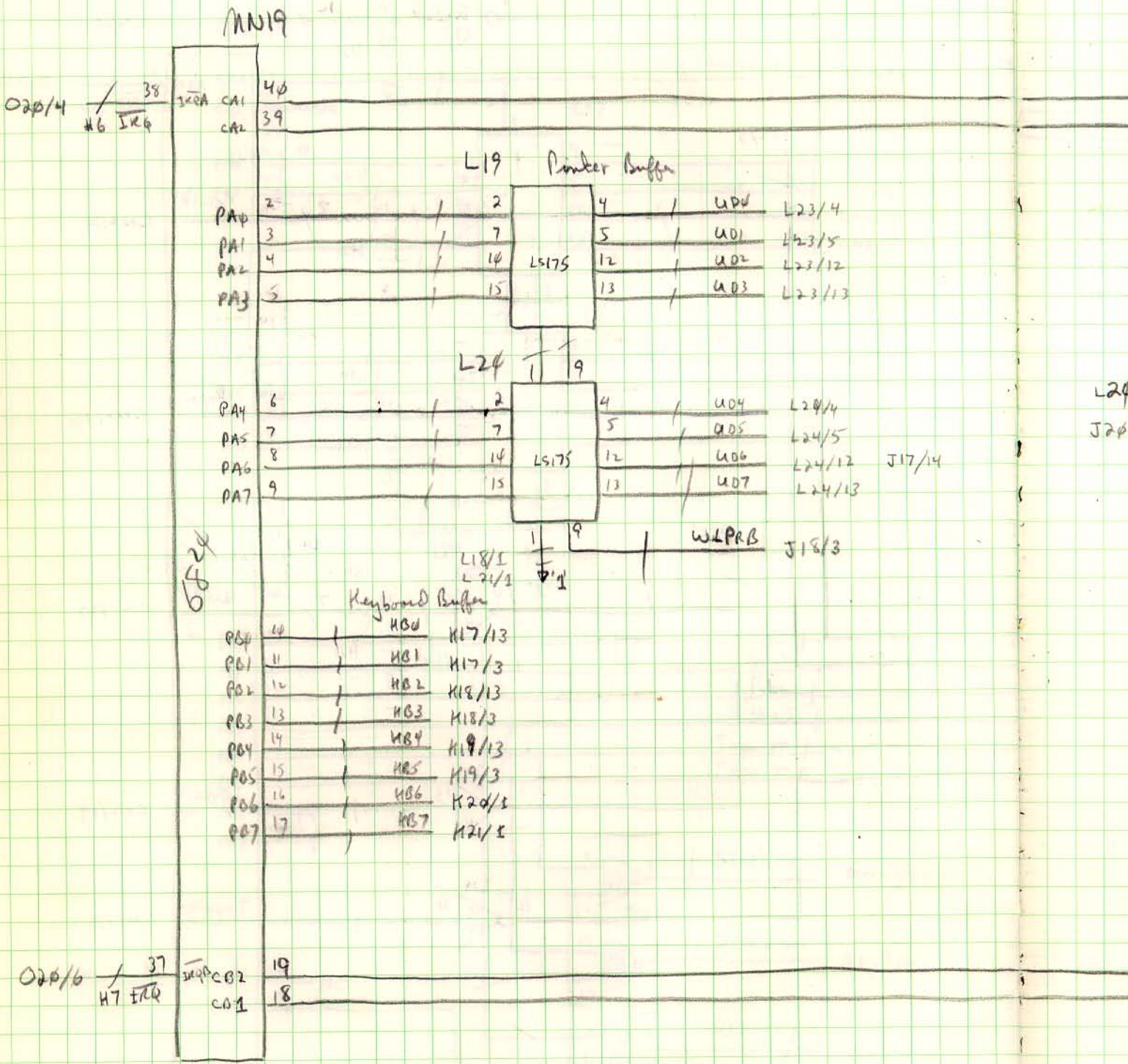
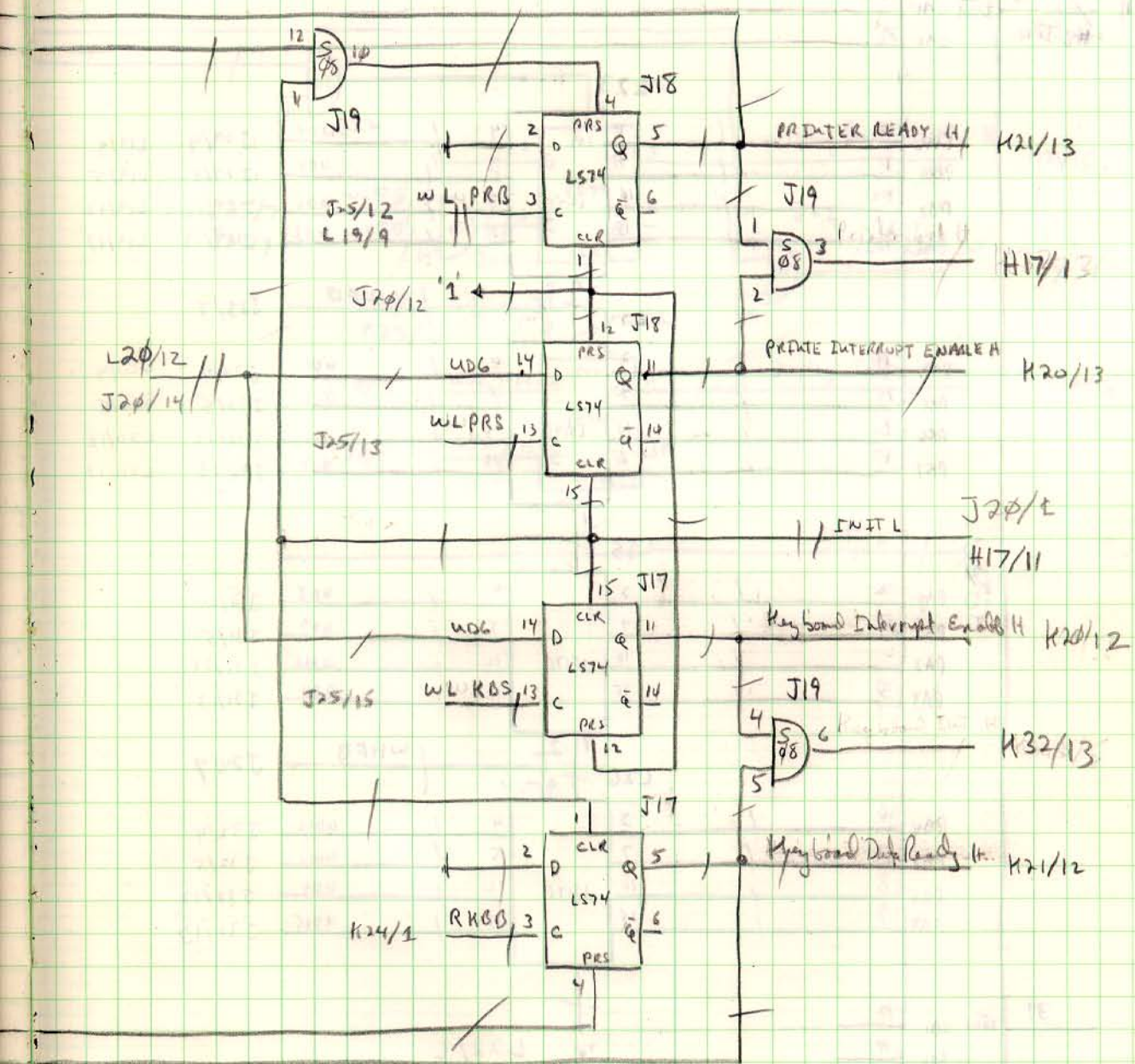
ARD

Reg Set 6 Terminal (Keyboard/Crt) I/O for UNIBUS



PRB - Printer Buffer
PRS - Printer Status
KBB - Keyboard Buffer
KBS - Keyboard Status



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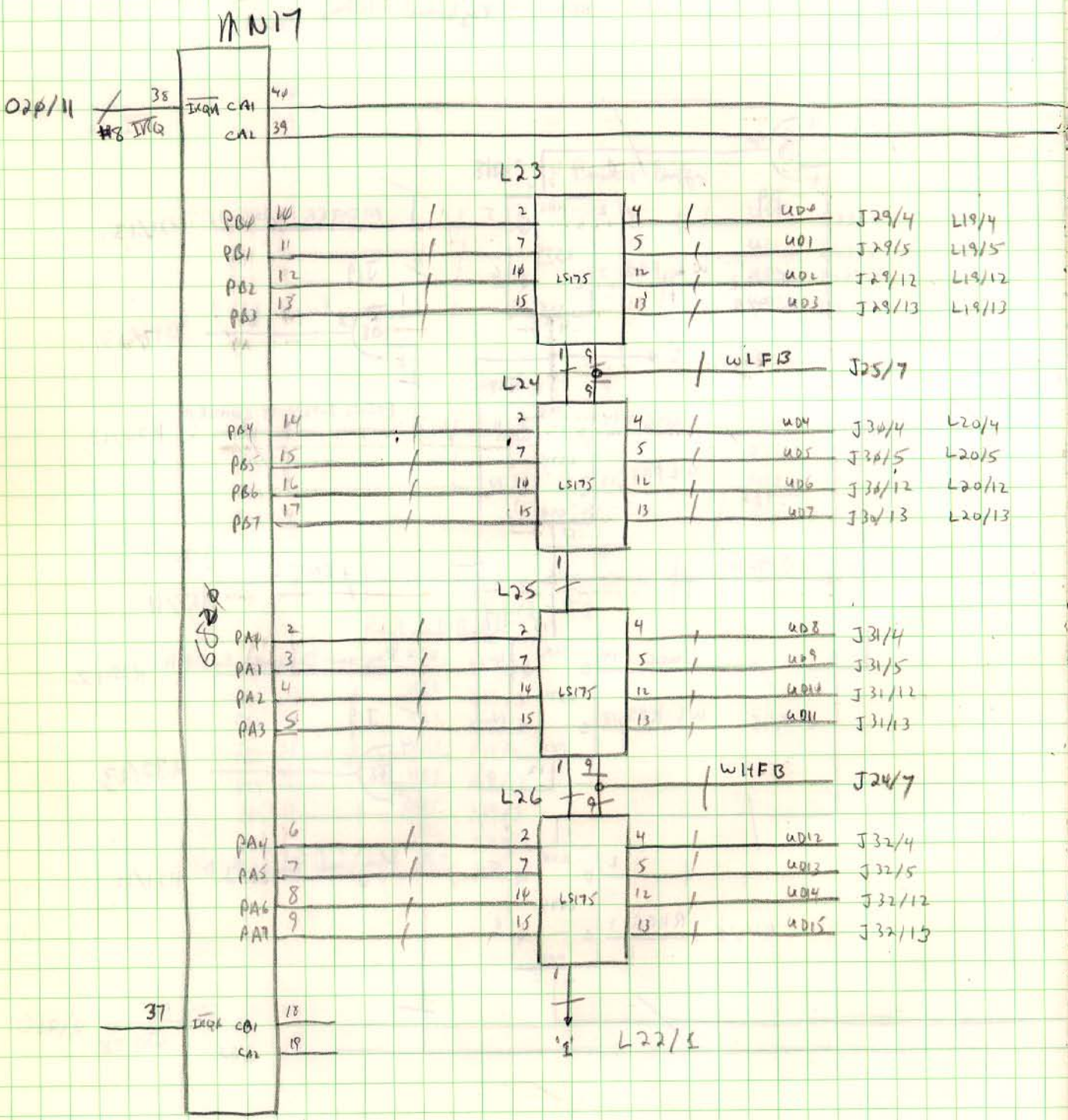
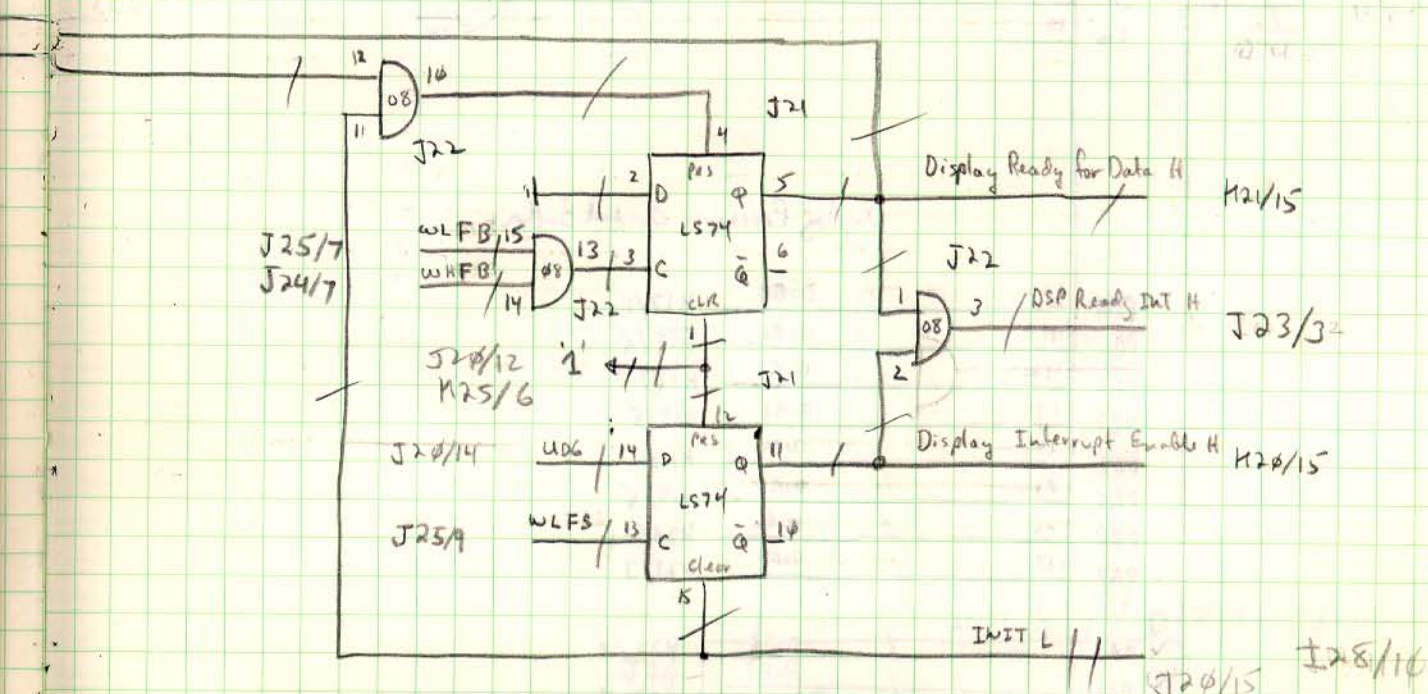
ARD

Reg Set 4 — Display Processor Input Data from UNIBUS



DIB - Display Input Buffer
DIBS - Display Input Status register
DOB - Display Output Buffer
DOBS - Display Output Status



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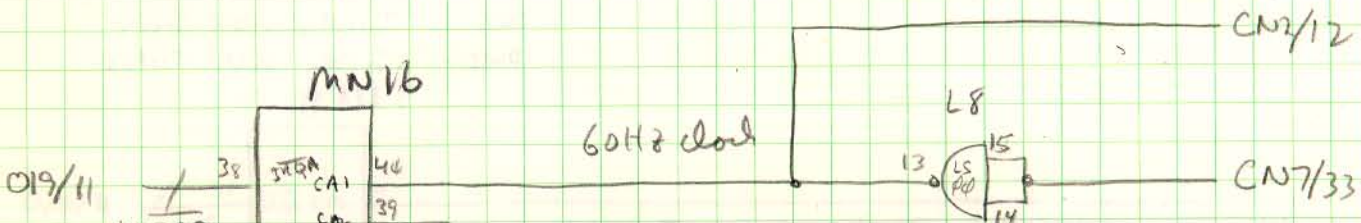
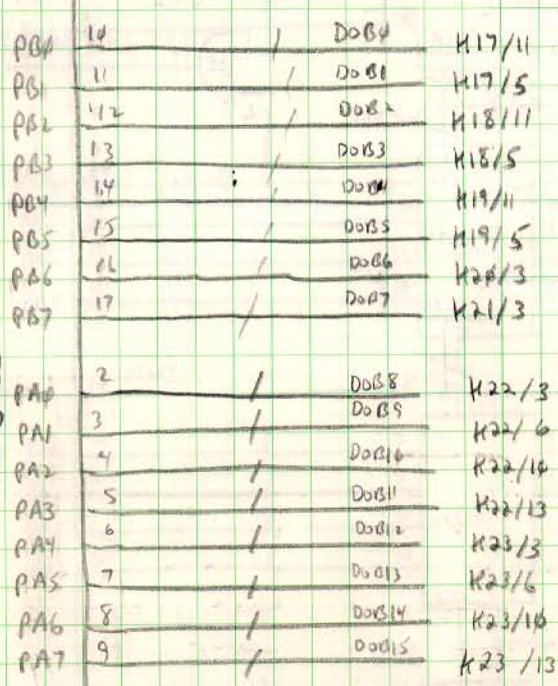
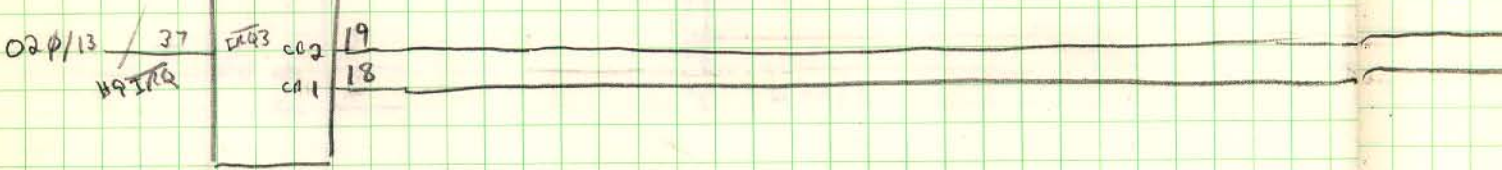
ARD

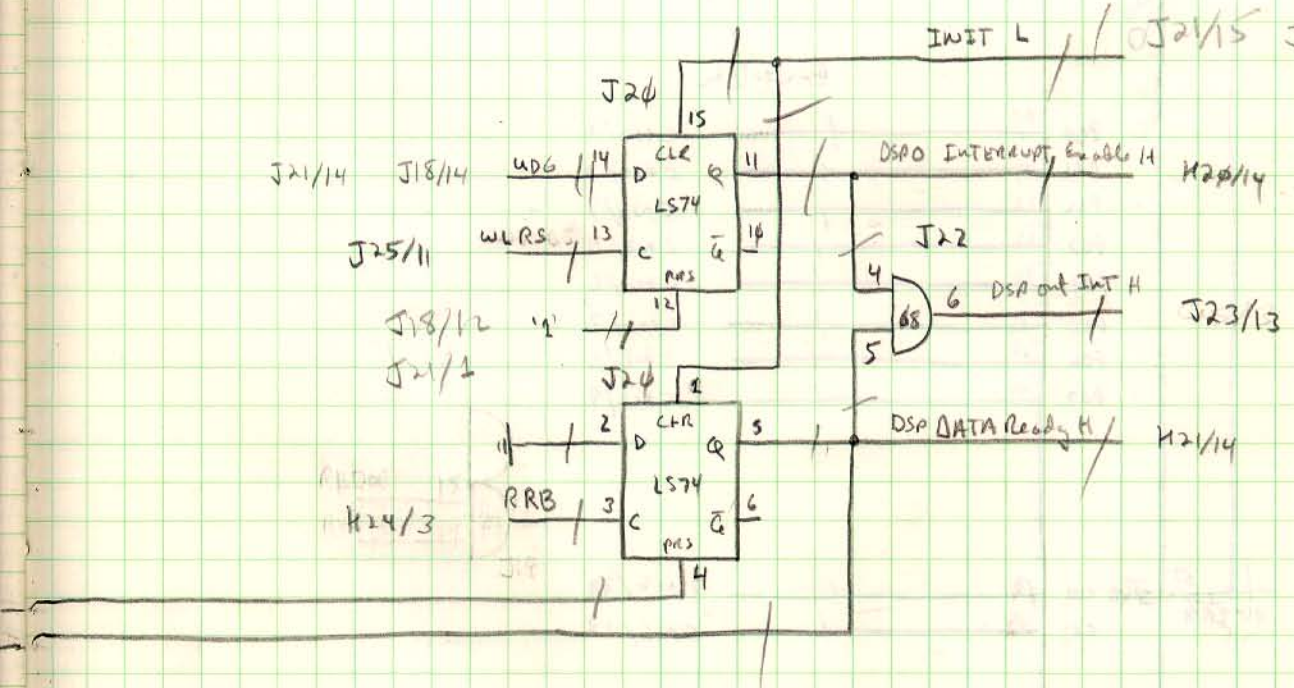
Reg Set 5 — Display Processor Output Data to UNIBUS



Display Processor Output Buffer






INIT L
J21/15
J19/11
J2ϕ
15
J21/14
J18/14
UDG
14
D
CLR
Q
11
LS74
DSPO INTERRUPT Enable H
H2ϕ/14
J25/11
WLRS
13
C
PRS
10
J22
12
4
J18/12
J21/1
'1'
6
DSP out INT H
J23/13
5
J2ϕ
1
2
CLR
3
H24/3
RRB
6
4
DSP DATA Ready H
H21/14

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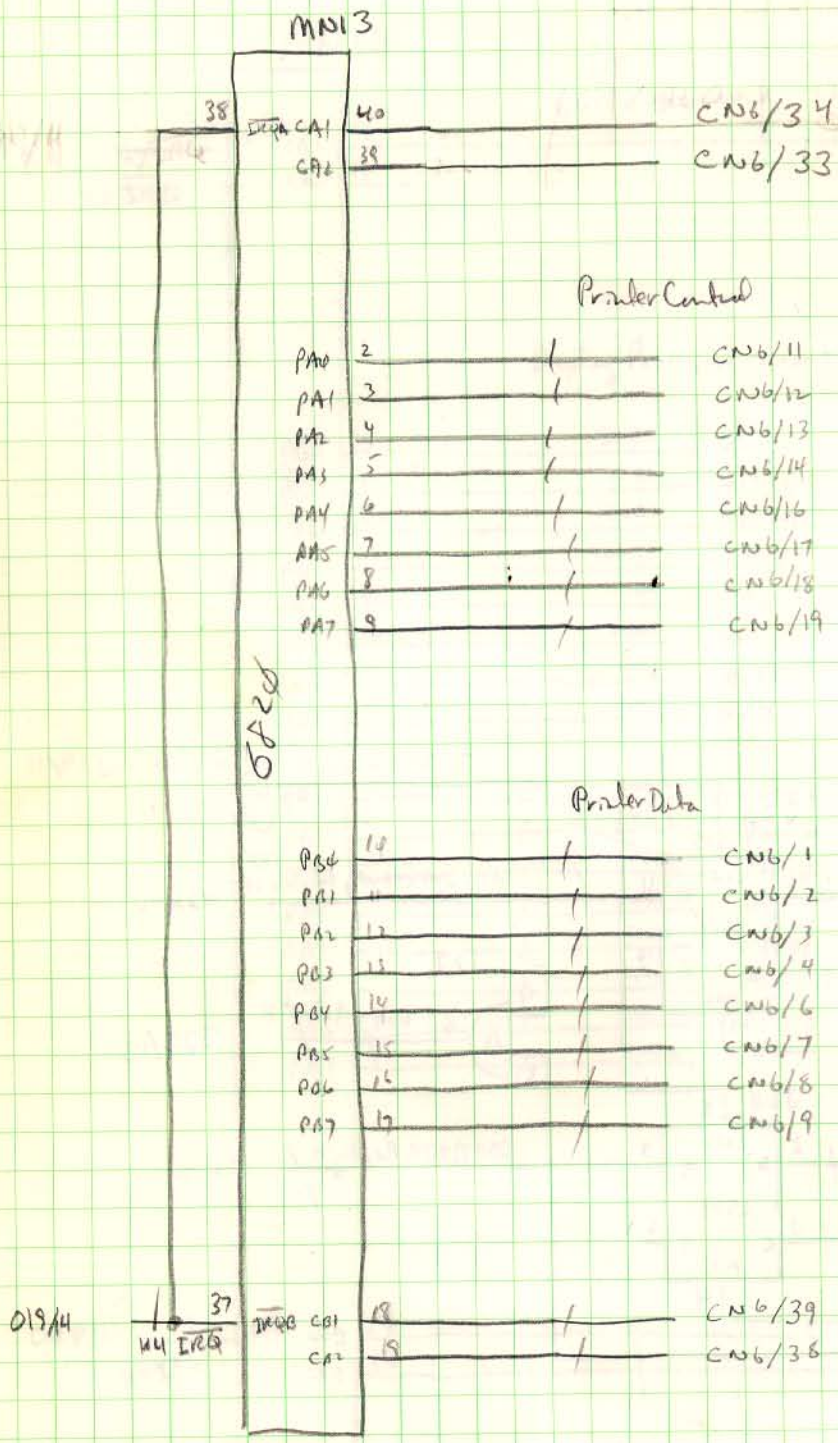
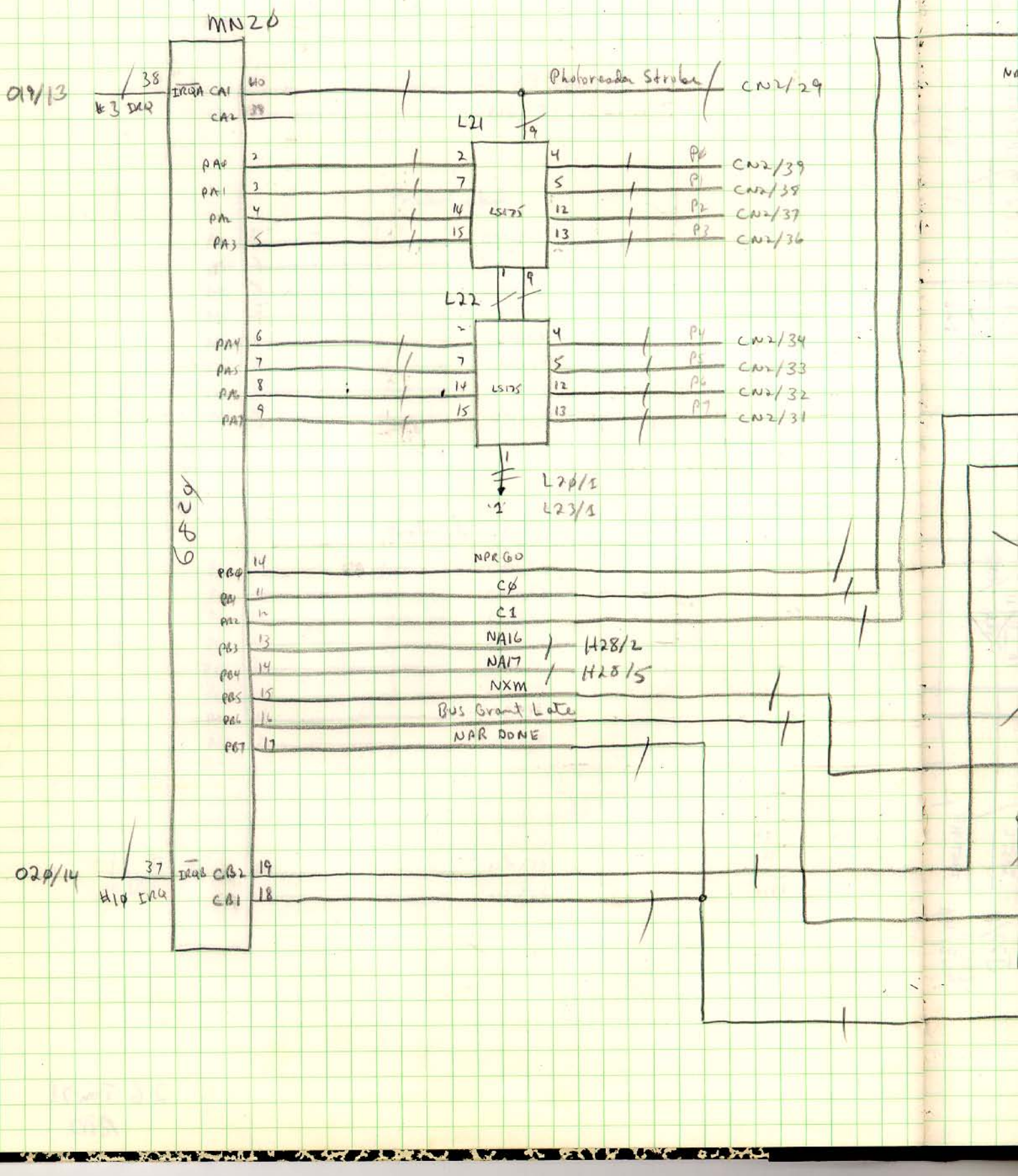
ARB

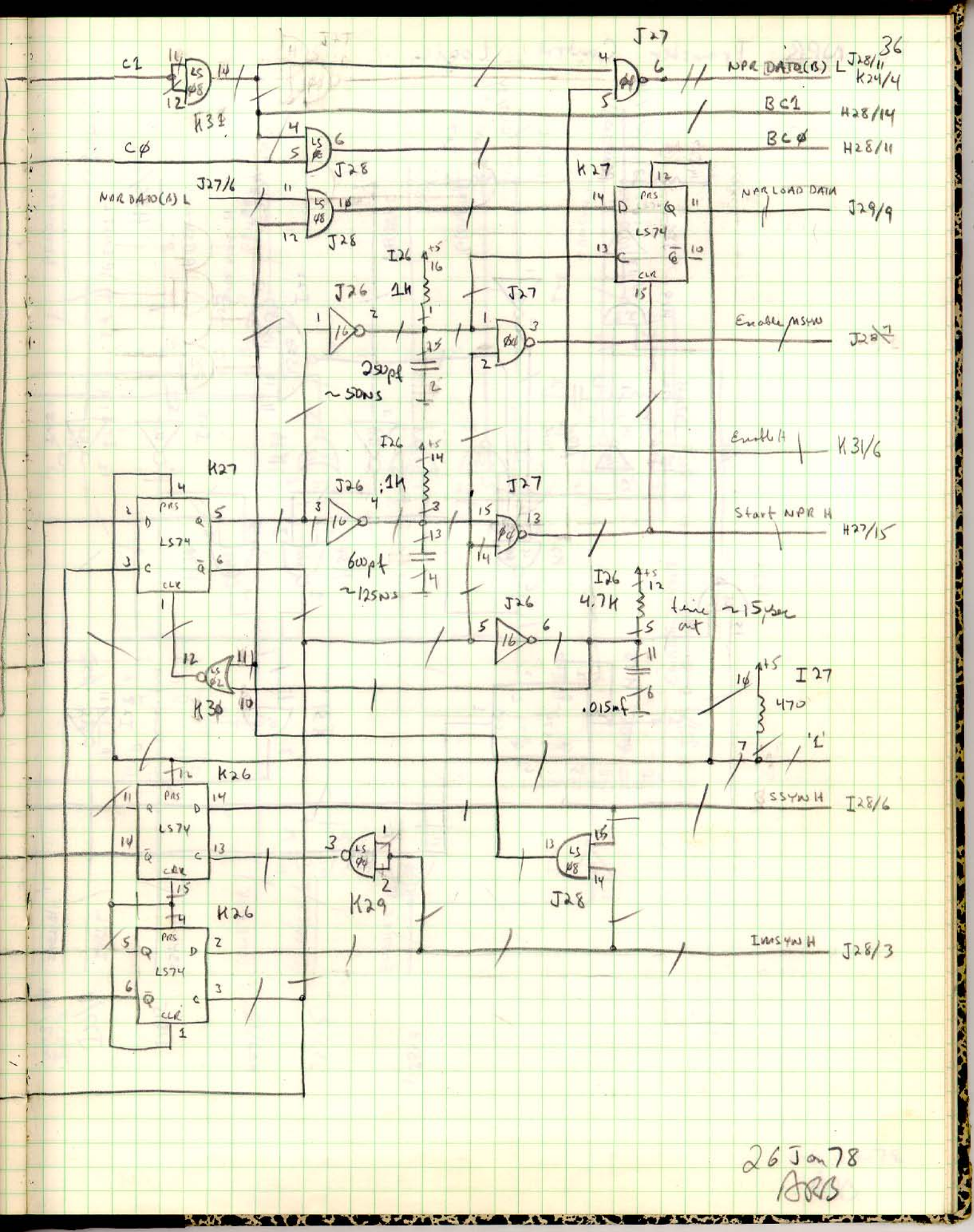
Reg Set 8

Printer Control



Reg Set 9 Photoreader & NPR Control




C1
Cφ
H31
J28
J27/6
NAR DATA(A) L
J27
NPR DATA(B) L
J28/11
K24/4
BC1
H28/14
BCφ
H28/11
K27
NAR LOAD DATA
J29/9
LS74
PRS
CLR
I26
+5
1K
J26
J27
Enable MSYN
J28/7
250pf
~50NS
Enable H
K31/6
Start NPR H
H27/15
600pf
~125NS
4.7K
time out ~15μsec
.015mf
I27
470
'1'
K30
K26
SSYN H
I28/6
K29
J28
INMSYN H
J28/3
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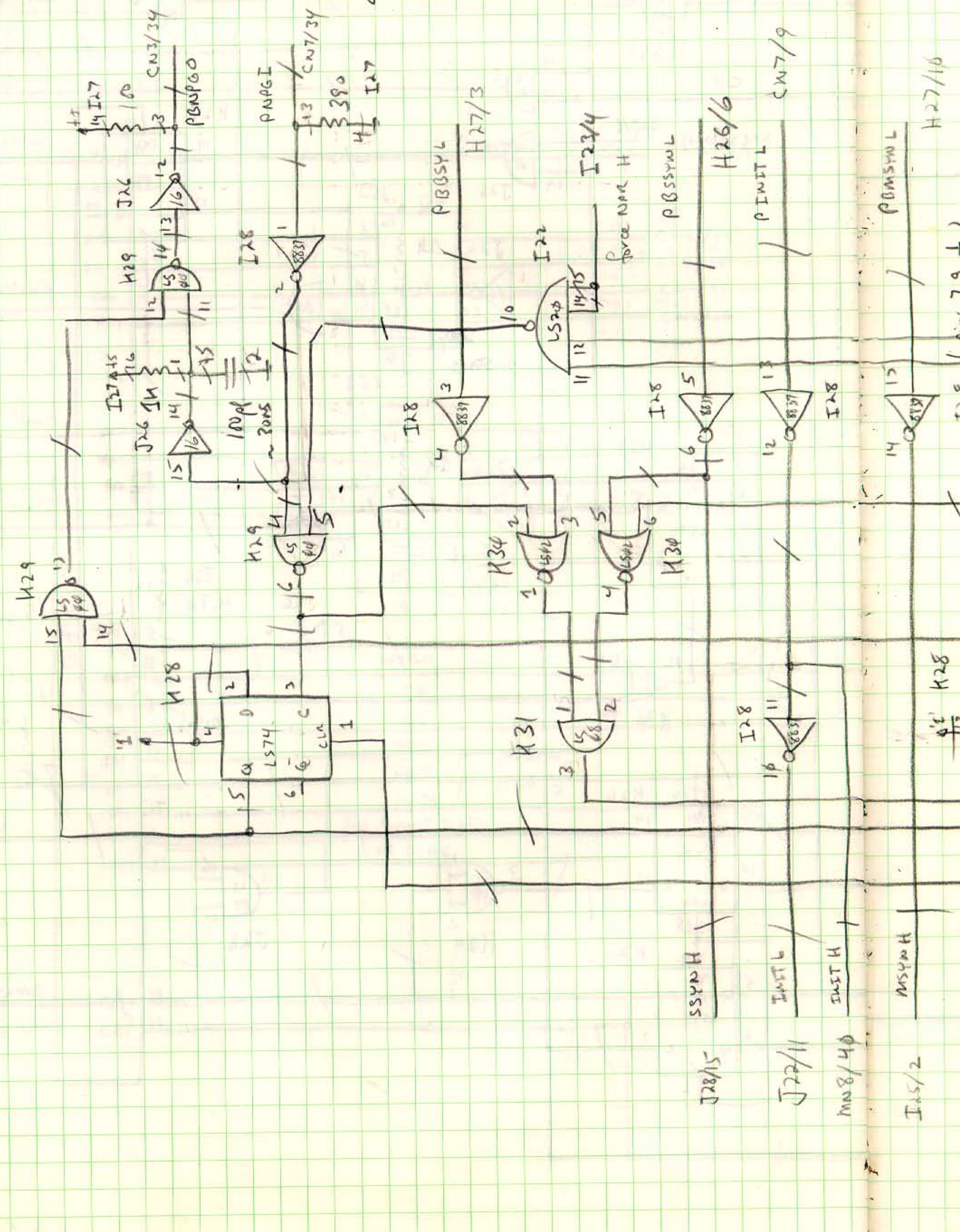
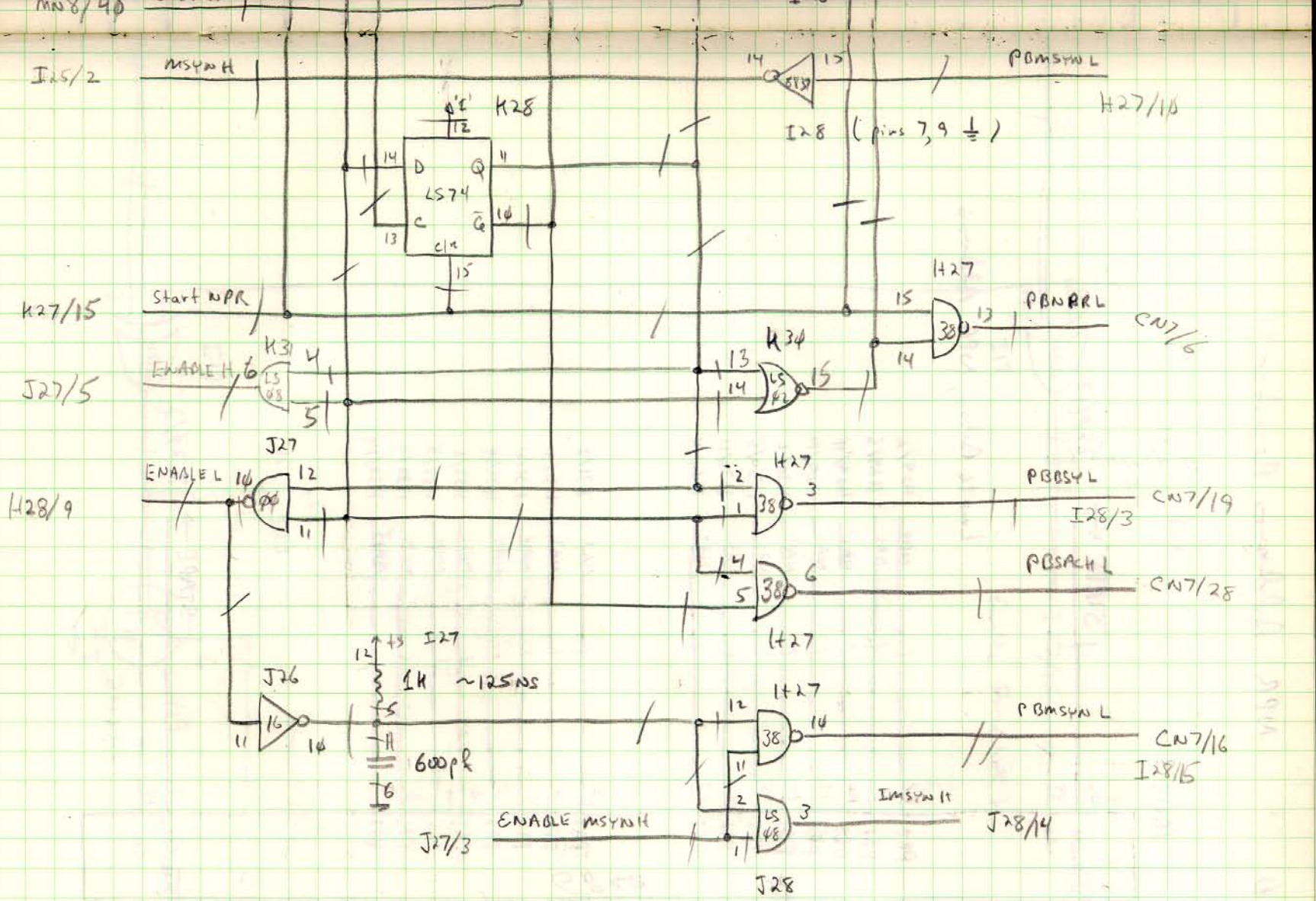
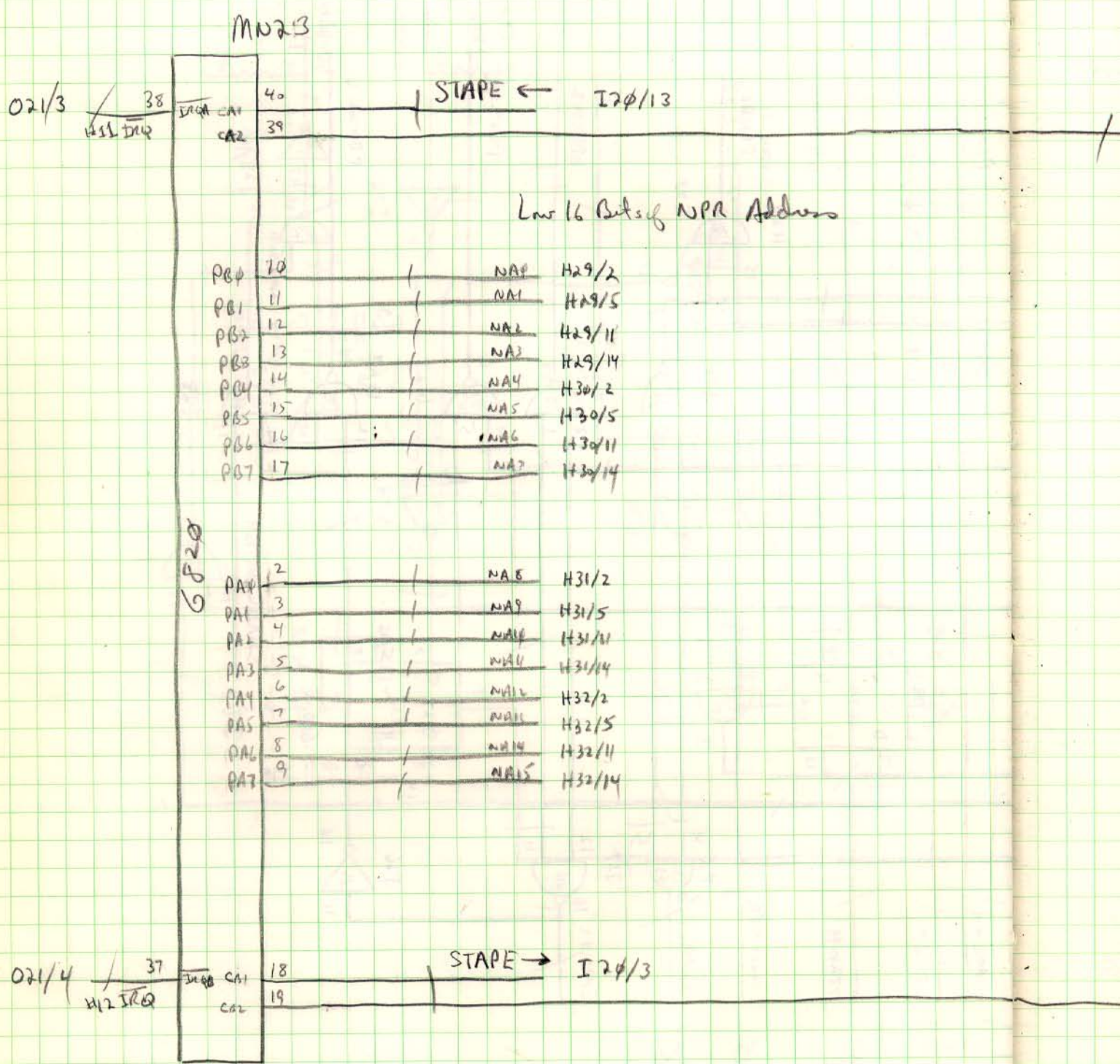
ARB

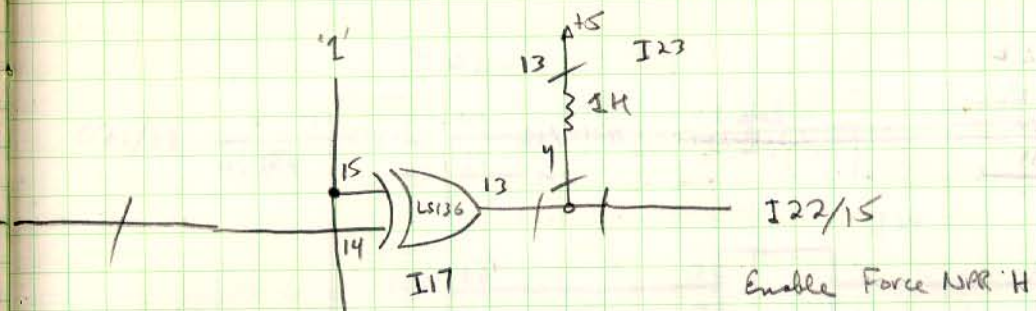
NPR Transfer Control Logic




MN8/40
I25/2
MSYN H
PBMSYN L
H27/10
I28 (pins 7, 9 ⏚)
H28
LS74
H27/15
Start NPR
H27
PBNPRL
CN7/6
H34
J27/5
ENABLE H
H31
J27
ENABLE L
H28/9
PBDSYL
CN7/19
I28/3
PBSACH L
CN7/28
J26
I27
1K ~125NS
600pf
PBMSYN L
CN7/16
I28/16
IMSYN H
ENABLE MSYN H
J27/3
J28/14
J28

Reglet 10 NPR Address Register




'1'
+5
13
I23
1H
4
15
LS136
13
14
I17
I22/15
Enable Force NPR H

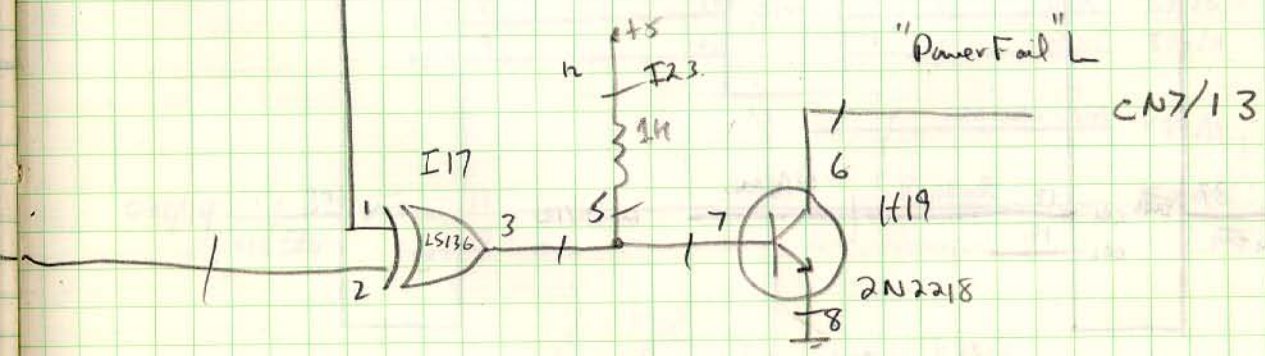

+5
12
I23
1H
I17
1
LS136
3
5
7
6
H19
2N2218
2
8
"Power Fail" L
CN7/13

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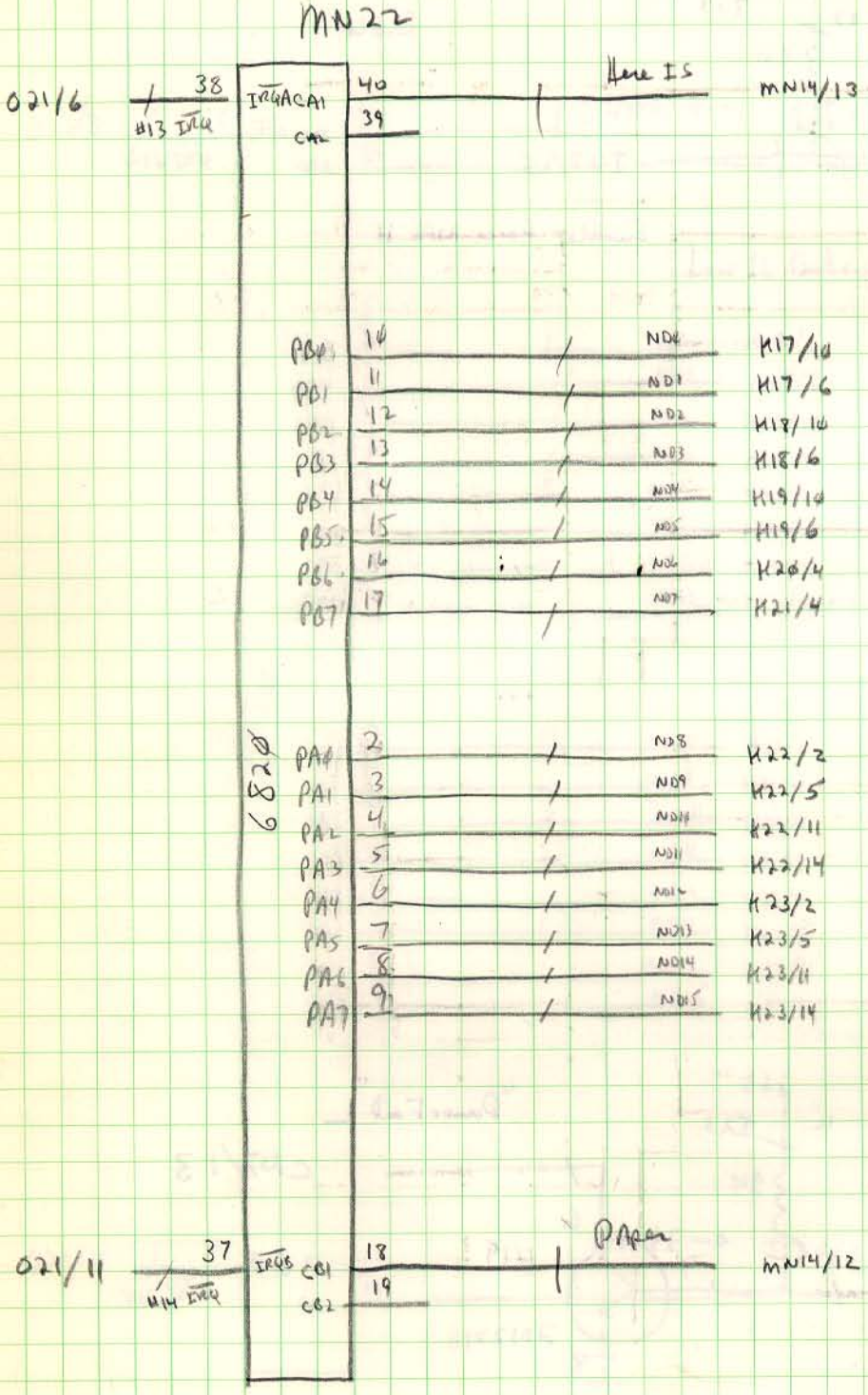
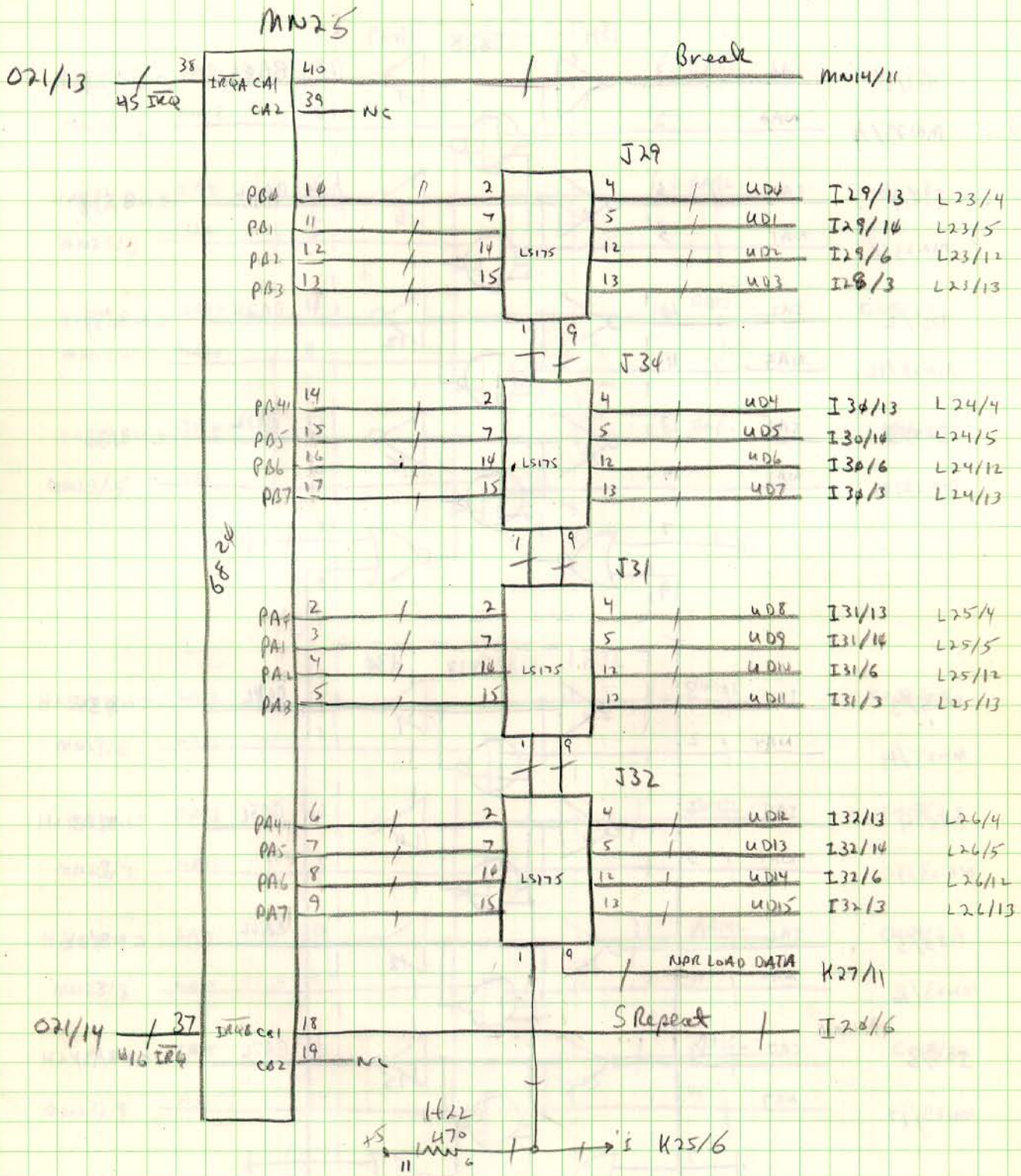
ABB

Reg Set 11 NPR Data to UNIBUS

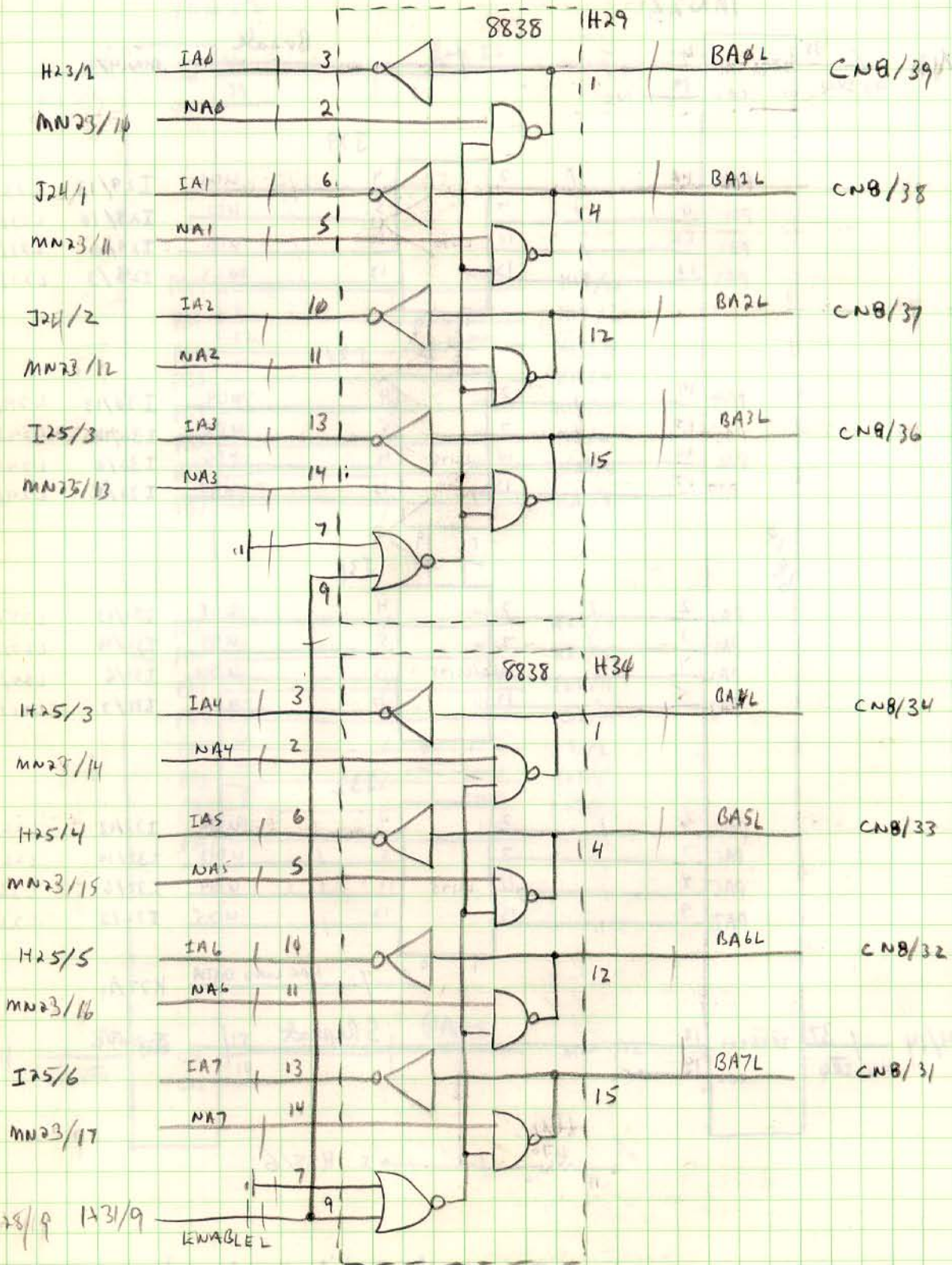


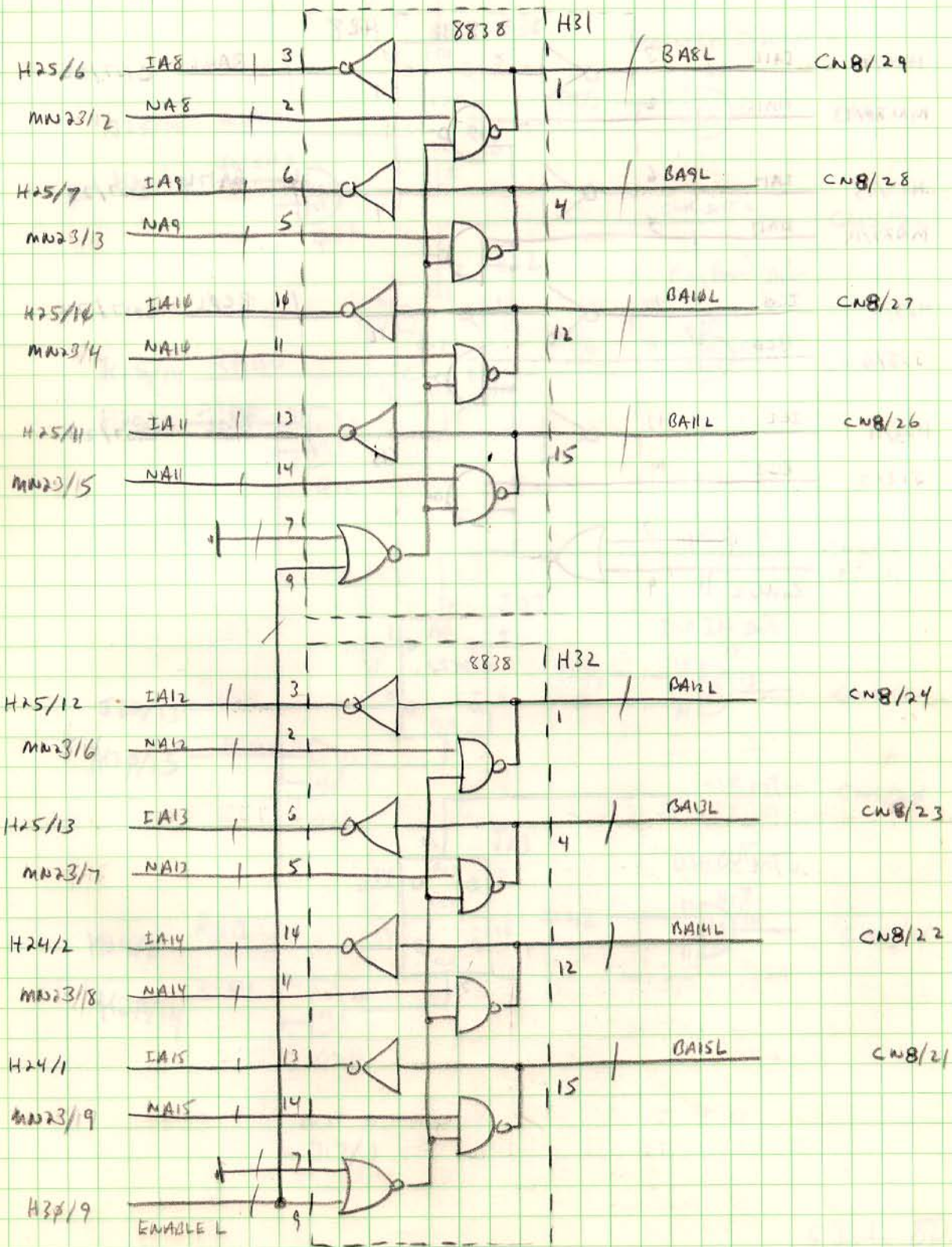


Day of the White Hurricane! 26 Jan 78

ARB

UNIBUS ADDRESS Drivers / Receivers




8838
H31
H25/6
IA8
3
BA8L
CN8/29
MN23/2
NA8
2
1
H25/7
IA9
6
BA9L
CN8/28
4
MN23/3
NA9
5
H25/10
IA10
10
BA10L
CN8/27
MN23/4
NA10
11
12
H25/11
IA11
13
BA11L
CN8/26
MN23/5
NA11
14
15
7
9
8838
H32
H25/12
IA12
3
BA12L
CN8/24
MN23/6
NA12
2
1
H25/13
IA13
6
BA13L
CN8/23
MN23/7
NA13
5
4
H24/2
IA14
14
BA14L
CN8/22
MN23/8
NA14
11
12
H24/1
IA15
13
BA15L
CN8/21
MN23/9
NA15
14
15
7
H30/9
ENABLE L
9

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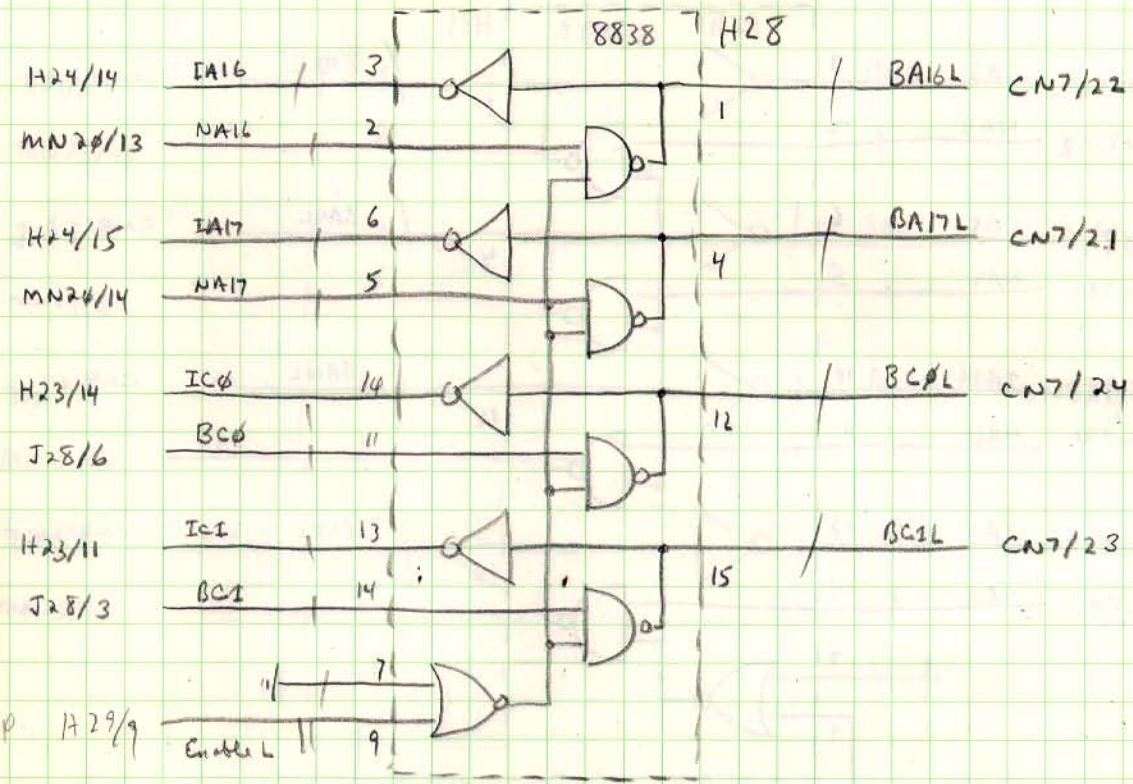
ARD

UNIBUS Address Drivers / Receivers



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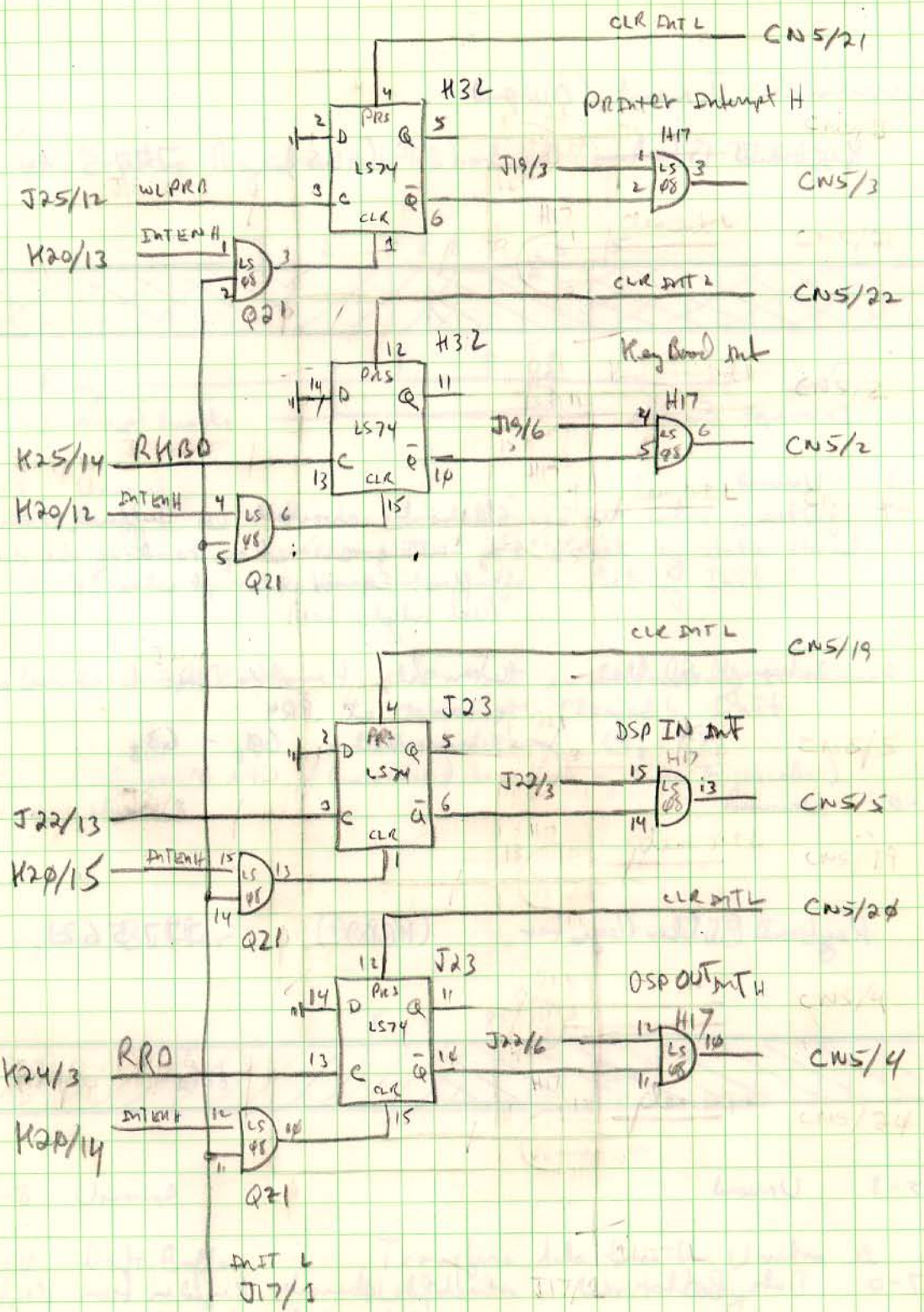
AMD

Interrupt Latches



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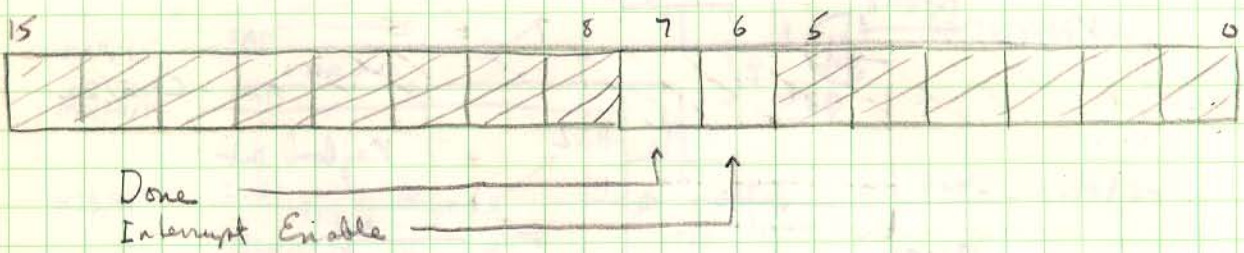
ARD

Description of UNIBUS Addressable Locations

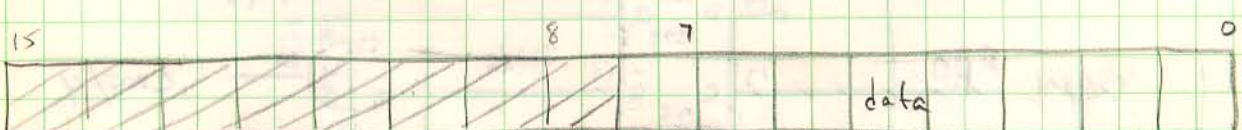
Terminal Input/Output

Keyboard Status Register (KBS) 777560_8



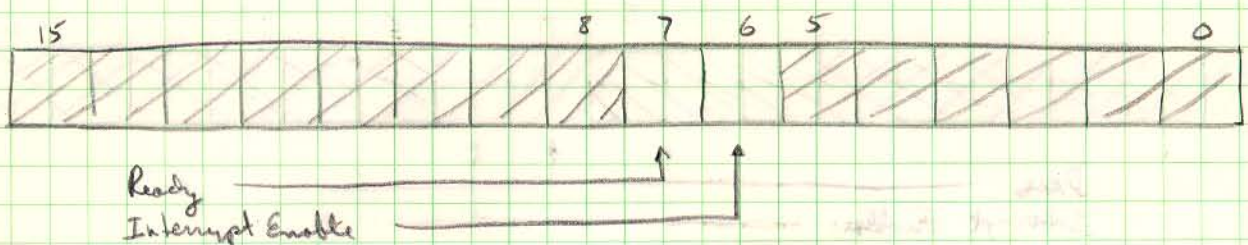
15-8	Unused	
7	Done	Character available in Buffer, cleared by INIT; cleared by reading the data buffer. Causes interrupt when IE = 1. Read only
6	Interrupt Enable	When set, it enables DONE to cause an interrupt at BR4. Normal Vector 60_8 - 63_8 (determined by CPU Microcode)
5-0	Unused	

Keyboard Buffer Register (KBB) 777562_8



15-8	Unused	
7-0	Data Buffer	Holds character keyed in from Keyboard or read by phototreader. Read only

Printer Status Register (PRS) 777564_8



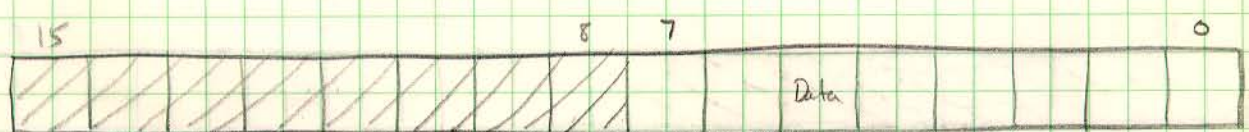
15-8 Unused

7 Ready — Printer available, is set when printing is complete. is reset by data stored into printer buffer. Set by Init. Read only.

6 Interrupt Enable — when set enables Ready to cause interrupt. Cleared by Init
Normal Vector 64_8-87_8
(determined by CPU Microcode)

5-0 Unused

Printer Buffer (PRB) 777566_8



15-8 Unused

7-0 Data Buffer — Transfers data from the Unibus to the printer. Write only

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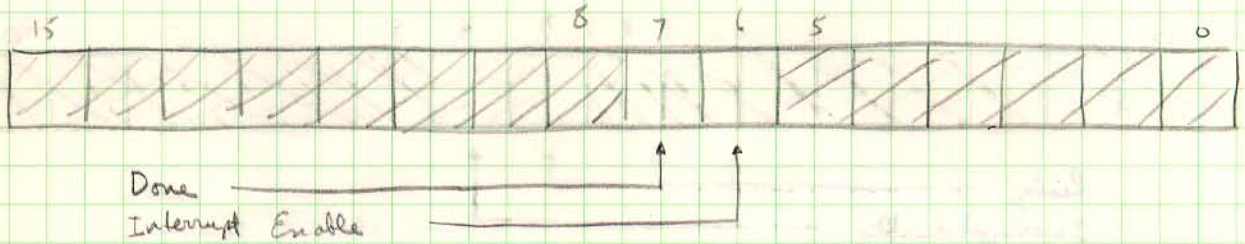
ARS

Display Processor INPUT/OUTPUT

DSP RESULT STATUS REGISTER 776670$_8$



15-8 Unused

7 Done — Operation Complete, Output data available in DSP Output Buffer (if applicable). Cleared by reading Buffer, Causes interrupt when IE = 1. Read only

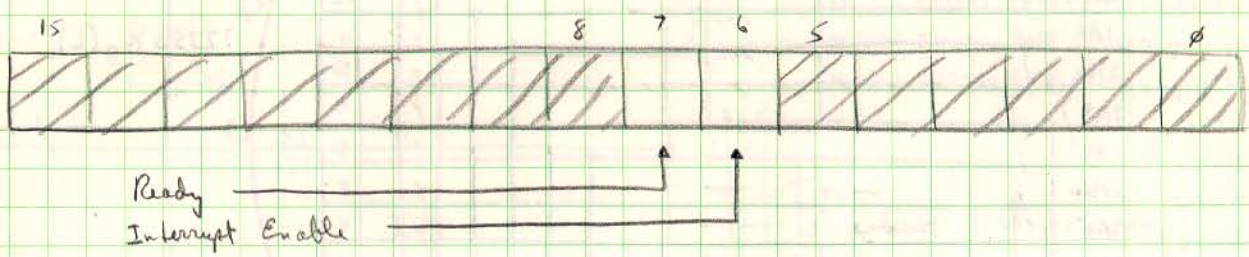
6 Interrupt Enable — when set allows Done to cause an interrupt at BR4. Normal Vector 170$_8$ - 173$_8$ (determined by CPU Microcode)

5-0 Unused

DSP RESULT Buffer Register 776672$_8$

15-0 Data Buffer — Holds data from DSP Processor. Read only

DSP FUNCTION Status Register 776674_8



15-8 Unused

7 Ready — Function Complete, is reset by data is read in the Function Buffer, set by init
Read only

6 Interrupt Enable — when set allows ready to cause interrupt
cleared by Init
Normal Vector $174_8 - 177_8$
(determined by CPU Microcode)

5-ø Unused

DSP FUNCTION Buffer Register 776676_8

15-ø FUNCTION Buffer — Holds data for DSP Processor
Write only

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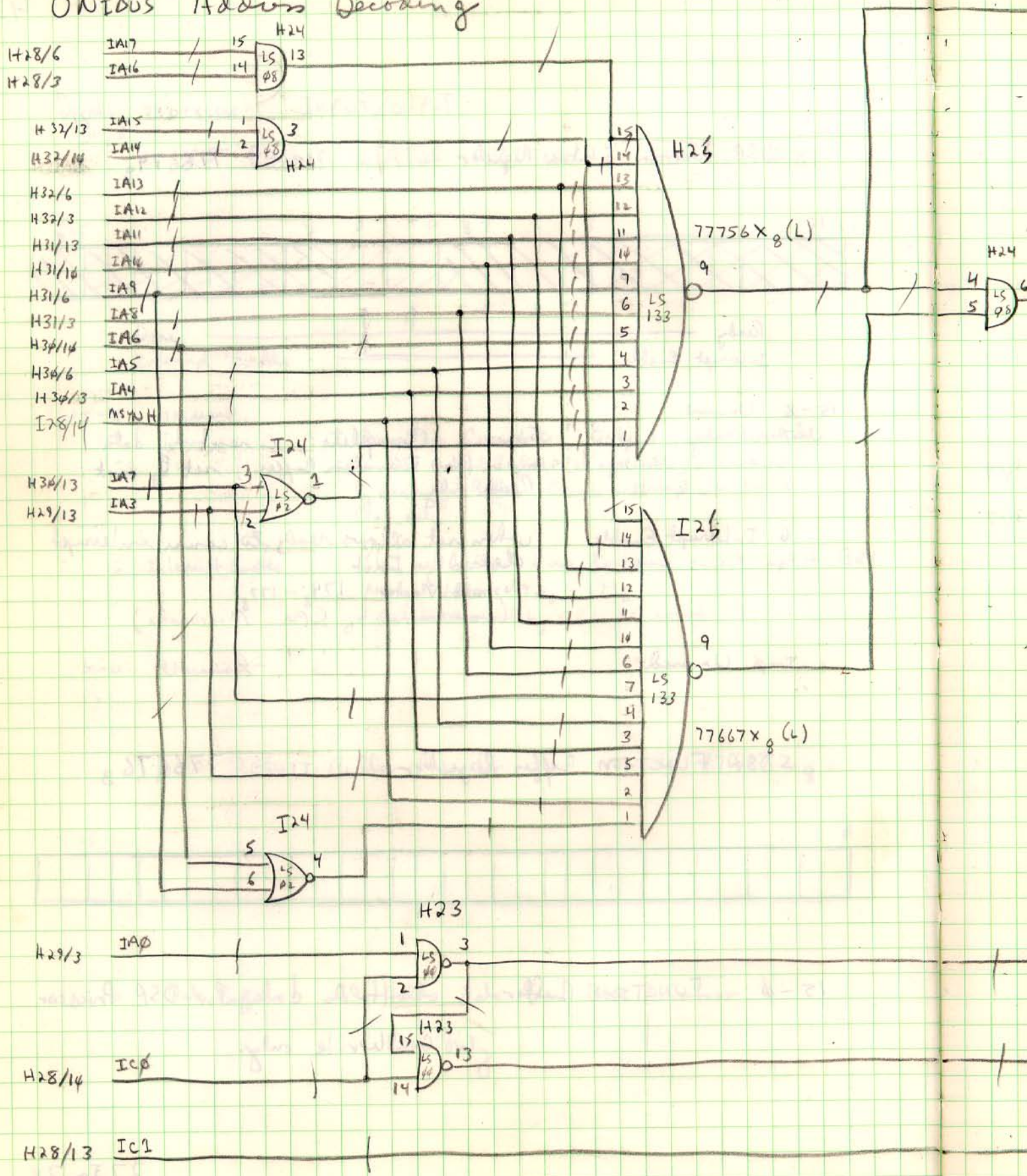
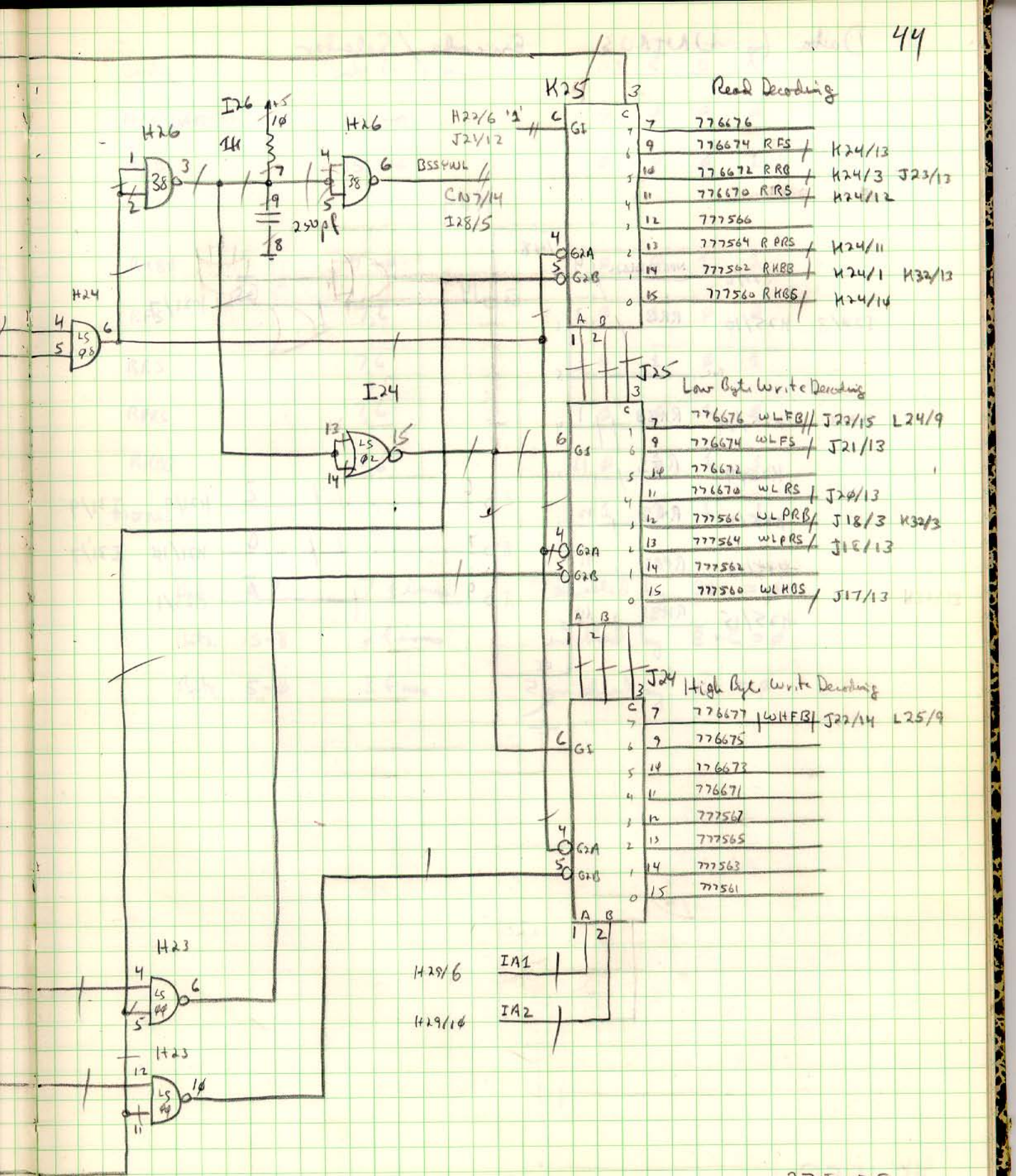
UNIBUS Address Decoding




K25
Read Decoding
H27/6 '1'
J21/12
H26
H26
I26
+5
10
1K
BSSYWL
CN7/14
I28/5
250pf
H24
I24
J25
Low Byte Write Decoding
J24
High Byte Write Decoding
H23
H23
IA1
IA2
H29/6
H29/10
777676
776676 RFS
776674 RRB
776672 RRS
776670
777566
777564 RPRS
777562 RHBB
777560 RHBS
776676 WLFB
776674 WLFS
776672
776670 WLRS
777566 WLPRB
777564 WLPRS
777562
777560 WLHBS
776677 WHFB
776675
776673
776671
777567
777565
777563
777561
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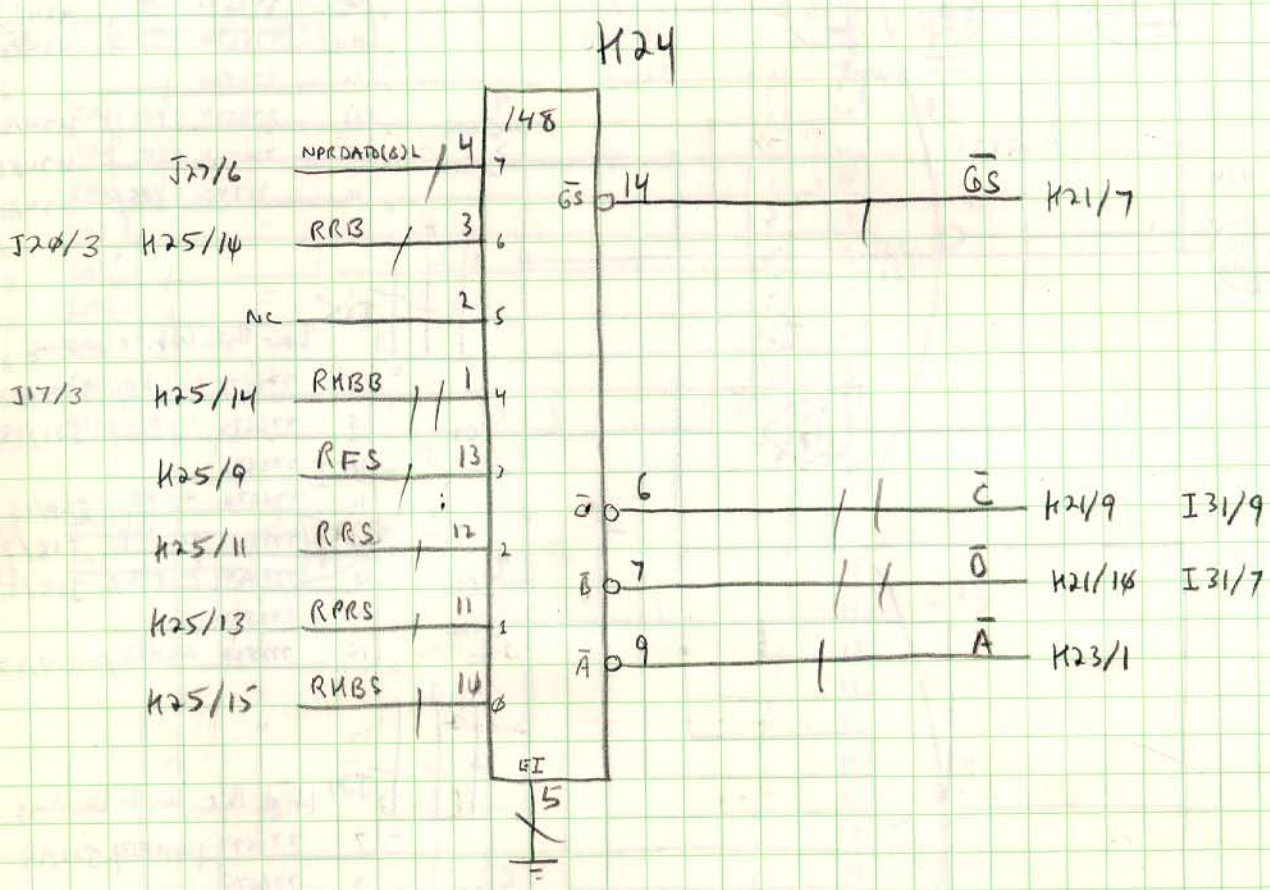
ARD

Data to UNIBUS Encode/Selector



Code	Bits to Unibus	$\overline{GS}$	$\overline{C}$	$\overline{B}$	$\overline{A}$
NPR DATO(B)	15 – 0	0	0	0	0
RRB	15 – 0	0	0	0	1
RHBB	7 – 0	0	0	1	1
RFS	7, 6	0	1	0	0
RRS	7, 6	0	1	0	1
RPRS	7, 6	0	1	1	0
RKBS	7, 6	0	1	1	1
None		1	1	1	1

Bits 6, 7	7 times	enabled by $\overline{GS} = 0$
Bits 15-8	2 times	enabled by $\overline{B} = \overline{C} = 0$
Bits 5-0	3 times	enabled by $\overline{C} = 0$

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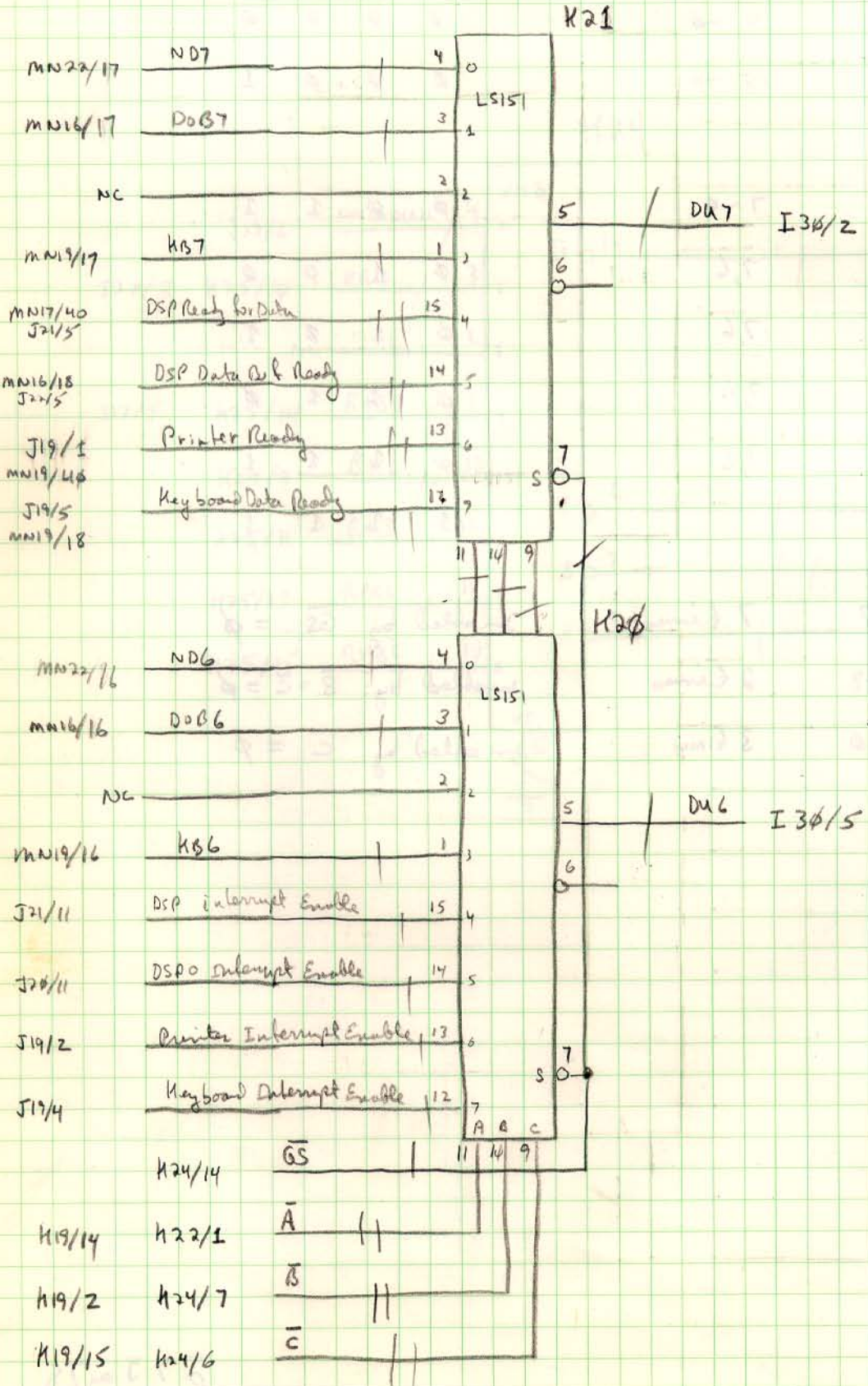
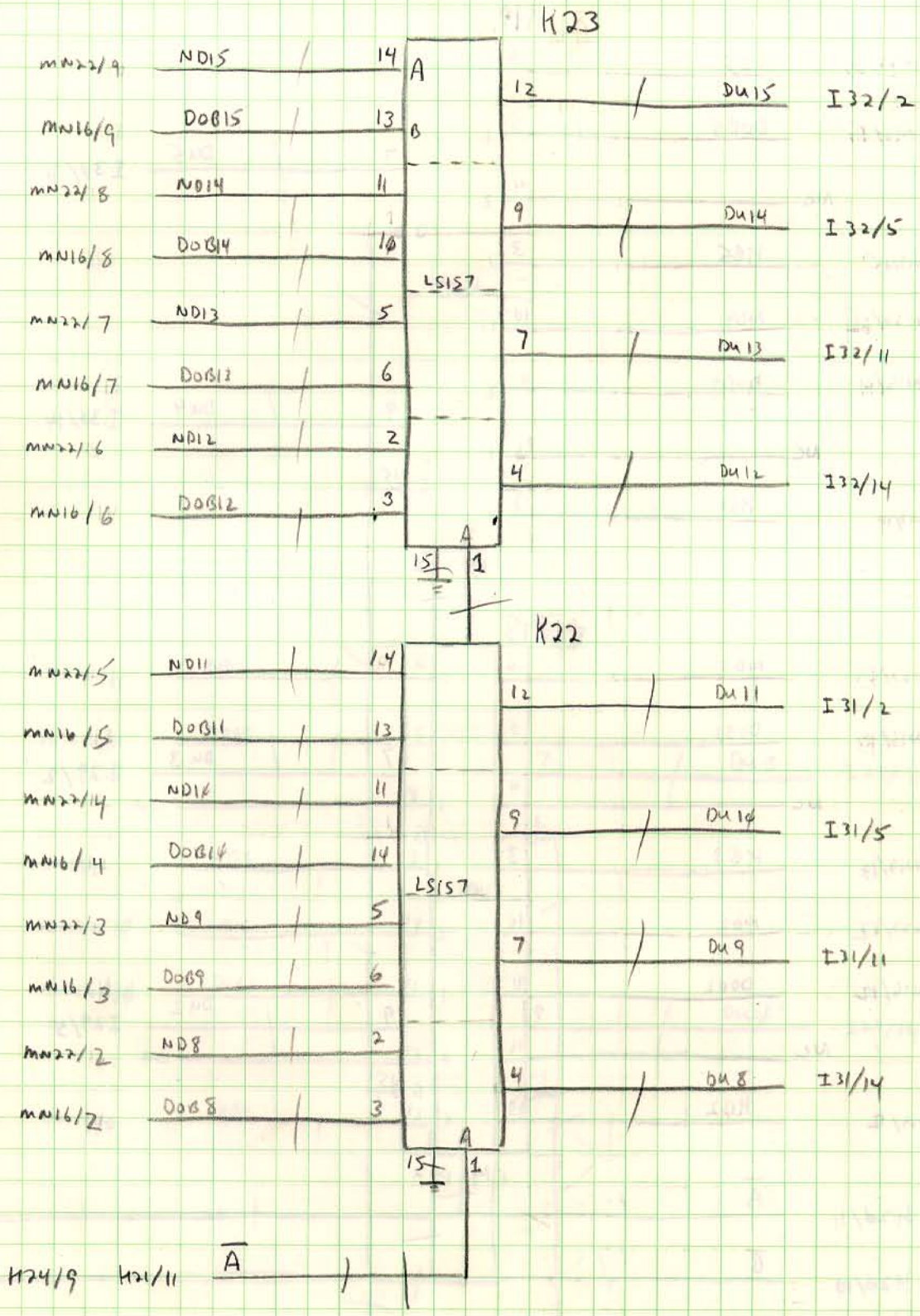
Data Selectors Bits 6-15




K23
MN22/9
NDI5
14
A
12
DU15
I32/2
MN16/9
DOBI5
13
B
MN22/8
NDI4
11
9
DU14
I32/5
MN16/8
DOBI4
10
LSI57
MN22/7
NDI3
5
7
DU13
I32/11
MN16/7
DOBI3
6
MN22/6
NDI2
2
4
DU12
I32/14
MN16/6
DOBI2
3
A
15
1
K22
MN22/5
NDII
14
12
DU11
I31/2
MN16/5
DOBII
13
MN22/4
NDI4
11
9
DU10
I31/5
MN16/4
DOBI4
14
LSI57
MN22/3
ND9
5
7
DU9
I31/11
MN16/3
DOB9
6
MN22/2
ND8
2
4
DU8
I31/14
MN16/2
DOB8
3
A
15
1
H24/9
H21/11
A

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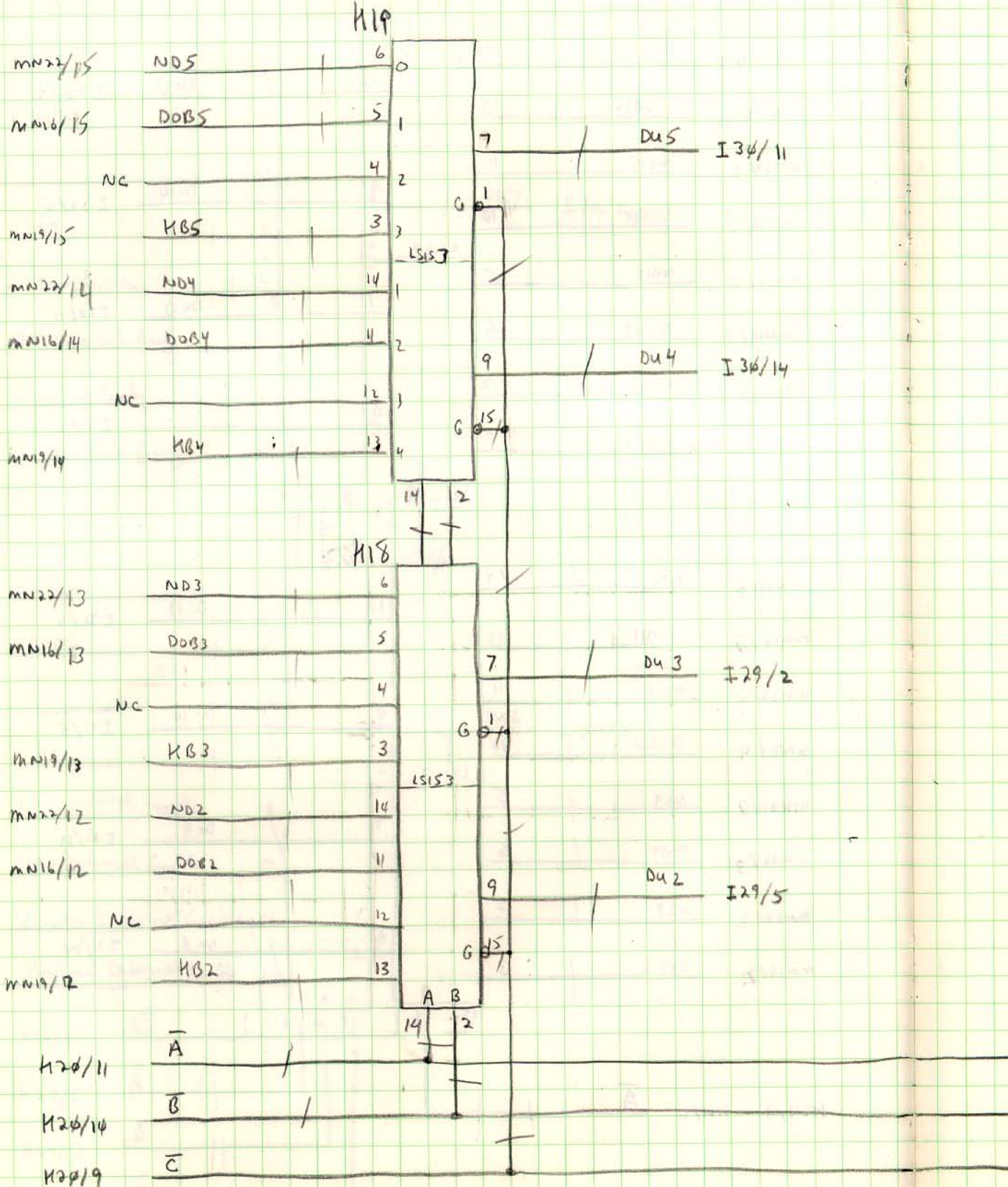
Data Selectors Bits Ø-5



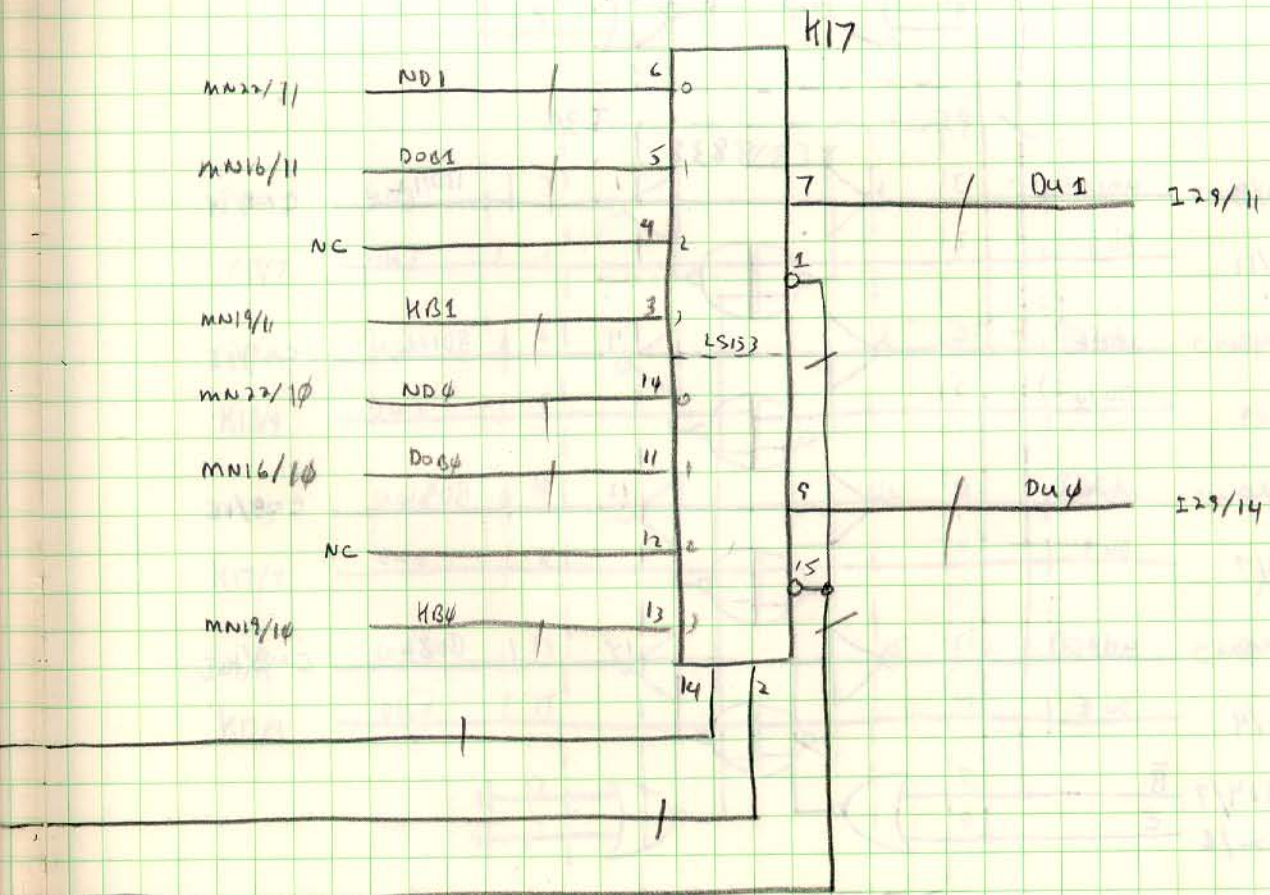

K17
MN22/11
ND1
6
MN16/11
DOB1
5
7
DU1
I29/11
NC
4
2
1
MN19/11
HB1
3
LS153
MN22/10
ND0
14
MN16/10
DOB0
11
9
DU0
I29/14
NC
12
15
MN19/10
HB0
13
14
2

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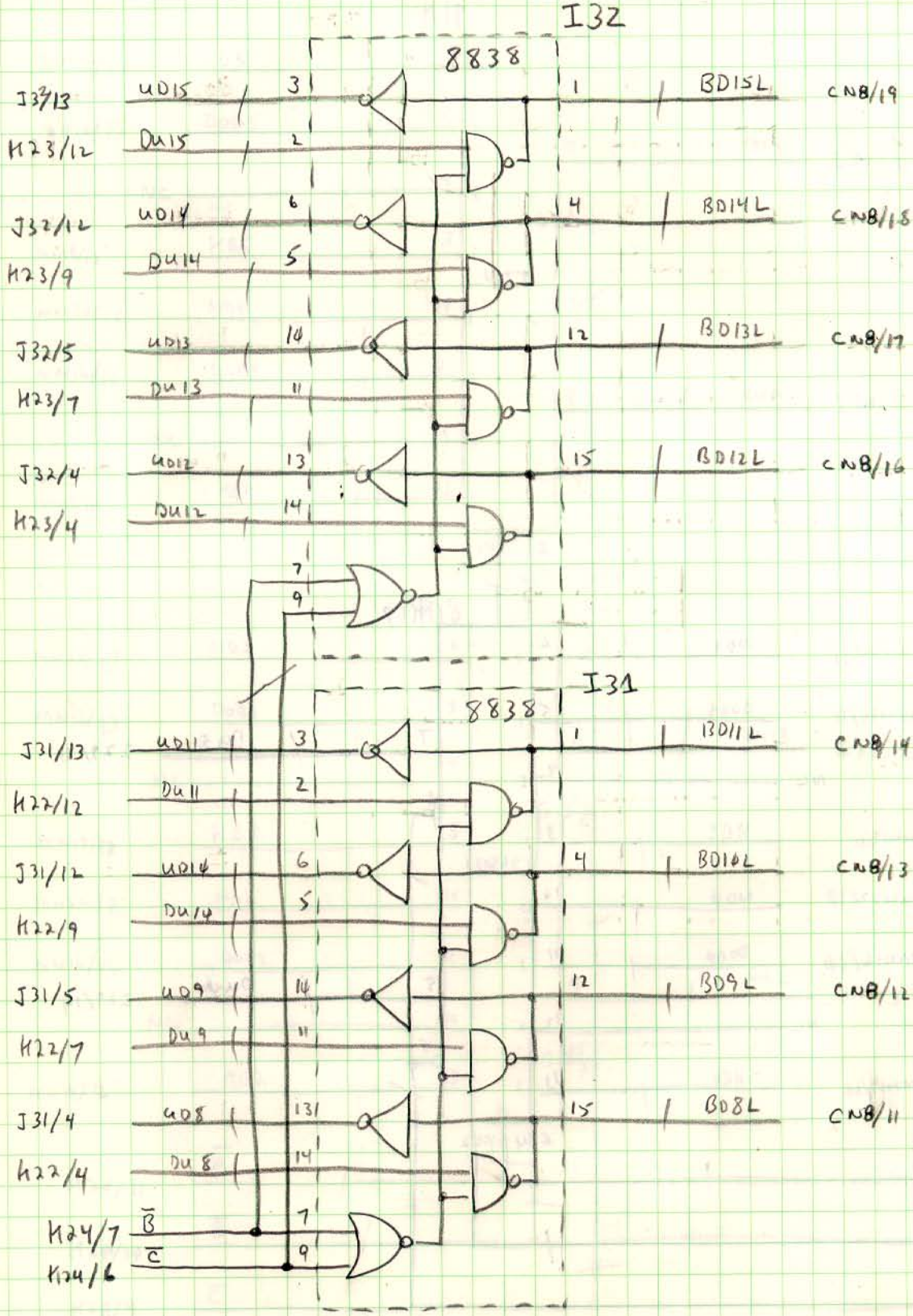
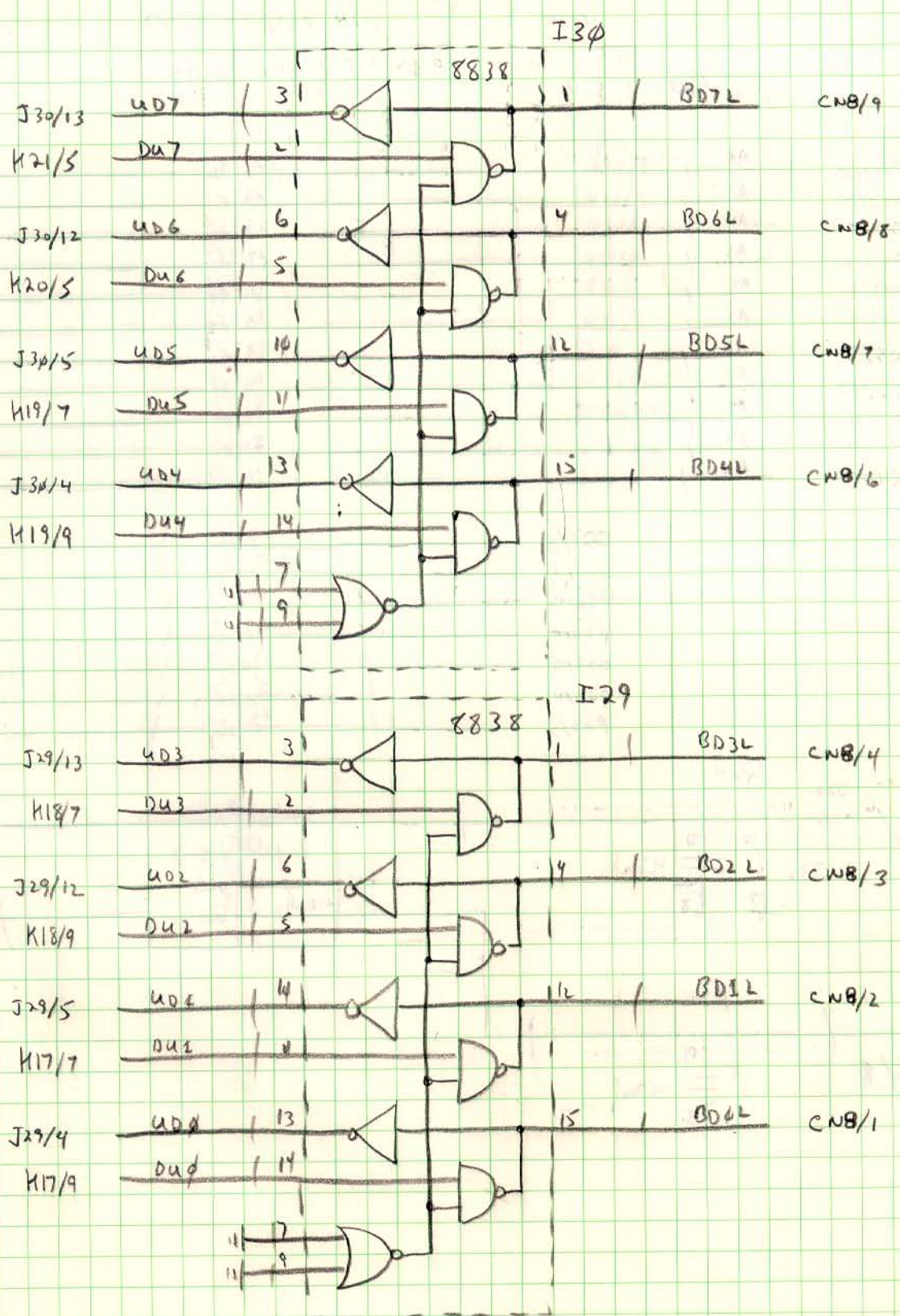
ABB

UNIBUS DATA Drivers / Receivers




I3Ø
8838
J3Ø/13
UD7
3
1
BD7L
CN8/9
H21/5
DU7
2
J3Ø/12
UD6
6
4
BD6L
CN8/8
H2Ø/5
DU6
5
J3Ø/5
UD5
1Ø
12
BD5L
CN8/7
H19/7
DU5
11
J3Ø/4
UD4
13
15
BD4L
CN8/6
H19/9
DU4
14
7
9
I29
8838
J29/13
UD3
3
1
BD3L
CN8/4
H18/7
DU3
2
J29/12
UD2
6
4
BD2L
CN8/3
H18/9
DU2
5
J29/5
UD1
1Ø
12
BD1L
CN8/2
H17/7
DU1
11
J29/4
UD0
13
15
BD0L
CN8/1
H17/9
DU0
14
7
9

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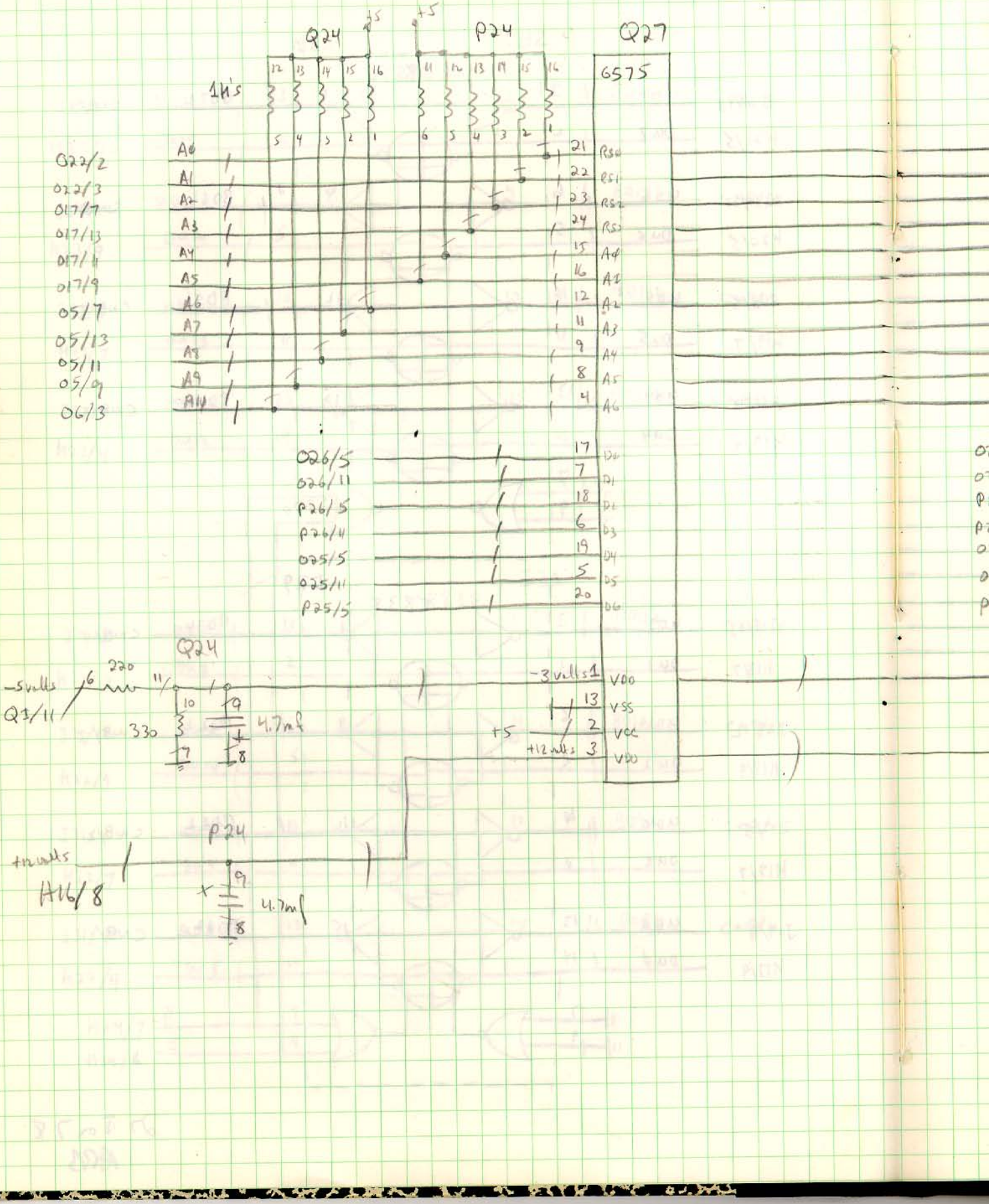
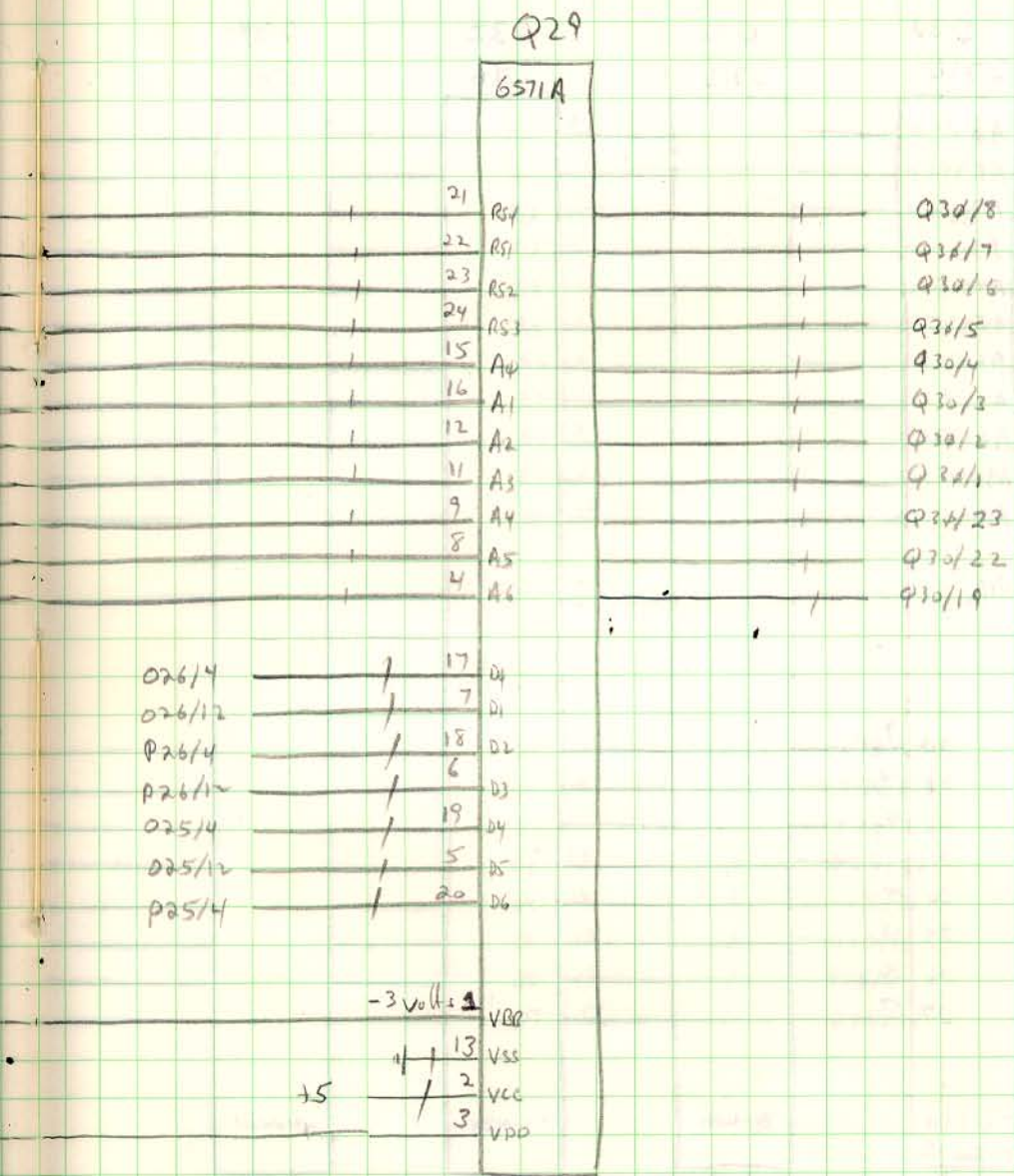
ARB

Character Roms




Q29
6571A
21 RS4
22 RS1
23 RS2
24 RS3
15 A4
16 A1
12 A2
11 A3
9 A4
8 A5
4 A6
Q30/8
Q30/7
Q30/6
Q30/5
Q30/4
Q30/3
Q30/2
Q30/1
Q30/23
Q30/22
Q30/19
Q26/4
Q26/12
P26/4
P26/12
Q25/4
Q25/12
P25/4
17 D0
7 D1
18 D2
6 D3
19 D4
5 D5
20 D6
-3 volts
1 VBB
13 VSS
+5
2 VCC
3 VPO

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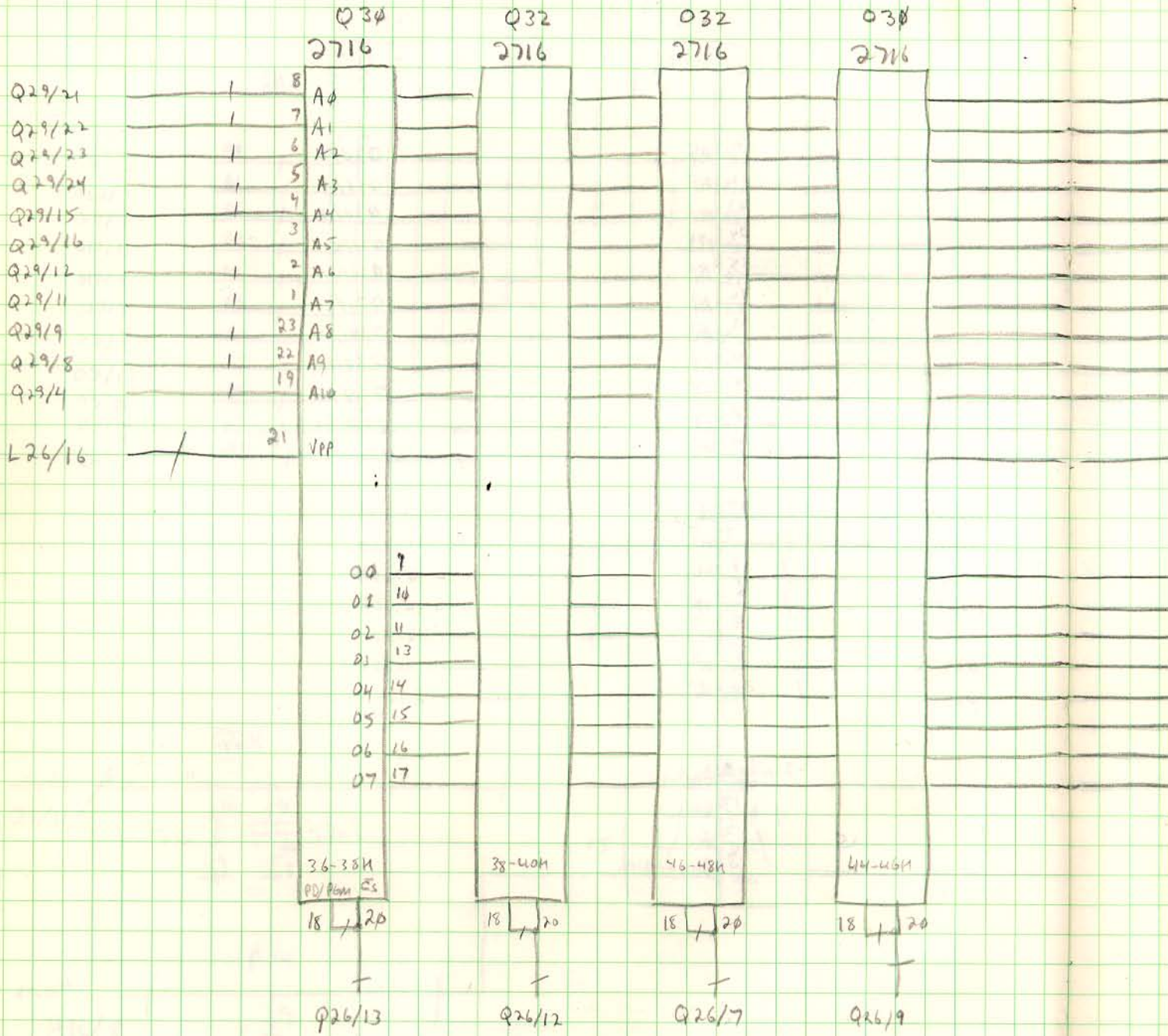
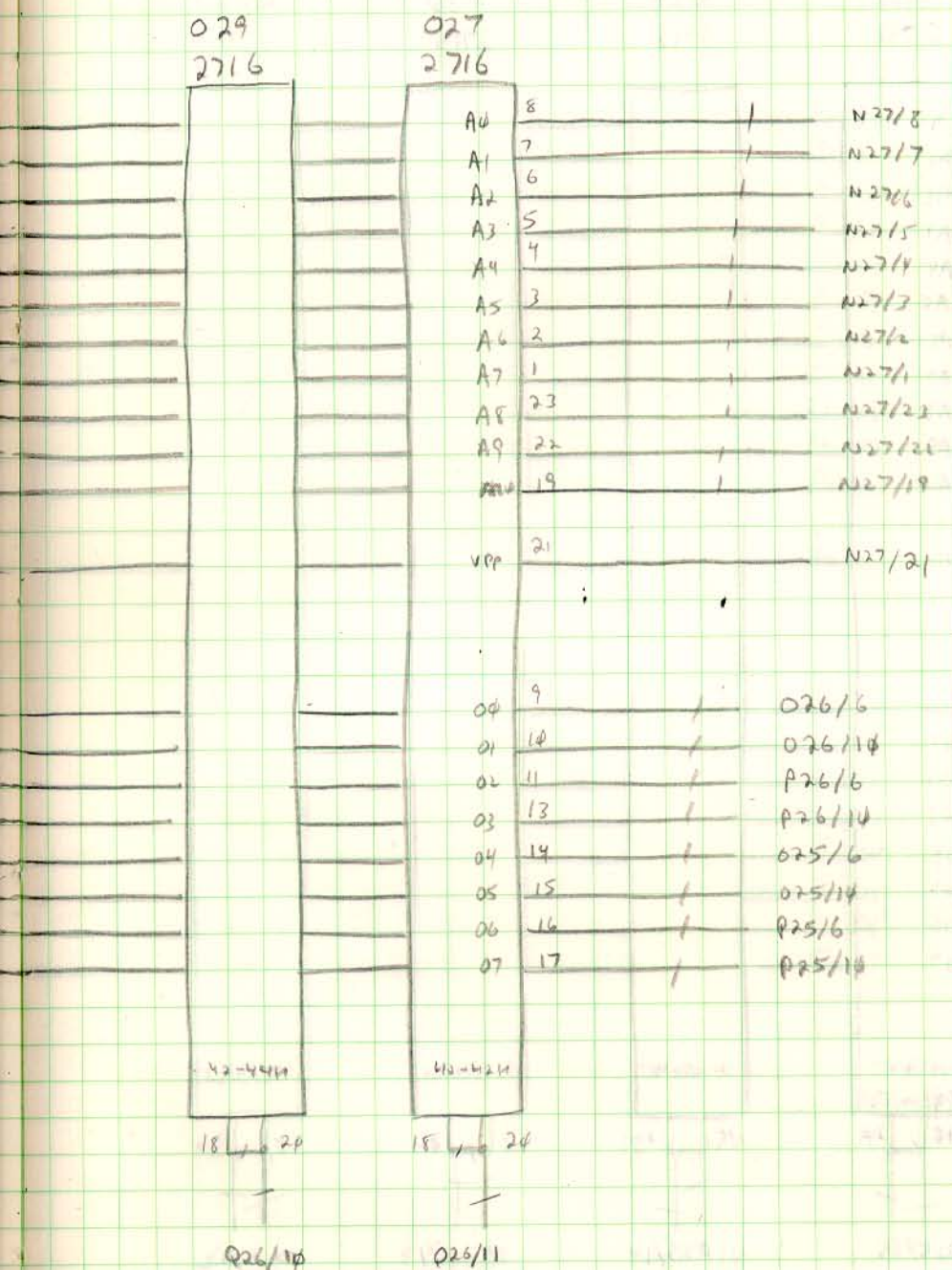
ARB

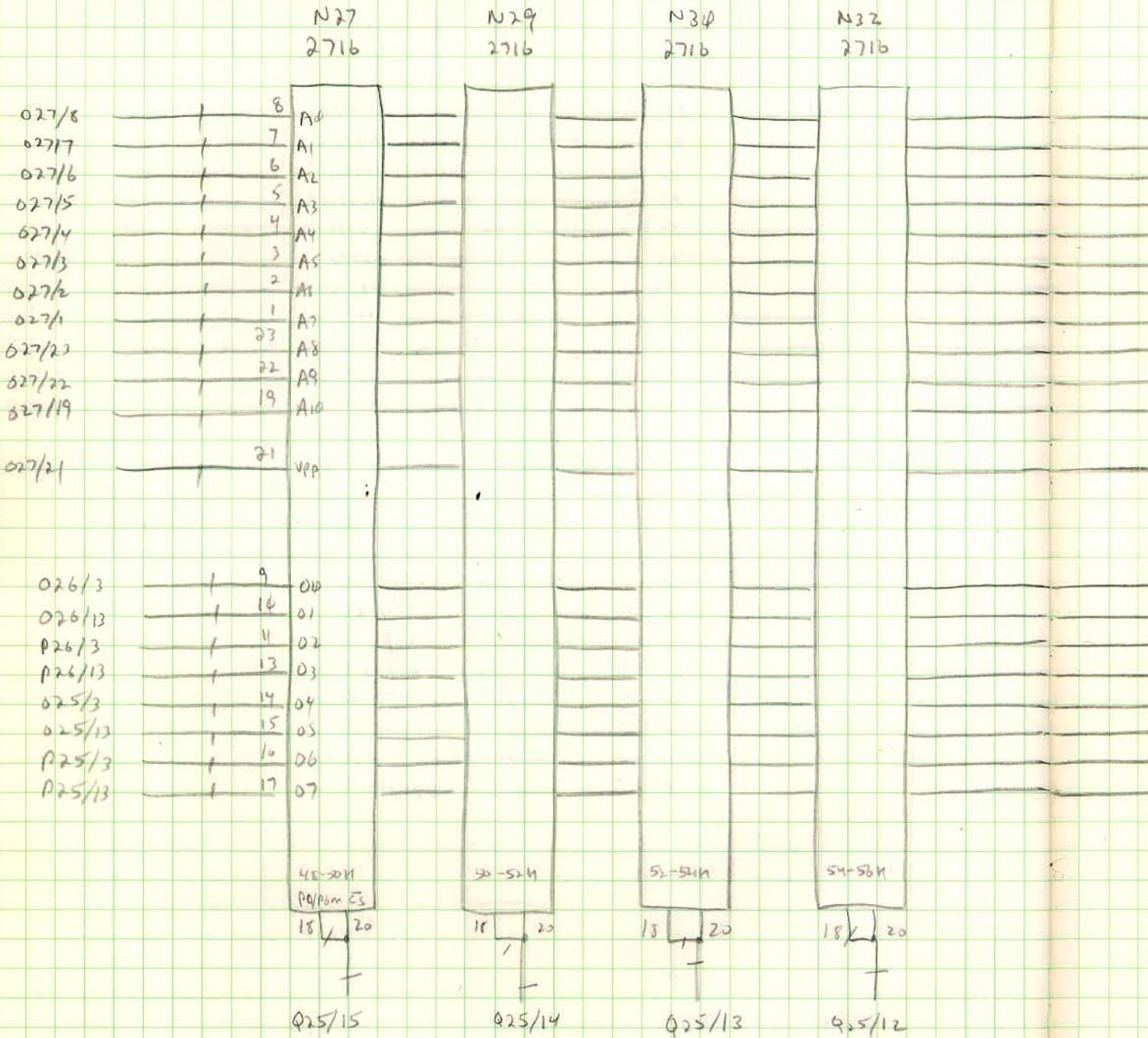
36-48H Rom in 2K x 8 Blocks

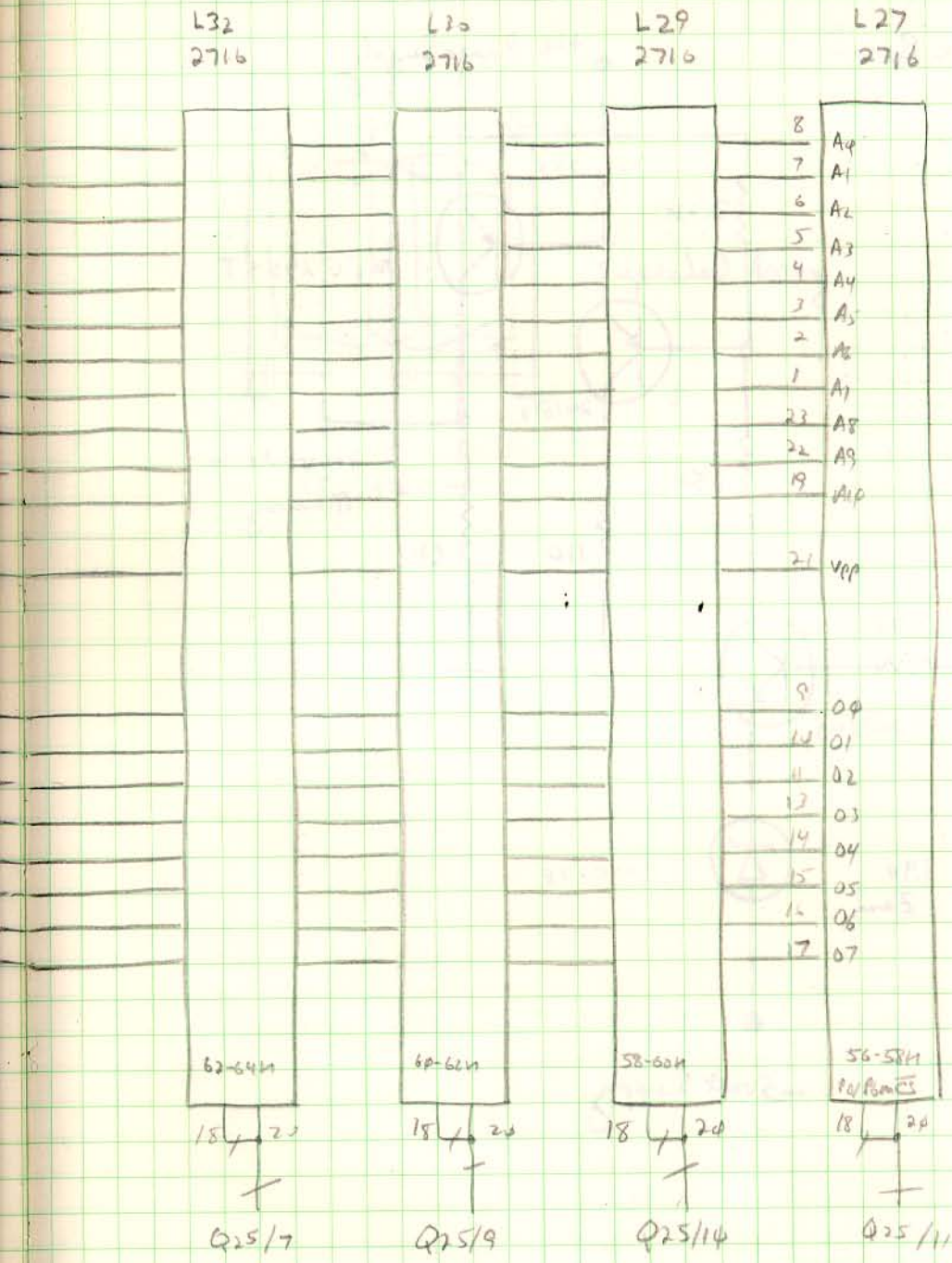



029
2716
027
2716
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
VPP
O0
O1
O2
O3
O4
O5
O6
O7
8
7
6
5
4
3
2
1
23
22
19
21
9
10
11
13
14
15
16
17
N27/8
N27/7
N27/6
N27/5
N27/4
N27/3
N27/2
N27/1
N27/23
N27/22
N27/19
N27/21
O26/6
O26/10
P26/6
P26/10
O25/6
O25/10
P25/6
P25/10
42-44μH
40-42μH
18
20
18
20
Q26/10
Q26/11

IIF-A7 P
ARC

48-64K ROM in 2K x 8 Blocks

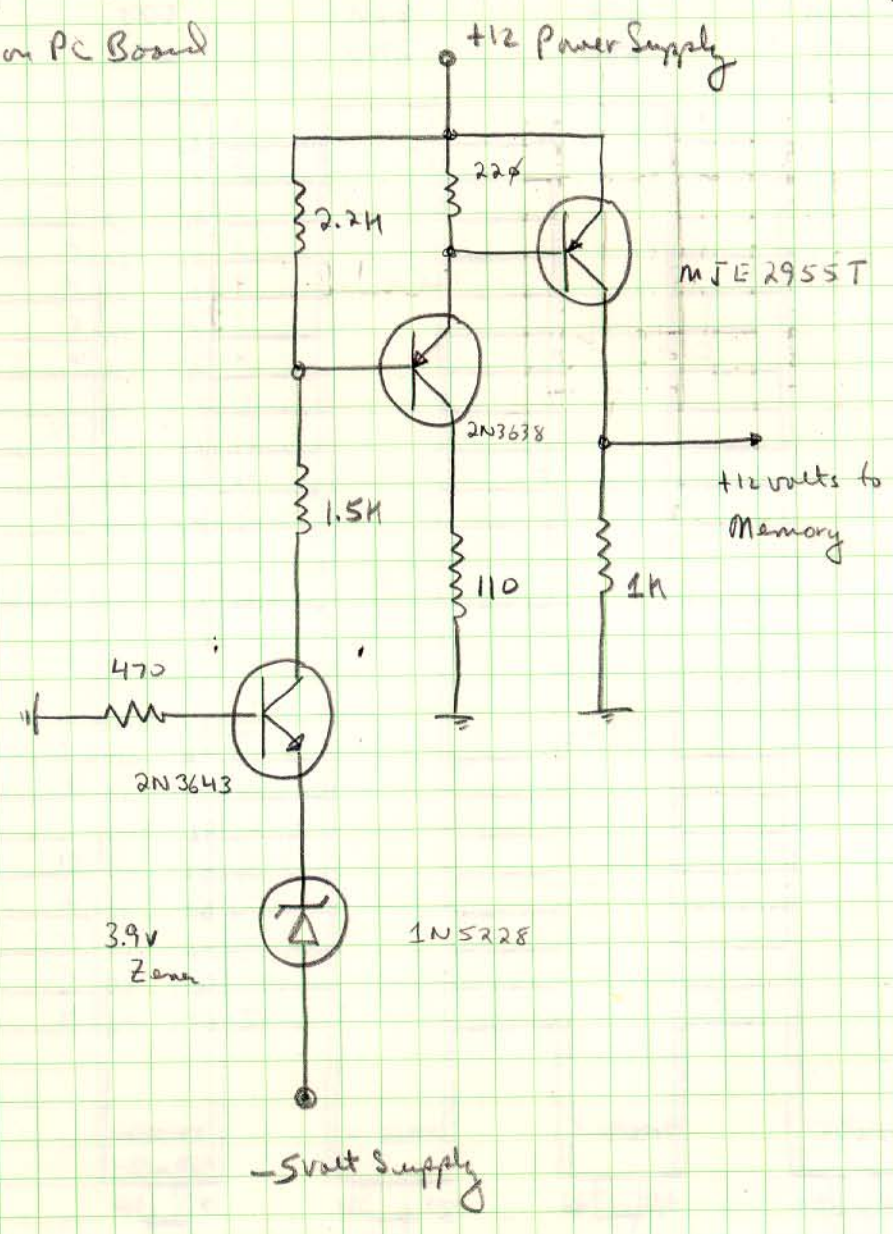



L32
2716
L30
2716
L29
2716
L27
2716
8
A0
7
A1
6
A2
5
A3
4
A4
3
A5
2
A6
1
A7
23
A8
22
A9
19
A10
21
VPP
9
O0
10
O1
11
O2
13
O3
14
O4
15
O5
16
O6
17
O7
62-64M
60-62M
58-60M
56-58M
PD/PGM
CS
18
20
Q25/7
Q25/9
Q25/14
Q25/11

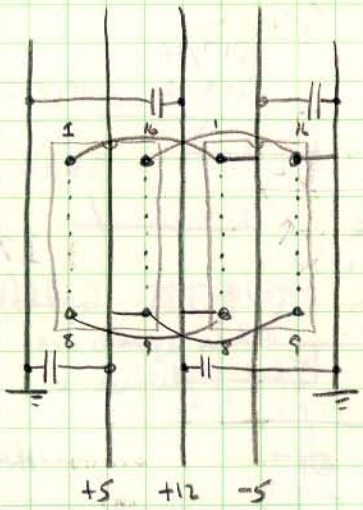
11F-0678
ABD

Memory Bias Protect Cricuit

Hardwired on PC Board



Memory Power Connections (4096)



repeated Array

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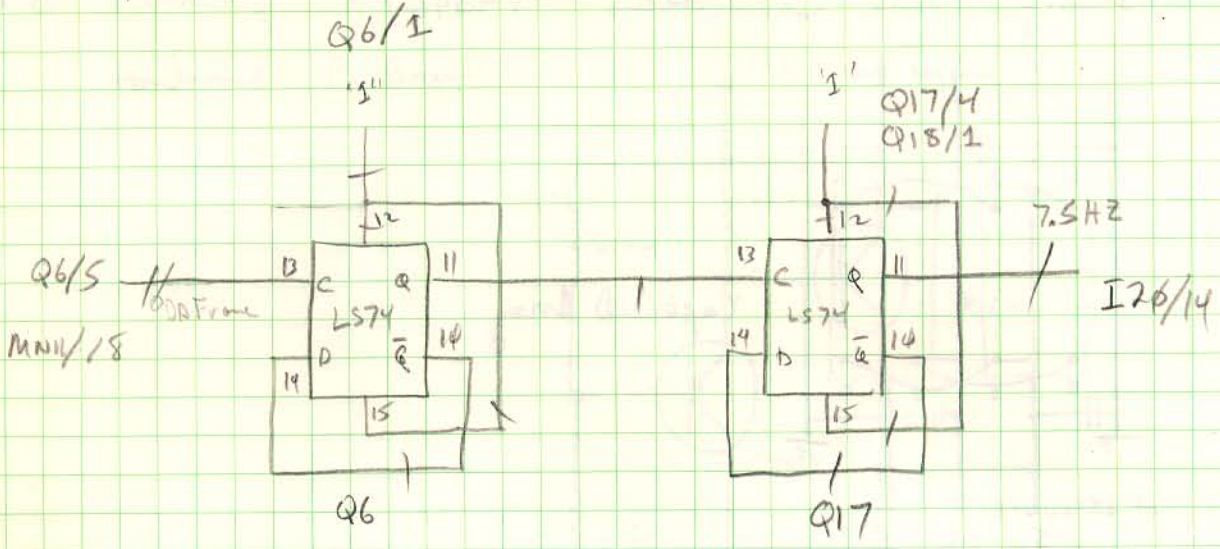
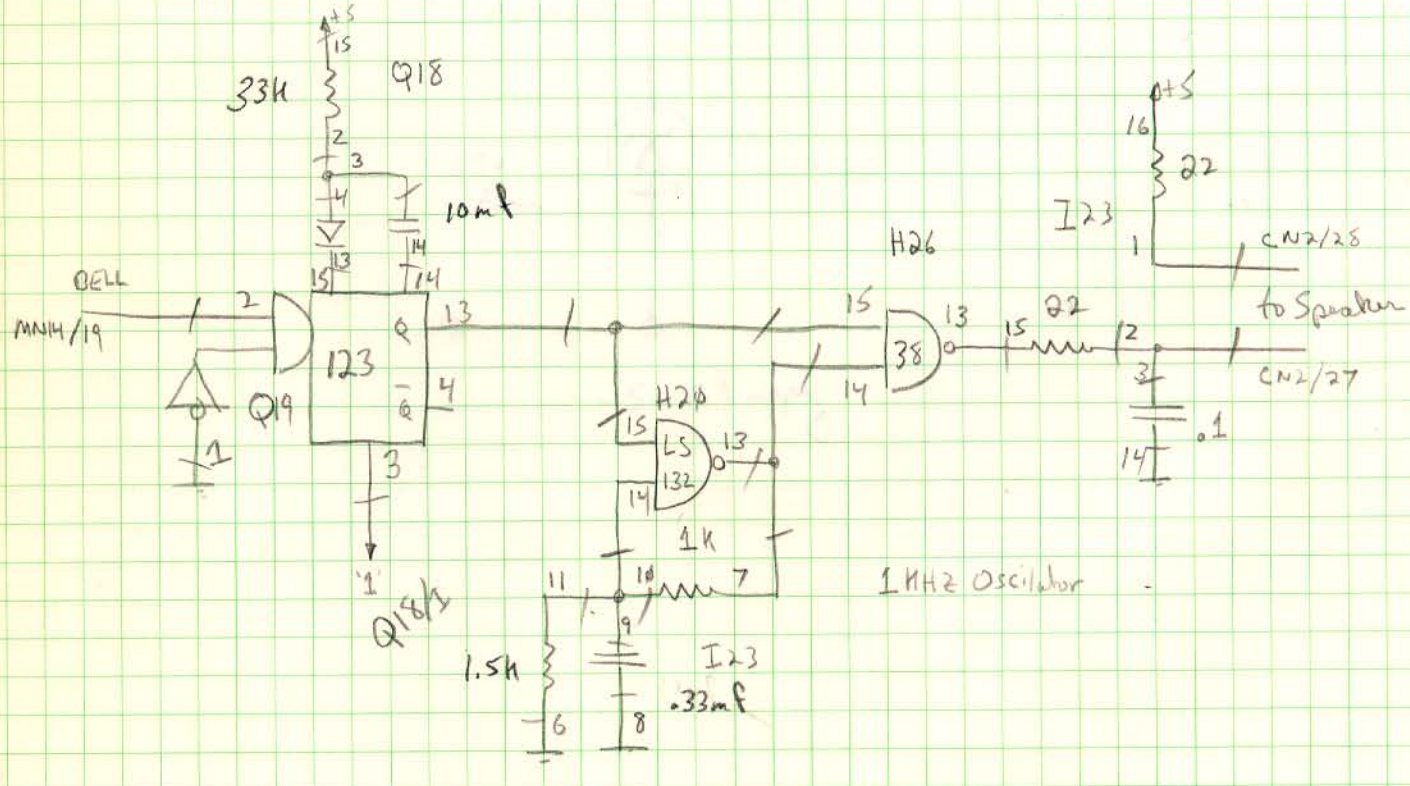
ARD

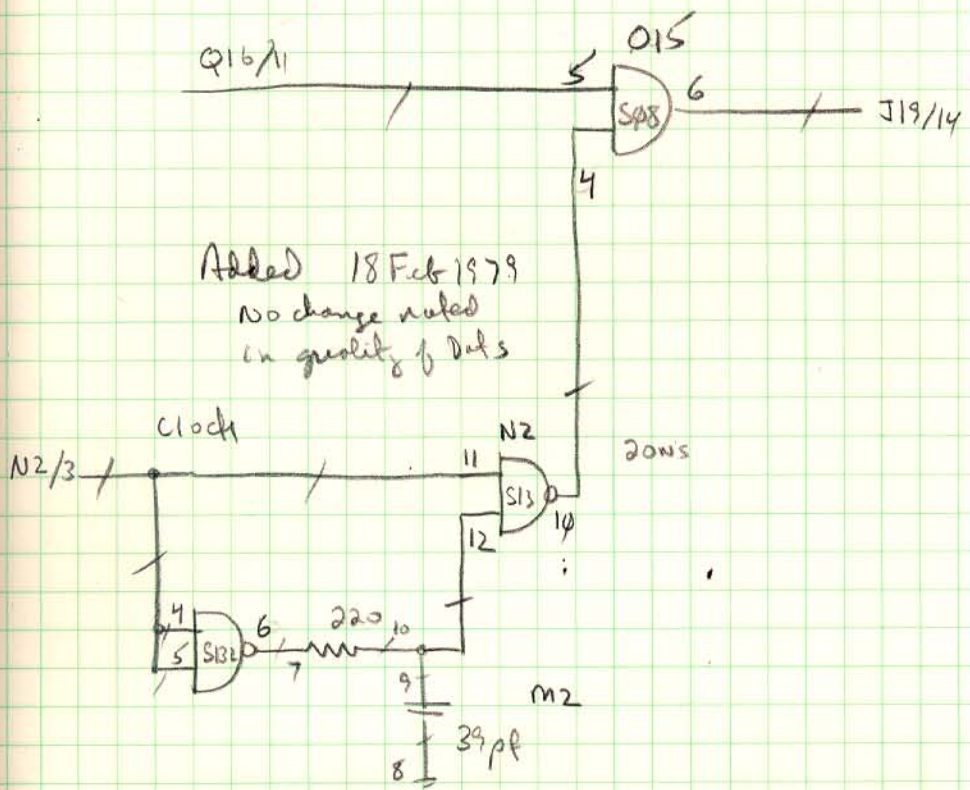
Repeat Divider



Bell Sounder



Dat chopper (See page 29)



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ARO

IC Types & Location

A9 - A16	4096 Memory	Pages
B9 - B16	"	22, 23, 25
C9 - C16	"	
D9 - D16	"	
E9 - E16	"	
F9 - F16	"	
G9 - G16	"	
H9 - H16	"	

		Page
H17	LSØ8	41
H18	RES	29
H19	RES	11, 31
H2Ø	LS132	11, 53
H21	LSØL	11
H22	RES	31
H23	LSØØ	44
H24	LSØ8	44
H25	LS133	44
H26	38	44, 53
H27	38	37
H28	8838	41
H29	8838	4Ø
H3Ø	8838	4Ø
H31	8838	4Ø
H32	8838	4Ø

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ARD

I9	S153	22
I10	S253	23
I11	S253	24
I12	365	24
I13	8T95	24
I14	8T95	24
I15	LS175	30
I16	LS175	30

I17	LS136	29
I18	S86	29
I19	RES	29
I20	LSØØ	31
I21	LS14	31
I22	LS2Ø	11
I23	RES	'53
I24	LSØ2	44
I25	LS133	44
I26	RES	36, 44
I27	RES	37
I28	8837	37
I29	8838	48
I30	8838	48
I31	8838	48
I32	8838	48

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J9	S153	22
J14	S253	23
J11	S253	24
J12	365	23
J13	Φ8	16
J14	Φ8	16
J15	LS157	3Φ
J16	LS157	3Φ

J17	LS74	32
J18	LS74	32
J19	S08	32, 34
J20	LS74	34
J21	LS74	33
J22	08	33
J23	~~*~~LS74	41
J24	LS138	44
J25	LS138	44
J26	16	36, 37
J27	04	36, 37
J28	LS08	36
J29	LS175	39
J30	LS175	39
J31	LS175	39
J32	LS175	39

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ARM

H9	S153	22
H10	S253	23
H11	S253	24
H12	X	
H13	Ø4	16
H14	LS138	16
H15	165	3Ø

H17	LS153	47
H18	LS153	47
H19	LS153	47
H20	LS151	46
H21	LS151	46
H22	LS157	46
H23	LS157	46
H24	148	45
H25	LS138	44
H26	LS74	36
H27	LS74	36
H28	LS74	37
H29	HS00	36, 37
H30	LS02	36, 37
H31	LS08	37
H32	LS74	41

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AGM

L1	32	14 , 15 , 16
L2	ØØ	8 , 15
L3	32	15
L4	LS153	2Ø
L5	LS153	2Ø
L6	LS153	2Ø
L7	LS153	2Ø
L8	ØØ	8, 34 , 29
L9	LS157	16
L10	LS32	14
L11	LS138	14
L12	RES	, 14 , 3Ø
L13	LSØ5	14
L14	LSØ4	15 , 16 , 18 , 2Ø , 21 .
L15	LS138	15
L16	LS138	15

L17	LS175	31
L18	LS175	31
L19	LS175	32
L20	LS175	32
L21	LS175	36
L22	LS175	36
L23	LS175	33
L24	LS175	33
L25	LS175	33
L26	LS175	33
L27		
L29		
L34		
L32		

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AHD

M1	SΦΦ	9
M2	X	
M3	LS133	18
M5	8833	2Φ
M26	8833	21

N1	164	8
N2	S132	8, 9
N3	RES	7, 8, 11
N5	8833	2Φ
N26	8833	21
N27		
N29		
N3Φ		
N32		

MN 4	6800	11
MN 7	6820	26 , 28
MN 8	6820	26 , 27
MN 10	6820	26 , 27
MN 11	6820	26 , 28
MN 13	6820	26 , 35
MN 14	6820	26 , 31
MN 16	6820	26 , 34
MN 17	6820	26 , 33
MN 19	6820	26 , 32
MN 20	6820	26 , 36
MN 22	6820	26 , 39
MN 23	6820	26 , 39
MN 25	6820	26 , 38

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ARD

01	S74	8
02	LS193	8
03	33	8
04	8T95	11
05	8T95	11
06	8T95	11
07	LS193	28
08	LS193	28
09	LS193	27
014	LS193	27
011	LS193	27
012	LS193	27
013	LS193	28
014	LS193	28
015	LS48	29, 14
016	X	

017	8T95	19
018	LS174	19
019	LS174	19
020	LS174	19
021	LS174	19
022	LS02	18
023	LS10	18 , 20
024	LS00	20 , 21
025	LS153	21
026	LS153	21
027		
029		
030		
032		

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AMD

P1	123	8
P2	RES	8
P3	LS1ϕ	8, 15
P4	RES	29
P5	ϕ4	7
P6	RES	27, 28
P7	LS266	28
P8	LS266	28
P9	LS266	27
P10	LS266	27
P11	LS266	27
P12	LS266	27
P13	LS32	28
P14	LS32	28, 29
P15	LS74	29
P16	LS74	29

P17	LSØ8	18, 19
P18	LS11	19
P19	148	19
P2Ø	148	19
P21	148	19
P22	LSØ4	18, 19
P23	LS11	18
P24	RES	49
P25	LS153	21
P26	LS153	21
P27		
P29		
P3Ø		
P32		

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ARD

Q1	X	
Q2	Crystal	7
Q3	4024	7
Q4	LS74	7
Q5	5320	7
Q6	LS74	7
Q7	LS74	10
Q8	04	9, 10
Q9	LS193	10
Q10	LS193	10
Q11	X	
Q12	08	29
Q13	LS74	29
Q14	LS74	29
Q15	LS74	29
Q16	S74	29

Q17	LS74	19
Q18	RES	19, 53
Q19	123	53
Q20	X	
Q21	LS08	41
Q22	X	
Q23	X	
Q24	RES	49
Q25	LS138	14
Q26	LS138	14
Q27	MC6575	Character Rom
Q29	MC6571A	Character Rom
Q34		
Q32		

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ABD

4.0 ELECTRICAL DESCRIPTION.

4.1 Input power requirements: +5 VDC ± 5% @ 200 Ma Max.

-12 VDC ± 10% @ 50 Ma Max.

4.2 Output signals:

4.2.1 TTL compatible signal.

4.2.1.1 The strobe, Bits 1 through 7, $\overleftarrow{\text{TAPE}}$ and $\overrightarrow{\text{TAPE}}$ provide TTL compatible signals with the following logic levels:

$$2.4v < \text{"1"} < 5.5v$$

$$0v < \text{"0"} < 0.4v$$

The strobe, $\overleftarrow{\text{TAPE}}$ and $\overrightarrow{\text{TAPE}}$ idle at logic "1" and change from logic "1" to "0" to "1" upon switch depression. Bits 1 through 7 follow the positive logic convention.

4.2.2 Non TTL compatible signals.

4.2.2.1 Stations 15, 16, 48 and 49 provide contact closures to ground when depressed.

4.3 Parity: NONE .

4.4 Strobe signal is delayed10 milliseconds nominal to allow data to stabilize.

4.5 Rollover:

Keyboard Specifications

4.4 Strobe signal is delayed10 milliseconds nominal to allow data to stabilize.

4.5 Rollover:

4.5.1 Two key rollover description. If a key is depressed before a previously operated key is released, the output code of that second key is transmitted after the first key is released.

4.6 Schematic diagram: ref. drawing no. 710107-E64.

4.7 Test Cable: ref. drawing no. 701106-E48.

4.8 Coding. Seven bit coding per Table II.

TABLE II (Column/Row Code)

STA.	US	U CASE	SHIFT	CONT
1	UPPER CASE			
2	3/1	3/1	2/1	---
3	3/2	3/2	2/2	---
4	3/3	3/3	2/3	---
5	3/4	3/4	2/4	---
6	3/5	3/5	2/5	---
7	3/6	3/6	2/6	---
8	3/7	3/7	2/7	---
9	3/8	3/8	2/8	---
10	3/9	3/9	2/9	---
11	3/0	3/0	---	---
12	2/13	2/13	3/13	---
13	5/14	5/14	7/14	1/14
14	5/12	5/12	7/12	1/12

STA.	US	U CASE	SHIFT	CONT
25	6/9	4/9	4/9	0/9
26	6/15	4/15	4/15	0/15
27	7/0	5/0	5/0	1/0
28	4/0	4/0	6/0	0/0
29	5/11	5/11	7/11	1/11
30	5/15	5/15	5/15	1/15
31	0/10	0/10	0/10	0/10
32	0/13	0/13	0/13	0/13
33	CTRL			
34	SHIFT LOCK			
35	6/1	4/1	4/1	0/1
36	7/3	5/3	5/3	1/3
37	6/4	4/4	4/4	0/4
38	6/6	4/6	4/6	0/6

12	2/13	2/13	3/13	---
13	5/14	5/14	7/14	1/14
14	5/12	5/12	7/12	1/12
15	HERE IS			
16	PAPER ADVANCE			
17	1/11	1/11	1/11	1/11
18	7/1	5/1	5/1	1/1
19	7/7	5/7	5/7	1/7
20	6/5	4/5	4/5	0/5
21	7/2	5/2	5/2	1/2
22	7/4	5/4	5/4	1/4
23	7/9	5/9	5/9	1/9
24	7/5	5/5	5/5	1/5

36	7/3	5/3	5/3	1/3
37	6/4	4/4	4/4	0/4
38	6/6	4/6	4/6	0/6
39	6/7	4/7	4/7	0/7
40	6/8	4/8	4/8	0/8
41	6/10	4/10	4/10	0/10
42	6/11	4/11	4/11	0/11
43	6/12	4/12	4/12	0/12
44	3/11	3/11	2/11	---
45	3/10	3/10	2/10	---
46	5/13	5/13	7/13	1/13
47	7/15	7/15	7/15	7/15
48	REPT			

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GENERAL INSTRUMENT company

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4.8 (cont'd)

STA.	US	U CASE	SHIFT	CONT
49	BREAK			
50	SHIFT			
51	7/10	5/10	5/10	1/10
52	7/8	5/8	5/8	1/8
53	6/3	4/3	4/3	0/3
54	7/6	5/6	5/6	1/6
55	6/2	4/2	4/2	0/2
56	6/14	4/14	4/14	0/14
57	6/13	4/13	4/13	0/13
58	2/12	2/12	3/12	---
59	2/14	2/14	3/14	---
60	2/15	2/15	3/15	---
61	SHIFT			

59	2/14	2/14	3/14	---
60	2/15	2/15	3/15	---
61	SHIFT			
62	TAPE ←			
63	TAPE →			
64	2/0	2/0	2/0	2/0

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a GENERAL INSTRUMENT company

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4.9 Pin assignments (card edge only, ref. 3.2). Reference Table III and Fig. A.

TABLE III

DATA CONNECTOR	
Pin	Function
1	BIT 6
2	Switch Connector Pin J
3	BIT 1
4	BIT 3
5	REPT
6	TAPE ←
7	TAPE →
8	GROUND
9	+5 VDC
10	-12 VDC
A	BIT 7
B	BIT 5
C	BIT 2
D	BIT 4
E	BREAK
F	Switch Connector Pin H
H	Strobe
J	HERE IS
K	PAPER ADV
L	800 HZ Clock

SWITCH CONNECTOR	
Pin	Function
1	X1
2	X2
3	X3
4	X4
5	X5
6	OPEN
7	GROUND
8	GROUND
A	Y1
B	Y2
C	Y3
D	Y4
E	OPEN
F	OPEN
H	Data Connector Pin F
J	Data Connector Pin 2

J	HERE IS
K	PAPER ADV
L	800 HZ Clock

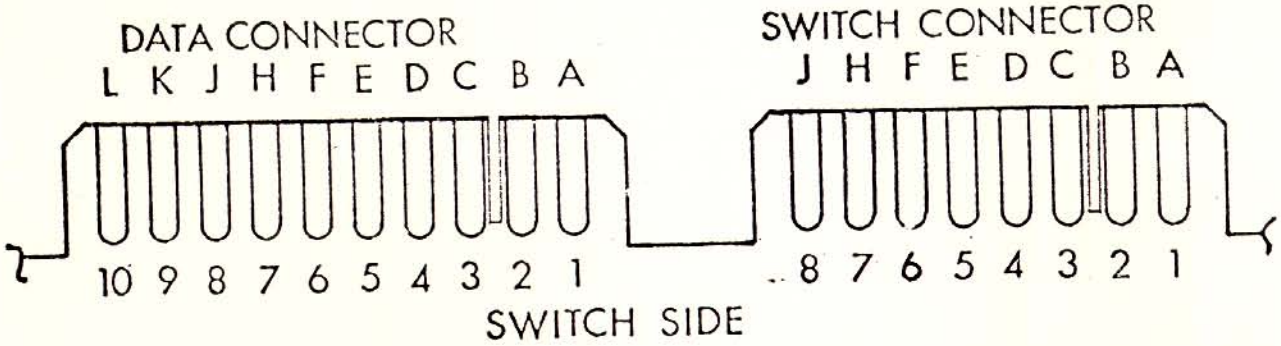

FIG. A

CLARE-PENDAR
A GENERAL INSTRUMENT COMPANY

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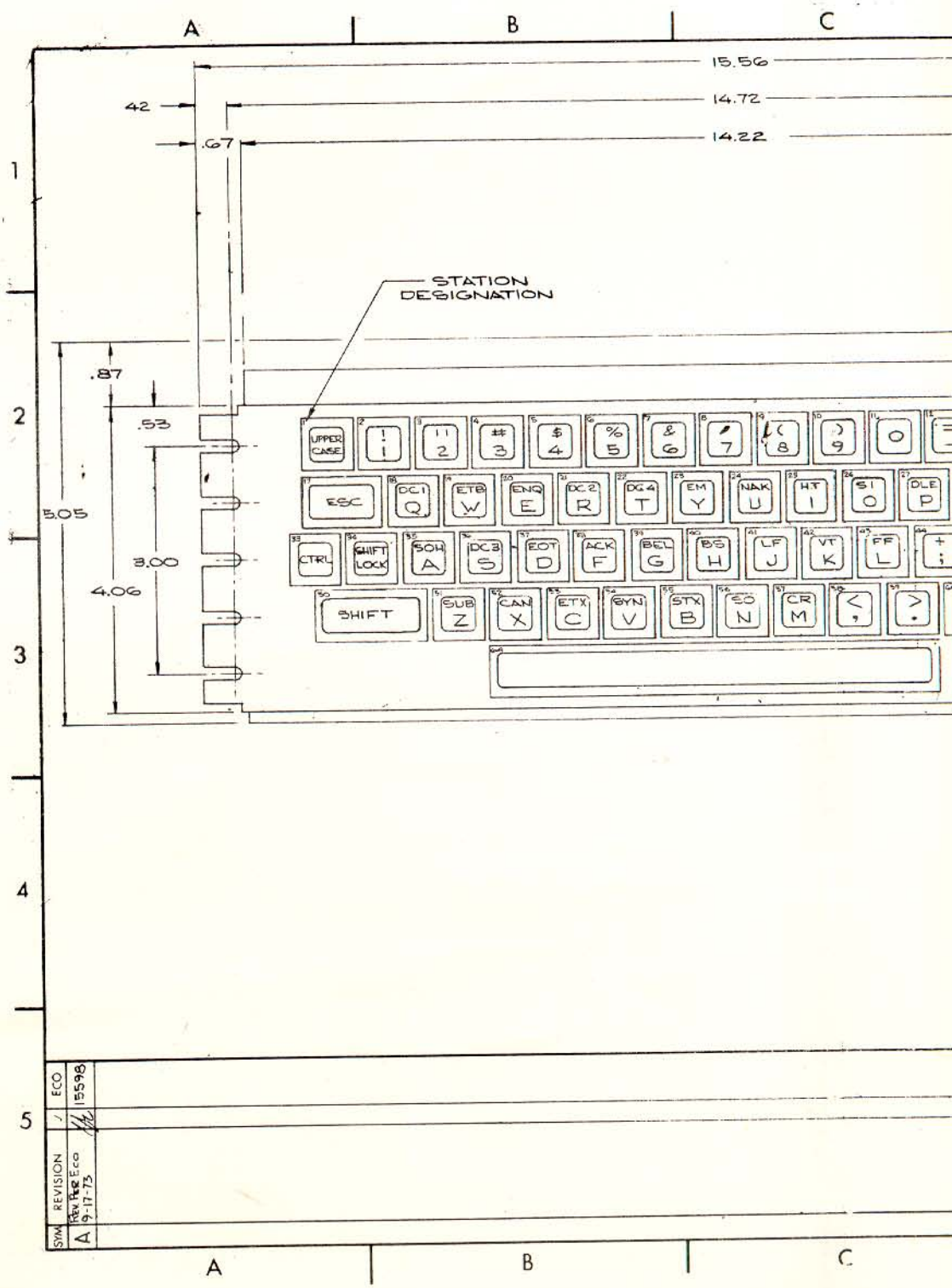
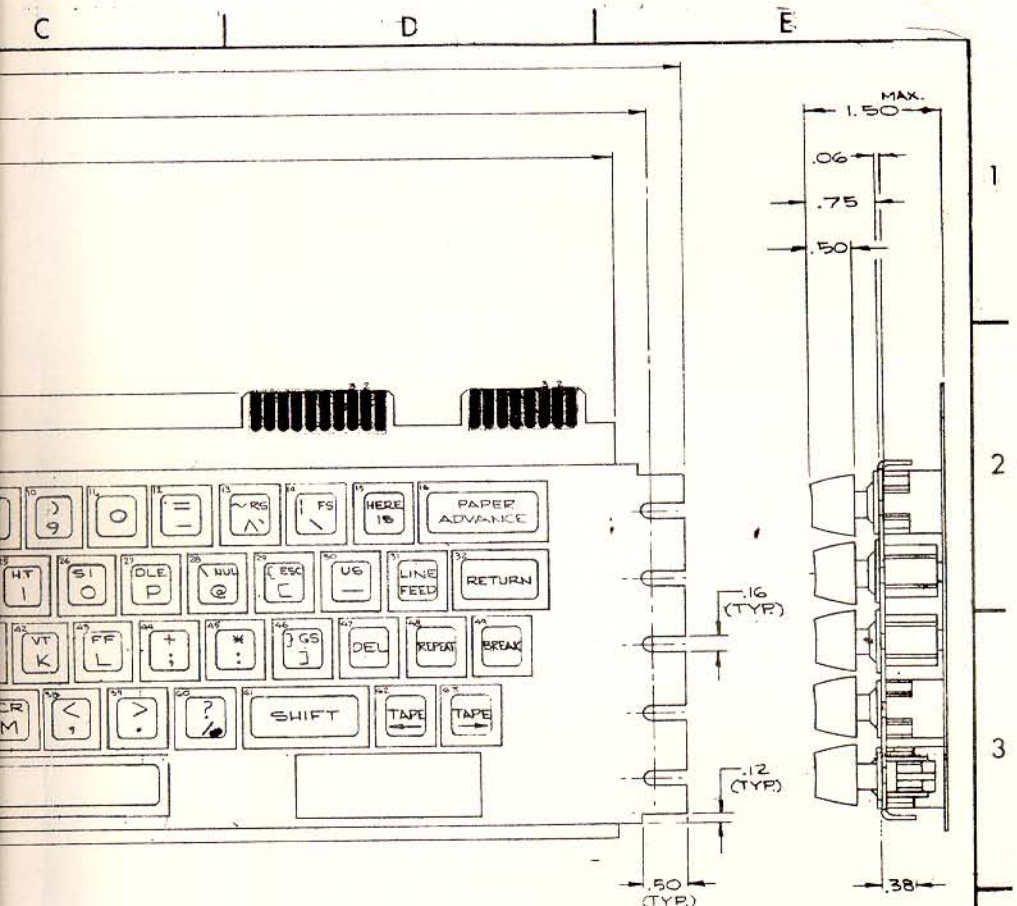
Page 6


A
B
C
15.56
14.72
14.22
.42
.67
STATION DESIGNATION
.87
.53
3.05
3.00
4.06
UPPER CASE
ESC
CTRL
SHIFT LOCK
SHIFT
SYM
REVISION
ECO
A
15598
9-17-73



TM 20K438 B/P1

SCALE FULL	ITEM	PART NO	DISCRIPTION	QTY
TOL EXCEPT AS NOTED XX ± .02 XXX ± .010 FRACT ± 1/32 ANG ± 0° 30' FINISH √	DWG Beckham 8-16-72 CHK Strickland 8/21/72 APP ENGLAR 8/21/72 APP [illegible] 8-22-72 CUST TEXAS INSTRUMENTS #4 NO 959326 EWO KEWO 4366	CLARE-PENDAR TITLE: KEYBOARD ASSY., 64 STA CODE [redacted] 97[redacted] DRAWING NUMBER 720731-K1 DO NO[redacted] WING		SHEET

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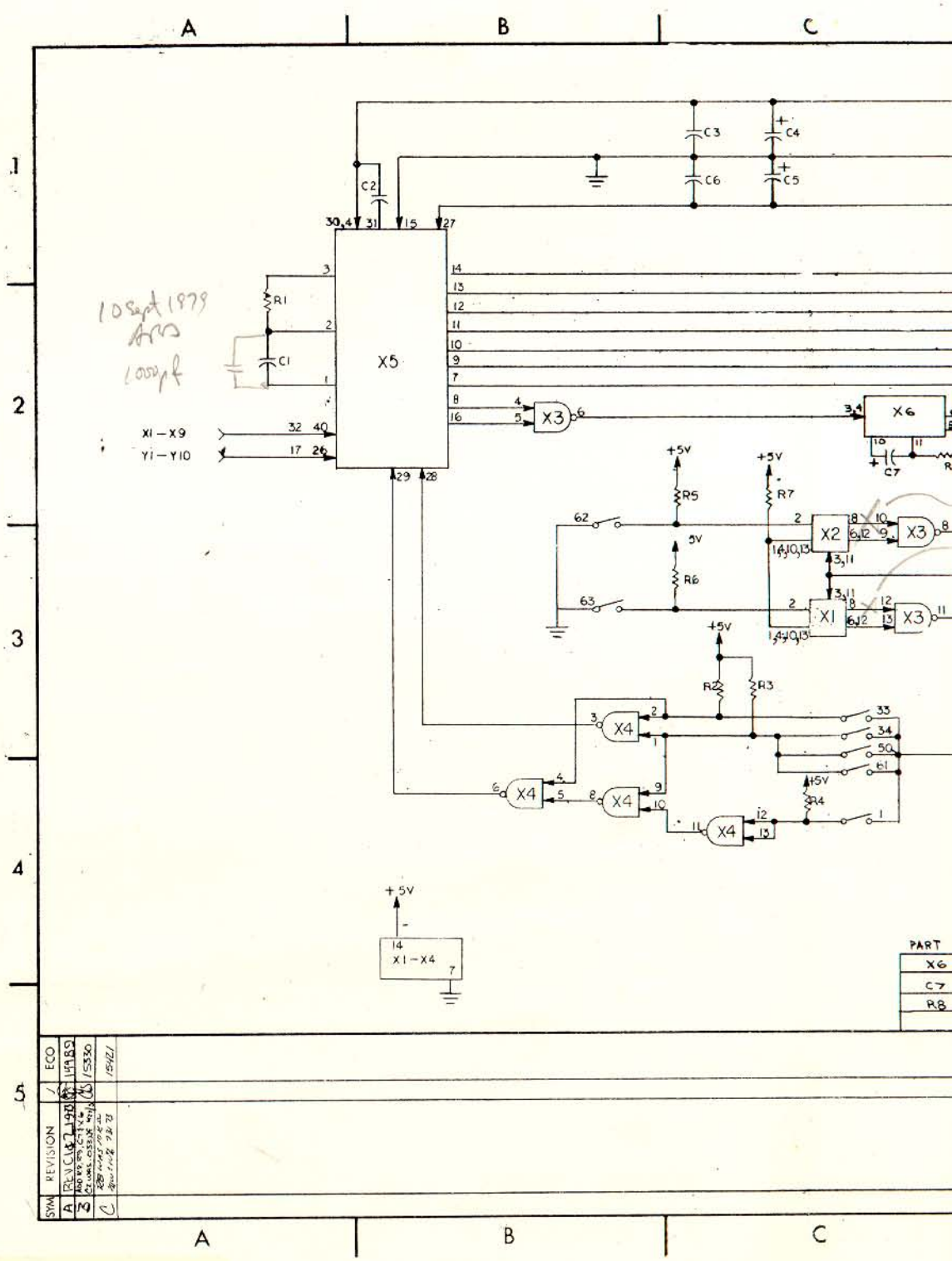
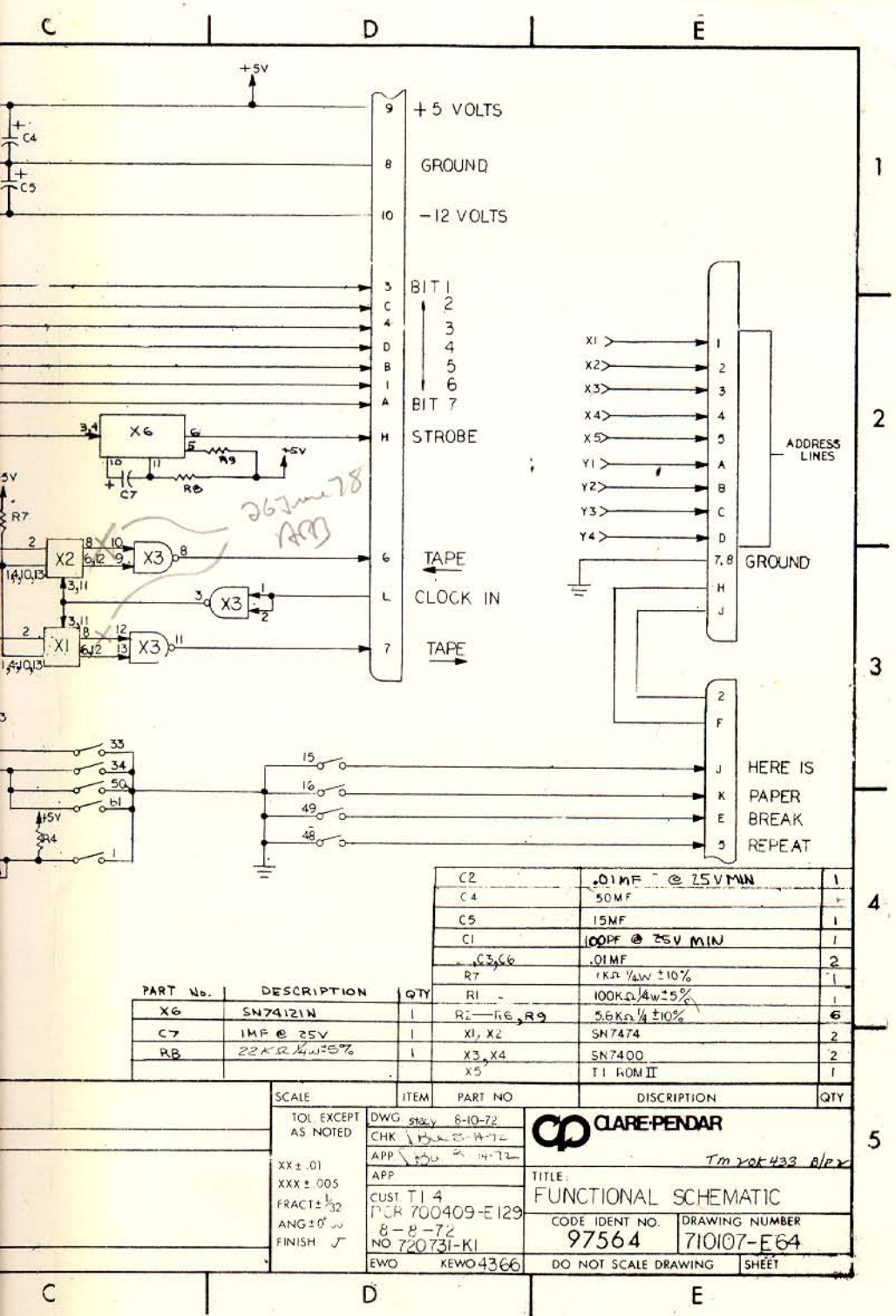

A
B
C
1
2
3
4
5
C3
C4
C6
C5
C2
30,4
31
15
27
R1
C1
X5
10 Sept 1979
ARS
1000pf
X1 – X9
Y1 – Y10
32
40
17
26
29
28
X3
X6
C7
+5V
R5
R7
62
63
5V
R6
X2
X1
R2
R3
X4
33
34
50
61
R4
X1 – X4
PART
X6
C7
R8
SYM
REVISION
ECO
A
B
C
15421



PART No.	DESCRIPTION	QTY
X6	SN74121N	1
C7	1MF @ 25V	1
R8	22KΩ ¼W ±5%	1

C2	.01MF @ 25V MIN	1
C4	50MF	1
C5	15MF	1
C1	100PF @ 35V MIN	1
C3,C6	.01MF	2
R7	1KΩ ½W ±10%	1
R1	100KΩ ¼W ±5%	1
R2—R6, R9	3.6KΩ ¼ ±10%	6
X1, X2	SN7474	2
X3, X4	SN7400	2
X5	TI ROM II	1

SCALE	ITEM	PART NO	DISCRIPTION	QTY

TOL EXCEPT AS NOTED
XX ± .01
XXX ± .005
FRACT ± 1/32
ANG ± 0° 30'
FINISH √

DWG stacy 8-10-72
CHK 8-14-72
APP 8-14-72
APP
CUST TI 4
PCR 700409-E129
8-8-72
NO 720731-K1
EWO KEWO4366

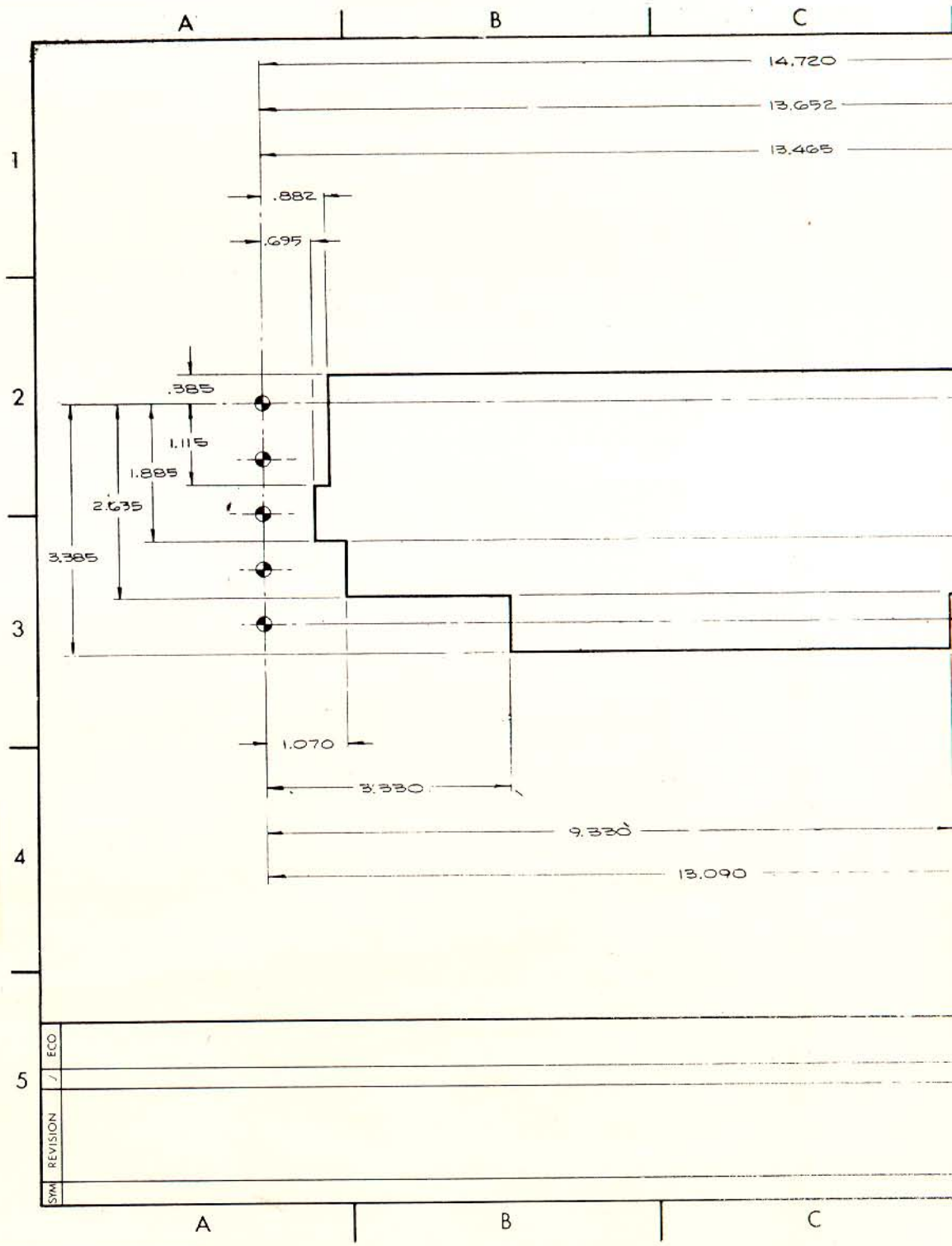
CLARE-PENDAR
Tm YOK 433 B/ex

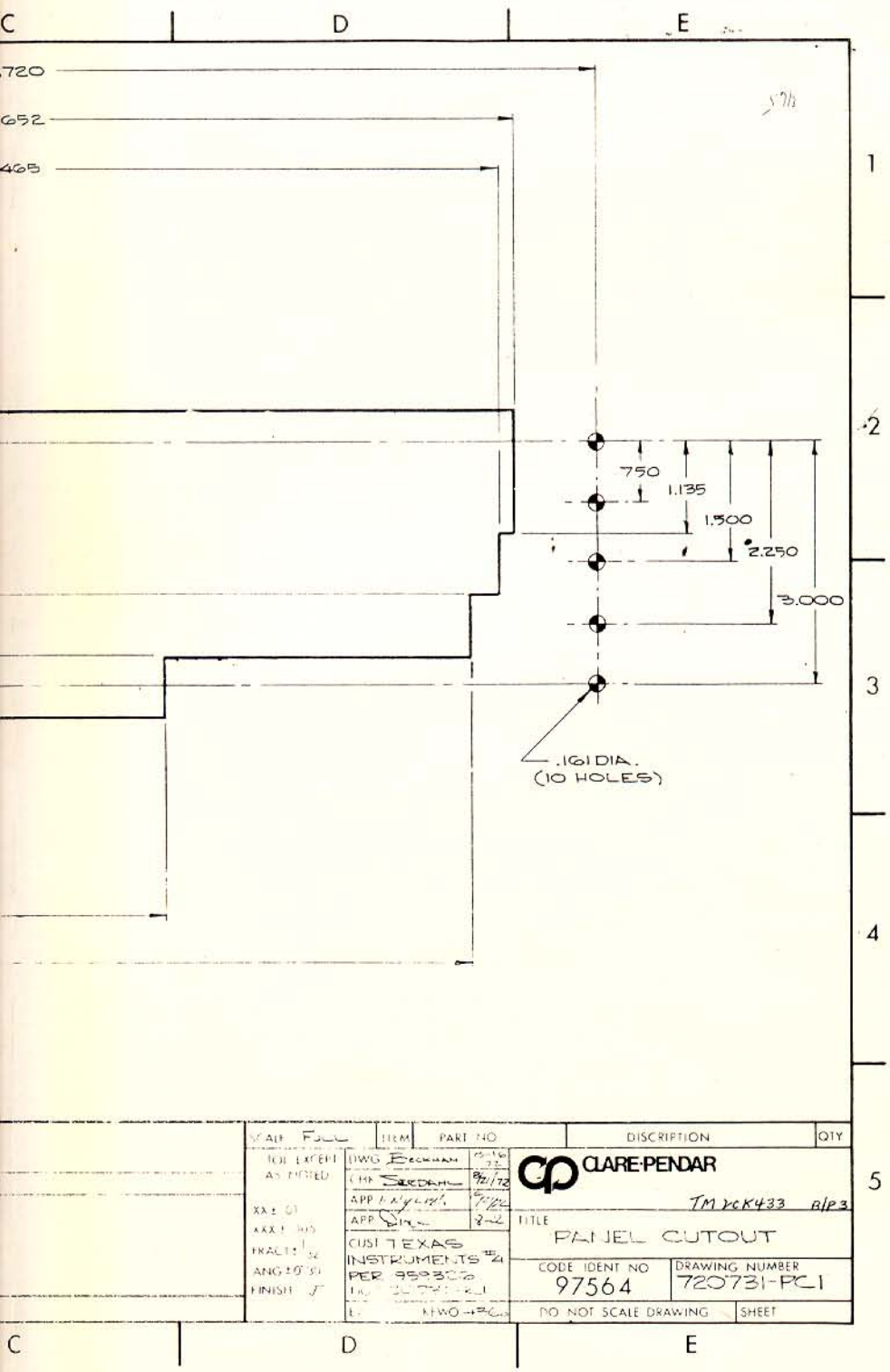
TITLE: FUNCTIONAL SCHEMATIC

CODE IDENT NO. 97564
DRAWING NUMBER 710107-E64

DO NOT SCALE DRAWING
SHEET

18F d 25
ARD


A
B
C
1
2
3
4
5
14.720
13.652
13.465
.882
.695
.385
1.115
1.885
2.635
3.385
1.070
3.330
9.330
13.090
SYM
REVISION
/
ECO



SCALE FULL	ITEM	PART NO	DISCRIPTION	QTY
TOL EXCEPT AS NOTED	DWG Beckman	8/11/72	CLARE-PENDAR	
XX ± .01	CHK Seedahl	8/11/72	TM YCK433 A/P3	
XXX ± .005	APP		TITLE PANEL CUTOUT	
FRACT ± 1/64	APP	8-2		
ANG ± 0° 30'	CUST TEXAS INSTRUMENTS INC PER 99330		CODE IDENT NO 97564	DRAWING NUMBER 720731-PC1
FINISH			DO NOT SCALE DRAWING	SHEET

18 Feb 78
ASD

36 pin interconnect Cable

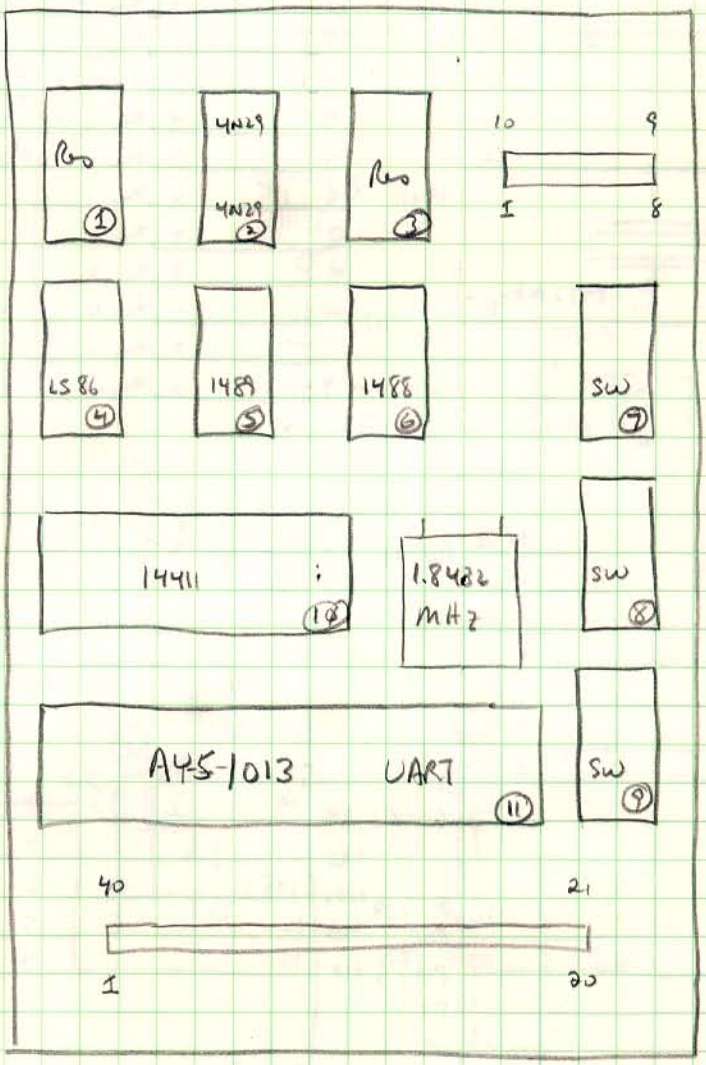
) signifies twisted pair

1	H0	BLUE)
2	H1	White)
3	H2	Green)
4	H3	Red)
5	H4	White)
6	H5	Red)
7	H6	ORANGE)
8	—	Black)
9	GND	Red/Blue
10	HSTROB	Black)
11	clock	White)
12	Repeat	Red)
13	Break	Yellow)
14	PAper	Red)
15	Here IS	Brown)
16	Tape →	Red)
17	Tape ←	Orange)
18	GND	Black / Green
19	GND	ORANGE)
20	P0	Green)
21	P1	Yellow)
22	P2	Black)
23	P3	Yellow)
24	P4	Black)
25	P5	Brown)
26	P6	Black)
27	P7	Red)
28	GND	Green)
29	PSTROBE	White)
30	SPHR	Green)
31	SPHR	Brown)
32	-12 V.	Green)
33	+5	Blue)
34	+5	Black)
35	+5	Blue)
36	+5	Green)

Printer Parallel Interface Cable

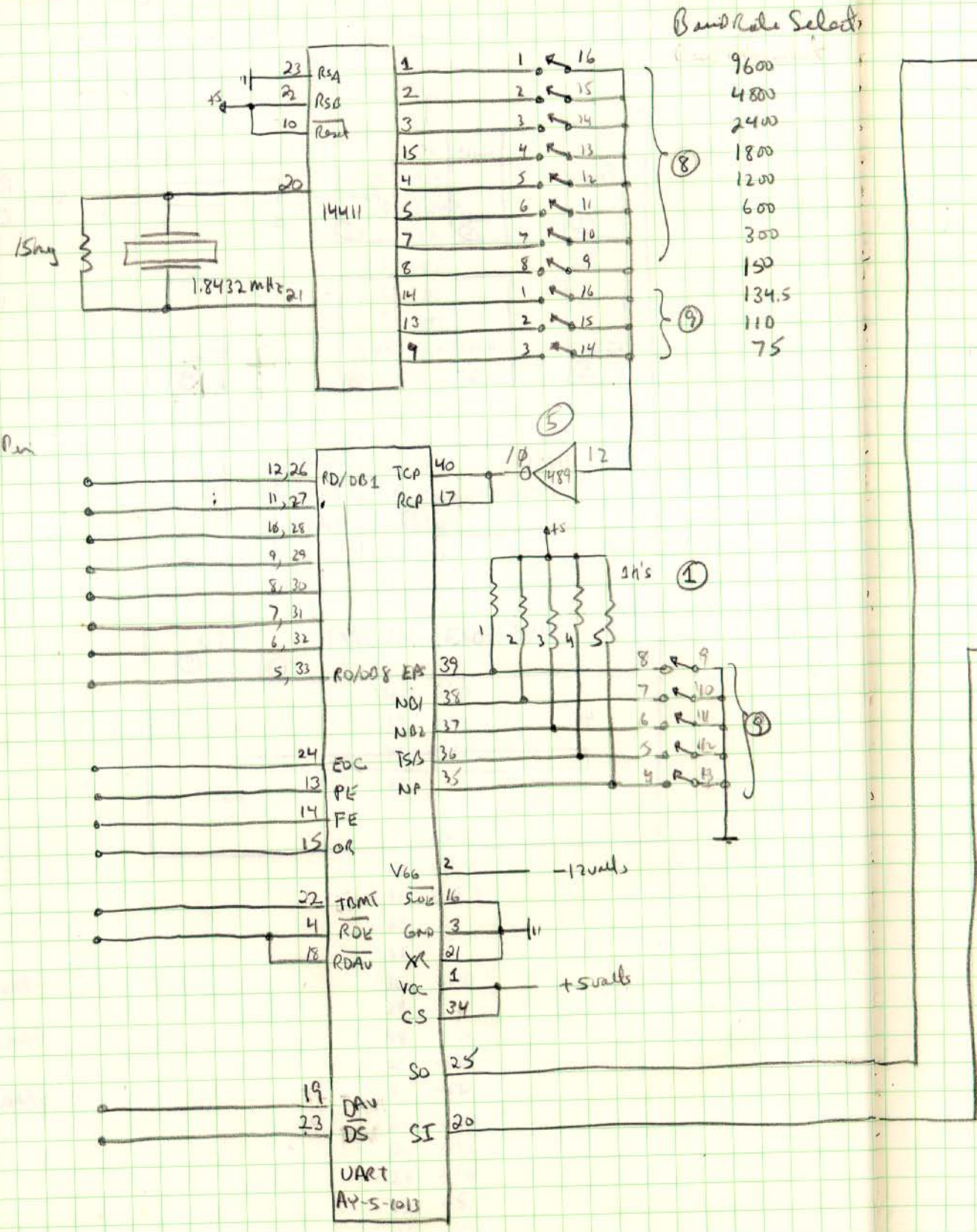
Cable		Board Pins	
1	D0	1	D0
2	D1	2	D1
3	D2	3	D2
4	D3	4	D3
5	D4	5	GND
6	D5	6	D4
7	D6	7	D5
8	D7	8	D6
9	GND	9	D7
10	C0	10	GND
11	C1	11	C0
12	C2	12	C1
13	C3	13	C2
14	C4	14	C3
15	C5	15	GND
16	C6	16	C4
17	C7	17	C5
18	GND	18	C6
		19	C7
19	GND	20	GND
20	CB1		
21	CB2	40	GND
22		39	CB1
23		38	CB2
24	CA1	37	
25	CA2	36	
26		35	GND
27	GND	34	CA1
28	GND	33	CA2
29		32	
30		31	
31	-12 volts	30	GND
32	-12	29	
33	+12 volts	28	
34	+12	27	-12
35	+5 volts	26	-12
36	+5	25	GND
		24	+12
		23	+12
		22	+5
		21	+5

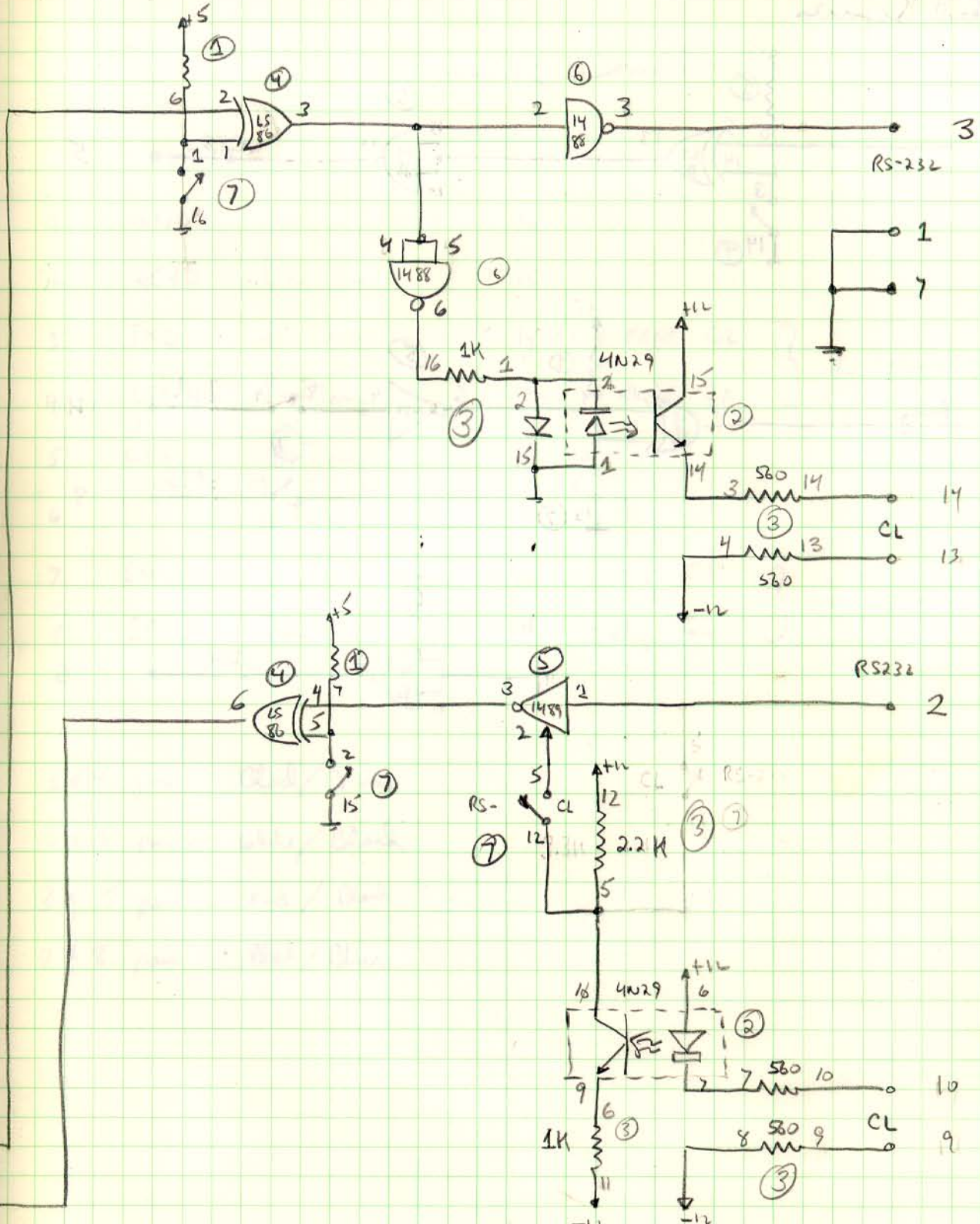
Parallel to Serial Board layout



10 Mar 79
ARD

Parallel to Serial logic




+5
LS 86
1488
1K
4N29
+12
-12
560
CL
RS-232
RS232
RS-
2.2K
3
14
13
10
9
2
1
7

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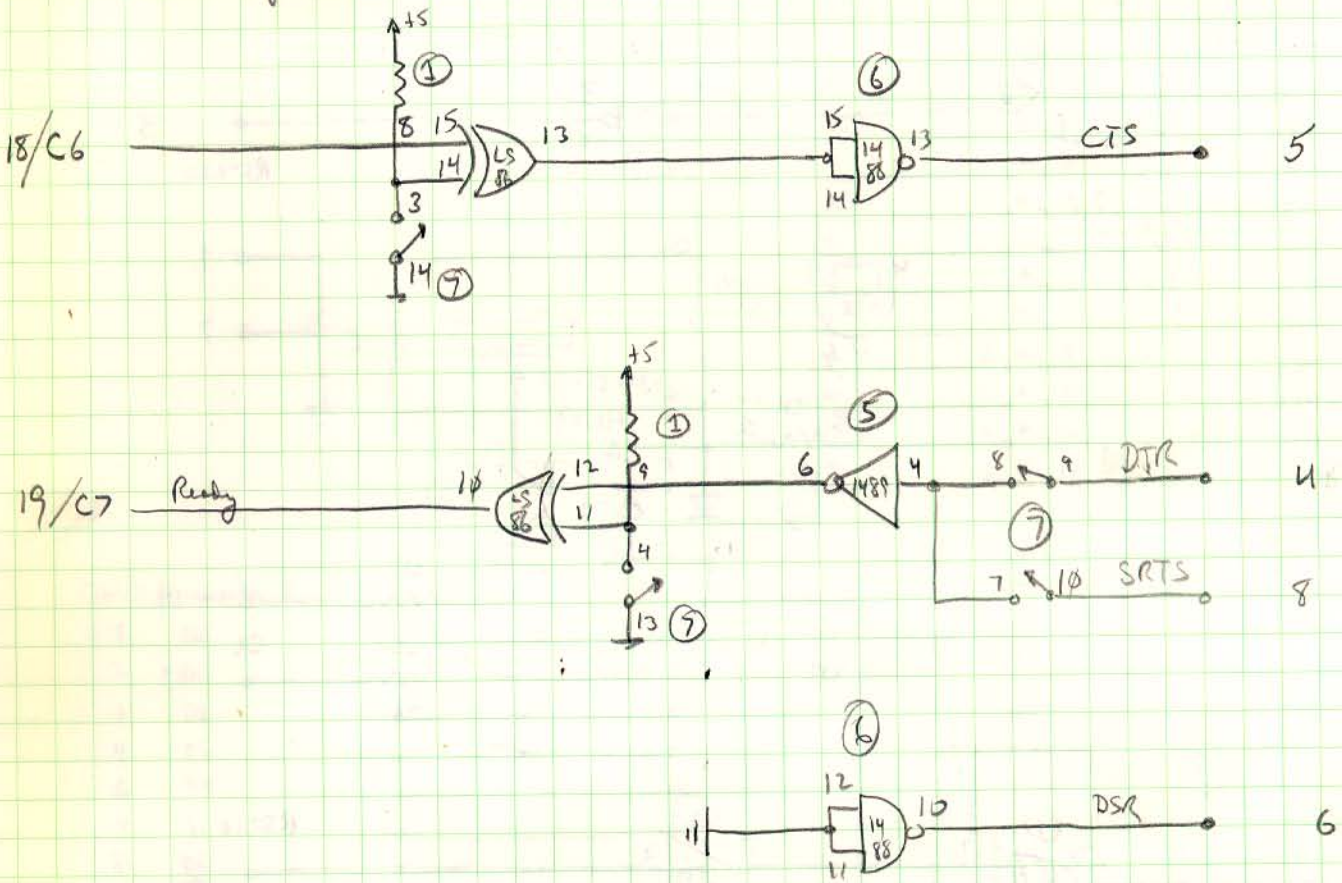
Control Signals



Terminal Connections

RS-232

1	GND		16		
2	RCVD	from Term	15		
3	TXD	to Term	14	+ PRNT CL	} to Terminal Printer
4	DTR	from Term	13	- PRNT CL	} to Terminal Printer
5	CTS	to Term	12		
6	DSR	to Term	11		
7	GND		10	+ Key CL	} from Terminal Keyboard
8	SRTS	from Term	9	- Key CL	} from Terminal Keyboard

1 & 4 pair Black / Green

2 & 6 pair White / Black

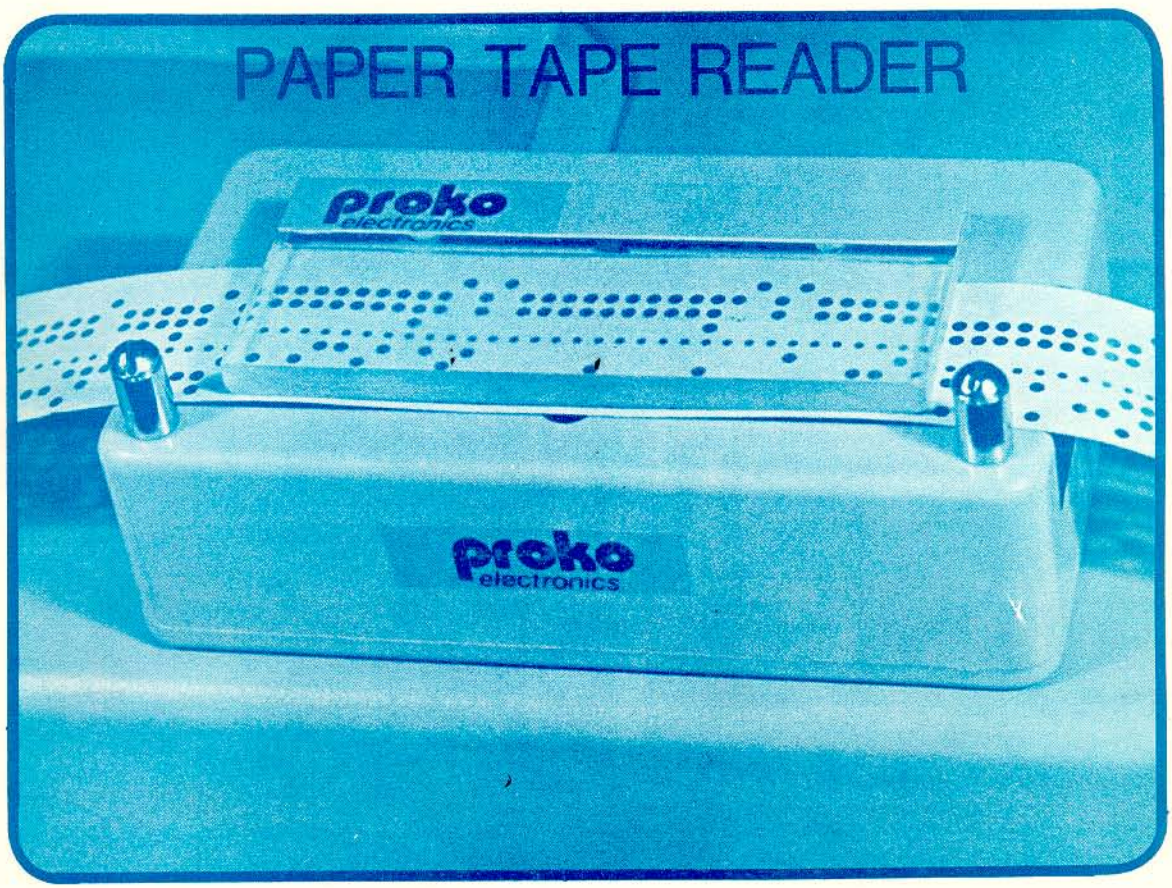
3 & 5 pair red / Black

7 & 8 pair Black / Blue

10 March 79
ARD

THE proko electronics PTR-II

PAPER TAPE READER



FEATURES

- LOW COST
- POCKET SIZE
- RELIABLE
- TTL COMPATABLE
- SIMPLE TO OPERATE
- TAPE CAN BE REMOVED FROM SIDE

USES

- BACK UP FOR DATA INPUT
- TROUBLE SHOOTING AID
- HOBBIEST INPUT DEVICE
- PAPER TAPE TO CASSETE
- SYSTEM BOOTSTRAP

 proko electronics "EMPIRICAL ENGINEERING"

INTRODUCTION

The new, high speed, low-cost paper tape reader from Proko Electronics means a more convenient and economical way to load commercially available programs. This unit has no moving parts, and can input data nearly as fast as you can pull it through. The PTR II is ideally suited for loading basic, assembler, monitors, etc., into your machine. This unit can interface to any computer with an eight-bit parallel input port. The paper tape can be removed or inserted from either end or from the side of the unit at any place in the tape.

Some fairly fancy mechanical assembly is required in this kit, the first place to look for missing bits is in poor optical allignment.

Read this manual carefully as you assemble the PTR II and refer to it if you encounter difficulties.

PARTS LIST

(1) ABS plastic enclosure

(1) acrylic lens piece

(1) 25-pin type D connector with pins

(1) P.C. Board

(8) R_1-R_8 Value determined by kit _____K

(1) R_9 Value determined by kit _____K

(1) R_{10} - 4.7K $\frac{1}{4}$W

(1) C1 - 0.01 or 0.005uf capacitor

(1) C2 - 18uf tantilum 10V capacitor

(1) 18-pin socket

(2) 14-pin socket

(1) 3 feet 12-conductor ribbon cable

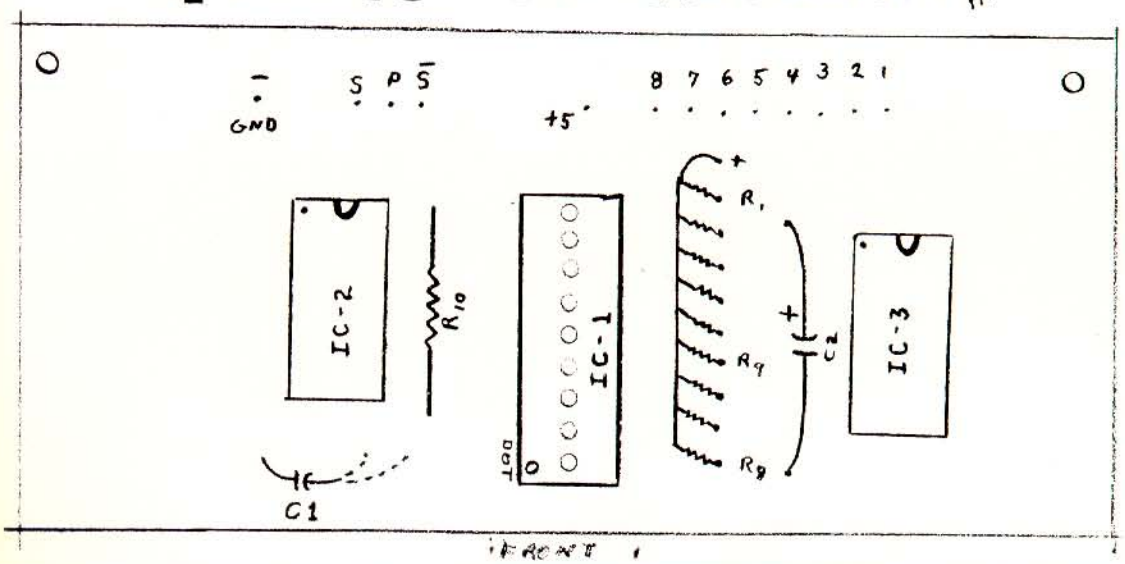
(1) IC-1 optical sensor array

(2) IC-2, IC-3 74LS14

(4) 4-40 machine screws

(2) 6-32 screws with washers

(2) spacers



-PRINTED CIRCUIT BOARD ASSEMBLY-

◇ Check kit contents against parts list.

◇ Insert two 14-pin and one 18-pin sockets into the component side of the board with the pin "1" index toward the upper left of the board. (The component side is the side on which there is no copper). Solder.
NOTE: Keep soldering tip clean to prevent rosin and sludge from being deposited on traces. Wipe tip frequently on a damp cloth.

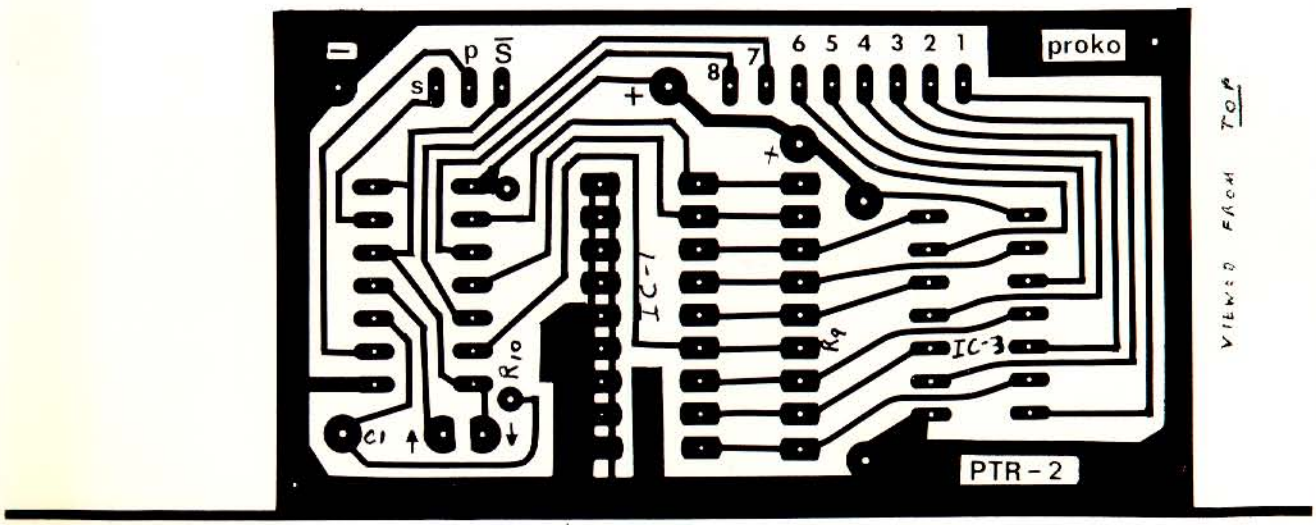
◇ Observing polarity, insert and solder the tantalum capacitor, C2.

◇ Insert and solder capacitor C1 and resistor R_{10}.

◇ Insert and solder resistors R_1 through R_9. Keep in mind R_9 is fourth from the front. These resistors stand vertically on the board and are soldered to a 5V bus wire

◇ Separate each conductor of the ribbon cable approximately $\frac{1}{2}$ inch.

proko electronics "EMPIRICAL ENGINEERING"



◇ With a pair of wire strippers, strip the insulation back 1/8th of an inch. Carefully tin each wire.

◇ Solder the first 11 wires of the ribbon cable to the PC board, omitting "S" and "$\overline{S}$".(Pads #1 thru #8, "P" ,"+" and "-")

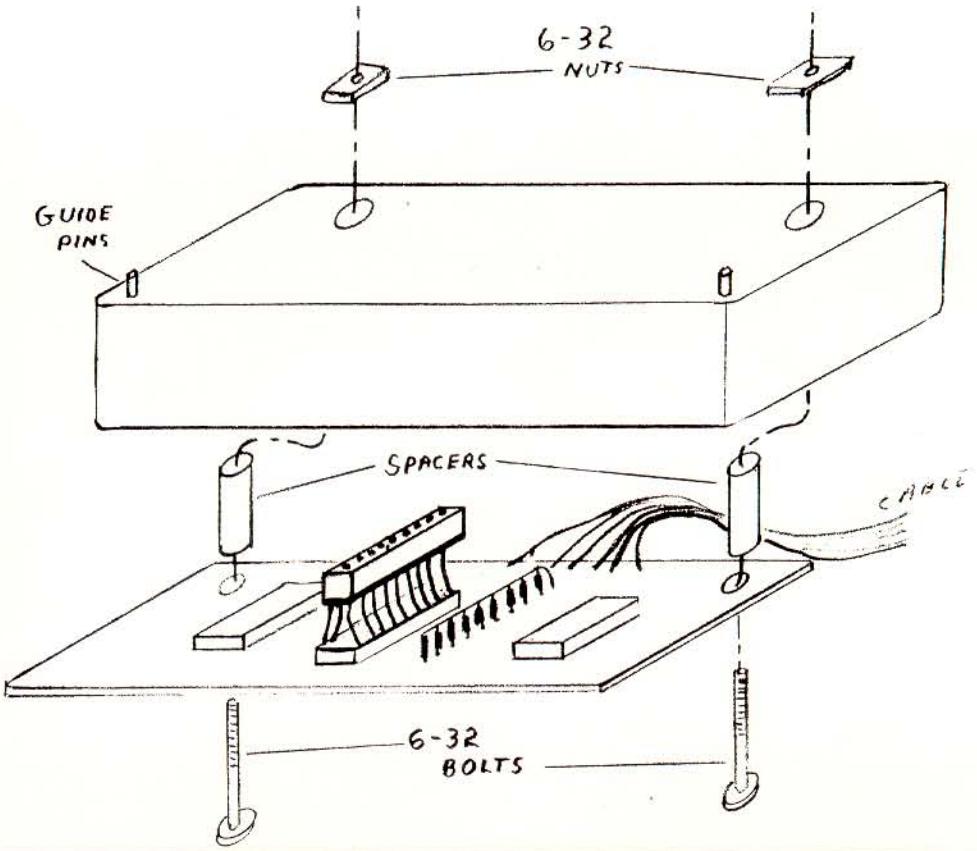
◇ Solder the remaining wire to the "$\overline{S}$" pad.

◇ Insert IC-2 and IC-3 with Pin 1 indexed toward the rear left.

◇ Insert IC-1 carefully bending the leads out so they properly allign with the IC socket.

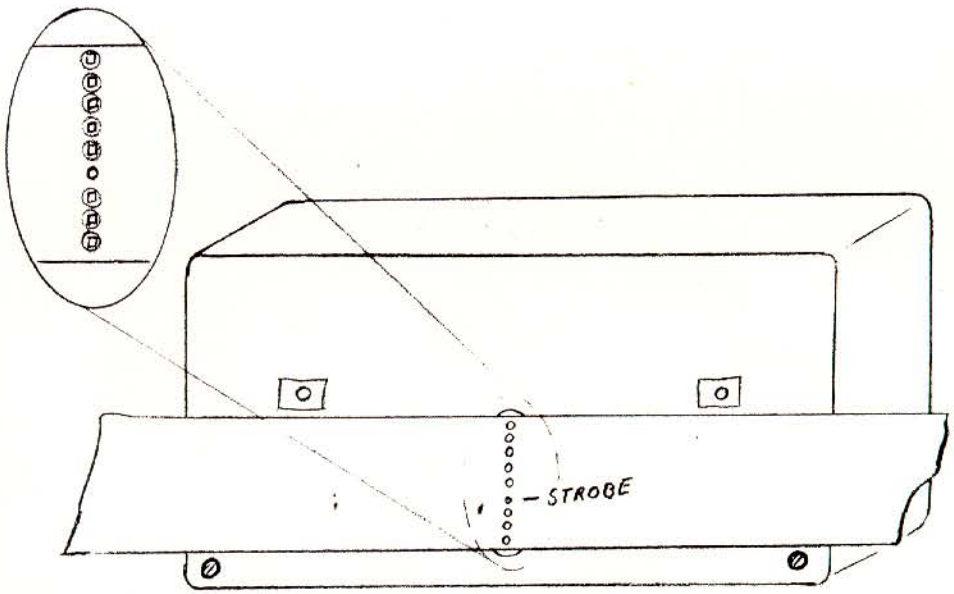
NOTE: The orientation of the optical sensor is important. Be sure the white spot is on the side away from resistors R_1- R_9.

◇ It will be helpful if you lift IC-1 slightly from it's socket. This will allow it to position itself during the mechanical assembly.(lift it only 1/16" or so)



MECHANICAL ASSEMBLY

- Work under a bright light.
- After P.C. board is assembled, install it in the PTR II housing without the acrylic lens piece, using, the two 6-32 nuts instead.
- With the readhead setting in the proper location, temporarily hold the black mask over the assembly and check for allignment with both the guide pins and the individual cells of the readhead. Loosen bolts and readjust if necessary.

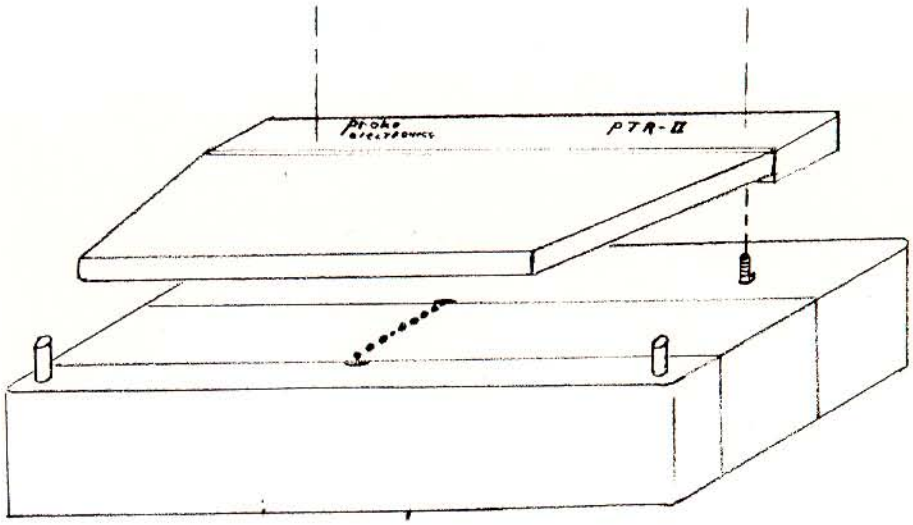


◇ When you are certain good allignment is possible, peel the backing from the mask and gently (without stretching) apply from the center out, and recheck for allignment.

◇ Tuck the ends of the mask inside of the box.

◇ It is a good idea at this point to try an actual piece of paper tape held over the black mask and over the readhead. Note that the strobe hole is smaller and nearer the bottom.

◇ If allignment seems difficult, it may be necessary to rebend the leads of the readhead or lift it slightly from its socket.



◇ Holding the bolts in place, remove the two 6-32 nuts and install the lens piece. Don't tighten bolts yet.

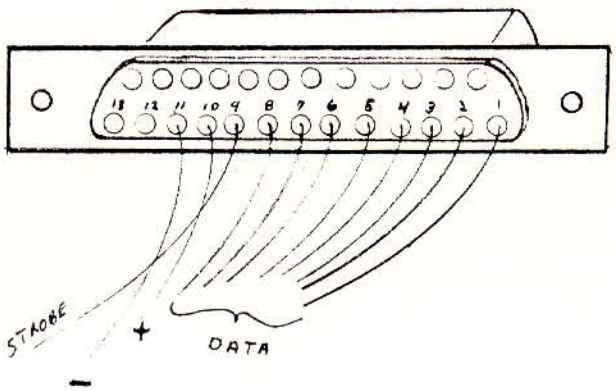
◇ Try the test tape again and position the lens piece for good allignment and free tape travel. Tighten the two bolts.

◇ Install the rear cover

* * * *

When unit is in use, dirt and dust may accumulate under the lens. For this reason, it is a good idea to periodically remove the lens piece and clean the mask with a damp cloth.

25 PIN "D" CONNECTOR



◇ If you are connecting the PTR II to an existing parallel port, you should wire the "D" connector to mate with that port (be sure to provide 5VDC). If not, the following connection can be made.

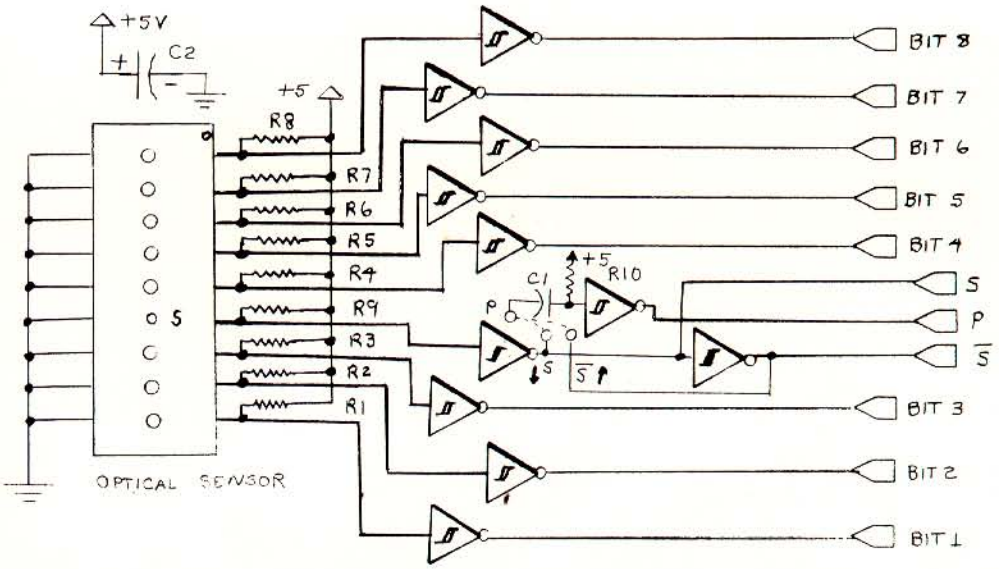
◇ Now you are ready to solder the 25-pin connector to the ribbon cable. It is suggested that Bit 1 be soldered to Pin 1 of the connector and Bit 2 to Pin 2, etc. Solder the pin to the wire first, then push the pins into the connector.

◇ Solder Pin 9 to the strobe of your choice.

See page 10

◇ Solder Pin 10 to plus 5V and Pin 11 to ground from the PTR II PC board (wires #10 & #11)

NOTE: The 5V supply must come from the I/O board to the PTR II, so provisions must be made to connect power to the PTR II.



The heart of the PTR-II is a precision 9-element silicon photo readhead. The elements of this optical sensor have been specially matched to greatly increase its reliability and reduce the circuitry.

Resistors R_1 through R_8 determine the sensitivity for each element. Resistor R_9 is larger to compensate for the reduced light from the strobe. The values for resistors R_1-R_9 are supplied to match the particular sensitivity of each readhead.

FINAL CHECK AND TROUBLE-SHOOTING

Your PTR II is now ready for testing.

Be certain the unit is clean and free of solder shorts. Most of the difficulties encountered with peripherals can be traced to software or a logical-hardware error. Be certain the input port is addressed correctly and that the strobe or status is used the way your software thinks it should be.

Make sure +5v and ground are properly connected to the I/O connector and I/O board.

There are four possible strobe outputs on the PTR II. They are:

1) strobe (a TTL level)
2) $\overline{\text{strobe}}$ "
3) pulse↑ (a short, negative pulse on the leading edge of the sprocket hole)
4) pulse↓ (as above but on the trailing edge)

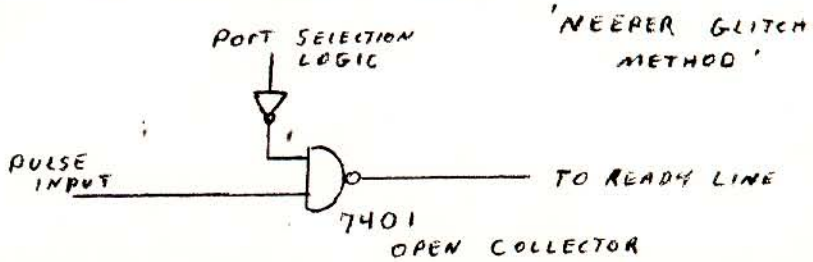
Most systems use $\overline{\text{strobe}}$.
The strobe and $\overline{\text{strobe}}$ outputs are brought to the edge of the PTR II P.C. board. The pulse is output on pad "P" (see Fig. 2). The direction and length of the pulse is determined by C1 and where it is placed. The larger its value the longer the pulse.

If the PTR II is to be used with an 8080 system, the following section may be some help.

Make sure +5V and ground are properly connected to the I/O connector and I/O card.

The first step in testing is to get the data displayed.

You might want to try the following method of input for the 8080. This modification would be wired from a spare nand gate on the I/O card.



When the port device is selected, the input strobe goes low causing the ready line to go low stopping the processor. The processor goes into a wait state. Only when a signal is applied to the pulse input does the processor run again.

Load and run the following program, where xx is the input port number.

```
0000    DBxx    LOOP: INPUT  PTRII     ; ACC=DATA
0002    2F            CMA
0003    D3FF          OUT              ;FRONT PANEL
0005    C30000        JMP    LOOP

    THIS ROUTINE DISPLAYS CONTINOUSLY, THE DATA

    FROM THE PTR II...
```

Obtain a test tape. Connect the modification shown above.

If you do not desire to use the "Neeper-Glitch" method, you can use a seperate port for status. The software would look something like this:

```
input   IN,   strobe
        CPI   2
        JNZ   input
        IN    DATA
        OUT   front panel
        JMP   input
```

If you do not own an IMSAI 8080, you can output to a terminal or perhaps some test lamps tied to an output port..

The light is somewhat critical. A small study lamp approximately 15W is best. For best results move the light closer to the sensor so all bits are on on the data bus lights. Now back off the lamp just until the bits with holes in the paper tape are on.
WARNING: With too strong a light and yellow paper tape, the light may go through the tape and cause error. Therefore, for best results and high reliability, the above test is recommended for each program loaded from yellow or light green tape.

If you should find that one or two bits refuse to change, try reversing IC-2 and IC-3.