

Internal / UNIBUS

Memory Agent / UNIBUS
MAP



53-110

Made in U.S.A.

Inler BUS Interface Internal BUS Buffer Logic
Power Distribution

3

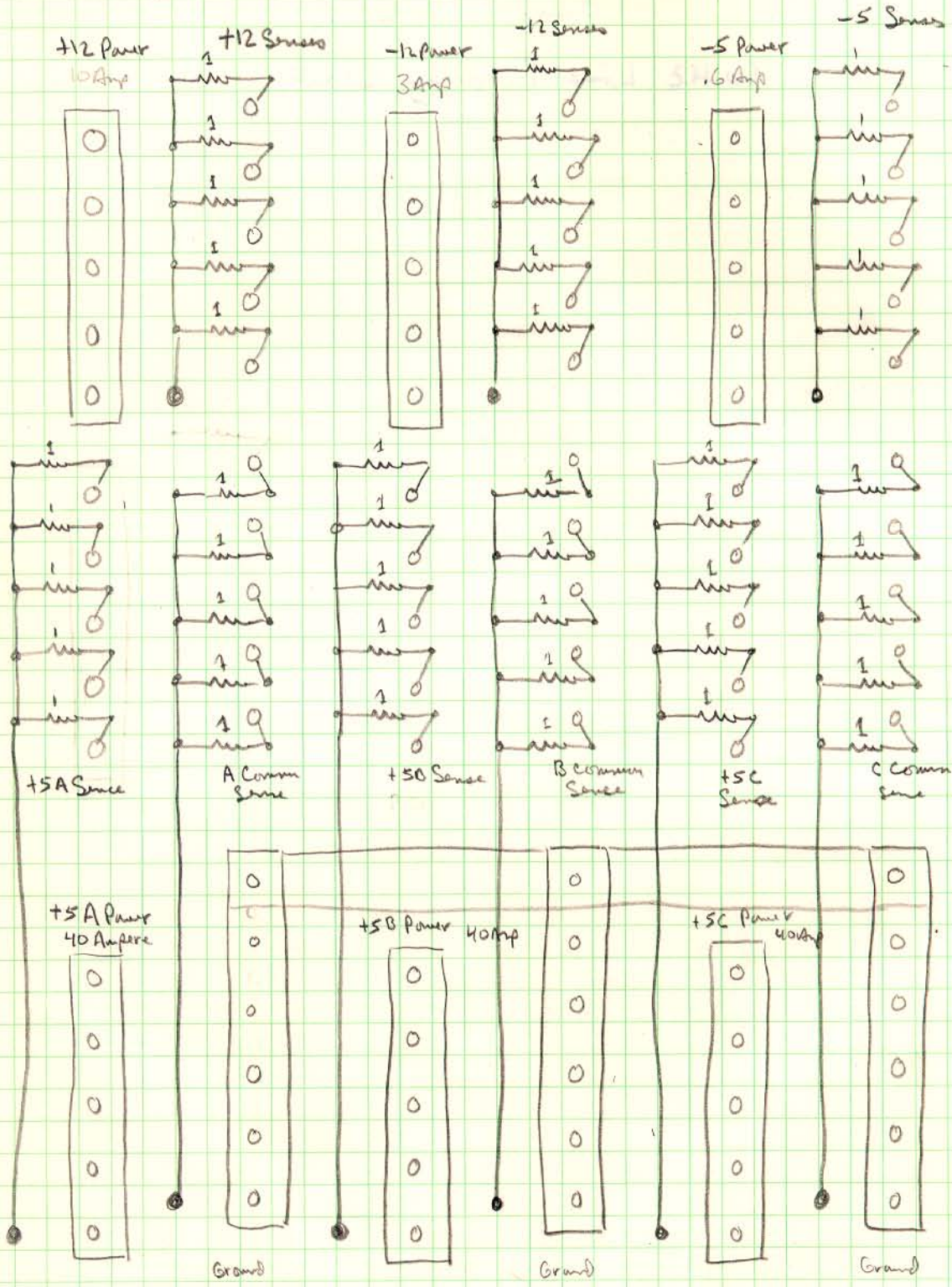
60 HZ Line Frequency Clock

23 April 77

Lower Half

[Front]

Power Distribution



23 April 77
ARD

CN6

Primary BUS Connector

← B

← A

S133	Con	CON	CON	CON	CON
28	8838	8838	8838	8838	8838
11	38	38	38	38	38
RES	175	175	175	175	175
S44	φ4	8838	8838	8838	8838
φ4	φ8	157	157	157	157
S139	φ8	157	157	157	157
S44	φ4	8838	8838	8838	8838
RES	175	175	175	175	175
11	38	38	38	38	38
S266	8838	8838	8838	8838	8838
S133	Term	Term	Term	Term	Term

← B

← A

CN7

Secondary BUS Connector

5
32
31
30
29
28
27
26
25
24
23
22
21
20
19
18
17

INTERNAL BUS

CN1 - Address + Control

1	$\overline{IA0}$	+	C21/1
2	$\overline{IA1}$	+	C21/4
3		+	C21/12
4		+	C21/15
5	GND		
6		+	B21/1
7		+	B21/4
8		+	B21/12
9		+	B21/15
10	GND		
11		+	A21/1
12		+	A21/4
13		+	A21/12
14		+	A21/15
15	GND		
16		+	C24/1
17		+	C24/4
18		+	C24/12
19	$\overline{IA15}$	+	C24/15
20	GND		

40	GND		
39	$\overline{IA16}$	+	B24/1
38	$\overline{IA17}$	+	B24/4
37	$\overline{IA18}$	+	B24/12
36	$\overline{IA19}$	+	B24/15
35	GND		
34	$\overline{IA24}$	+	A24/1
33	$\overline{IA21}$	+	A24/4
32	$\overline{IC0D}$	+	A24/12
31	$\overline{IC1D}$	+	A24/15
30	GND		
29	IXMSYNH	+	D21/4
28			
27	ISSYNL	+	A23/13
26	UASYNL	+	A23/13
25	GND		
24	IMSYNH	+	D21/1
23			
22			
21	IWITCLEAR H	+	B23/14

CN2 - Data

1	DIU	+	D23/3
2		+	D23/5
3		+	D23/7
4		+	D23/9
5	GND		
6		+	D23/11
7		+	D23/13
8		+	C23/3
9		+	C23/5
10	GND		
11		+	C23/7
12		+	C23/9
13		+	C23/11
14		+	C23/13
15	GND		
16		+	B23/3
17		+	B23/5
18		+	B23/7
19	DEIS	+	B23/9
20	GND		

40	GND		
39	$\overline{DO0}$	+	D22/1
38		+	D22/4
37		+	D22/12
36		+	D22/15
35	GND		
34		+	C22/1
33		+	C22/4
32		+	C22/12
31		+	C22/15
30	GND		
29		+	B22/1
28		+	B22/4
27		+	B22/12
26		+	B22/15
25	GND		
24		+	A22/1
23		+	A22/4
22		+	A22/12
21	$\overline{DO15}$	+	A22/15

CN3 - Control

1	BR4	+	J30/10	40	GND		
2	BR5	+	J30/11	39	B64	+	L30/9
3	BR6	+	J30/6	38	B65	+	H30/9
4	BR7	+	J30/5	37	B66	+	J30/9
5	GND			36	B67	+	I30/9
6	NPR	+	D30/13	35	GND		
7				34	NPG	+	E31/15
8				33	60 Hz Clock	+	C28/3
9	INIT	+	L30/5 + E31/1	32	LINEFRM CLOCK INIT	+	B26/1
10	GND			31	Line Frag. Clock Clear	+	C26/1
11	ACLO	+	A32/11	30	GND		
12	DCLO	+	A31/11	29	INTR	+	L30/6
13	Power Fail L	-		28	SACK	+	E27/3
14	BSSYN	+	H28/13	27	PB0	+	H30/5
15	GND			26	PB1	+	H30/6
16	Bmsyn	+	E27/6	25	GND		
17				24	C0L	+	H29/12
18				23	C1L	+	H29/15
19	BOSY	+	E27/13	22	A16L	+	H29/1
20	GND			21	A17L	+	H29/4

CN4 - Data & Address

1	D0L	+	L30/15	40	GND		
2	D1L	+	L30/14	39	A0L	+	L29/1
3		+	L30/13	38	A1L	+	L29/4
4		+	L30/12	37		+	L29/12
5	GND			36		+	L29/15
6		+	J30/15	35	GND		
7		+	J30/14	34		+	J29/1
8		+	J30/13	33		+	J29/4
9		+	J30/12	32		+	J29/12
10	GND			31		+	J29/15
11		+	H30/15	30	GND		
12		+	H30/14	29		+	H29/1
13		+	H30/13	28		+	H29/4
14		+	H30/12	27		+	H29/12
15	GND			26		+	H29/15
16		+	I30/15	25	GND		
17		+	I30/14	24		+	I29/1
18		+	I30/13	23		+	I29/4
19	DISL	+	I30/12	22		+	I29/12
20	GND			21	AISL	+	I29/15

23 April 77
ARS

INTERNAL BUS Connector

CNS

A				B			
A1	GND	+	D23/8	A1	GND	+	B21/8
A2		+	D23/2	A2	IA0	+	C21/3
B1	DI0	+	D23/4	B1		+	C21/6
B2		+	D23/6	B2		+	C21/10
C1		+	D23/10	C1		+	C21/13
C2		+	D23/12	C2		+	B21/3
D1		+	D23/14	D1	IAS	+	B21/6
D2		+	C23/2	D2	GND	+	C21/8
E1		+	C23/4	E1	IAG	+	B21/10
E2		+	C23/6	E2		+	B21/13
F1		+	C23/14	F1		+	A21/3
F2		+	C23/12	F2		+	A21/6
H1		+	C23/14	H1		+	A21/10
H2		+	B23/2	H2	IA11	+	A21/13
J1		+	B23/4	J1	GND	+	A21/8
J2		+	B23/6	J2	IA12	+	C24/3
K1	DI15	+	B23/10	K1		+	C24/6
K2	GND	+	B23/8	K2		+	C24/10
L1	GND	+	D22/8	L1		+	C24/13
L2	DO0	+	D22/3	L2		+	B24/3
M1		+	D22/6	M1	IA17	+	B24/6
M2		+	D22/14	M2	GND	+	C24/8
N1		+	D22/13	N1	IA18	+	B24/14
N2		+	C22/3	N2		+	B24/13
P1		+	C22/6	P1		+	A24/3
P2		+	C22/10	P2	IA21	+	A24/6
R1		+	C22/13	R1	IC0D	+	A24/14
R2		+	B22/3	R2	IC1D	+	A24/13
S1		+	B22/6	S1	GND	+	B24/8
S2		+	B22/14	S2	IXMSYN	+	D21/6
T1		+	B22/13	T1	INTERLOCK [L]	+	D21/15
T2		+	A22/3	T2	IMSYN	+	D21/3
U1		+	A22/6	U1	GND	+	A21/8
U2		+	A22/10	U2	ISSYNL	+	A23/14
V1	DO15	+	A22/13	V1	UBSYNL	+	A23/2
V2	GND	+	D22/8	V2	INIT CLEAN L	+	B23/13

Primary UniBus Connector (DEC Compatible)

CWL

A	A 1	PINIT L	+	L34/5
	A 2	+5 Volts	+	L34/16
	B 1	PINTR L	+	L34/6
	B 2	GND	+	L34/8
	C 1	PD00L	+	L34/15
	C 2	GND	+	L34/8
	D 1	PD02L	+	L34/13
	D 2	PD02L	+	L34/14
	E 1	PD04L	+	J34/15
	E 2	PD03L	+	L34/12
	F 1	PD06L	+	J34/13
	F 2	PD05L	+	J34/14
	H 1	PD08L	+	K34/15
	H 2	PD07L	+	J34/12
	J 1	PD10L	+	K34/13
	J 2	PD09L	+	K34/14
	M 1	PD12L	+	I34/15
	M 2	PD11L	+	K34/12
	L 1	PD14L	+	I34/13
	L 2	PD13L	+	I34/14
	M 1	P PAL	+	K134/5
	M 2	PD15L	+	I34/12
	N 1	GND	+	K34/8
	N 2	P PBL	+	K34/6
	P 1	GND	+	J34/8
	P 2	P RBSYL	+	H34/6
	R 1	GND	+	K34/8
	R 2	PSACK L	+	H34/14
	S 1	GND	+	I34/8
	S 2	P N PRL	+	I34/6
	T 1	GND	+	J34/8
	T 2	P BR7L	+	J34/5
	U 1	P N P0H	+	H34/9
	U 2	P BR6L	+	J34/6
	V 1	P BG7H	+	I34/9
	V 2	GND	+	I34/8

B	A 1	PBG6H	+	J34/9
	A 2	+5 Volts	+	J34/16
	B 1	PBG5H	+	K34/9
	B 2	GND	+	H34/8
	C 1	P BR5L	+	J34/11
	C 2	GND	+	H34/8
	D 1	GND	+	G34/8
	D 2	P BR4L	+	J34/10
	E 1	GND	+	G34/8
	E 2	PBG4L	+	L34/9
	F 1	PACL0L	+	I34/11
	F 2	P DCL0L	+	I34/10
	H 1	PA01L	+	L34/2
	H 2	PA04L	+	L34/11
	J 1	PA03L	+	L34/3
	J 2	PA02L	+	L34/4
	H 1	PA05L	+	J34/2
	H 2	PA04L	+	J34/1
	L 1	PA07L	+	J34/4
	L 2	PA06L	+	J34/3
	M 1	PA09L	+	K34/2
	M 2	PA08L	+	K34/1
	N 1	PA11L	+	K34/14
	N 2	PA10L	+	K34/3
	P 1	PA13L	+	I34/2
	P 2	PA12L	+	I34/1
	R 1	PA15L	+	I34/4
	R 2	PA14L	+	I34/3
	S 1	PA17L	+	H34/2
	S 2	PA16L	+	H34/1
	T 1	GND	+	G34/8
	T 2	PCI L	+	H34/4
	U 1	PSSYNL	+	H34/12
	U 2	PC0L	+	H34/3
	V 1	PMSYNL	-	H34/14
	V 2	GND	+	H34/8

A

Secondary Units Connector (DEC Compatible)

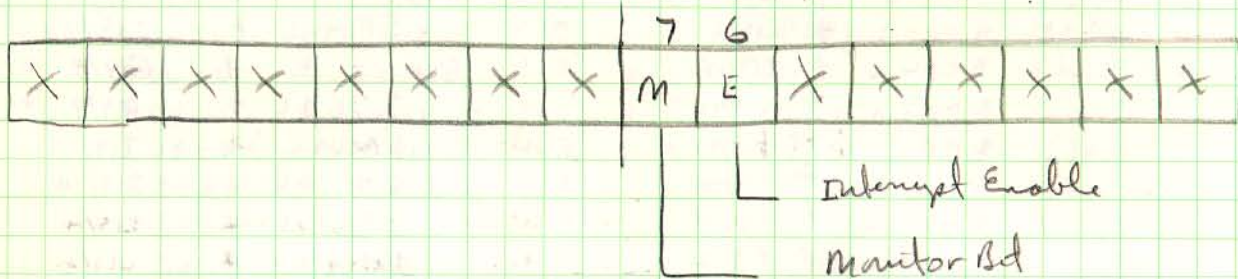
A				B			
A 1		SINIL L	+ L19/5	A 1		S B G 6 H	+ J19/9
A 2		NC		A 2		NC	
B 1		S INTR L	+ L19/6	B 1		S B G 5 H	+ K19/9
B 2	GND		+ L19/8	B 2	GND		+ H19/8
C 1		S D 0 0 L	+ L19/15	C 1		S B R 5 L	+ J19/11
C 2	GND		+ L19/8	C 2	GND		+ H19/8
D 1		S D 0 2 L	+ L19/13	D 1	GND		+ H19/8
D 2		S D 0 1 L	+ L19/14	D 2		S B R 4 L	+ J19/10
E 1		S D 0 4 L	+ J19/15	E 1	GND		+ G19/8
E 2		S D 0 3 L	+ L19/12	E 2		S B G 4 L	+ L19/9
F 1		S D 0 6 L	+ J19/13	F 1		S A C 0 L	+ I19/11
F 2		S D 0 5 L	+ J19/14	F 2		S D C 0 L	+ I19/10
H 1		S D 0 8 L	+ K19/15	H 1		S A 0 1 L	+ L19/12
H 2		S D 0 7 L	+ J19/12	H 2		S A 0 0 L	+ L19/11
J 1		S D 1 0 L	+ K19/13	J 1		S A 0 3 L	+ L19/14
J 2		S D 0 9 L	+ K19/14	J 2		S A 0 2 L	+ L19/13
K 1		S D 1 2 L	+ I19/15	K 1		S A 0 5 L	+ J19/12
K 2		S D 1 1 L	+ K19/12	K 2		S A 0 4 L	+ J19/11
L 1		S D 1 4 L	+ I19/13	L 1		S A 0 7 L	+ J19/14
L 2		S D 1 3 L	+ I19/14	L 2		S A 0 6 L	+ J19/13
M 1		S P A L	+ K19/15	M 1		S A 0 9 L	+ K19/12
M 2		S D 1 5 L	+ I19/12	M 2		S A 0 8 L	+ K19/11
N 1	GND		+ K19/8	N 1		S A 1 1 L	+ K19/14
N 2		S P B L	+ K19/6	N 2		S A 1 0 L	+ K19/13
P 1	GND		+ K19/8	P 1		S A 1 3 L	+ I19/12
P 2		S B B 5 L	+ H19/6	P 2		S A 1 2 L	+ I19/11
R 1	GND		+ J19/8	R 1		S A 1 5 L	+ I19/14
R 2		S S A C H L	+ H19/10	R 2		S A 1 4 L	+ I19/13
S 1	GND		+ J19/8	S 1		S A 1 7 L	+ H19/12
S 2		S N P R L	+ I19/6	S 2		S A 1 6 L	+ H19/11
T 1	GND		+ I19/8	T 1	GND		+ G19/8
T 2		S B R 7 L	+ J19/5	T 2		S C 1 L	+ H19/14
U 1		S N P 0 H	+ H19/9	U 1		S S S Y N L	+ H19/12
U 2		S R R 6 L	+ J19/6	U 2		S C 0 L	+ H19/13
V 1		S B G 7 H	+ I19/9	V 1		S M S Y N L	+ H19/14
V 2	GND		+ I19/8	V 2	GND		+ G19/8

23 April 77
ARR

60 Hz line Frequency Clock

Clock Address

777546



Bit 7 set by 'tick' of line frequency or INIT
cleared by program

Bit 6 interrupt enable bit set/cleared by program
access, cleared by INIT

if Bits 6 & 7 are set then an interrupt
will occur at level 6

a CPU priority of 6 or higher inhibits
interrupt

777100

777102

777104

777106

The Secondary BUS Interface Allows two independent processors to access any location on the other's UNIBUS -

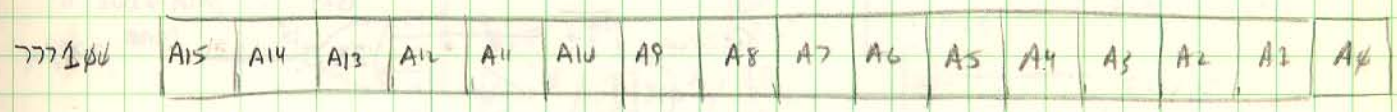
Each processor has a peripheral located at 77710X which allows interbus communication by NPR accesses to the other BUS

777100 - Control Register 0

Read/Write - lower sixteen bits of the word/byte address

777102 - Control Register 1

Read/write - two bit address extension plus a flag (read only) indicating if Read or Write attempted by NPR was successful



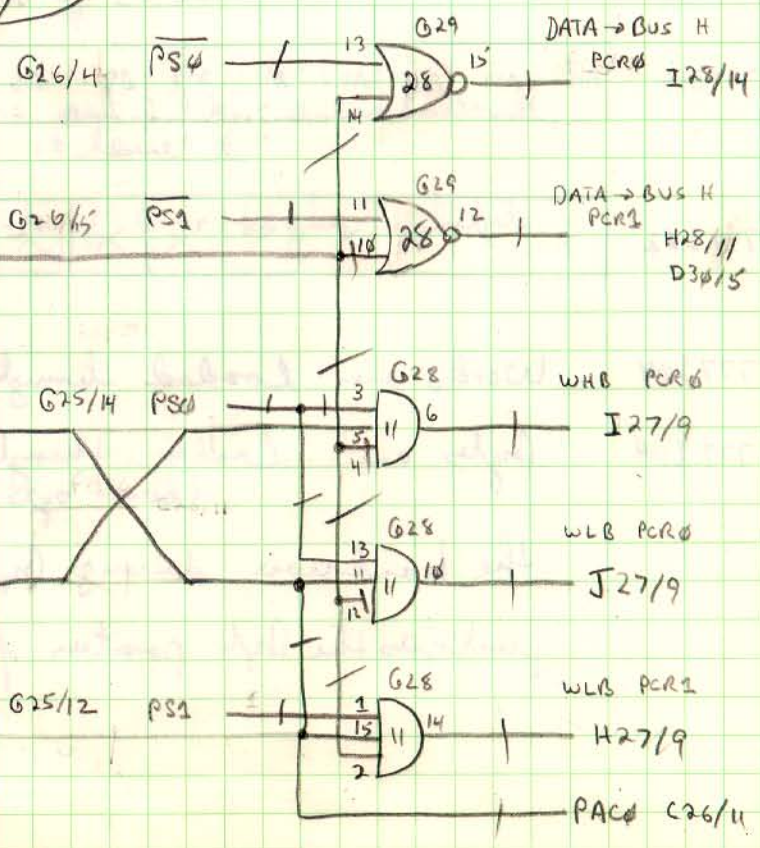
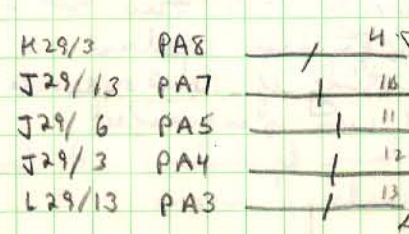
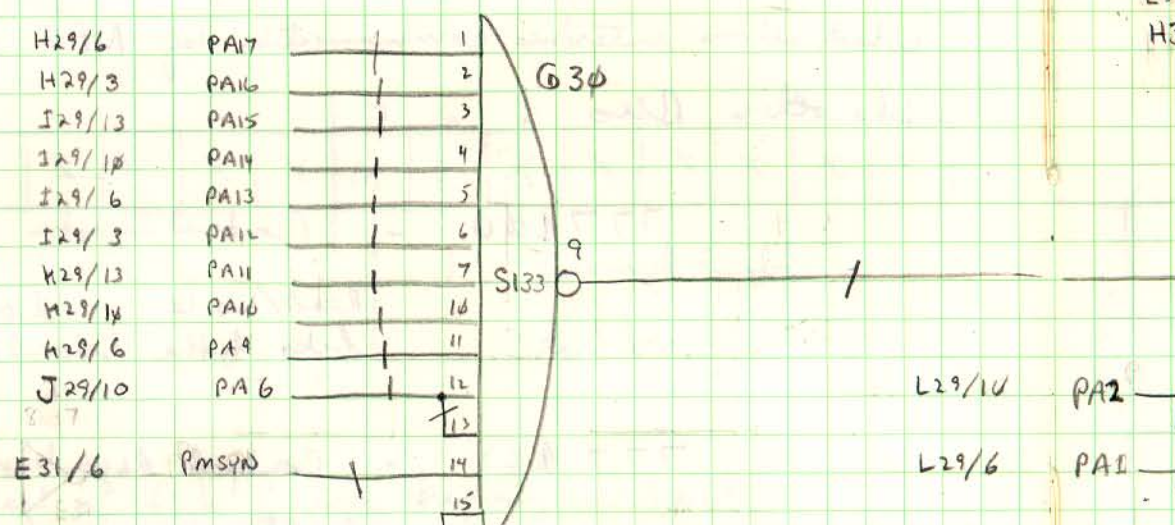
777104 Words are loaded through location 777104

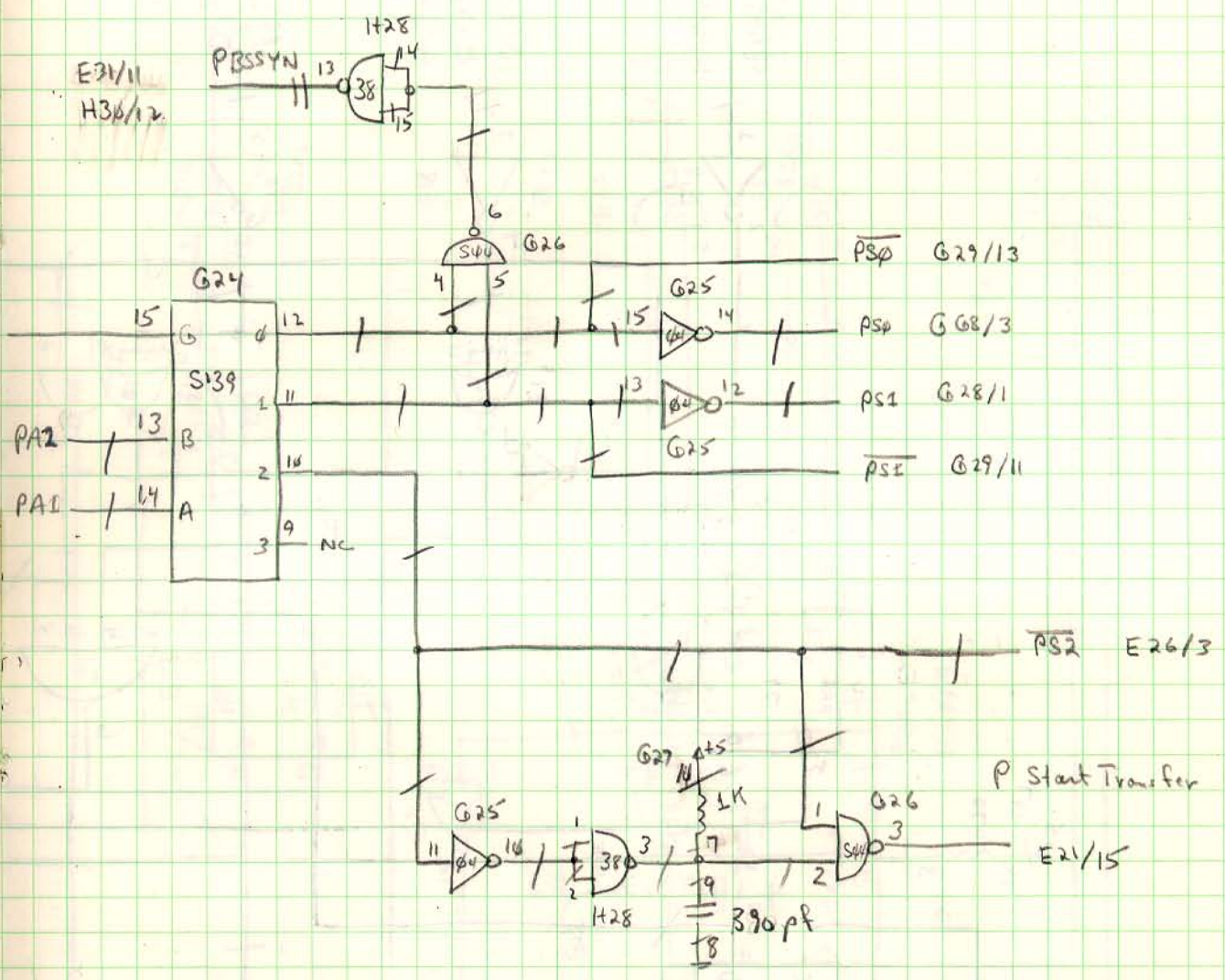
777104 Bytes are loaded through location 777104 (lower byte position)

The hardware during byte read or writes automatically justifies the byte position for proper reading & writing

23 April 77
AMS

Primary Bus Address Decoder - Read/Write Logic



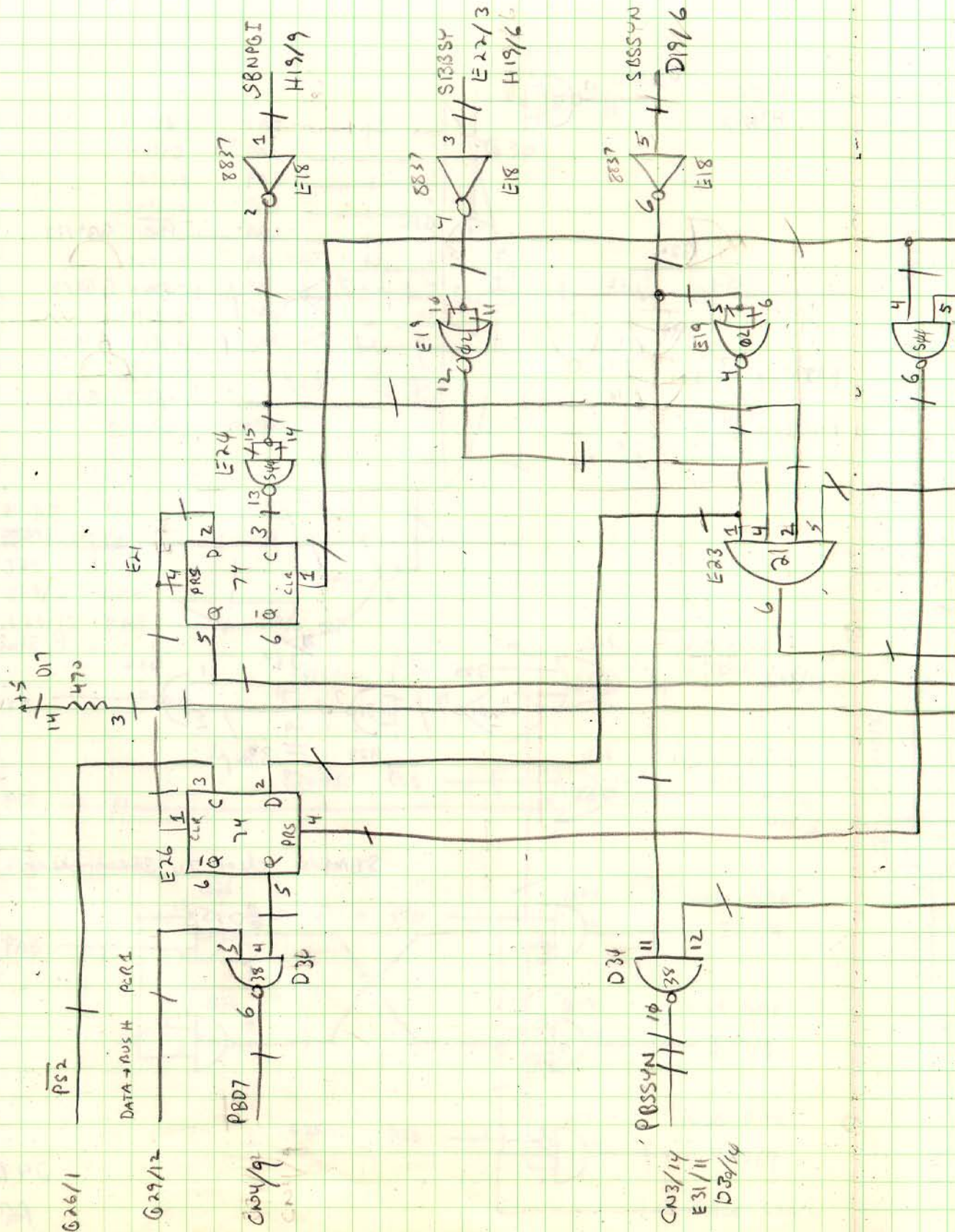


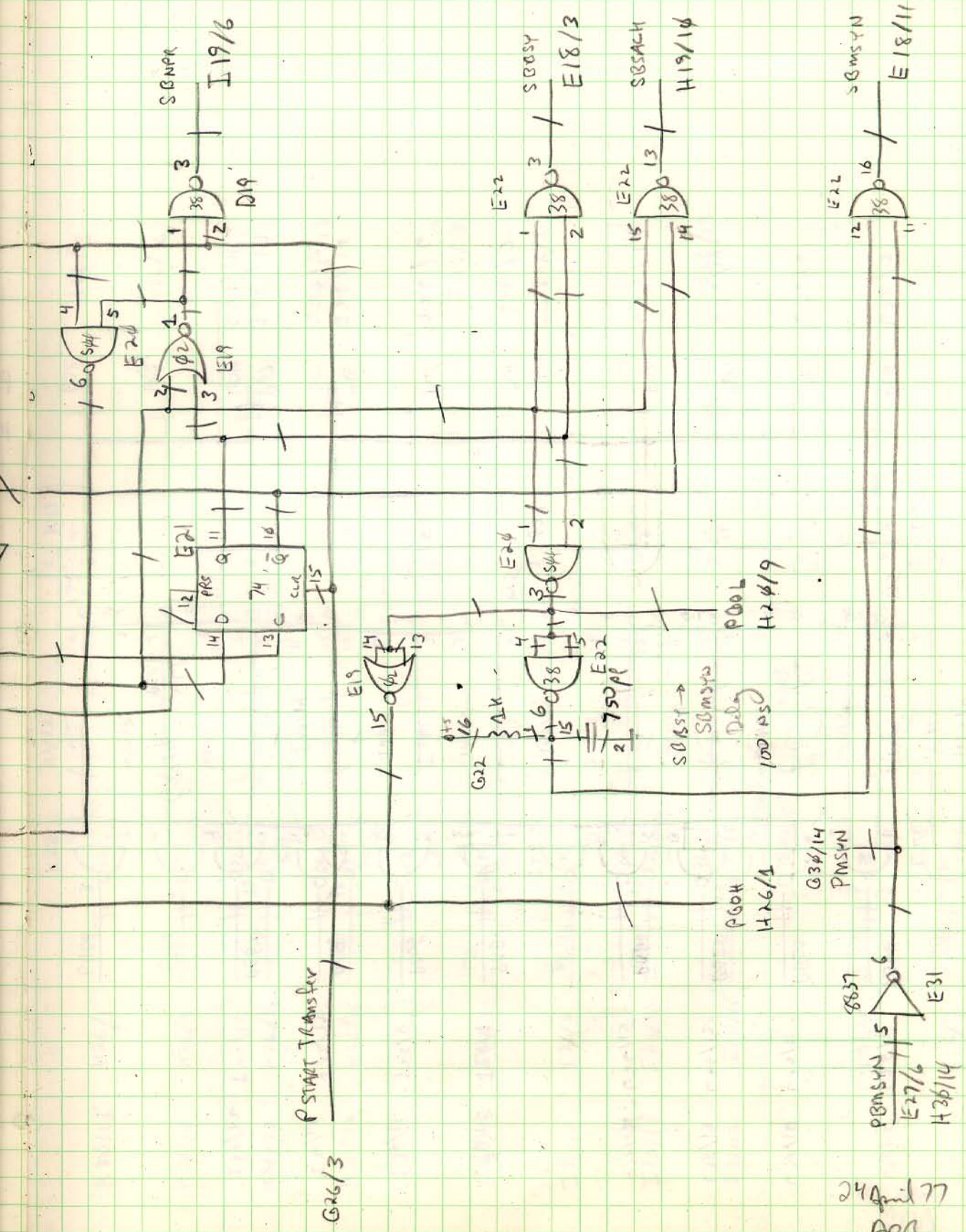
SBMSYN clear to SBRSY clear delay
 ~60NS

24 April 77
 ARS

NPR Transfer Logic

Primary → NPR Secondary

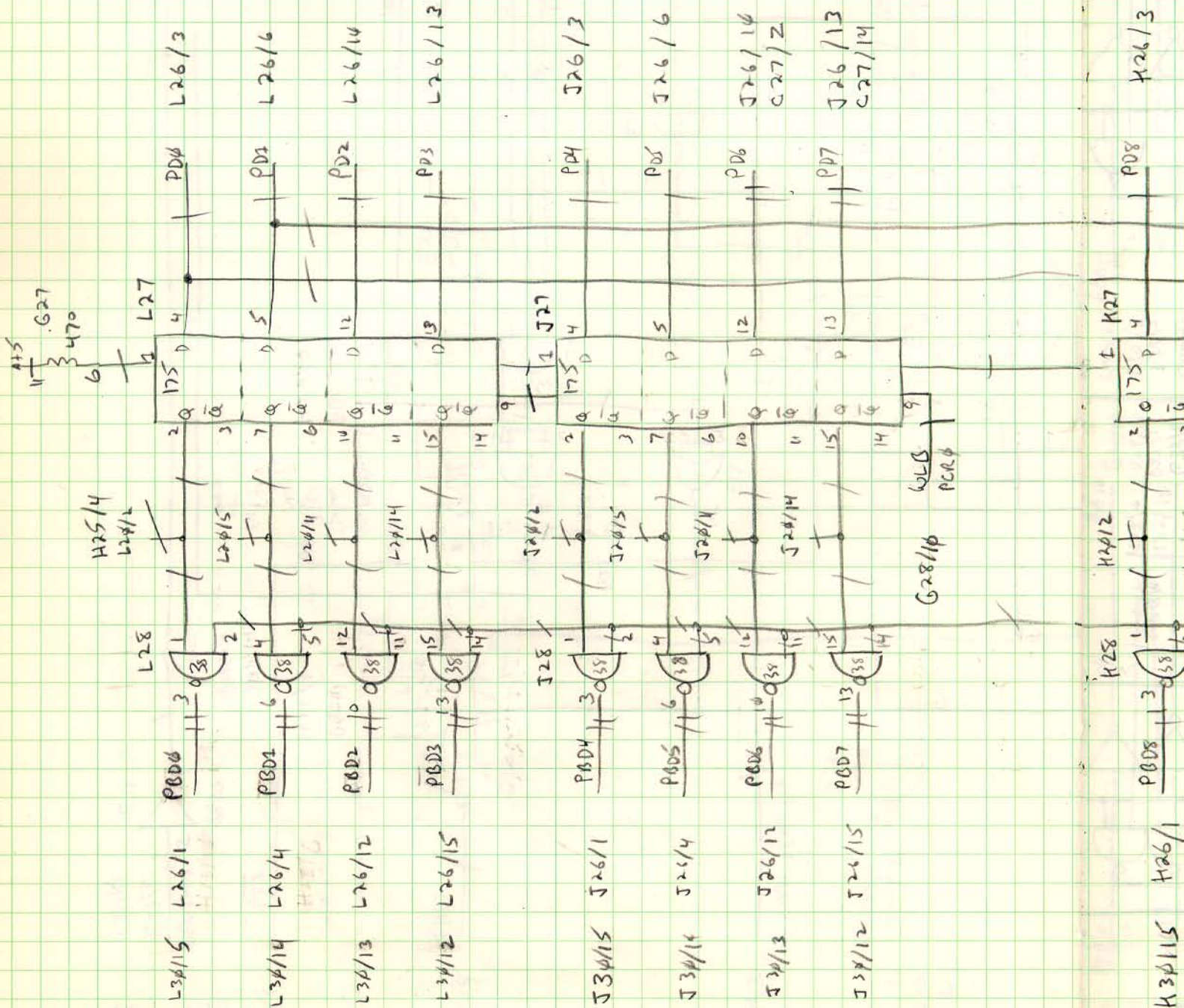


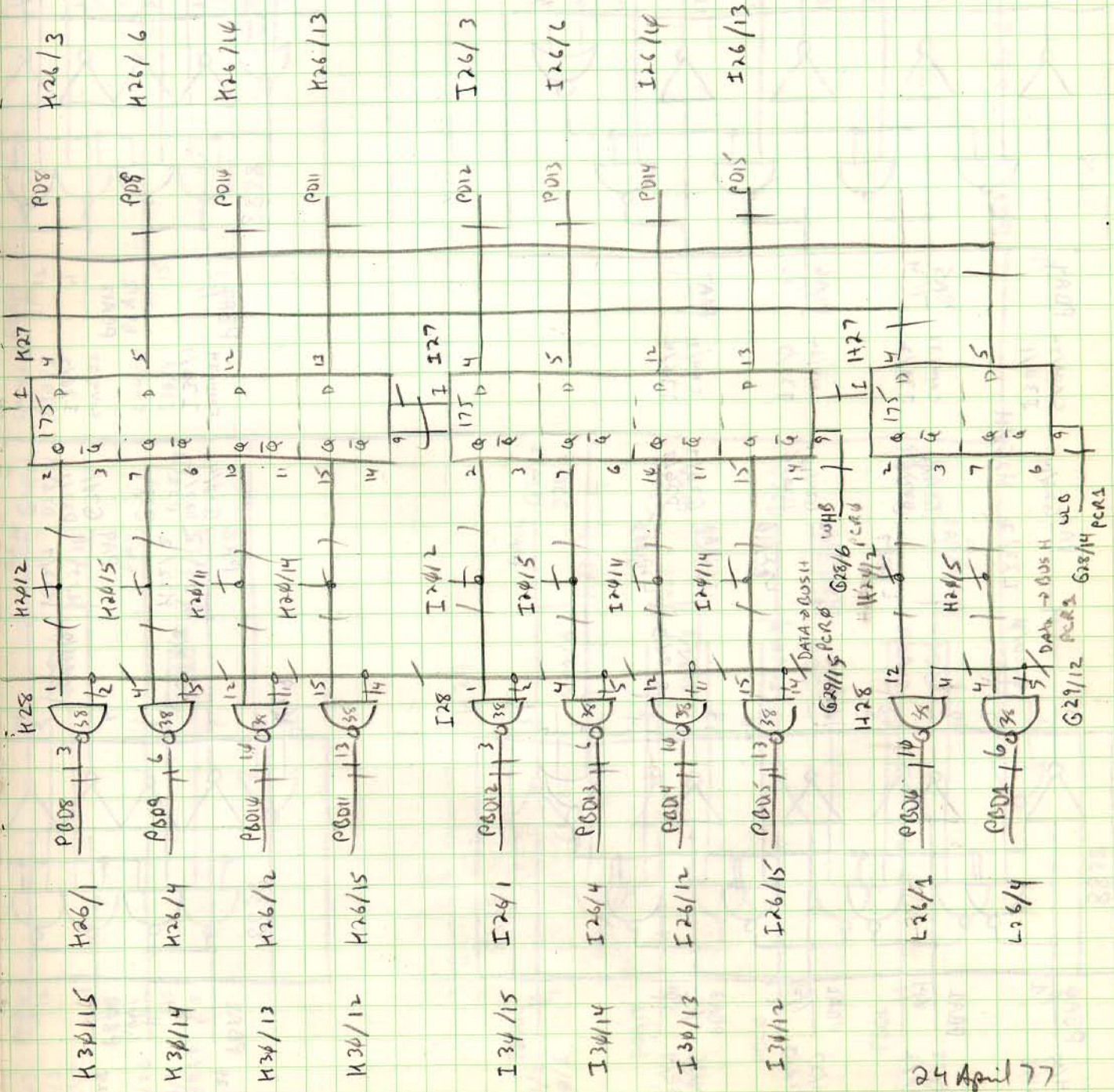


24 April 77
RBB

Primary Bus Control Registers

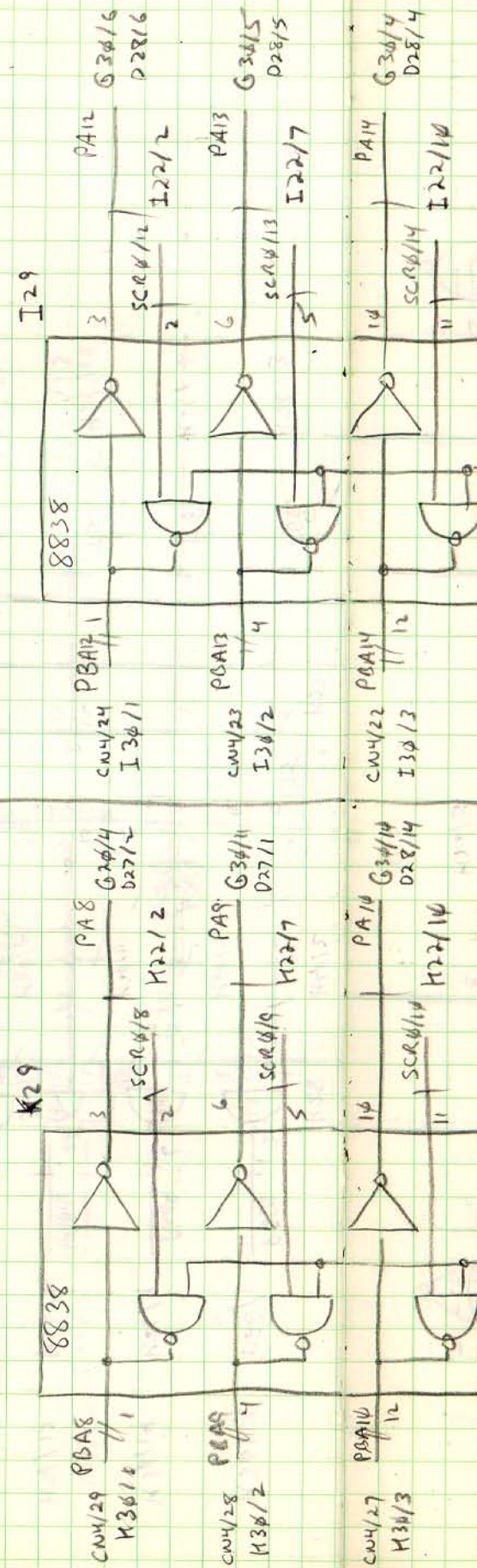
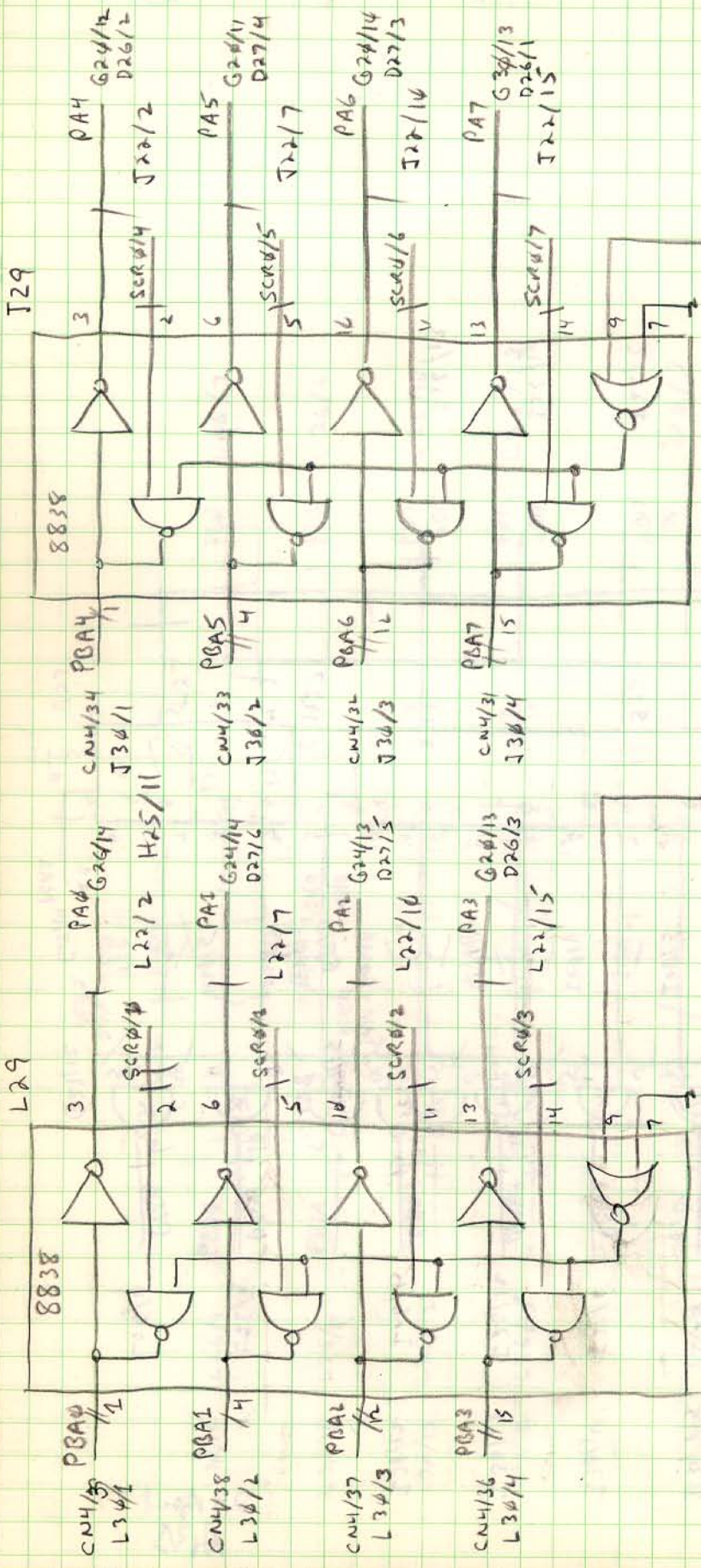
Page 1

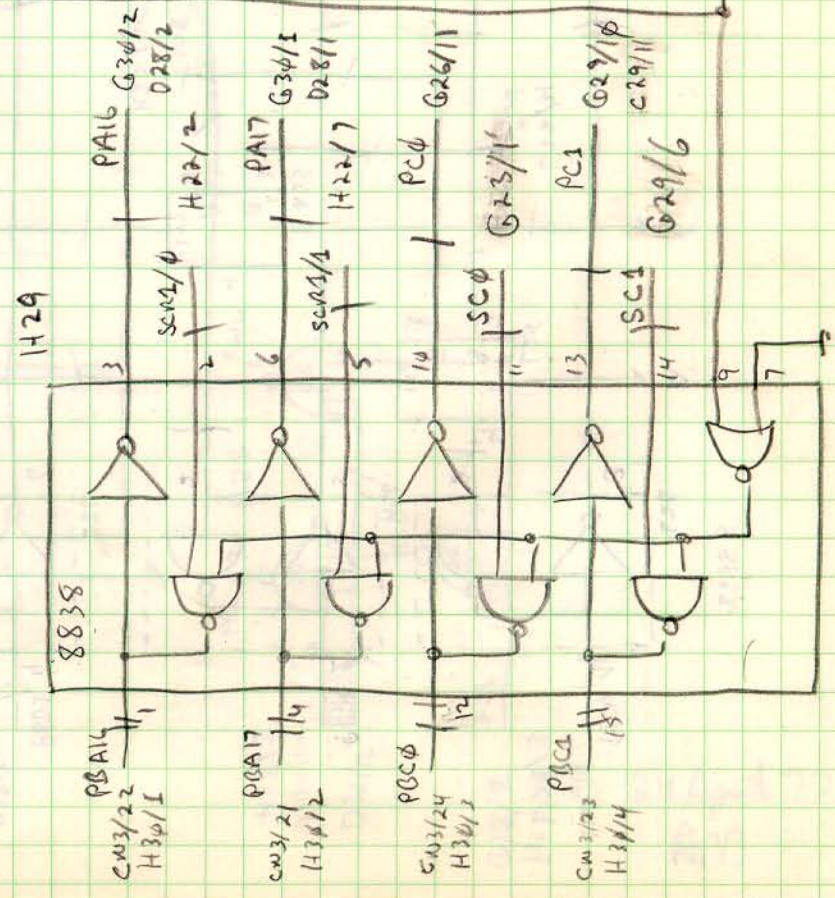
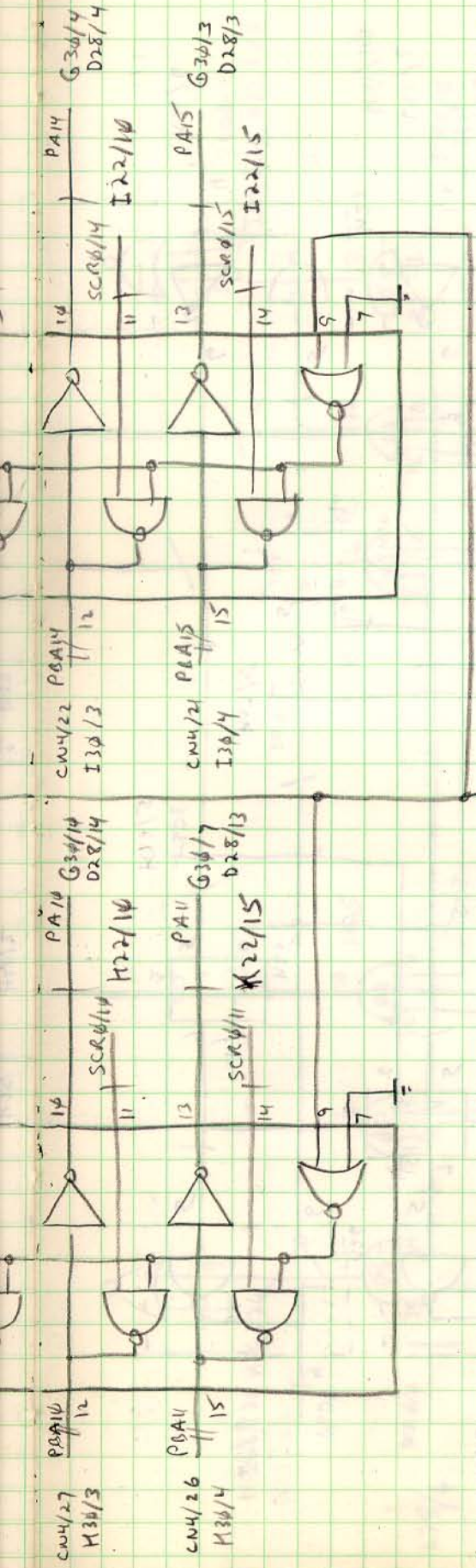




24 April 77
 ARS

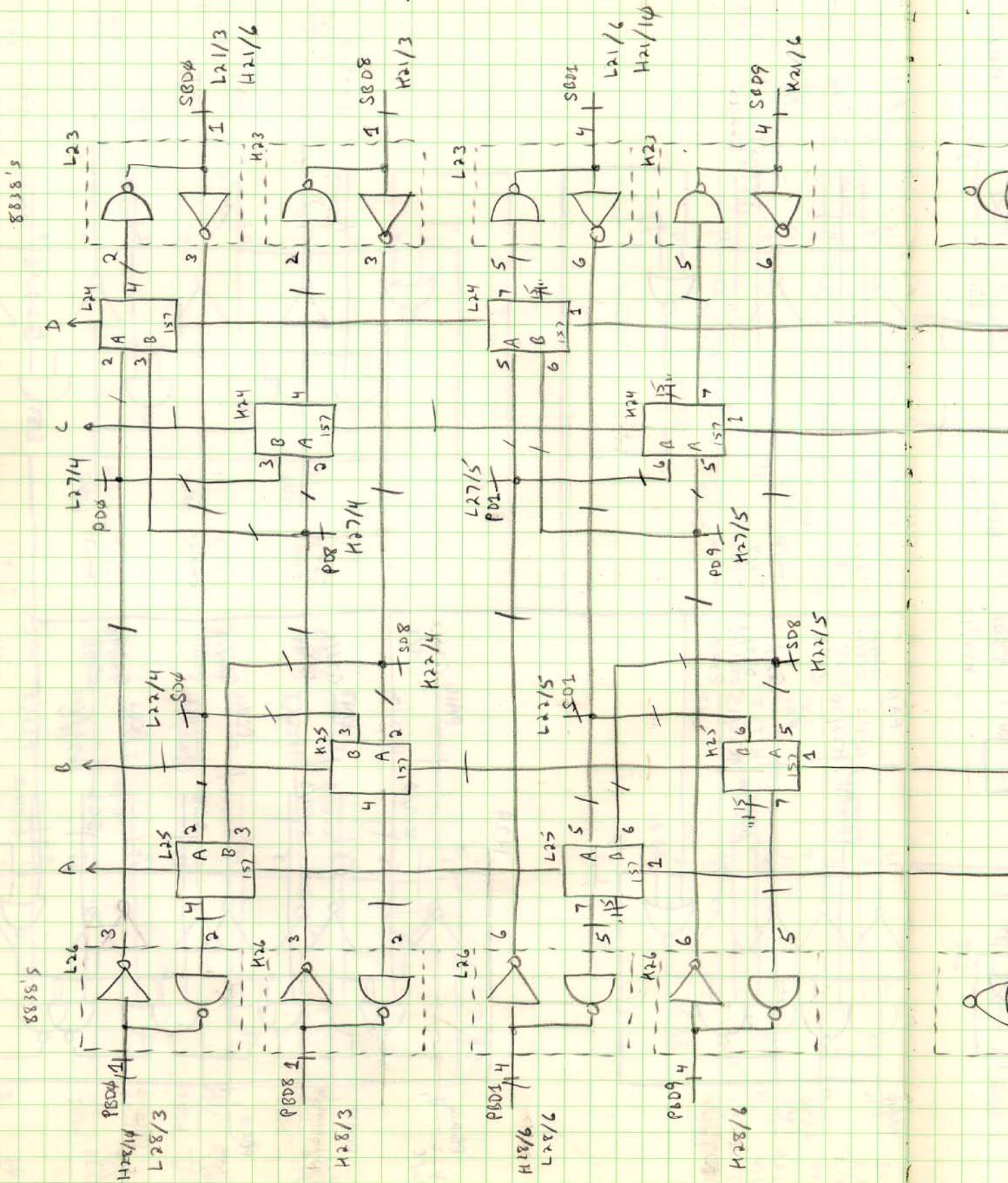
Primary Bus Address Receivers/Drivers

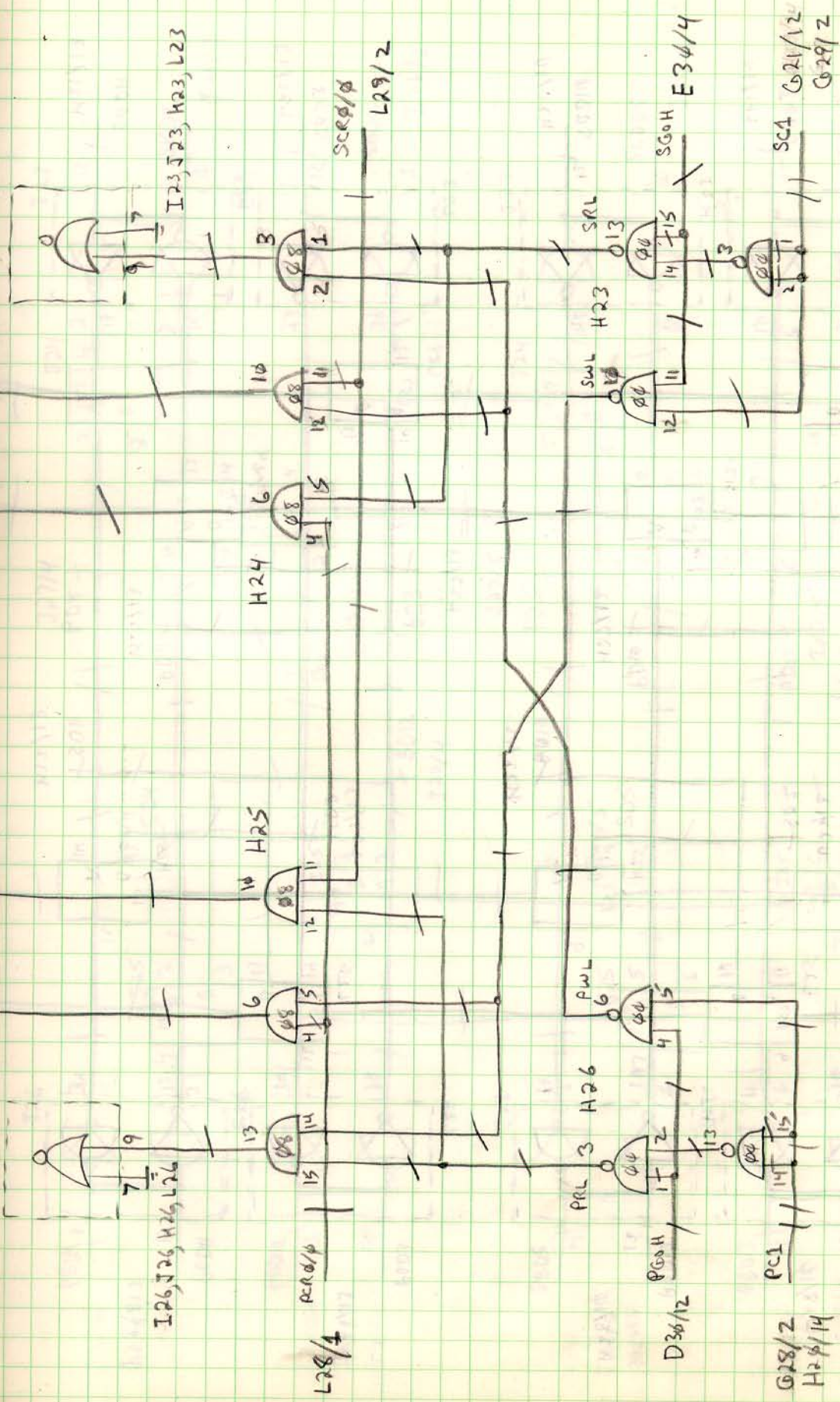




SOOL E29/6

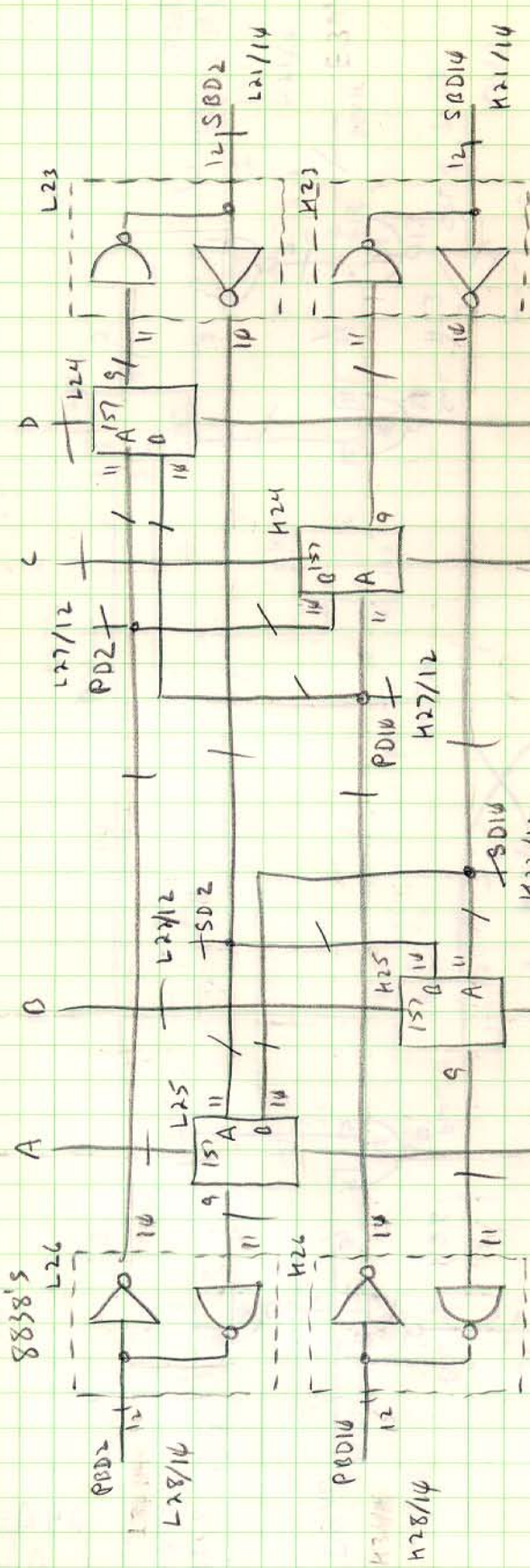
Data Drive Control Logic





24 April 77
 ARB

8838's

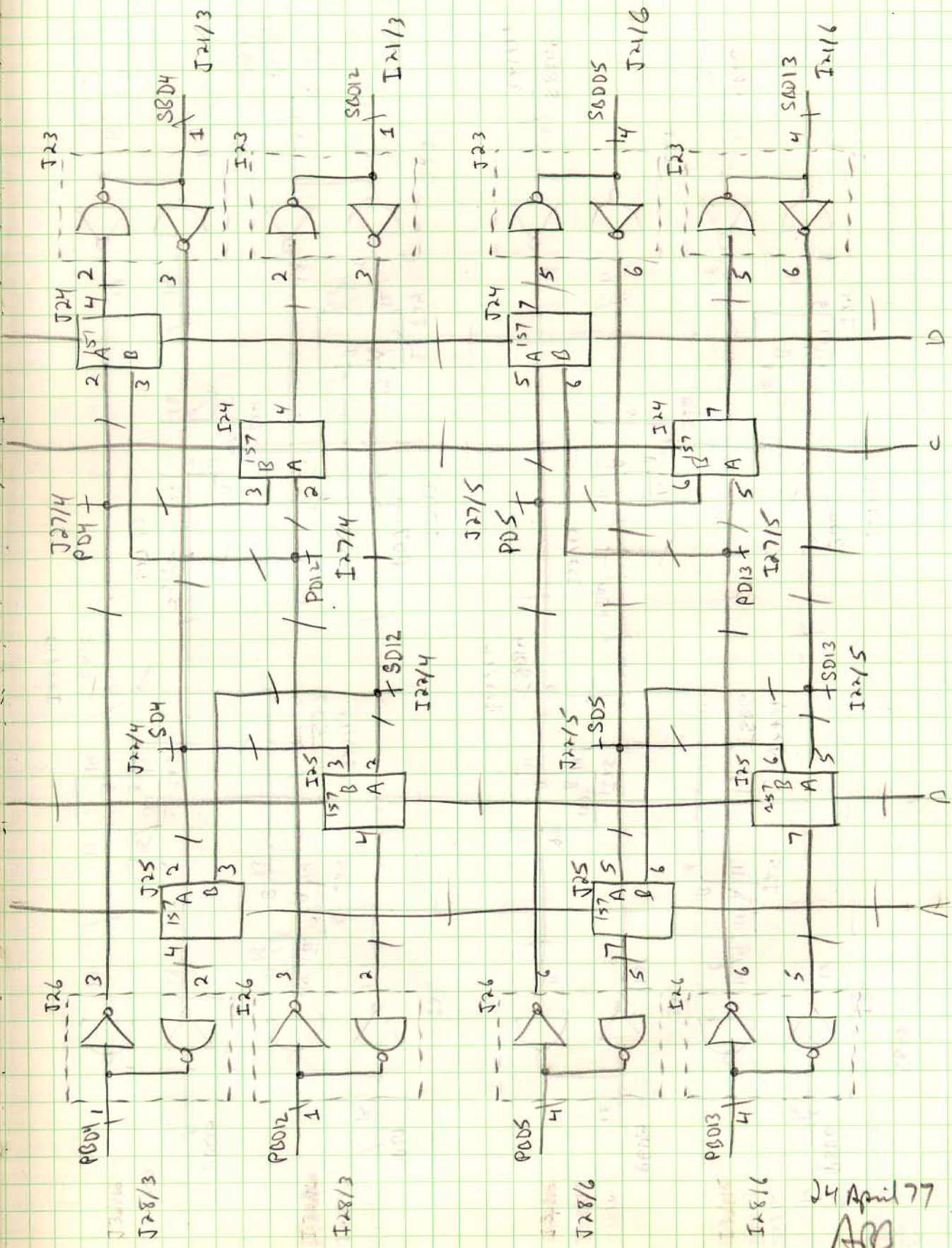


J23

J274 PD4

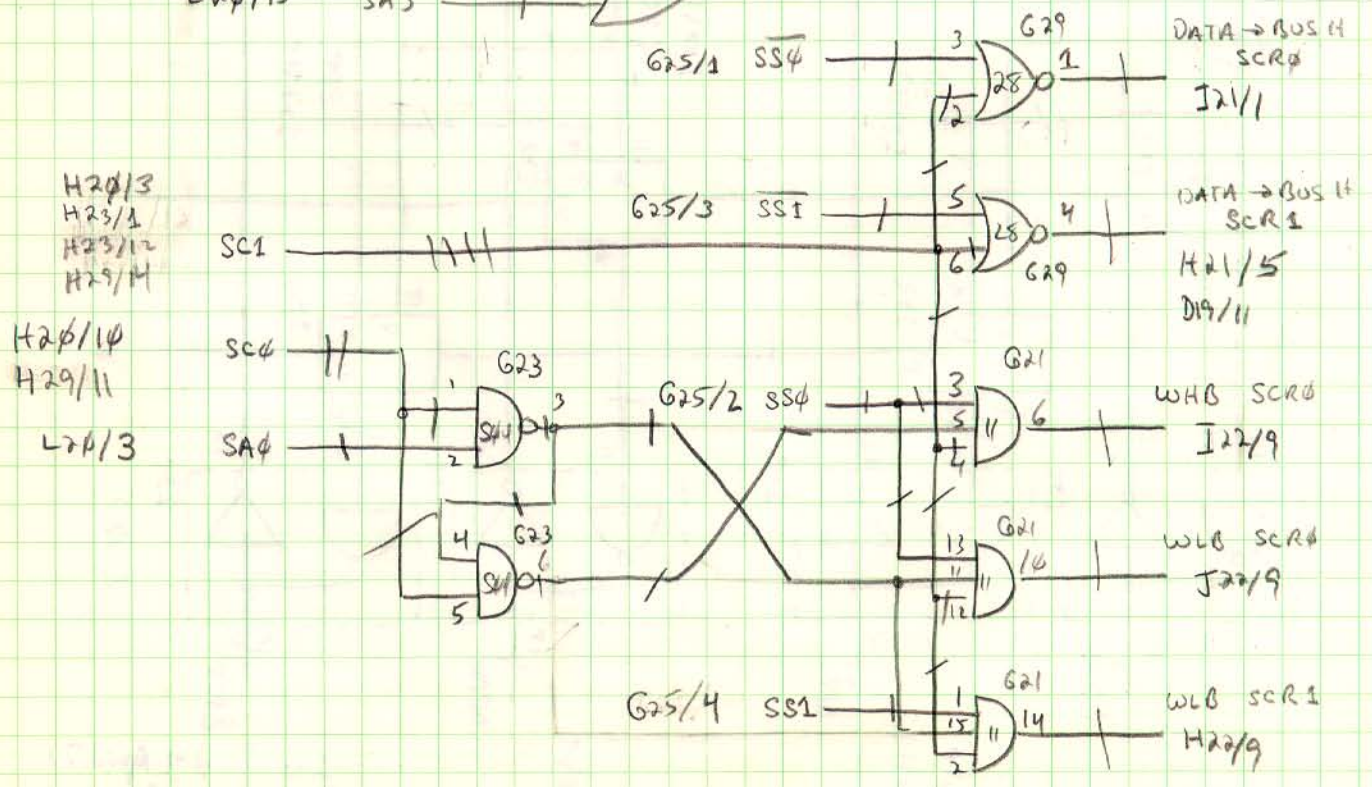
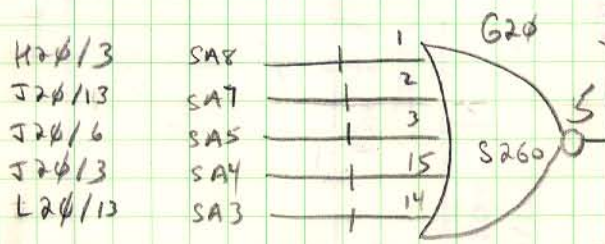
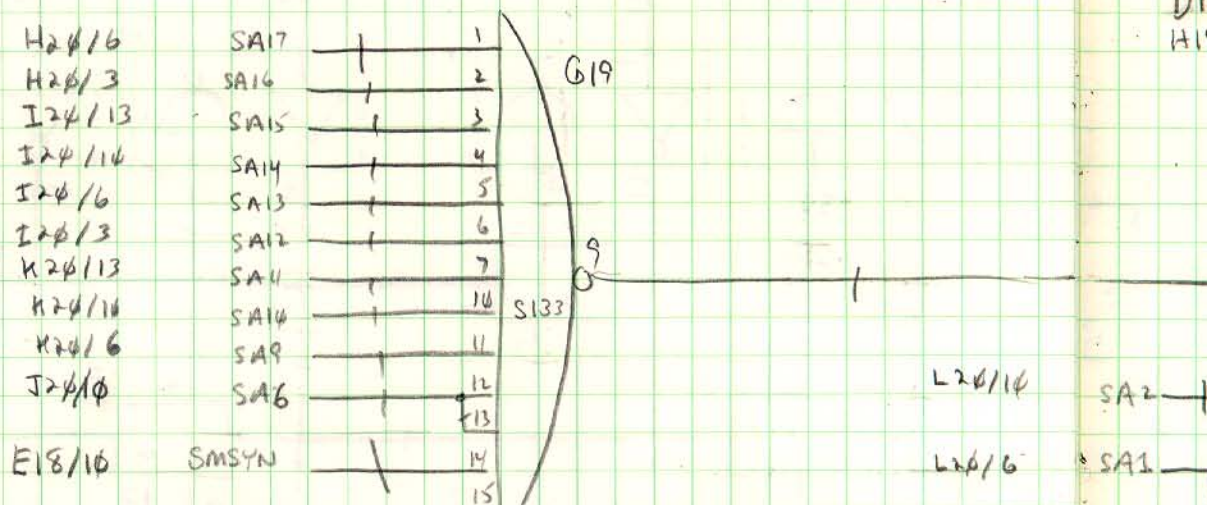
J26

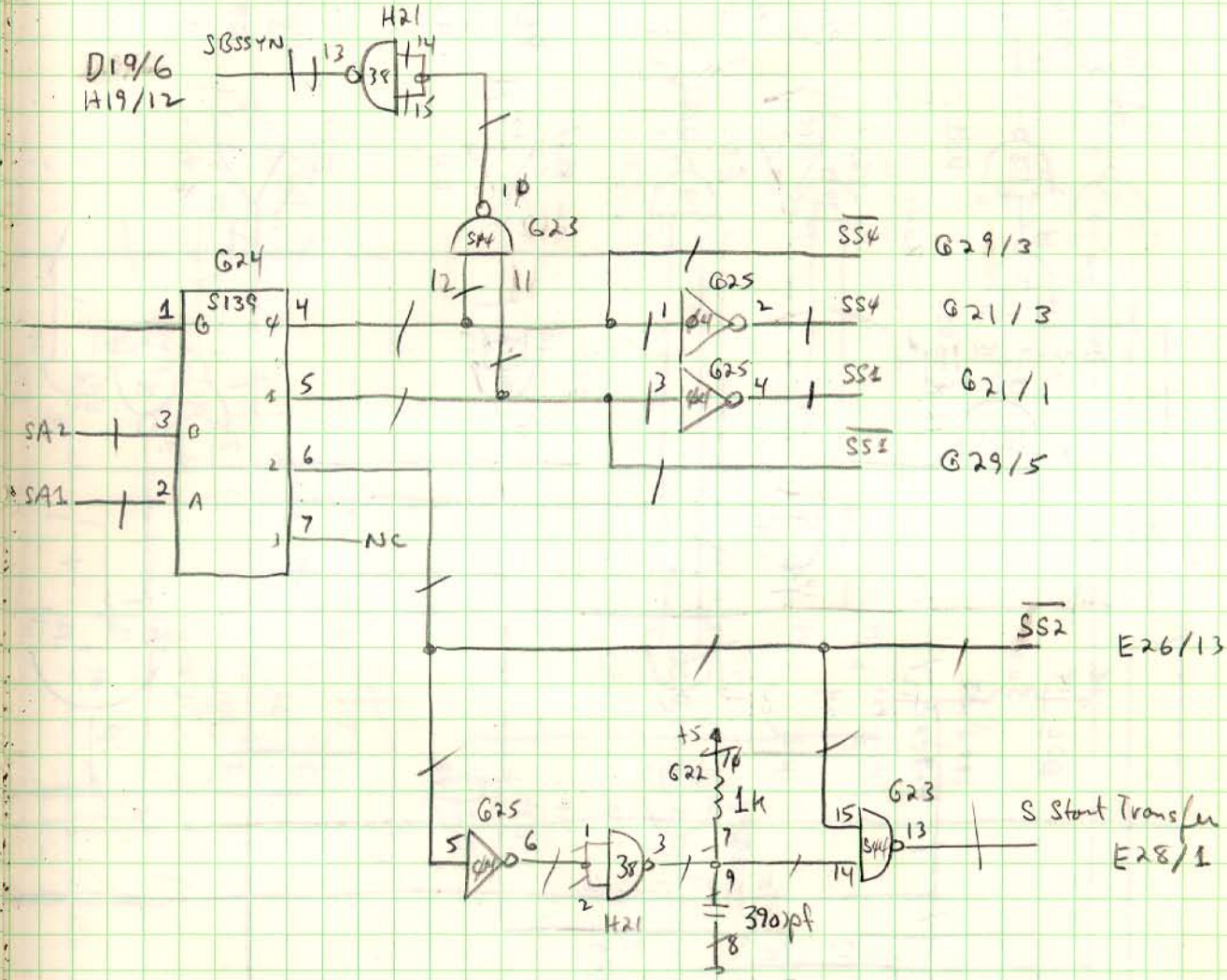
PD4



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 AB

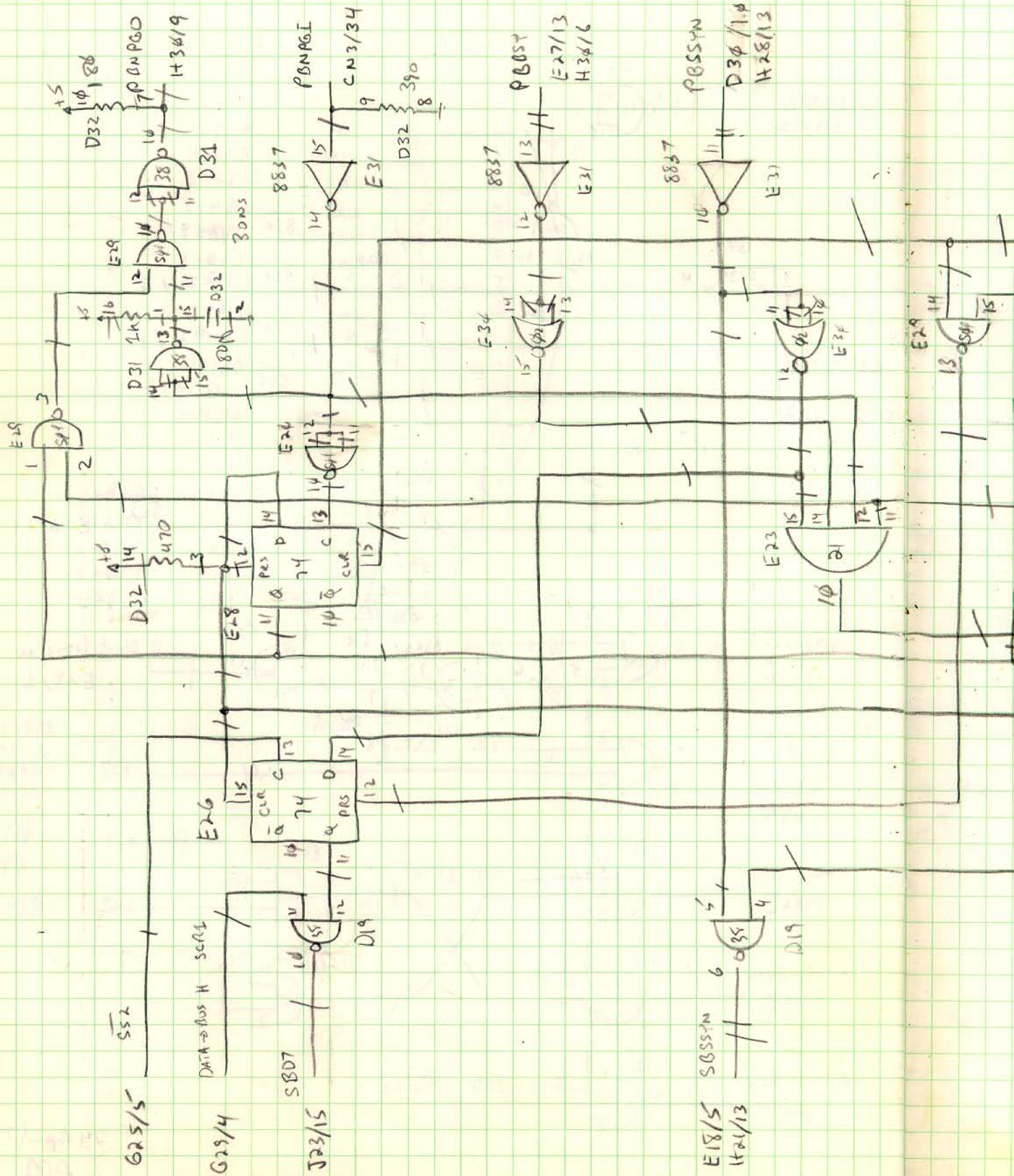
Secondary BUS Address Decoder - Read/Write Logic

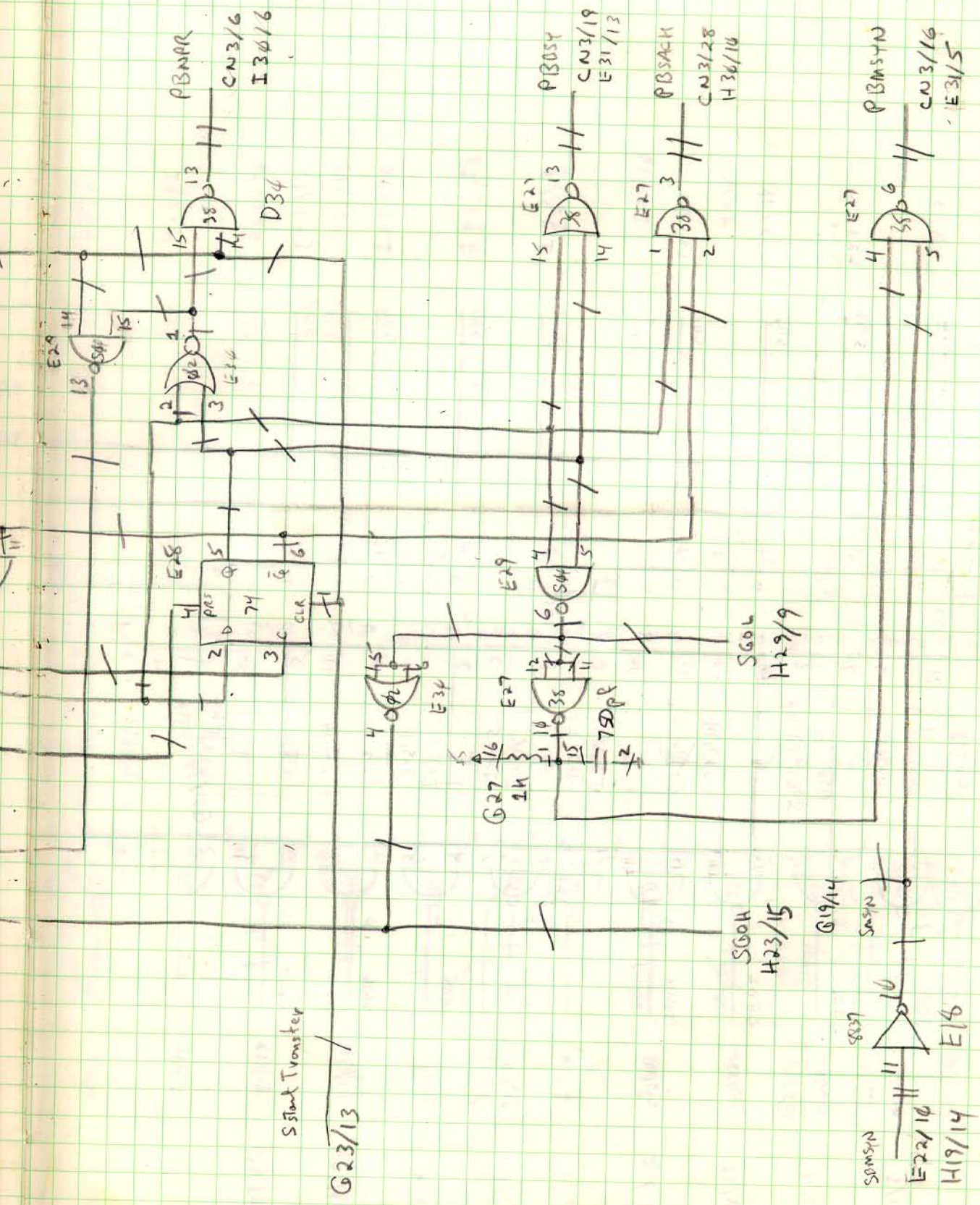




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 APD

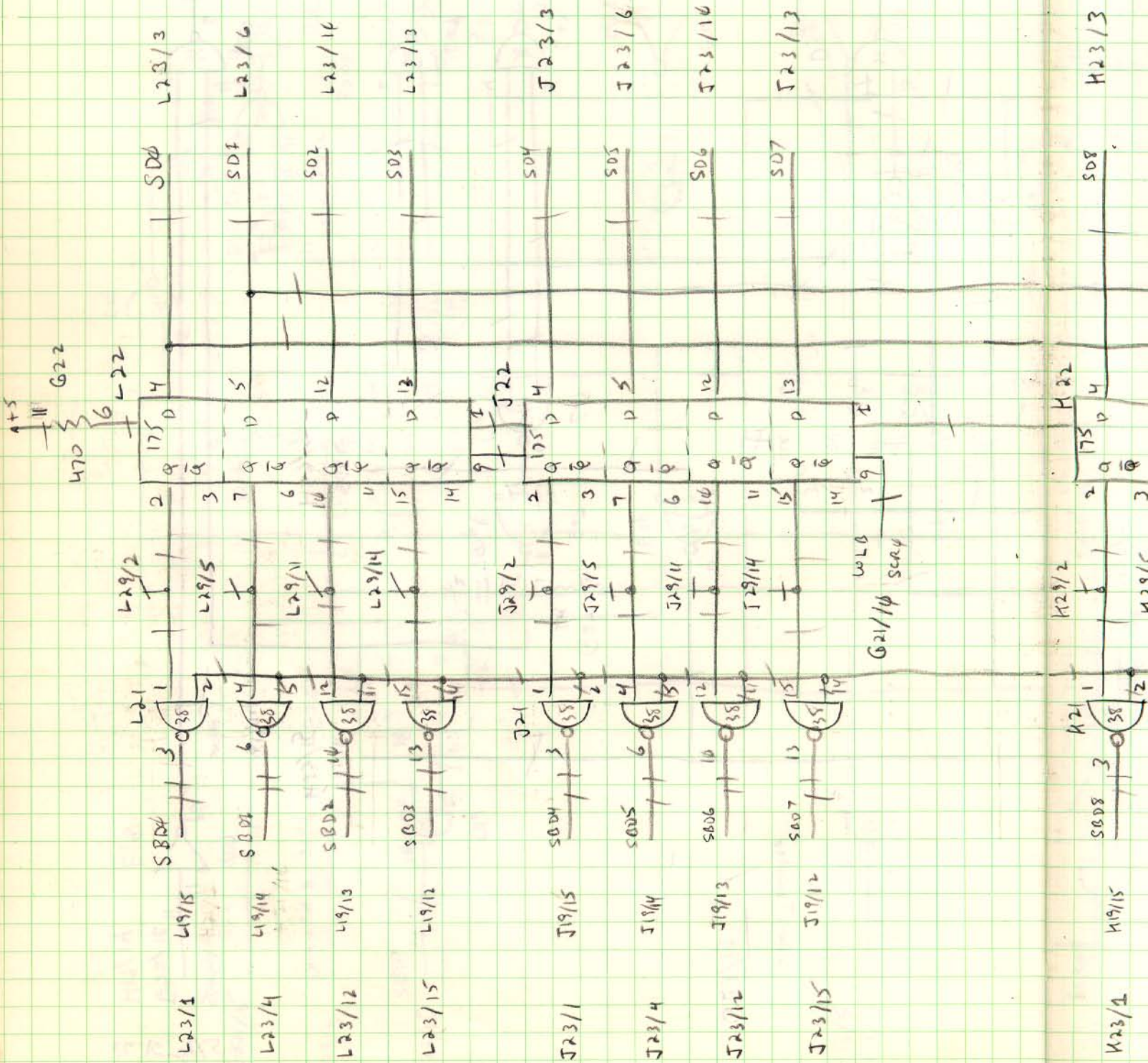
NPR Transfer Logic Secondary → NPR Primary

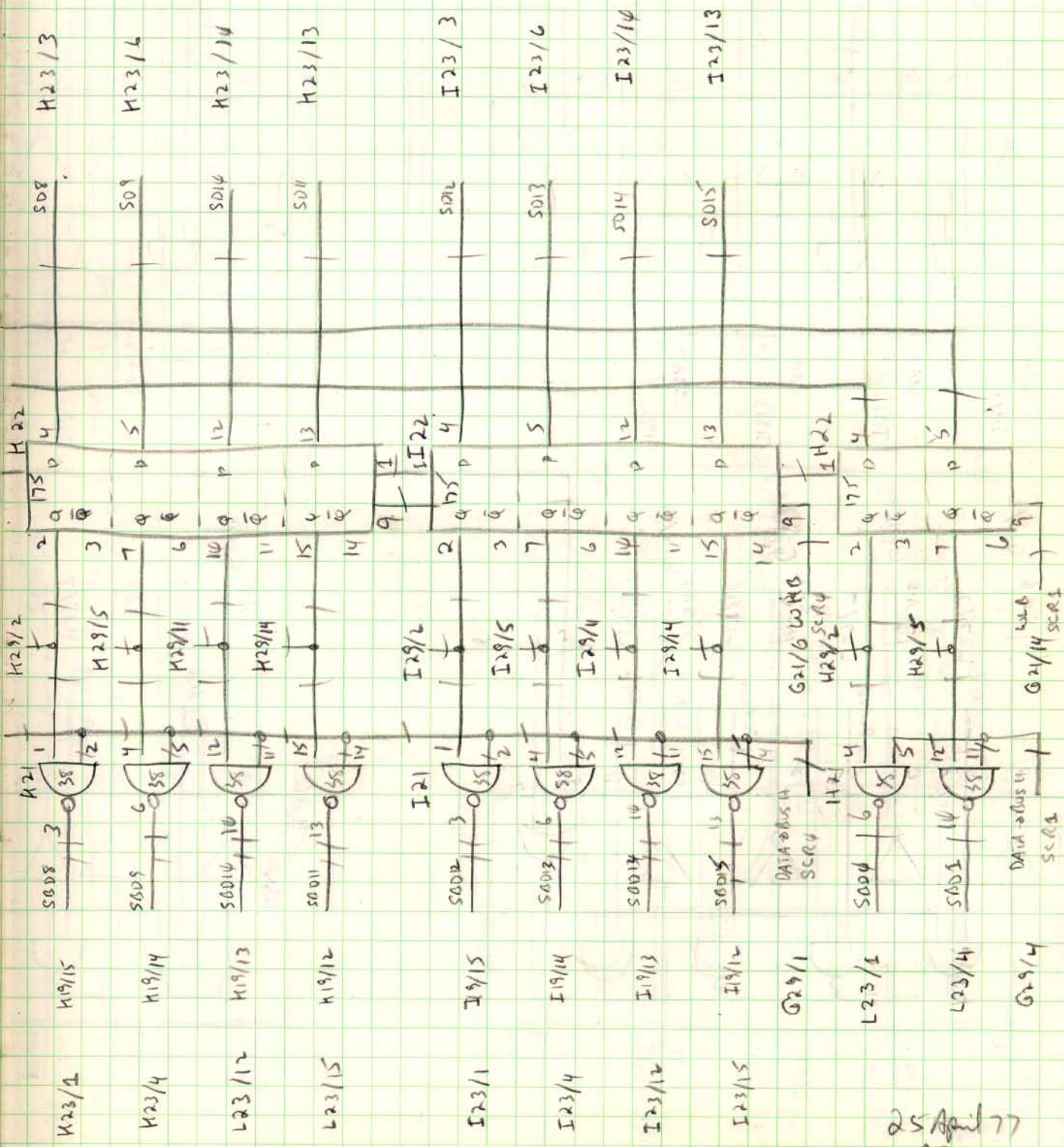




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 ASD

Secondary Bus Central Registers P. 1

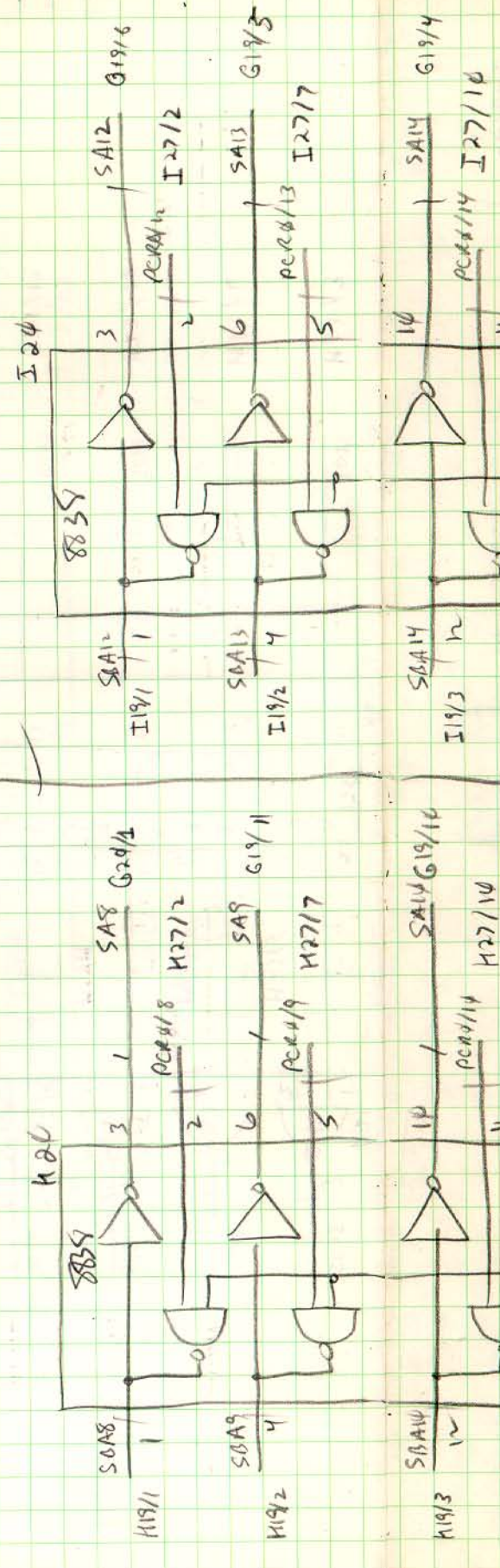
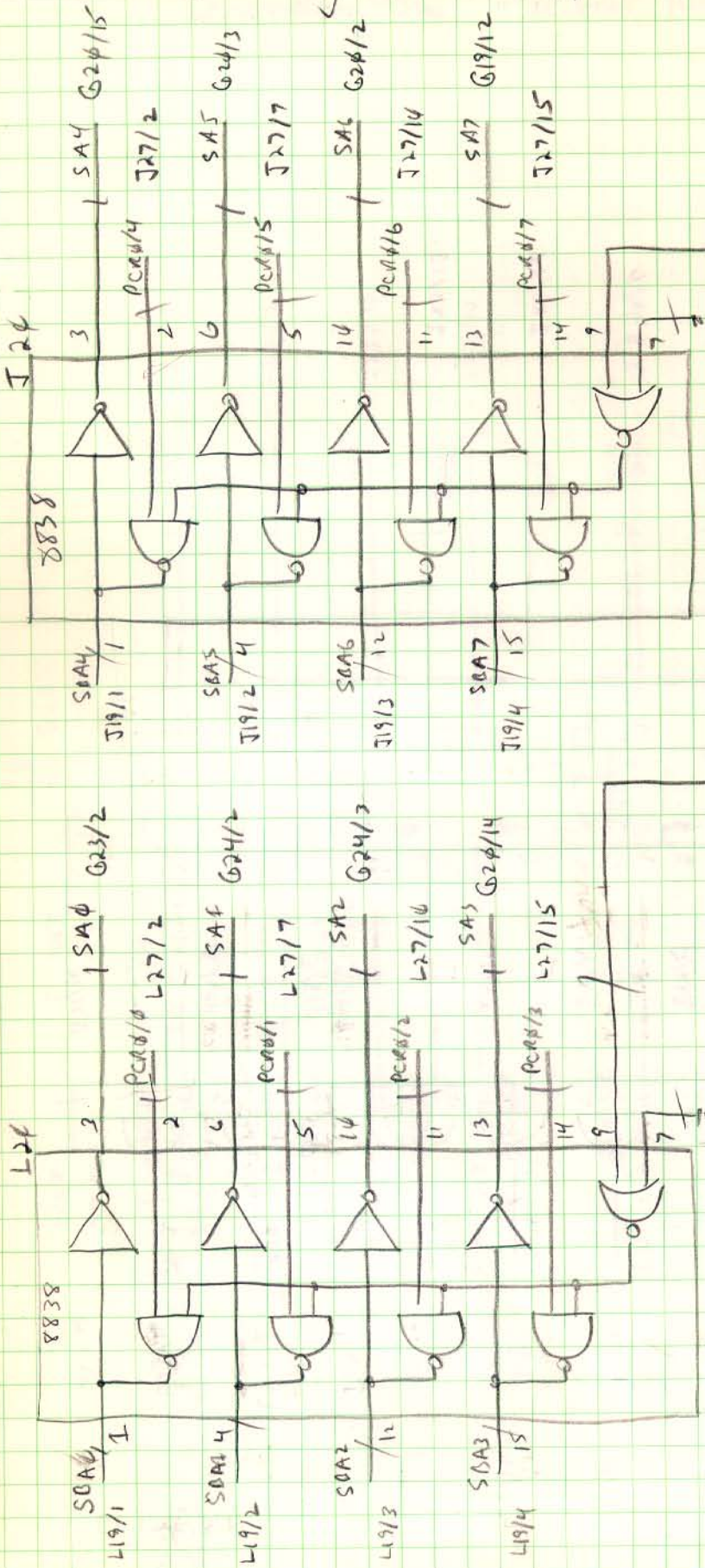


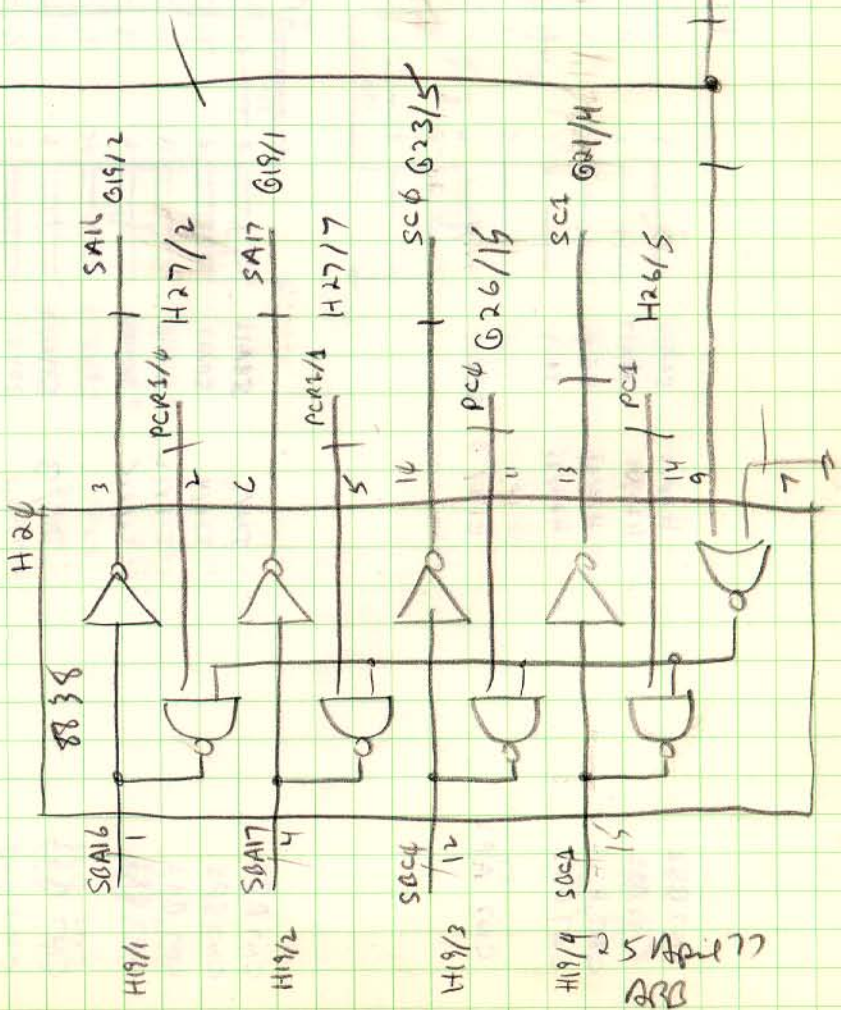
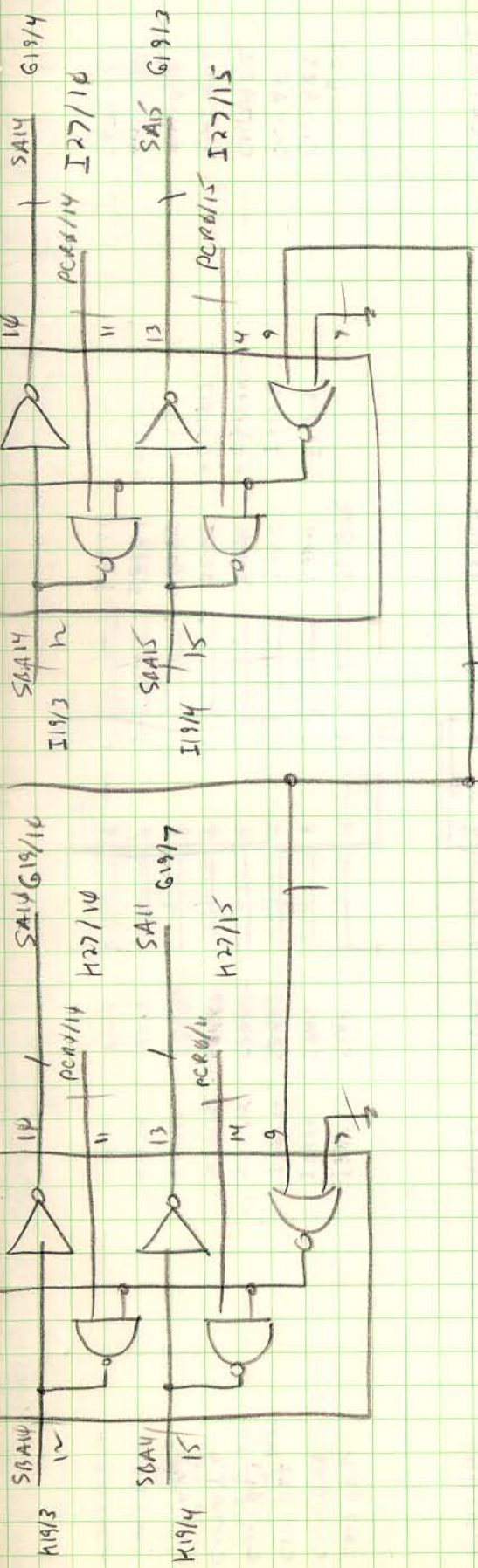


25 April 77
 ARP

Secondary Bus

Address Receivers/Drivers





25 April 77
ARB

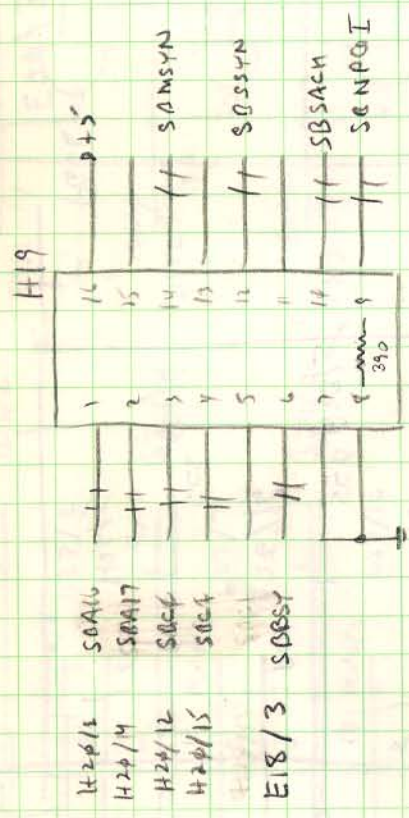
Secondary BUS Terminator

CN7 BS2
CN7 BS1
CN7 BU2
CN7 BT2

CN7 AP2

CN7 BV1
CN7 BU1
CN7 AR2
CN7 AU1

E18/11
H21/13
E22/13
E18/11

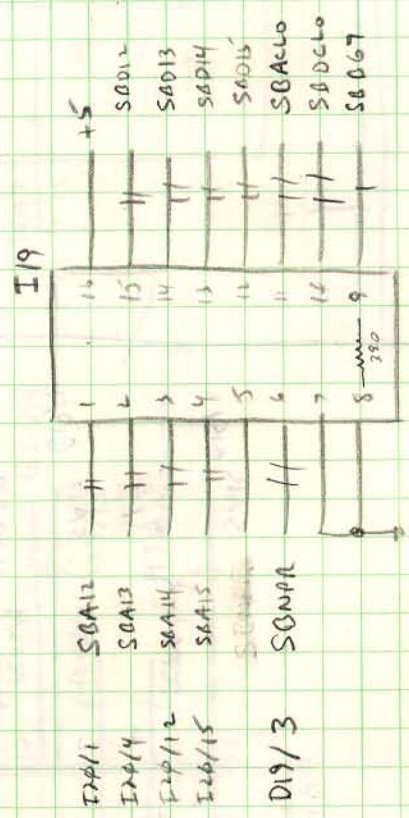


CN7 BP2
CN7 BP1
CN7 BR2
CN7 BR1

CN7 AS2

CN7 AK1
CN7 AL2
CN7 AL1
CN7 AM2
CN7 BF1
CN7 BF2
CN7 AV1

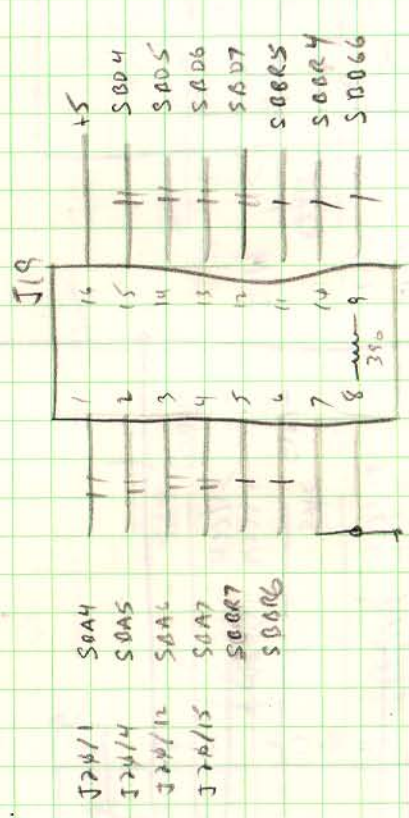
I21/3
I21/6
I21/14
I21/13
A32/11
A31/11



CN7 BH2
CN7 BH1
CN7 BL2
CN7 BL1
CN7 AT2
CN7 AU2

CN7 AE1
CN7 AF2
CN7 AF1
CN7 AH2
CN7 BC1
CN7 BD2
CN7 BA1

J21/3
J21/6
J21/14
J21/13



K19

CN7 BM2

CN7 BM2
 CN7 BM1
 CN7 BN2
 CN7 BN1
 CN7 AM1
 CN7 AN2

CN7 BH2
 CN7 BH1
 CN7 BJ2
 CN7 BJ1
 CN7 AI1
 CN7 AI2

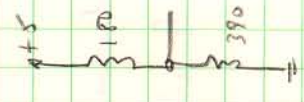
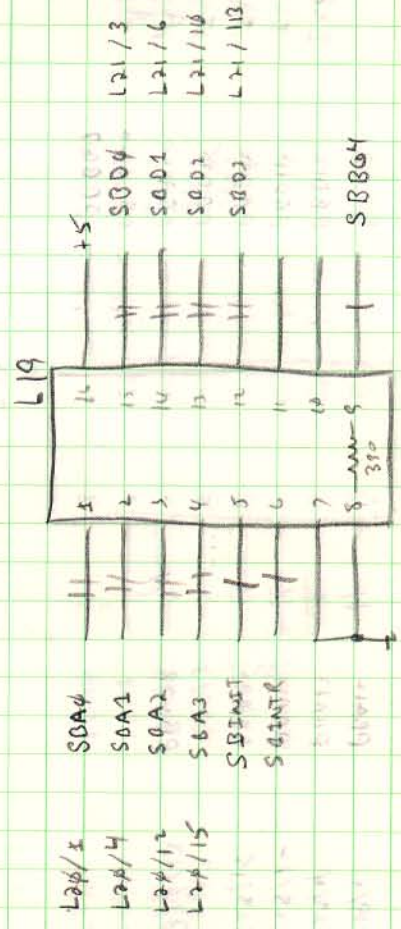
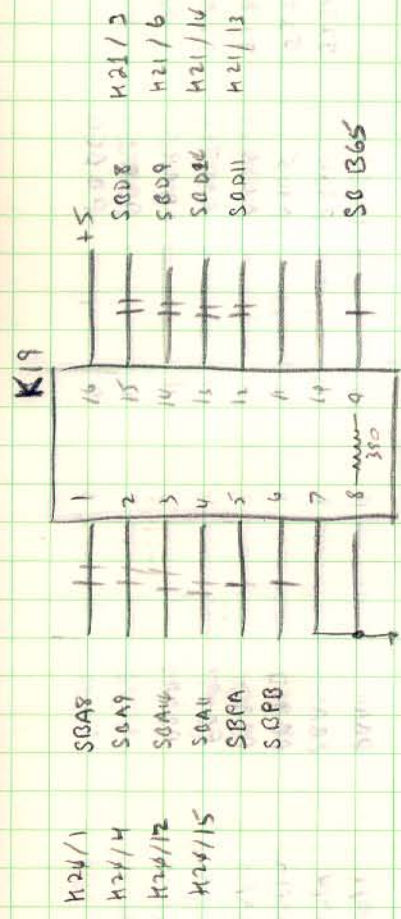
25 April 77
 BRB

CN7 AH1
 CN7 AJ2
 CN7 AJ1
 CN7 AK2

CN7 B01

CN7 AC1
 CN7 AD2
 CN7 AD1
 CN7 AE2

CN7 BE2



Pins 1-6, 16-15 Bus Termination
 End of Secondary BUS

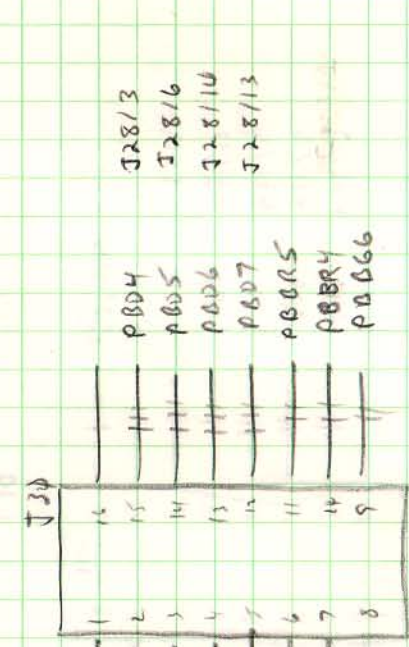
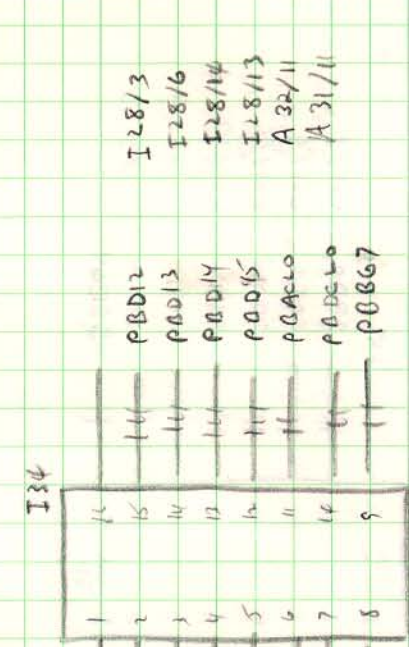
Primary BUS Terminator Locations (Terminators)

mut

Location	Terminator	Label
H29/1	PDA16	CN6BS2
H29/4	PDA17	CN6BS1
H29/12	PBC4	CN6BU2
H29/15	PBC4	CN6BT2
E31/13	PDB5	CN6AP2

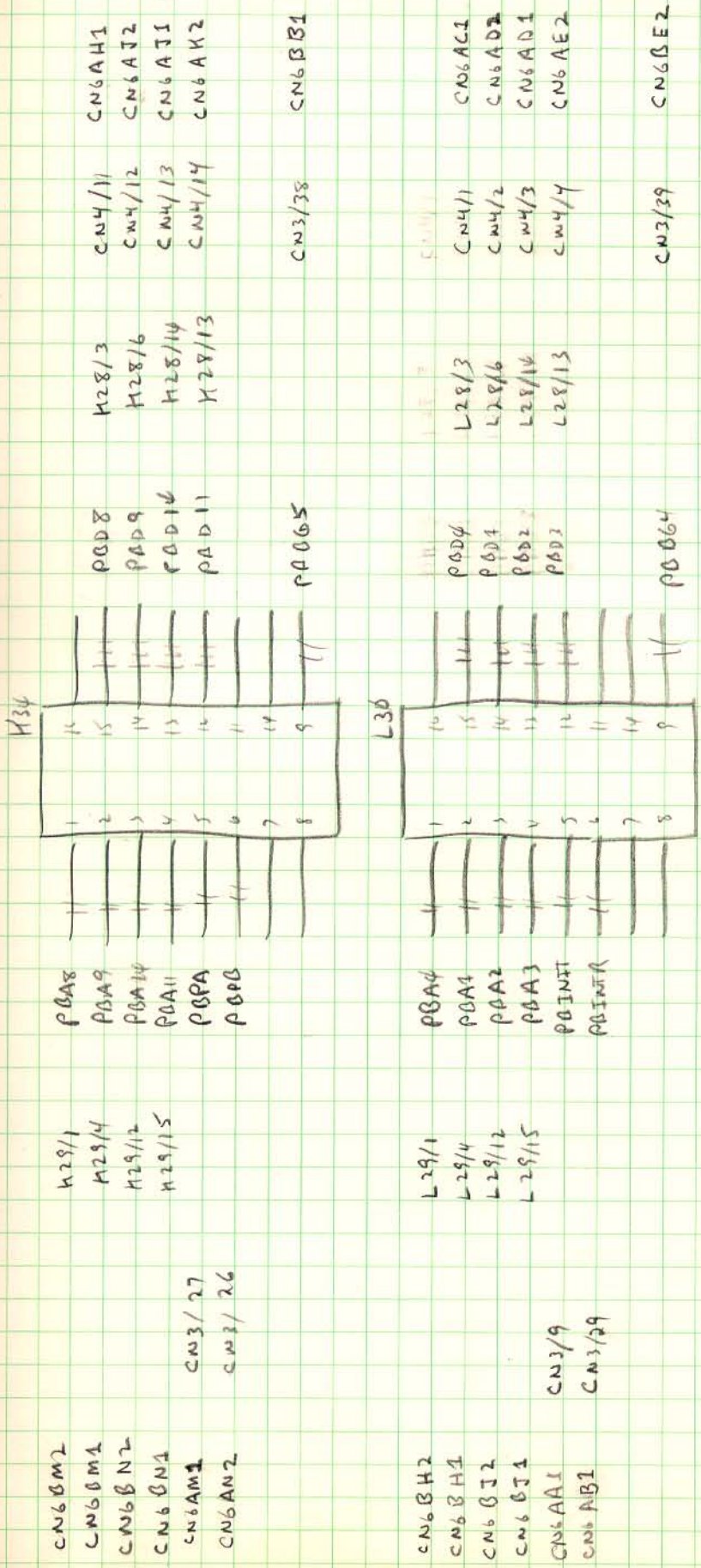
Location	Terminator	Label
I29/1	PBA12	CN6BP2
I29/4	PBA13	CN6BP1
I29/12	PDA14	CN6BR2
I29/15	PDA15	CN6BR1
D36/13	PBNPR	CN6AS2

Location	Terminator	Label
J29/1	PBA4	CN6BK2
J29/4	PBA5	CN6BK1
J29/12	PBA6	CN6BL2
J29/15	PBA7	CN6BL1
CN3/4	PBB7	CN6AT2
CN3/3	PBB6	CN6AU2



H34

not normally used here)

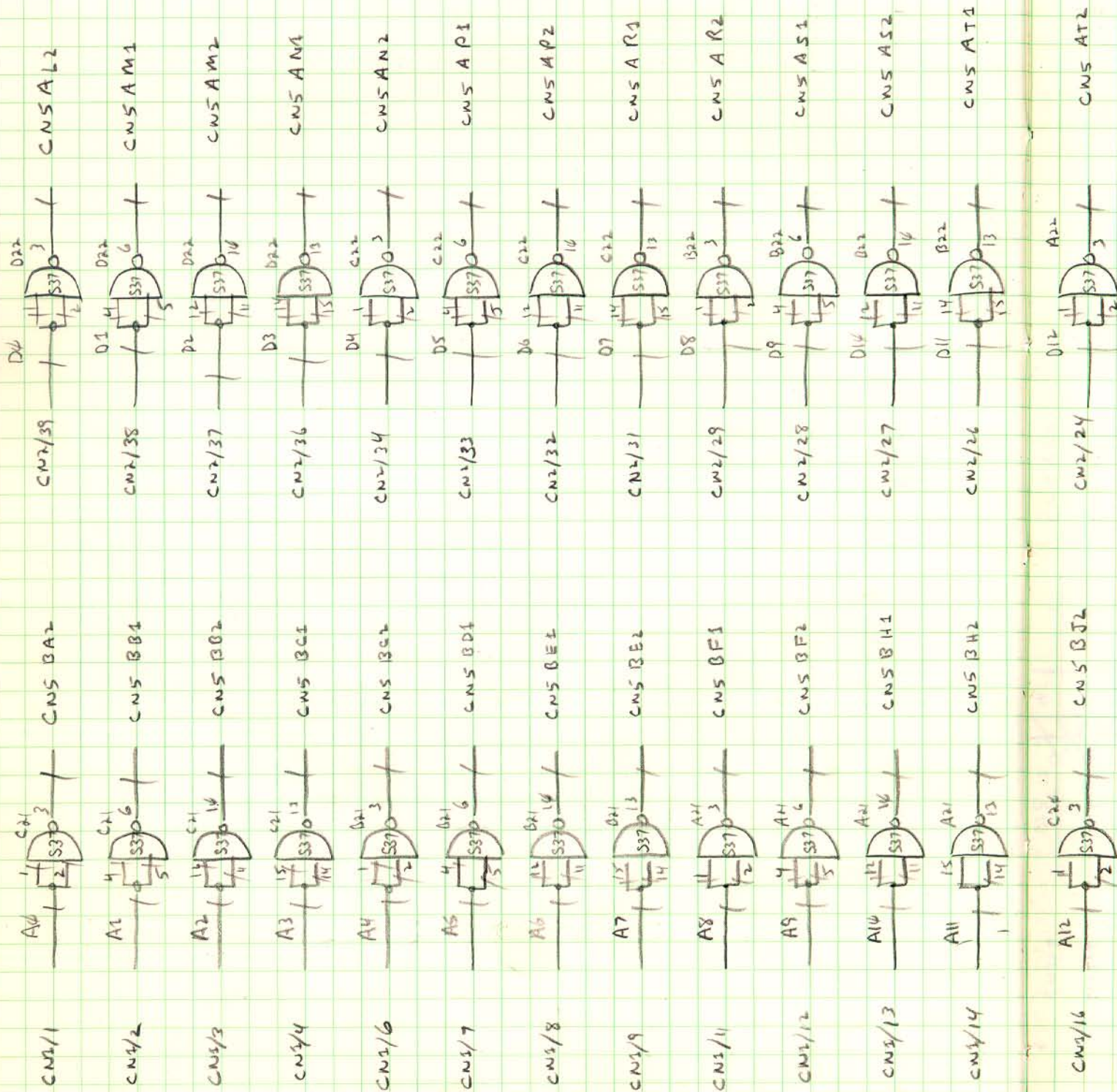


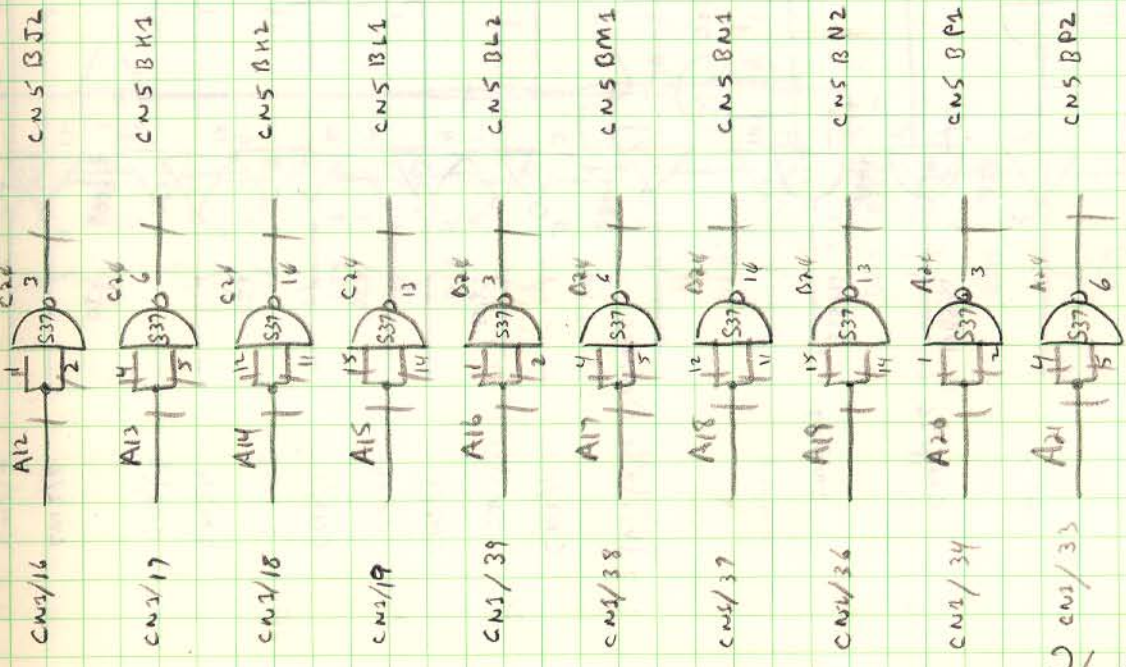
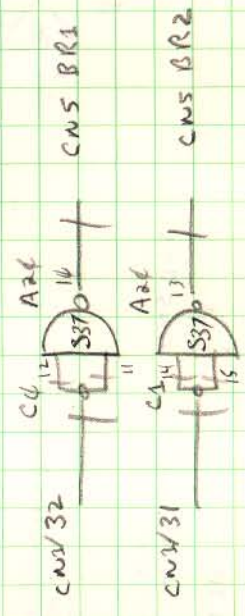
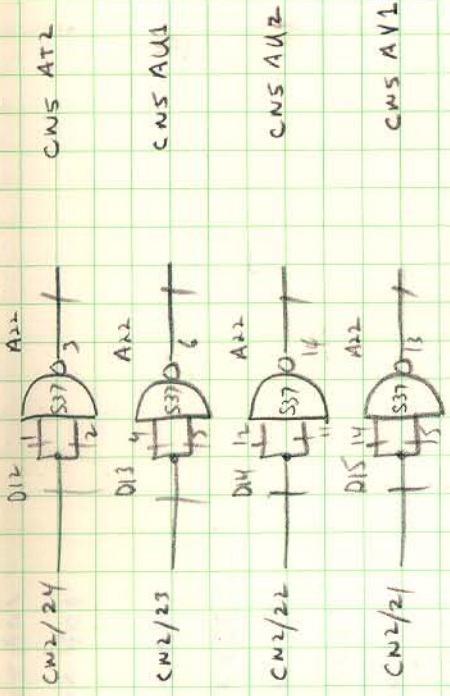
Terminators not normally inserted

as this is not the end of the Primary Bus

25 April 77
APD

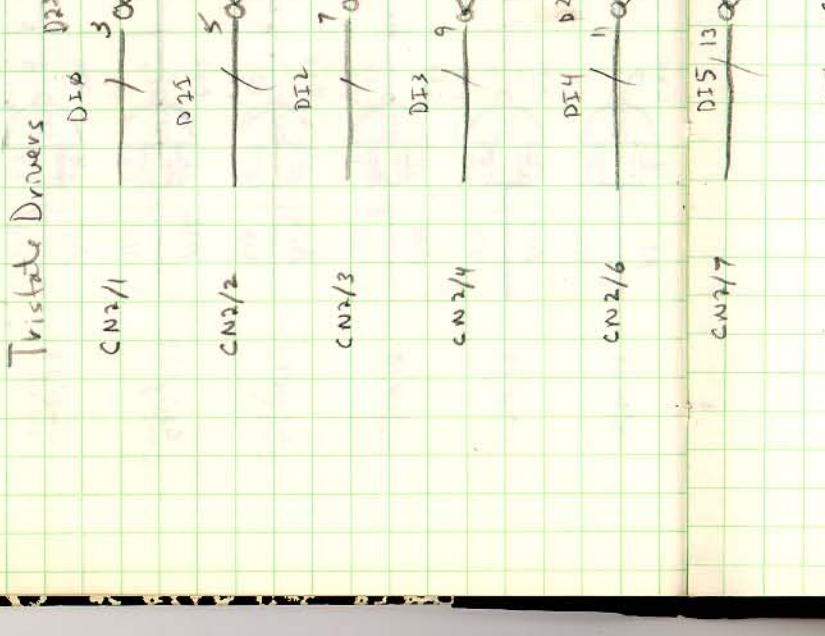
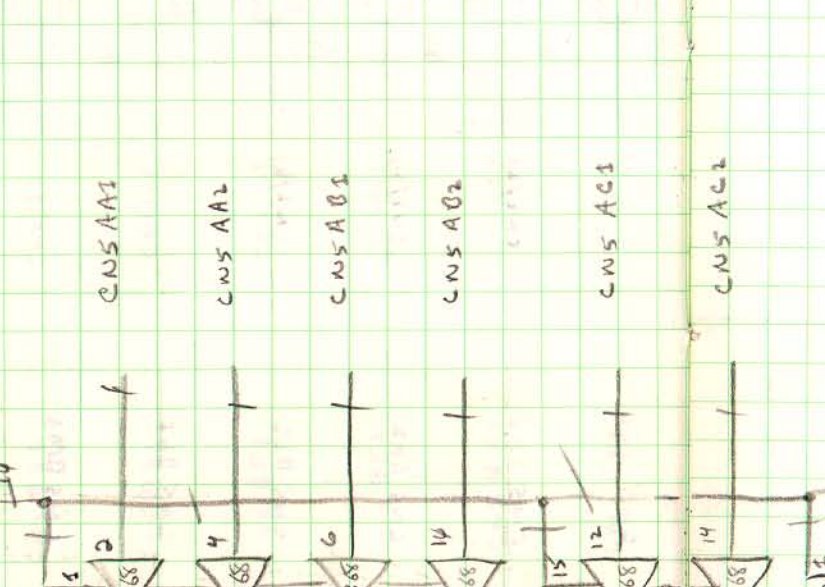
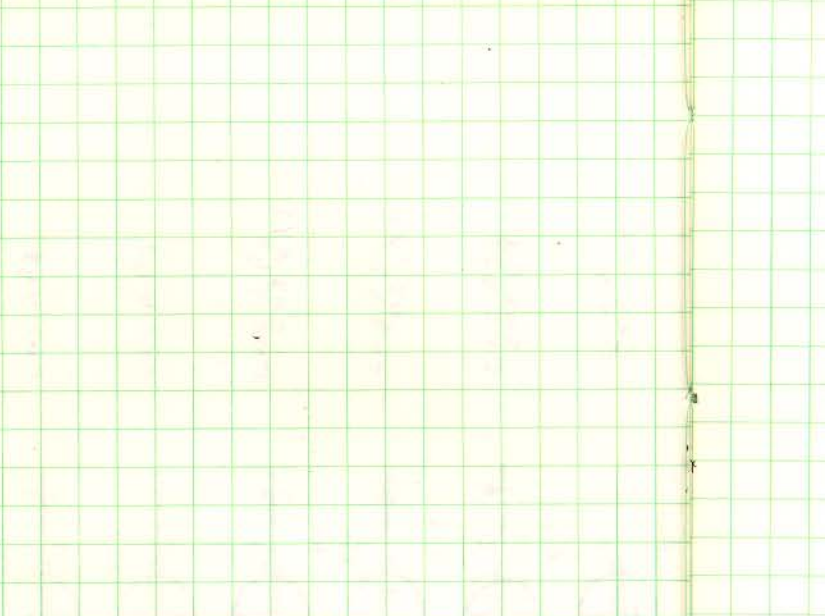
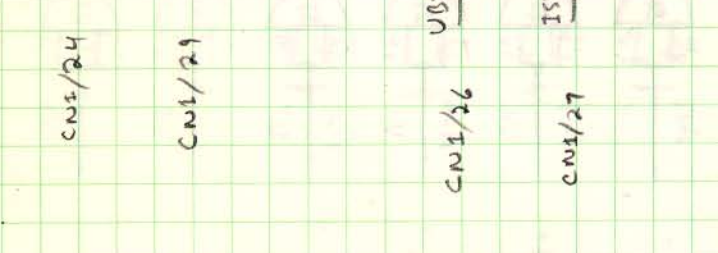
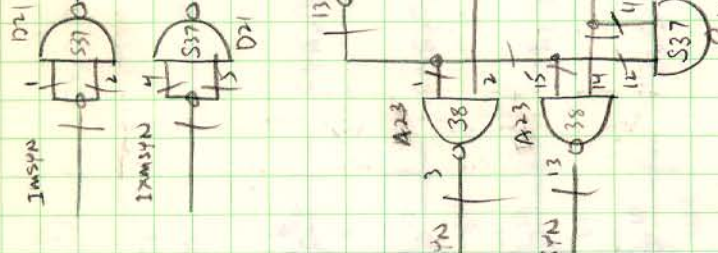
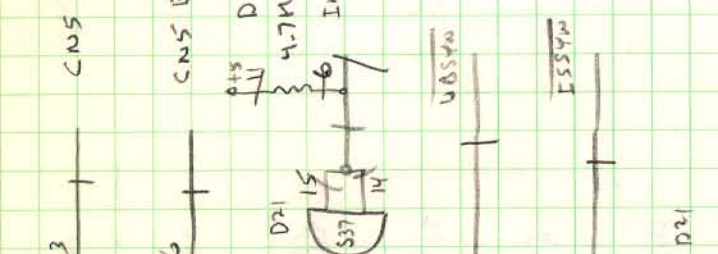
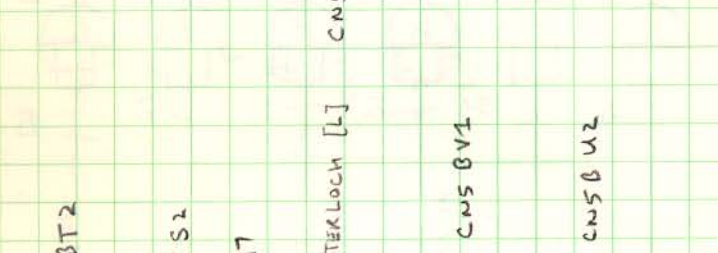
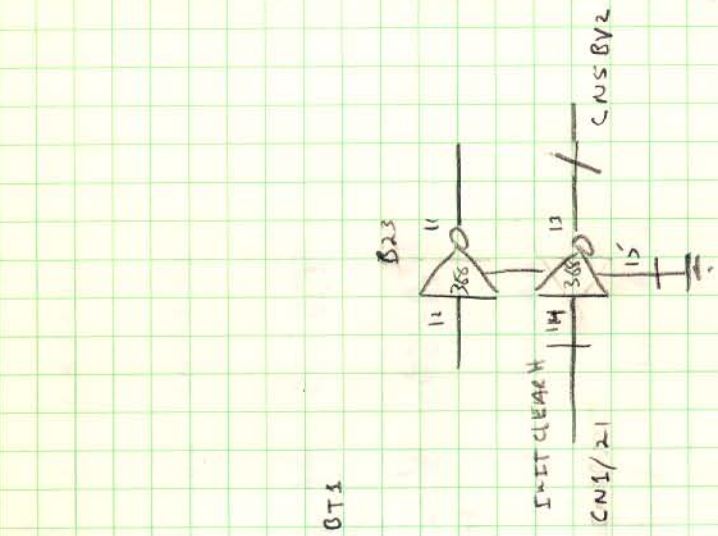
Internal BUS Buffer Logic

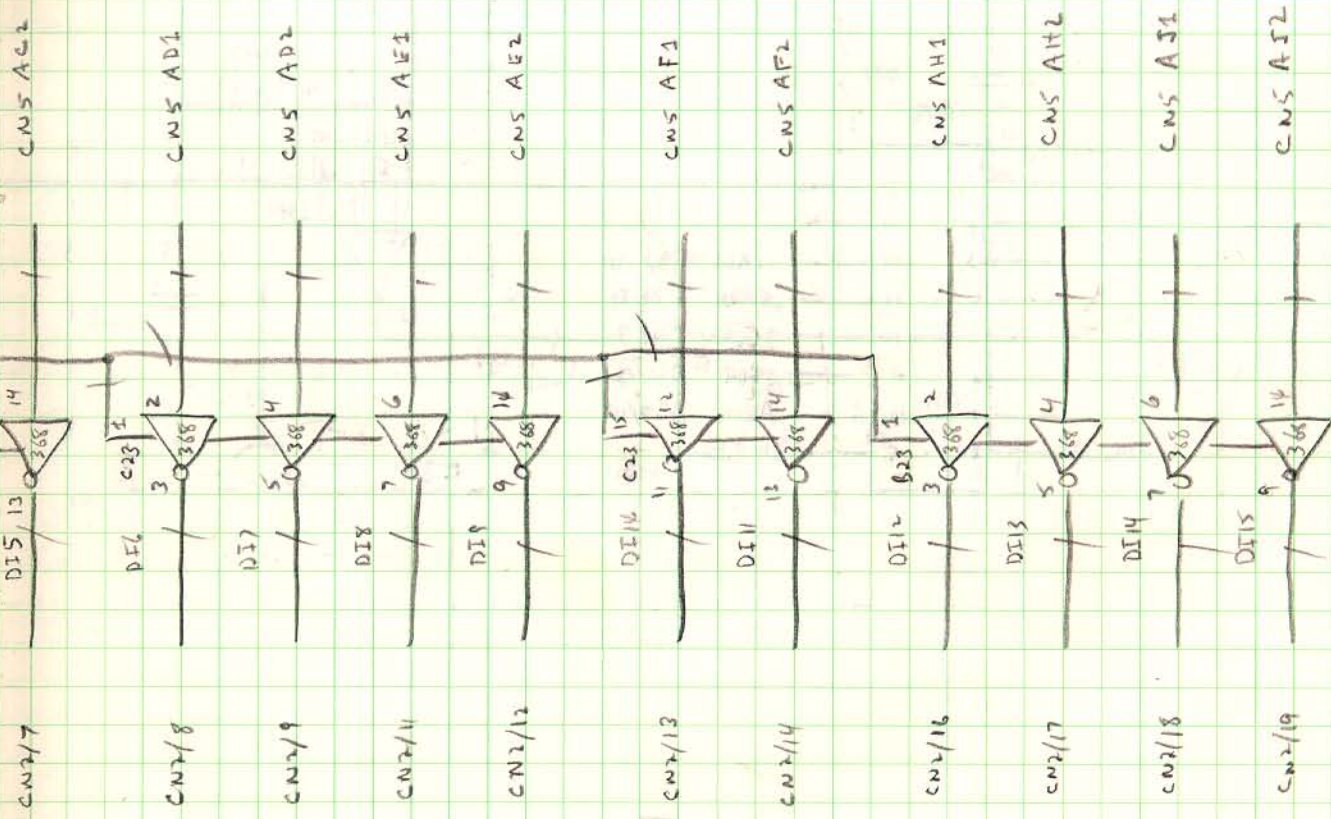




26 April 77
ABD

Interlock Bus Buffer Logic

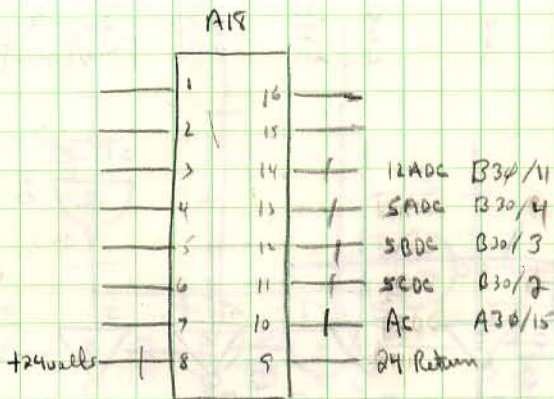
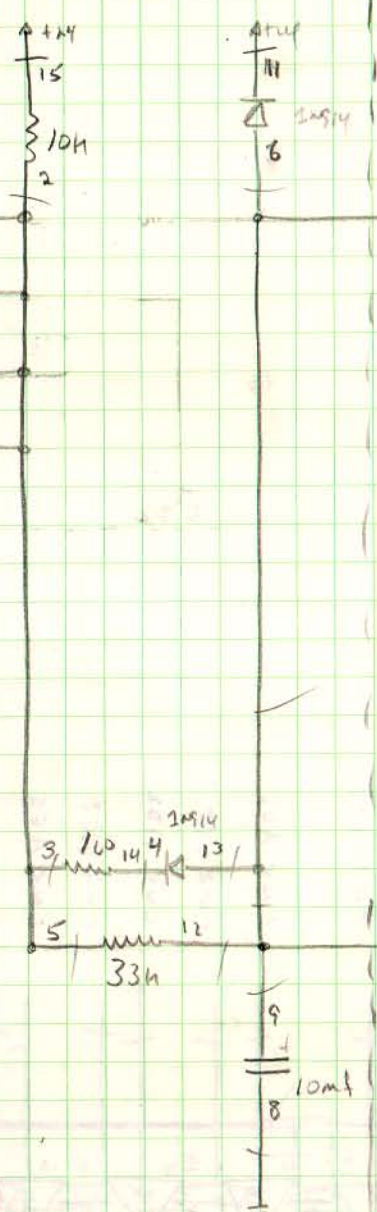
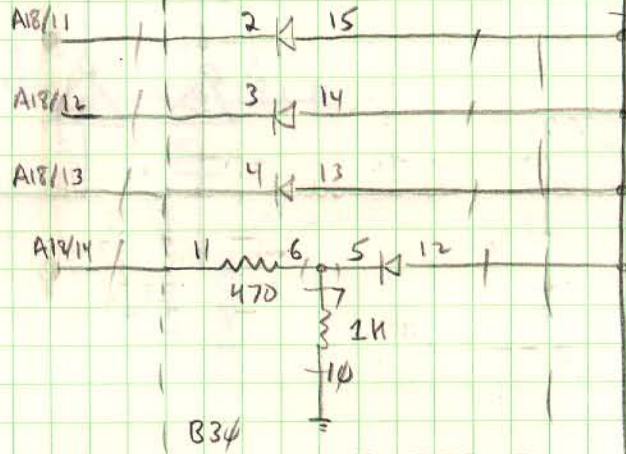




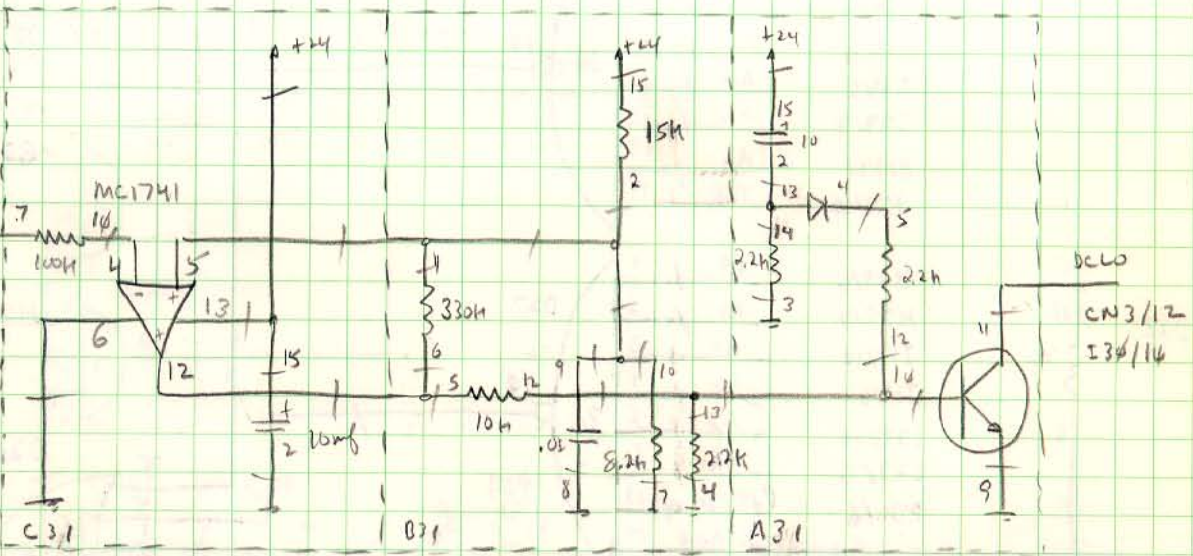
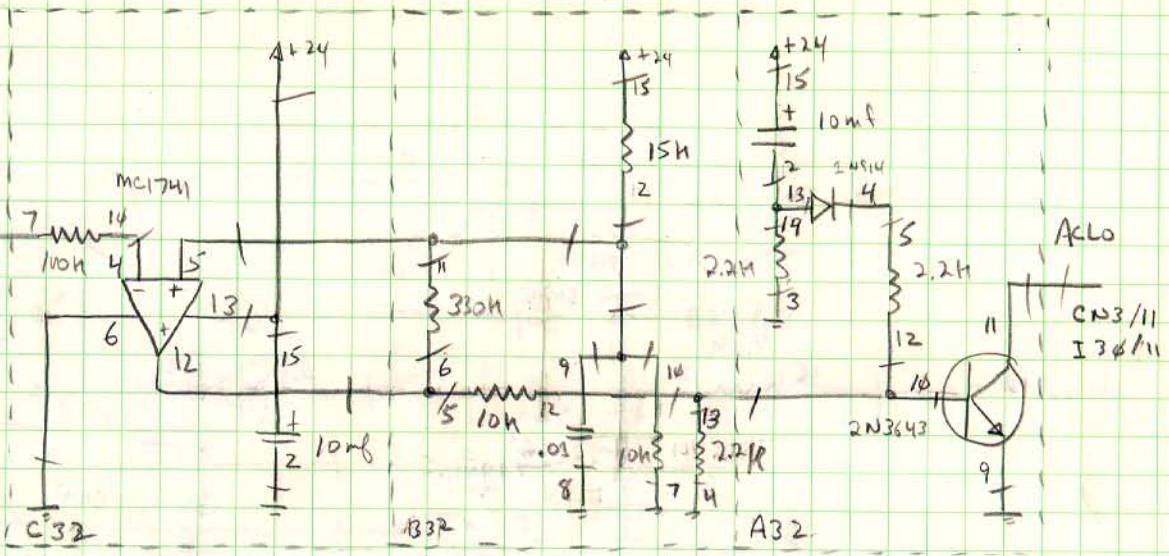
April 26 77
 ASD

AC/DC LO Sequence Logic

+5 Suppl
 +5 Suppl
 +5 Suppl
 +12, -12, -5 Suppl

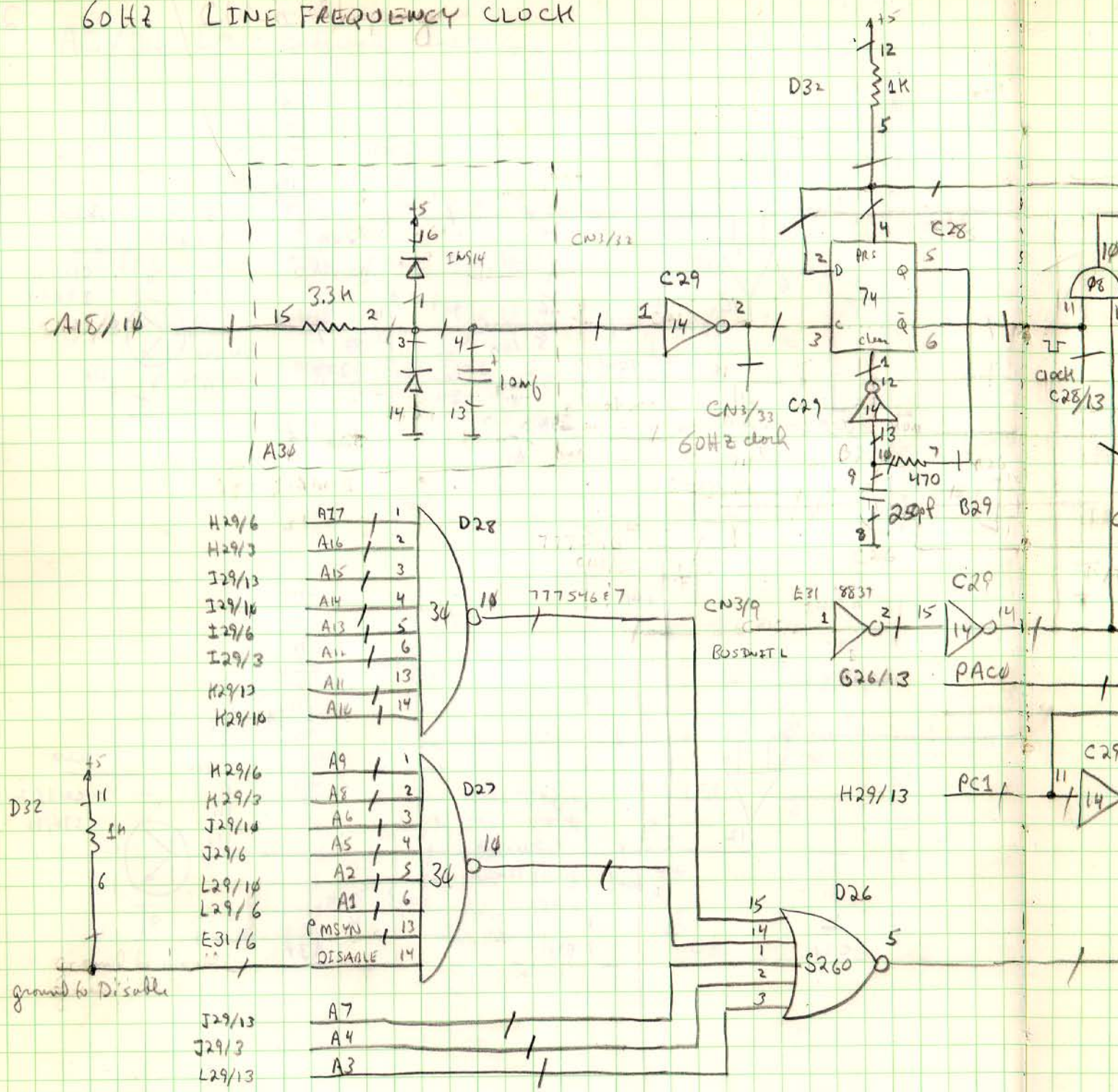


C34



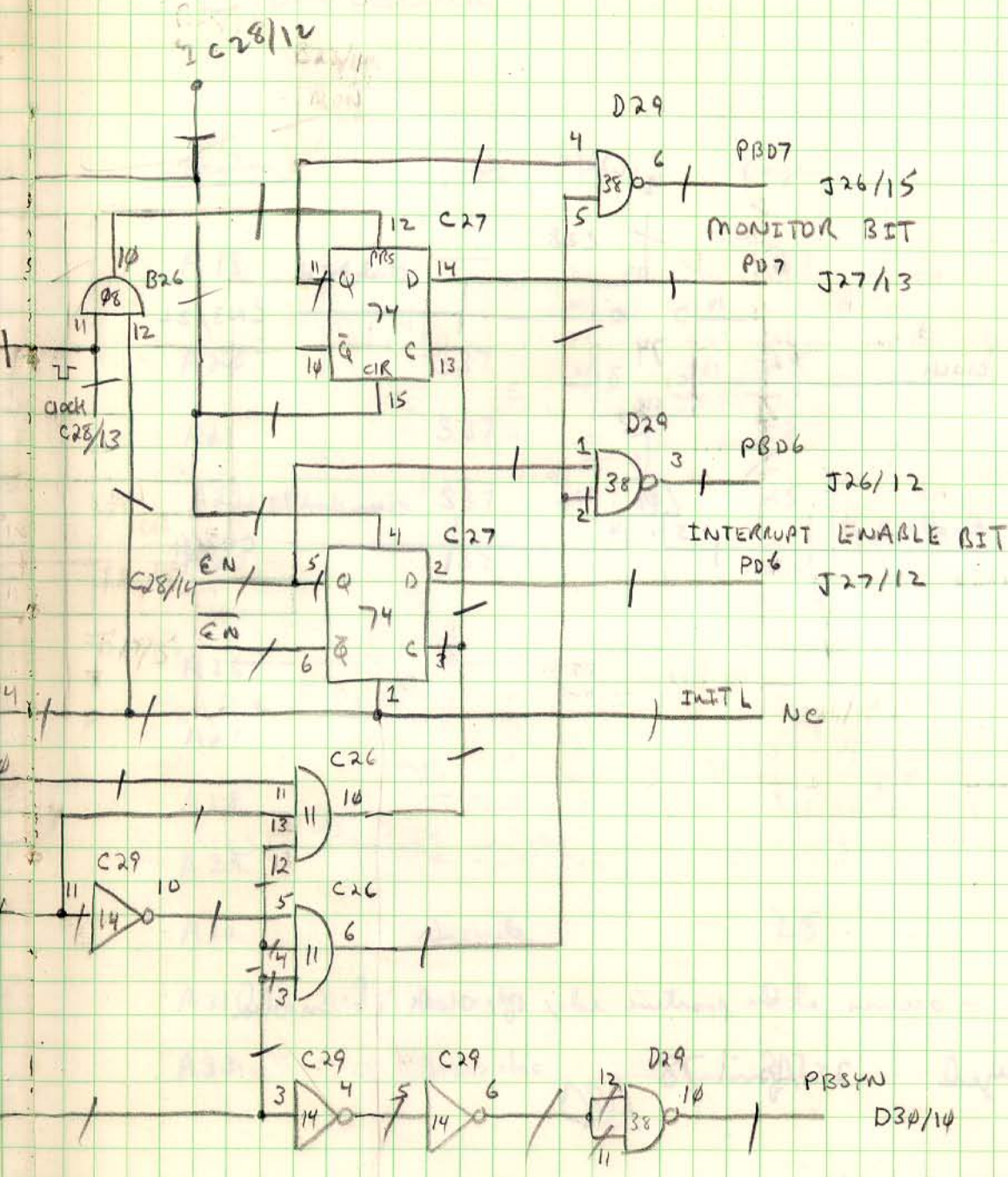
26 April 77
 ASD

60 Hz LINE FREQUENCY CLOCK



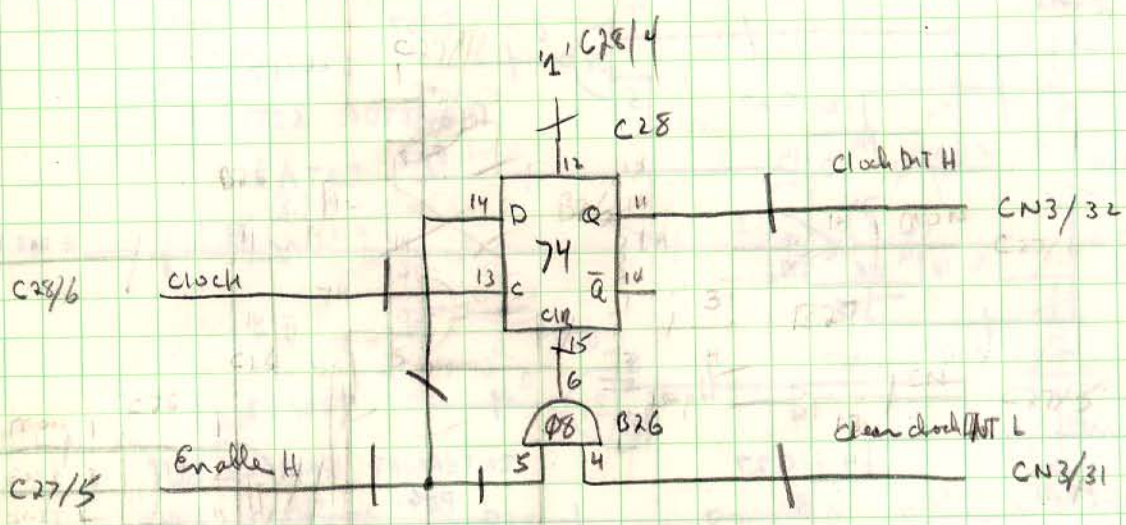
- H29/6 A17 / 1
- H29/3 A16 / 2
- J29/13 A15 / 3
- J29/14 A14 / 4
- J29/6 A13 / 5
- J29/6 A12 / 6
- J29/3 A11 / 13
- H29/13 A10 / 14
- H29/10 A9 / 1
- H29/6 A8 / 2
- H29/3 A6 / 3
- J29/14 A5 / 4
- J29/6 A2 / 5
- L29/14 A1 / 6
- L29/6 PMSYN / 13
- E31/6 DISABLE / 14
- J29/13 A7 / 1
- J29/3 A4 / 2
- L29/13 A3 / 3

25 Oct 1977
ARD



Changes in Clock
 25 April 78
 Changes in Clock
 12 March 78
 ASD

Line Frequency Clock Interrupt Sequencer



Clock Int H - occurs at the positive edge of clock if Enabled

finalized 25 April 78
 ARO

18 March 78
 ARO

Circuit Location

29

<u>Location</u>	<u>part</u>	<u>page</u>
A18	—	27
A20	S37	25
A21	S37	25
A22	S37	25
A23	38	26
A26	--	
A27	--	
A28	--	
A29	--	
A30	Discretes	28
A31	Discretes	27
A32	Discretes	27

<u>Location</u>	<u>Part #</u>	<u>Page</u>
B24	S37	25
B21	S37	25
B22	S37	25
B23	368	26
B26	74	29
B27	--	
B28	--	
B29	--	
B34	Discretes	27
B31	Discretes	27
B32	Discretes	27

<u>Location</u>	<u>Part #</u>	<u>Page</u>	
C24	S37	25	850
C21	S37	25	
C22	S37	25	
C23	368	26	
C26	11	28, 29	
C27	74	28	
C28	74	28	
C29	14	28	
C30	Discrete	27	
C31	Discretes	27	
C32	Discretes	27	

<u>Location</u>	<u>Part #</u>	<u>Page</u>
D17	Discretes	12
D18	--	
D19	38	12, 19
D20	--	
D21	S37	26
D22	S37	25
D23	368	26
D24		
D26	S260	28
D27	30	28
D28	30	28
D29	38	28
D30	38	12, 19
D31	38	19
D32	Discretes	19

<u>Location</u>	<u>Part #</u>	<u>Page</u>	<u>Notes</u>
E18	8837	12, 19	
E19	02	12	
E20	S44	12, 19	
E21	74	12	
E22	38	12	
E23	21	12, 19	
E26	74	12, 19	
E27	38	19	
E28	74	19	
E29	S44	19	
E30	02	19	
E31	8837	12, 19, 28	

<u>Location</u>	<u>Part #</u>	<u>Page</u>
G19	S133	18
G24	S260	11, 18
G21	11	18
G22	Discretes	12, 18
G23	Sφφ	18
G24	S139	11, 18
G25	φ4	11, 18
G26	Sφφ	11
G27	Discretes	11
G28	11	11
G29	28	11, 18
G34	S133	11

<u>Locales</u>	<u>Part #</u>	<u>Page</u>
H19	Terminator	22
H20	8838	21
H21	38	18, 20
H22	175	20
H23	04	15
H24	08	15
H25	08	15
H26	04	15
H27	175	13
H28	38	11, 13
H29	8838	14
H30	---	23

<u>Locales</u>	<u>Part "</u>	<u>page</u>
I19	Terminator	22
I20	8838	21
I21	38	24
I22	175	24
I23	8838	16, 17
I24	157	16, 17
I25	157	16, 17
I26	8838	16, 17
I27	175	13
I28	38	13
I29	8838	14
I30	---	23

LocationPart #page

J19	Terminator	22
J24	8838	21
J21	38	24
J22	175	24
J23	8838	16, 17
J24	157	16, 17
J25	157	16, 17
J26	8838	16, 17
J27	175	13
J28	38	13
J29	8838	14
J34	---	23

<u>Location</u>	<u>Part #</u>	<u>Page</u>
H19	Terminator	22
H20	8838	21
H21	38	24
H22	175	24
H23	8838	15, 16
H24	157	15, 16
H25	157	15, 16
H26	8838	15, 16
H27	175	13
H28	38	13
H29	8838	14
H30	---	23

<u>Location</u>	<u>Part #</u>	<u>Page</u>
L19	Terminator	22
L20	8838	21
L21	38	24
L22	175	24
L23	8838	15, 16
L24	157	15, 16
L25	157	15, 16
L26	8838	15, 16
L27	175	13
L28	28	13
L29	8838	14
L34	— —	23

Memory Management Logic

Unibus Map Logic

16 K x 16 Memory

Operational 26 April 78
ARD

26 Feb 78
ARD

E	RES	S157	RES	S157	RES	S157	RES	S157	RES	151	151	151	151	151	151	151	151
F	LS139	X	LS283	LS283	S21	S157	S157	S157	S157	151	151	151	151	151	151	151	151
G	93410	93410	93410	93410	93410	93410	93410	93410	93410	LS85	LS85	LS34	37	LS188	LS200	Res	Res
H	93410	93410	93410	93410	93410	93410	93410	93410	93410	X	LS86	LS16	32	8795	Res	Res	Res
I	X	93410	93410	93410	93410	X	RES	X	RES	X	X	X	18795	8795	Res	Res	Res
J	93410	93410	93410	93410	93410	93410	93410	93410	RES	X	X	X	18795	8795	Res	Res	Res
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Required 6 Aug 82 36

06 Feb 78
ARD

CN1

MMIO DATA IN/OUT

Pin	Label	Direction	Pin
1	MMIO0	+	A10/2
2		+	A10/5
3		+	A10/11
4		+	A10/14
5	GND		
6		+	A11/2
7		+	A11/5
8		+	A11/11
9		+	A11/14
10	GND		
11		+	A12/2
12		+	A12/5
13		+	A12/11
14		+	A12/14
15	GND		
16		+	A13/2
17		+	A13/5
18		+	A13/11
19	MMIO5	-	A13/14
20	GND		

Pin	Label	Direction	Pin
40	GND		
39	MMIO0	+	A10/4
38		+	A10/7
37		+	A10/9
36		+	A10/12
35	GND		
34		+	A11/4
33		+	A11/7
32		+	A11/9
31		+	A11/12
30	GND		
29		+	A12/4
28		+	A12/7
27		+	A12/9
26		+	A12/12
25	GND		
24		+	A13/4
23		+	A13/7
22		+	A13/9
21	MMIO5	+	A13/12

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20

CN2

1		24	GND
2		23	
3		22	
4		21	
5		20	
6	GND	19	
7		18	GND
8		17	
9		16	
10		15	
11		14	
12	GND	13	

1
2
3
4
5
6
7
8
9
10
11
12

1	MMBT C0	+	B9/14	40	GND
2	MMBT C1	+	B9/2	39	PSR8 - C3/3
3	MMBT C2	+	C9/2	38	PSR9 + C3/2
4	MMBT ReadyH	+	C11/10	37	PSR10 + C3/5
5	GND			36	PSR11 + C3/6
6	MM2 WLB	+	A9/4	35	GND
7	MM2 WLB	+	A9/12	34	PSR12 + A9/14
8	MM2 Read	+	D16/4	33	PSR13 + A9/15
9	MMBT GOL	+	B10/5	32	PSR14 + A9/2
10	GND			31	PSR15 + A9/3
11	MM2 WLB	+	B6/9	30	GND
12	MM2 WLB	+	D8/9	29	INIT CLEAR L + A3/1
13	MM2 Read	+	D16/3	28	XL + B11/2
14	MMBT ERL	+	C9/11	27	XH + B11/3
15	GND			26	XA + B11/6
16	MM2 WLB	-		25	GND
17	MM2 WLB	-		24	MMBT ENH + C10/15
18	MM2 Read	+	D16/2	23	
19	GOL	+	B10/2	22	
20	GND			21	MMBT INET - NC

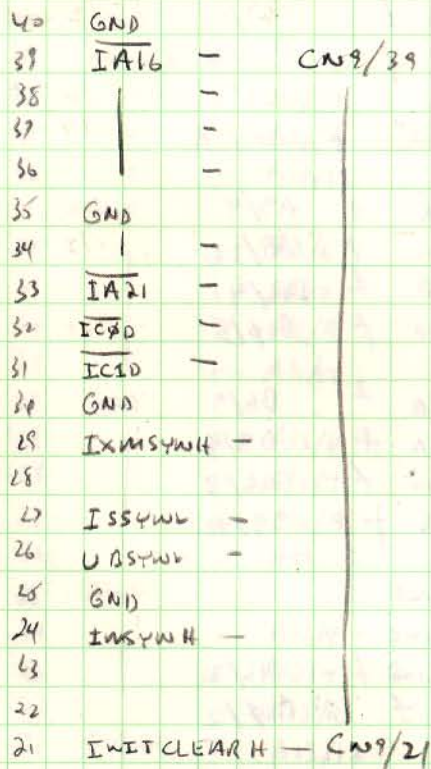
CN8

UNIBUS MAP / mmbt Extra's

1	UBA18	+	C26/6	24	GND
2	UBA19	+	C26/10	23	
3	UBA20	+	D26/6	22	
4	UBA21	+	D26/10	21	
5	UMDFL	- NC		20	
6	GND			19	
7				18	GND
8				17	
9	CID (DATA0)	+	B10/15	16	AD-BUS L + D25/1
10	DATA R H	+	D9/11	15	
11	DATA L	+	H12/1	14	
12	GND			13	

CN3

INTERNAL BUS Address OUT



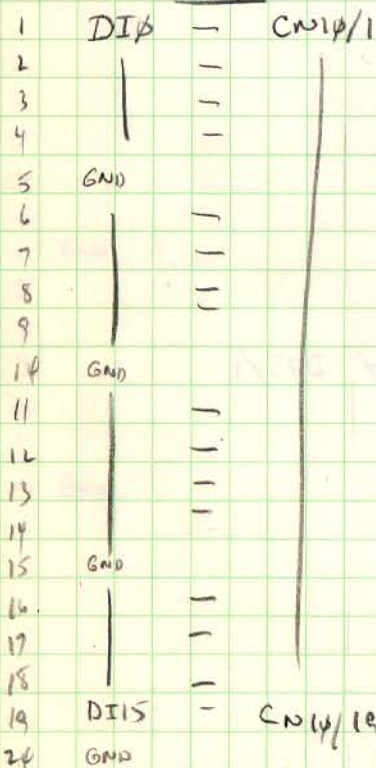
CN4
To CPU

INTERNAL BUS

Data

OUT/in

(away from CPU)



Pin	Signal	Direction	Address	Pin	Signal	Direction	Address
1	IA4	-	A17/2	40	GND	-	
2		-	A17/3	39	IA16	-	B18/5
3		-	A17/6	38		-	B18/1
4		-	A17/7	37		-	B17/15
5	GND	-		36		-	B17/11
6		-	A18/2	35	GND	-	
7		-	A18/3	34		-	B17/5
8		-	A18/6	33	IA21	-	B17/3
9		-	A18/7	32	ICAD	-	
10	GND	-		31	ICAD	-	
11		-	A19/2	30	GND	-	
12		-	A19/3	29	INMSYAL	-	A21/3
13		-	A19/6	28		-	
14		-	A19/7	27	ISSYAL	-	B14/16
15	GND	-		26	UASPYAL	-	B14/6
16		-	A20/2	25	GND	-	
17		-	A20/3	24	INMSYAL	-	A21/1
18		-	A20/6	23		-	
19	IA15	-	B18/11	22		-	
20	GND	-		21	INIT CLEAR KH	-	CN3/21 - NE

CN16

INTERNAL BUS

DATA

IN/OUT

(toward CPU)

Pin	Signal	Direction	Address	Pin	Signal	Direction	Address
1	DI4	-	A22/3	40	GND	-	
2		-	A22/5	39	DO4	-	B21/2
3		-	A22/7	38		-	B21/3
4		-	A22/9	37		-	B21/6
5	GND	-		36		-	B21/7
6		-	A22/11	35	GND	-	
7		-	A22/13	34		-	B22/2
8		-	A23/3	33		-	B22/3
9		-	A23/5	32		-	B22/6
10	GND	-		31		-	B22/7
11		-	A23/7	30	GND	-	
12		-	A23/9	29		-	B23/2
13		-	A23/14	28		-	B23/3
14		-	A23/13	27		-	B23/6
15	GND	-		26		-	A23/7
16		-	A24/3	25	GND	-	
17		-	A24/5	24		-	B24/2
18		-	A24/7	23		-	B24/3
19	DI5	-	A24/9	22		-	B24/6
20	GND	-		21	DO15	-	B24/7

26 Feb 78
ARD

FS CNS UNIBUS Control (OUT)

Pin	Label	Connection	Pin	Label	Connection	Pin
1	BA4	- CN11/1	40	GND		1
2	BA5	-	39	B64	- CN11/39	2
3	BA6	-	38	B65	-	3
4	BA7	-	37	B66	-	4
5	GND		36	B67	-	5
6	NPR	-	35	GND		6
7			34	NPG	-	7
8			33			8
9	INET	-	32	LINE FRAGMENT INT	-	9
10	GND		31	Line Frag. clock CLR	-	10
11	ACLO	-	30	GND		11
12	DCLO	-	29	INTR	-	12
13			28	SACK	-	13
14	BSSYNL	- CN11/14	27	PB0	-	14
15	GND		26	PBI	-	15
16	BMSYNL	+ A28/15	25	GND		16
17		CN11/17	24	C0L	-	17
18			23	C1L	- CN11/23	18
19	BBSY	- CN11/19	22	A16L	+ A28/1	19
20	GND		21	A17L	+ A28/4	20

CN6 UNIBUS DATA/Address

Pin	Label	Connection	Pin	Label	Connection	Pin
1	D0L	- CN12/1	40	GND		1
2		-	39	A0L	- A29/1	2
3		-	38		- A29/4	3
4		-	37		- A29/12	4
5	GND		36		- A29/15	5
6		-	35	GND		6
7		-	34		- A30/1	7
8		-	33		- A30/4	8
9		-	32		- A30/12	9
10	GND		31		- A30/15	10
11		-	30	GND		11
12		-	29		- A31/1	12
13		-	28		- A31/4	13
14		-	27		- A31/12	14
15	GND		26		- A31/15	15
16		-	25	GND		16
17		-	24		- A32/1	17
18		-	23		- A32/4	18
19	DISL	- CN12/19	22		- A32/12	19
20	GND		21	A15L	- A32/15	20

CN11 UNIBUS - CONTROL (IN)

40

1	BR4	-	CNS/1	40	GND	
2	BR5	-		39	B64	- CNS/39
3	BR6	-		38	B65	-
4	BR7	-		37	B66	-
5	GND			36	B67	-
6	NPR	-		35	GND	
7				34	NPG	-
8				33		
9	INIT	-		32	LINE FREQ CLOCK INT# -	
10	GND			31	Line Freq Clock Clear -	
11	ACLO	-		30	GND	
12	DCLO	-		29	INTA	-
13				28	SACK	-
14	BSSPWL	-		27	P00	-
15	GND		26	P01	-	
16	BMSPWL	+ B28/15	25	GND		
17		CNS/17	24	C0L	-	
18			23	C1L	- CNS/23	
19	BSY	- CNS/19	22	A16L	+ B28/11	
20	GND		21	A17L	+ B28/4	

CN12 UNIBUS DATA/ADDRESS

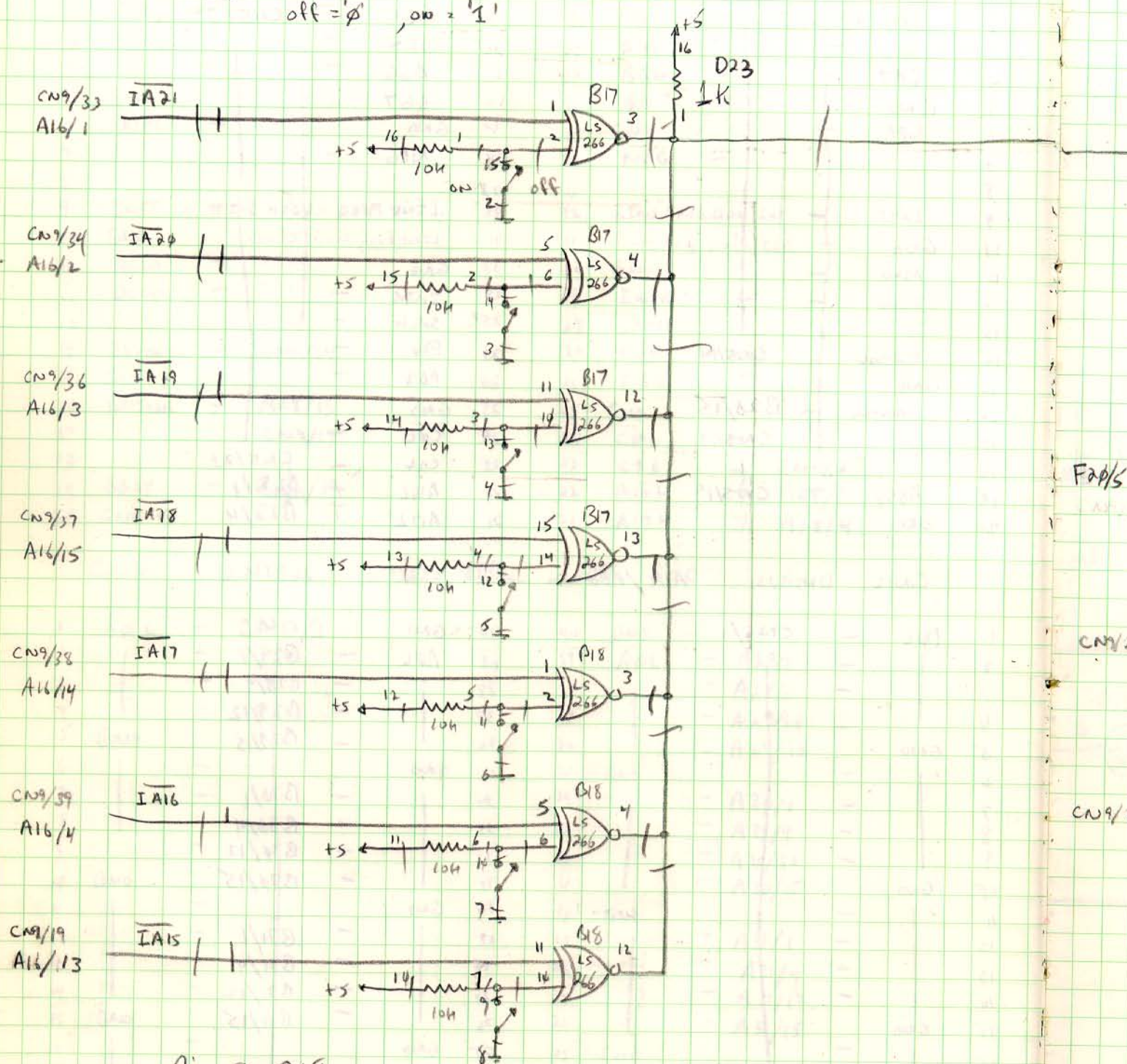
1	D0L	-	CN6/1	40	GND			
2		-		39	A0L	- B29/1		
3		-		38		- B29/4		
4		-		37		- B29/12		
5		GND			36		- B29/15	
6				-	35	GND		
7				-	34		- B30/1	
8				-	33		- B30/4	
9				-	32		- B30/12	
10				GND		31		- B30/15
11					-	30	GND	
12					-	29		- B31/1
13					-	28		- B31/4
14					-	27		- B31/12
15	GND				26		- B31/15	
16		-	25	GND				
17		-	24		- B32/1			
18		-	23		- B32/4			
19		D15L	- CN6/19	22		- B32/12		
20		GND		21	A15L	- B32/15		

27 Feb 78
ABD

16 K Memory

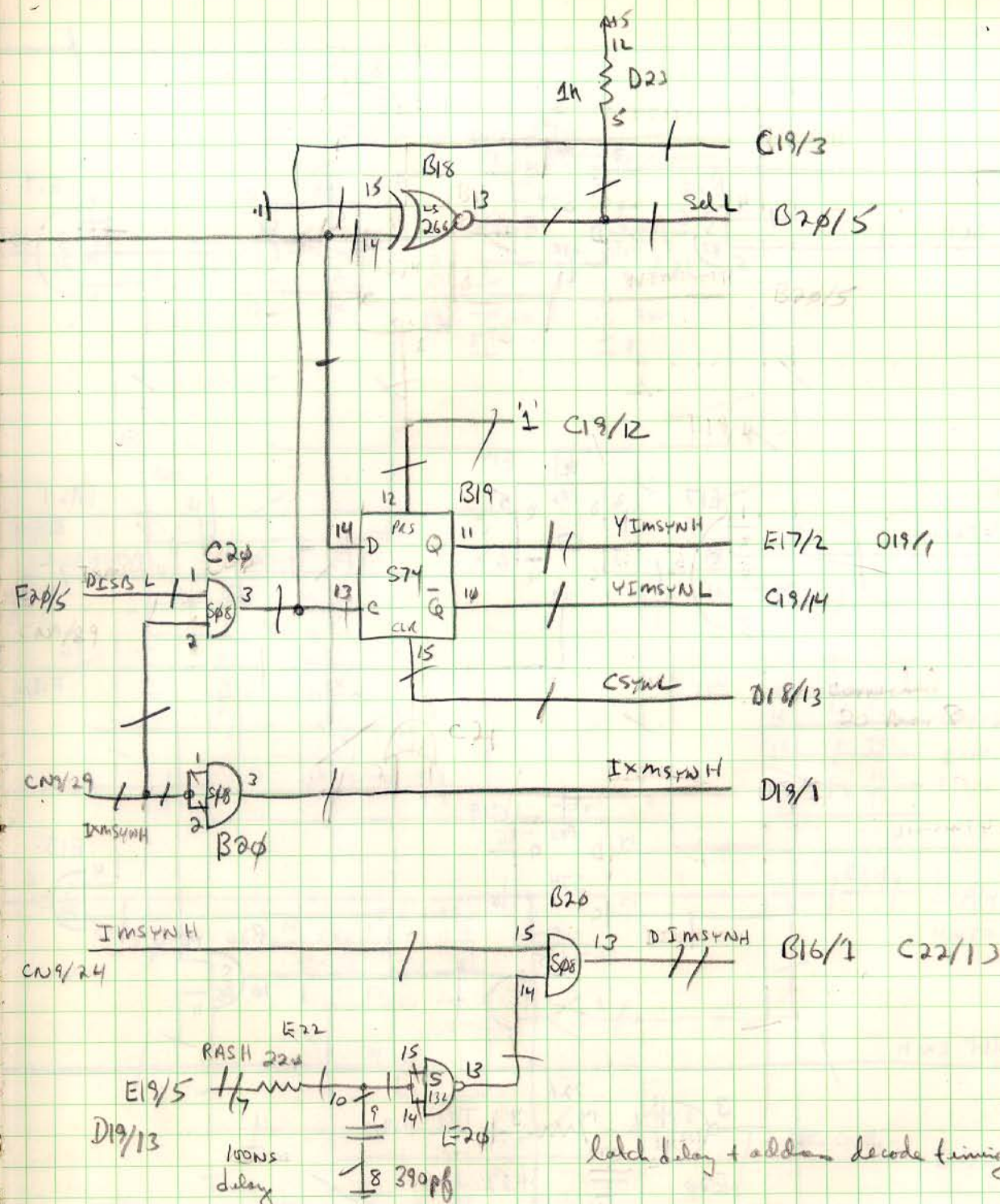
Address Selector

off = '0', on = '1'



R's @ C18
Switches @ C17

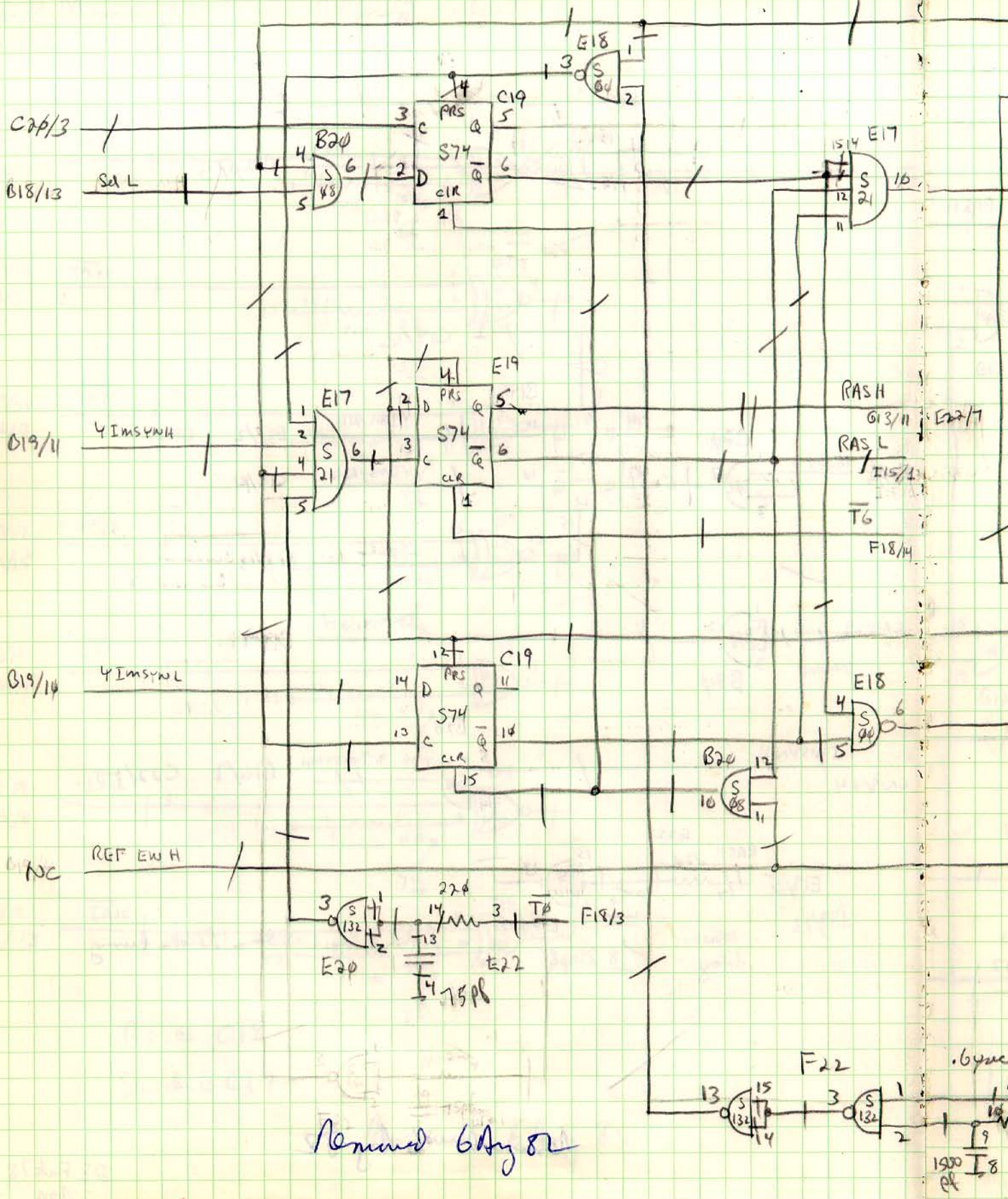
Revised 6 Aug 81



latch delay + address decode timing

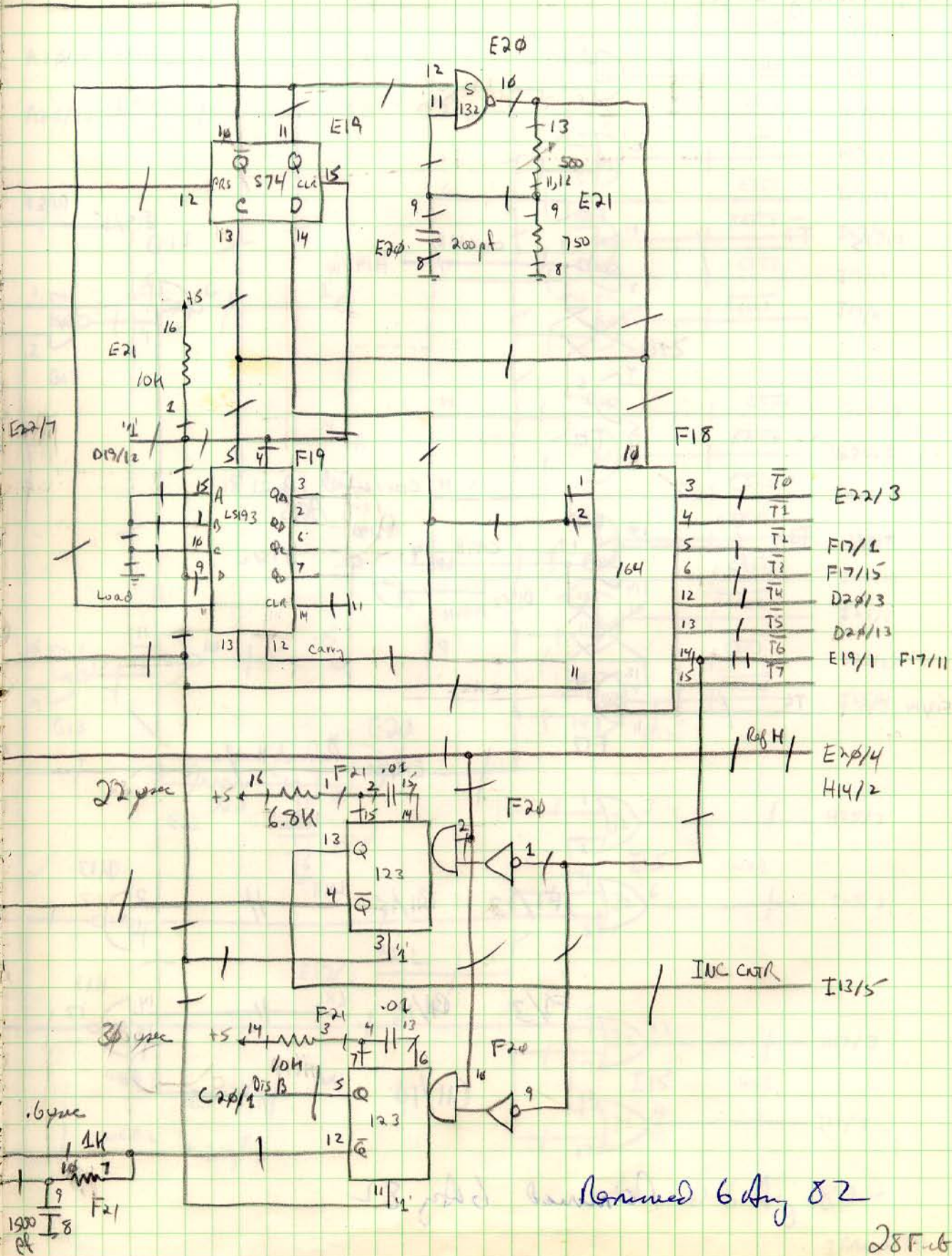
Revised 6 Aug 82

28 Feb 78
ARB



Removed 6 by 82

.6µsec
1500 pF

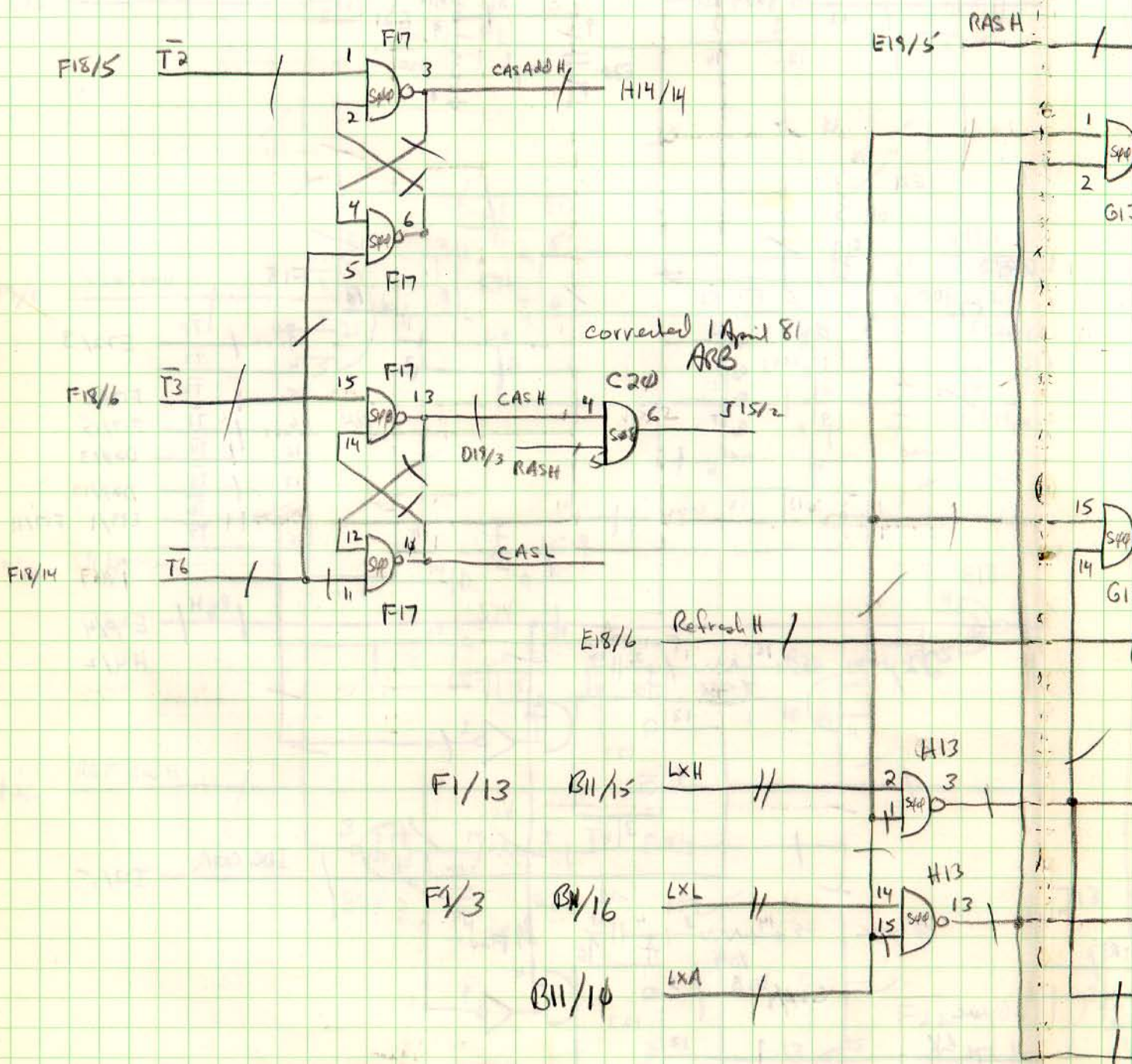


Revised 6 Aug 82

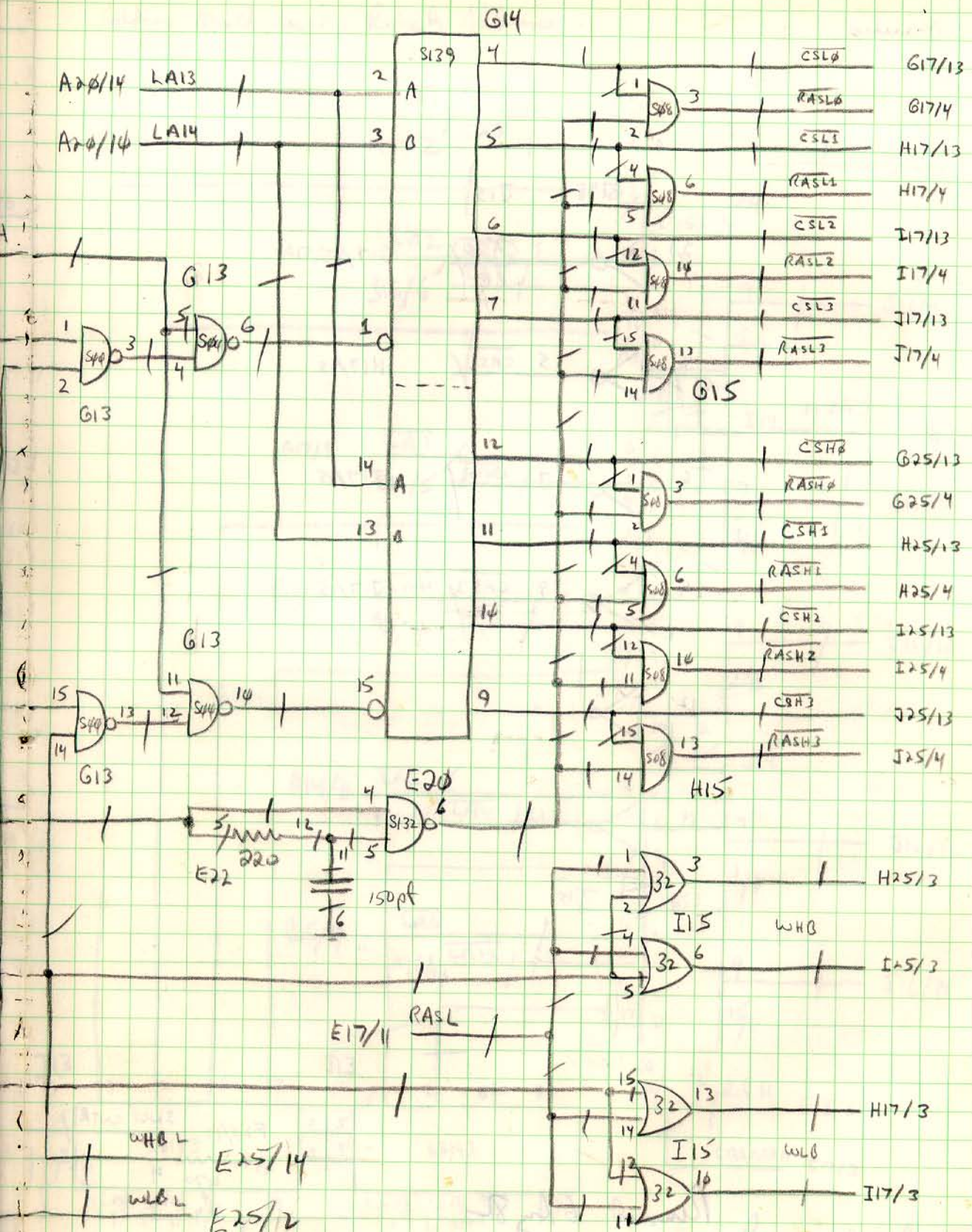
28F-678
ARD

Memory Timing Logic

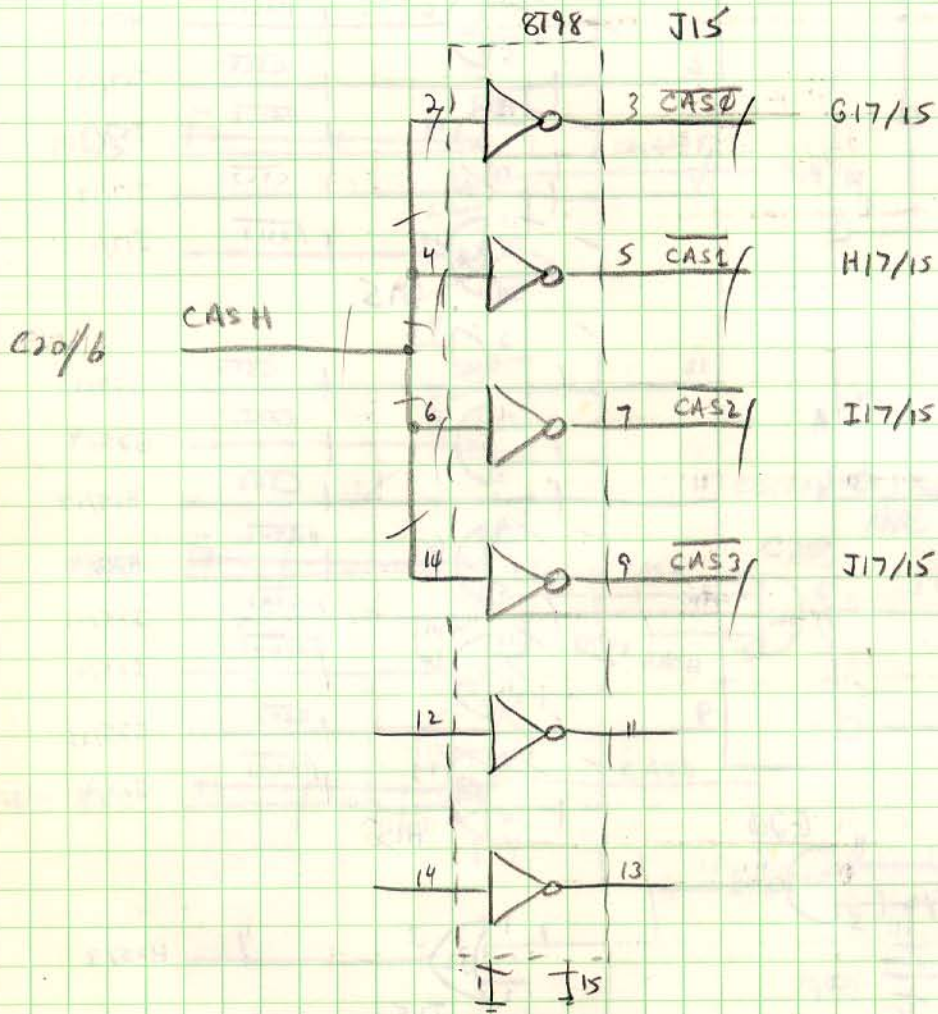
Arb/1
Arb/1



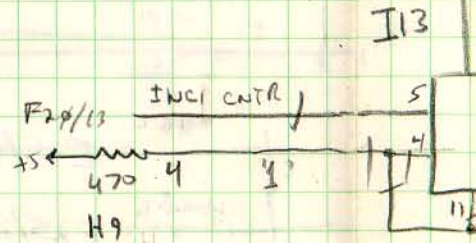
Revised 6 Aug 82



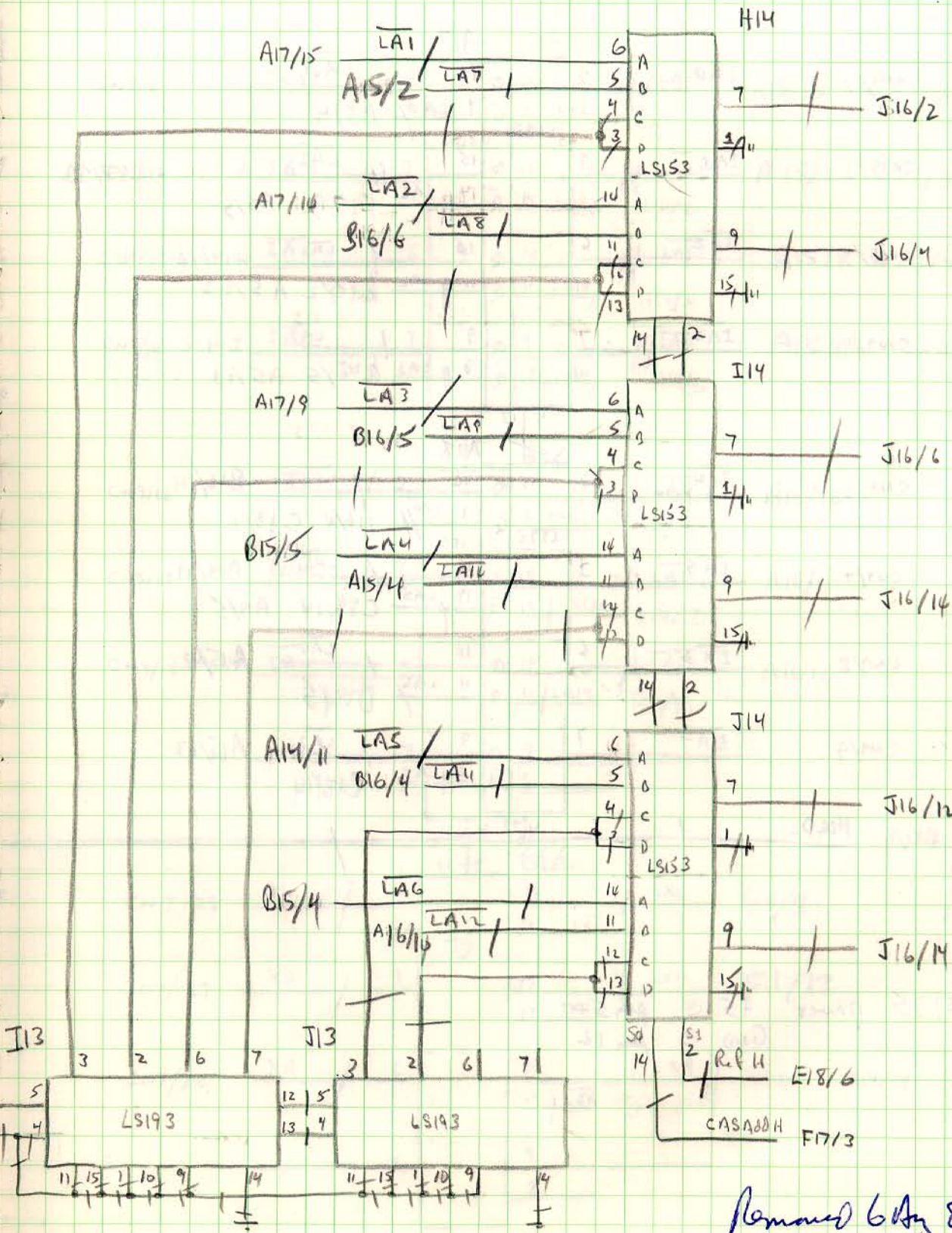
Revised 6 Aug 82
 1 March 78
 APO



Revised 6 Aug 82



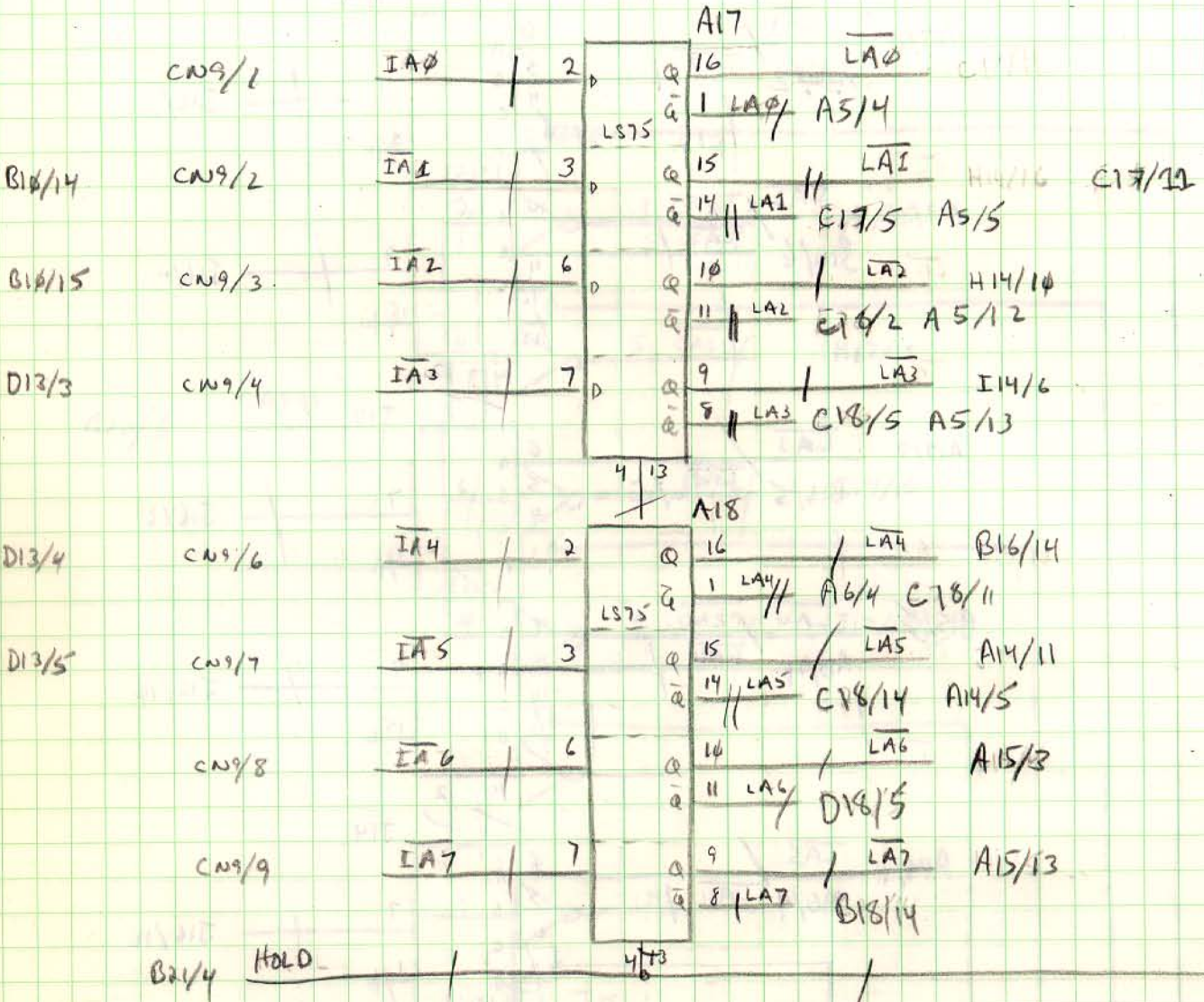
Address Multiplexer / Refresh Address



Removed 6 Aug 82

1 March 78
ADD

Transparent Address/Control Latches



74(LS)75 power +5 @ pin 5
 GND @ pin 12

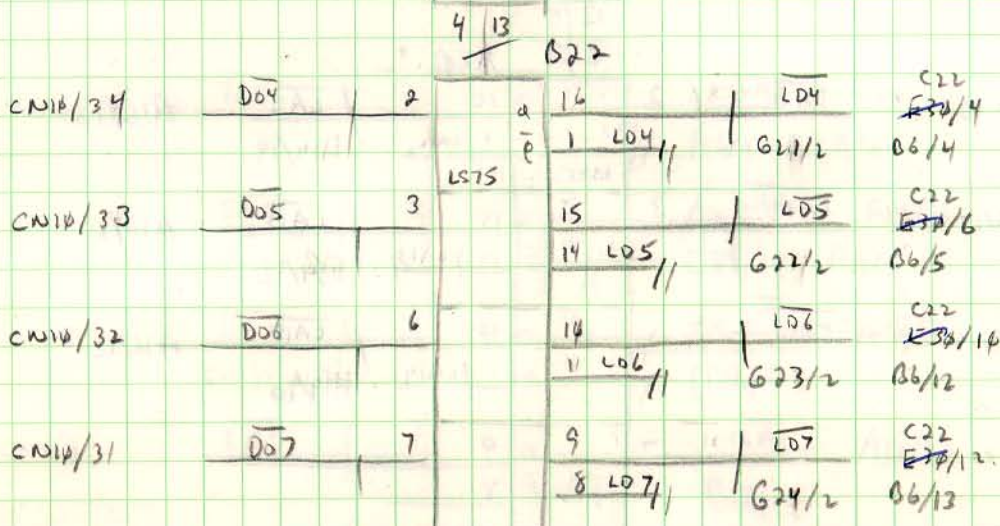
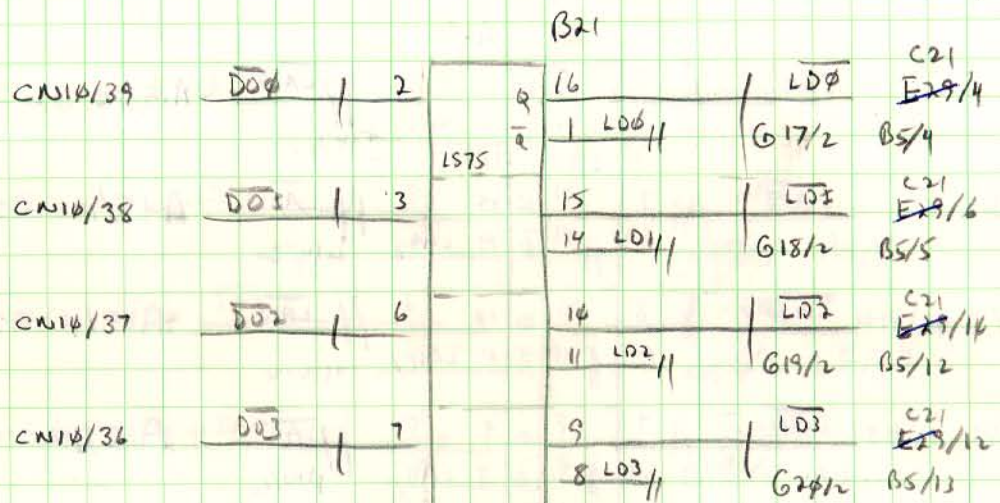
		A19			
CN9/11	IA8 / 2	16	11 LA8	A15/14	C22/6
		1	LA8		
			I14/10		
CN9/12	IA9 / 3	15	11 LA9	A15/11	C22/5
		14	LA9		
			H14/2		
CN9/13	IA10 / 6	14	11 LA10	A15/11	C22/4
		11	LA10		
			H14/4		
CN9/14	IA11 / 7	9	11 LA11	A15/12	C22/3
		8	LA11		
			H14/6		
		13	4		

		A20			
CN9/16	IA12 / 2	16	11 LA12	A16/10	
		1	LA12		
			H14/14		
CN9/17	IA13 / 3	15	11 LA13	A16/11	
		14	LA13		
			H14/12		
CN9/18	IA14 / 6	14	11 LA14	A16/12	
		11	LA14		
			H14/10		
NC		9			
		8			
		12	4		

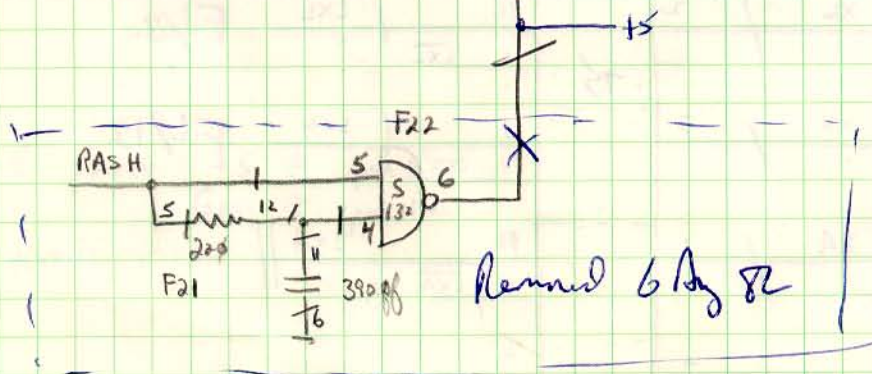
		B11			
CN7/28	XL / 2	16	11 LXL	F1/3	
		1	LXL		
CN7/27	XH / 3	15	11 LXH	F1/13	
		14	LXH		
CN7/26	XA / 6	10	11 LXA	A14/14	
		11	LXA		
NC		9			
		8			
		12	4		

1/6 = 4
 5/6
 1.6
 9.6
 14
 + 60
 2000

Transparent Data Latches



A20/113 HOLD / 4/13



7045

		B23			
CN18/29	D08	2	16	L08	C23 EST/4 07/4
			1	L08//	625/2
		LS75			
CN18/28	D09	3	15	L09	C23 EST/6 07/5
			14	L09//	626/2
CN18/27	D014	6	10	L014	C23 EST/14 07/12
			11	L014//	627/2
CN18/26	D011	7	9	L011	C23 EST/12 07/13
			8	L011//	628/2

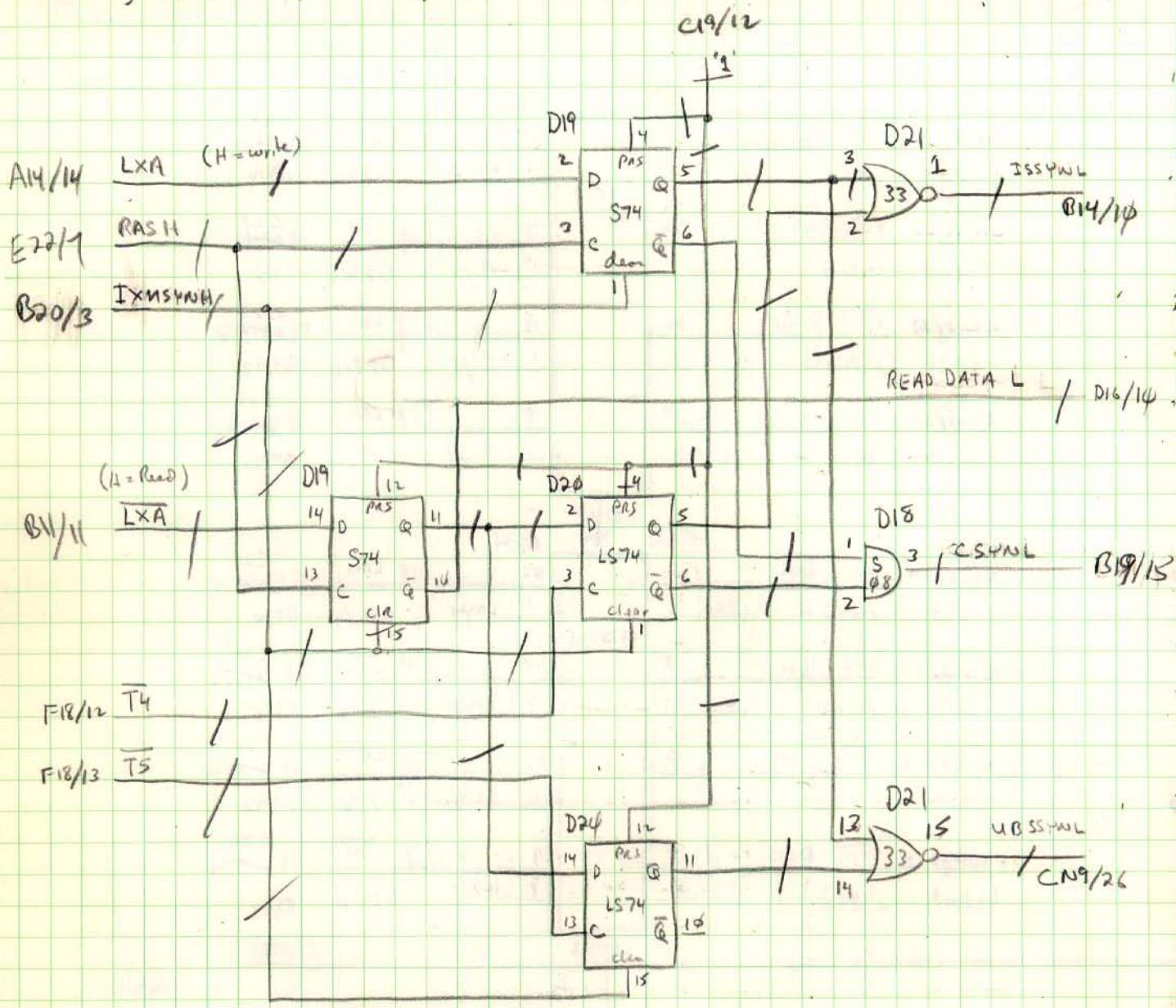
4/13

		B24			
CN18/24	D012	2	16	L012	C24 EST/4 08/4
			1	L012//	629/2
		LS75			
CN18/23	D013	3	15	L013	C24 EST/6 08/5
			14	L013//	630/2
CN18/22	D014	6	10	L014	C24 EST/14 08/12
			11	L014//	631/2
CN18/21	D015	7	9	L015	C24 EST/12 08/13
			8	L015//	632/2

4/13

Handwritten signature or note at the bottom of the page.

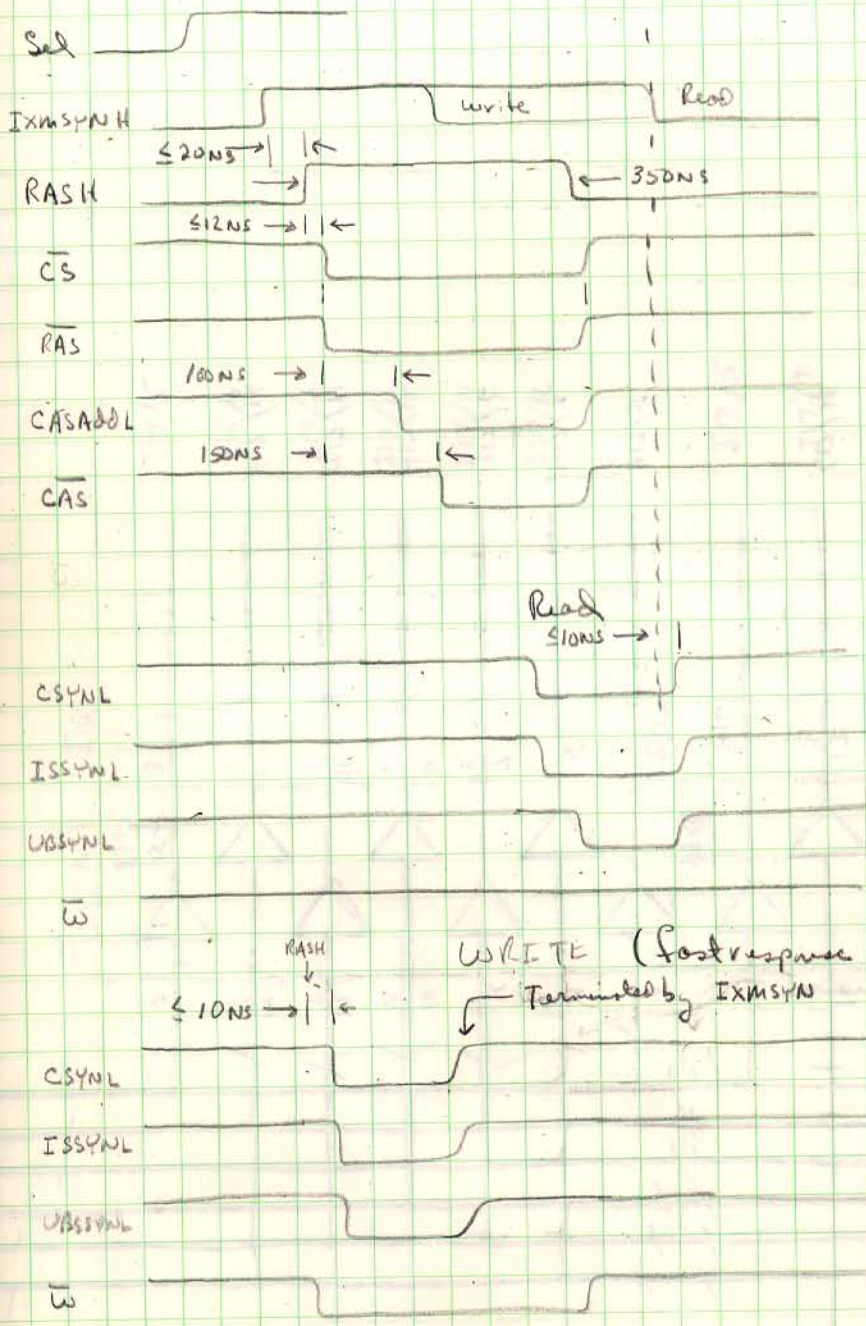
Memory BUS Response Logic



Remained 6 Aug 82

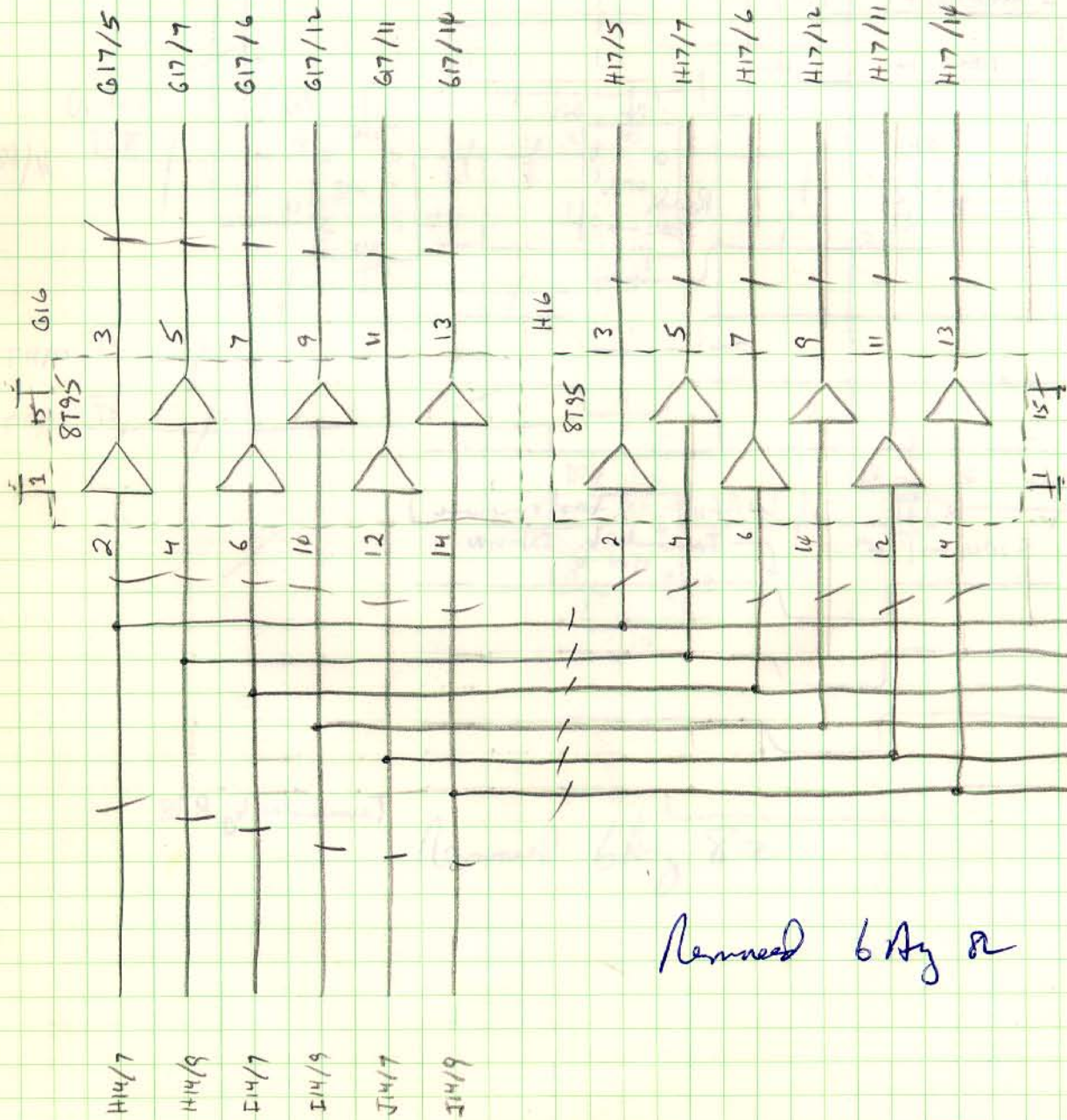
Simplified Timing Diagrams

READ / write

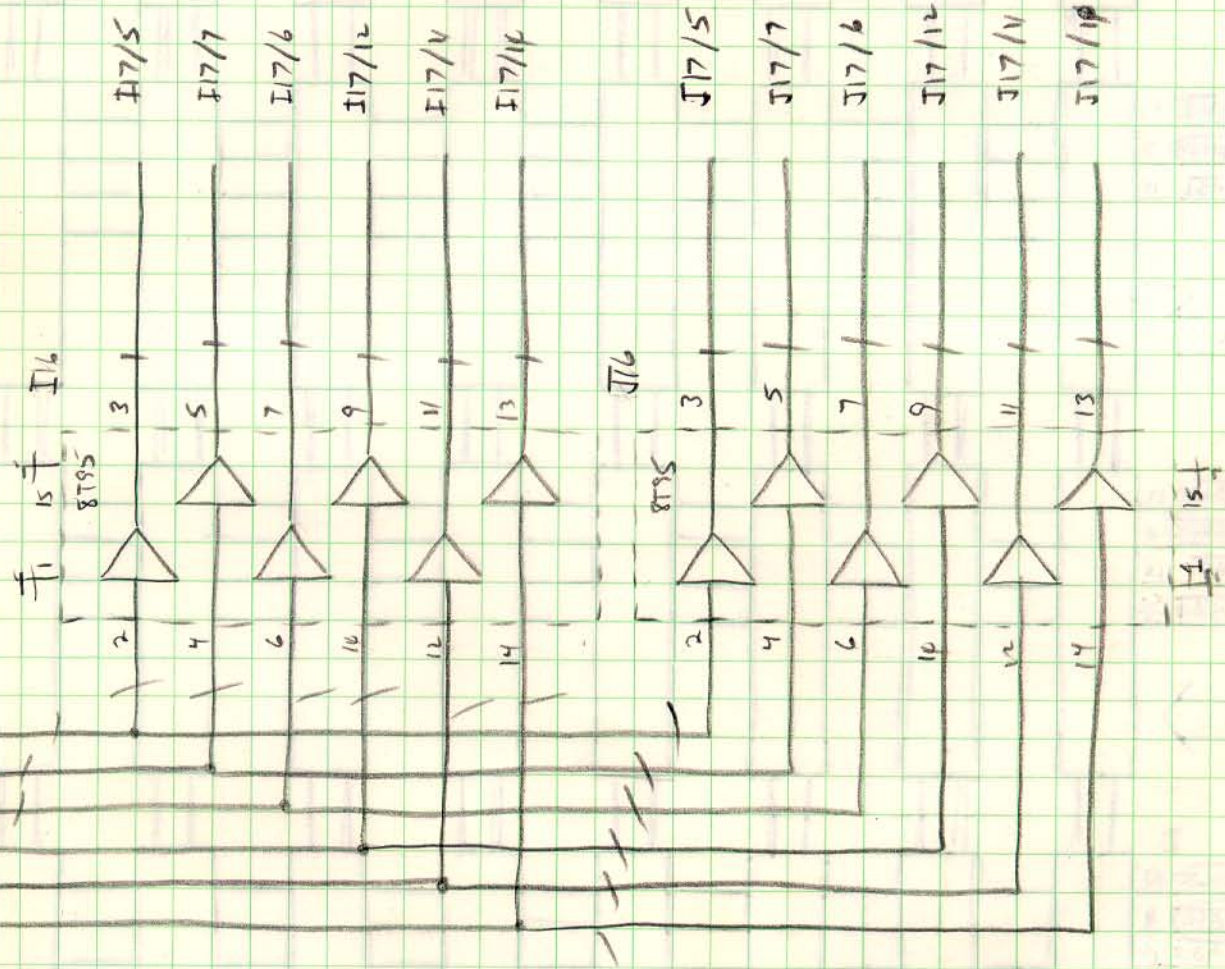


1 March 78
ARD

Memory Address Drivers



Remmed by a

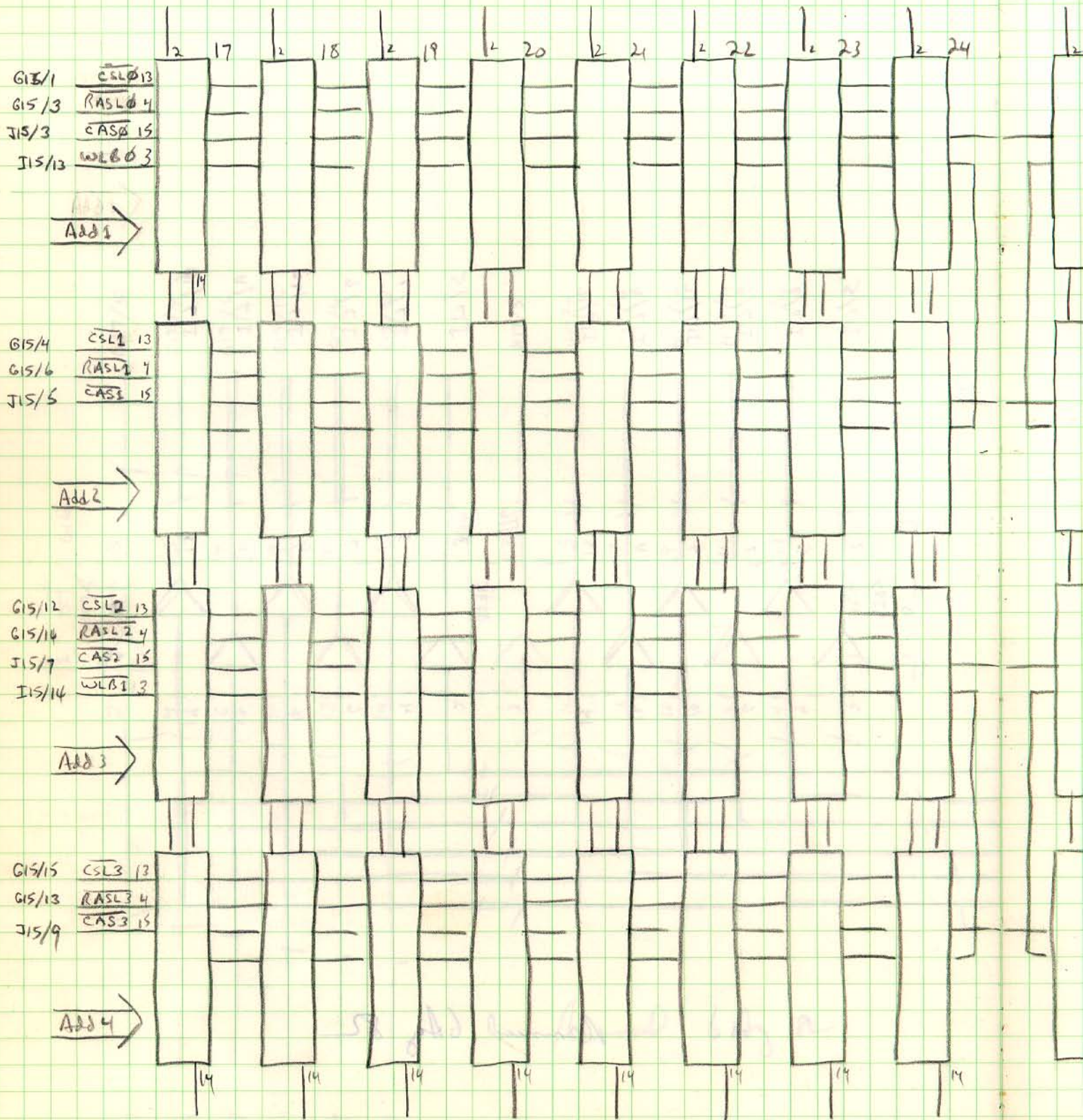


Revised 6 Aug 82

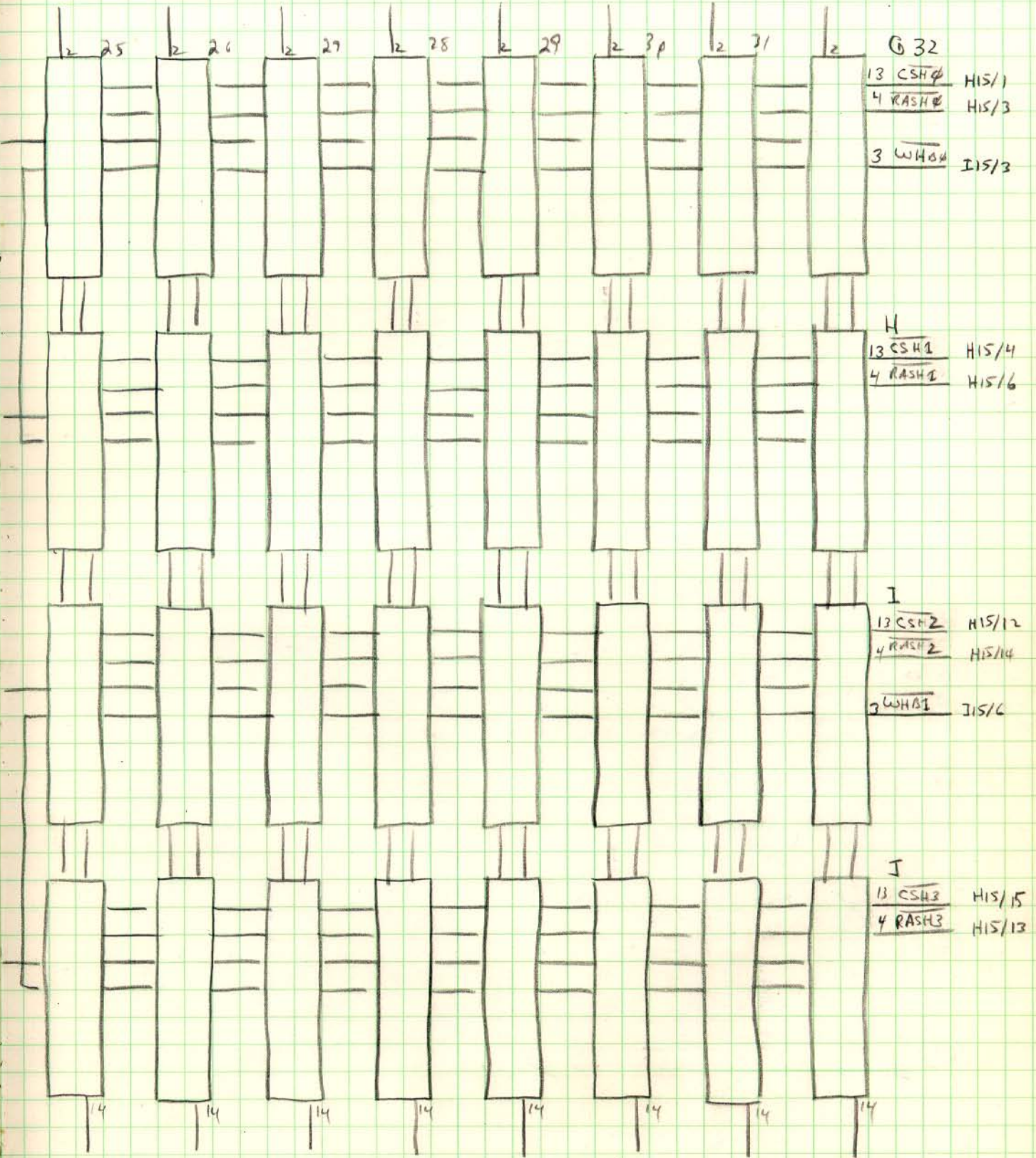
2 March 78
ARD

Memory Layout (chips μ PD414-E or equivalent) Low Byte

DI



Revised 6 Aug 82



80

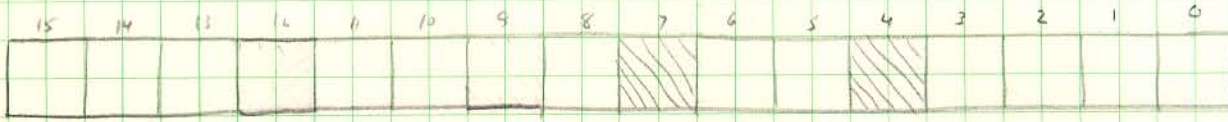
Remind 6 A 8

2 March 78
ARB

Memory Management Status + Control

Status Register ϕ (SR ϕ)

17777572₈



15 { Abort - Non resident caused by accessing a Page with the ACF = ϕ 4 or an illegal mode in the PSW.
 14 { Abort - Page length outside the range specified in the PLF
 13 { Abort - Read only attempting to write into a page with ACF = 2

12 { Ext MMGT = 0 Not used
 11 { Ext MMGT = 1 Specifies the PAR/PDR set selected when the abort occurred
 10, 11 indicate Bank selected (Normally from SRI)
 9 { 10, 9 indicate group selected (Normally from PSW) frozen by abort bits 15, 14, 13
 8 { Maintenance Bit - enables location only in fixed destination

6 { Mode of operation (normally from CPU PSW) frozen by abort bits 15, 14, 13
 5 {

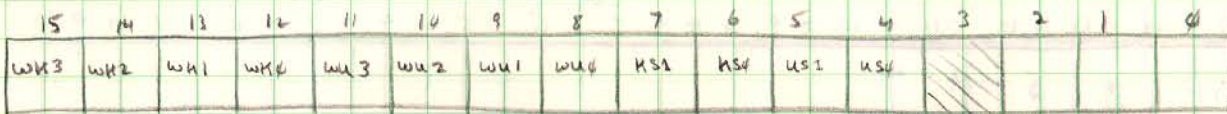
3 { Page Number during abort
 2 { frozen by abort bits 15, 14, 13
 1 {

ϕ { Enable MMGT Bit

Status Register 1 (SR1)

17 / 7 7 7 5 7 4 8

Read/Write



Specifies one of sixteen PAR/PDR groups for reading or writing when Accessing Kernel Addressing 17772300-2317, 17772340-2357
Enabled only if Extended MMIO Enabled

Specifies one of sixteen PAR/PDR groups for Reading or writing when Accessing User Addressing 1777600-617, 1777640-657
Enabled only if Extended MMIO Enabled

Kernel PAR/PDR Bank Select
Enabled only if Extended MMIO Enabled

User PAR/PDR Bank Select
Enabled only if Extended MMIO Enabled

UNIBUS MAP Enable

18bit/22bit MMIO

Enable Extended MMIO

15
14
13
12

11
10
9
8

7
6

5
4

2

1

0

4 March 78
ADD

Status Register 2 (SR2)

17/777576



16 Bit Virtual Address
of instruction, frozen by Aborts Read only

Notes: The CPU Microcode allows 4 modes
of addressing

- a) current
- b) previous
- c) Kernel
- d) User

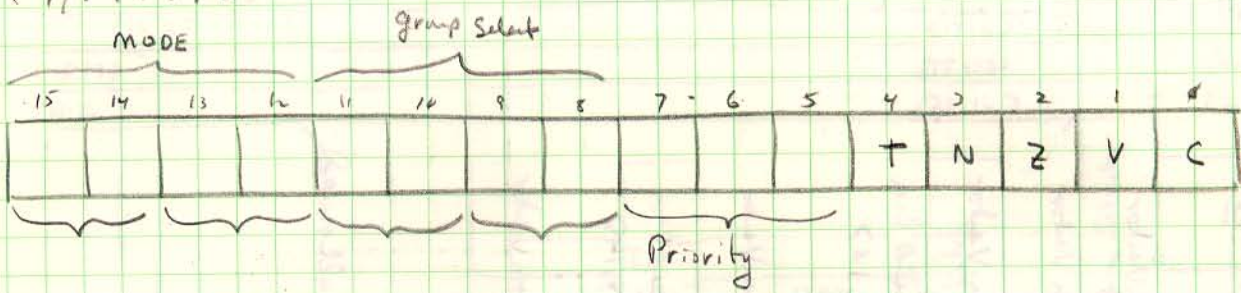
The Kernel, User Modes always refer to
Kernel, User Bank = 0, group = 0

Thus PDP11 interrupts/traps always go through the
same Kernel field

The current, previous modes use
whatever Bank, group is selected and enabled

Redefined CPU Processor Status Word

1777776



Current Mode

Previous Mode
from <15:14>

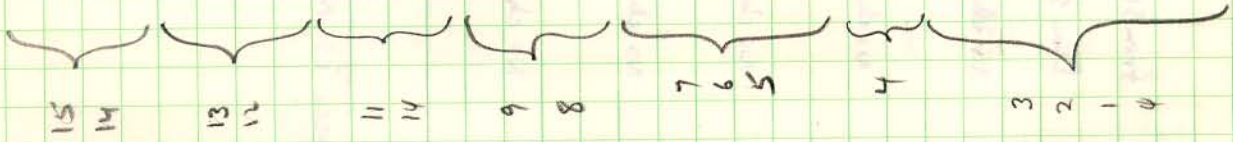
Current group

Previous group
from <11:10>

cpu priority

Trace Bit

cpu Status



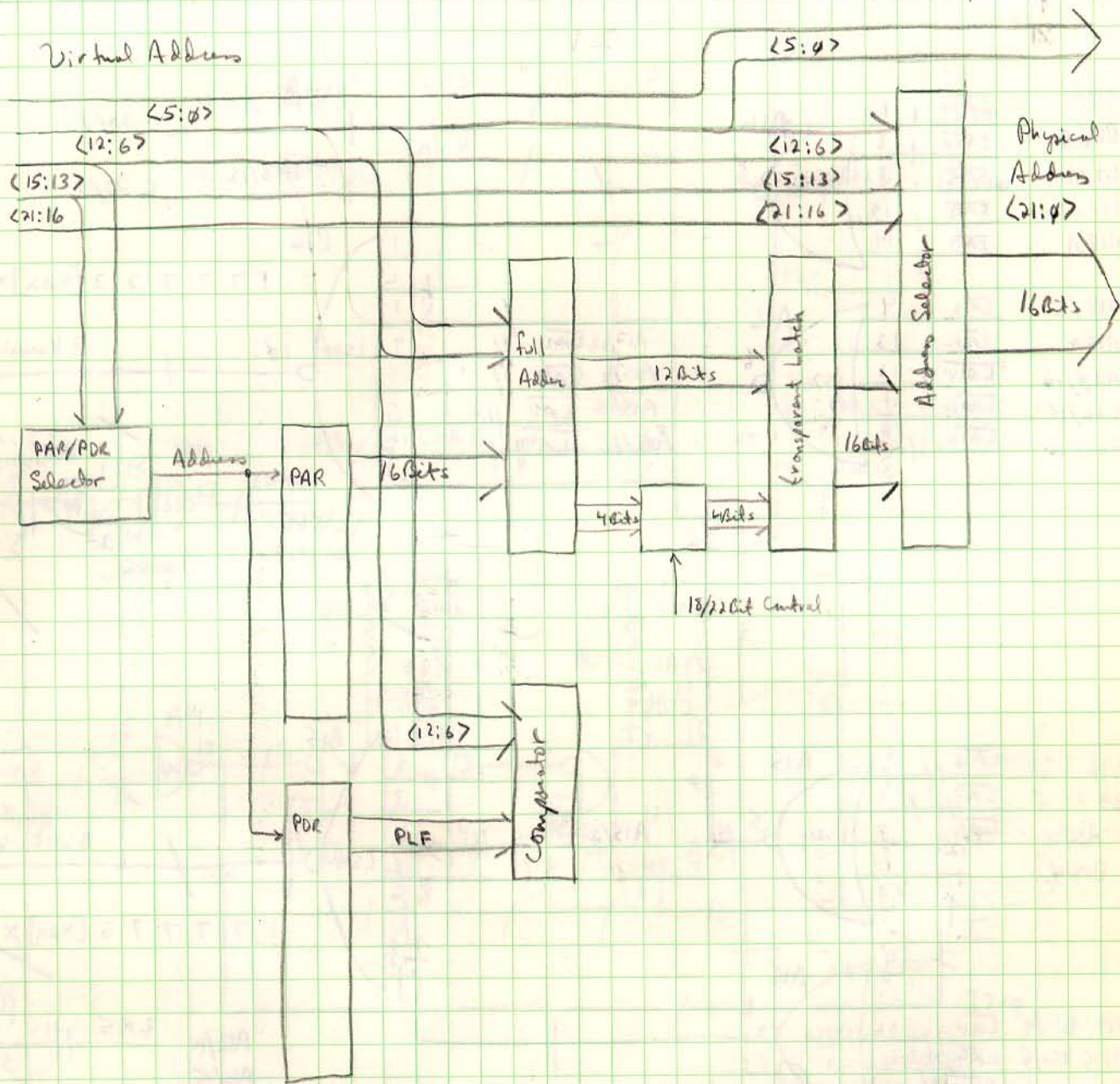
4 March 78
ASD

Notes on PSW operation with MM6T

PSW Bits	User RTI/KTI	Kernel RTI/KTI	User/Kernel Trap & Interrupts	Explicit Address
<03:04> Condition Codes	From Stack	From Stack	From Vector	*
<04> Trace Bit	From Stack	From Stack	From Vector	No change
<07:05> Priority	No change	From Stack	From Vector	*
<09:08> previous group	No change	copied from <11, 10>	copied from <11, 10>	*
<11, 10> current group	No change	From Stack	From Vector	*
<13, 12> previous Mode	No change	copied from <15, 14>	copied from <15, 14>	*
<15, 14> Current Mode	No change	from stack	from Vector	*

* - if Space is mapped, explicit addressing is allowed

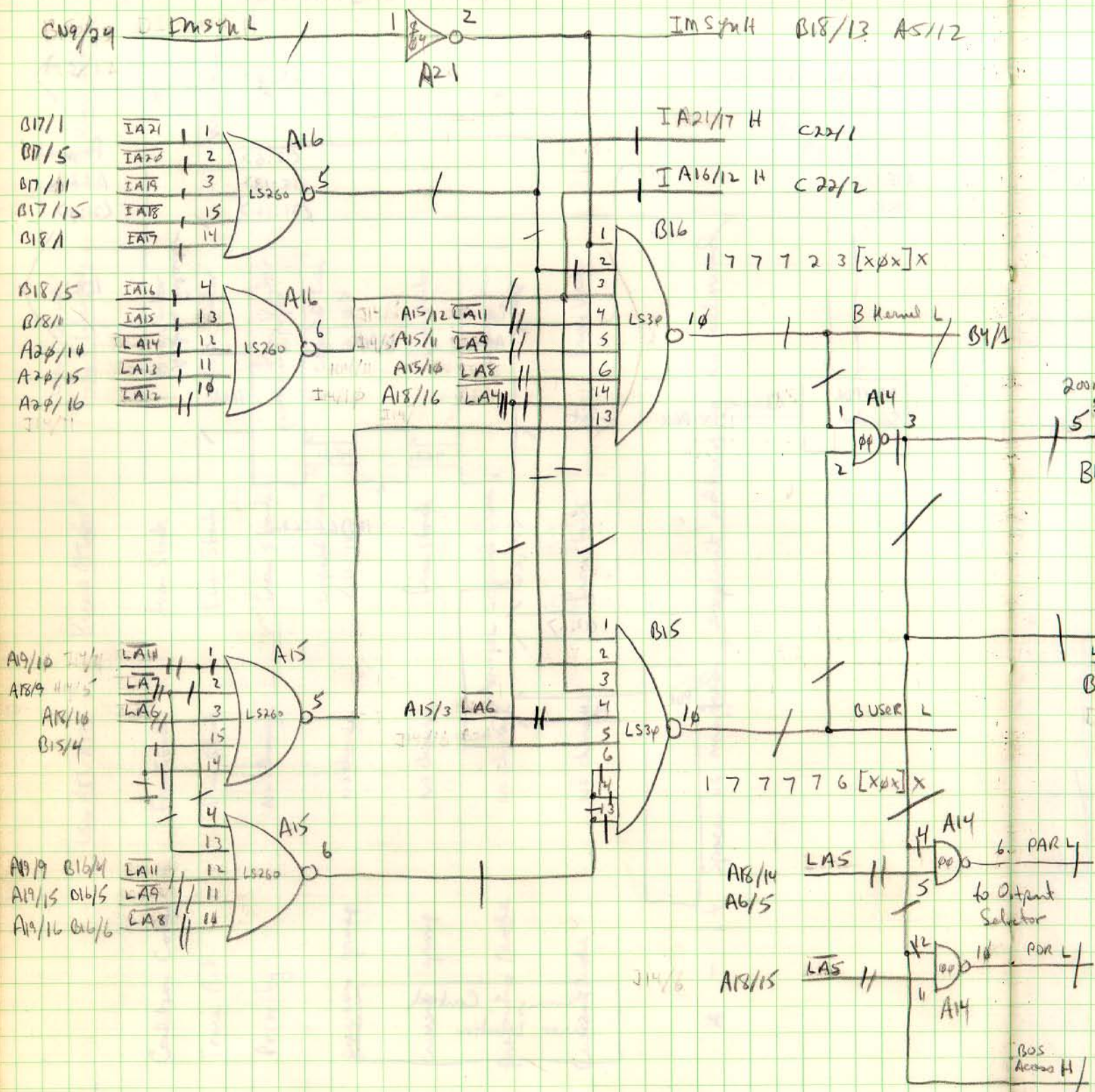
Simplified Block Diagram of Physical Address Generation



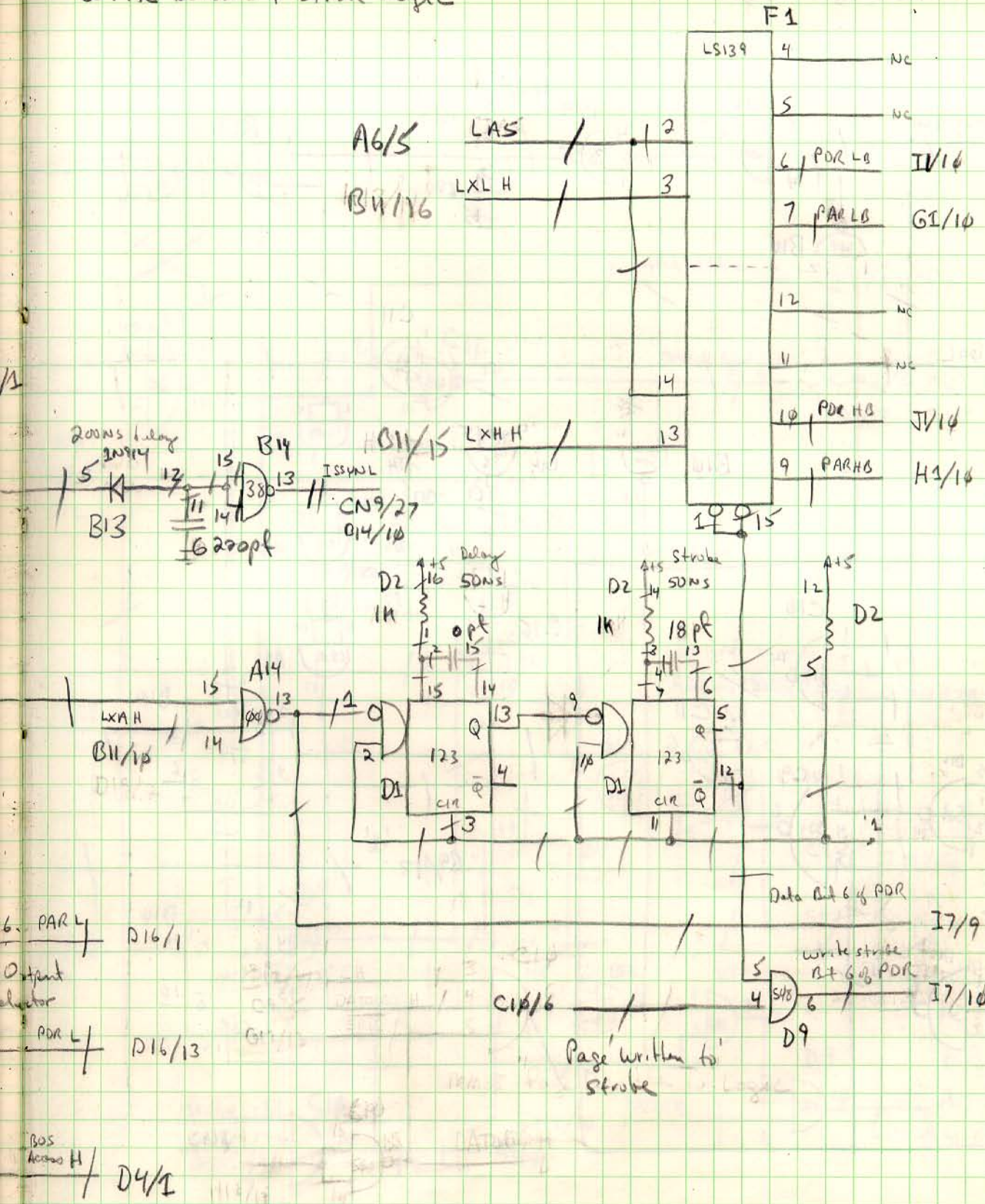
Timing & Control
Error Detection

11 March 78
4 March 78
AFO

PAR/PDR BUS Access Decoder

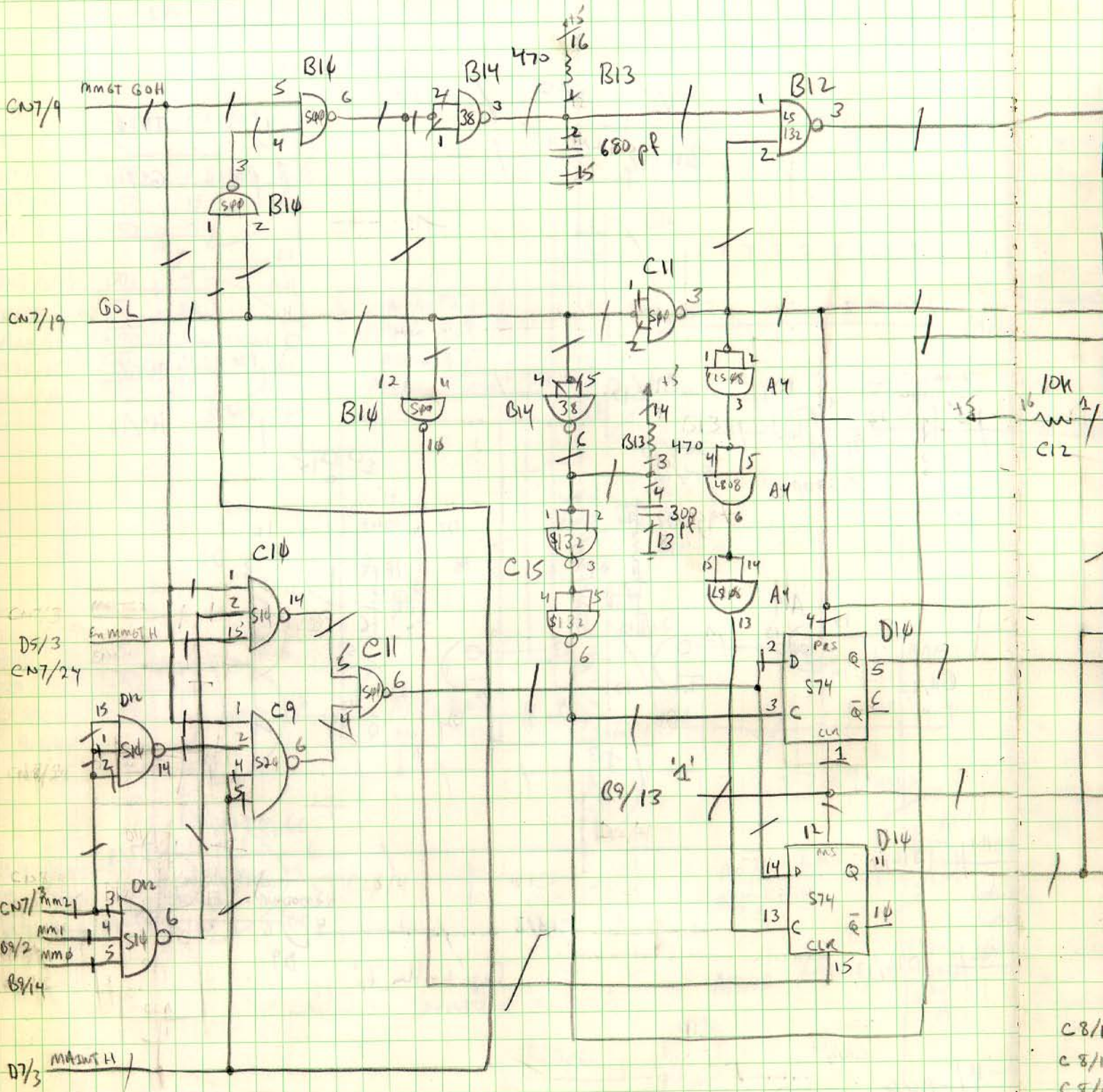


Write Decoder + Strobe Logic

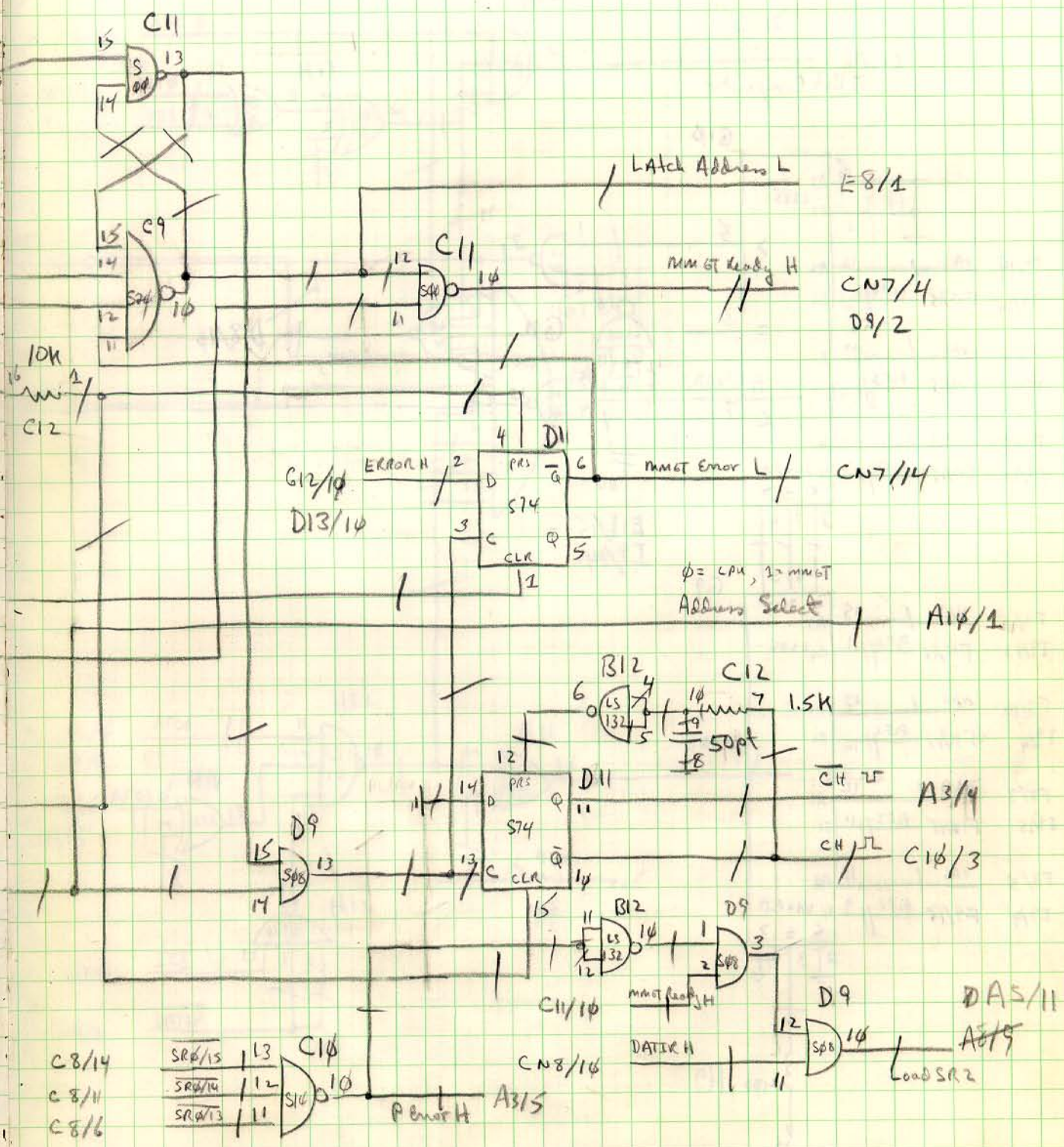


11 March 78
ARD

MMGT Timing Logic



C8/1
C8/11
C8/16

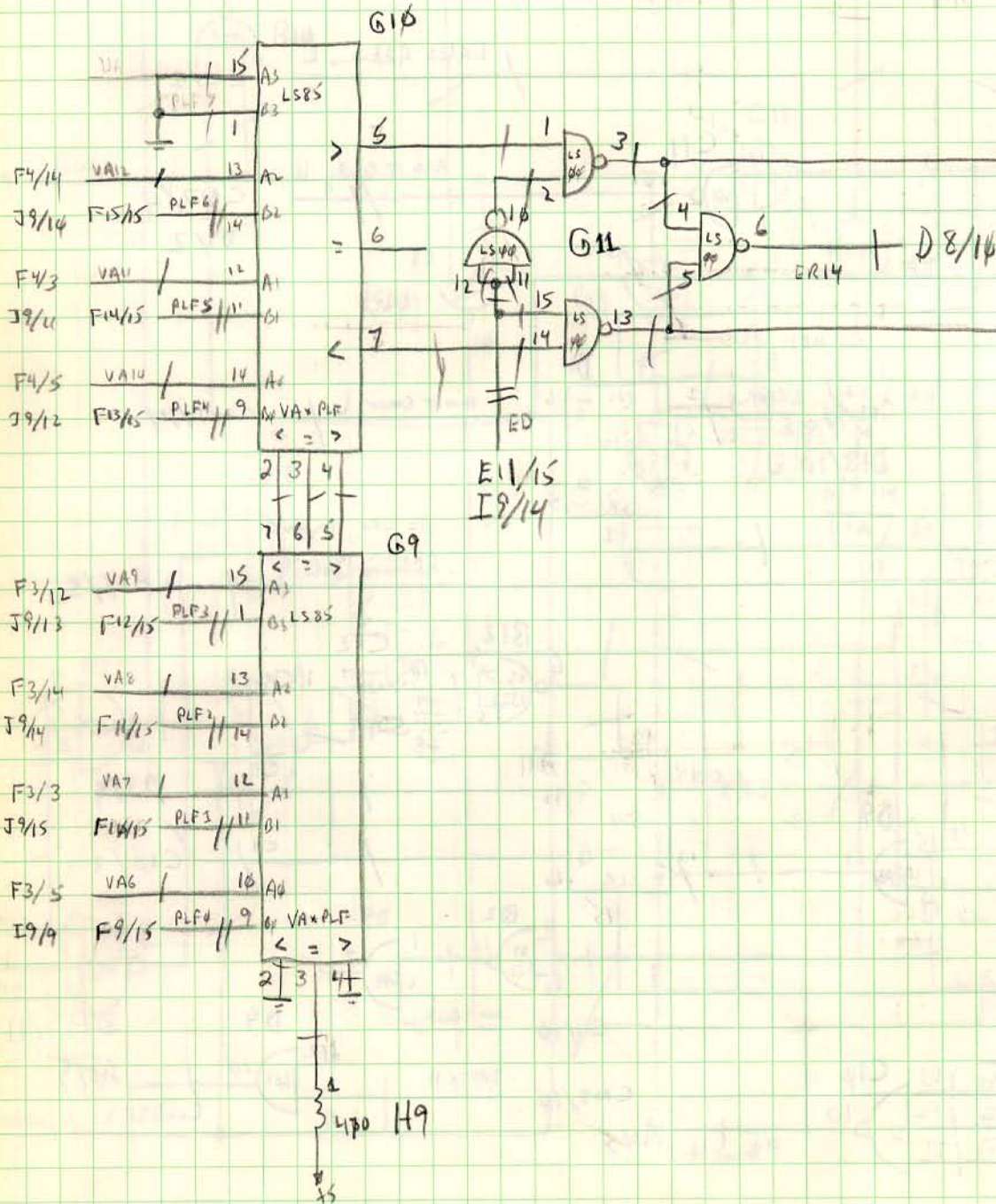


11 March 78
ARBS

Error Detection Logic

PLF Length Comparator

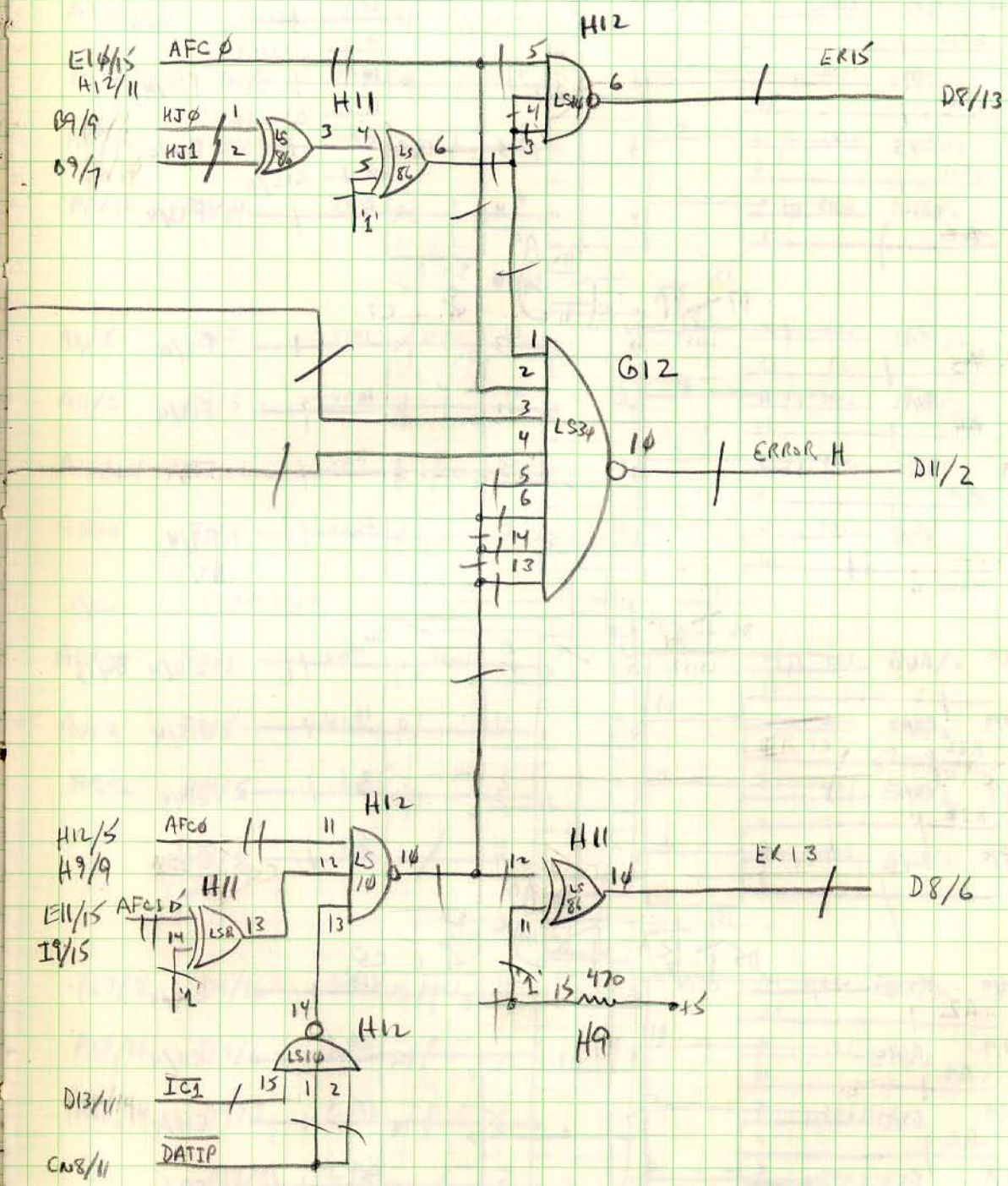
7 Bit Comparator



E14
A1
B9/9
B9/7

H12/
H9/
E11/15
I9/15

D13/
C08/

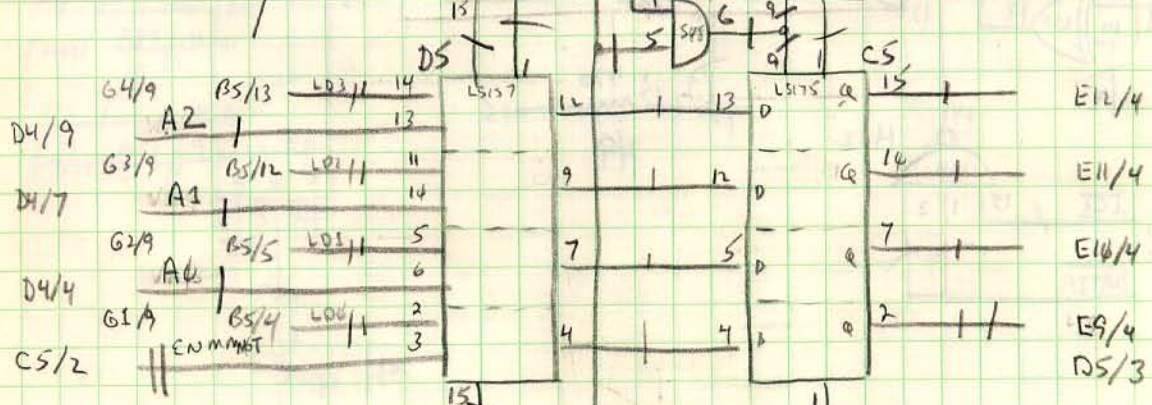
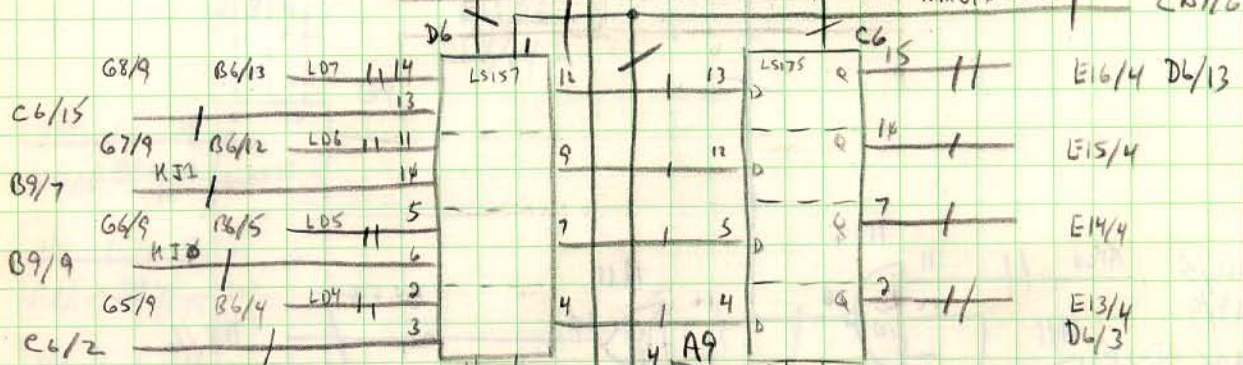
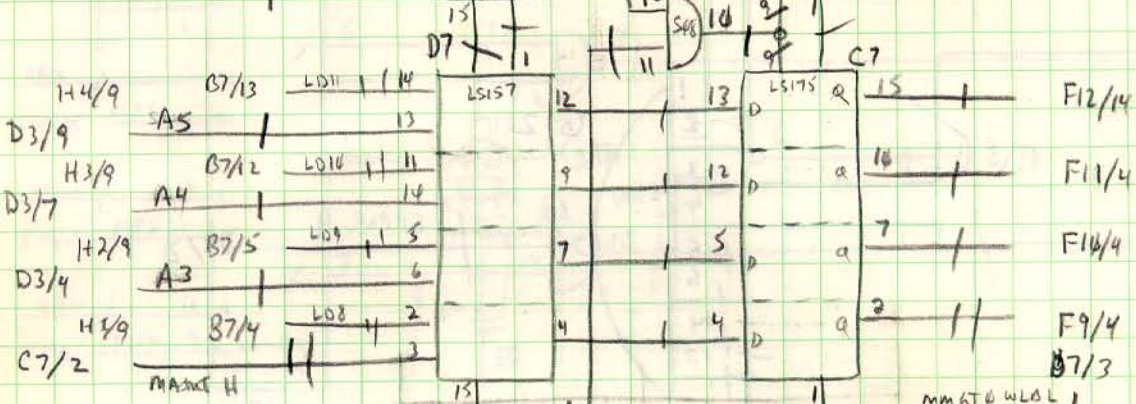
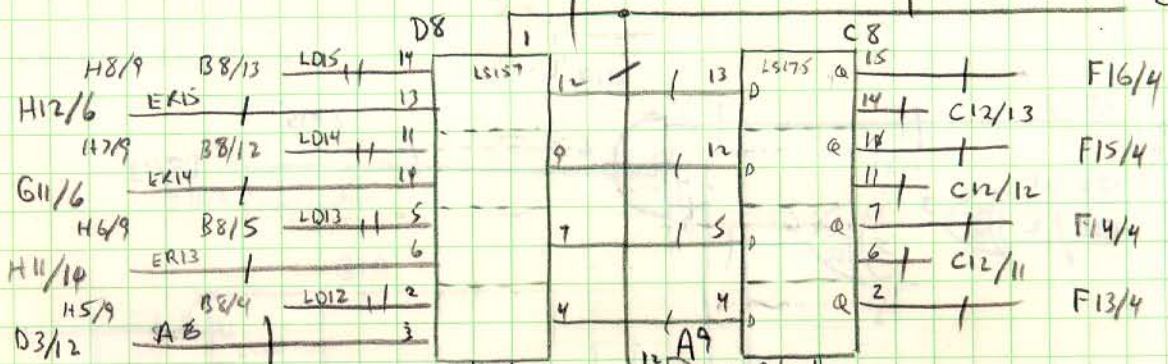


12 March 78
ARD

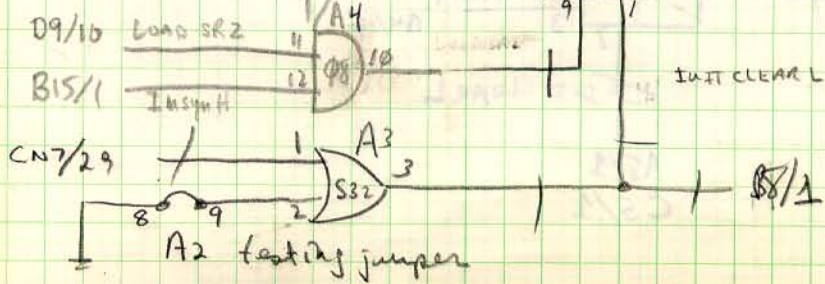
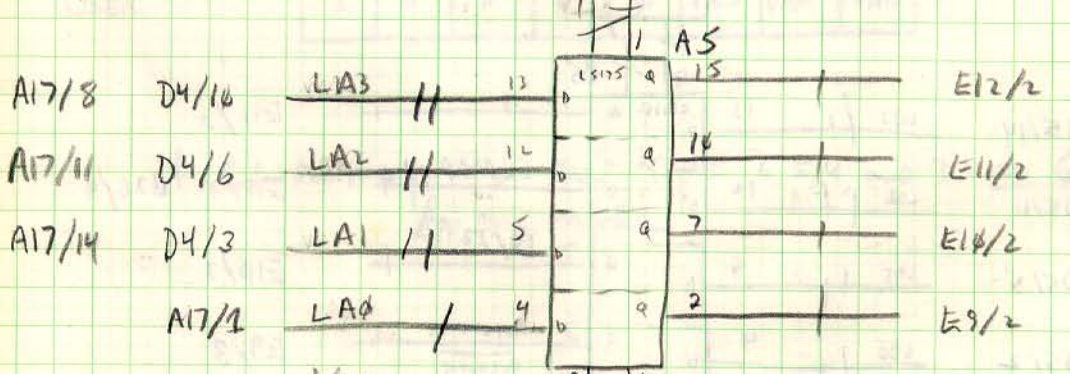
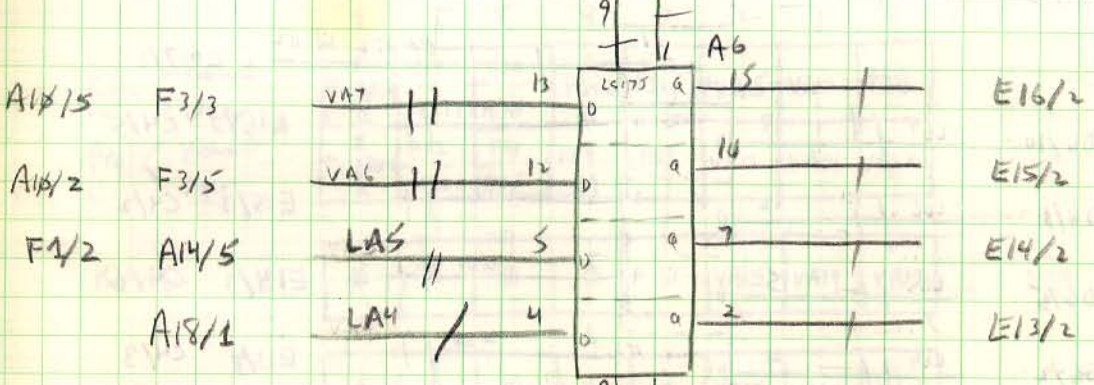
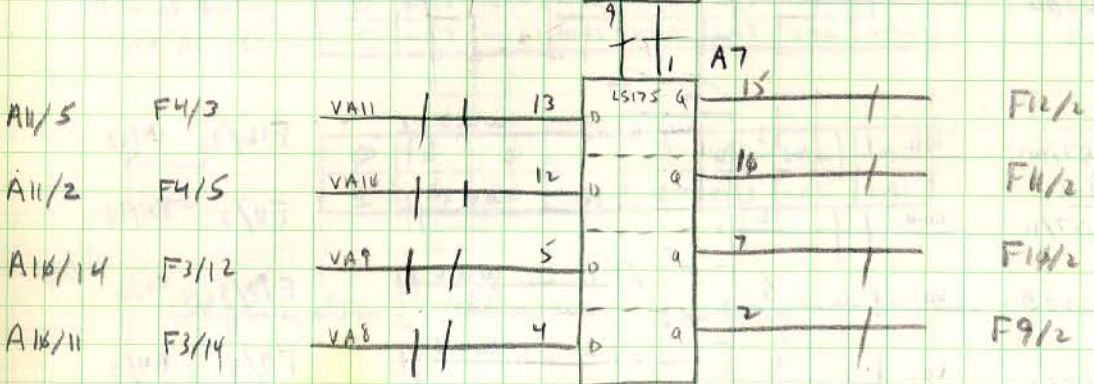
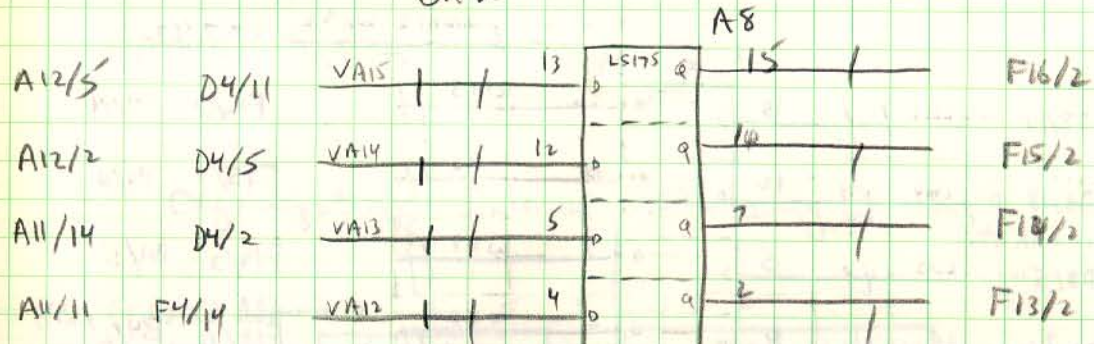
Status Registers

SRφ

MMSTB WHOL CN7/7

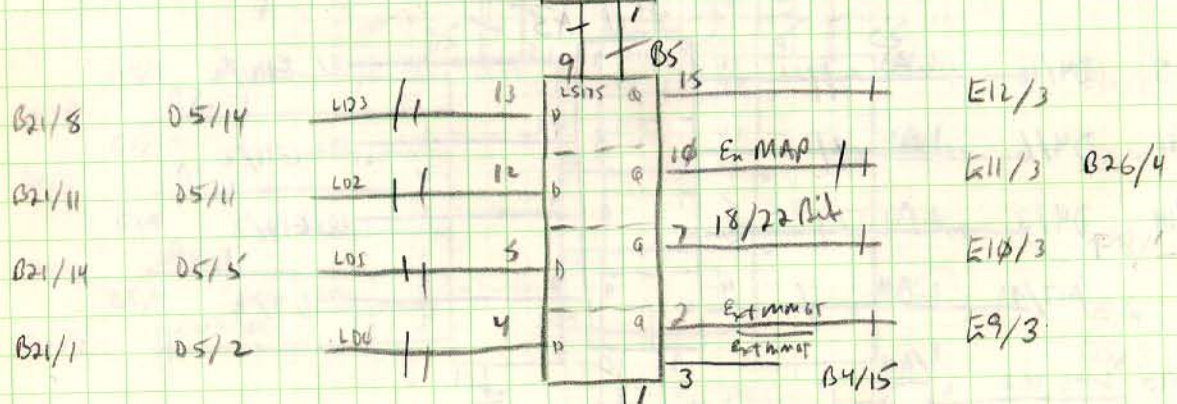
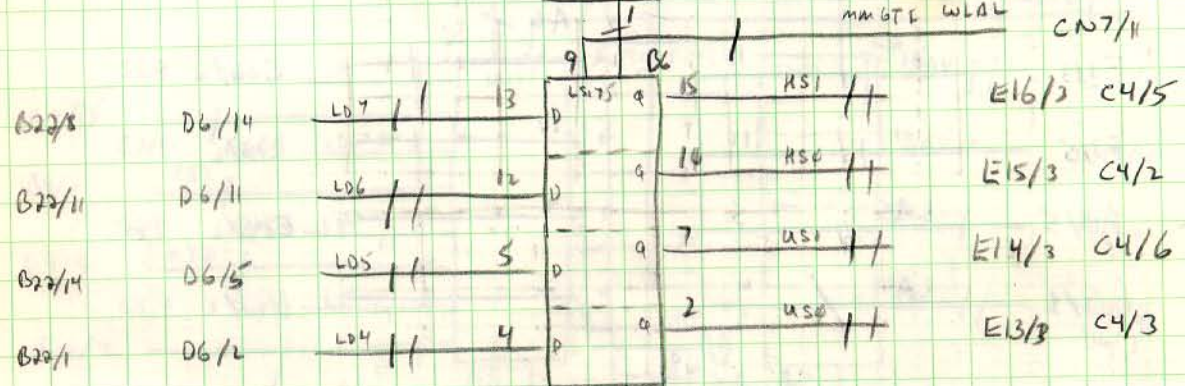
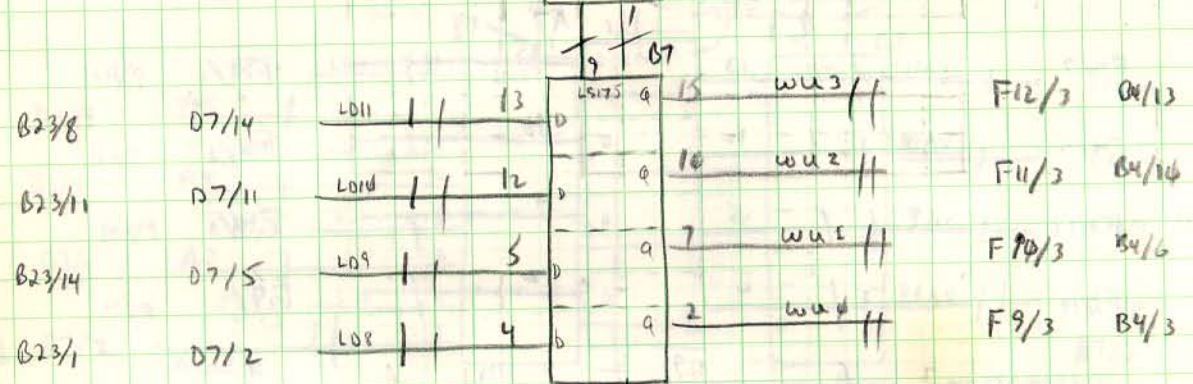
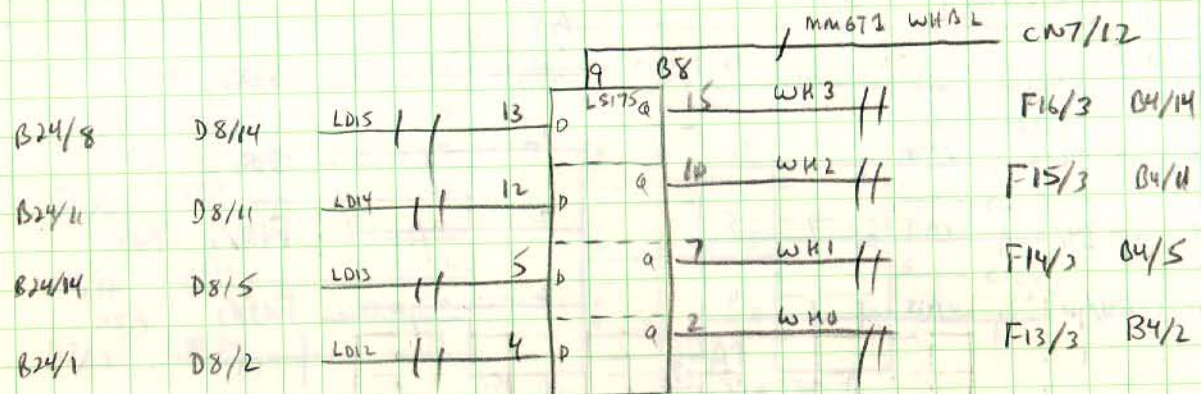


SR 2



12 March 78
ABP

Status Register SRI



3
 EXT CLEAR L
 A8/1
 C5/1

Description of PAE/PDE Address generation in the MM6T System

Organization of Internal Addressing During a BUS Cycle to MM6T

8 Bit (1 of 256) Address	7	6	5	4	3	2	1	0	
Kernel Access	0	WK3	WK2	WK1	WK0	LA3	LA2	LA1	if Extended MM6T Enabled
User Access	1	WK3	WK2	WK1	WK0	LA3	LA2	LA1	

Kernel	0	0	0	0	0	LA3	LA2	LA1	if Extended MM6T Not enabled
User	1	0	0	0	0	LA3	LA2	LA1	

Organization of Addressing during relocation addressing

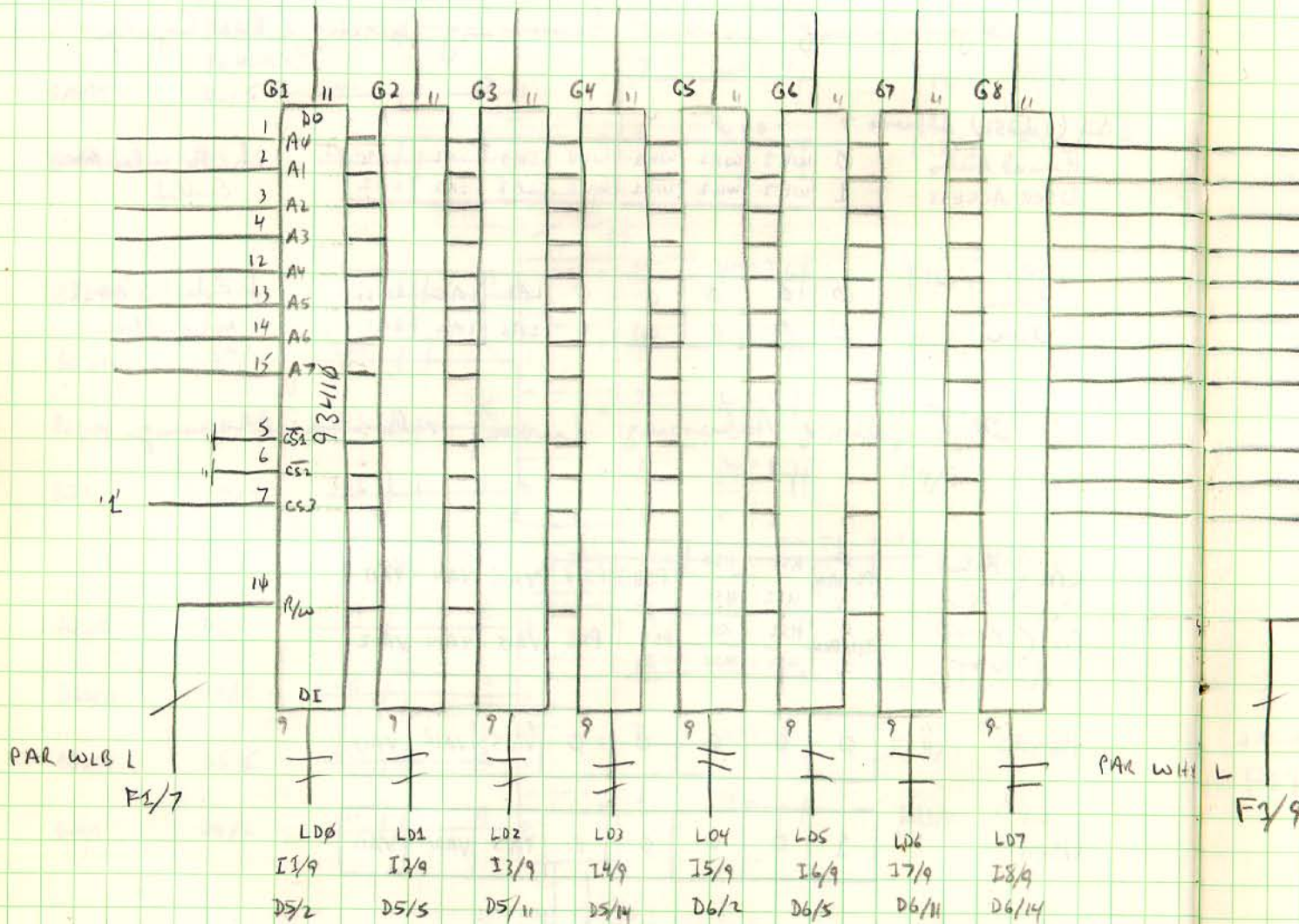
	7	6	5	4	3	2	1	0
CM (Kernel User)	0 PS7/MS7	KS1	KS0	PS11	PS10	VA15	VA14	VA13
	1 US7/MS7	US1	US0					
PM (Kernel User)	0 PS13/MS12	KS2	KS1	PS9	PS8	VA15	VA14	VA12
	1 US13/MS12	US2	US1					
Kernel	0	0	0	0	0	VA15	VA14	VA13
USER	1	0	0	0	0	VA15	VA14	VA13

if Extended MM6T = 0 then Bits 6, 5, 4, and 3 \equiv 0 for any mode

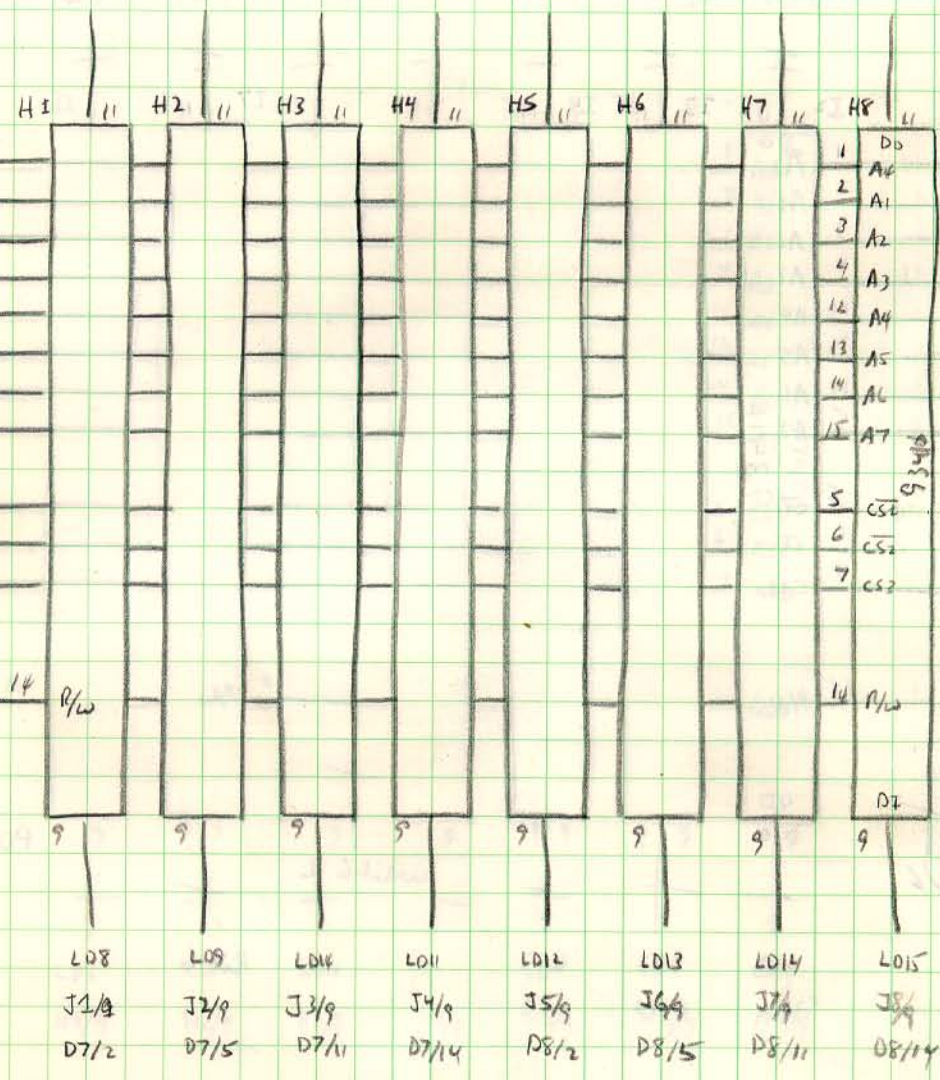
12 March 78
ABP

MMBT Central Memory (PAR)

H9/6	H9/7	I9/1	I9/2	I9/3	I9/4	I9/5	I9/6
F3/6	F3/2	F3/15	F3/11	F4/6	F4/2	F4/15	F4/11
PAF4	PAF1	PAF2	PAF3	PAF4	PAF5	PAF6	PAF7



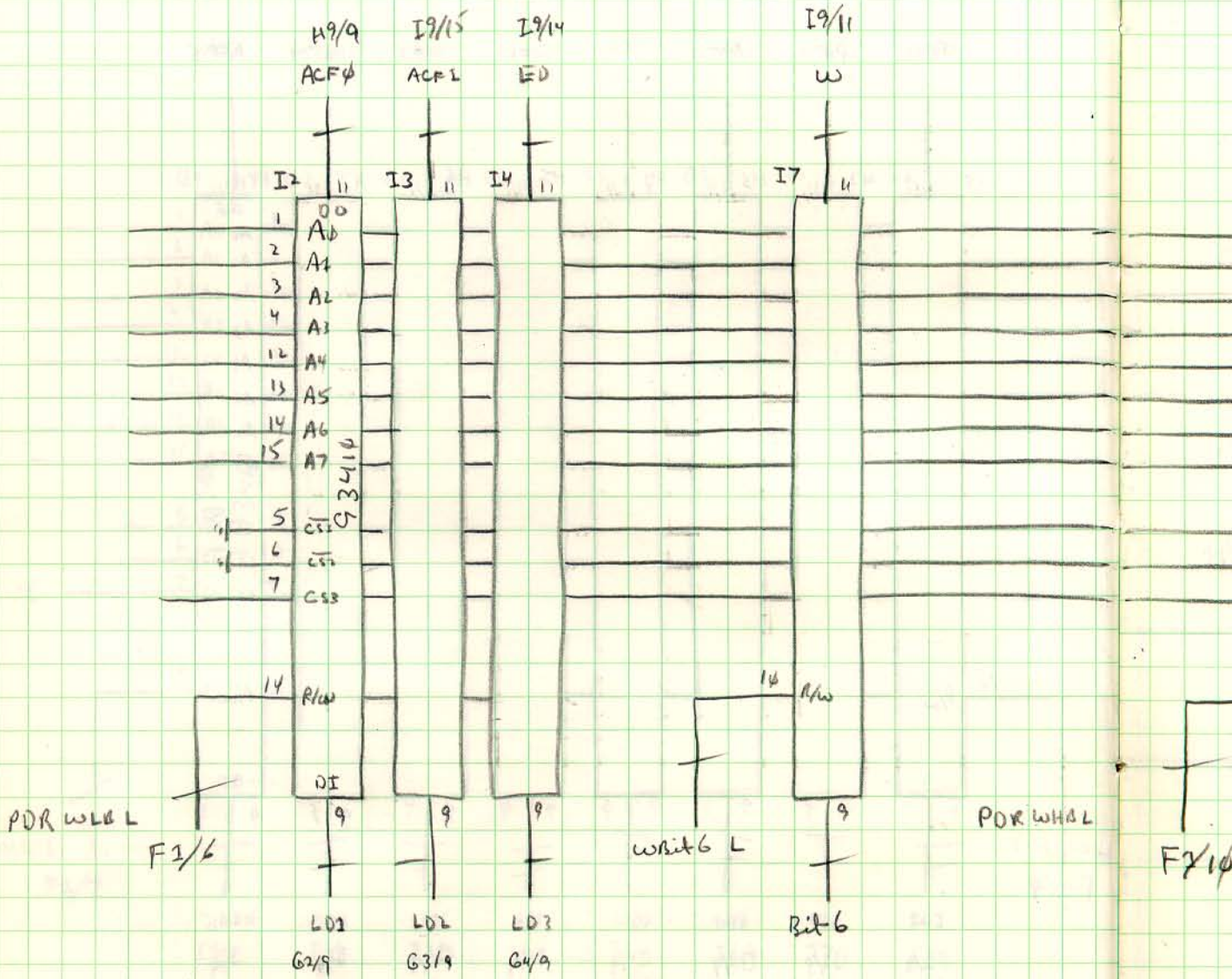
I 9/7 J 9/11 J 9/12 J 9/13 J 9/14 J 9/15 J 9/16 J 9/17
 F5/6 F5/2 F5/15 F5/11 F6/6 F6/2 F6/15 F6/11
 PAF8 PAF9 PAF10 PAF11 PAF12 PAF13 PAF14 PAF15

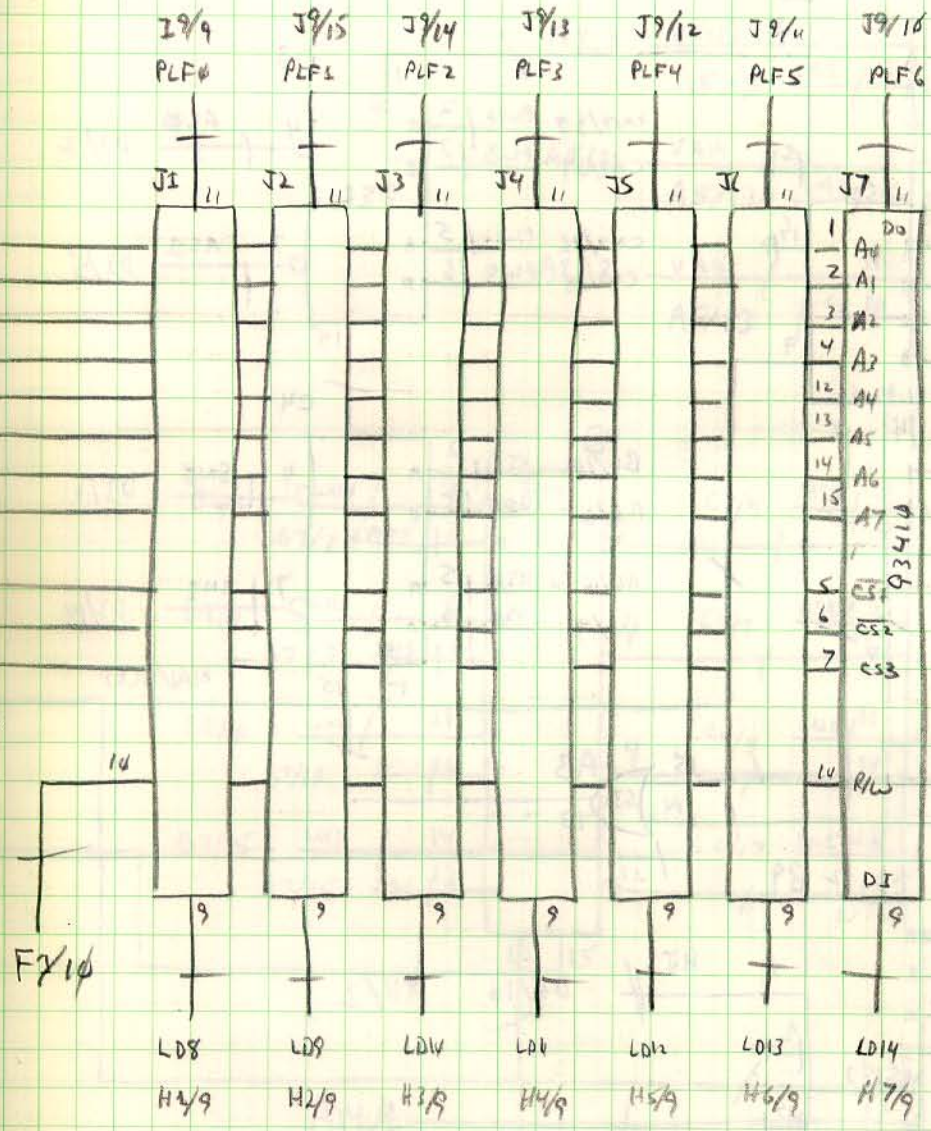


all H, I, J 9's are 470 ohm pulsed resistors

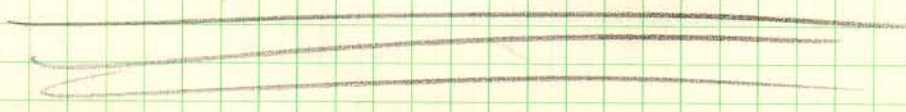
14 March 78
 ARD

MM6T Central Memory (PLF, W, LD, ACF)





All H, I, J 9's are 470Ω Pullup Resistors

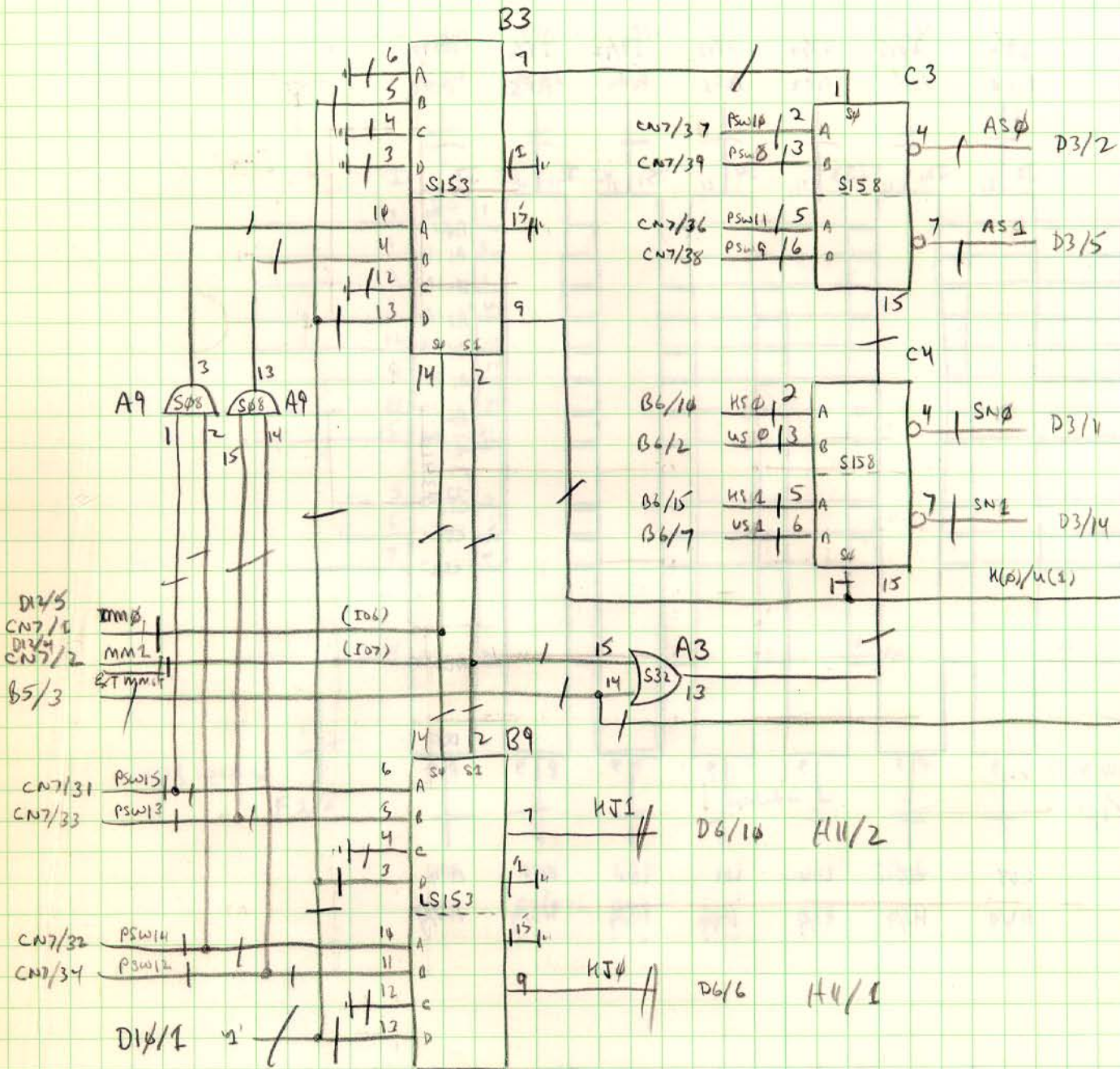


14 March 78
ARD

MMGT Address Generation

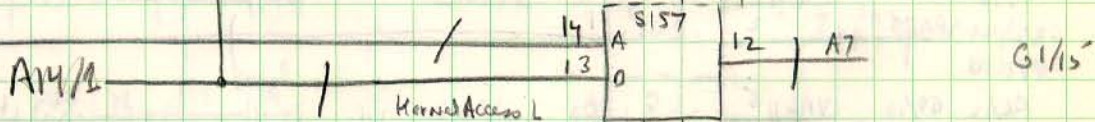
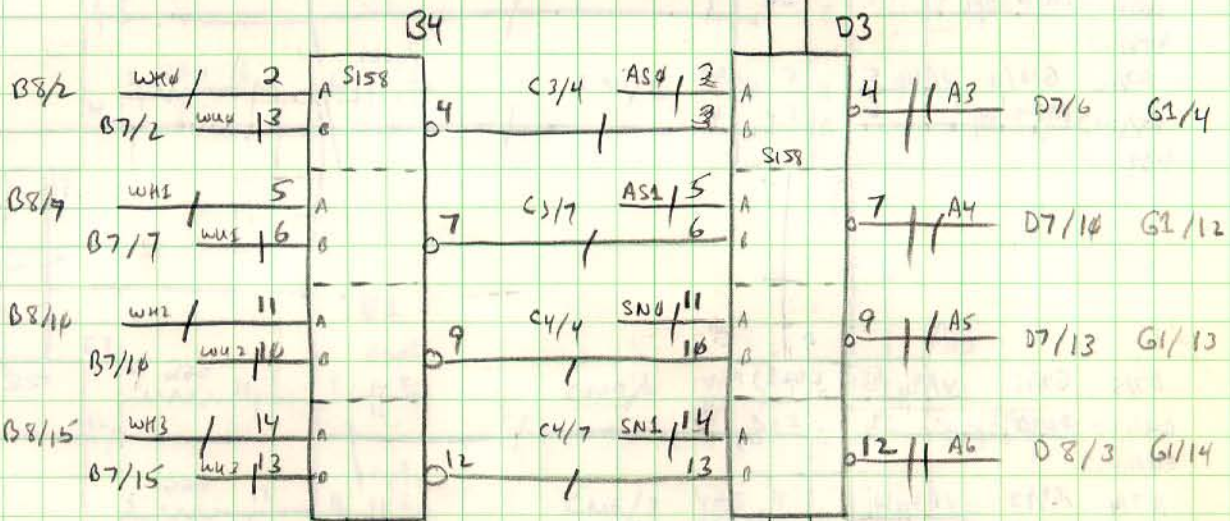
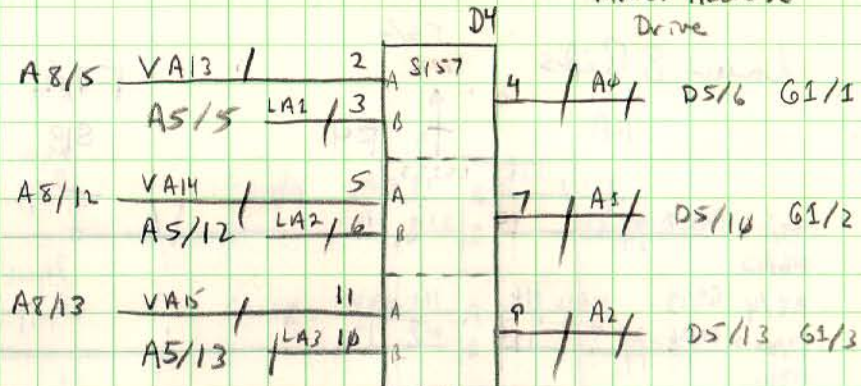
(Virtual → Physical)

BUS



BUS & Combined Multiplexing

MMGT Address Drive

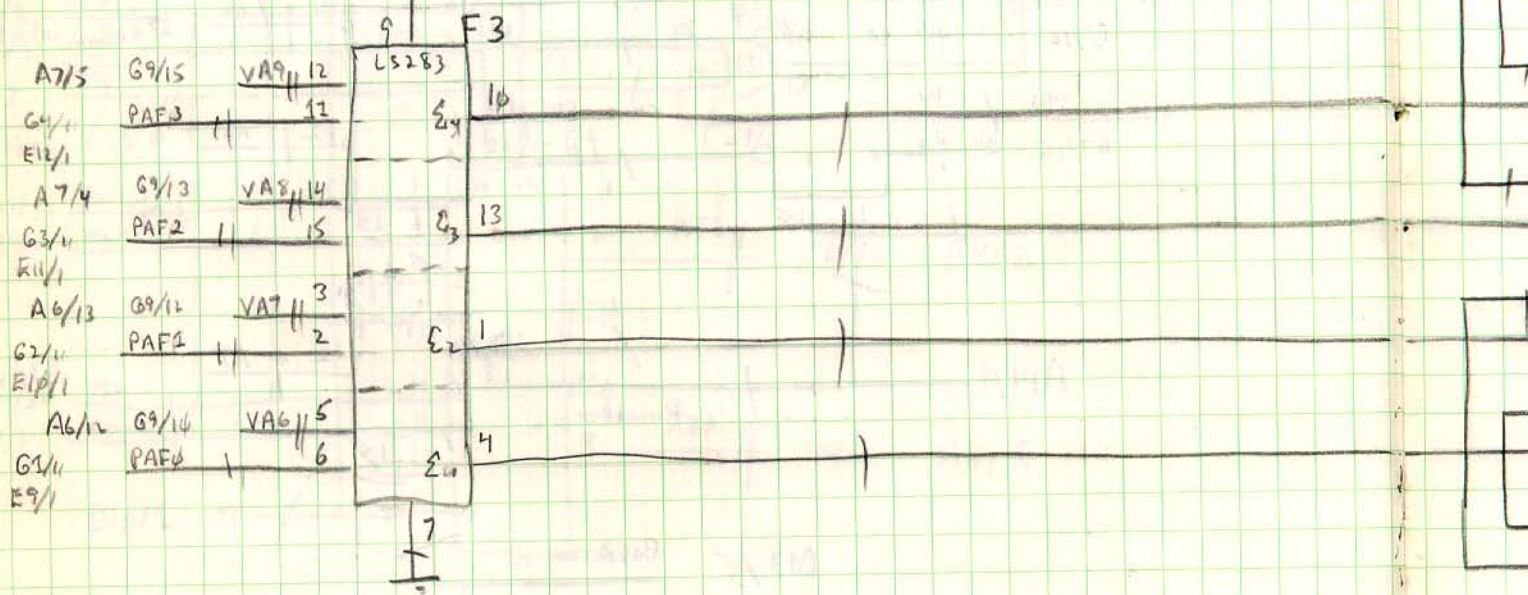
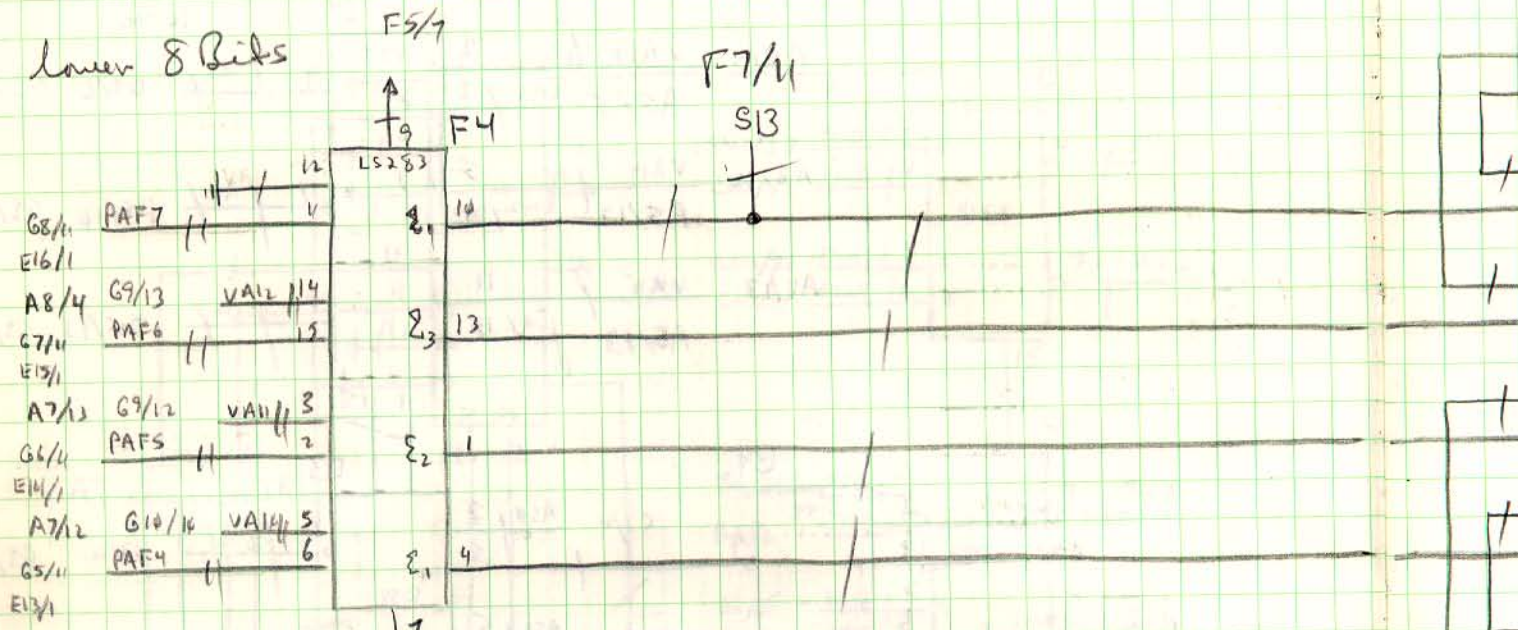


B13/5 BUS ACCESS H

14 March 78
ASB

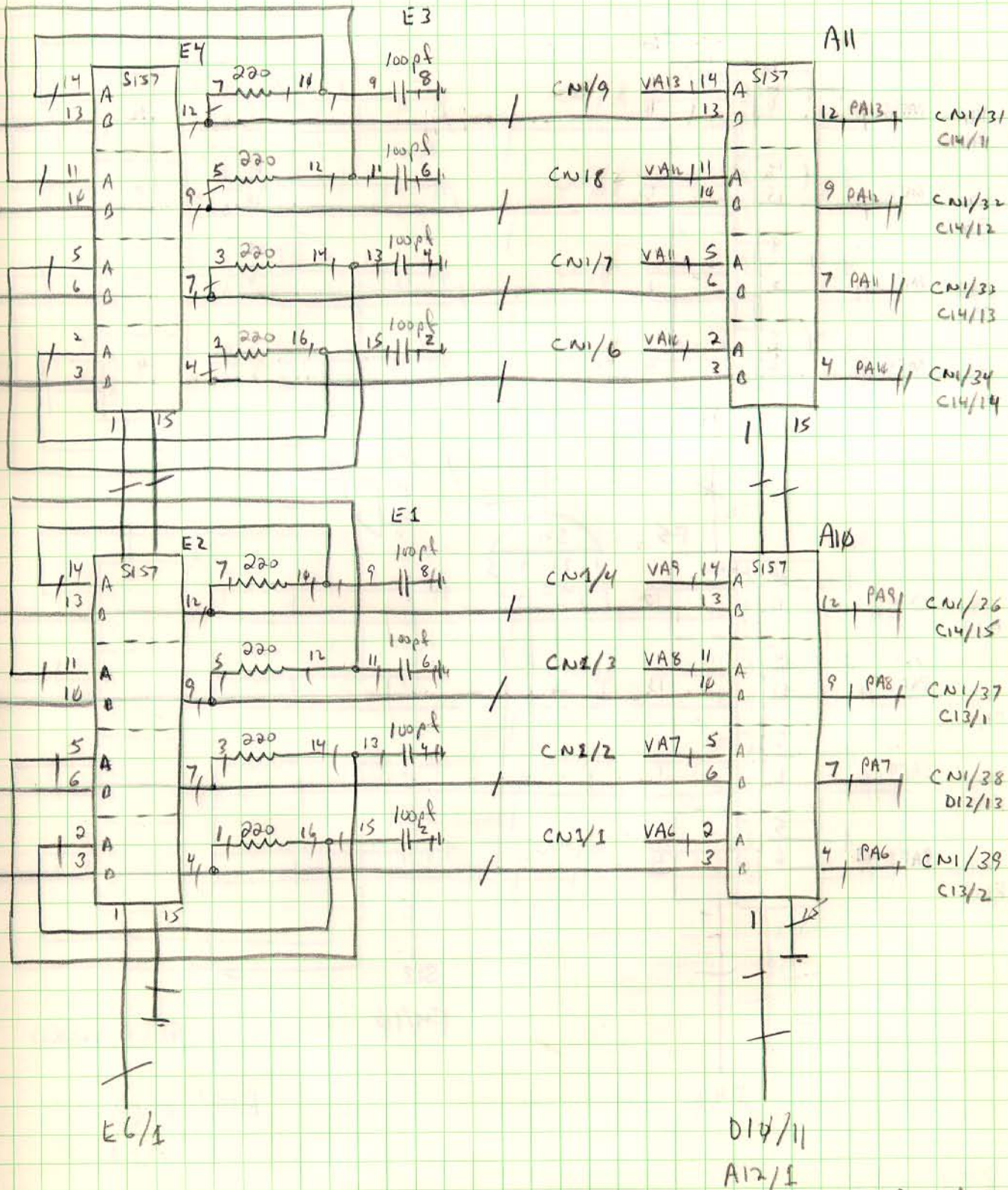
MM6T Relocation Addr / Address Latch / Address Multiplexer

Lower 8 Bits



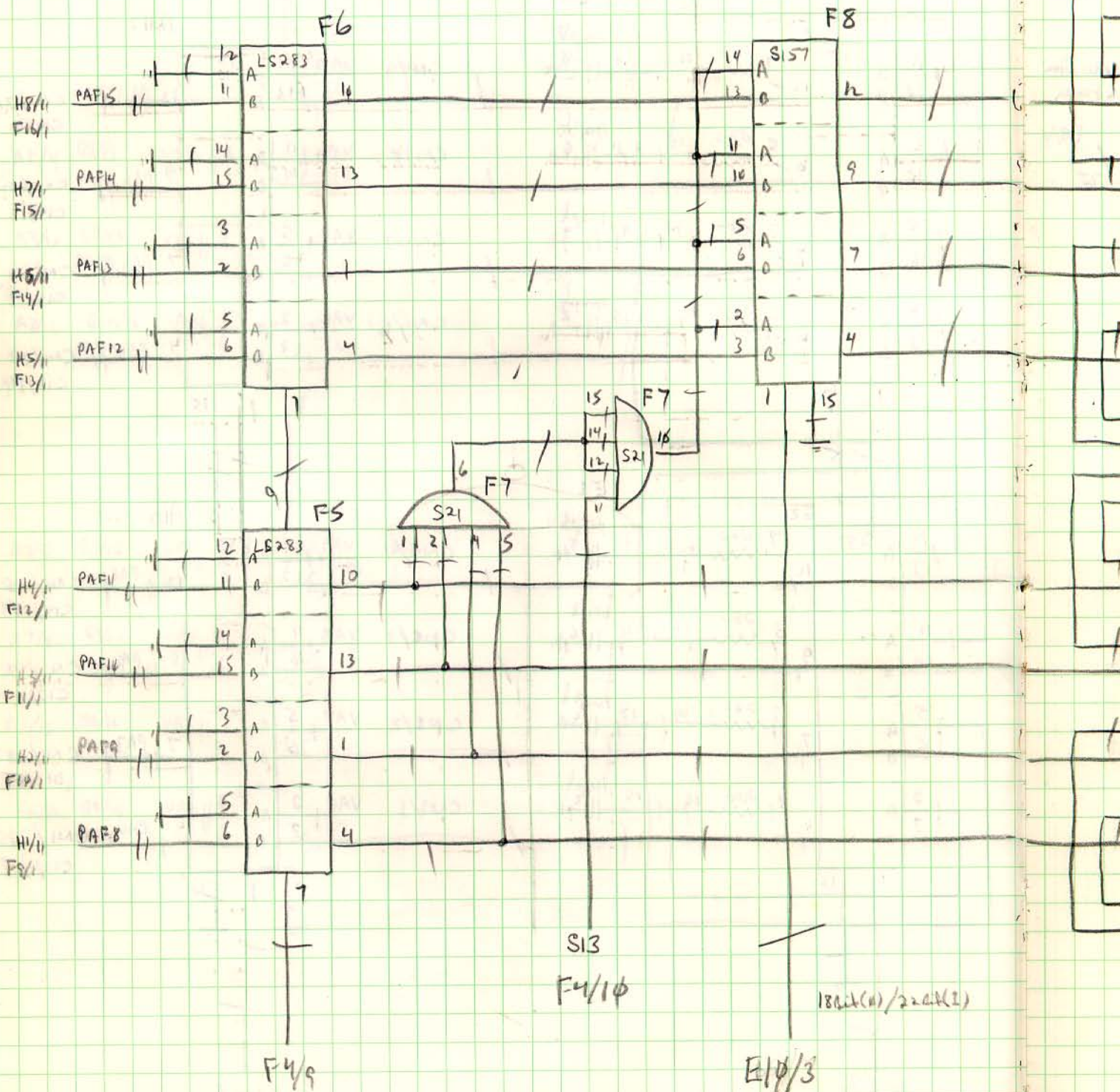
Transparent Latch

CPU/MMIO Address Selector



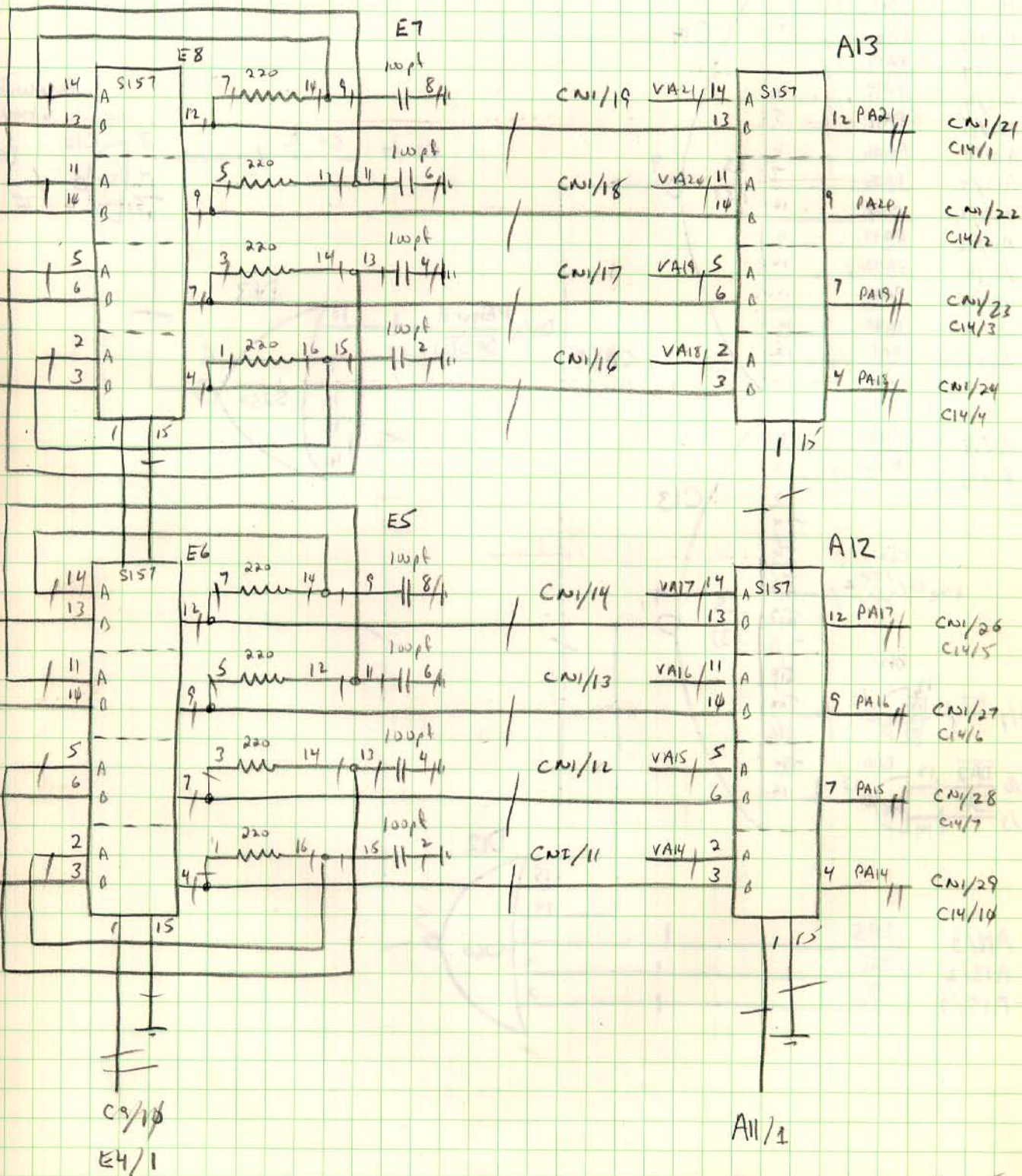
14 March 78
ABO

Upper 8 Bits



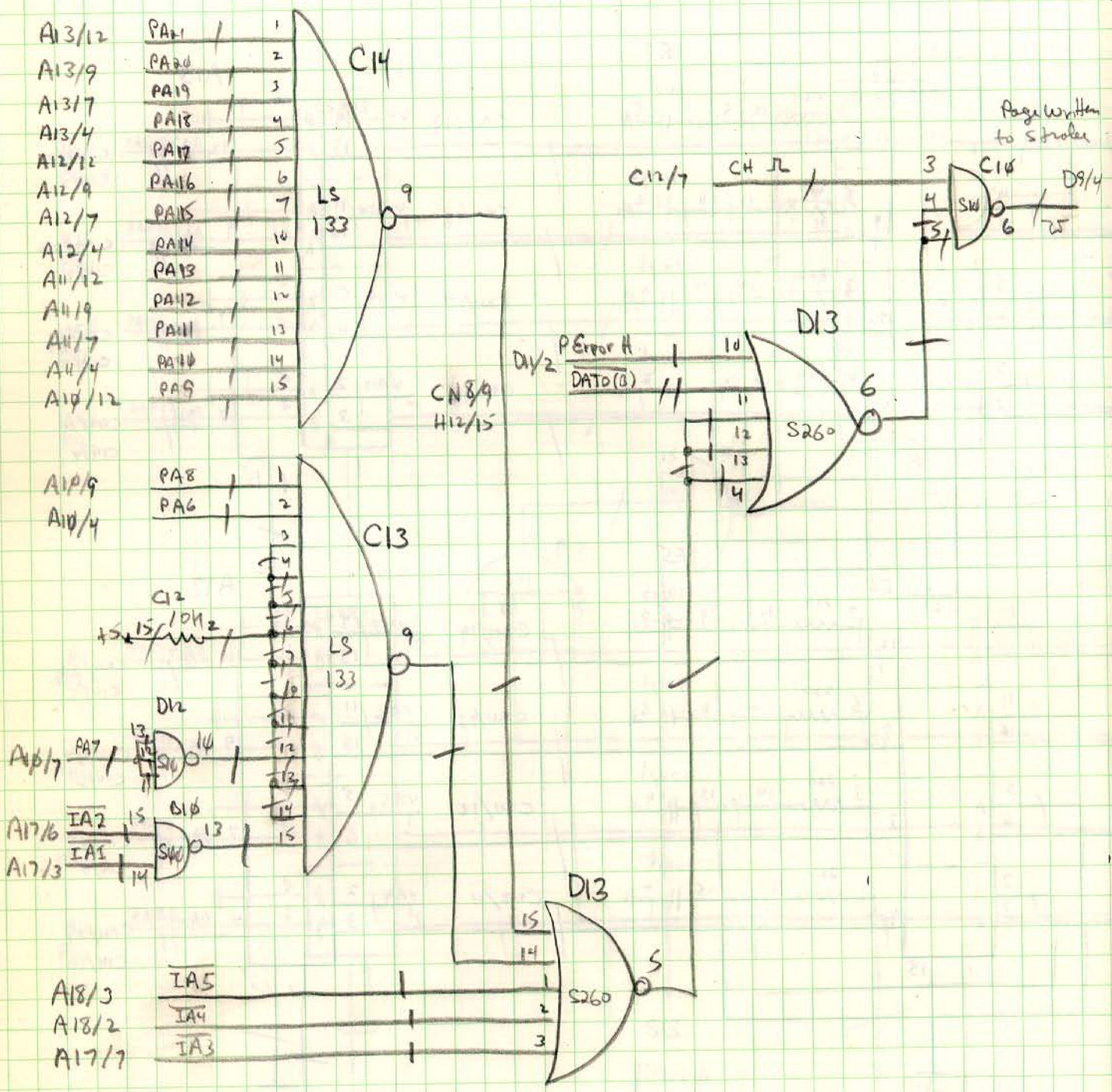
Transparent Latch

CPU/micro Address Selector



14 March 78
ARB

Page written to logic

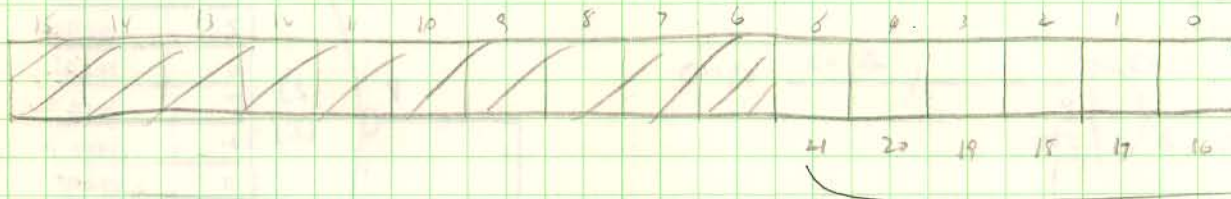


26 April 78
ARD

UNIBUS MAP Logic

17770200 - 17770367

17770 [01x] [x1x]

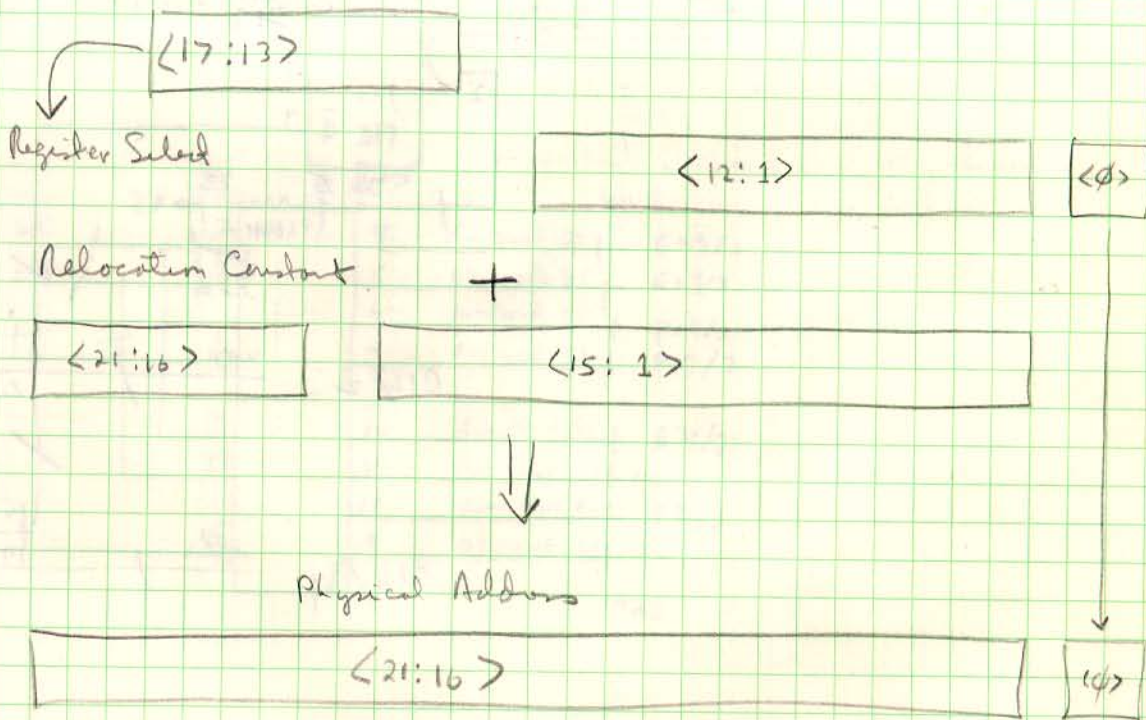


The unibus map is composed of 31 pairs of registers -
each 4K increment of UNIBUS space selects a separate
register pair. The register pair provides a relocation
offset for the UNIBUS Address

17770 [01x]x [x0x]

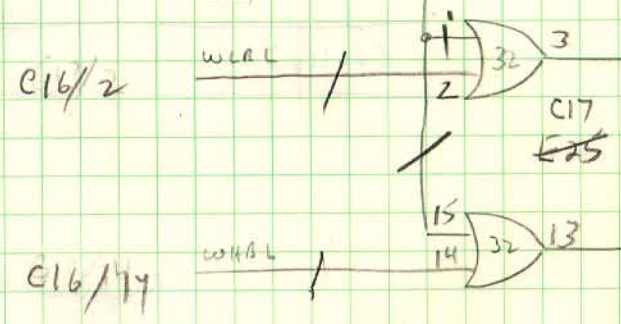
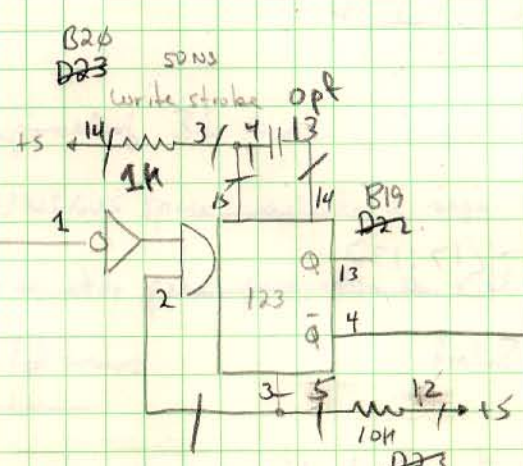
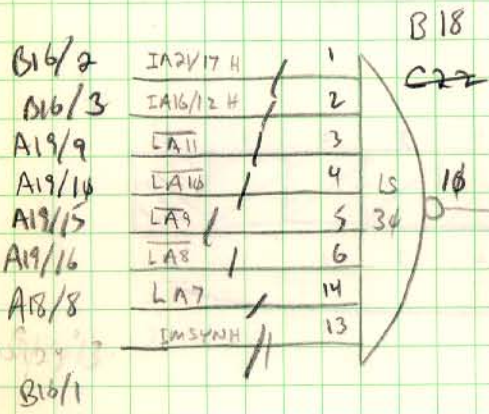


Relocation Constant



20 March 78
ARR

Address Decoder / Write Logic



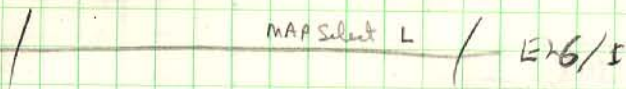
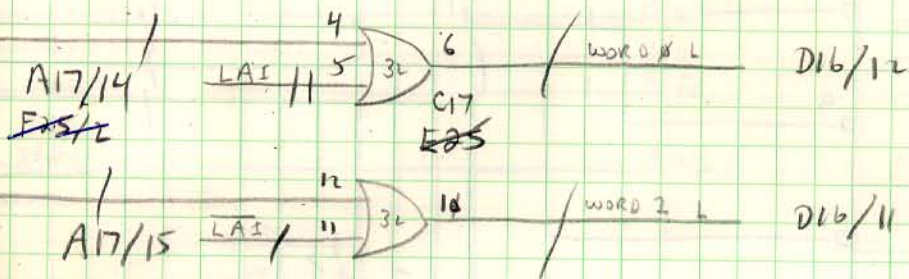
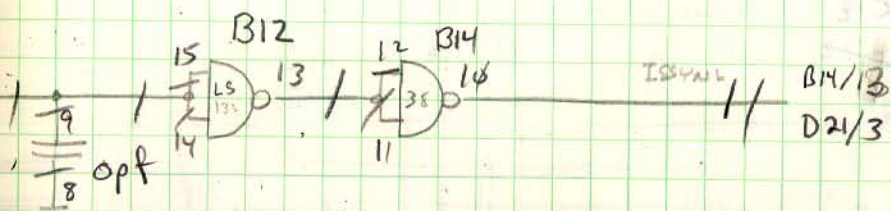
7.5NS delay

7.5k

B13



A
E



D17		WLB	
LAI	2	4	Even word B1
LAI	3	5	ODD word B1
LAI	0	6	Even word B2
LAI	1	7	ODD word B2
LAI	14	12	Even word B1
LAI	13	11	ODD word B1
LAI	15	9	Even word B2
LAI	0	8	ODD word B2

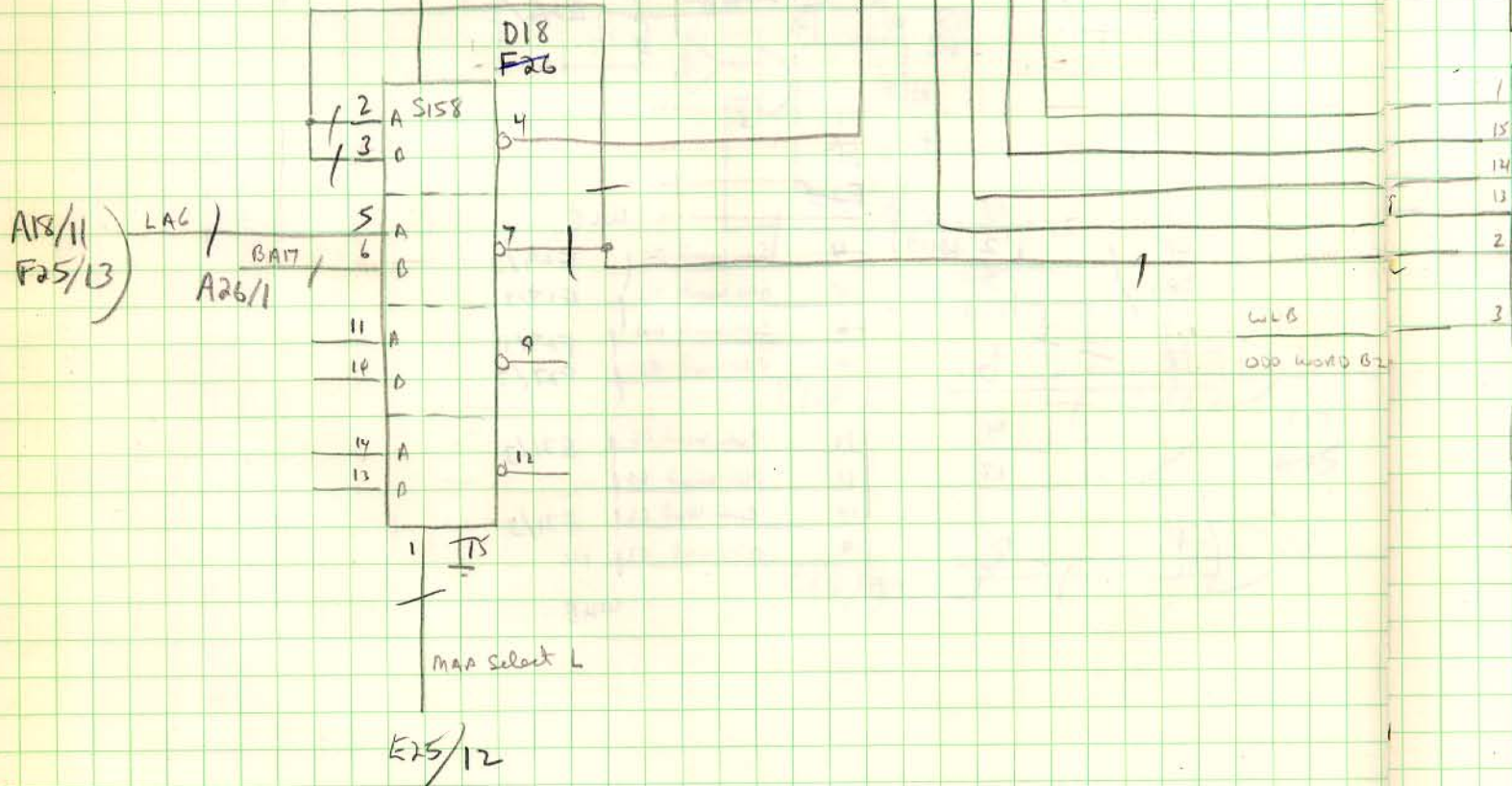
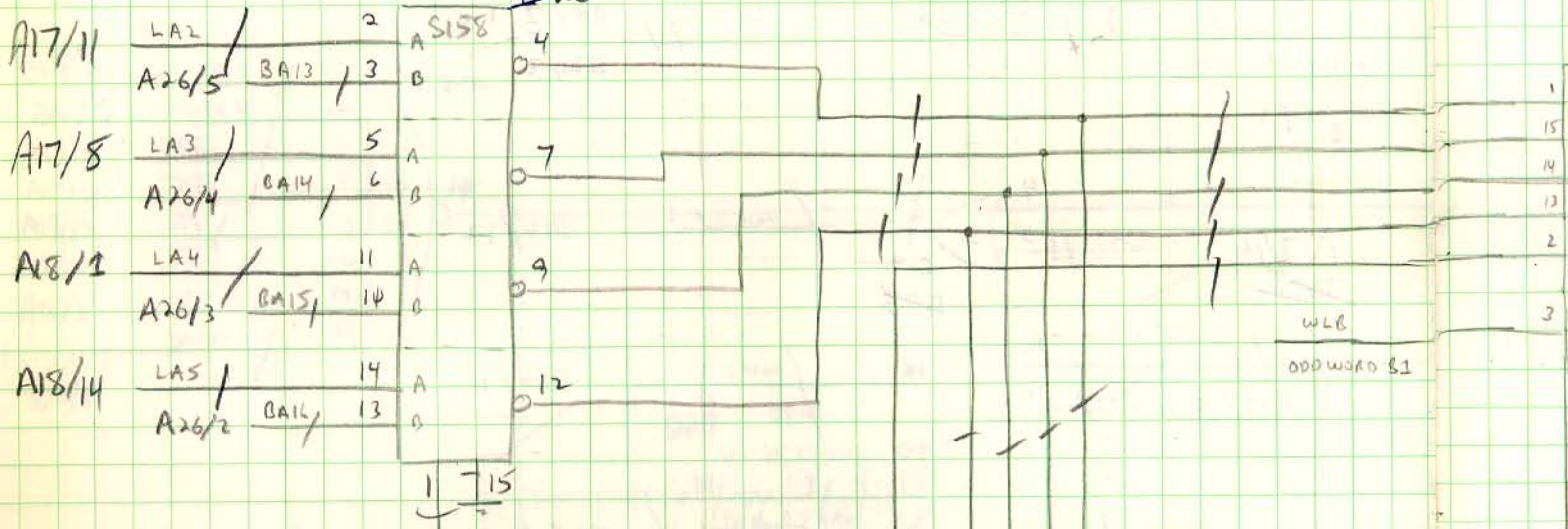
WLB
 WHB

21 March 78
ARB

Memory ORGANIZATION / ODD words

C18 Address Drivers

E26



WLB
ODD WORD B1

WLB
ODD WORD B2

E25/12

C19
~~F28~~

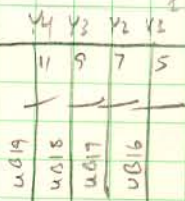
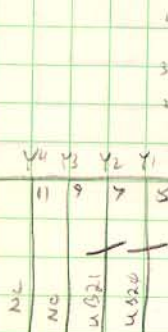
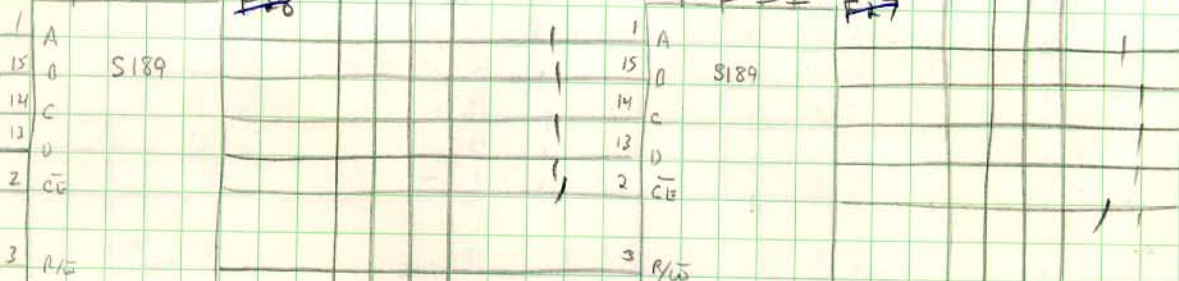
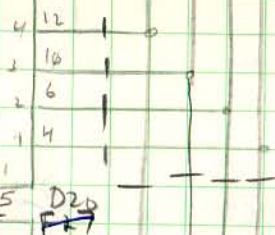
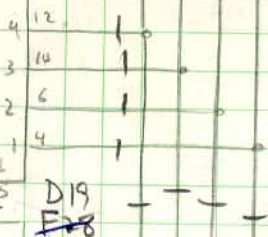
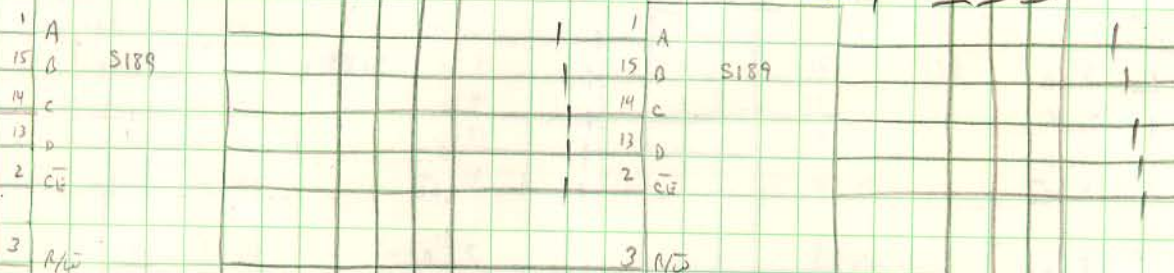
NS4
WG
LD5
LD4

C22
~~F27/6~~
~~F27/4~~

C20
~~F27~~

LD3
LD2
LD1
LD4

C21
~~F27/2~~
~~F27/16~~
~~F27/6~~
~~F27/4~~



D27/2
D27/6

D28/11
D28/15
D28/2
D26/6

21 March 78
ARB

B23/9
B23/10
B23/15
B23/16

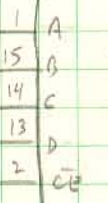
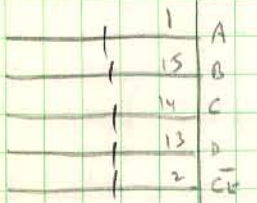
B23/9
B23/10
B23/15
B23/16

C24
~~E32~~

C23
~~E31~~

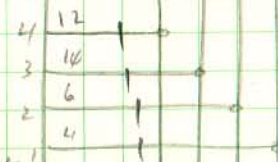
L115
L114
L113
L112

L115
L114
L113
L112



wHB 3
Even word B1

wHB 3

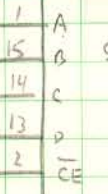
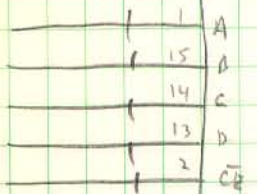


Y4 Y3 Y2 Y1
11 9 7 5

Y4 Y3 Y2 Y1
11 9 7 5

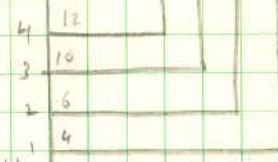
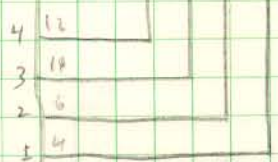
D24
~~E32~~

D23
~~E31~~



wHB 3
Even word B2

wHB 3



Y4 Y3 Y2 Y1
11 9 7 5

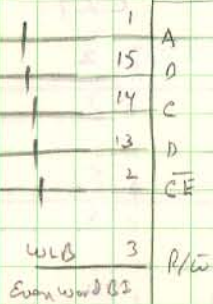
Y4 Y3 Y2 Y1
11 9 7 5

u015
u014
u013
u012

u011
u010
u009
u008

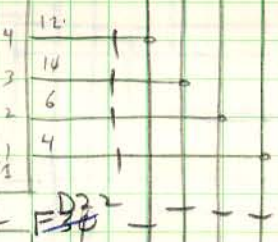
D32/11
D32/15
D32/2
P32/6

D31/11
D31/15
D31/2
D31/6

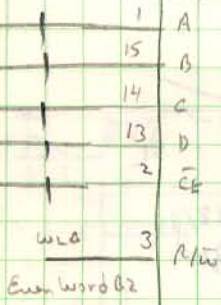


C22
~~F30~~

L07 B28/9
 L06 B28/10
 L05 B28/15
 L04 B28/16
 B28/4

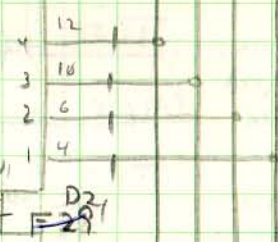


~~D22~~



C21
~~E29~~

L03 C19/12
 L02 C19/14
 L01 C19/16
 L00 C19/16
 C19/4



~~D21~~

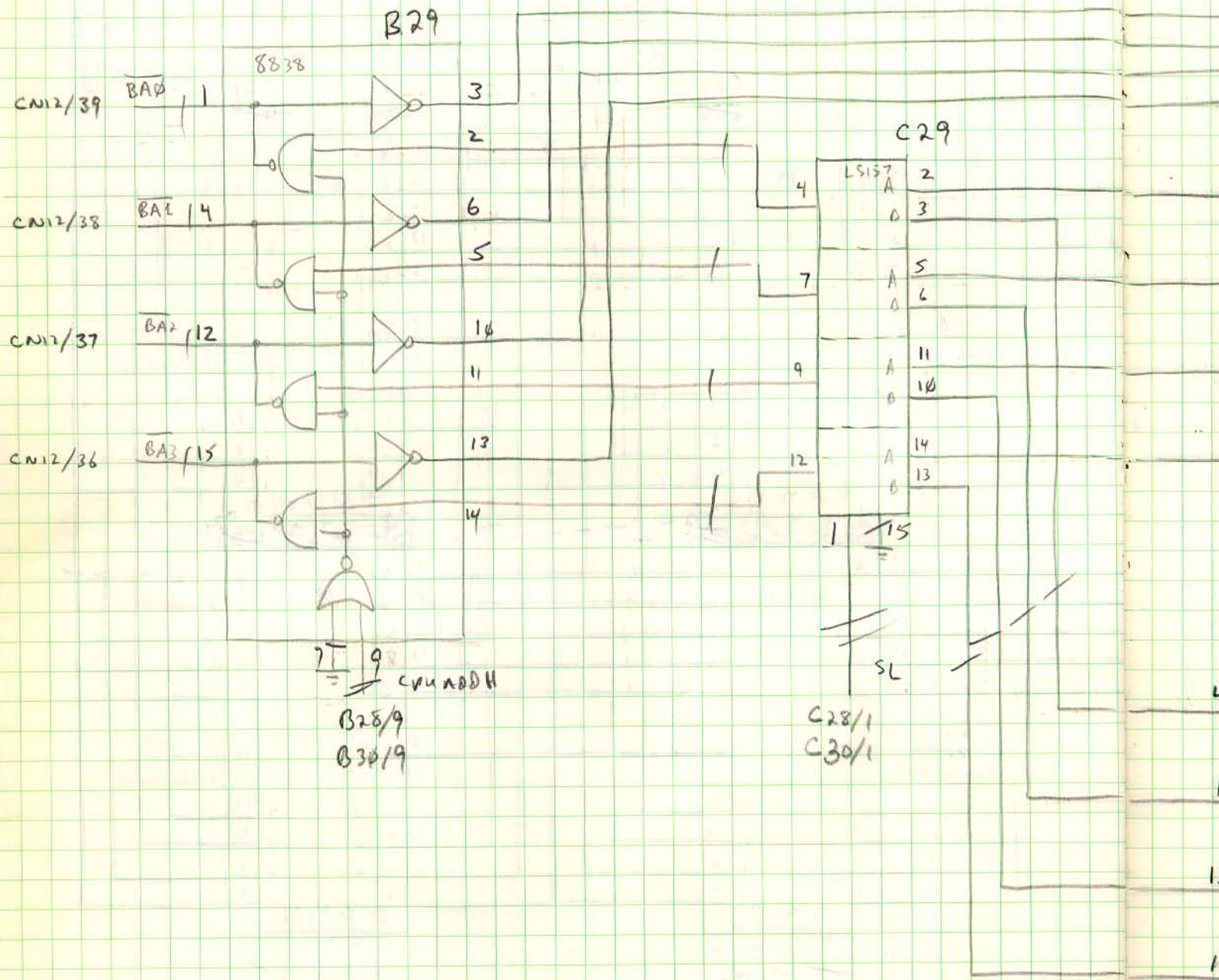
D30/11
 D30/15
 D30/2
 D30/6

D29/11
 D29/15
 D29/2

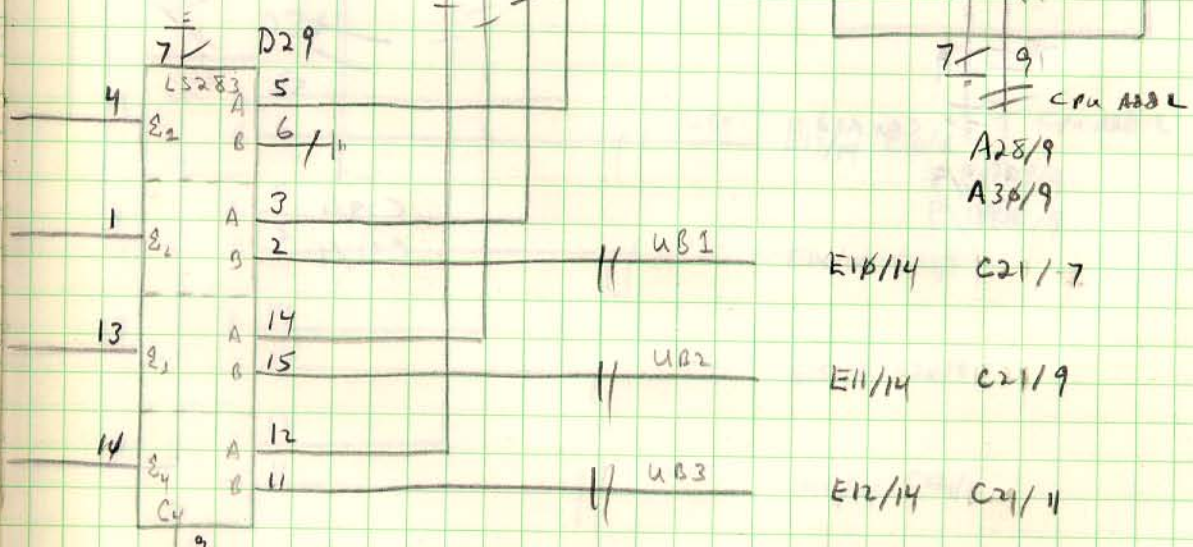
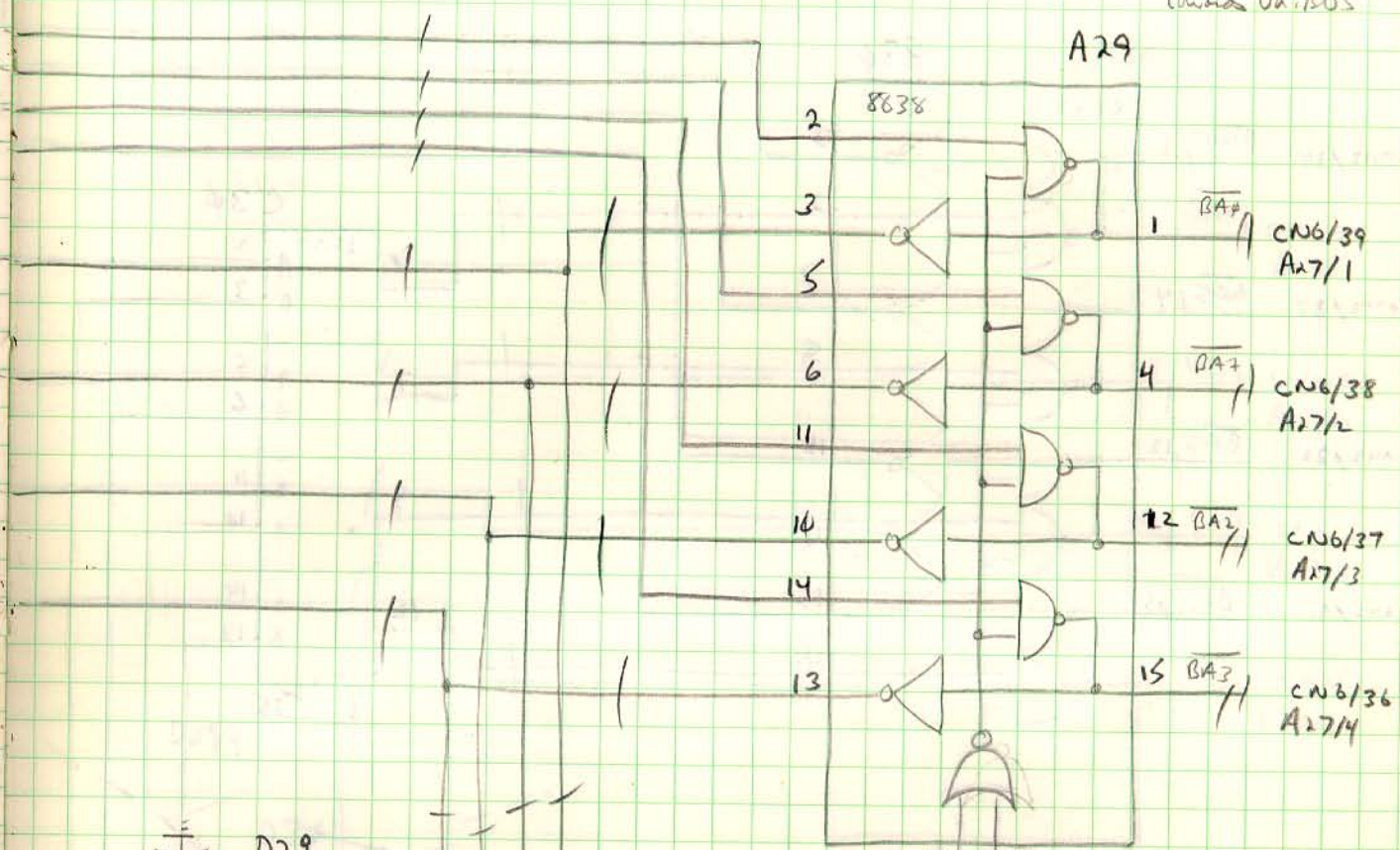
21 March 78
 ARD

Address Drivers & Relocation Address

forwards CPU



Trouble Unibus



D3p/7

21 March 78
ARD

B34

8838

CN12/34

BA4 / 1

CN12/33

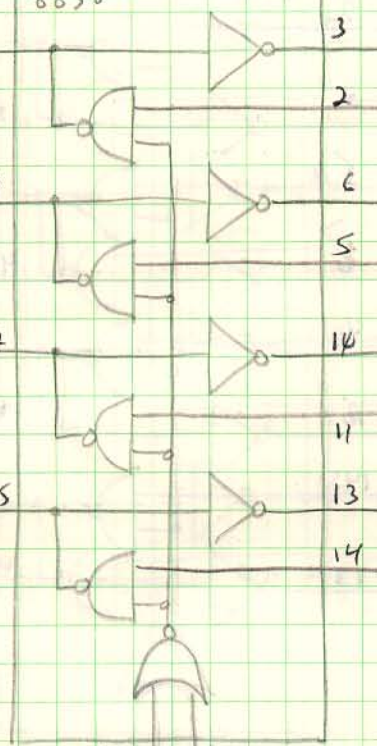
BA5 / 4

CN12/32

BA6 / 12

CN12/31

BA7 / 15



7 = 9

CPU ADDR

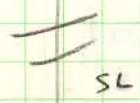
B29/9
B31/9

C34

LS157



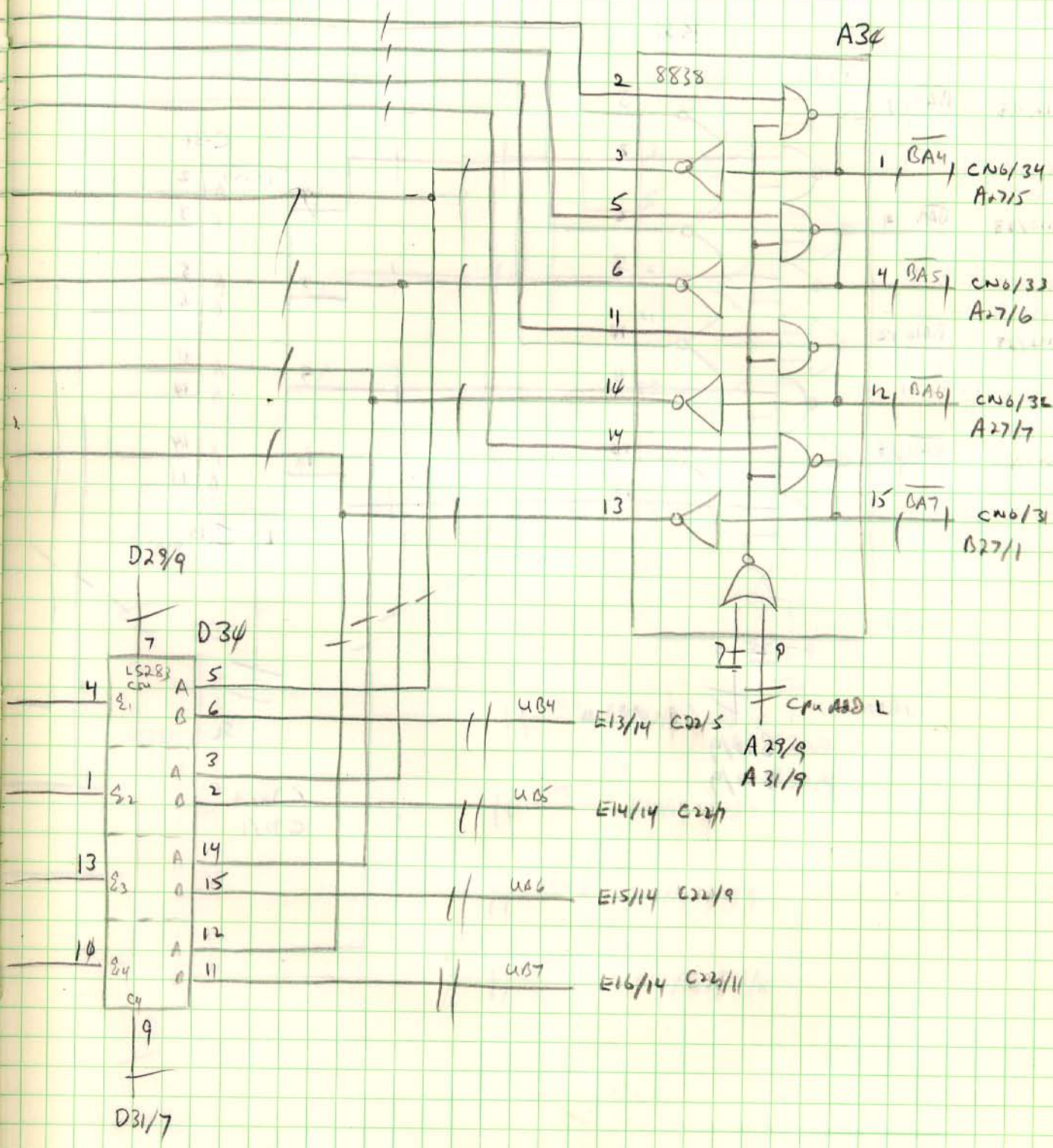
1 15



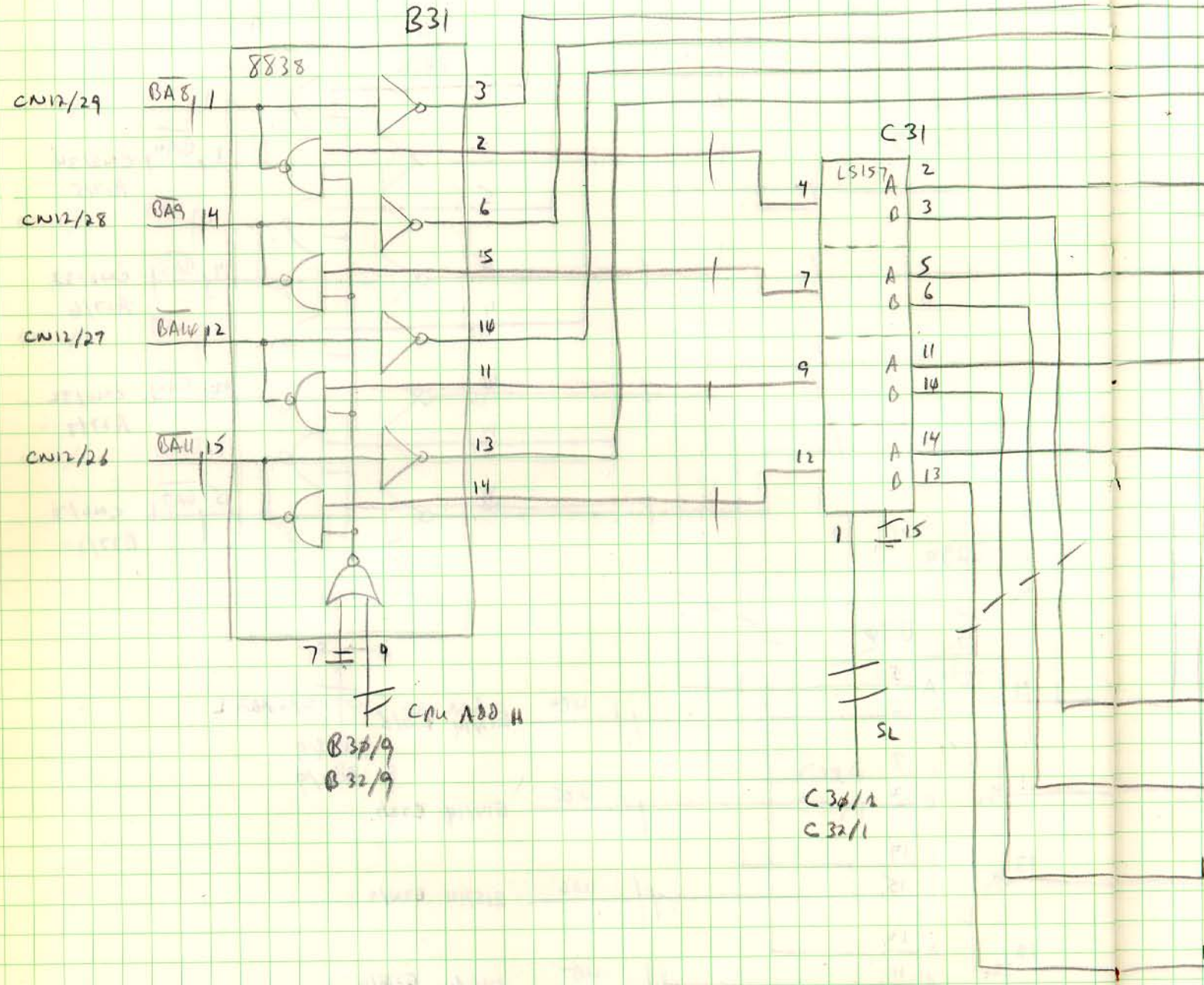
C29/1
C31/1

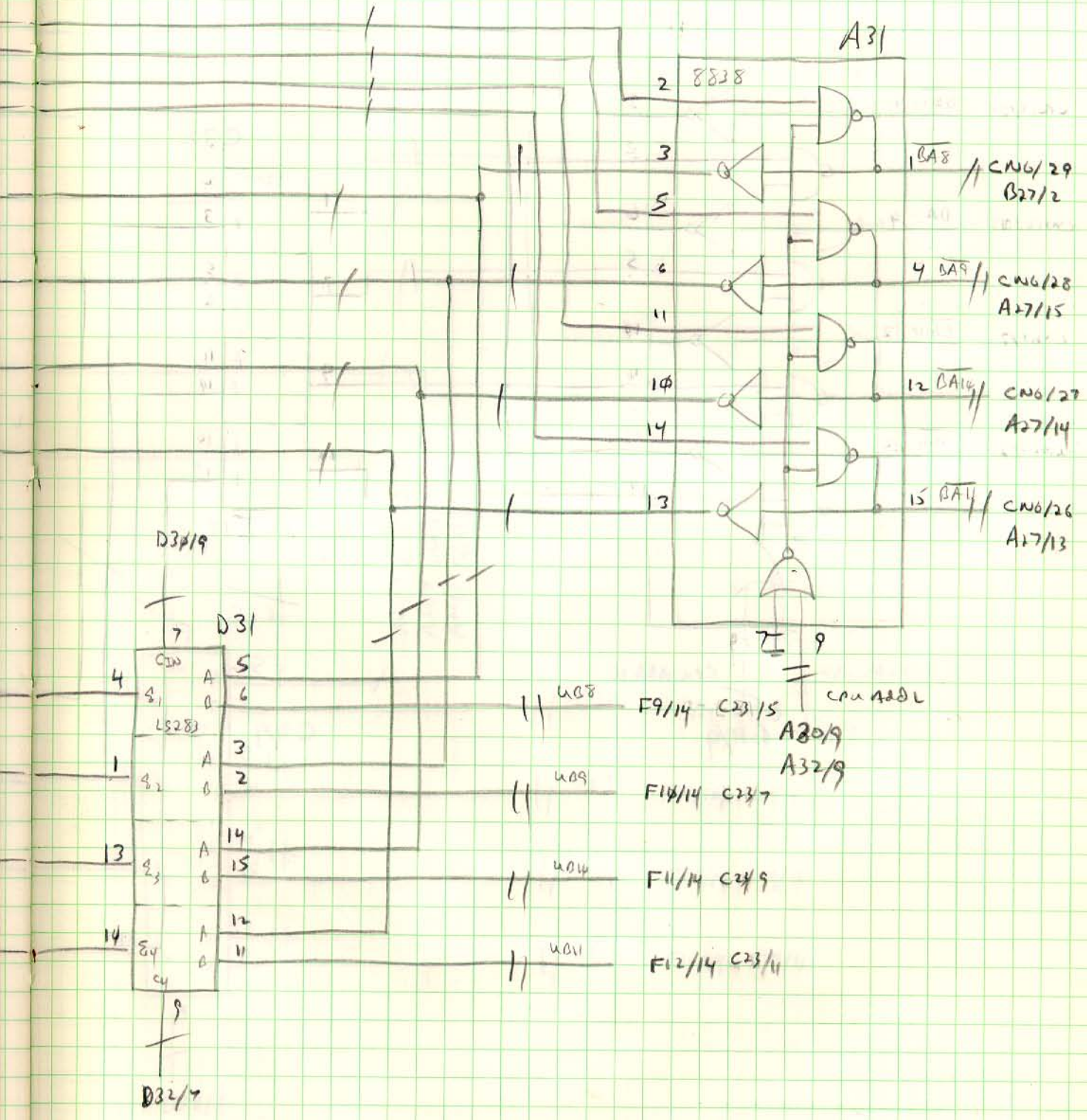
13

14



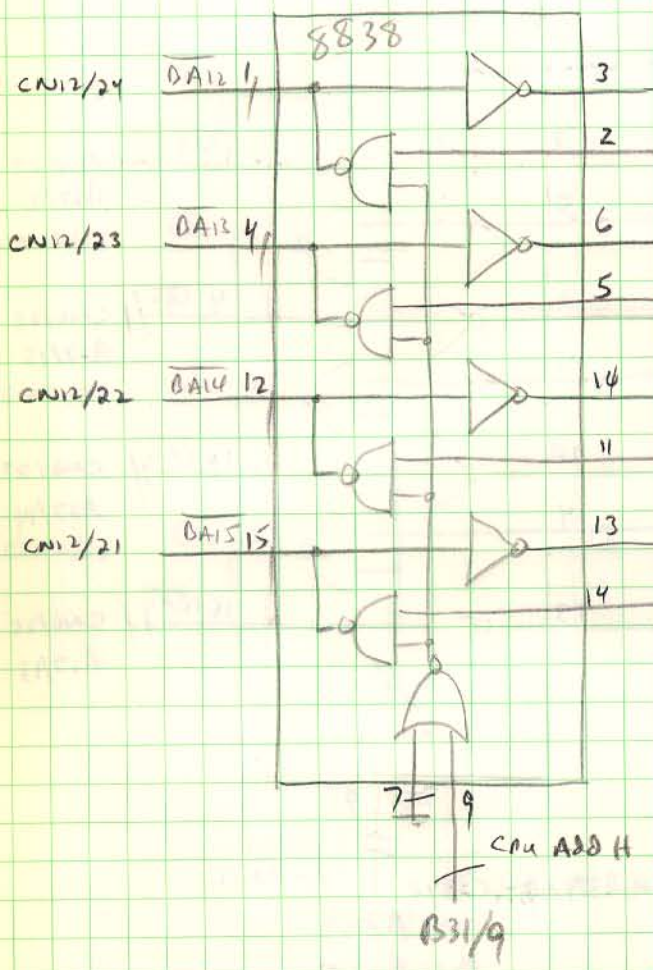
22 March 78
ARP



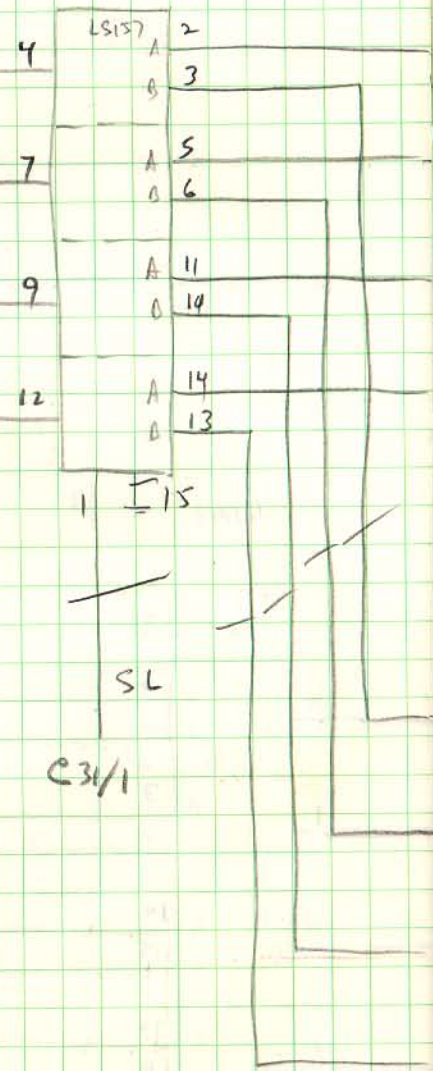


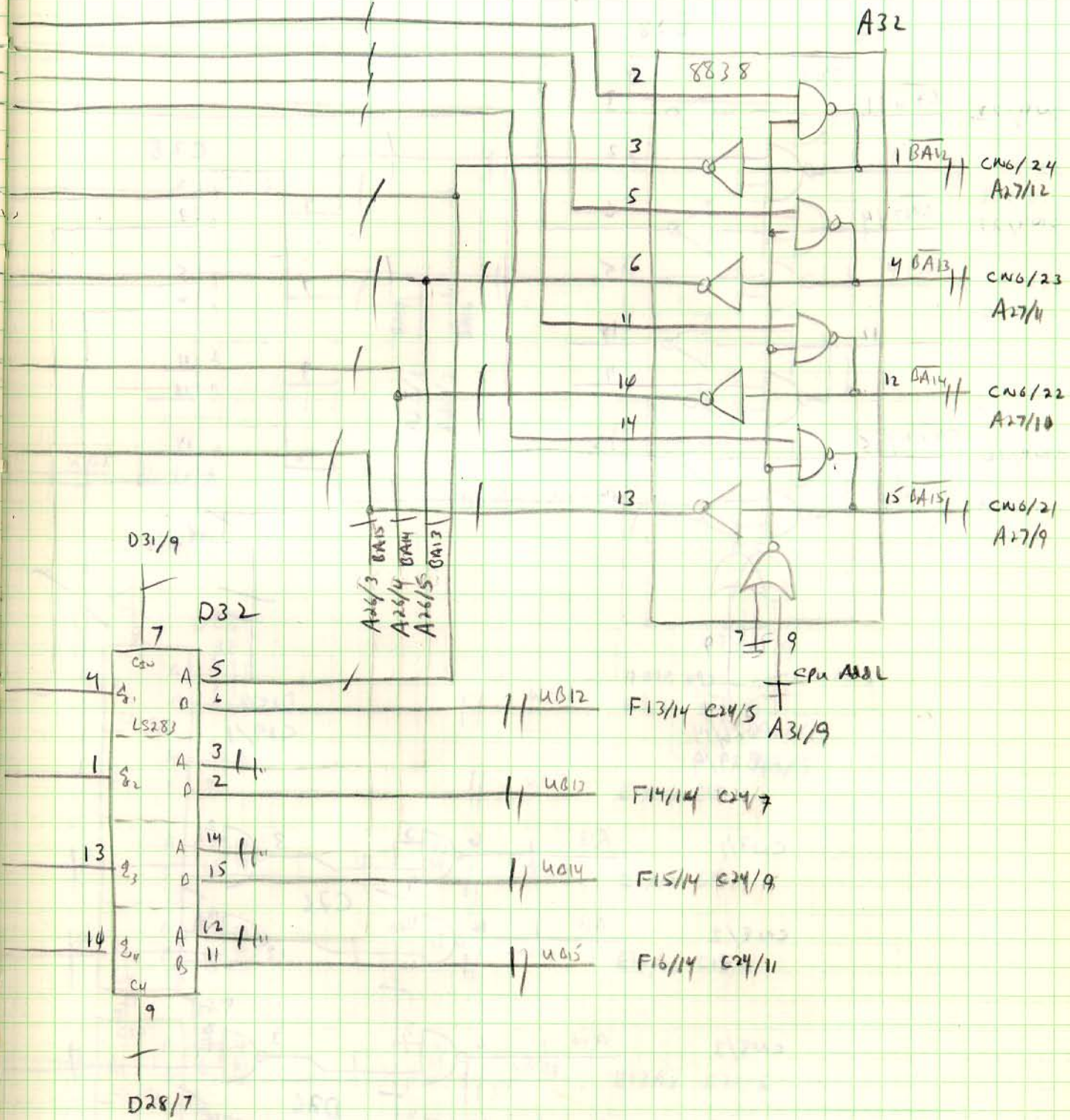
22 March 78
APD

B32



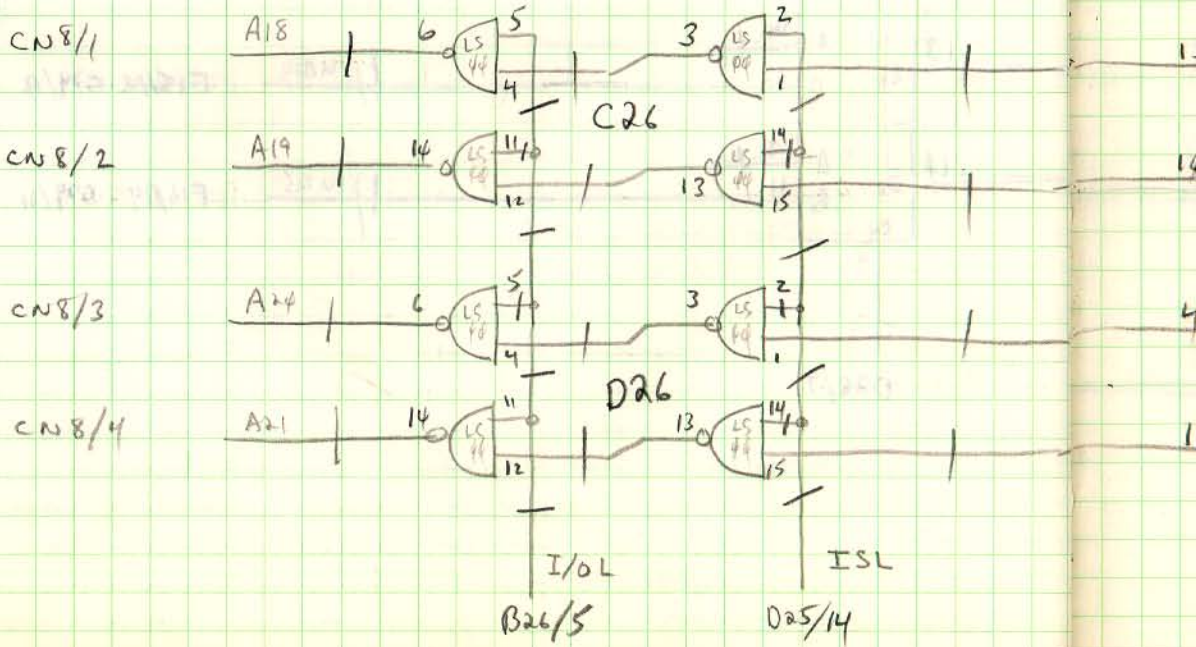
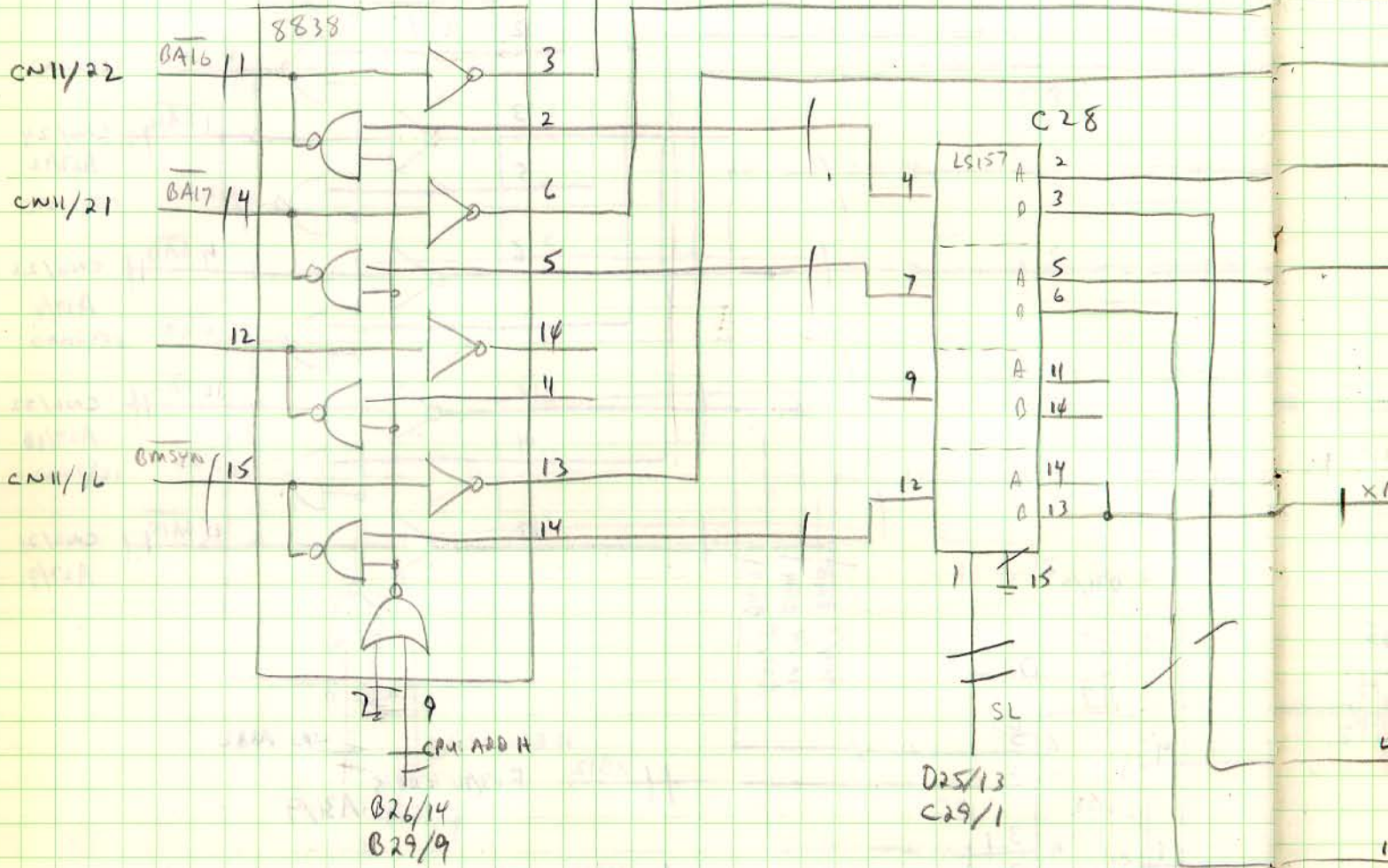
C32

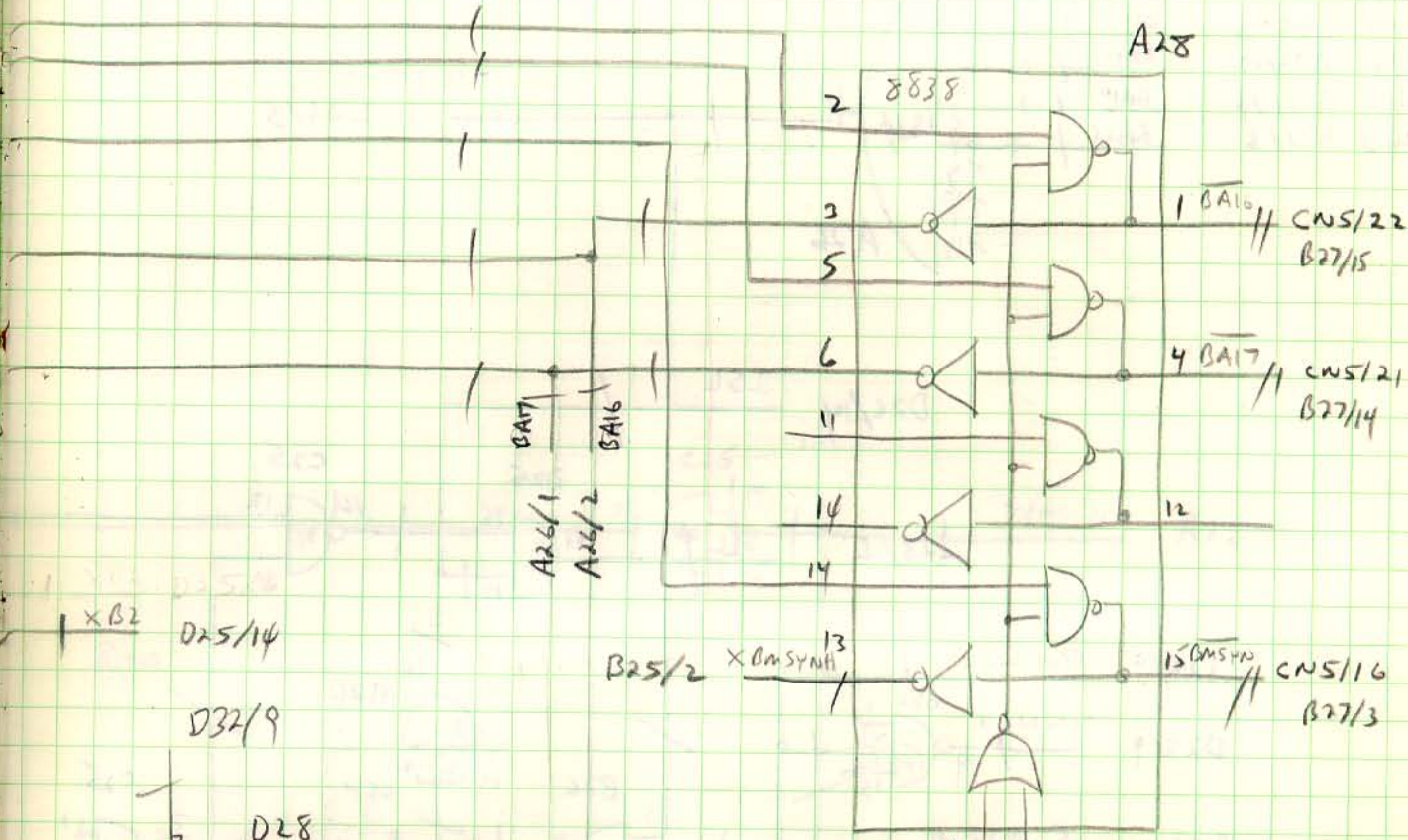




22 March 78
APD

B28





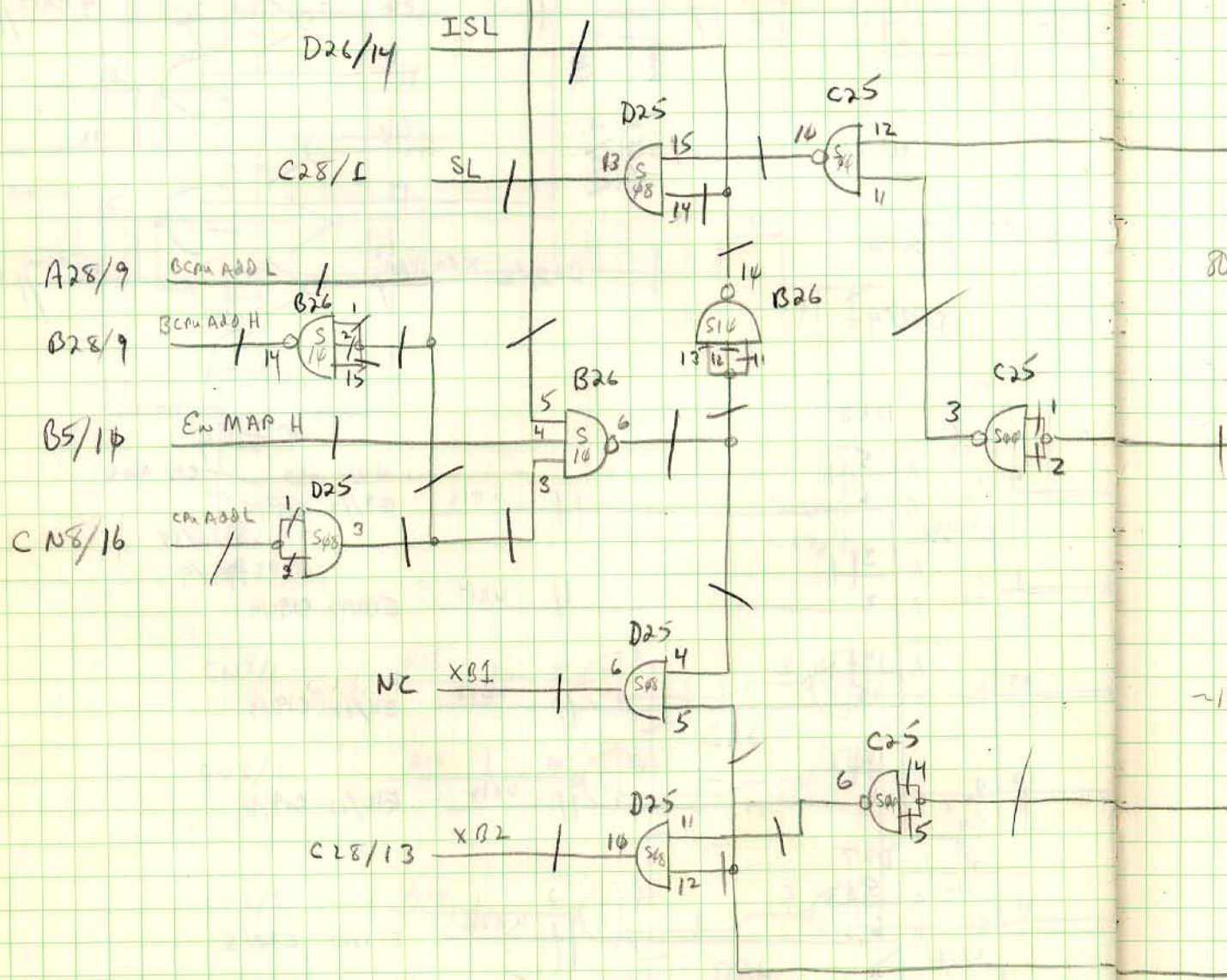
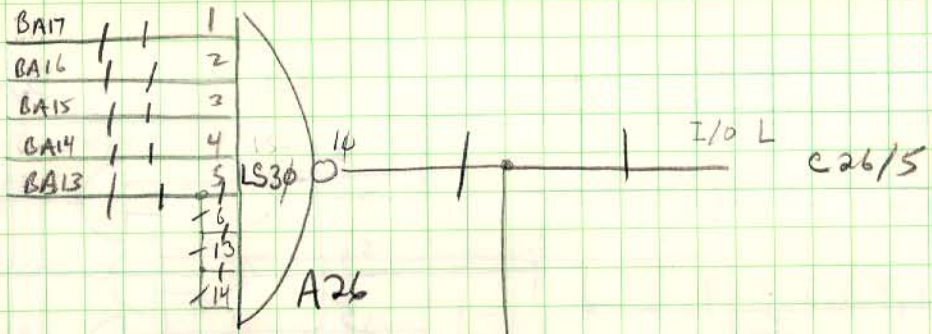
D28		D27	
4	Σ_1	A	5
	LS282	D	6
1	Σ_2	A	3
		D	2
13	Σ_3	A	14
		D	15
10	Σ_4	A	12
	C4	D	11
4	Σ_1	A	5
	LS283	D	6
1	Σ_2	A	3
		D	2

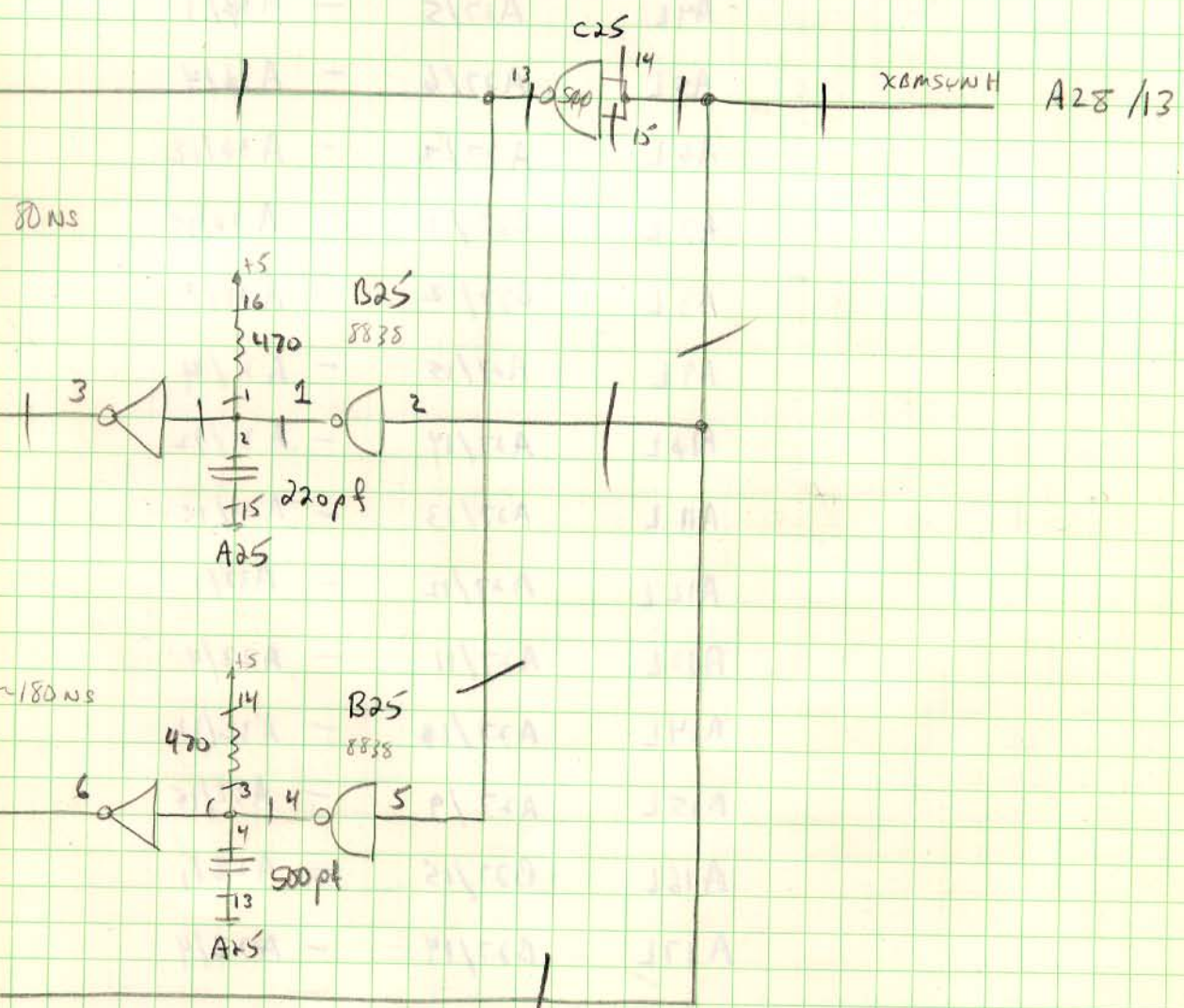
u016	E9/13	E19/15
u017	E18/13	E19/17
u018	E11/13	C19/19
u019	E12/13	C19/11
u024	E13/13	C20/5
u021	E14/13	C20/7

22 March 78
APD

UNIBUS MAP Control Logic

- E26/6 A28/6
- E26/13 A28/3
- E26/14 A32/13
- E26/6 A32/14
- E26/3 A32/6

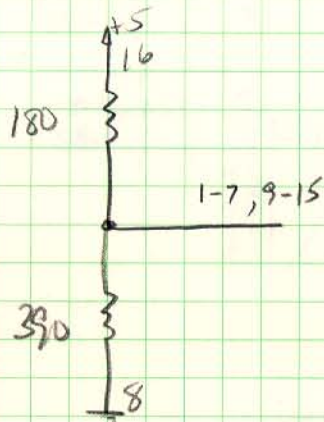




22 March 78
ABD

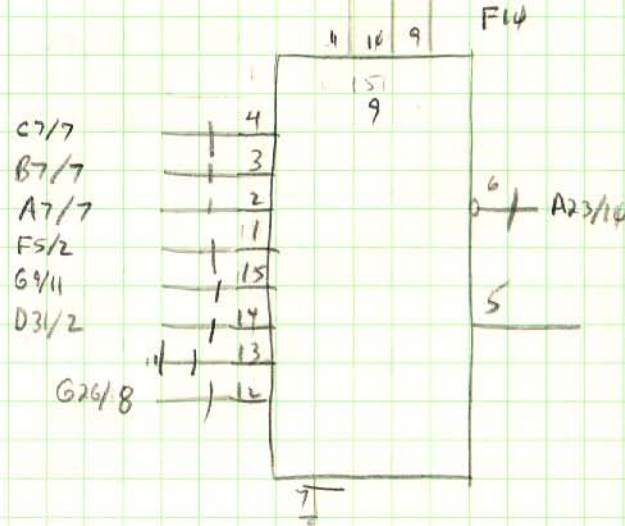
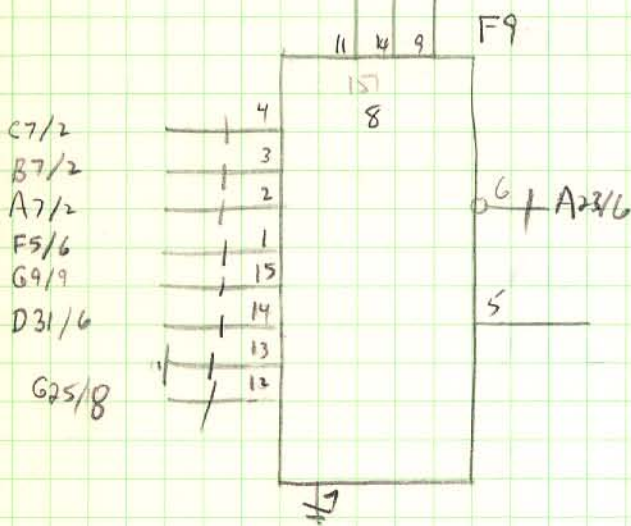
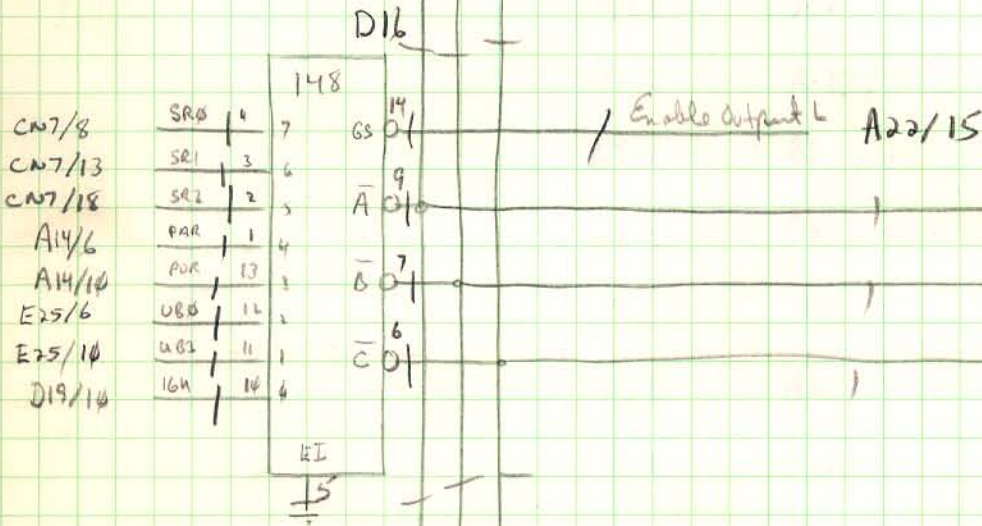
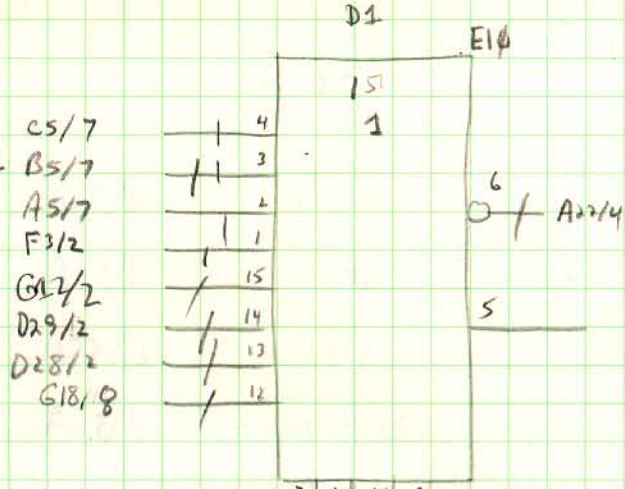
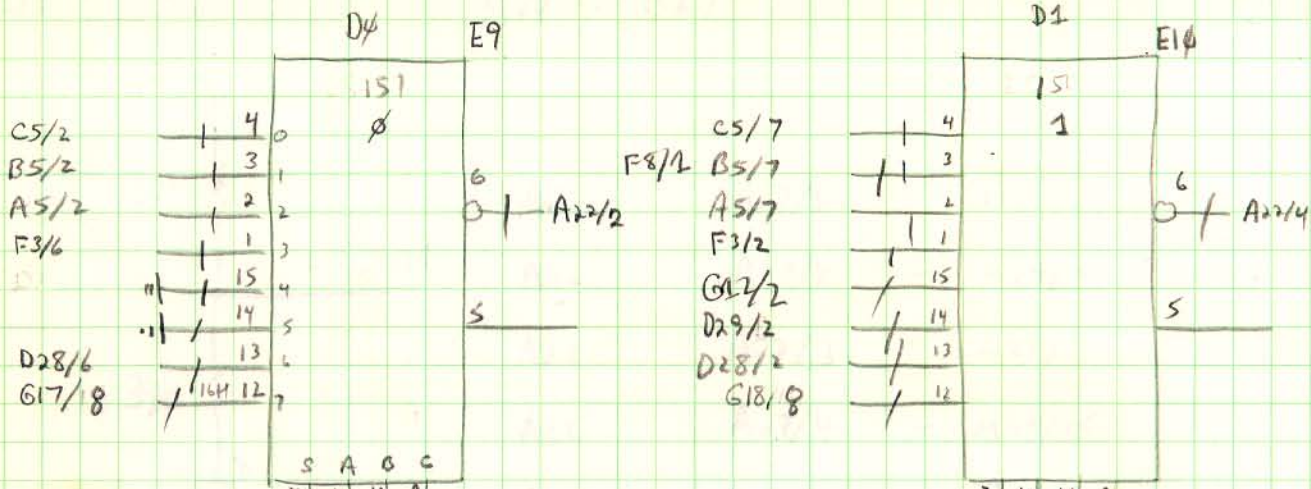
BUS Terminations

A27 / B27



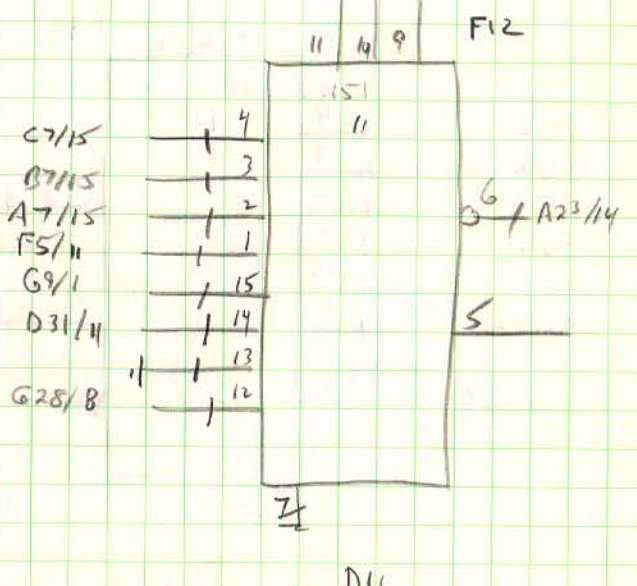
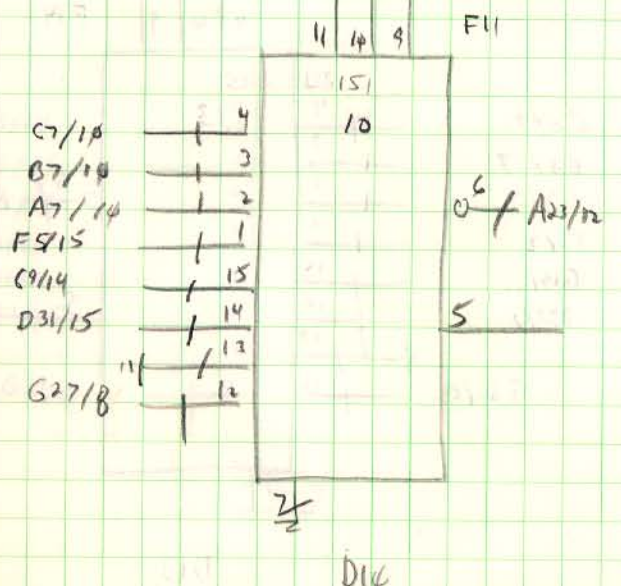
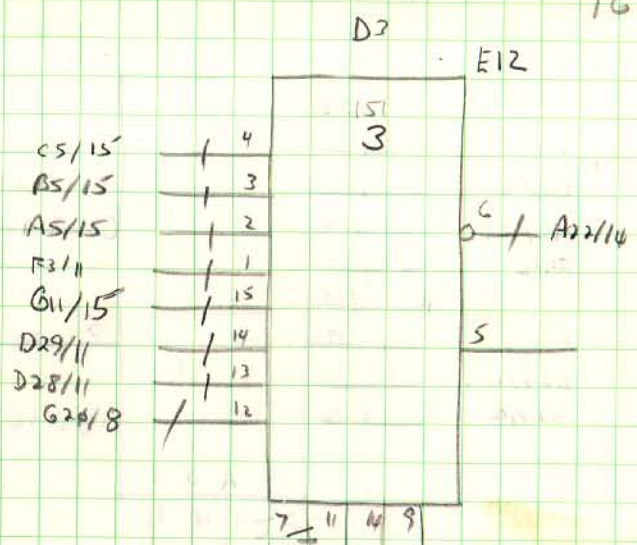
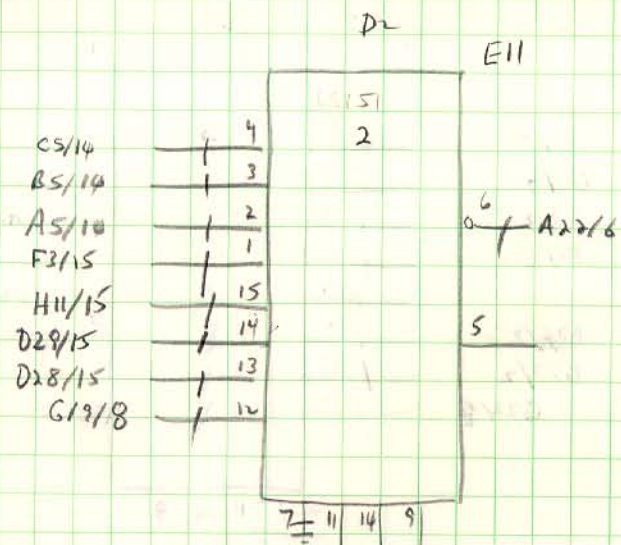
A0L	A27/1	-	A29/1
A1L	A27/2	-	A29/4
A2L	A27/3	-	A29/12
A3L	A27/4	-	A29/15
A4L	A27/5	-	A30/1
A5L	A27/6	-	A30/4
A6L	A27/7	-	A30/12
A7L	B27/1	-	A30/15
A8L	B27/2	-	A31/1
A9L	A27/15	-	A31/4
A10L	A27/14	-	A31/12
A11L	A27/13	-	A31/15
A12L	A27/12	-	A32/1
A13L	A27/11	-	A32/4
A14L	A27/10	-	A32/12
A15L	A27/9	-	A32/15
A16L	B27/15	-	A28/1
A17L	B27/14	-	A28/4
BmsynL	B27/3	-	A29/15

Data → BUS MULTIPLEXER

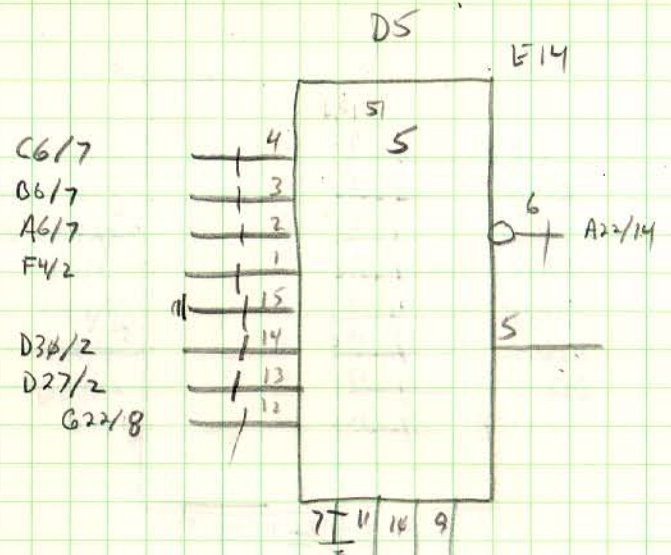
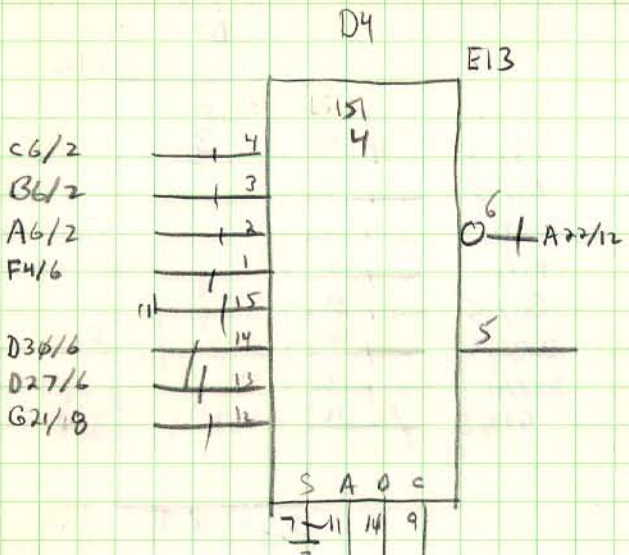


D8

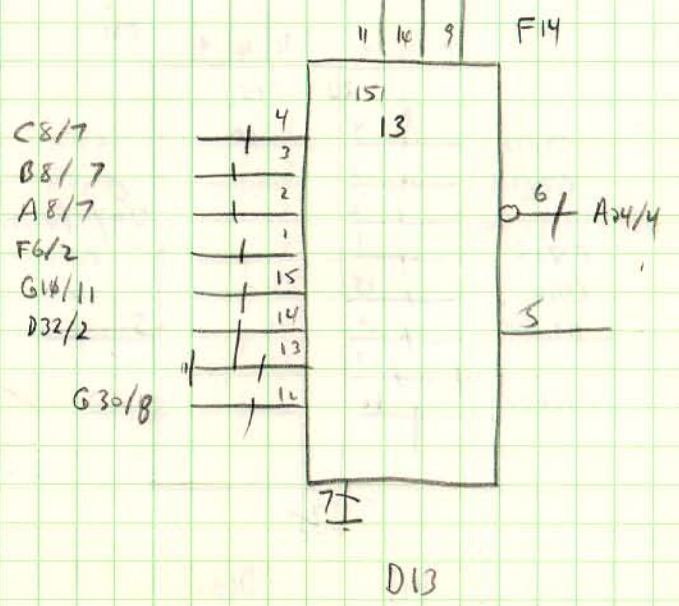
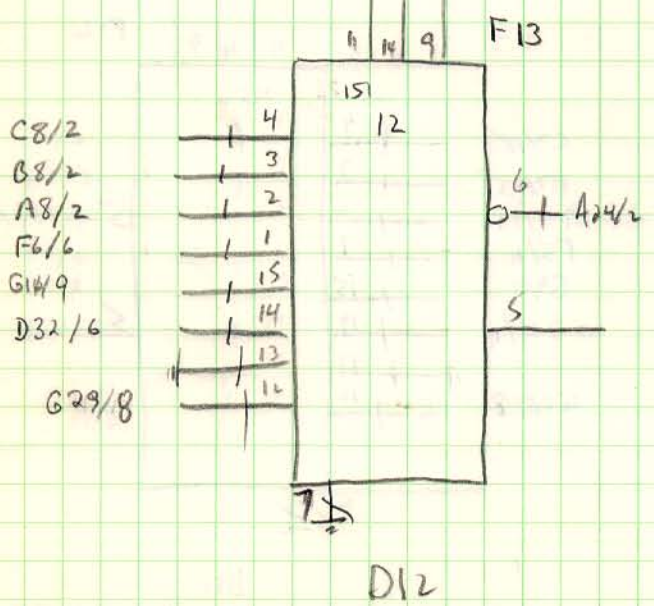
D9



22 March 78
APD



C6/
B6/
A6/
F4/
I9/
D30/



C8/
B8/
A8/
F6/
G14/
D32/

D6

E15



C6/14
B6/14
A6/14
F4/15
I9/11
D30/15

G23/8

7 14 9

D7

E16



C6/15
D6/15
A6/15
F4/11

D30/11

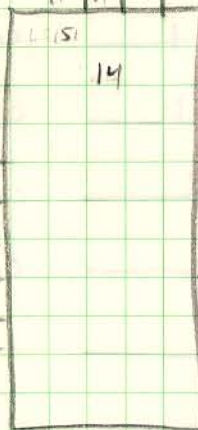
G24/8

7 14 9

77

11 14 9

F15



C8/14
B8/14
A8/14
F6/15
G10/14
D32/15

G31/8

7

D14

11 14 9

F16



C8/15
D8/15
A8/15
F6/11

D32/11

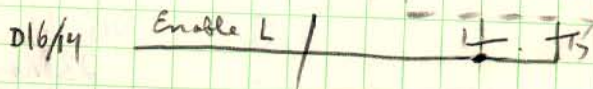
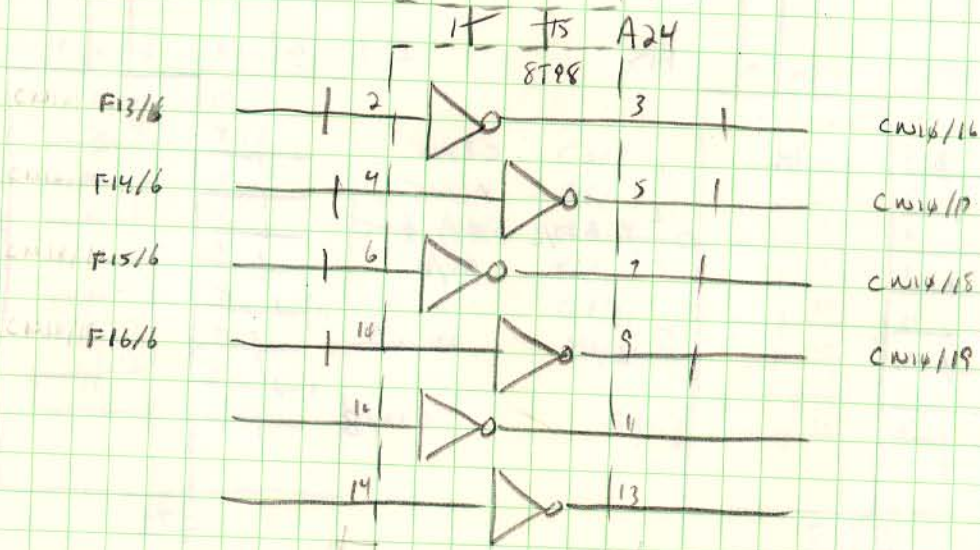
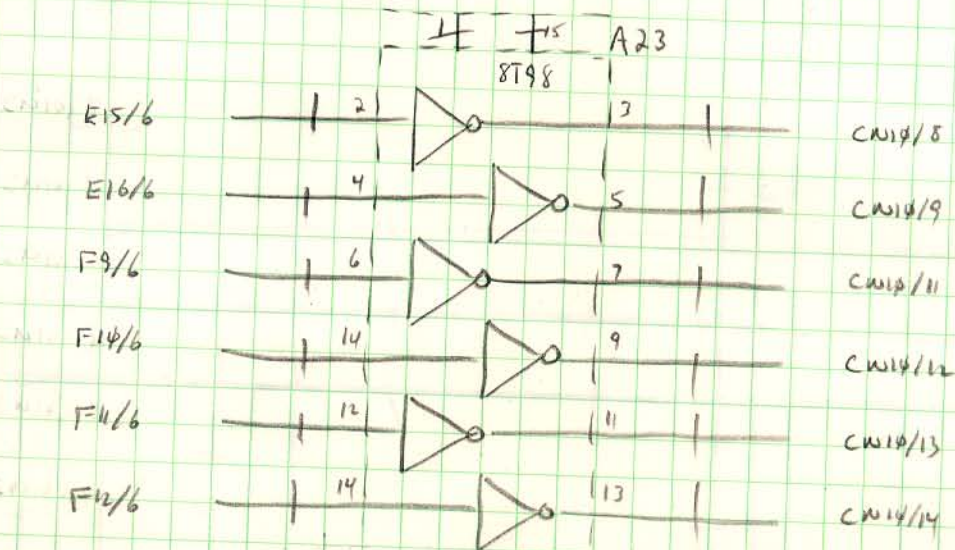
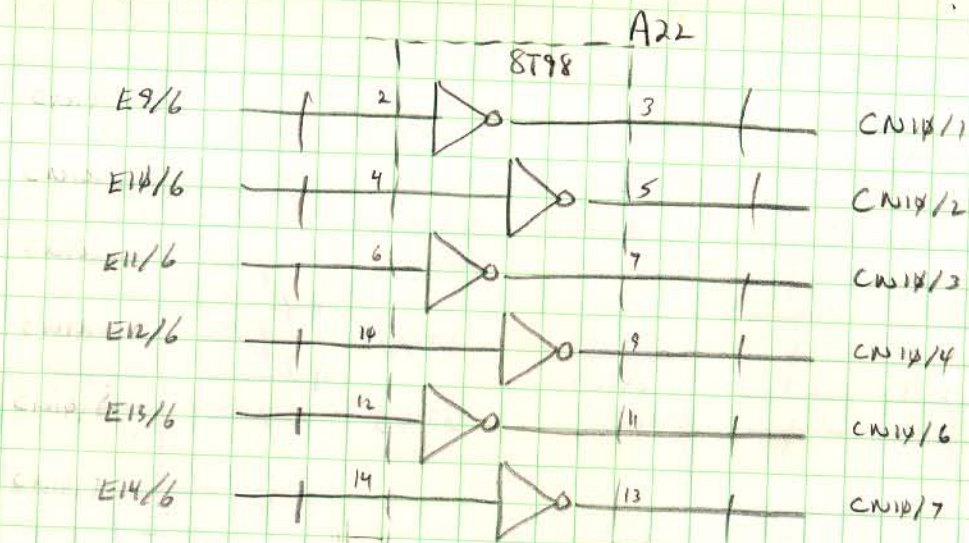
G32/8

7

D15

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APB

Tristate BUS Drivers



Row A

1	—	
2	—	
3	S32	57, 61
4	L808	57
5	LS175	57
6	LS175	57
7	LS175	57
8	LS175	57
9	S88	57, 61
10	S157	62
11	S157	62
12	S157	63
13	S157	63
14	∅	54
15	S260	54
16	S260	54
17	LS75	45
18	LS75	45
19	LS75	45
20	LS75	45
21	S44	54, 87
22	8798	78
23	8798	78
24	8798	78
25	RES	74
26	LS30	74
27	RES	75
28	8838	73
29	8838	69
30	8838	74
31	8838	71
32	8838	72

1	—	
2	—	
3	S153	61
4	S158	61
5	LS175	58
6	LS175	58
7	LS175	58
8	LS175	58
9	LS153	61
10	S44	55
11	75	45
12	LS132	55, 66
13	RES	54, 55, 66
14	38	54, 55, 66
15	LS30	54
16	LS34	54
17	LS266	41
18	LS266	41
19	S74	41
20	S48	41, 42
21	LS75	46
22	LS75	46
23	LS75	46
24	LS75	46
25	8838	74
26	S14	74
27	RES	75
28	8838	73
29	8838	69
30	8838	74
31	8838	71
32	8838	72

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AFO

Row C

1	—	
2	—	
3	S158	61
4	S158	61
5	LS175	57
6	LS175	57
7	LS175	57
8	LS175	57
9	S20	55
10	S10	55, 64
11	S00	55, 64
12	RES	55
13	LS133	64
14	LS133	64
15	\$132	55
16	—	
17	switches	41
18	RES	41
19	S74	42
20	S08	41, 43
21	S32	41
22	LS30	66
23	—	
24	—	
25	S00	74
26	LS00	73
27	—	
28	LS157	73
29	LS157	69
30	LS157	70
31	LS157	71
32	LS157	72

1	123	54
2	RES	54
3	S158	61
4	S157	61
5	LS157	57
6	LS157	57
7	LS157	57
8	LS157	57
9	S48	54, 55
10	S74	55, 64
11	S74	55, 64
12	S14	55
13	S260	64
14	<hr/>	
15	<hr/>	
16	148	76
17	<hr/>	
18	S48	47
19	S74	47
20	LS74	47
21	33	47
22	123	66
23	RES	41, 66
24	<hr/>	
25	S48	74
26	LS44	73
27	LS283	73
28	LS283	73
29	LS283	69
30	LS283	74
31	LS283	71
32	LS283	72

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ABD

Raw E

1	RES	62	
2	S157	62	
3	RES	62	
4	S157	62	
5	RES	63	
6	S157	63	
7	RES	63	
8	S157	63	
9	151		76
10	151		76
11	151		76
12	151		76
13	151		77
14	151		77
15	151		77
16	151		77
17	S21		42
18	S00		42
19	S74		42
20	S132		41, 42, 43
21	RES		42
22	RES		41, 42
23	—		
24	—		
25	32		66
26	S158		67
27	S189		67
28			67
29			68
30			68
31			68
32	S189		68

1	LS139	54
2	<u>LS139</u>	
3	LS283	62
4	LS283	62
5	LS283	63
6	LS283	63
7	S21	63
8	S157	63
9	151	76
10	151	76
11	151	76
12	151	76
13	151	77
14	151	77
15	151	77
16	151	77
17	S04	43
18	164	42
19	LS193	42
20	123	42
21	RES	42
22	S132	42, 46
23	<u> </u>	
24	<u> </u>	
25	LS139	66
26	S158	67
27	S189	67
28		67
29		68
30		68
31		68
32	S189	68

9 April 78
ARR

Row G

1	93410	
2		}
3		
4		
5		
6		
7		
8	93410	
9	LS85	56
10	LS85	56
11	LS00	56
12	LS30	56
13	S00	43
14	S139	43
15	SP8	43
16	BT95	48
17	YPD 414-E	}
18		
19		
20		
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		
31		
32	YPD414E	

1	93416	
2		} 59
3		
4		
5		
6		
7		
8	93410	
9	RES	56
10	---	
11	LS86	56
12	LS14	56
13	Sφφ	43
14	LS153	44
15	Sφ8	43
16	8T95	48
17	YPD 414-E	} 49
18		
19		
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21		
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28		
29		
30		
31		
32	YPD 414-E	

9 April 78
ARD

Row I

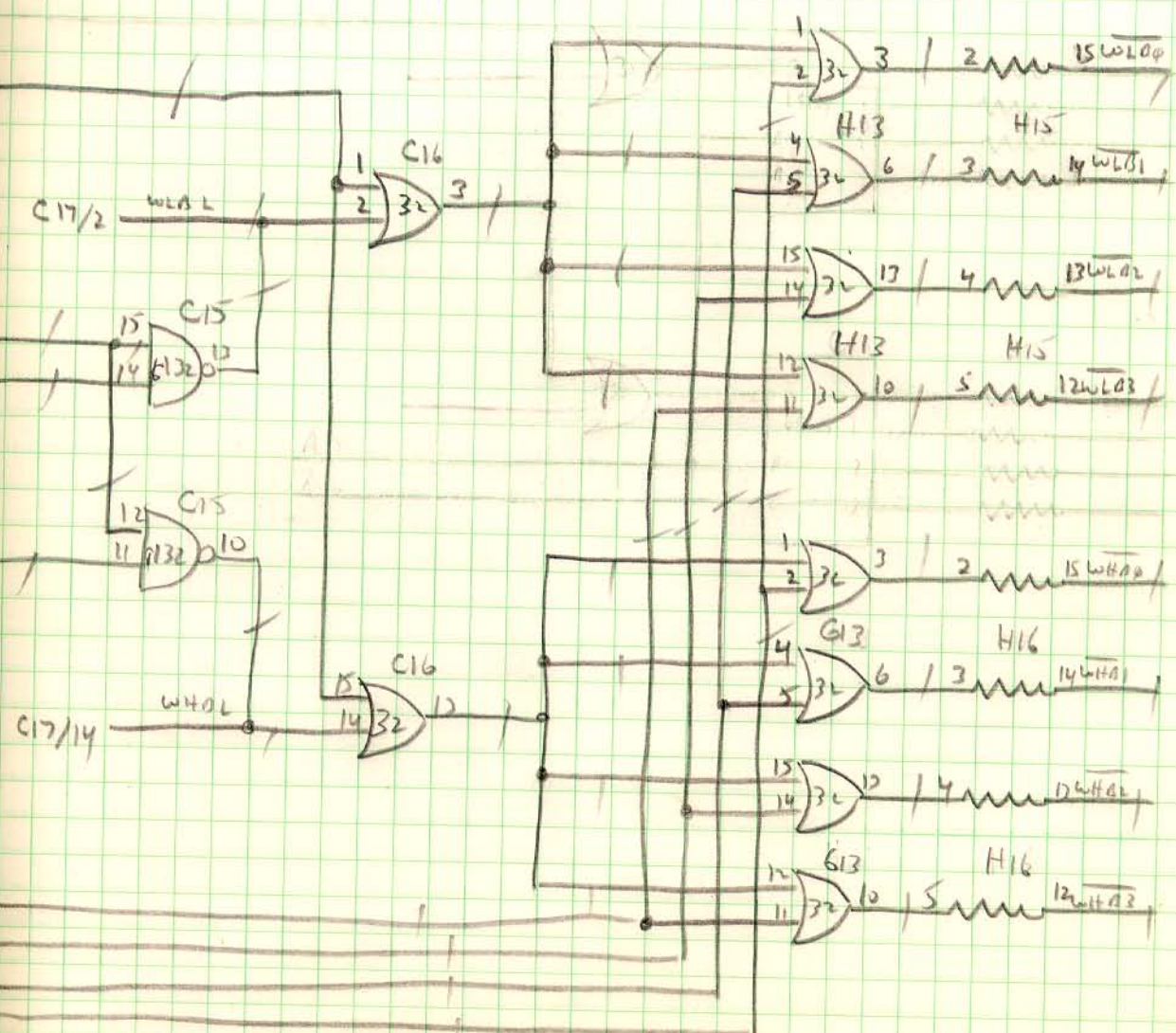
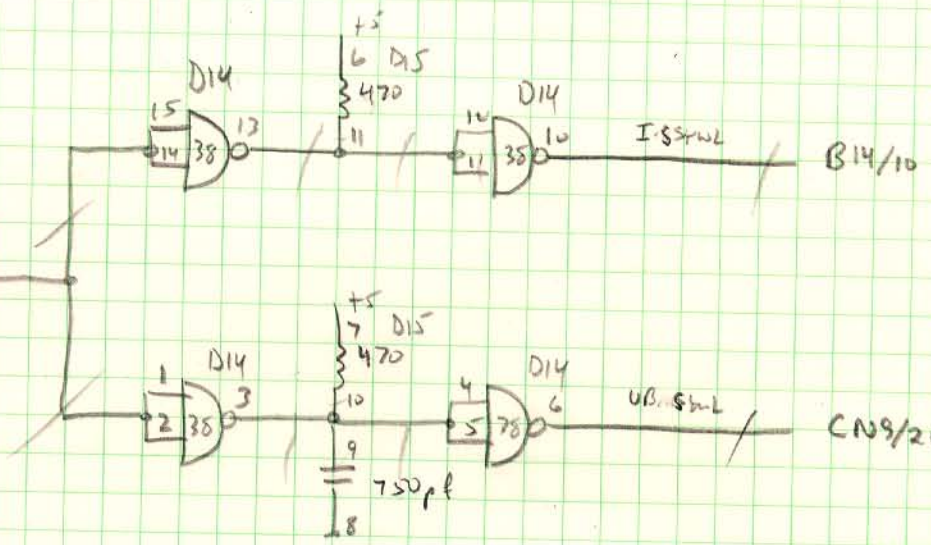
1	—	
2	93410	60
3	93410	60
4	93410	60
5	—	
6	—	
7	93410	60
8	—	
9	RES	59, 60
10	—	
11	—	
12	—	
13	LS193	44
14	LS153	44
15	32	43
16	8T95	48
17	YPD 414-E	
18		} 49
19		
20		
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		
31		
32	YPD 414-E	

1	93414	
2		
3		
4		
5		
6		
7	93414	
8	-----	
9	RES	59,60
10	-----	
11	-----	
12	-----	
13	LS193	44
14	LS153	44
15	8T98	44
16	8T95	48
17	HPD 414 E	
18		
19		
20		
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22		
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25		
26		
27		
28		
29		
30		
31		
32	HPD 414 E	

} 60

} 49

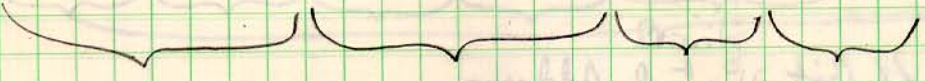
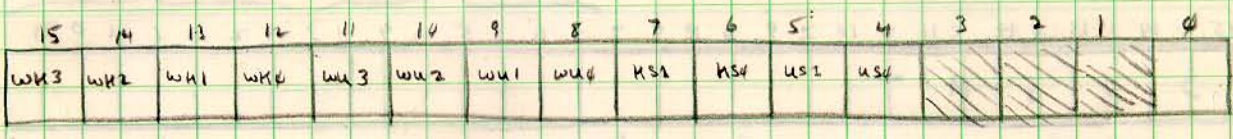
9 April 78
ARR



Status Register 1 (SR1)

17 / 7 7 7 5 7 4 8

Read/Write



Specifies one of sixteen PAR/PDR groups for reading or writing when Accessing Kernel Addressing 17772300-2317, 17772340-2357
Enabled only if Extended MM6T enabled

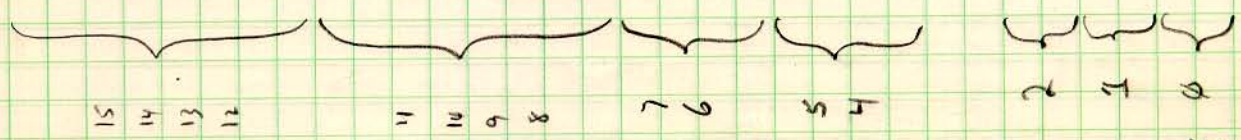
Specifies one of sixteen PAR/PDR groups for Reading or writing when Accessing User Addressing 1777600-617, 1777640-657
Enabled only if Extended MM6T Enabled

Kernel PAR/PDR Bank Select
Enabled only if Extended MM6T Enabled

User PAR/PDR Bank Select
Enabled only if Extended MM6T Enabled

UNIVS MAP Enable } Removed Nov 2009
18 bit/22 bit MM6T } See page 89

Enable Extended MM6T



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ADD

Status Register SRI

				mmGT1 WHAL		CN7/12	
				9	B8		
B24/8	D8/14	LD15	13	D	LS175a 15	WH3	F16/3 CH/14
B24/11	D8/11	LD14	12	D	q 10	WH2	F15/3 CH/11
B24/14	D8/5	LD13	5	D	q 7	WH1	F14/3 CH/5
B24/1	D8/2	LD12	4	D	q 2	WH0	F13/3 CH/2

				mmGT1 WHAL		CN7/11	
				9	B7		
B23/8	D7/14	LD11	13	D	LS175a 15	WH3	F12/3 CH/13
B23/11	D7/11	LD10	12	D	q 10	WH2	F11/3 CH/10
B23/14	D7/5	LD9	5	D	q 7	WH1	F10/3 CH/6
B23/1	D7/2	LD8	4	D	q 2	WH0	F9/3 CH/3

				mmGT1 WHAL		CN7/11	
				9	B6		
B22/8	D6/14	LD7	13	D	LS175a 15	HS1	E16/3 CH/5
B22/11	D6/11	LD6	12	D	q 10	HS0	E15/3 CH/2
B22/14	D6/5	LD5	5	D	q 7	US1	E14/3 CH/6
B22/1	D6/2	LD4	4	D	q 2	US0	E13/3 CH/3

				mmGT1 WHAL		CN7/11	
				9	B5		
B21/8	D5/14	LD3	13	D	LS175a 15		E12/3
B21/11	D5/11	LD2	12	D	q 10	EMAP	E11/3
B21/14	D5/5	LD5	5	D	q 7	18/22/24	E10/3
B21/1	D5/2	LD6	4	D	q 2	Estimate	E9/3

Removed
Nov 2009
see page 89

3
INST CLEAR
A8/1
C5/1

Data → BUS MULTIPLEXER

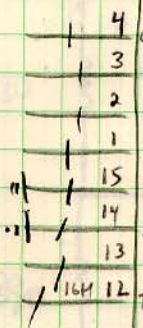
D4

E9

D1

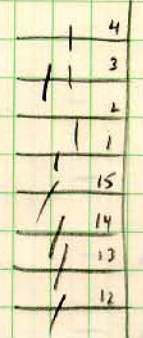
E10

- C5/2
- B5/2
- A5/2
- F3/6
- D28/6
- G17/8



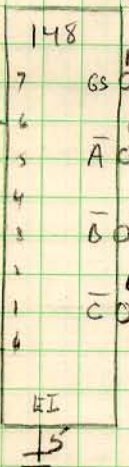
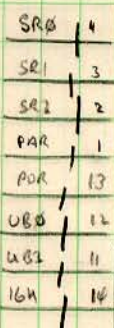
NW 2009
See page 89

- C5/7
- B5/7
- A5/7
- F3/2
- G17/2
- D29/2
- D28/2
- G18/8



D16

- C17/8
- C17/13
- C17/18
- A14/6
- A14/10
- E25/6
- E25/10
- D19/10



Enable output L A22/15

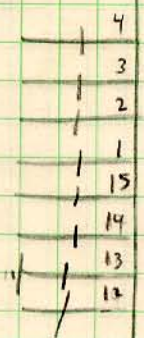
D8

F9

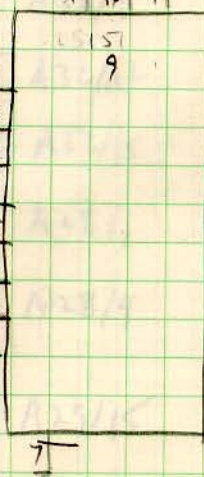
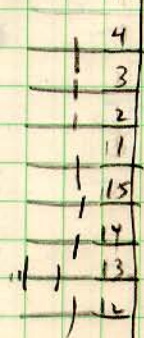
D9

F10

- C7/2
- B7/2
- A7/2
- F5/6
- G9/9
- D31/6
- G25/8

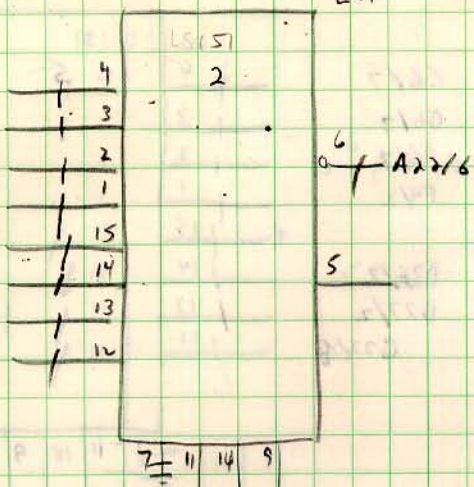


- C7/7
- B7/7
- A7/7
- F5/2
- G9/11
- D31/2
- G26/8

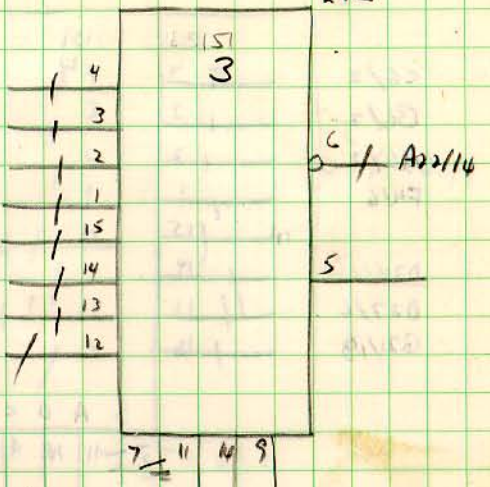


NOV 2009
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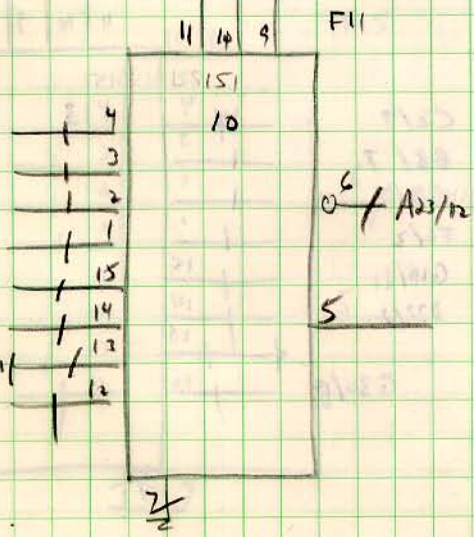
- CS/14
- ~~BS/14~~
- AS/10
- F3/15
- H11/15
- D29/15
- D28/15
- G19/8



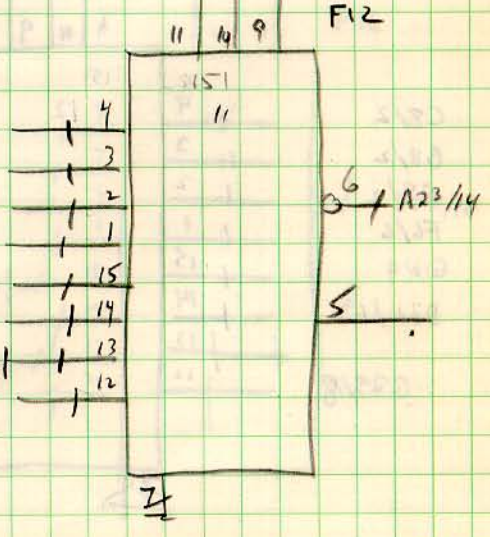
- CS/15
- BS/15
- AS/15
- F3/11
- G11/15
- D29/11
- D28/11
- G29/8



- C7/18
- B7/18
- A7/14
- F5/15
- C9/14
- D31/15
- G27/8

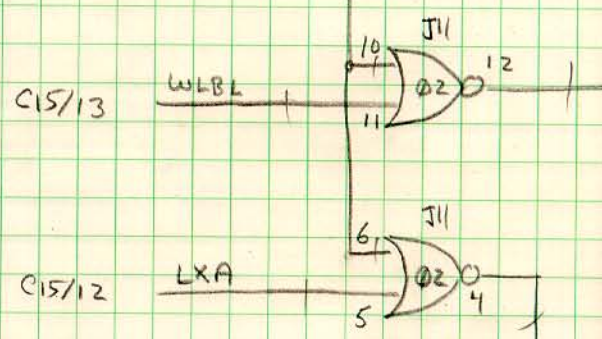
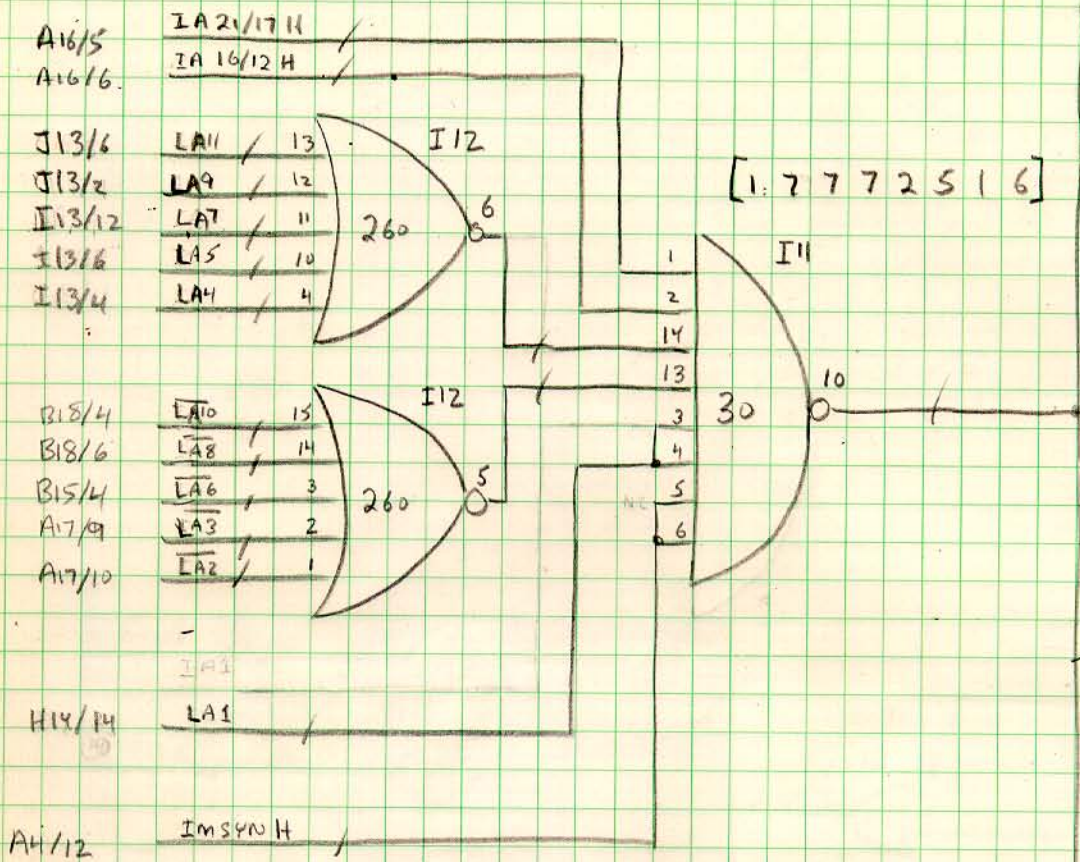


- C7/15
- B7/15
- A7/15
- F5/11
- G9/1
- D31/11
- G28/8



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APD

MMGT SR3

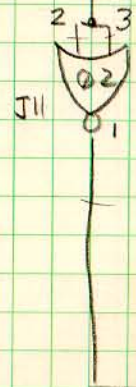


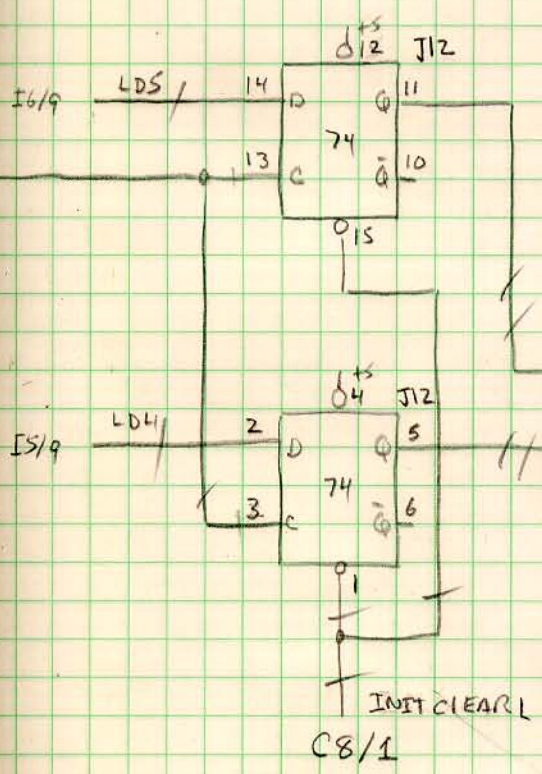
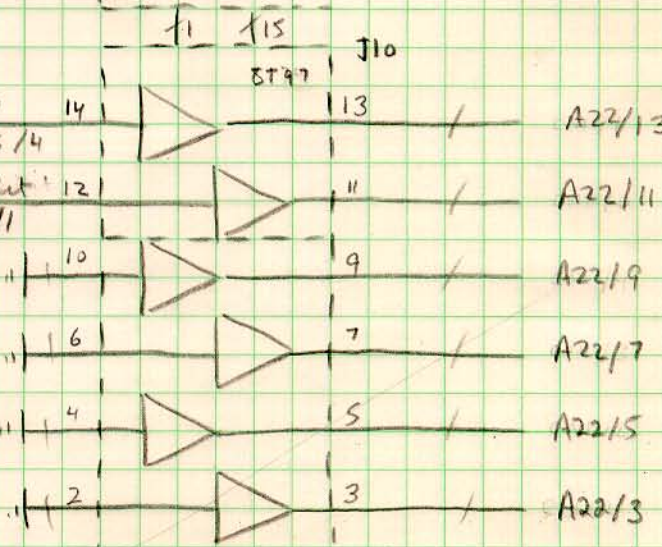
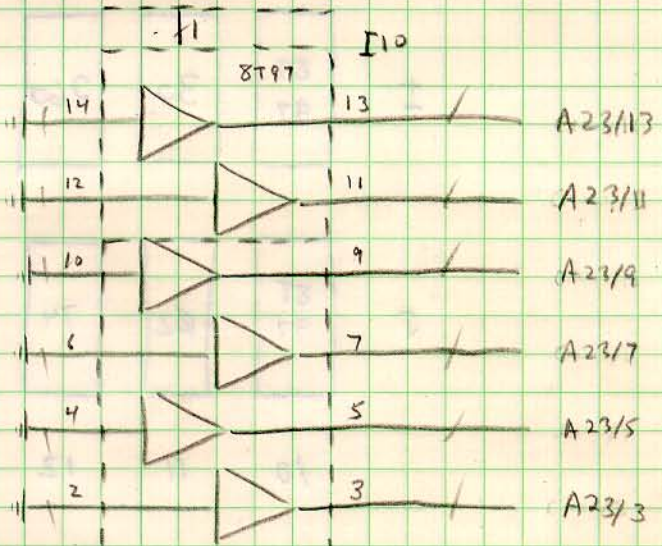
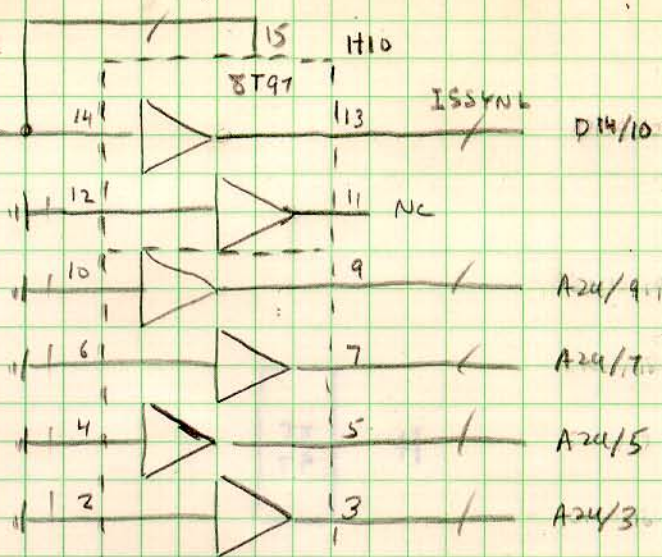
MM SR3

1 7 7 7 2 5 1 6

Enable MAP

13/02 BIT





11

87
97

I

87	30	260
97		

J

87	02	74
97		

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11

12