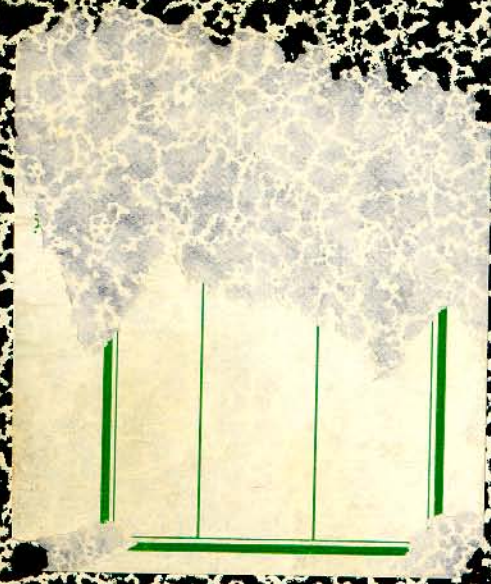

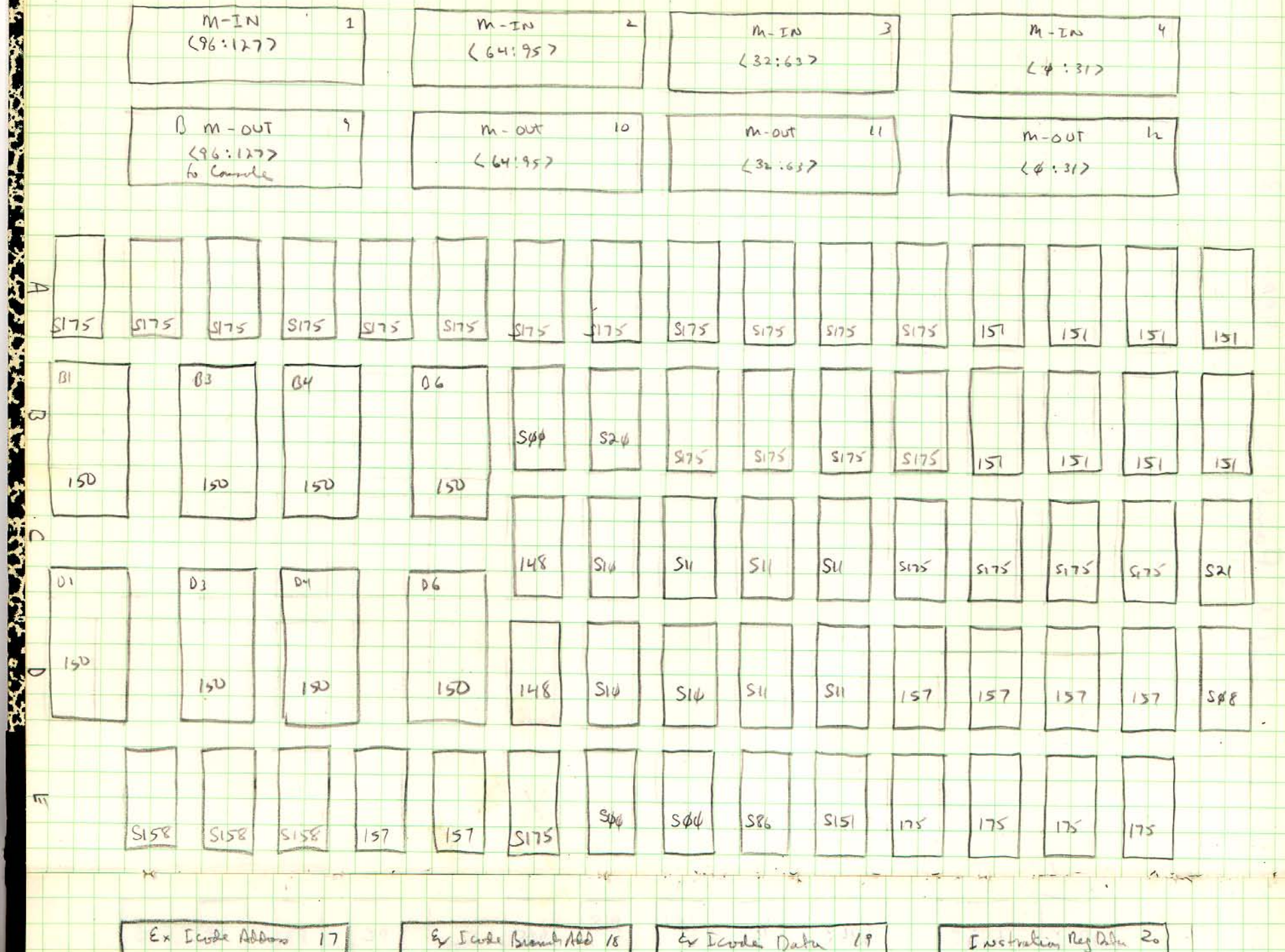
M-IN 1
<96:127>
M-IN 2
<64:95>
M-IN 3
<32:63>
M-IN 4
<0:31>
B M-OUT 9
<96:127>
to Console
M-OUT 10
<64:95>
M-OUT 11
<32:63>
M-OUT 12
<0:31>
A
B
C
D
E
S175
157
151
B1
B3
B4
D6
150
S00
S20
148
S10
S11
S21
D1
D3
D4
D6
S08
S158
S86
S151
175
Ex Icode Address 17
Ex Icode Branch Add 18
Ex Icode Data 19
Instruction Reg Data 20
to CPU

Ex Icode Address 17

Ex Icode Branch Add 18

Ex Icode Data 19

Instruction Reg Data 20 to CPU 1

Switch Data 25 from Console

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
F	S64	S74	X	X	157	S37	S74	365	LS253	LS253	Switches	Switch Data 25 from Console				123
G	S∅∅	×	×	×	Res	Res	LS 32	365	S257	S257	Switches	Res	S258	S258	S258	RES
H	Res	4∅∅1	Trans	Res	74	74	∅4	1∅	123	Res	367	367	367	367	367	367
I	Res	4∅∅2	11	8838	74	74	∅8	S37	74	74	74	74	74	74	74	74
J	LS175	LS175	LS175	LS175	SW	SW	S257	S257	S257	S257	LS∅2	4116R-002 470 Ω	LS∅∅	LS30	LS70	4116R-002 470 Ω
K	0 S201	1 S201	2 S201	3 S201	4 S201	5 S201	6 S201	7 S201	8 S201	9 S201	10 S201	11 S201	12 S201	13 S201	14 S201	15 S201

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ARB

MCODE/ICODE ADD 5
to Console
+ E0 - E7

M & I Address 6
OUT

Buffered Address 7
OUT

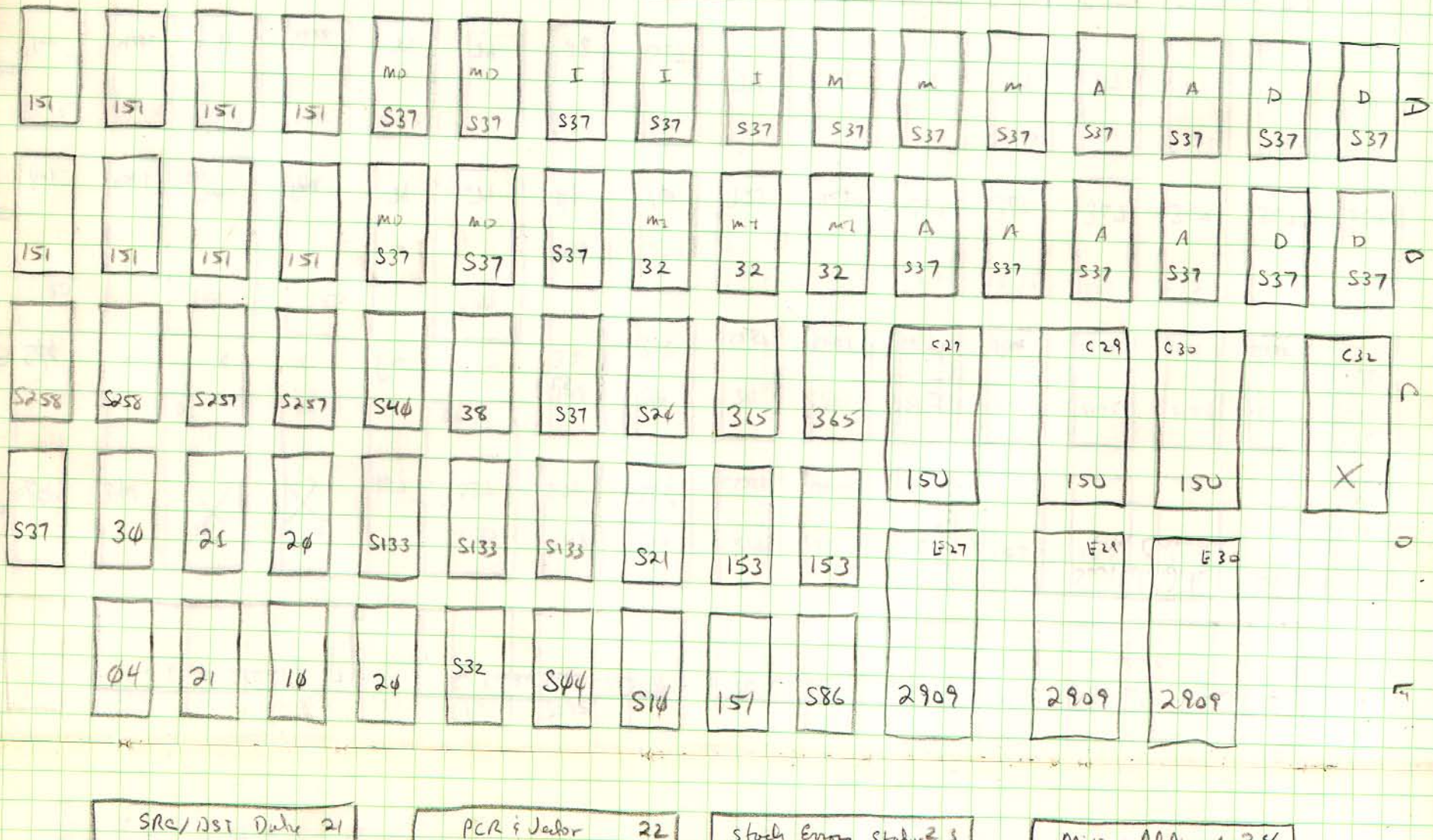
Buffered Int Data 8
- OUT

Buffer Mcode 13
<64:95>
to Console

M & I Data 14
out

Internal Address 15
IN

Internal Data 16
IN

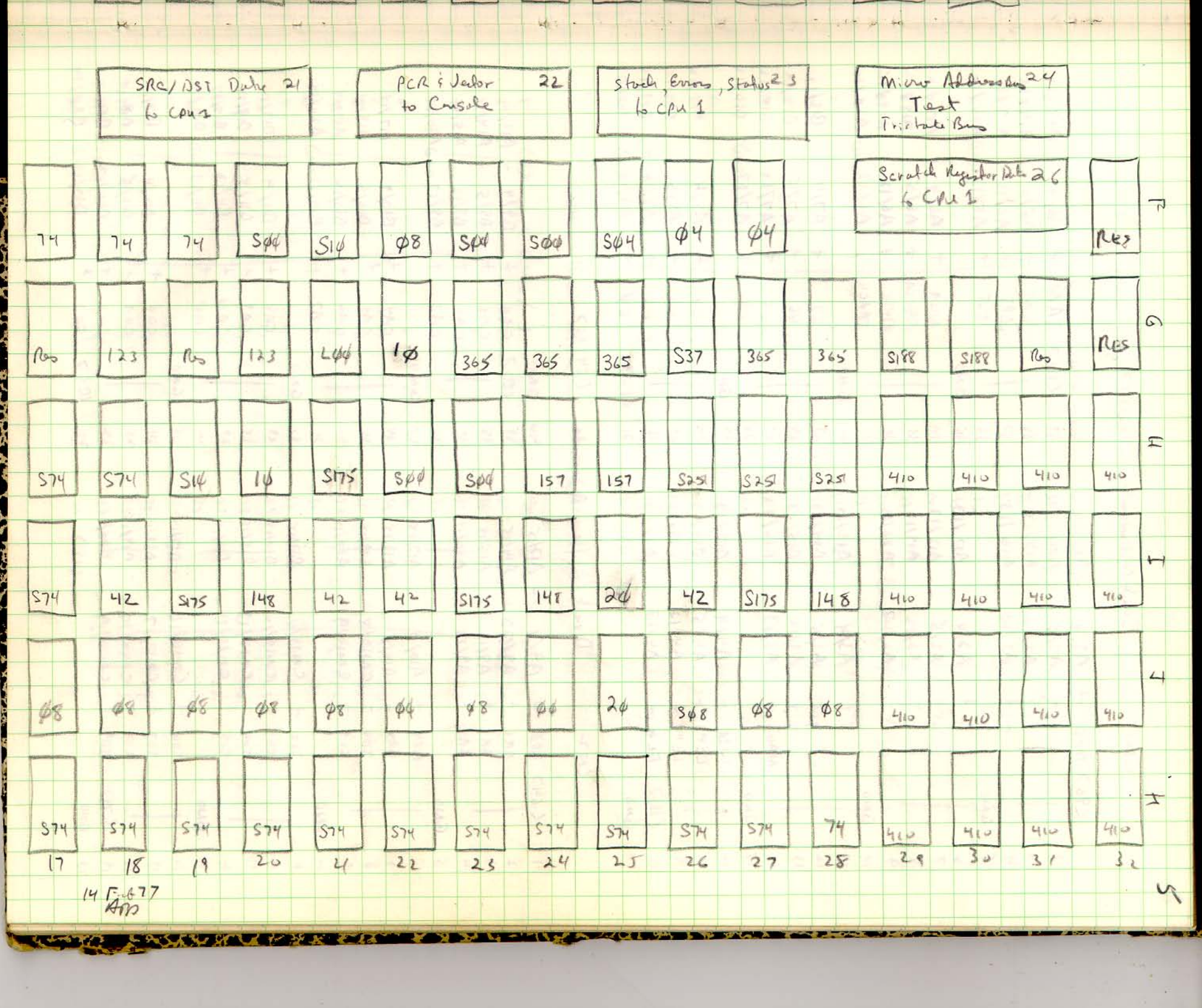


SRC/DST Data 21
to CPU I

PCR & Vector 22
to Console

Stack, Errors, Status 23
to CPU I

Micro Address 24


SRC/DST Data 21
to CPU 1
PCR & Vector 22
to Console
Stack, Errors, Status 23
to CPU 1
Micro Address Bus 24
Test
Tri-state Bus
Scratch Register Data 26
to CPU 1
74 74 74 SØØ SIØ ØØ8 SØØ SØØ SØ4 Ø4 Ø4 RES
Ø00 123 Ø00 123 LØØ 1Ø 365 365 365 S37 365 365 S188 S188 Ø00 RES
S74 S74 SIØ 1Ø S175 SØØ SØØ 157 157 S251 S251 S251 410 410 410 410
S74 42 S175 148 42 42 S175 148 2Ø 42 S175 148 410 410 410 410
ØØ8 ØØ8 ØØ8 ØØ8 ØØ8 ØØ4 ØØ8 ØØ4 2Ø S008 ØØ8 ØØ8 410 410 410 410
S74 S74 S74 S74 S74 S74 S74 S74 S74 S74 S74 74 410 410 410 410
17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
14 F-677
AMD

CN1 Direct Microcode <96:127>

1	<96>	MA0	+	A1/4	- A13/13	40	GND				
2			-	A1/5	A14/13	39	<112>	TRAP	+	A5/4	- A13/12
3			+	A1/12	A15/13	38		LINT	+	A5/5	A14/12
4			+	A1/13	A16/13	37		BPT	+	A5/12	A15/12
5	GND					36		IOT	+	A5/13	A16/12
6			+	A2/4	A17/13	35	GND				
7			+	A2/5	A18/13	34		NOA	+	A6/4	A17/12
8			-	A2/12	A19/13	33		SPECIAL	+	A6/5	A18/12
9			-	A2/13	A20/13	32		BPTE	+	A6/12	A19/12
10	GND					31		TRACE	+	A6/13	A20/12
11			+	A3/4	B13/13	30	GND				
12			+	A3/5	B14/13	29		E7	+	A7/4	B13/12
13			+	A3/12	B15/13	28		E6	+	A7/5	B14/12
14		MA11	+	A3/13	B16/13	27		E5	+	A7/12	B15/12
15	GND					26		E4	+	A7/13	B16/12
16		WIR	+	A4/4	B17/13	25	GND				
17		LCM2	+	A4/5	B18/13	24		E3	+	A8/4	B17/12
18		LCM1	+	A4/12	B19/13	23		E2	+	A8/5	B18/12
19	<111>	FLH	+	A4/13	B20/13	22		E1	+	A8/12	B19/12
20	GND					21	<127>	E0	+	A8/13	B20/12

CN2 Direct Buffered Microcode <64:95>

1	<64>	BR0	+	A9/4	- A13/15	40	GND				
2		BR1	+	A9/5	A14/15	39	<80>	CA0	+	B9/4	- A13/14
3		BR2	+	A9/12	A15/15	38		CA1	+	B9/5	A14/14
4		BR3	+	A9/13	A16/15	37		CA2	+	B9/12	A15/14
5	GND					36		CA3	+	B9/13	A16/14
6		BR4	+	A10/4	A17/15	35	GND				
7		BR5	+	A10/5	A18/15	34		CA4	+	B10/4	A17/14
8		IO0	+	CN10/8	A19/15	33		CA5	+	B10/5	A18/14
9		IO1	+	CN10/9	A20/15	32		CA6	+	B10/12	A19/14
10	GND					31		CA7	+	B10/13	A20/14
11		IO2	+	CN10/4	B13/15	30	GND				
12		IO3	+	CN10/12	B14/15	29		CA8	+	B11/4	B13/14
13		IO4	+	CN10/13	B15/15	28		CA9	+	B11/5	B14/14
14		IO5	+	CN10/14	B16/15	27		CA10	+	B11/12	B15/14
15	GND					26		CA11	+	B11/13	B16/14
16		IO6	+	CN10/16	B17/15	25	GND				
17		IO7	+	CN10/17	B18/15	24		CO0	+	B12/4	B17/14
18		IO8	+	CN10/18	B19/15	23		CO1	+	B12/5	B18/14
19	<79>	IO9	+	CN10/19	B20/15	22		CO2	+	B12/12	B19/14
20	GND					21	<95>	CO3	+	B12/13	B20/14

CN3 Direct Microcode ⟨32:63⟩

1	⟨32⟩	+	CN11 / 1	-	40	GND			
2		+	2		39	⟨48⟩	+	CN11 / 39	-
3		+	3		38		+		38
4		+	4		37		+		37
5	GND				36		+		36
6		+	6		35	GND			
7		+	7		34		+		34
8		+	8		33		+		33
9		+	9		32	CB	-	+	A19/1
10	GND				31		+	CN11 /	31
11		+	11		30	GND			
12		+	12		29		+		29
13		+	13		28		+		28
14		+	14		27		+		27
15	GND				26		+		26
16		+	16		25	GND			
17		+	17		24		+		24
18		+	18		23		+		23
19	⟨47⟩	+	19		22		+	✓	22
20	GND				21	⟨63⟩	+		21

CN4 Direct Microcode ⟨0:31⟩

1	⟨0⟩	+	CN12 / 1		40	GND			
2		+	2		39	⟨16⟩	+	CN12 / 39	
3		+	3		38		+		38
4		+	4		37		+		37
5	GND				36		+		36
6		+	6		35	GND			
7		+	7		34		+		34
8		+	8		33		+		33
9		+	9		32		+		32
10	GND				31		+		31
11		+	11		30	GND			
12		+	12		29		+		29
13		+	13		28		+		28
14		+	14		27		+		27
15	GND				26		+		26
16		+	16		25	GND			
17		+	17		24		+		24
18			18		23		+		23
19	⟨15⟩		19		22		+		22
20	GND				21	⟨31⟩	+		21

CN5 MCode / ICode Addresses to Console

1	$\overline{IA\phi}$	+	CN6/39	−			
2		+	38	−			
3		+	37	−			
4		+	36	−			
5	GND						
6		+	34	−			
7		+	33	−			
8		+	32	−			
9		+	31	−			
10	GND						
11		+	29	−			
12		+	28	−			
13		+	27	−			
14	$\overline{IA11}$	+	26	−			
15	GND						
16	ETL	+	I21/1				
17	EGL	+	I21/2				
18	ESL	+	I21/3				
19	EYL	+	I21/4				
20	GND						
40	GND						
39	$\overline{MA\phi}$	+	CN6/1	−			
38		+	2	−			
37		+	3	−			
36		+	4	−			
35	GND						
34		+	6	−			
33		+	7	−			
32		+	8	−			
31		+	9	−			
30	GND						
29		+	11	−			
28		+	12	−			
27		+	13	−			
26	$\overline{MA11}$	+	14	−			
25	GND						
24	EBL	+	I21/5				
23	EZL	+	I21/6				
22	EIL	+	I21/7				
21	EØL	+	I21/9				

CN6 $\overline{M}$ & I Addresses (out)

1	$\overline{MA\phi}$	+	CN5/39	+	A26/3	40	GND					
2		+	38	+	A26/6	39	$\overline{IA\phi}$	+	CN5/1	+	A23/3
3		+	37	+	A26/10	38		+	2	+	A23/6
4		+	36	+	A26/13	37		+	3	+	A23/10
5	GND					36		+	4	+	A23/B
6		+	34	+	A27/3	35	GND				
7		+	33	+	A27/6	34		+	6	+	A24/3
8		+	32	+	A27/10	33		+	7	+	A24/6
9		+	31	+	A27/13	32		+	8	+	A24/10
10	GND					31		+	9	+	A24/13
11		+	29	+	A28/3	30	GND				
12		+	28	+	A28/6	29		+	11	+	A25/3
13		+	27	+	A28/10	28		+	12	+	A25/6
14	$\overline{MA11}$	+	26	+	A28/13	27		+	13	+	A25/10
15	GND					26	$\overline{IA11}$	+	14	+	A25/13
16	MCLOCH	+	C23/3			25	GND				
17						24	ICLOCH	+	C23/10		
18	$\overline{MDone}$	+	G1/15			23					
19	MDSL	−				22	IDone	+	F7/13		
20	GND					21	IDSL	−			

CN7 Buffered Internal Address (OUT)

1	$\overline{IA0}$	+	A29/3
2		+	A29/6
3		+	A29/10
4		+	A29/13
5	GND		
6		+	A30/3
7		+	A30/6
8		+	A30/10
9		+	A30/13
10	GND		
11		+	A29/3
12		+	B29/6
13		+	B29/10
14		+	B29/13
15	GND		
16		+	B30/3
17		+	B30/6
18		+	B30/10
19	$\overline{IA15}$	+	B30/13
20	GND		

40	GND		
39	$\overline{IA16}$	+	B27/3
38		+	B27/6
37		+	B27/10
36		+	B27/13
35	GND		
34	1	+	B28/3
33	$\overline{IA21}$	+	B28/6
32	$\overline{IC0D}$	+	B28/10
31	$\overline{IC1D}$	+	B28/13
30	GND		
29	IXMSYNL	+	CN15/29
28			CN15/28
27	ISSYNL	+	CN15/27
26	UBSYNL	+	CN15/26
25	GND		
24	IMSYNL	+	CN15/24
23			CN15/23
22			CN15/22
21	INITCLEAR H	+	CN15/21

CN8 Buffered Internal Data (out)

1	DI0	+	CN16/1	−	C17/4
2		+	CN16/2	−	C17/7
3		+	CN16/3	+	C17/9
4		+	CN16/4	+	C17/12
5	GND				
6		+	CN16/6	+	C18/4
7		+	CN16/7	+	C18/7
8		+	CN16/8	+	C18/9
9		+	CN16/9	+	C18/12
10	GND				
11		+	CN16/11	+	C19/4
12		+	CN16/12	+	C19/7
13		+	CN16/13	+	C19/9
14		+	CN16/14	+	C19/12
15	GND				
16		+	CN16/16	+	C20/4
17		+	CN16/17	+	C20/7
18		+	CN16/18	+	C20/9
19	DI15	+	CN16/19	+	C20/12
20	GND				

40	GND		
39	$\overline{DO0}$	+	A31/3
38		+	A31/6
37		+	A31/10
36		+	A31/13
35	GND		
34		+	A32/3
33		+	A32/6
32		+	A32/10
31		+	A32/13
30	GND		
29		+	B31/3
28		+	B31/6
27		+	B31/10
26		+	B31/13
25	GND		
24		+	B32/3
23		+	B32/6
22		+	B32/10
21	$\overline{DO15}$	+	B32/13

CN9 Buffered Microcode to Console

1	<96>	B-MAØ	+	A1/3
2			+	A1/6
3			+	A1/11
4			+	A1/14
5	GND			
6			+	A2/3
7			+	A2/6
8			+	A2/11
9			+	A2/14
10	GND			
11			+	A3/3
12			+	A3/6
13			+	A3/11
14		B-MA11	+	A3/14
15	GND			
16		B-WIR	+	A4/3
17		B-LC#2	+	A4/6
18		B-LC#1	+	A4/11
19	<117>	B-FLK	+	A4/14
20	GND			

40	GND			
39	<112>	B-TRAP	+	A5/3
38		B-EMI	+	A5/6
37		B-NAT	+	A5/11
36		B-IOT	+	A5/14
35	GND			
34		B-NDA	+	A6/3
33		B-SPECIAL	+	A6/6
32		B-BYTE	+	A6/11
31		B-TRACE	+	A6/14
30	GND			
29		B-E7	+	A7/3
28		B-E6	+	A7/6
27		B-E5	+	A7/11
26		B-E4	+	A7/14
25	GND			
24		B-E3	+	A8/3
23		B-E2	+	A8/6
22		B-E1	+	A8/11
21	<127>	B-E0	+	A8/14

CN10 Buffered Microcode to CPU #1

1	<64>	B-BRØ	+	A9/2		
2		B-BR1	+	A9/7		
3		B-BR2	+	A9/10		
4		B-BR3	+	A9/15		
5	GND					
6		B-BR4	+	A10/2		
7		B-BR5	+	A10/7		
8	<78>	IOØ	+	CN2/8	-	A10/12
9		IO1	+	CN2/9	-	A10/13
10	GND					
11		IO2	+	CN2/11	-	A11/4
12		IO3	+	CN2/12	-	A11/5
13		IO4	+	CN2/13	-	A11/12
14		IO5	+	CN2/14	-	A11/13
15	GND					
16		IO6	+	CN2/16	-	A12/4
17		IO7	+	CN2/17	-	A12/5
18		IO8	+	CN2/18	-	A12/12
19	<79>	IO9	+	CN2/19	-	A12/13
20	GND					

40	GND					
39	<80>	B-CAØ	+	B9/2		
38		B-CA1	+	B9/7		
37		B-CA2	+	B9/10		
36		B-CA3	+	B9/15		
35	GND					
34		B-CA4	+	B10/2		
33		B-CA5	+	B10/7		
32		B-CA6	+	B10/10		
31		B-CA7	+	B10/15		
30	GND					
29		B-CA8	+	B11/2		
28		B-CA9	+	B11/7		
27		B-CA10	+	B11/10		
26		B-CA11	+	B11/15		
25	GND					
24		B-COØ	+	B12/2	-	C27/15
23		B-CO1	+	B12/7	-	C27/14
22		B-CO2	+	B12/10	-	C27/13
21	<95>	B-CO3	+	B12/15	-	C27/11

CN11 — Direct Microcode ⟨32:63⟩

1	⟨32⟩	*	CN3/1	⊥	A13/2	40	GND				
2		+	2	+	A14/2	39	⟨48⟩	+	CN3/39	⊥	A13/1
3		+	3	+	A15/2	38		+	38	⊥	A14/1
4		+	4	+	A16/2	37		+	37	+	A15/1
5	GND					36		+	36	⊥	A16/1
6		+	6	+	A17/2	35	GND				
7		+	7	+	A18/2	34		+	34	⊥	A17/1
8		+	8	+	A19/2	33		+	33	⊥	A18/1
9		+	9	⊥	A20/2	32	B-CS	+	#21/11		
10	GND					31		⊥	31	⊥	A20/1
11		+	11	+	B13/2	30	GND				
12		+	12	+	B14/2	29		+	29	⊥	B13/1
13		+	13	⊥	B15/2	28		+	28	⊥	B14/1
14		+	14	⊥	B16/2	27		+	27	⊥	B15/1
15	GND					26		+	26	⊥	B16/1
16		+	16	+	B17/2	25	GND				
17		+	17	⊥	B18/2	24		+	24	⊥	B17/1
18		+	18	⊥	B19/2	23		+	23	⊥	B18/1
19	⟨47⟩	+	19	⊥	B20/2	22		+	22	⊥	B19/1
20	GND					21	⟨63⟩	+	21	⊥	B20/1

CN12 — Direct Microcode ⟨0:31⟩

1	⟨07⟩	+	CN4/1	⊥	A13/4	40	GND				
2		+	2	+	A14/4	39	⟨16⟩	-	CN4/39	+	A13/3
3		+	3	+	A15/4	38		+	38	⊥	A14/3
4		+	4	+	A16/4	37		+	37	⊥	A15/3
5	GND					36		+	36	⊥	A16/3
6		+	6	⊥	A17/4	35	GND				
7		+	7	+	A18/4	34		+	34	⊥	A17/3
8		+	8	+	A19/4	33		+	33	+	A18/3
9		+	9	+	A20/4	32		+	32	+	A19/3
10	GND					31		+	31	+	A20/3
11		+	11	+	B13/4	30	GND				
12		+	12	+	B14/4	29		+	29	+	B13/3
13		+	13	+	B15/4	28		+	28	+	B14/3
14		+	14	+	B16/4	27		+	27	+	B15/3
15	GND					26		+	26	+	B16/3
16		+	16	+	B17/4	25	GND				
17		+	17	+	B18/4	24		+	24	⊥	B17/3
18		+	18	+	B19/4	23		+	23	⊥	B18/3
19	⟨15⟩	+	19	+	B20/4	22		+	22	⊥	B19/3
20	GND					21	⟨31⟩	+	21	⊥	B20/3

CN13 Buffered Microcode to Console

1	<64>	B-BR0	+	A9/3
2		B-BR1	+	A9/6
3		B-BR2	+	A9/11
4		B-BR3	+	A9/14
5	GND			
6		B-BR4	+	A10/3
7		B-BR5	+	A10/6
8		B-IO0	+	A10/11
9		B-IO1	+	A10/14
10	GND			
11		B-IO2	+	A11/3
12		B-IO3	+	A11/6
13		B-IO4	+	A11/11
14		B-IO5	+	A11/14
15	GND			
16		B-IO6	+	A12/3
17		B-IO7	+	A12/6
18		B-IO8	+	A12/11
19	<79>	B-IO9	+	A12/14
20	GND			

40	GND			
39	<80>	B-CA0	+	B9/3
38		B-CA1	+	B9/6
37		B-CA2	+	B9/11
36		B-CA3	+	B9/14
35	GND			
34		B-CA4	+	B10/3
33		B-CA5	+	B10/6
32		B-CA6	+	B10/11
31		B-CA7	+	B10/14
30	GND			
29		B-CA8	+	B11/3
28		B-CA9	+	B11/6
27		B-CA10	+	B11/11
26		B-CA11	+	B11/14
25	GND			
24		B-CO0	+	B12/3
23		B-CO1	+	B12/6
22		B-CO2	+	B12/11
21	<95>	B-CO3	+	B12/14

CN14

1	DA0	+		A21/3
2		+		A21/6
3		+		A21/10
4		+		A21/13
5	GND			
6		+		A22/3
7		+		A22/6
8		+		A22/10
9		+		A22/13
10	GND			
11		+		B21/3
12		+		B21/6
13		+		B21/10
14		+		B21/13
15	GND			
16		+		B22/3
17		+		B22/6
18		+		B22/10
19	DA15	+		B22/13
20	GND			

40	GND			
39	WLB[L]	+		B23/15
38		-		
37		-		
36	WHB[L]	+		C23/15
35	GND			
34	WA0	+		B23/3
33	WA1	+		B23/6
32	WA2	+		B23/11
31		-		
30	GND			
29	XA CLOCK	+		C23/6
28		-		
27		-		
26	XA DONE	+		G1/12
25	GND			
24		-		
23		-		
22		-		
21		-		

CN15 INTERNAL Address Bus (IN)

1	IAØ	+	A29/1
2	|	+	A29/4
3	|	+	A29/12
4	|	+	A29/15
5	GND		
6	|	+	A30/1
7	|	+	A30/4
8	|	+	A30/12
9	|	+	A30/15
10	GND		
11	|	+	B29/1
12	|	+	B29/4
13	|	+	B29/12
14	|	+	B29/15
15	GND		
16	|	+	B30/1
17	|	+	B30/4
18	|	+	B30/12
19	IA15	+	B30/15
20	GND		

40	GND		
39	IA16	+	B27/1
38	|	+	B27/4
37	|	+	B27/12
36	|	+	B27/15
35	GND		
34	|	+	B28/1
33	IA21	+	B28/4
32	ICØD	+	B28/12
31	IC1D	+	B28/15
30	GND		
29	IXMSYNL	+	CN7/29 + E10/4
28		+	CN7/28
27	ISSYNL	+	CN7/27 + C22/3
26	UBSYNL	+	CN7/26 + C22/6
25	GND		
24	IMSYNL	+	CN7/24 + E10/1
23		+	CN7/23
22		+	CN7/22
21	INIT CLEAR [H]	+	CN7/21

CN16 Internal Data (IN)

1	DIØ	+	CN8/1
2	|	+	CN8/2
3	|	+	3
4	|	+	4
5	GND		
6	|	+	6
7	|	+	7
8	|	+	8
9	|	+	9
10	GND		
11	|	+	11
12	|	+	12
13	|	+	13
14	|	+	14
15	GND		
16	|	+	16
17	|	+	17
18	|	+	18
19	DI15	+	19
20	GND		

40	GND		
39	DOØ	+	A31/1
38	|	+	A31/4
37	|	+	A31/12
36	|	+	A31/15
35	GND		
34	|	+	A32/1
33	|	+	A32/4
32	|	+	A32/12
31	|	+	A32/15
30	GND		
29	|	+	B31/1
28	|	+	B31/4
27	|	+	B31/12
26	|	+	B31/15
25	GND		
24	|	+	B32/1
23	|	+	B32/4
22	|	+	B32/12
21	DO15	+	B32/15

CN17 External I Code Address generation

1	$\overline{XICA0}$	+	E2/3
2	$\overline{XICA1}$	+	E2/6
3	$\overline{XICA2}$	+	E2/10
4		+	E2/13
5	GND		
6		+	E3/3
7		+	E3/6
8		+	E3/10
9		+	E3/13
10	GND		
11		+	E4/3
12		+	E4/6
13		+	E4/10
14	$\overline{XICA11}$	+	E4/13
15	GND		
16	$\overline{IAR0}$	+	I11/6 + E4/2
17	$\overline{IAR1}$	+	I11/10 + E4/5
18	$\overline{IAR2}$	+	I12/6 + E4/11
19	$\overline{IAR3}$	+	I12/10 + E4/14
20	GND		

40	GND		
39	$\overline{I0}$	+	C12/3
38	$\overline{I1}$	+	G12/6
37		+	C12/11
36		+	C12/14
35	GND		
34		+	C13/3
33		+	C13/6
32		+	C13/11
31		+	C13/14
30	GND		
29		+	C14/3
28		+	C14/6
27		+	C14/11
26		+	C14/14
25	GND		
24		+	C15/3
23		+	C15/6
22		+	C15/11
21	$\overline{I15}$	+	C15/14

CN18 External Icode Branch Address

1	XIBA0	+	F8/2
2		+	F8/4
3		+	F8/6
4		+	F8/10
5	GND		
6		+	F8/12
7		+	F8/14
8		+	G8/2
9		+	G8/4
10	GND		
11		+	G8/6
12		+	G8/10
13		+	G8/12
14	XBA11	+	G8/14
15	GND		
16	XA0	-	F5/2
17	XA1	-	F05/4 - F9/14
18	XA2	-	F05/6 F9/2
19	XCOND	-	F5/6
20	GND		

40	GND		
39	B-MA0	+	A1/2 - F9/3
38	B-MA1	+	A1/7 - F9/13
37		+	A1/10 - F10/3
36		+	A1/15 - F10/13
35	GND		
34		+	A2/2 - G9/3
33		+	A2/7 - G9/6
32		+	A2/10 - G9/10
31		+	A2/15 - G9/13
30	GND		
29		+	A3/2 - G10/3
28		+	A3/7 - G10/6
27		+	A3/10 - G10/10
26	B-MA11	+	A3/15 - G10/13
25	GND		
24	STXIRDCD	+	F7/14 - CN21/4
23	XBR	+	F5/13
22	XFIRDCD	+	F6/1
21	XIRDCD	+	F5/3

CN19 External Iconic Data

1	XSRC0	†	E5/3	40	GND		
2	XSRC1	†	E5/6	39	DIR0	†	E12/2
3	XSRC2	†	E5/10	38	|	†	E12/7
4	XSRC3	†	E5/13	37	|	†	E12/10
5	GND			36	|	†	E12/15 – F9/5
6	XDST0	†	E6/3	35	GND		
7	XDST1	†	E6/6	34	|	†	E13/2 – F9/11
8	XDST2	†	E6/10	33	|	†	E13/7 – F10/5
9	XDST3	†	E6/13	32	|	†	E13/10
10	GND			31	|	†	E13/15
11	C	†	E11/12 † CN23/39	30	GND		
12	V	†	E11/13 † CN23/38	29	|	†	E14/2
13	Z	†	E11/3 † CN23/37	28	|	†	E14/7 – F9/6
14	N	†	E11/15 † CN23/36	27	|	†	E14/10 – F9/10
15	GND			26	|	†	E14/15 – F10/6
16	CVZ	†	E11/14 † CN23/34	25	GND		
17	C⊕N	†	† CN23/33	24	|	†	E15/2
18	V⊕N	†	E11/2 † CN23/32	23	|	†	E15/7
19	(V⊕N)VZ	†	E11/1 † CN23/31	22	|	†	E15/10
20	GND			21	DIR1	†	E15/15

CN20 INSTRUCTION Register Data (pgs

1	IR0	†	D12/2	40	GND		
2	IR1	†	D12/5	39	$\overline{\text{DIR0}}$	†	E12/3
3	|	†	D12/11	38	|	†	E12/6
4	|	†	D12/14	37	|	†	E12/11
5	GND			36	|	†	E12/14
6	|	†	D13/2	35	GND		
7	|	†	D13/5	34	|	†	E13/3
8	|	†	D13/11	33	|	†	E13/6
9	|	†	D13/14	32	|	†	E13/11
10	GND			31	|	†	E13/14
11	|	†	D14/2	30	GND		
12	|	†	D14/5	29	|	†	E14/3
13	|	†	D14/11	28	|	†	E14/6
14	|	†	D14/14	27	|	†	E14/11
15	GND			26	|	†	E14/14
16	|	†	D15/2	25	GND		
17	|	†	D15/5	24	|	†	E15/3
18	|	†	D15/11	23	|	†	E15/6
19	IR15	†	D15/14	22	|	†	E15/11
20	GND			21	$\overline{\text{DIR15}}$	†	E15/14

CN21 SRC/DST/other

1	LD IR	-	D14/11
2	LB IR	-	D16/15
3	HB IR	-	D16/1
4	ST IR DCD	+	CN18/24
5	GND		
6	IR DCD	+	F7/10
7	PCRWLB	+	F26/1
8	PCRWHB	+	F26/15
9	PCR Read	+	H15/15
10	GND		
11	XL	+	E20/3
12	XH	+	E20/15
13	XA	+	D17/10
14	WAITH	+	A4/2
15	GND		
16	E0-E6[H]	+	G20/10
17	MSRC L	-	F22/6
18	IRBUSY L	+	D19/14
19	PSR4	+	H22/2 + E25/3
20	GND		

40	GND		
39	SRC0	+	E5/4 + E25/13
38	SRC1	+	E5/7
37	SRC2	+	E5/9
36	SRC3	+	E5/12
35	GND		
34	DST0	+	E6/4
33	DST1	+	E6/7
32	DST2	+	E6/9
31	DST3	+	E6/12
30	GND		
29	D-BYTE	+	A6/10
28	D-SPECIAL	+	A6/7
27	D-NDA	+	A6/2
26	LKAD	+	F1/10
25	GND		
24	I WLB	+	E20/6
23	I WHB	+	E20/14
22	I Read	+	E18/1
21			

CN22 PCR & Vector Data

1	PCR <0>	+	H11/12 + C21/11
2	|	+	H11/14 + E21/11
3	|	+	H12/12
4	|	+	H12/14 - E22/4
5	GND		
6	|	+	H12/2
7	|	+	H12/4
8	|	+	H12/6
9	|	+	H12/10
10	GND		
11	|	+	H24/11
12	|	+	H25/11
13	|	+	H25/14
14	|	+	H24/2
15	GND		
16	|	+	H15/2
17	|	+	H15/4
18	|	+	H15/6
19	PCR<15>	+	H15/10
20	GND		

40	GND		
39	VECTOR <0>	+	G23/3
38	|	+	G23/5
37	|	+	G23/7
36	|	+	G23/9
35	GND		
34	|	+	G24/4
33	|	+	G23/13
32	|	+	G24/3
31	VECTOR <7>	+	G24/5
30	GND		
29	VECTOR <8>	+	G24/7
28	|	+	G24/9
27	|	+	G24/11
26	|	+	G24/13
25	GND		
24	|	+	G25/3
23	|	+	G25/5
22	|	+	G25/7
21	Vector <15>	+	G25/9

CN23 STACH/ Errors / PSR STATUS

1	YS[H]	+	H28/2
2	CPUOIS	+	J19/14
3	CPUOΦ	+	J19/2
4	OASC	+	H19/3
5	GND		
6	CSOR	+	CN28/13
7	TMOT L	+	F24/4
8	ODD ADD L	+	K18/13
9	MMBTER L	+	F24/12
10	GND		
11	INIT CLR L	+	F18/1
12	EX	−	
13	SYSTEM INIT[L]	+	CN25/21 + D19/12 + G26/2
14	INIT TRIGGER[L]	+	I3/6
15	GND		
16	T DC LO	+	H45/5
17	R DC LO	+	H7/1
18	T AC LO	+	CN23/20 - GND
19	R AC LO	+	H6/13
20	GND		

40	GND		
39	C	+	CN19/11 + D25/5
38	V	+	CN19/12 + D25/4
37	Z	+	CN19/13 + D26/3
36	N	+	CN19/14 + D25/11
35	GND		
34	CVZ	+	CN19/16
33	C⊽N	+	CN19/17
32	N⊽V	+	CN19/18
31	ZV (V⊽N)	+	CN19/19
30	GND		
29	SPCL H	+	F21/14
28			
27			
26	$\overline{CPC}$	+	G26/1
25	GND		
24	$\overline{IA4}$	+	H28/4
23	IA3	+	H27/4
22	$\overline{IA2}$	+	H26/4
21	IED	+	H22/4

CN24 Microcontroller Output Address Bus + Tristate Control

1	Y0	−	E27/18 + F32/1
2	Y1	−	E27/19 + F32/2
3	Y2	−	E27/20 + F32/3
4	Y3	−	E27/21 + F32/4
5	GND		
6	Y4	−	E29/18 + F32/5
7	Y5	−	E29/19 + F32/6
8	Y6	−	E29/20 + F32/7
9	Y7	−	E29/21 + F38/9
10	GND		
11	Y8	−	E36/18 + F32/10
12	Y9	−	E36/19 + F32/11
13	Y10	−	E36/20 + F32/12
14	Y11	−	E36/21 + F32/13
15	GND		
16	OE	−	E23/5 + F32/14
17			
18			
19			
20	GND		

40	GND		
39	MDB0	+	E27/13
38	MDB1	+	E27/11
37	MDB2	+	E27/9
36	MDB3	+	E27/7
35	GND		
34	MDB4	+	E29/13
33	MDB5	+	E29/11
32	MDB6	+	E29/9
31	MDB7	+	E29/7
30	GND		
29	MDB8	+	E36/13
28	MDB9	+	E36/11
27	MDB10	+	E36/9
26	MDB11	+	E36/7
25	GND		
24	Hold clock Low [L]	+	F21/1
23			
22			
21			

CN25 Switch Data + Vector Addrs from Console

1	DSW0	+	G13/2
2		+	G13/5
3		+	G13/11
4		+	G13/14
5	GND		
6		+	G14/2
7		+	G14/5
8		+	G14/11
9		+	G14/14
10	GND		
11		+	G15/2
12		+	G15/5
13		+	G15/11
14		+	G15/14
15	GND		
16		-	H16/2
17		+	H16/4
18		+	H16/6
19	DSW15	+	H16/14
20	GND		

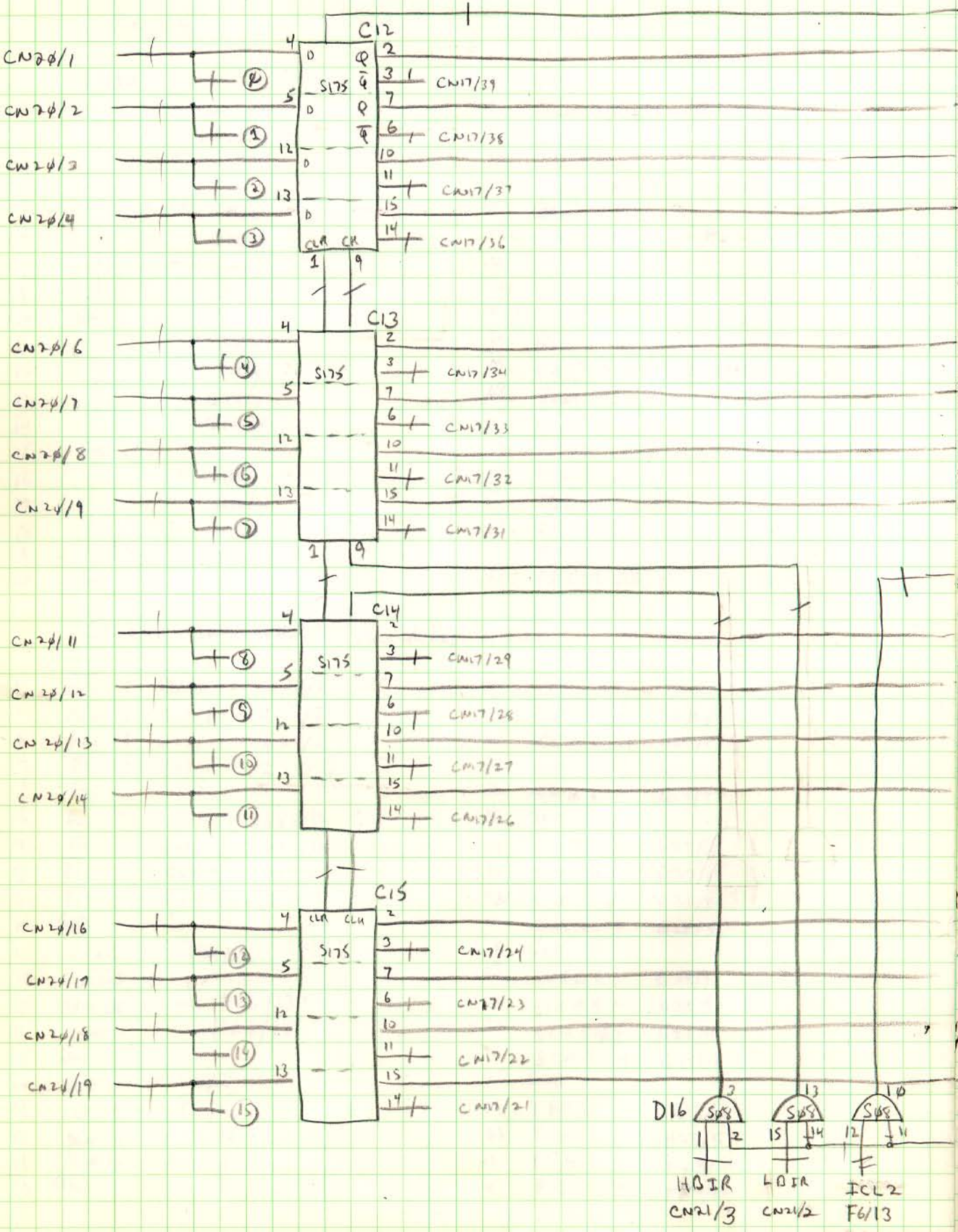
40	GND		
39	VCTA0	-	H28/6
38	VCTA1	-	H27/6
37	VCTA2	-	H26/6
36	VCTA3	-	H25/4
35	GND		
34	VCTA4	-	H25/7
33			
32			
31			
30	GND		
29	HALT [L]	+	I28/13
28	HALT [H]	-	
27			
26	LD PCR	+	H7/15
25	GND		
24	DIS [L]	+	H15/15
23	DIS [H]	-	
22	PFS [H]	+	H15/2
21	PANEL reset [L]	+	H3/4 + CN23/13

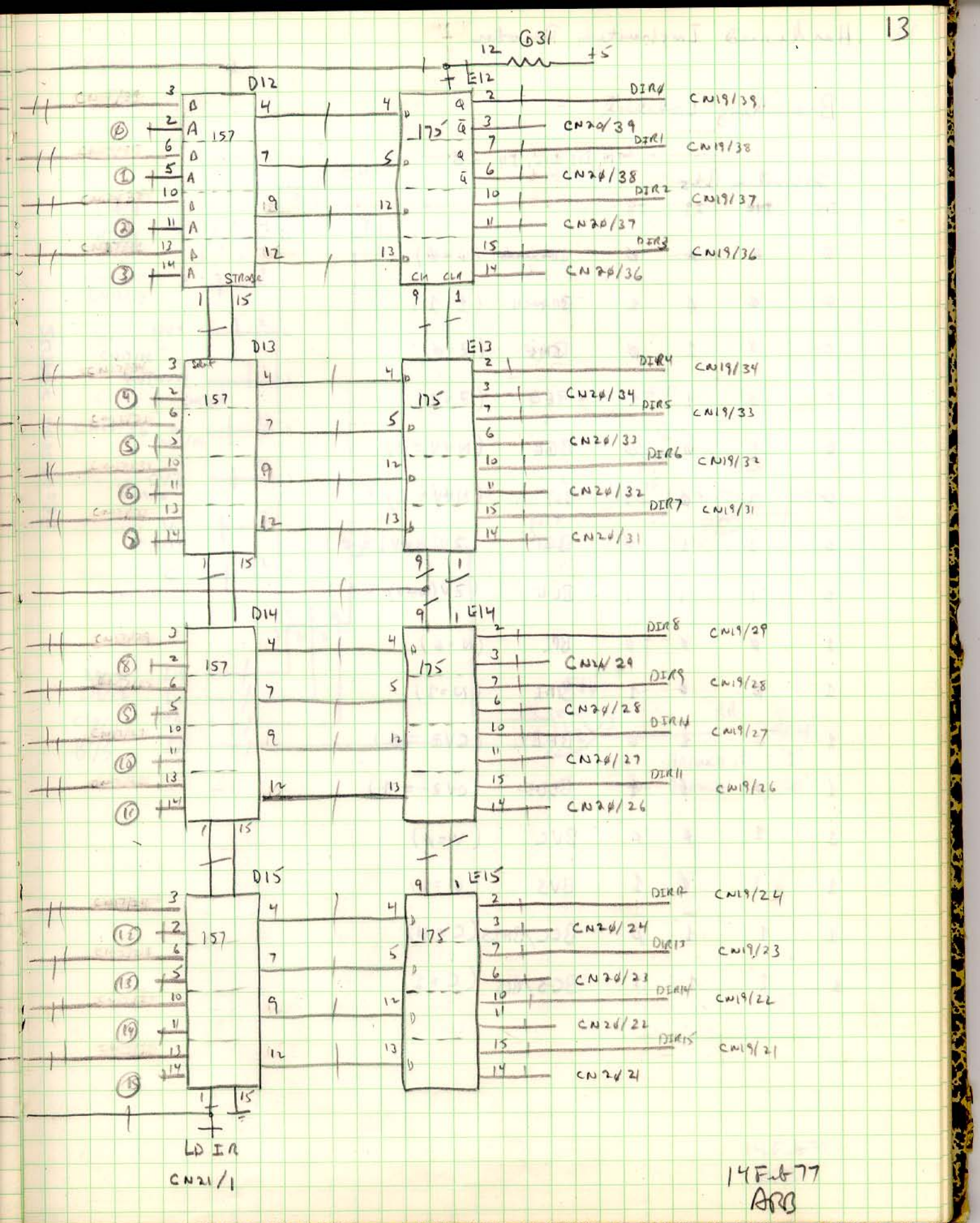
CN26 Interrupt Vector / Scratch Register Data

1	$\overline{PV0}$	+	G29/1	-	G23/2
2	$\overline{PV1}$	+	G29/2	-	G23/4
3	$\overline{PV2}$	+	G29/3	-	G23/6
4	$\overline{PV3}$	+	G29/4	-	G23/14
5	GND				
6	$\overline{PV4}$	+	G29/5	-	G23/12
7	$\overline{PV5}$	+	G29/6	-	G23/14
8	$\overline{PV6}$	+	G29/7	-	G24/2
9	$\overline{PV7}$	+	G29/9	-	G24/4
10	GND				
11	$\overline{BCN1}$	+	E24/13		
12	$\overline{BCN3}$	+	E24/11		
13	UMDF L	-	F23/13		
14	INHST L	+	F23/10		
15	GND				
16	SCRA0	+	F25/14		
17	SCRA1	+	F25/12		
18	SCRA2	+	F2/14		
19	SCR Read L	+	E24/6		
20	GND				

40	GND		
39	SCRB0	+	G27/3
38	SCRB1	+	G27/5
37	SCRB2	+	G27/7
36	SCRB3	+	G27/9
35	GND		
34	SCRB4	+	G27/11
33	SCRB5	+	G27/13
32	SCR 06	+	G28/3
31	SCR B7	+	G28/5
30	GND		
29	SCRB8	+	G28/7
28	SCRB9	+	G28/9
27	SCRB10	+	G28/11
26	SCRB11	+	G28/13
25	GND		
24	TBTH	+	H27/11
23	YSH	+	K28/5
22	PFH	+	H28/11
21	FBH	+	F24/13

INSTRUCTION Register RANKS 1 & 2 with Write Logic




G31
+5
D12
E12
157
175
STROBE
CLR
DIR0
DIR1
DIR2
DIR3
CN19/38
CN19/37
CN19/36
CN20/39
CN20/38
CN20/37
CN20/36
D13
E13
DIR4
DIR5
DIR6
DIR7
CN19/34
CN19/33
CN19/32
CN19/31
CN20/34
CN20/33
CN20/32
CN20/31
D14
E14
DIR8
DIR9
DIR10
DIR11
CN19/29
CN19/28
CN19/27
CN19/26
CN20/29
CN20/28
CN20/27
CN20/26
D15
E15
DIR12
DIR13
DIR14
DIR15
CN19/24
CN19/23
CN19/22
CN19/21
CN20/24
CN20/23
CN20/22
CN20/21
LD IR
CN21/1

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Hardwired Instruction Decoder

Branching Lookahead

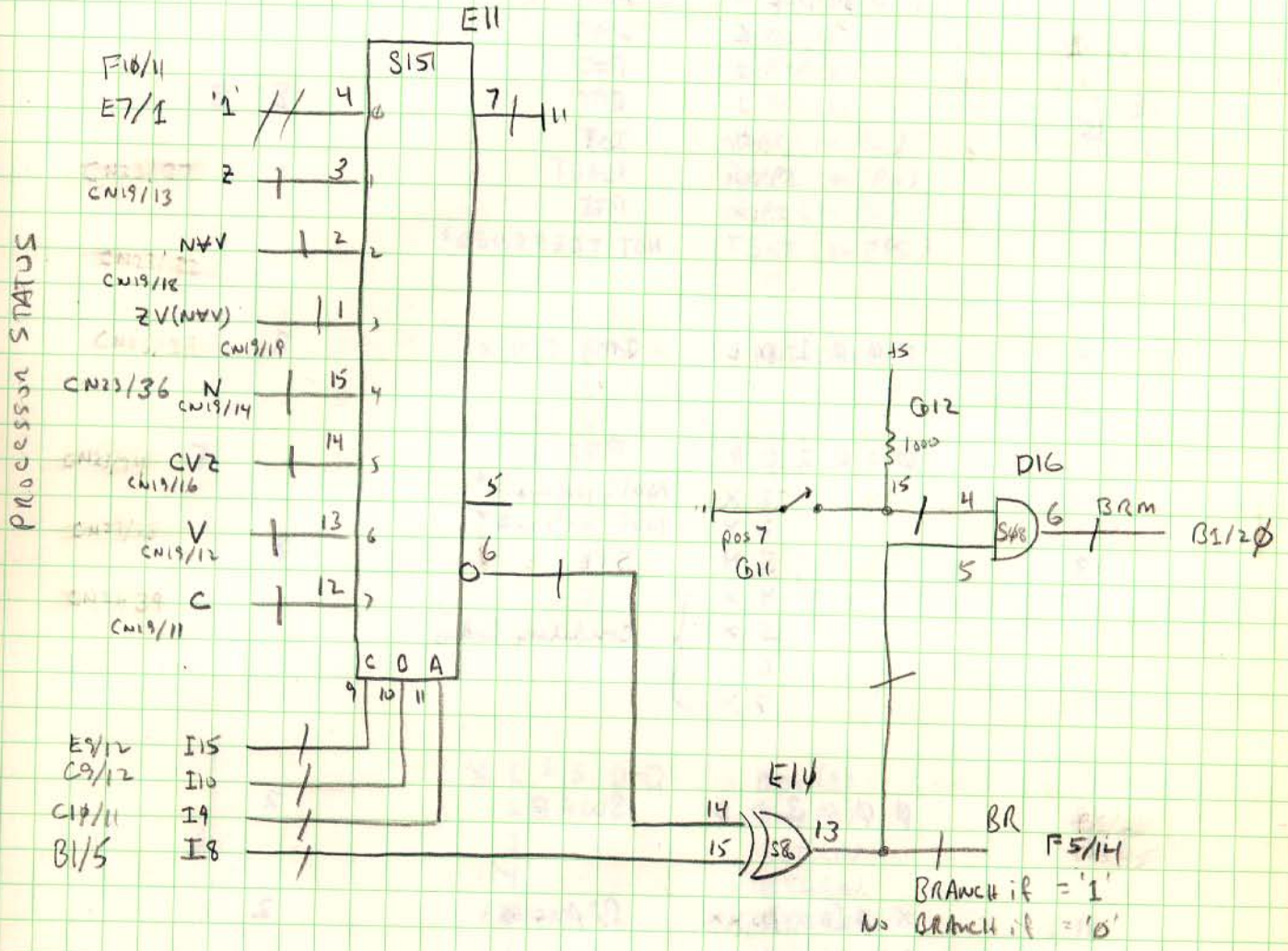
$I_{14}, I_{13}, I_{12}, I_{11} = \phi$

Instruction Bits

I15	I10	I9	I8		
ϕ	ϕ	ϕ	ϕ	Not used	$(\phi = \phi)$
ϕ	ϕ	ϕ	1	BRANCH	$(1 = 1)$
ϕ	ϕ	1	ϕ	BNE	$(Z = \phi)$
ϕ	ϕ	1	1	BEQ	$(Z = 1)$
ϕ	1	ϕ	ϕ	BGE	$(N \oplus V = \phi)$
ϕ	1	ϕ	1	BLT	$(N \oplus V = 1)$
ϕ	1	1	ϕ	BGT	$(Z \vee (N \oplus V) = \phi)$
ϕ	1	1	1	BLE	$(Z \vee (N \oplus V) = 1)$
1	ϕ	ϕ	ϕ	BPL	$(N = \phi)$
1	ϕ	ϕ	1	BMI	$(N = 1)$
1	ϕ	1	ϕ	BHI	$(C \vee Z = \phi)$
1	ϕ	1	1	BLOS	$(C \vee Z = 1)$
1	1	ϕ	ϕ	BVC	$(V = \phi)$
1	1	ϕ	1	BVS	$(V = 1)$
1	1	1	ϕ	BCC/BHIS	$(C = \phi)$
1	1	1	1	BCS/BLO	$(C = 1)$

PROCESSOR STATUS

Logic



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PDP-11 INSTRUCTION PRIORITY CHAIN (15 - 0)

Priority Group	Opcode	Mnemonic	# of States Encoded
	0 0 0 0 0 0	HALT	
	1	WAIT	
	2	RTI	
	3	BPT	
15	4	IOT	8
	5	RESET	
	6	RTT	
	7	NOT DEFINED*	
14	0 0 0 1 D D	JMP	2
	0 0 0 2 0 R	RTS	
	1 X	NOT Defined*	
	2 X	NOT Defined*	
13	3 N	SPL	8
	4 X		
	5 X	Condition Codes	
	6 X		
	7 X		
12	0 0 0 3 D D	SWAB	2
11	X 0 [0 xx] xxx	BRANCHS	2
10	0 0 4 R D D	JSR	2
	X 0 5 0 D D	CLR (B)	
	1	COM (B)	
	2	INC (B)	
9	3	DEC (B)	32
	4	NEG (B)	
	5	ADC (B)	
	6	SBC (B)	
	7	TST (B)	

* - May be encoded for additional instructions

Priority Group	OP Code	MNEMONIC	# of Shifts
	X Ø 6 0 D D	ROR (B)	
	1	ROL (B)	
8	2	ASR (B)	
	3	ASL (B)	32
	4	MARK (MTPS)	
	5	MFPI (MFPD)	
	6	MTPI (MTPD)	
	7	SXT (MFPS)	
	X Ø 7 Ø X X	NOT USED *	
	1		
	2		
7	3		16
	4		
	5		
	6		
	7		
	X 1 S S D D	MOV (B)	
	2	CMP (B)	
6	3	BIT (B)	48
	4	BIC (B)	
	5	BIS (B)	
	6	ADD (SUB)	

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Priority Group	Op Code	Mnemonic	# of States
5	075000 R	FADD	
	1	FSUB	
	2	FMUL	
	3	FDIV	16
	4	Not Used *	
	5	Not Used *	
	6	Not Used *	
	7	Not Used *	
	1(0-7)	Not Used *	
	070RSS	MUL	
	1	DIV	8
4	2	ASH	
	3	ASHC	
	4 RDD	XOR	
	5	ILLEGAL	
	6	Not Used *	8
	7 RNN	SOB	
3	104 [0xx]xx	EMT	
	104 [1xx]xx	TRAP	2
	1700xx	Not Used	
	|	(64 possible)	64
2	1777		
1	UNUSED		
0	Undefined 16 - 77 + others	None	1

Priority

12
15
6
13
9
8
4
7
5
14
12
11
10
3
0

ICODE Address generation

Priority	Select Bits 7	6	5	4	3	2	1	0	# of Slots
2	0	0	I11	I10	I9	I8	I7	I6	64
15	0	1	0	0	0	I2	I1	I0	8
6	0	1	I14	I13	I12	I15	D0	S0	48
13	0	1	1	1	1	I5	I4	I3	8
9	1	0	0	I8	I7	I6	I5	D0	32
8	1	0	1	I8	I7	I6	I5	D0	28
4	1	1	0	0	I11	I10	I9	D0	16
7	1	1	0	1	I15	I8	I7	I6	16
5	1	1	1	0	I6	I5	I4	I3	16
14	1	1	1	1	0	0	0	D0	2
12	1	1	1	1	0	0	1	D0	2
11	1	1	1	1	0	1	0	D0	2
10	1	1	1	1	0	1	1	BR	2
3	1	1	1	1	1	0	0	I8	2
0	1	1	1	1	1	1	1	1	1

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Resulting Icode Addresses and corresponding instruction

0-63	User defined				
64	HALT		96	BIC	D, S
65	WAIT		97	BIC	D, S@
66	RTI		98	BIC	D@, S
67	BPT		99	BIC	D@, S@
68	IOT		100	BICB	D, S
69	RESET		101	BICB	D, S@
70	RTT		102	BICB	D@, S
71	User defined		103	BICB	D@, S@
72	MOV	D, S	104	BIS	D, S
73	MOV	D, S@	105	BIS	D, S@
74	MOV	D@, S	106	BIS	D@, S
75	MOV	D@, S@	107	BIS	D@, S@
76	MOVB	D, S	108	BISB	D, S
77	MOVB	D, S@	109	BISB	D, S@
78	MOVB	D@, S	110	BISB	D@, S
79	MOVB	D@, S@	111	BISB	D@, S@
80	CMP	D, S	112	ADD	D, S
81	CMP	D, S@	113	ADD	D, S@
82	CMP	D@, S	114	ADD	D@, S
83	CMP	D@, S@	115	ADD	D@, S@
84	CMPB	D, S	116	SUB	D, S
85	CMPB	D, S@	117	SUB	D, S@
86	CMPB	D@, S	118	SUB	D@, S
87	CMPB	D@, S@	119	SUB	D@, S@
88	BIT	D, S	120	RTS	
89	BIT	D, S@	121	User Defined	
90	BIT	D@, S	122	User Defined	
91	BIT	D@, S@	123	SPL	
92	BITB	D, S	124	} condition Codes	
93	BITB	D, S@	125		
94	BITB	D@, S	126		
95	BITB	D@, S@	127		

```
128     CLR     D
129     CLR     DØ
130     CLRB    D
131     CLRB    DØ
132     COM     D
133     COM     DØ
134     COMB    D
135     COMB    DØ

136     INC     D
137     INC     DØ
138     INCB    D
139     INCB    DØ
140     DEC     D
141     DEC     DØ
142     DECB    D
143     DECB    DØ

144     NEG     D
145     NEG     DØ
146     NEGB    D
147     NEGB    DØ
148     ADC     D
149     ADC     DØ
150     ADCB    D
151     ADCB    DØ

152     SBC     D
153     SBC     DØ
154     SBCB    D
155     SBCB    DØ
156     TST     D
157     TST     DØ
158     TSTB    D
159     TSTB    DØ

160     ROR     D
161     ROR     DØ
162     RORB    D
163     RORB    DØ
164     ROL     D
165     ROL     DØ
166     ROLB    D
167     ROLB    DØ

168     ASR     D
169     ASR     DØ
170     ASRB    D
171     ASRB    DØ
172     ASL     D
173     ASL     DØ
174     ASLB    D
175     ASLB    DØ

176   } MARK
177
178     MTPS    D
179     MTPS    DØ
180     MFPI    D       (SS=DD)
181     MFPI    DØ
182     MFPD    D
183     MFPD    DØ

184     MTPI    D
185     MTPI    DØ
186     MTPD    D
187     MTPD    DØ
188     SXT     D
189     SXT     DØ
190     MFPS    D
191     MFPS    DØ
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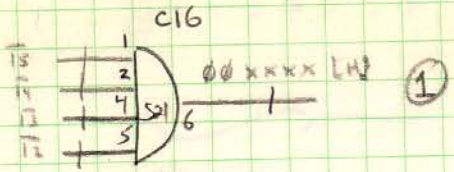
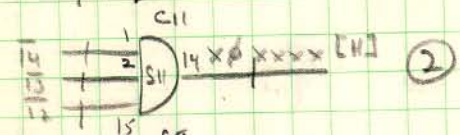
192	MUL	D	(SS=DD)
193	MUL	D#	
194	DIV	D	
195	DIV	D#	
196	ASH	D	
197	ASH	D#	
198	ASHC	D	
199	ASHC	D#	
200	XOR	D	
201	XOR	D#	
202	} ILLegal		
203			
204	} User Define		
205			
206	} SOB		
207			
208	} USER Defined		
209			
210			
211			
212			
213			
214			
215			
216	} User Defined		
217			
218			
219			
220			
221			
222			
223			

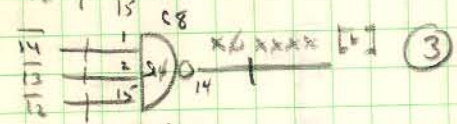
224	FADD
225	FSUB
226	FMUL
227	FDIV
228	} USER Defined
229	
230	
231	
232	} USER Defined
233	
234	
235	
236	
237	
238	
239	
240	JMP D
241	JMP D# (Illegal)
242	SWAB D
243	SWAB D#
244	NO Branch
245	Branch
246	JSR D
247	JSR D# (Illegal)
248	EMT
249	TRAP
250	|||
251	
252	
253	
254	
255	UNDEFINED - ILLEGAL

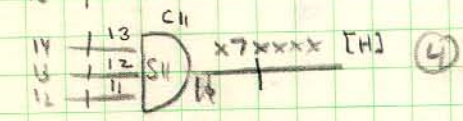
Printer

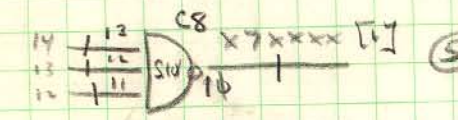
I code Address Encode Logic

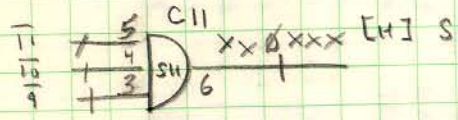


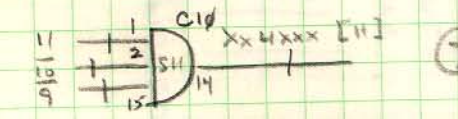


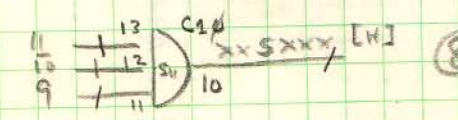


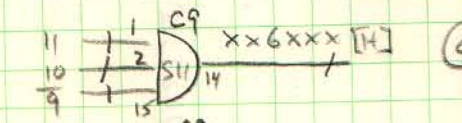


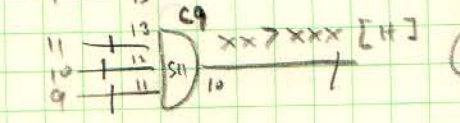


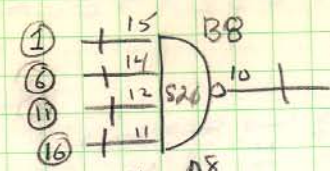


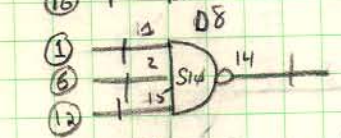


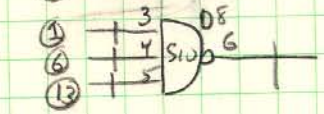


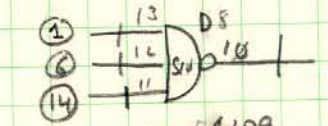


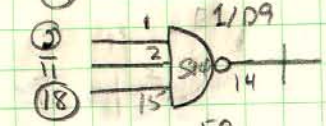


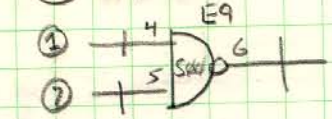


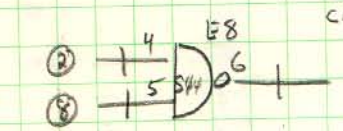


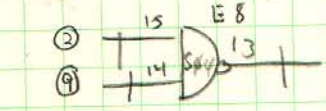


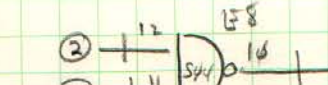


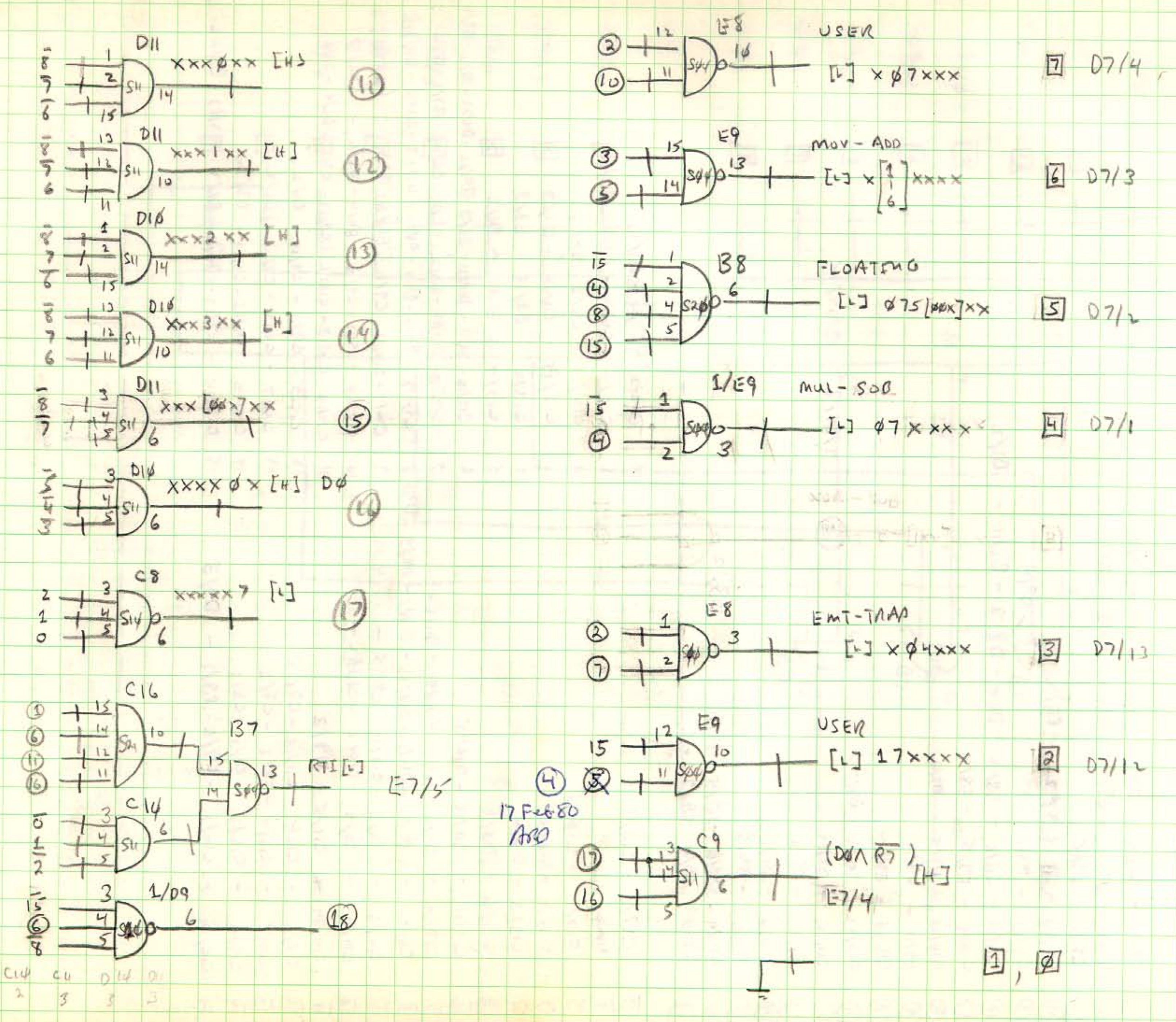












D11
XXXφXX [H]
D11
XXX1XX [H]
D1φ
XXX2XX [H]
D1φ
XXX3XX [H]
D11
XXX[φφX]XX
D1φ
XXXXφX [H] Dφ
C8
XXXXX7 [L]
C16
C14
B7
RTI [L]
E7/5
1/D9
E8
USER
[L] Xφ7XXX
7 D7/4
E9
MOV - ADD
[L] X[1 6]XXXX
6 D7/3
B8
FLOATING
[L] φ75[φφX]XX
5 D7/2
1/E9
MUL - SOB
[L] φ7XXXX
4 D7/1
E8
EMT-TRAP
[L] Xφ4XXX
3 D7/13
E9
USER
[L] 17XXXX
2 D7/12
17 Feb 80 ABB
C9
(DφΛ R7) [H]
E7/4
1, φ

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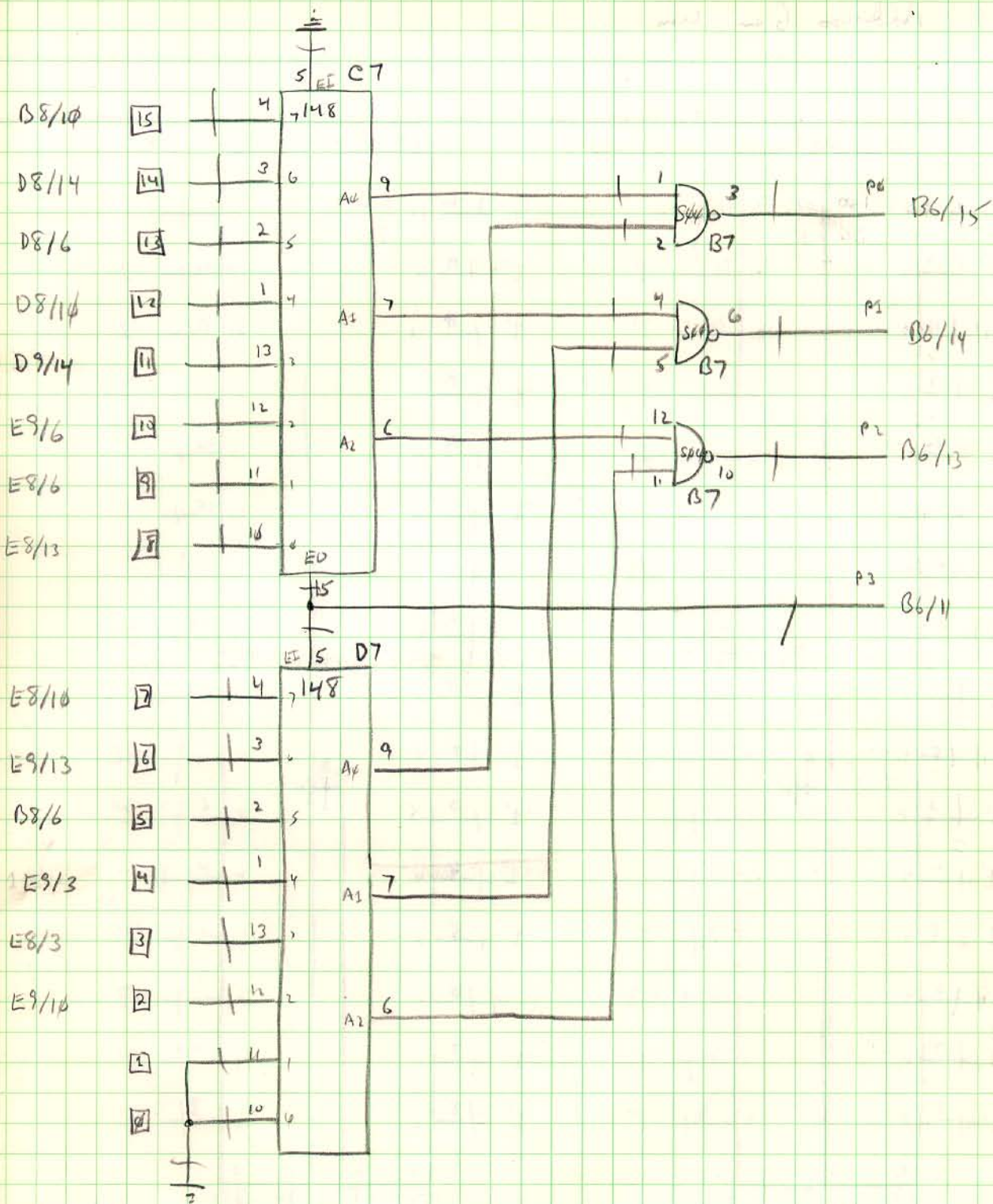
Icode Address Encoder Priority Encoder

① C16/6 – B8/15 – D8/13 – D8/11 – D8/3 – E9/4 – C16/15
② C11/14 – D9/1 – E8/15 – E8/12 – E8/5 – E8/1
③ C8/14 – E9/15
④ C11/10 – E9/2 – B8/2
⑤ C8/10 – E9/14 – E9/11
⑥ C16/14 – C11/6 – D8/12 – D8/4 – D8-2 – D9/4 – B8/14 – B1/2
⑦ C10/14 – E9/5 – E8/2
⑧ C10/10 – E8/5 – B8/4
⑨ C9/14 – E8/14
⑩ C9/10 – E8/11
⑪ C16/12 – D11/4 – B8/12
⑫ D11/10 – D8/15
⑬ D10/14 – D8/5
⑭ D10/10 – D8/11
⑮ D11/6 – B8/5
⑯ C16/11 – D10/6 – C9/5 – B8/11 — B3/2
⑰ C8/6 – C9/4 – C9/3
⑱ 1/09/6 – 1/09/15

Ø	C12/3 – C10/3	Ø C12/2 – C8/5 – B1/16
1	None	1 C12/7 – C10/4 – C8/4 – B3/16
2	C12/11 – C10/5	2 C12/10 – C8/3 B4/16
3	C12/14 – D10/5	3 C12/15 – B1/8 – B1/3
4	C13/3 – D10/4	4 C13/2 – B3/18 – B3/3
5	C13/6 – D10/3	5 C13/7 – B4/18 – B4/3
6	C13/11 – D11/15 – D10/15	6 C13/10 – D11/11 – D10/11 – B6/3 – B4/22 – B4/23 – B1/1 – B1/6
7	C13/14 – D11/2 – D11/4 – D11/5 – D11/12	7 C13/15 – D10/12 – D10/2 – B6/22 – B6/23 – B3/1 – B3/6
8	C14/3 – D11/13 – D11/1 – D10/13 – D10/1 – D11/3 – D9/5	8 C14/2 – B4/6 – B4/1 – D1/22 – D1/23 – B1/5 – E10/15
9	C14/6 – C4/3 – C10/15 – C9/15 —	9 C14/7 – C10/11 – C9/11 – B6/6 – B3/4 (E11/11)
10	C14/10 – C11/4 – C10/2 – C10/12 –	10 C14/10 – C9/12 – C9/2 – B4/4 – D3/6 (E11/10)
11	C14/14 – C11/5 – D9/2	11 C14/15 – C10/13 – C10/1 – C9/13 – C9/1 – B6/4 – D3/6
12	C15/3 – C16/5 – C11/15 – C8/15	12 C15/2 – C11/11 – C8/11 – B6/2
13	C15/6 – C16/4 – C11/2 – C8/2	13 C15/7 – C11/12 – C8/12 – D3/2
14	C15/11 – C16/2 – C4/1 – C8/1	14 C15/10 – C11/13 – C8/13 – D3/2
15	C15/14 – C16/1 – E9/1 – B8/1 – D9/3	15 C15/15 – E9/12 – B6/1 – B4/2 – B3/23 – B3/22 (E11/9)


C7
148
D7
148
B8/10
D8/14
D8/6
D8/10
D9/14
E9/6
E8/6
E8/13
E8/10
E9/13
B8/6
E9/3
E8/3
E9/10
A0
A1
A2
A3
EI
EO
B7
B6/15
B6/14
B6/13
B6/11
P0
P1
P2
P3

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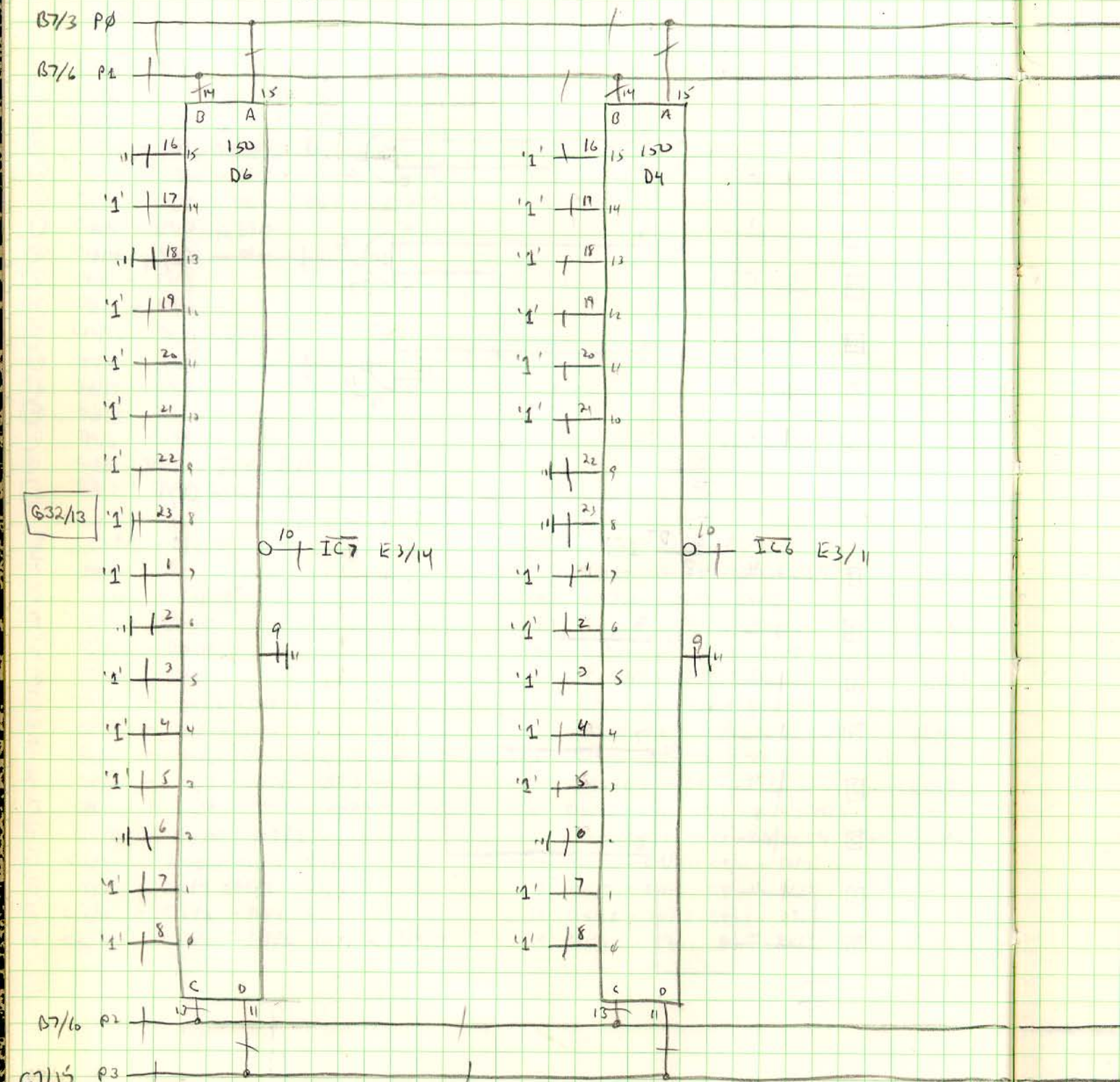
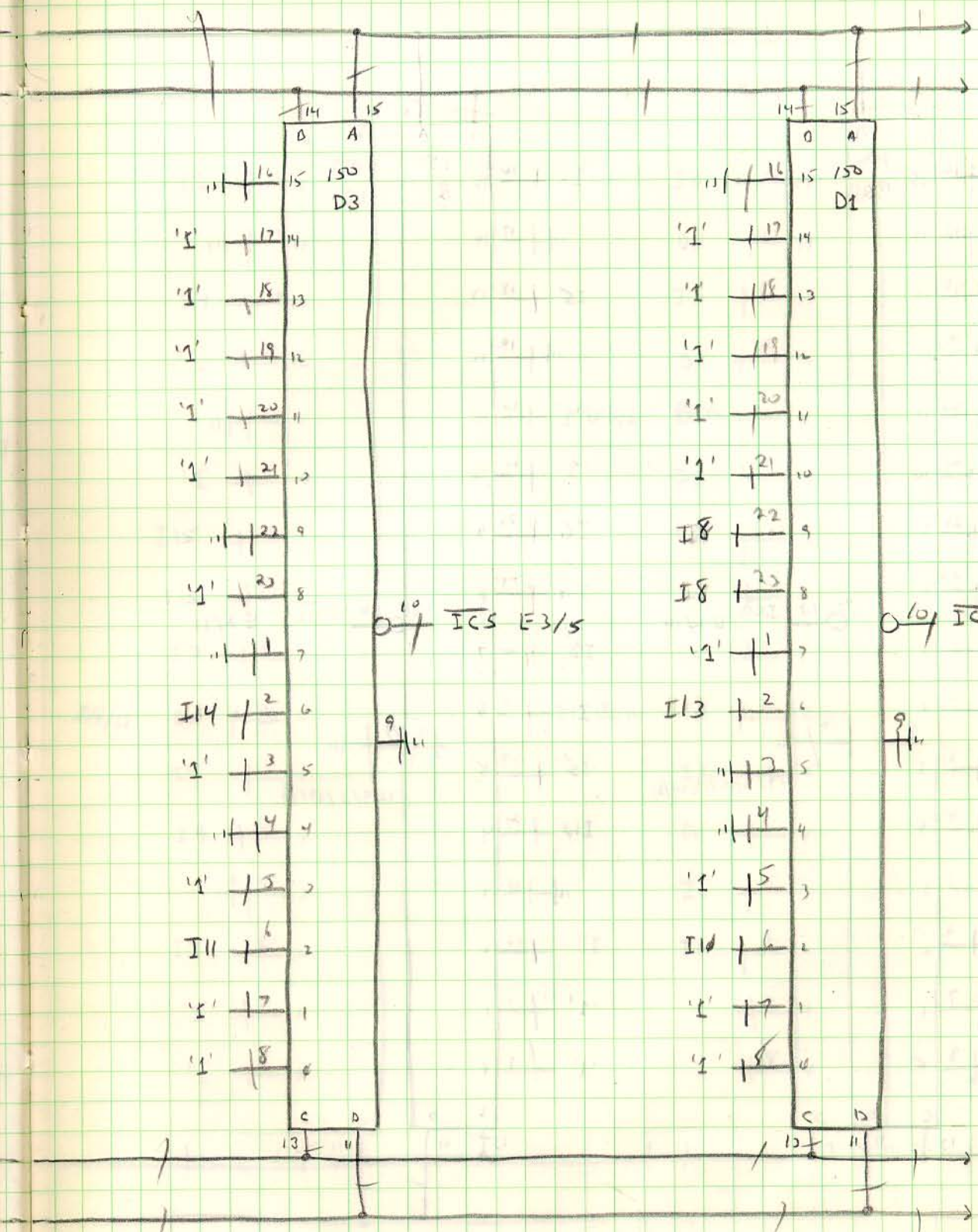
Icode Address Generation




14
15
D
A
150
D3
'1'
I14
I11
C
D
13
11
10
IC5 E3/5
9
14
150
D1
I8
I13
I10
IC4 E3/2

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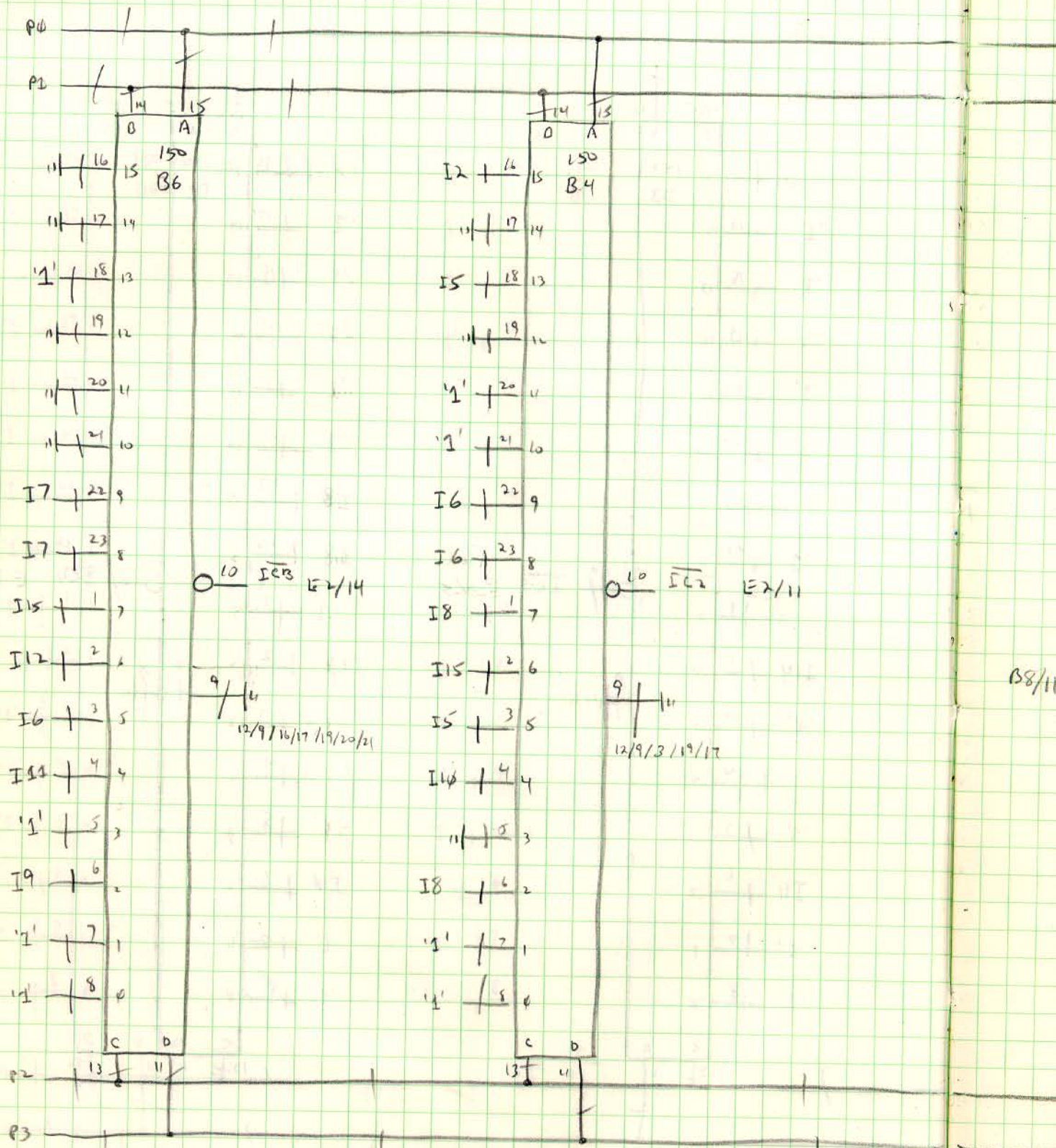
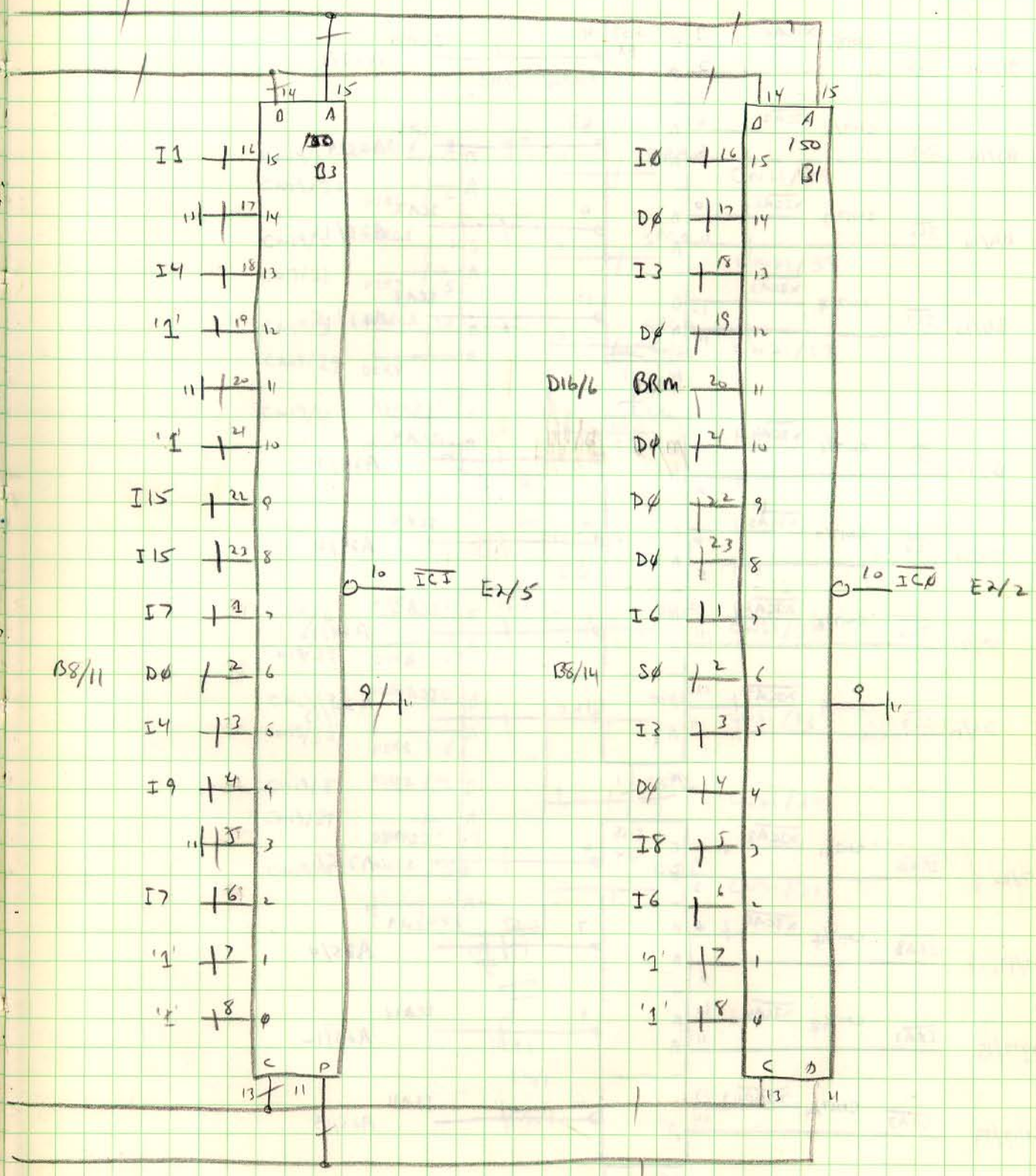
ARD


P0
P1
P2
P3
14
15
0
A
150
B6
150
B4
I2
'1'
I5
I7
I15
I12
I6
I11
I9
I8
I14
C
D
13
11
10
I$\overline{E3}$
E2/14
I$\overline{E2}$
E2/11
9
11
12/9/16/17/19/20/21
12/9/3/19/17
B8/11


14
15
0
A
150
B3
I1
16
15
17
14
I4
18
13
'1'
19
12
20
11
'1'
21
10
I15
22
9
I15
23
8
I7
1
7
B8/11
DØ
2
6
I4
3
5
I9
4
4
5
3
I7
6
2
'1'
7
1
'1'
8
Ø
C
D
13
11
10
ICI
E2/5
9
14
15
0
A
150
B1
IØ
16
15
DØ
17
14
I3
18
13
DØ
19
12
D16/6
BRm
20
11
DØ
21
10
DØ
22
9
DØ
23
8
I6
1
7
B8/14
SØ
2
6
I3
3
5
DØ
4
4
I8
5
3
I6
6
2
'1'
7
1
'1'
8
Ø
C
D
13
11
10
ICØ
E2/2
9
14

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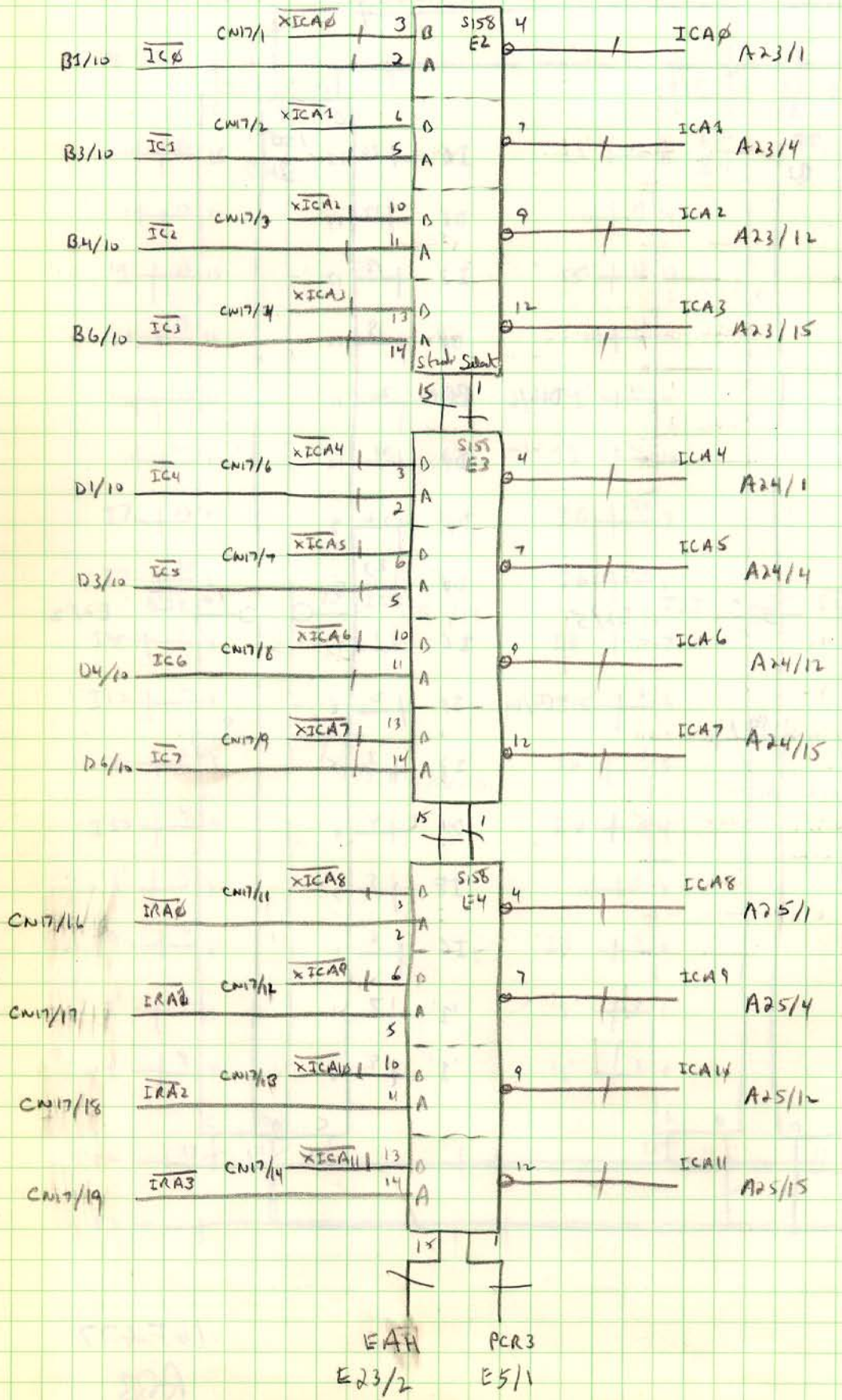
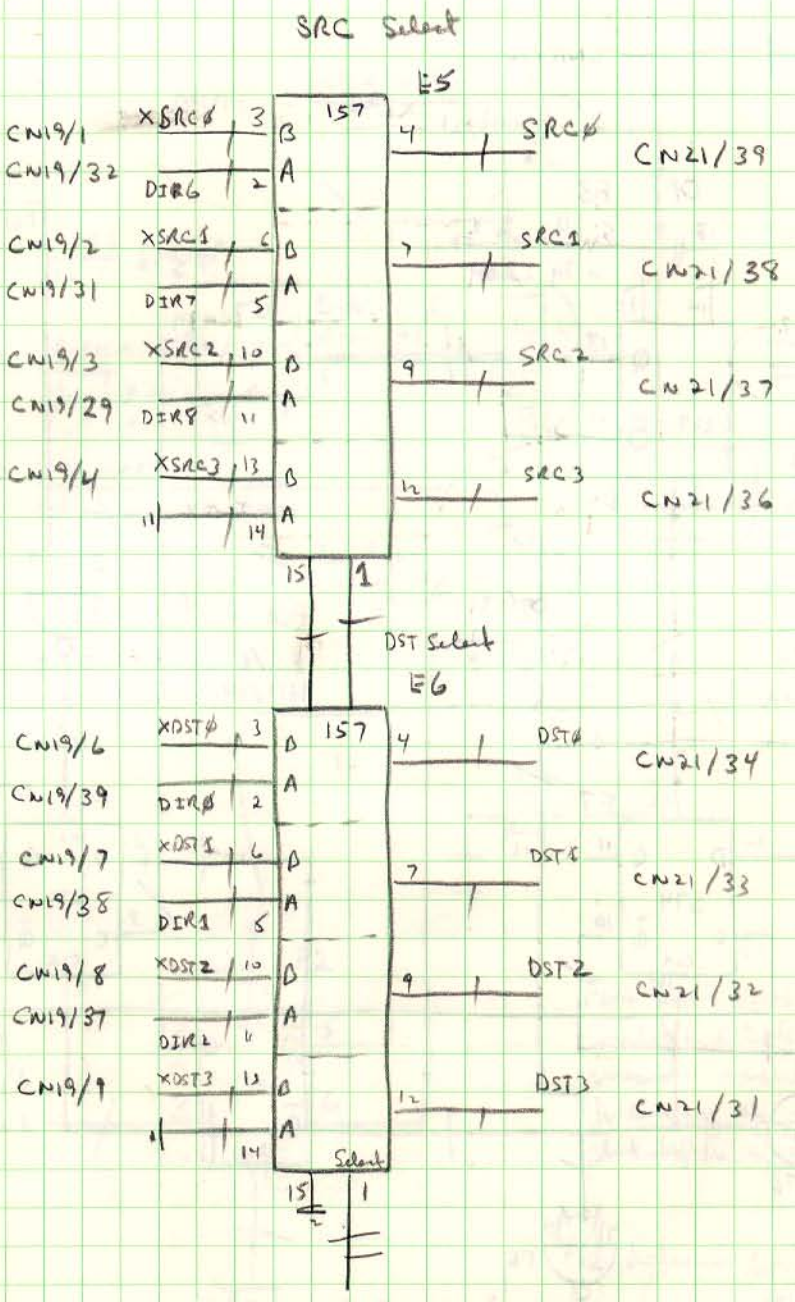
ARB

I Code Address Selector




SRC Select
E5
157
CN19/1
CN19/32
XSRC0
DIR6
CN19/2
CN19/31
XSRC1
DIR7
CN19/3
CN19/29
XSRC2
DIR8
CN19/4
XSRC3
SRC0
SRC1
SRC2
SRC3
CN21/39
CN21/38
CN21/37
CN21/36
DST Select
E6
CN19/6
CN19/39
XDST0
DIR0
CN19/7
CN19/38
XDST1
DIR1
CN19/8
CN19/37
XDST2
DIR2
CN19/9
XDST3
DST0
DST1
DST2
DST3
CN21/34
CN21/33
CN21/32
CN21/31
Select
PCR3
E4/1
F5/1

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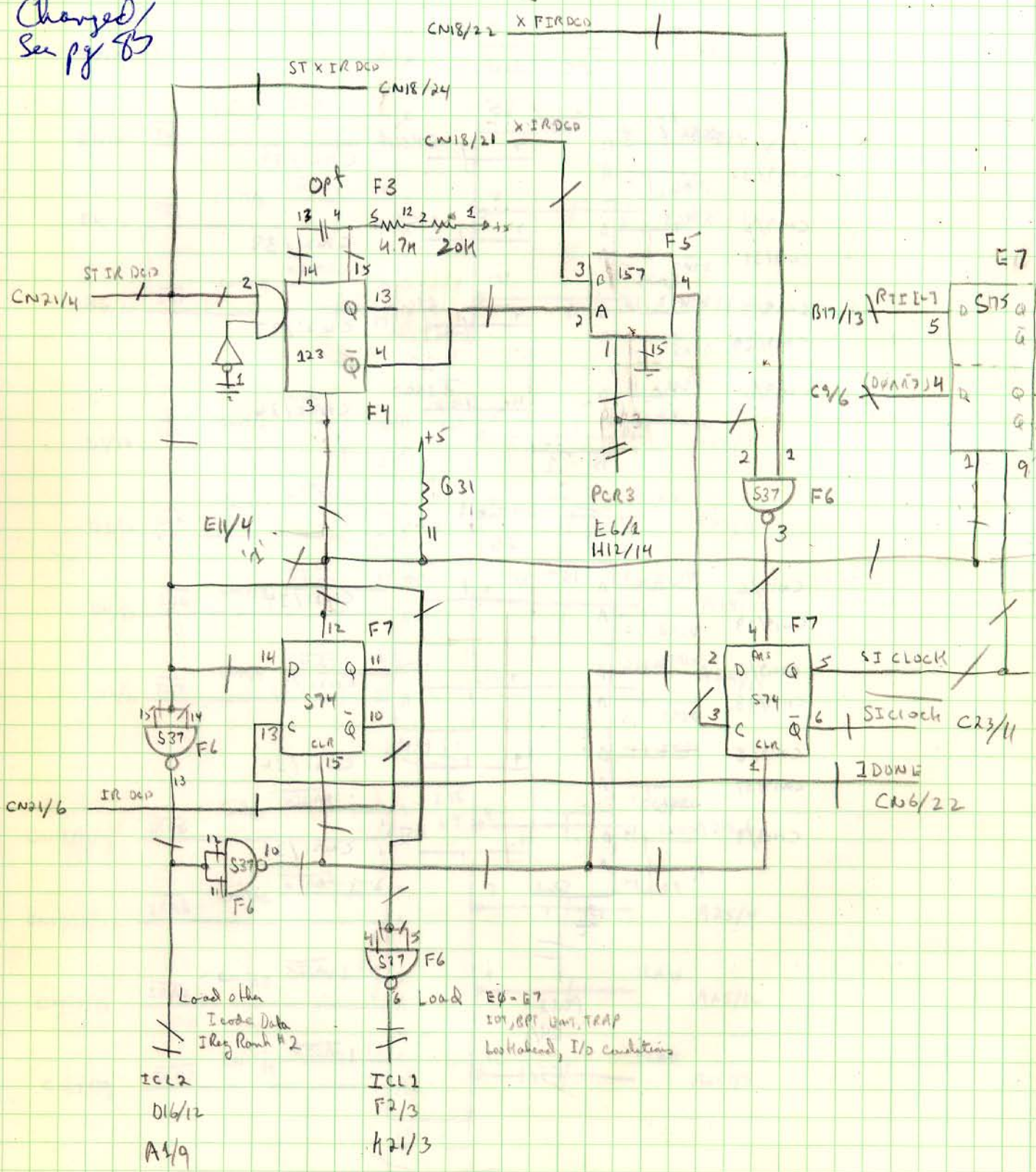
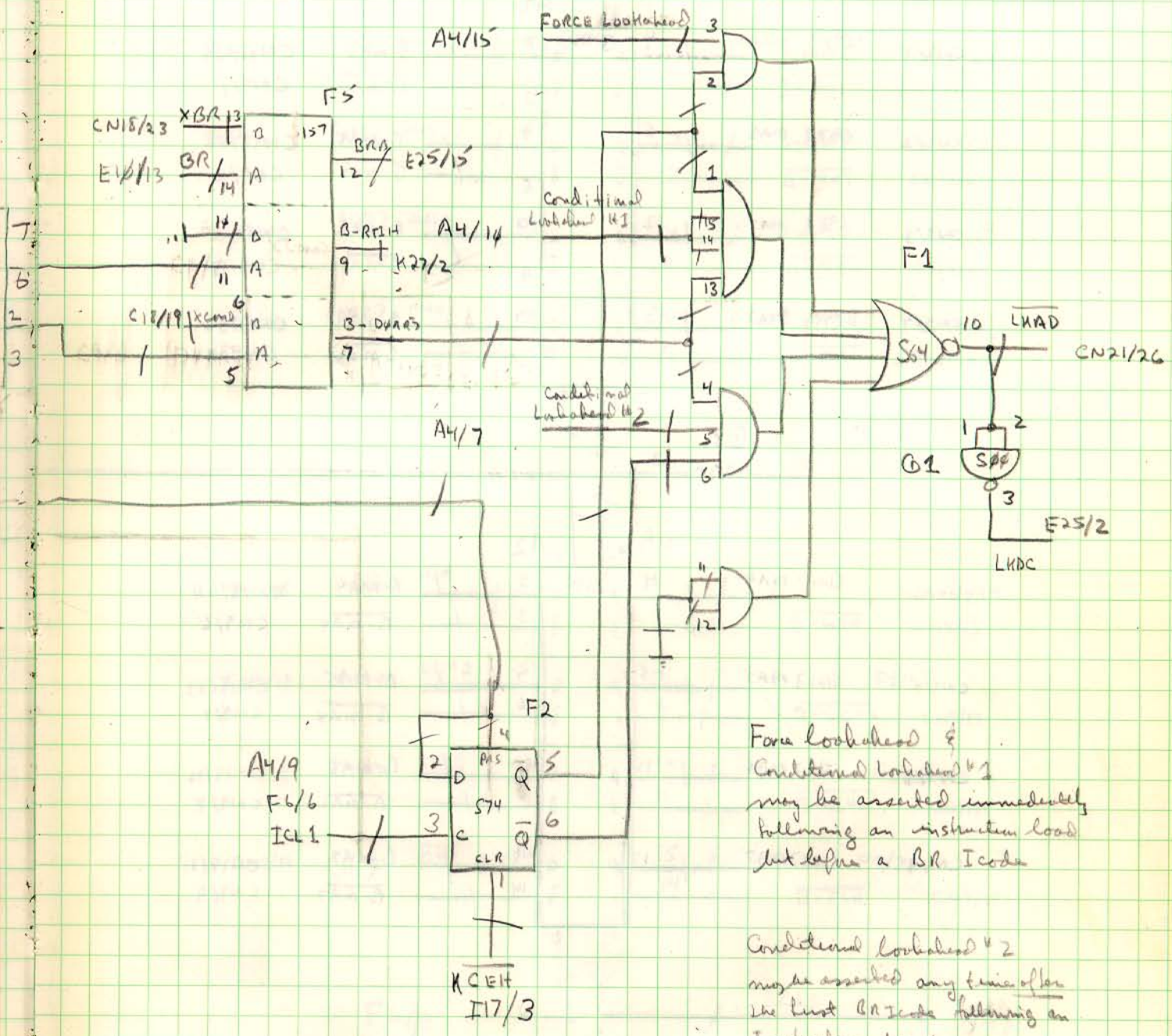
ARB

Instruction Address Encoding Timing / Icode Data loading

Changed/
See pg 85



Lookahead Encoding



Force Lookahead & Conditional Lookahead #1 may be asserted immediately following an instruction load but before a BR Icode

Conditional Lookahead #2 may be asserted any time after the first BR Icode following an Instruction decode.

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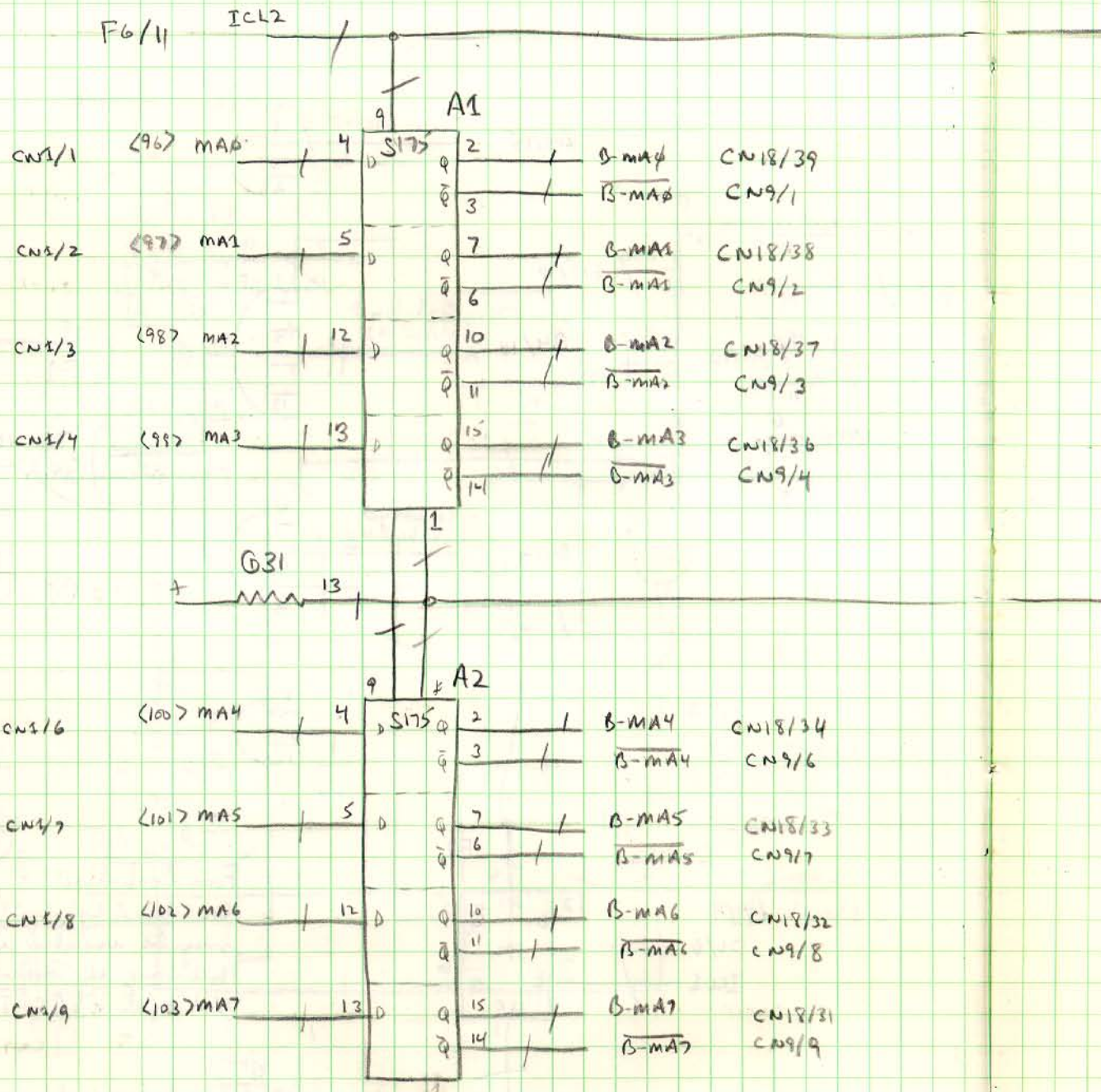
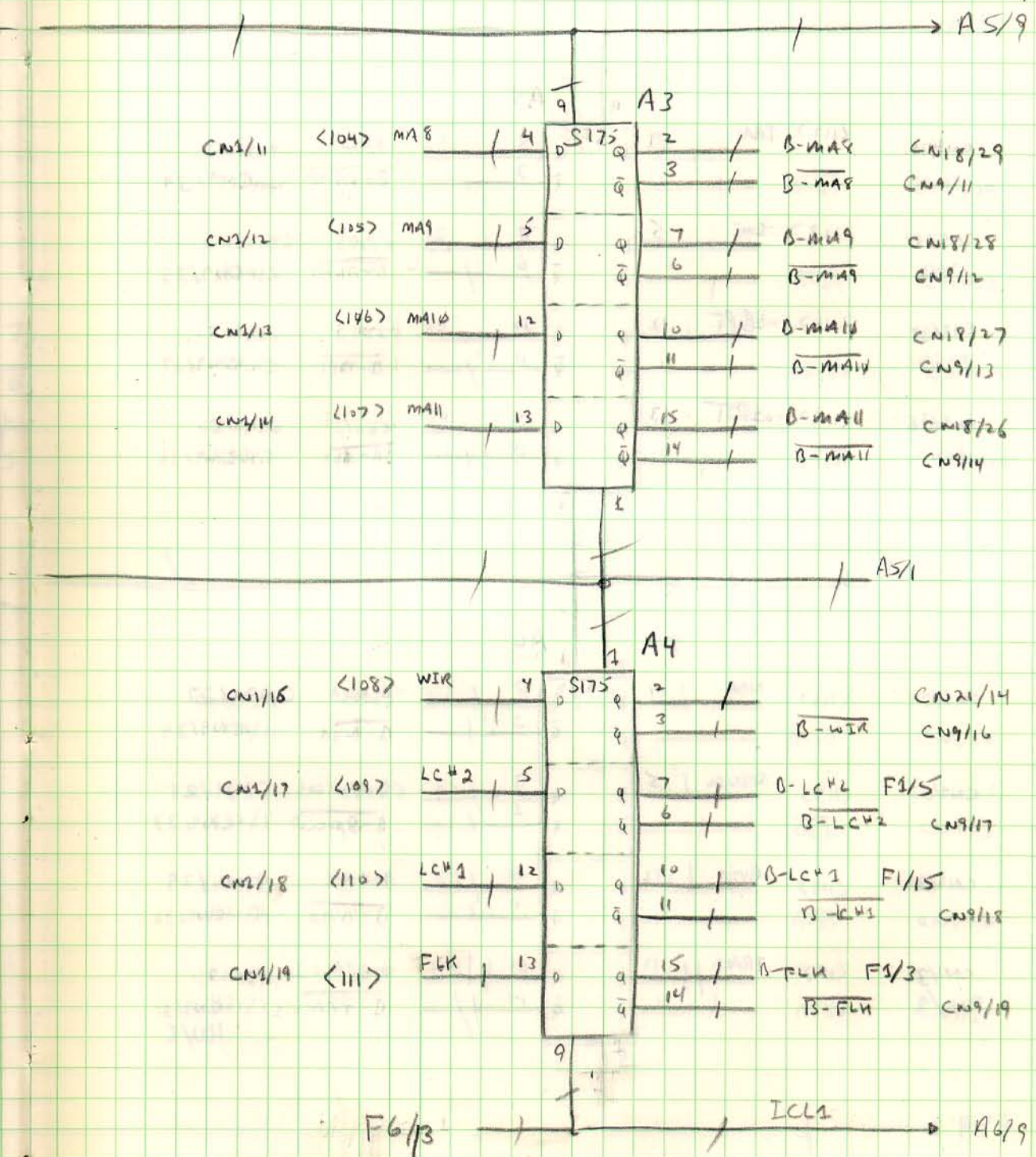
ARB

Icode Data Buffers




A5/9
A3
S175
CN1/11 <104> MA8 4 D Q 2 B-MA8 CN18/29
Q̄ 3 B-MA8 CN9/11
CN1/12 <105> MA9 5 D Q 7 B-MA9 CN18/28
Q̄ 6 B-MA9 CN9/12
CN1/13 <106> MA10 12 D Q 10 B-MA10 CN18/27
Q̄ 11 B-MA10 CN9/13
CN1/14 <107> MA11 13 D Q 15 B-MA11 CN18/26
Q̄ 14 B-MA11 CN9/14
A5/1
A4
S175
CN1/16 <108> WIR 4 D Q 2 CN21/14
Q̄ 3 B-WIR CN9/16
CN1/17 <109> LCH2 5 D Q 7 B-LCH2 F1/5
Q̄ 6 B-LCH2 CN9/17
CN1/18 <110> LCH1 12 D Q 10 B-LCH1 F1/15
Q̄ 11 B-LCH1 CN9/18
CN1/19 <111> FLK 13 D Q 15 B-FLK F1/3
Q̄ 14 B-FLK CN9/19
F6/13
ICL1
A6/9

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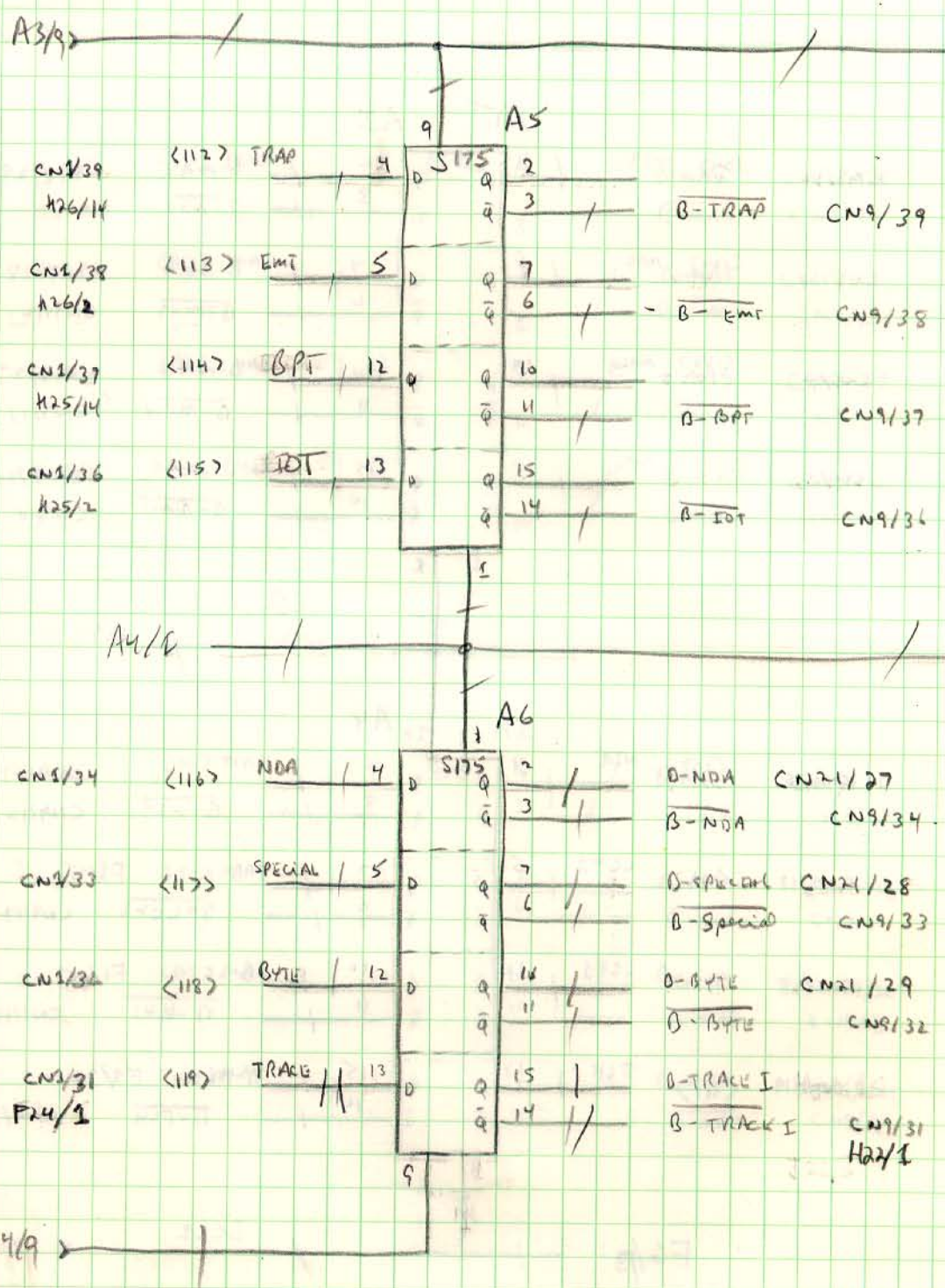
ARB

Icode Data Buffers (Continued)



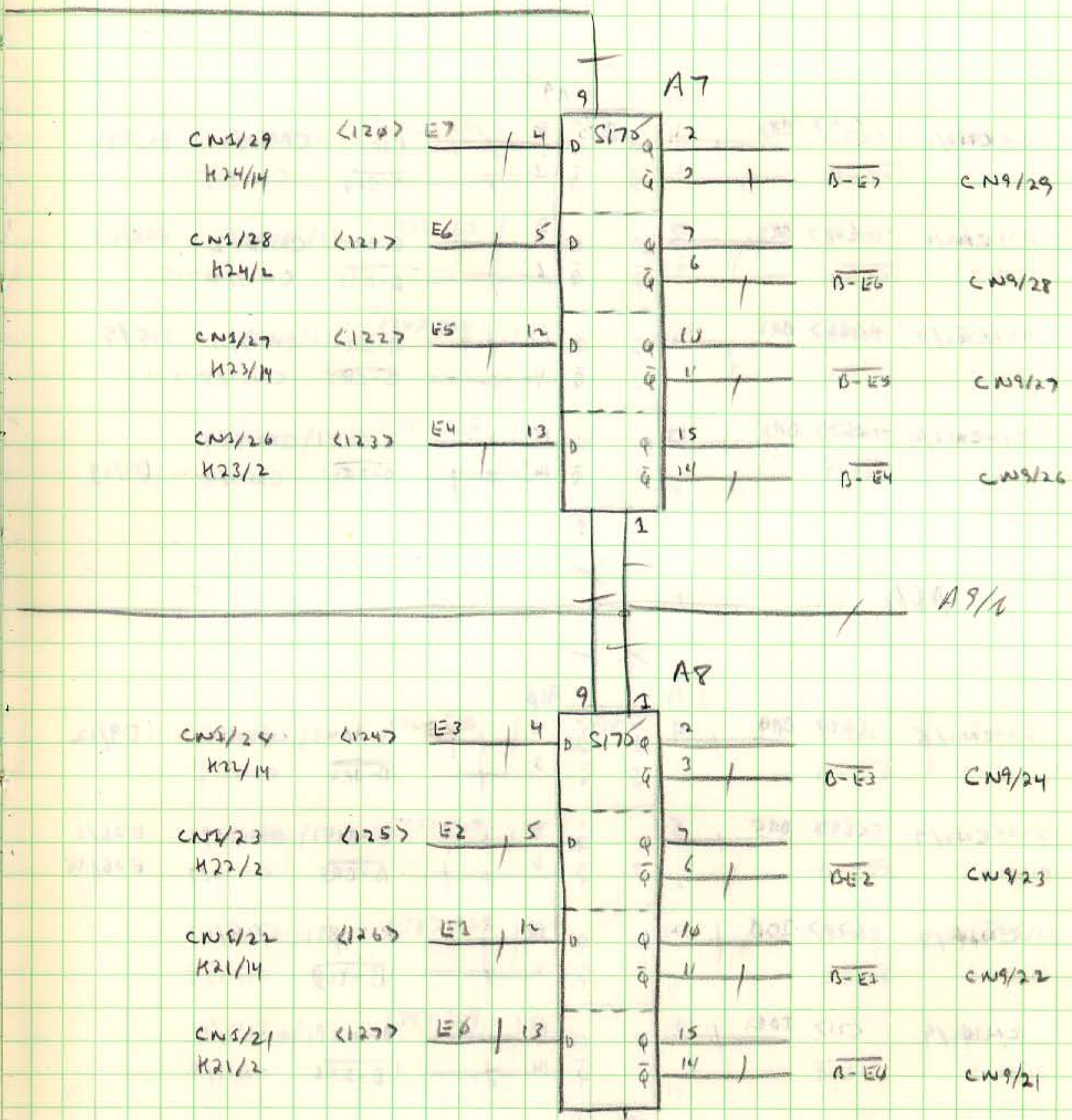

A7
S170
CN1/29 H24/14 <120> E7
CN1/28 H24/2 <121> E6
CN1/27 H23/14 <122> E5
CN1/26 H23/2 <123> E4
B-E7 CN9/29
B-E6 CN9/28
B-E5 CN9/27
B-E4 CN9/26
A9/1
A8
S170
CN1/24 H22/14 <124> E3
CN1/23 H22/2 <125> E2
CN1/22 H21/14 <126> E1
CN1/21 H21/2 <127> E0
B-E3 CN9/24
B-E2 CN9/23
B-E1 CN9/22
B-E0 CN9/21

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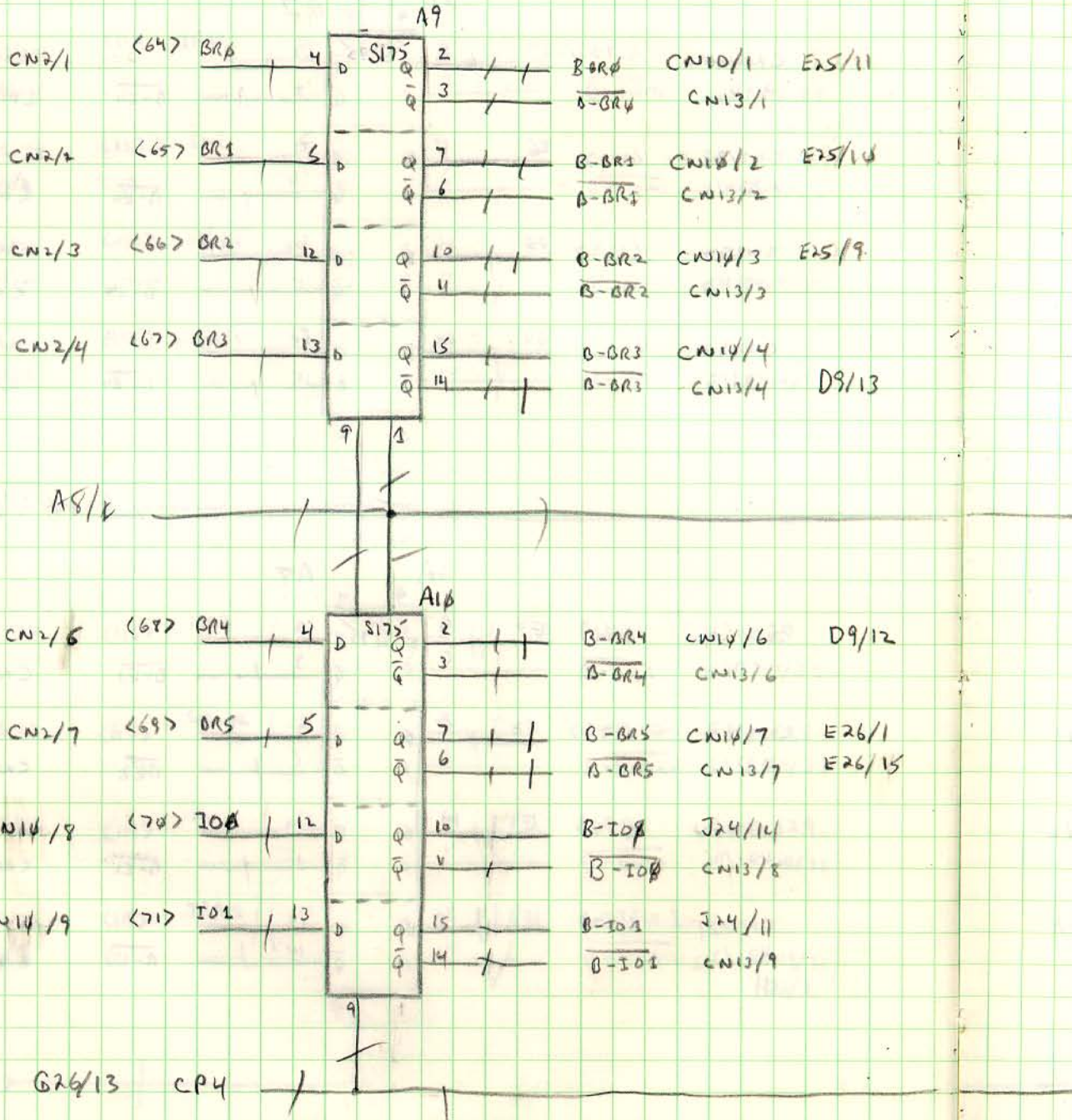
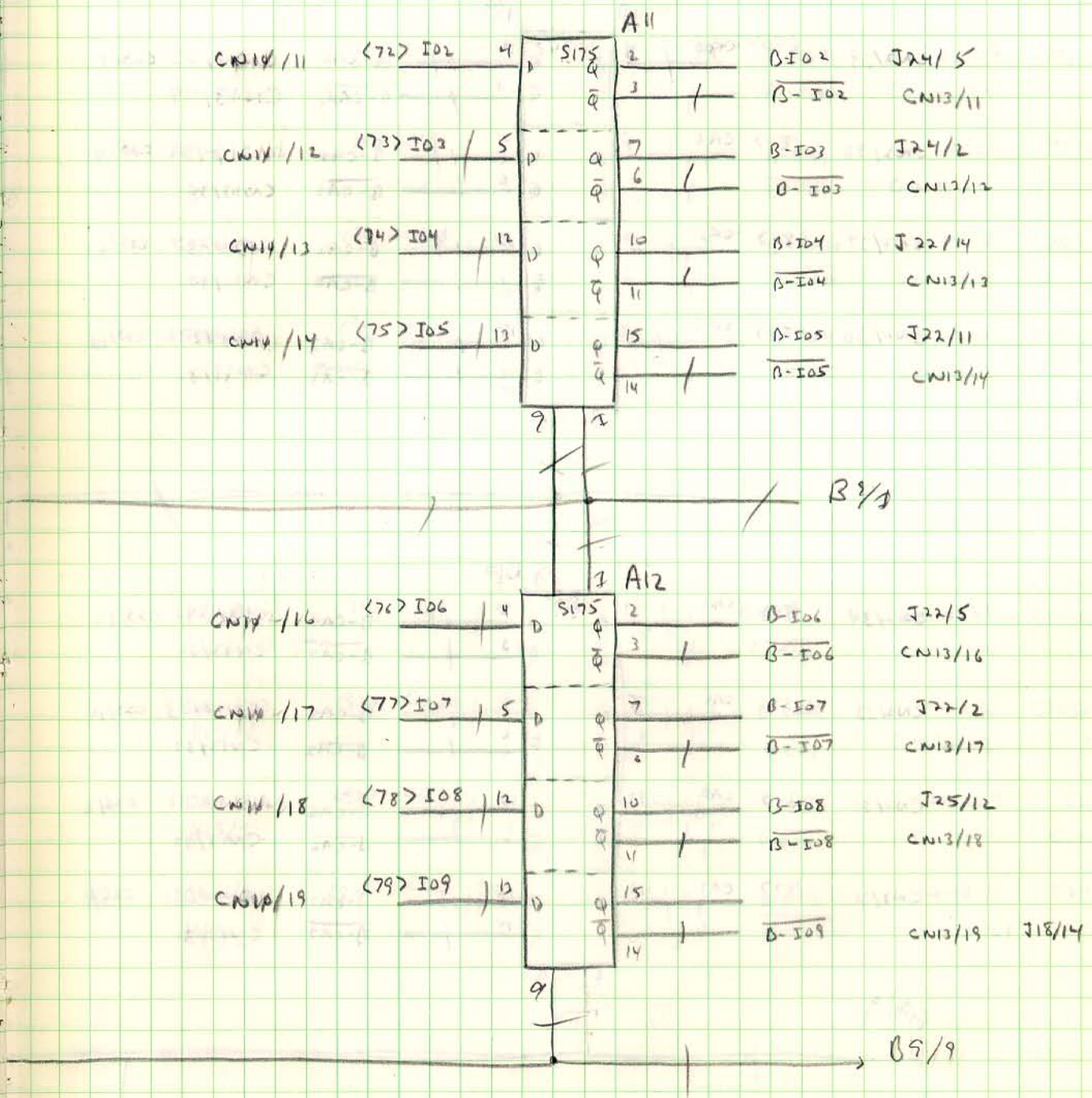
ABB

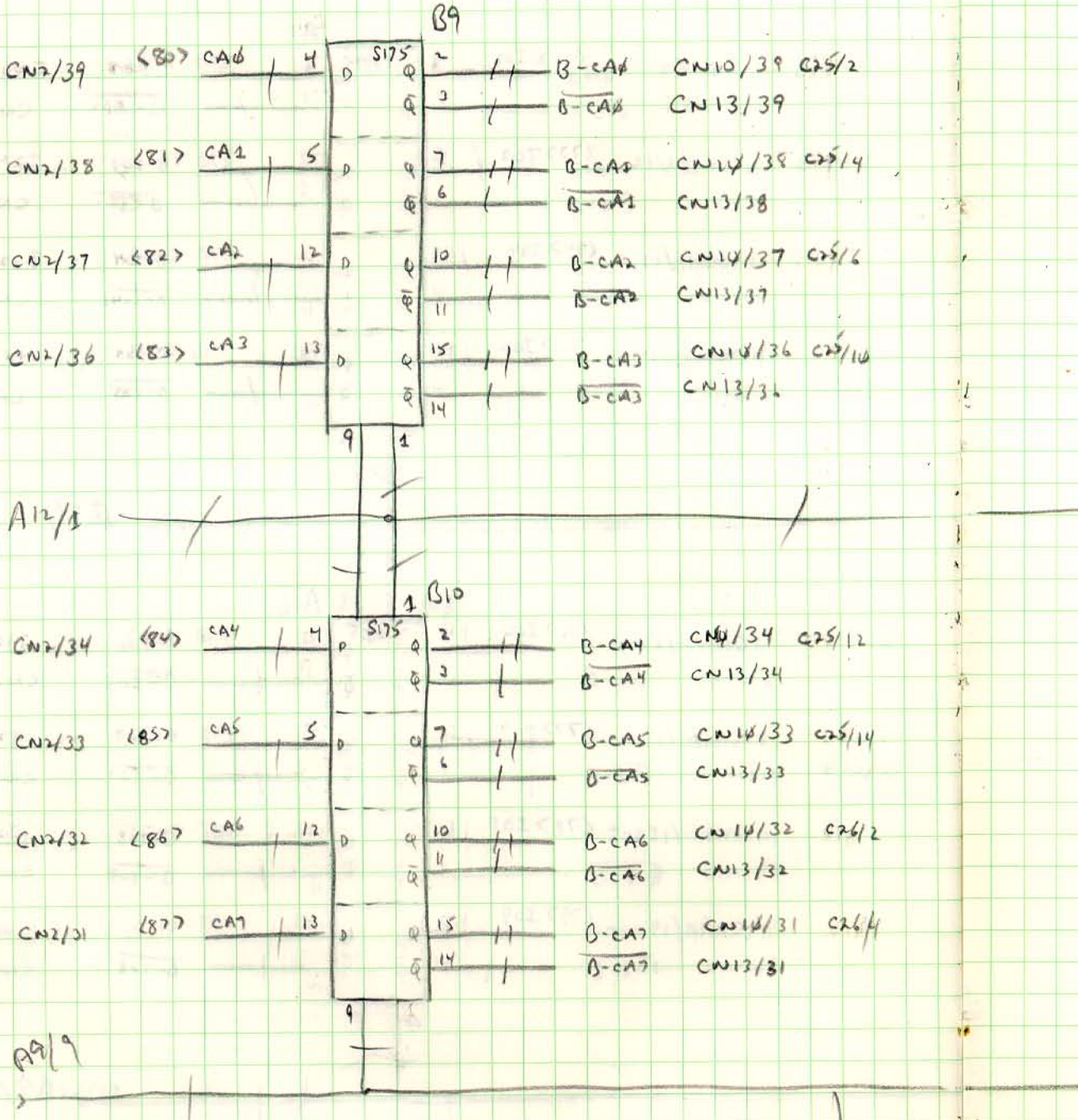
Microcode Data Buffers

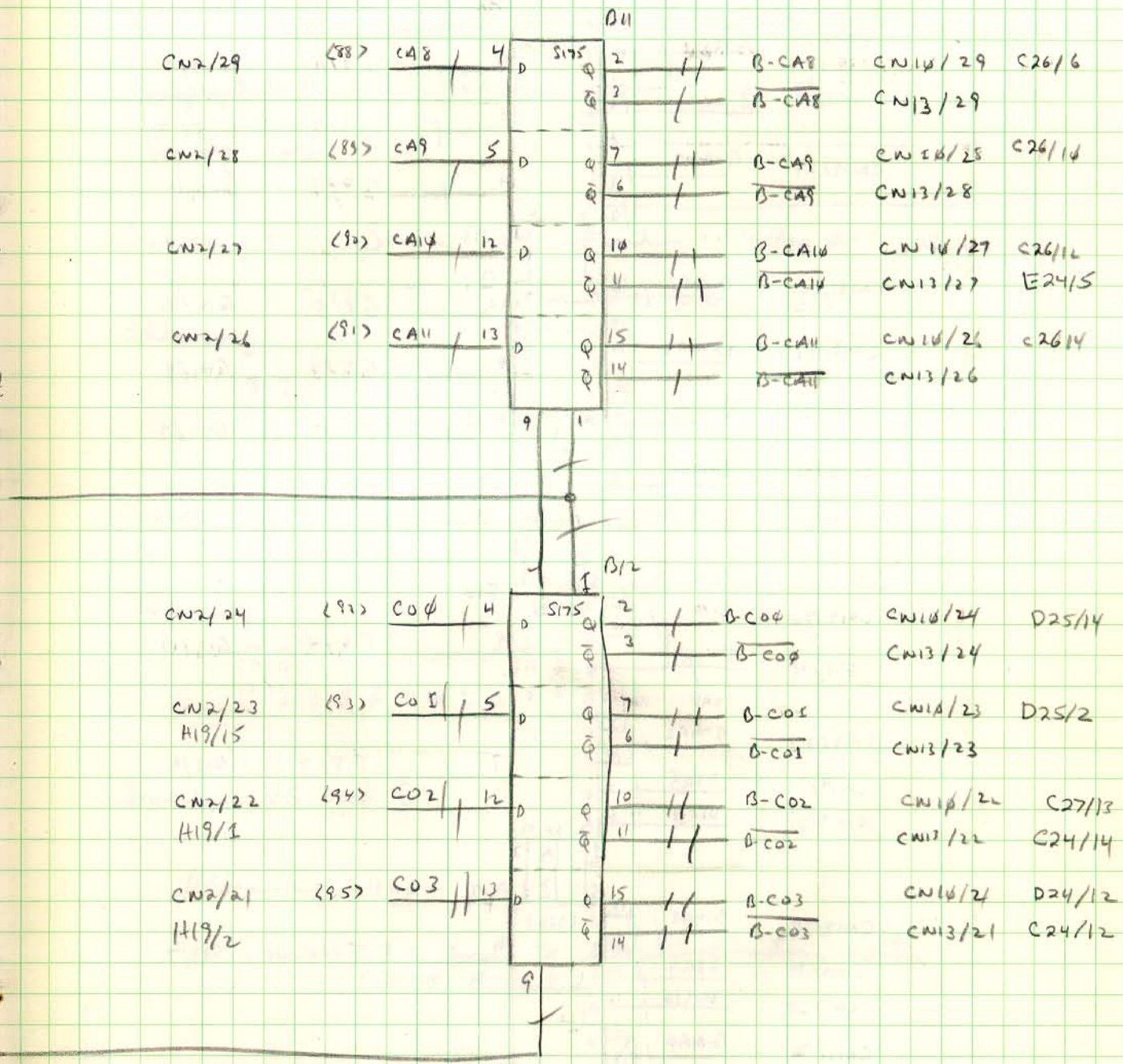



A11
A12
S175
CN14/11
CN14/12
CN14/13
CN14/14
CN14/16
CN14/17
CN14/18
CN14/19
<72> IO2
<73> IO3
<74> IO4
<75> IO5
<76> IO6
<77> IO7
<78> IO8
<79> IO9
B-IO2
B-IO3
B-IO4
B-IO5
B-IO6
B-IO7
B-IO8
B-IO9
J24/5
CN13/11
J24/2
CN13/12
J22/14
CN13/13
J22/11
CN13/14
J22/5
CN13/16
J22/2
CN13/17
J25/12
CN13/18
CN13/19
J18/14
B9/1
B9/9

19F477
ABD

Microcode Data Buffers (continued)




B11
CN2/29
<88>
CA8
4
S175
D
Q
Q̄
2
3
B-CA8
B-CA8
CN10/29
CN13/29
C26/6
CN2/28
<89>
CA9
5
7
6
B-CA9
B-CA9
CN10/25
CN13/28
C26/10
CN2/27
<90>
CA10
12
10
11
B-CA10
B-CA10
CN10/27
CN13/27
C26/12
E24/5
CN2/26
<91>
CA11
13
15
14
B-CA11
B-CA11
CN10/26
CN13/26
C26/14
9
1
B12
CN2/24
<92>
CO0
4
2
3
B-CO0
B-CO0
CN10/24
CN13/24
D25/14
CN2/23
H19/15
<93>
CO1
5
7
6
B-CO1
B-CO1
CN10/23
CN13/23
D25/2
CN2/22
H19/1
<94>
CO2
12
10
11
B-CO2
B-CO2
CN10/22
CN13/22
C27/13
C24/14
CN2/21
H19/2
<95>
CO3
13
15
14
B-CO3
B-CO3
CN10/21
CN13/21
D24/12
C24/12
9

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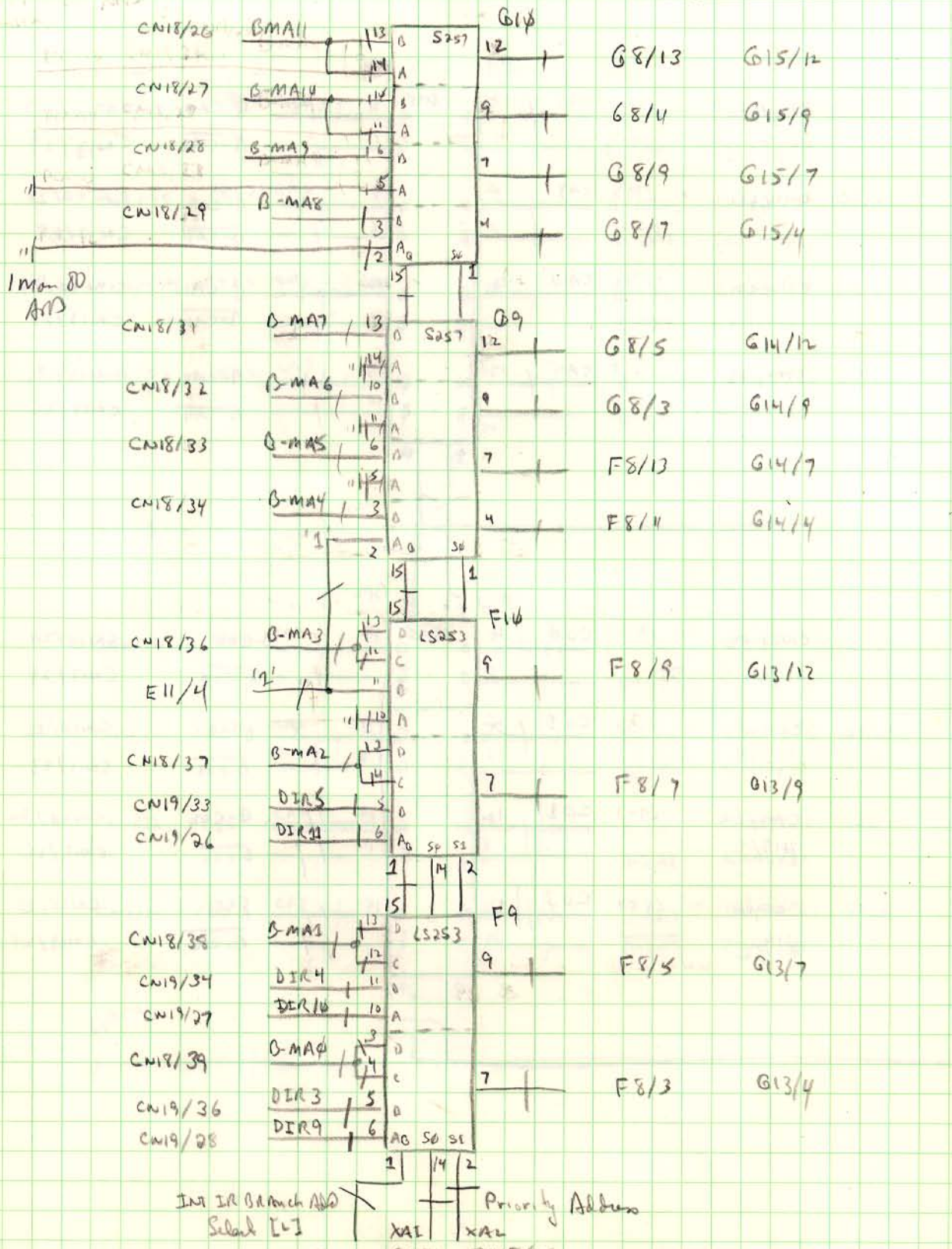
ASB

IR Decoded Branch Address Selection
(PDP-11 Decoder)

TRISTATE BUS TO MICRO controller



The PDP-11 Emulation decoder uses only four (4) of the possible 8 instruction programmed priorities - E1, E3, E5, and E7. BR Icodes to each of these selected priorities uses separate Microcode Addresses generated by the logic on the facing page:

Priority E1 Source Mode execution Modes ϕ-7

Source mode code from IR

Addressing

MA11	MA10	ϕ	ϕ	ϕ	ϕ	ϕ	1	ϕ	DIR11	DIR10	DIR9

Priority E3 Destination Mode execution Modes ϕ-7

Destination Mode Code from IR

Addressing

MA11	MA10	ϕ	ϕ	ϕ	ϕ	ϕ	1	1	DIR5	DIR4	DIR3

Priority E5 and E7

Addressing MAϕ - MA11

However E7 is used for illegal instructions in the PDP-11 Emulator

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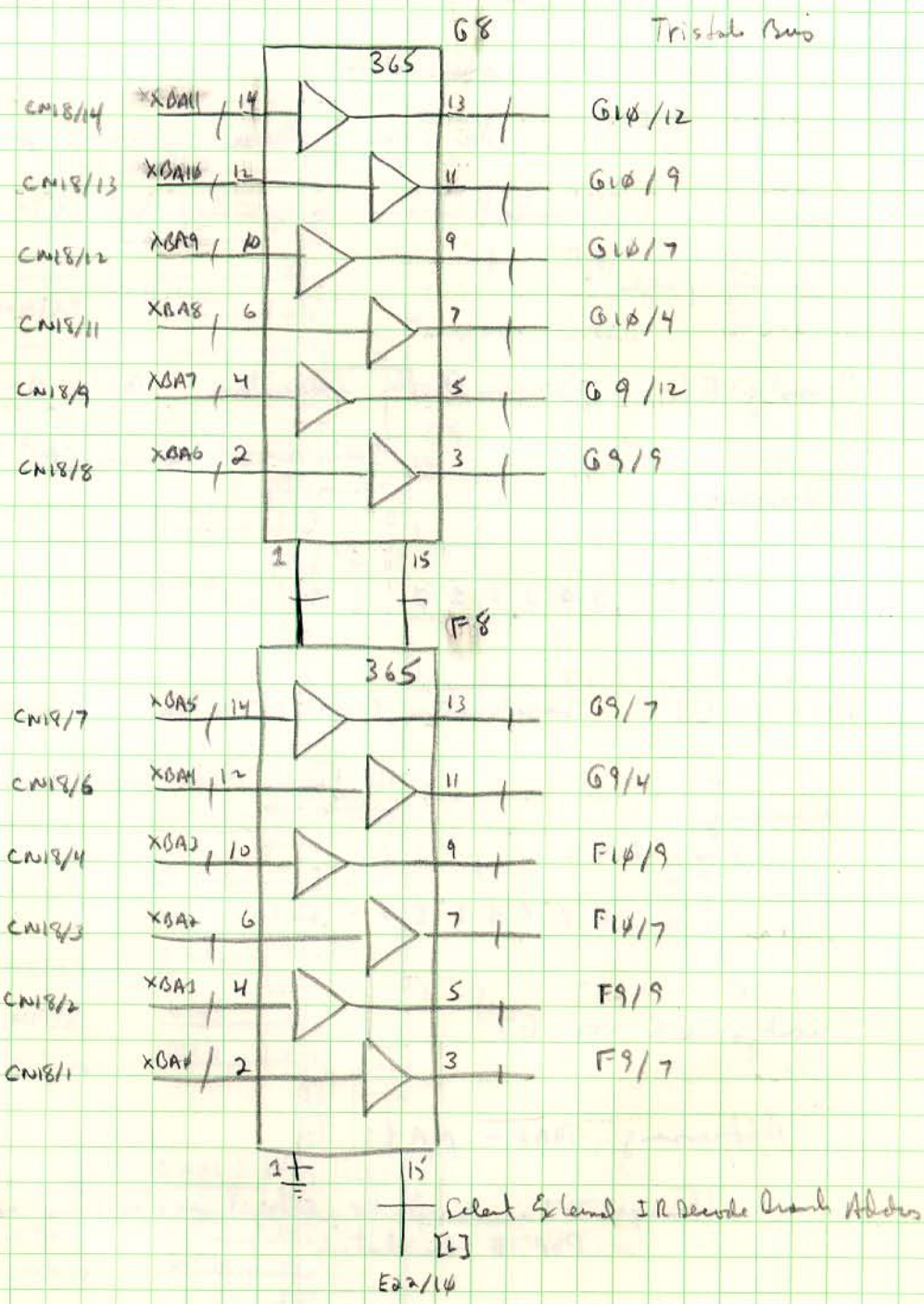
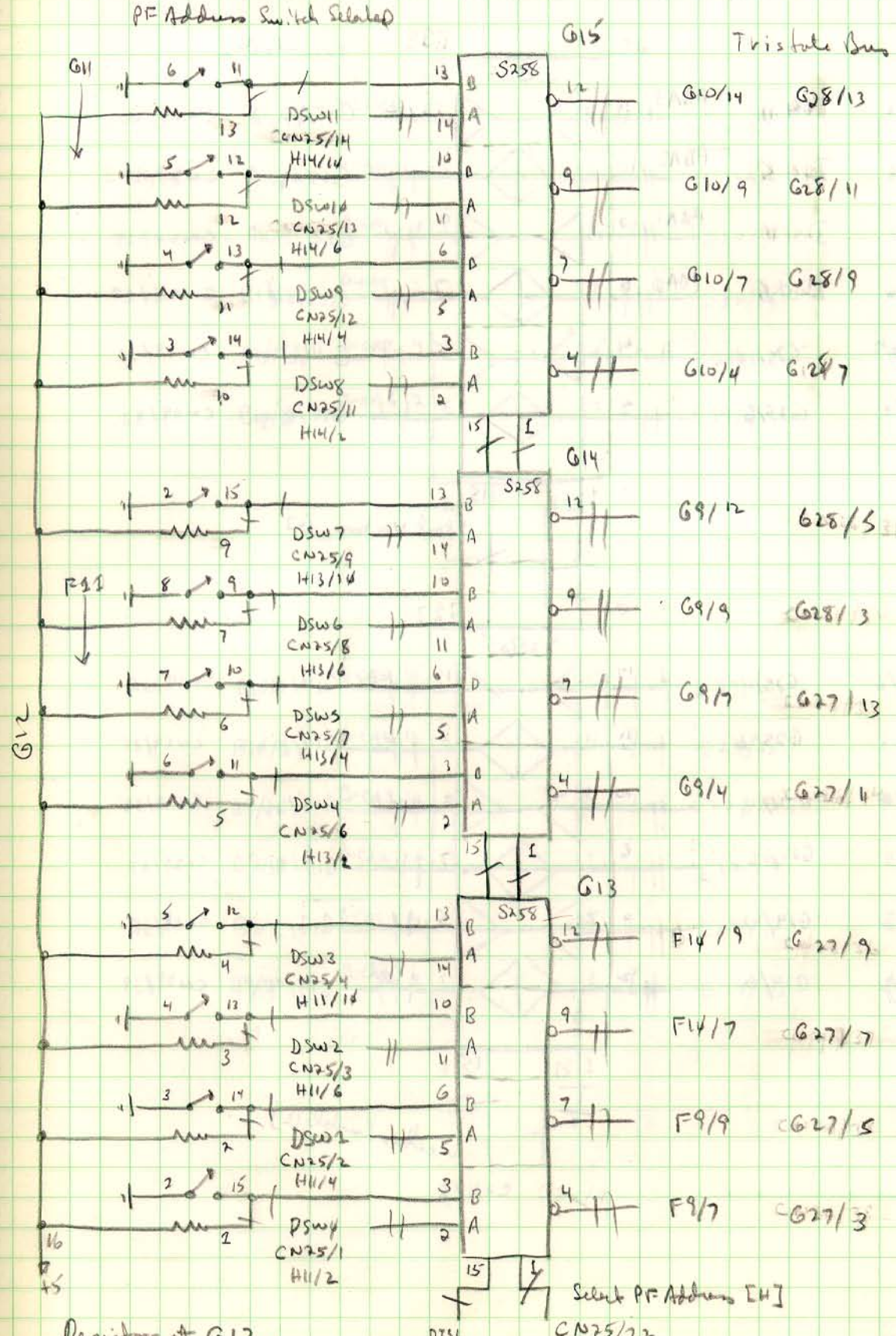
ARB

Extended IR Decode Branch Address Tristate Control



Power Fail Restart and Start Branch Address Tristate Control

PF Address Switch Selected



Resistors at G12
1050 ohm

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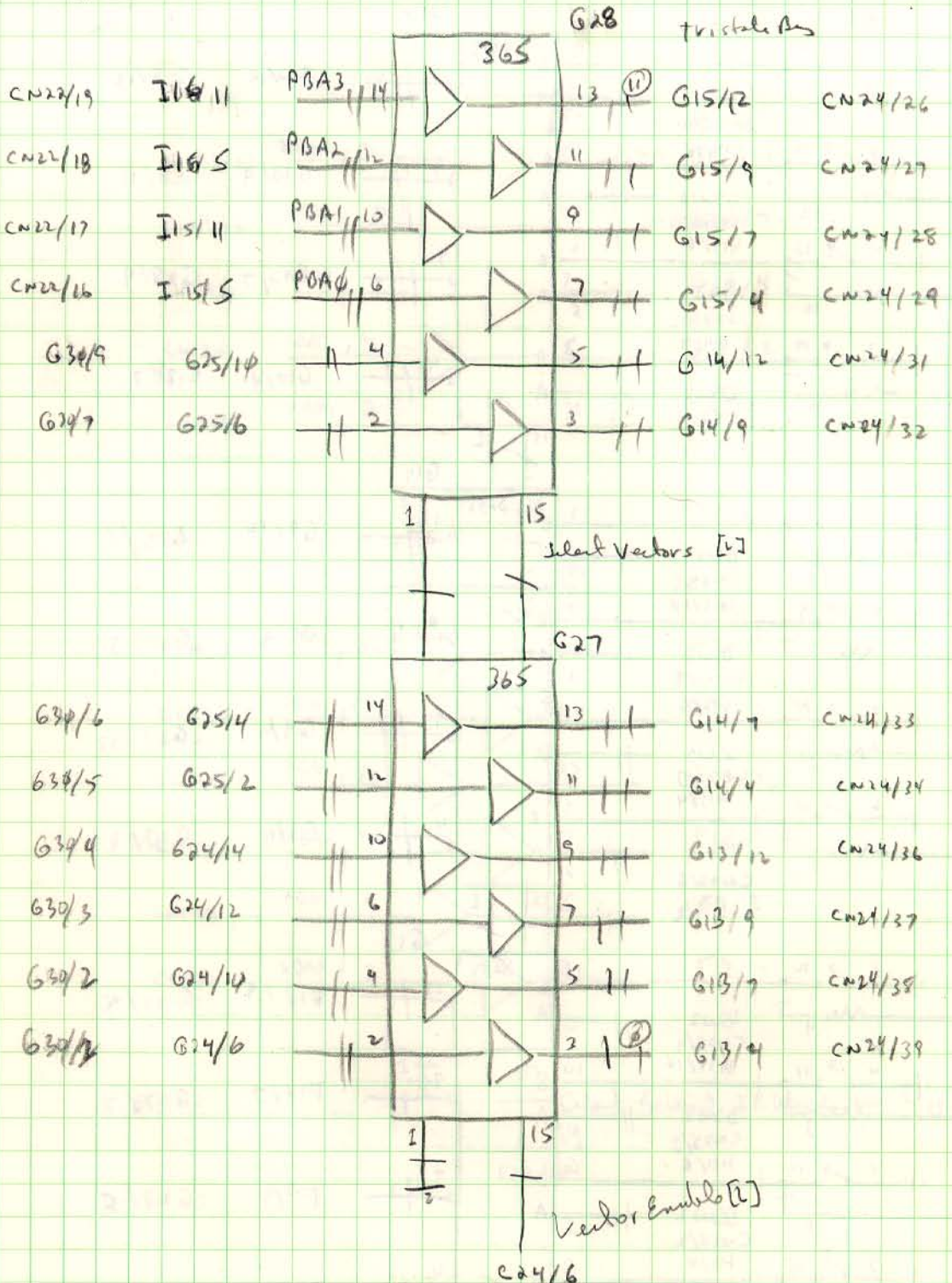
ABB

Vector Priority Branch Address Extension Bus Drive



Microcode Branch Address Bus Drivers

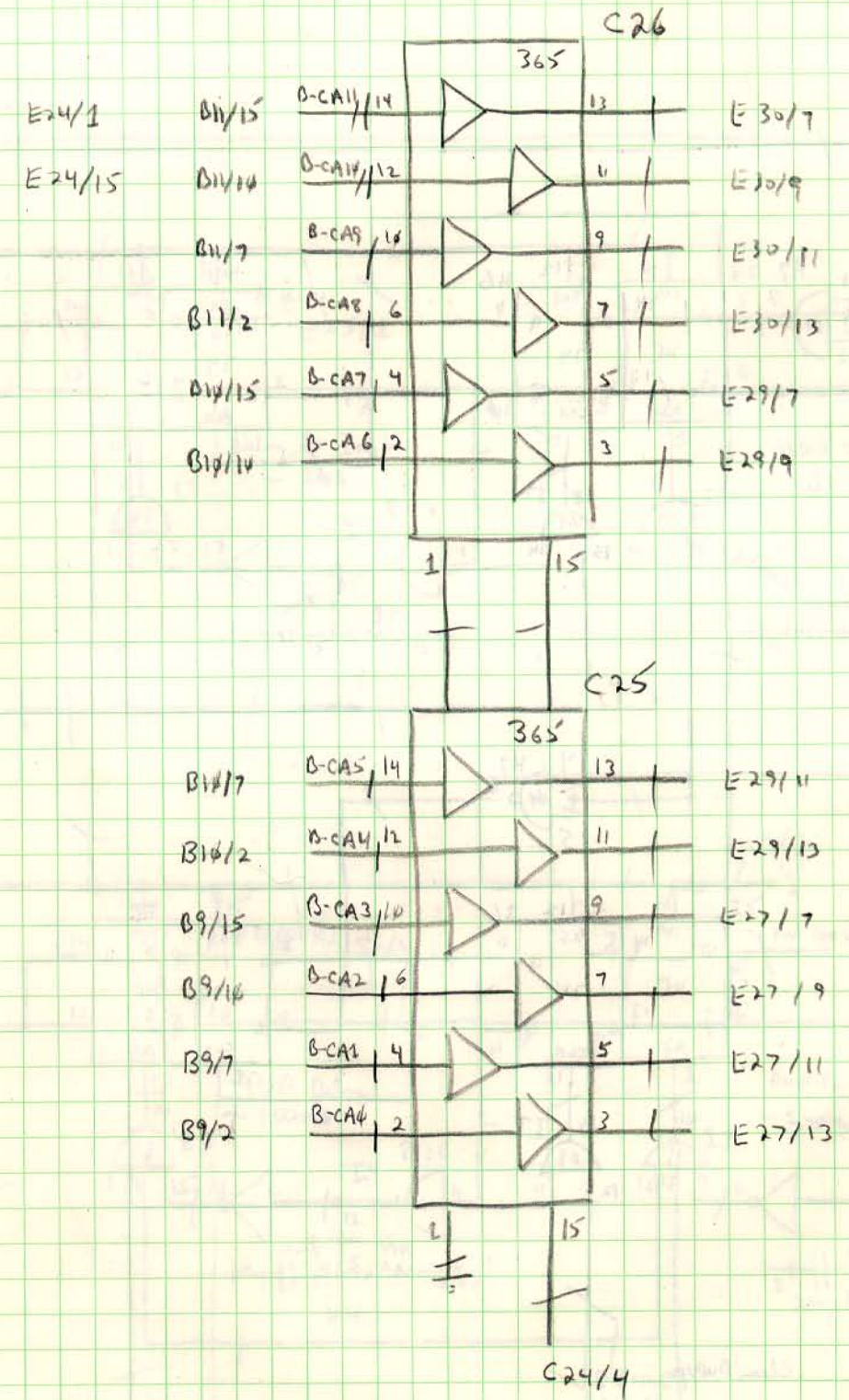


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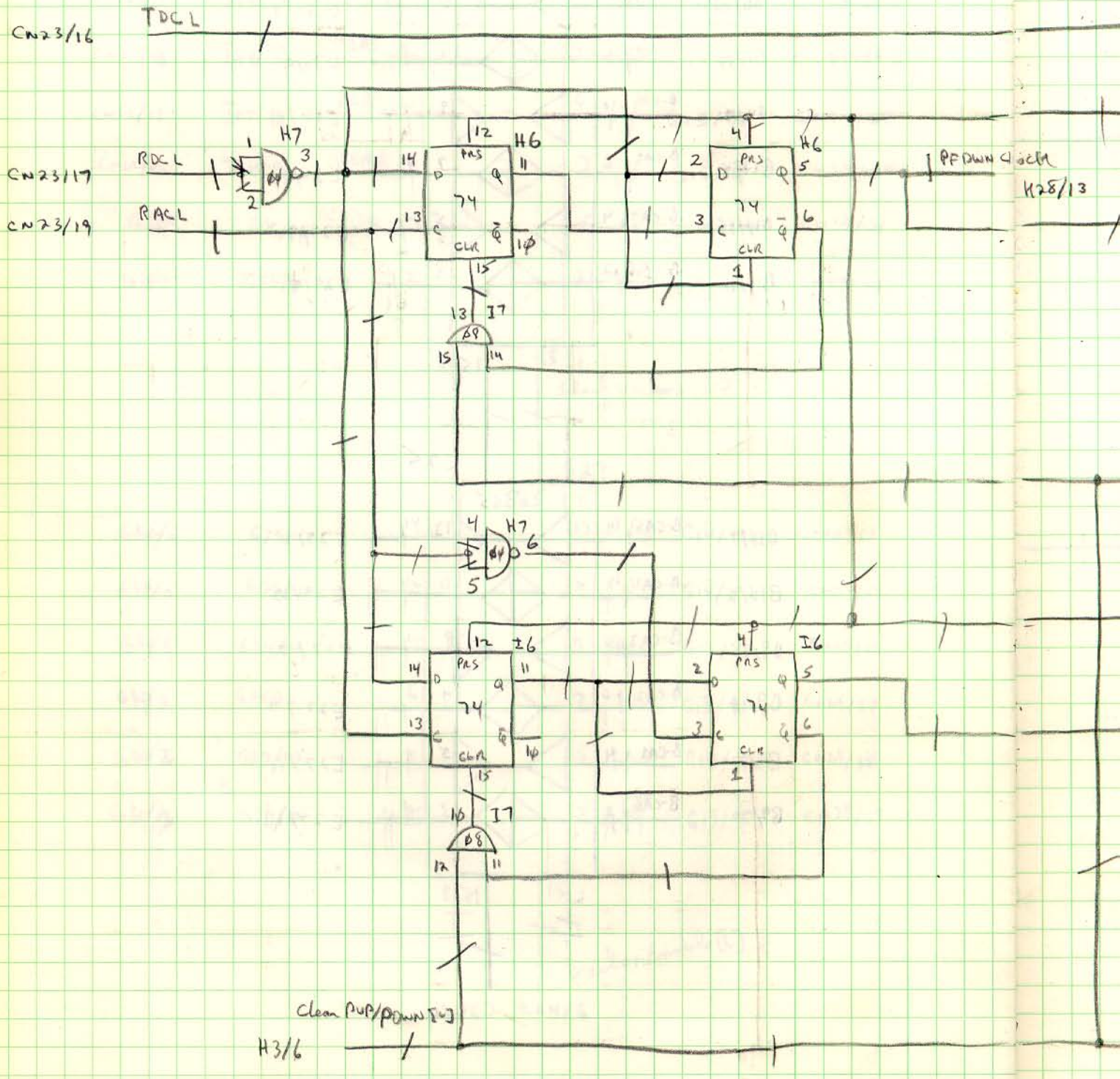
ABB

Power Fail Sequence Logic



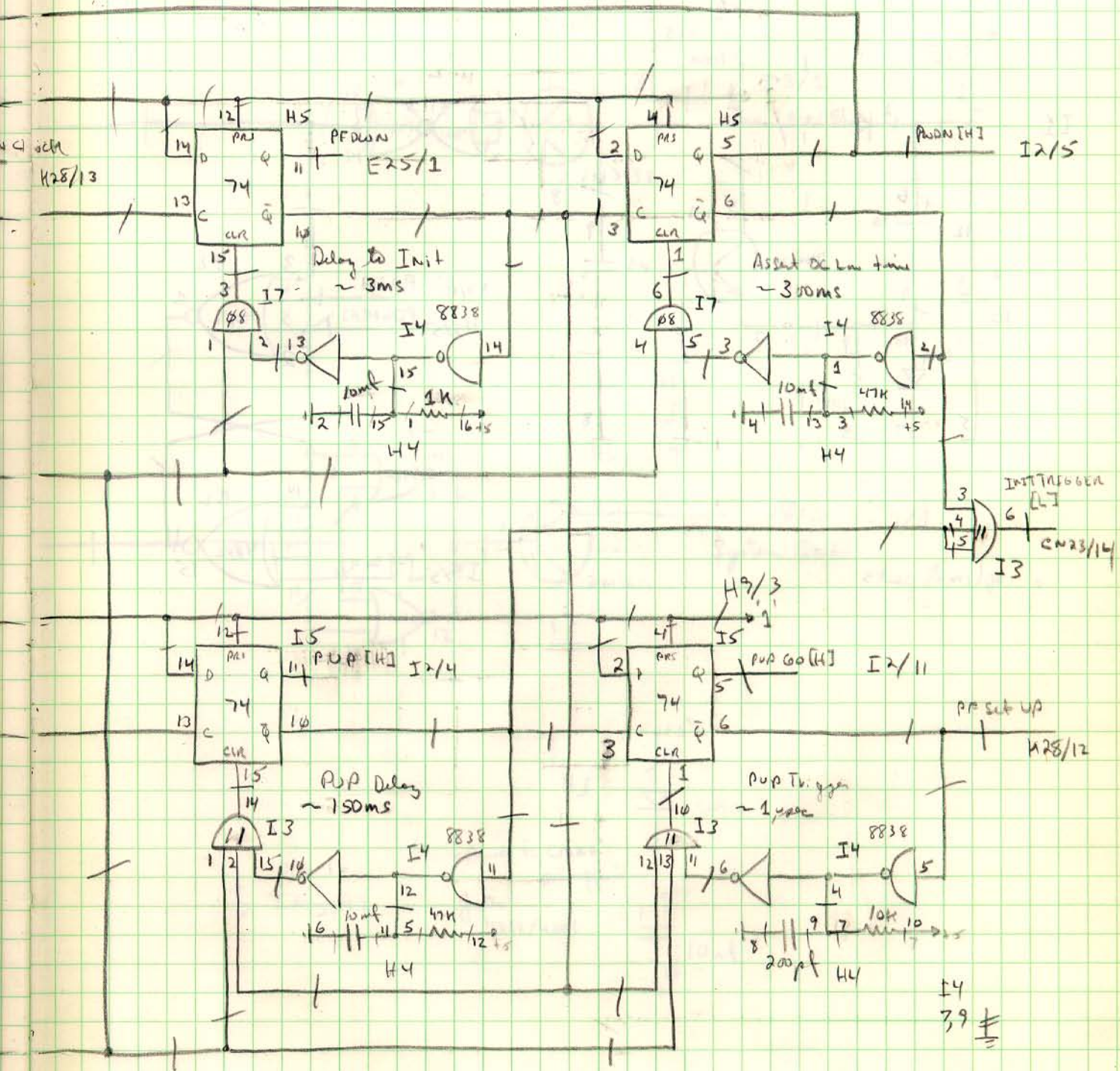

H5
PFDLON
E25/1
PWDN [H]
I2/5
Delay to Init
~ 3ms
Assert DC Low time
~ 350ms
8838
I4
I7
10mf
1K
47K
H4
INITTRIGGER [L]
CN23/14
I3
H3/3
I5
PUP [H]
I2/4
PUP GO [H]
I2/11
PF Set UP
H28/12
PUP Delay
~ 150ms
PUP Trigger
~ 1 μsec
200pf
10K
I4
7,9

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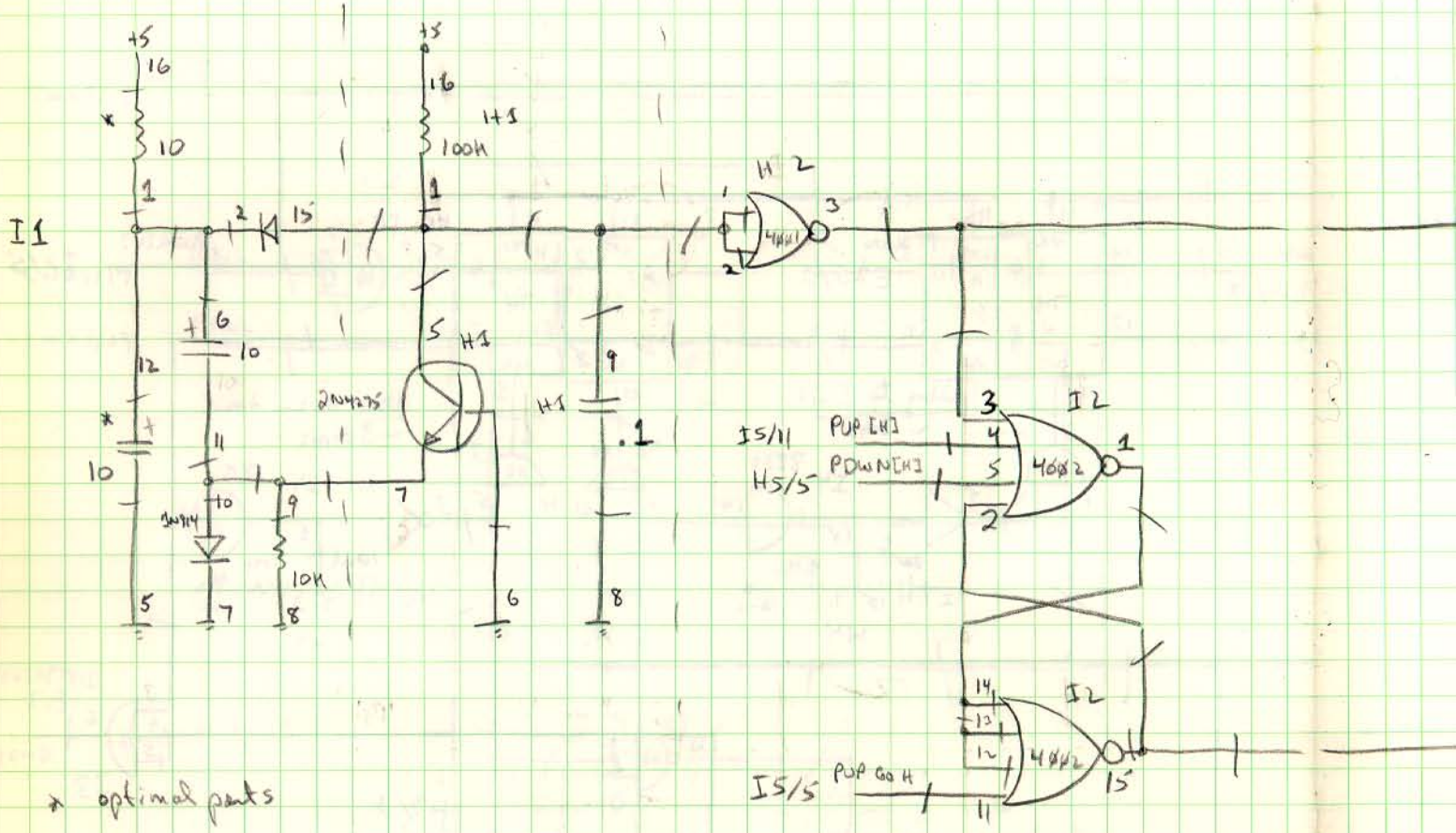
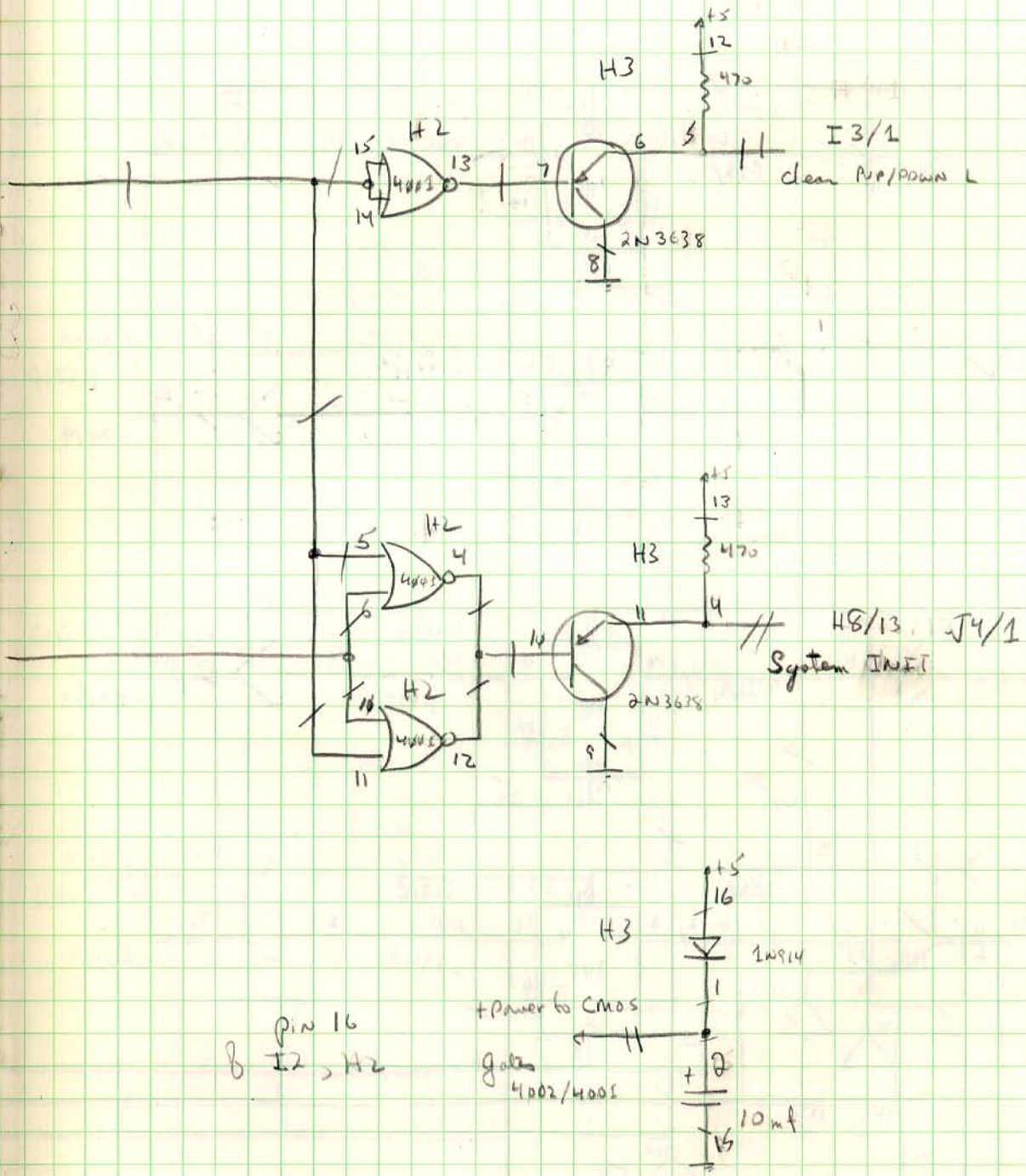
ABB

Power Fail Sequence Logic (Continued)



* optimal parts


+5
12
470
H3
H2
15
13
14
7
6
5
I3/1
clear PUP/PDWN L
2N3638
8
+5
13
H3
470
H2
5
4
6
11
4
H8/13. J4/1
System INIT
16
2N3638
9
H2
10
12
11
+5
16
H3
1N914
1
+Power to CMOS
gates
4002/4005
2
10 mf
8
PIN 16
8 I2, H2

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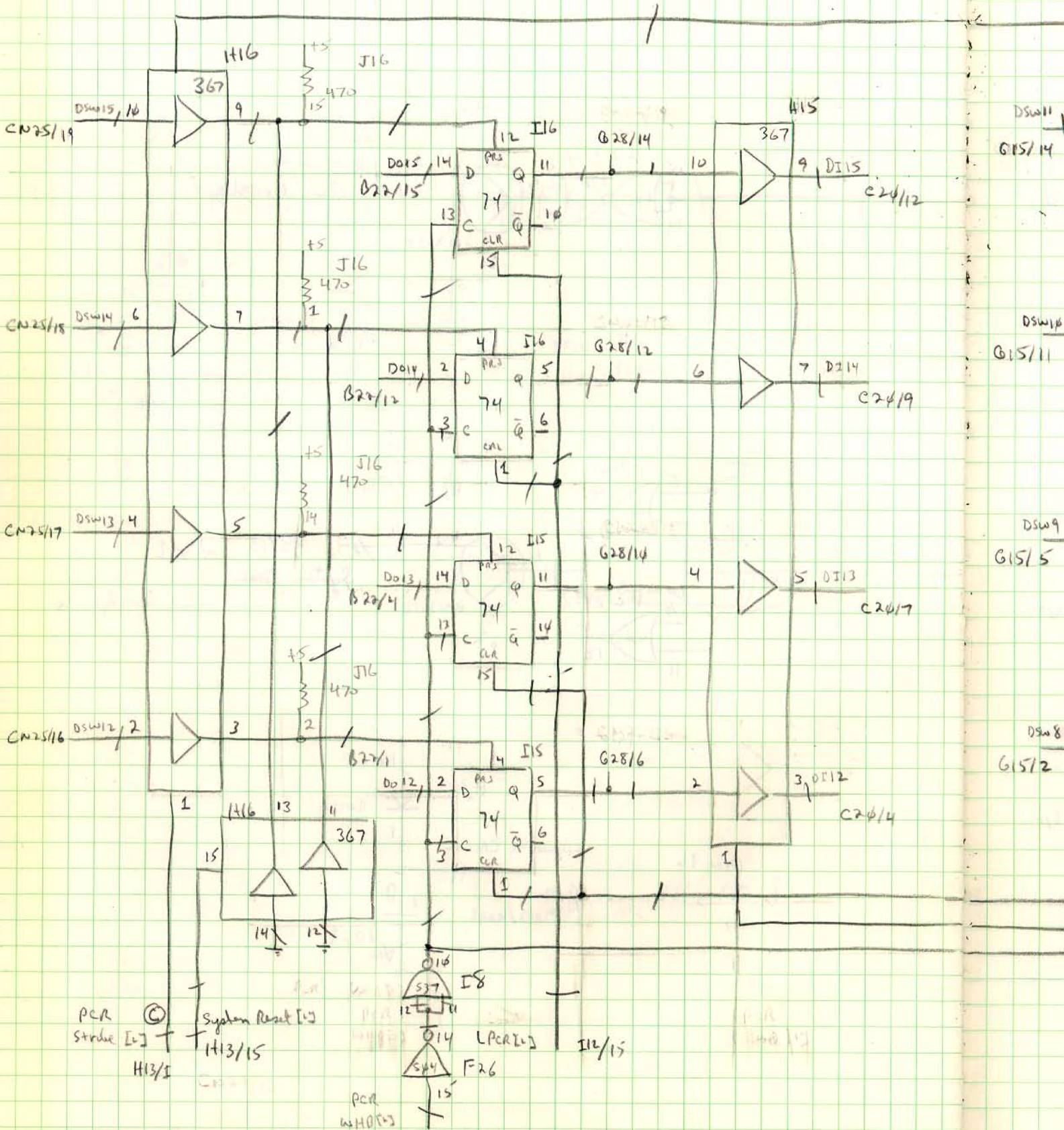
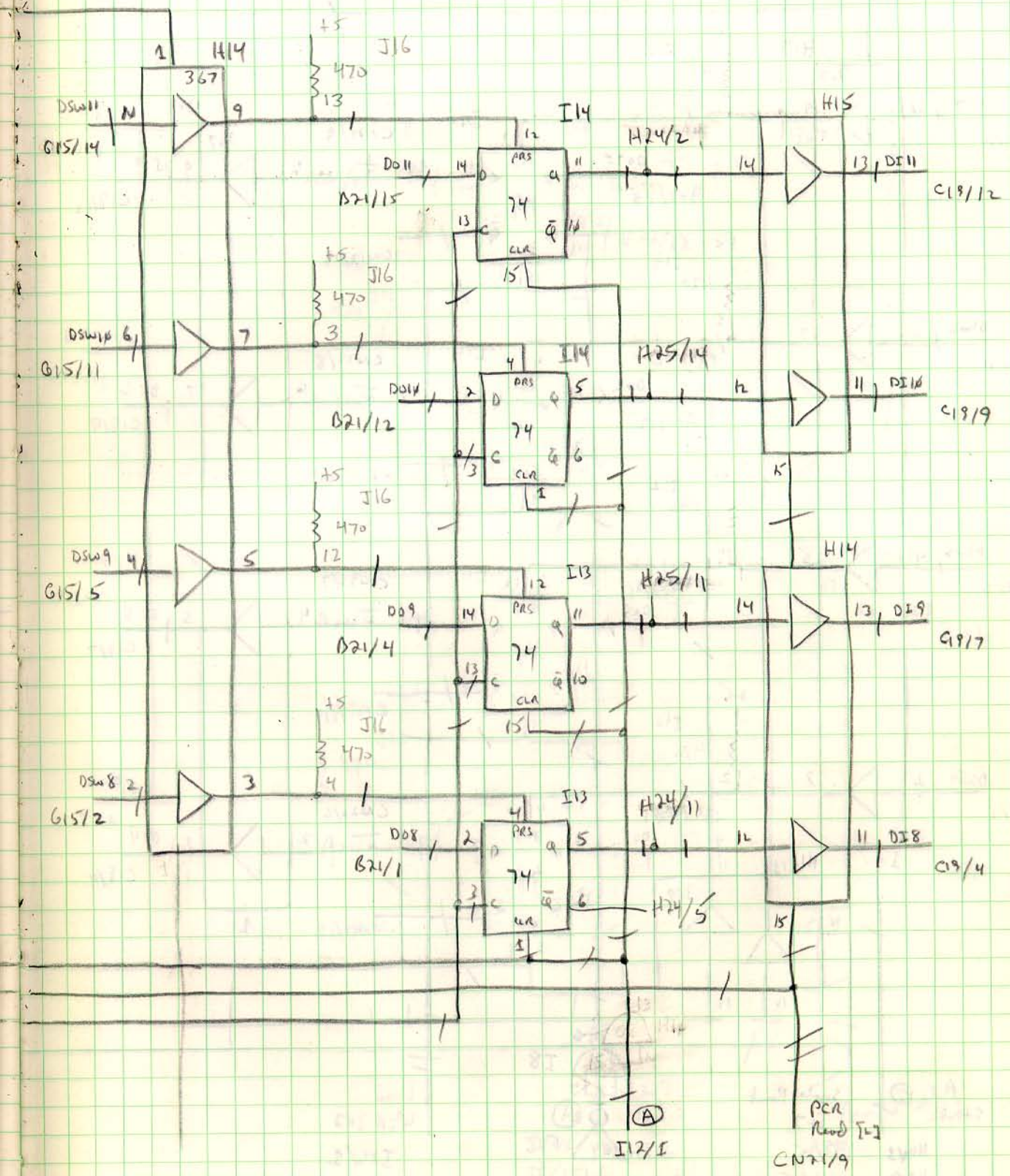
ABS

Processor Control Register




H14
367
J16
+5
470
DSW11
G15/14
I14
DO11
B21/15
H24/2
H15
DI11
C19/12
DSW10
G15/11
DO10
B21/12
H25/14
DI10
C19/9
DSW9
G15/5
I13
DO9
B21/4
H25/11
H14
DI9
C19/7
DSW8
G15/2
DO8
B21/1
H24/11
DI8
C19/4
H24/5
A
I12/I
PCR Read [L]
CN7 1/9
H12/1
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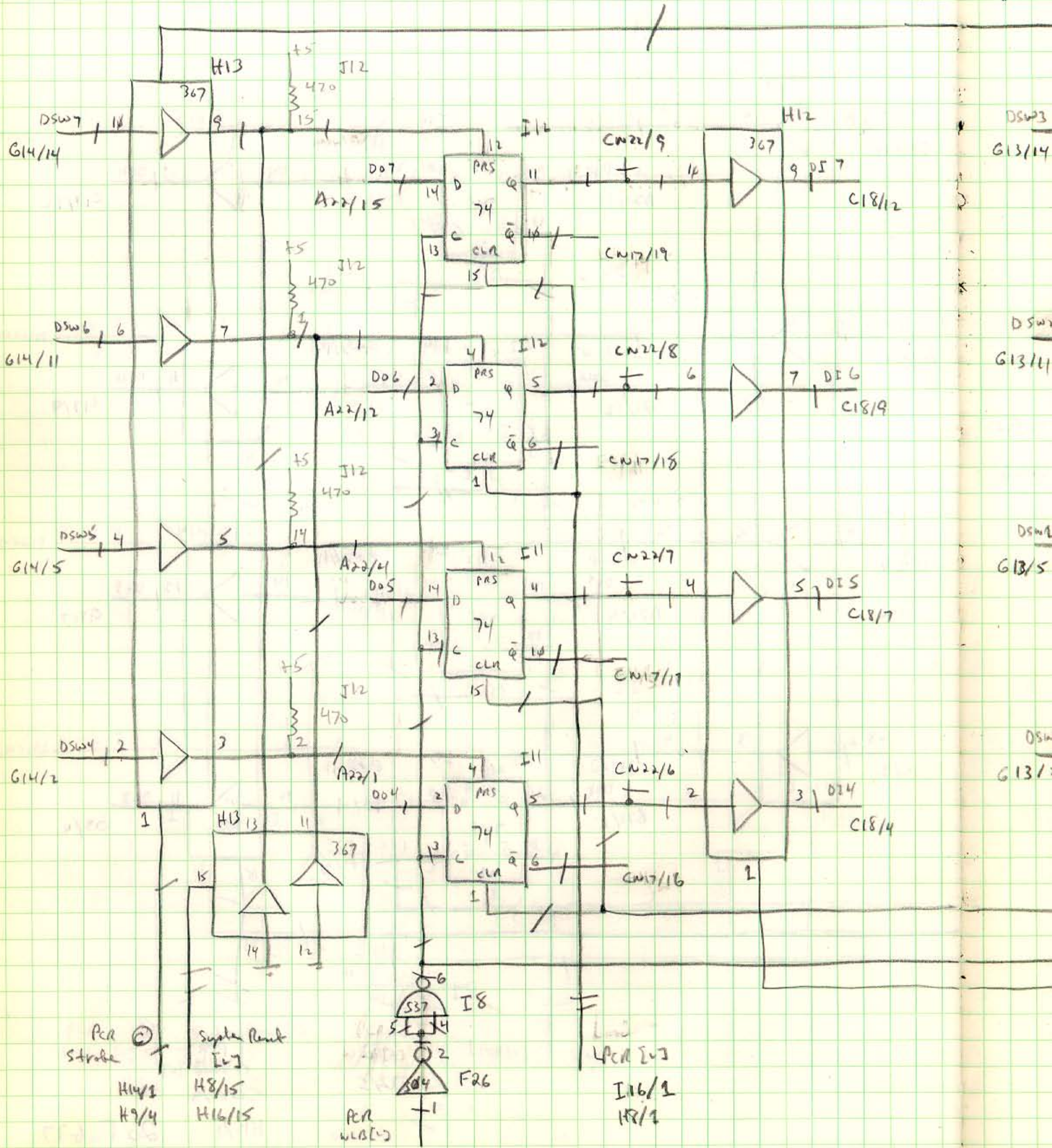
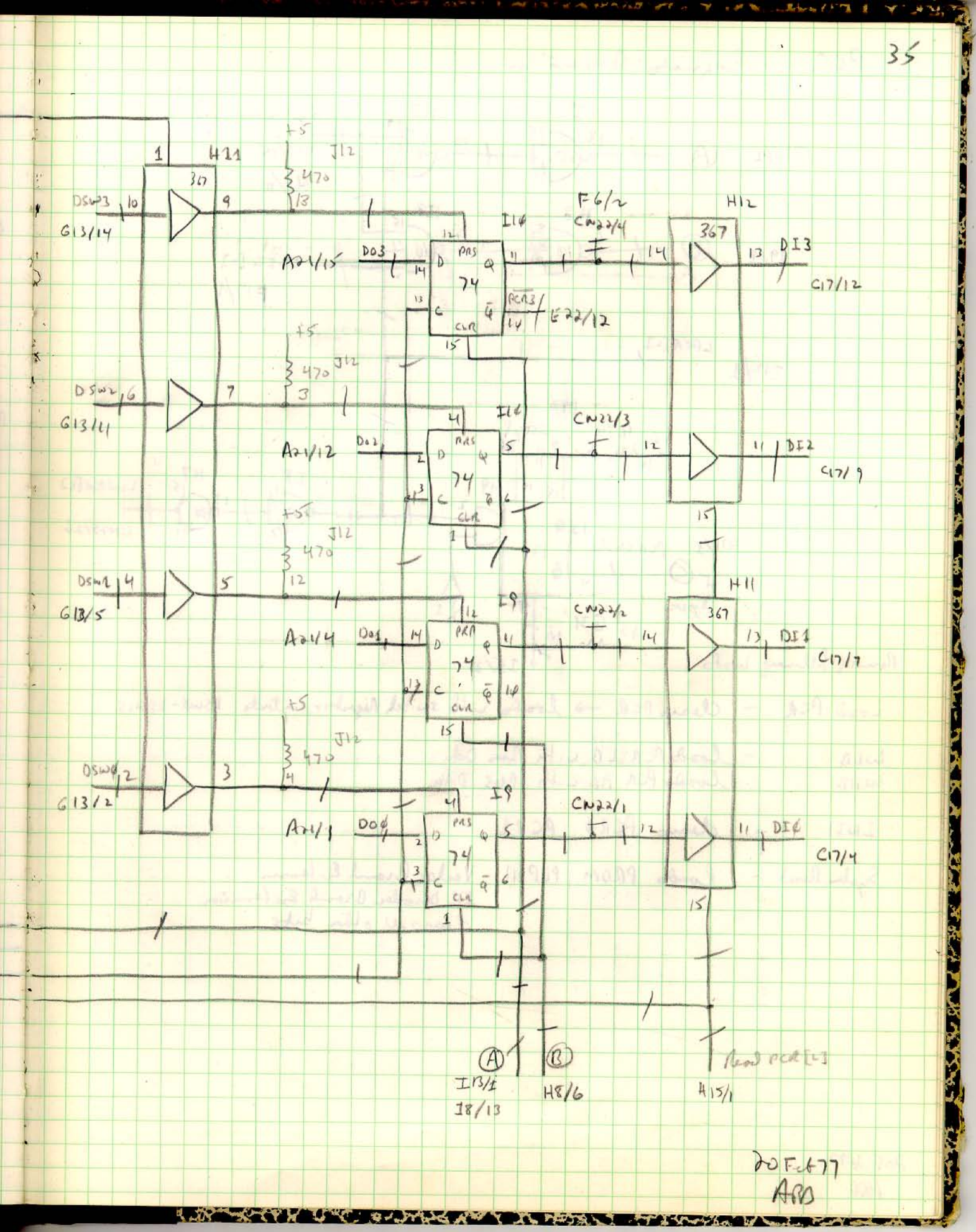
AB



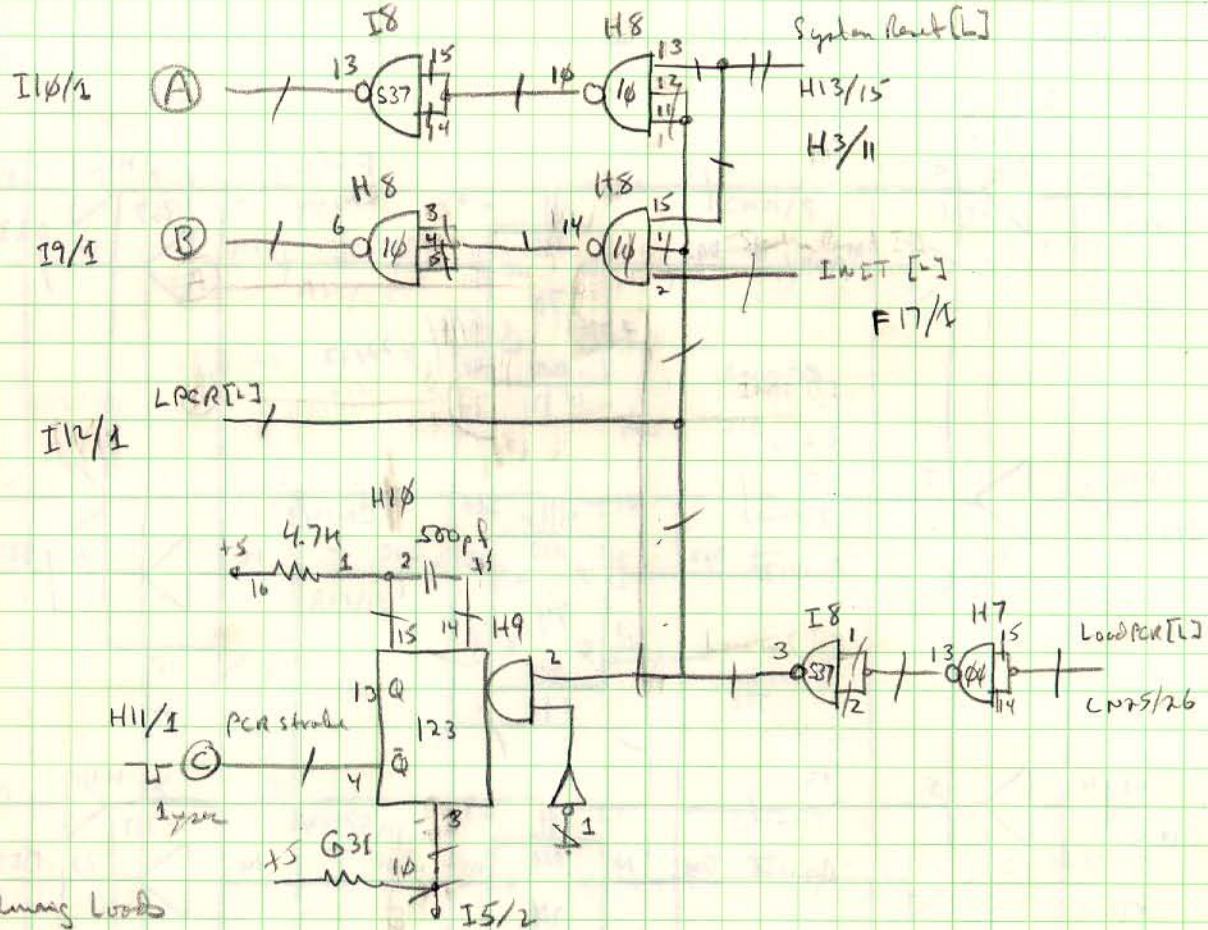
H13
367
J12
470
+5
DSW7
G14/14
DSW6
G14/11
DSW5
G14/5
DSW4
G14/2
I12
I11
74
PRS
CLR
D07
A22/15
D06
A22/12
D05
A22/4
D04
A22/1
CN22/9
CN22/8
CN22/7
CN22/6
CN17/19
CN17/18
CN17/17
CN17/16
H12
DI 7
DI 6
DI 5
DI 4
C18/12
C18/9
C18/7
C18/4
DSW3
G13/14
G13/11
G13/5
I8
F26
PCR Strobe
System Reset [L]
H14/1
H9/4
H8/15
H16/15
PCR WLB[L]
LPCR [L]
I16/1
H8/1


H11
367
DSW3
G13/14
DSW2
G13/11
DSW1
G13/5
DSW0
G13/2
+5
J12
470
DO3
DO2
DO1
DO0
A21/15
A21/12
A21/4
A21/1
I14
I16
I9
I8
74
PRS
CLR
F6/2
CN22/4
CN22/3
CN22/2
CN22/1
H12
H11
DI3
DI2
DI1
DI0
C17/12
C17/9
C17/7
C17/4
E22/12
I13/1
I8/13
H8/6
H15/1
Read PCA[-]

20 F 477

ABD

PCR Signals Generation



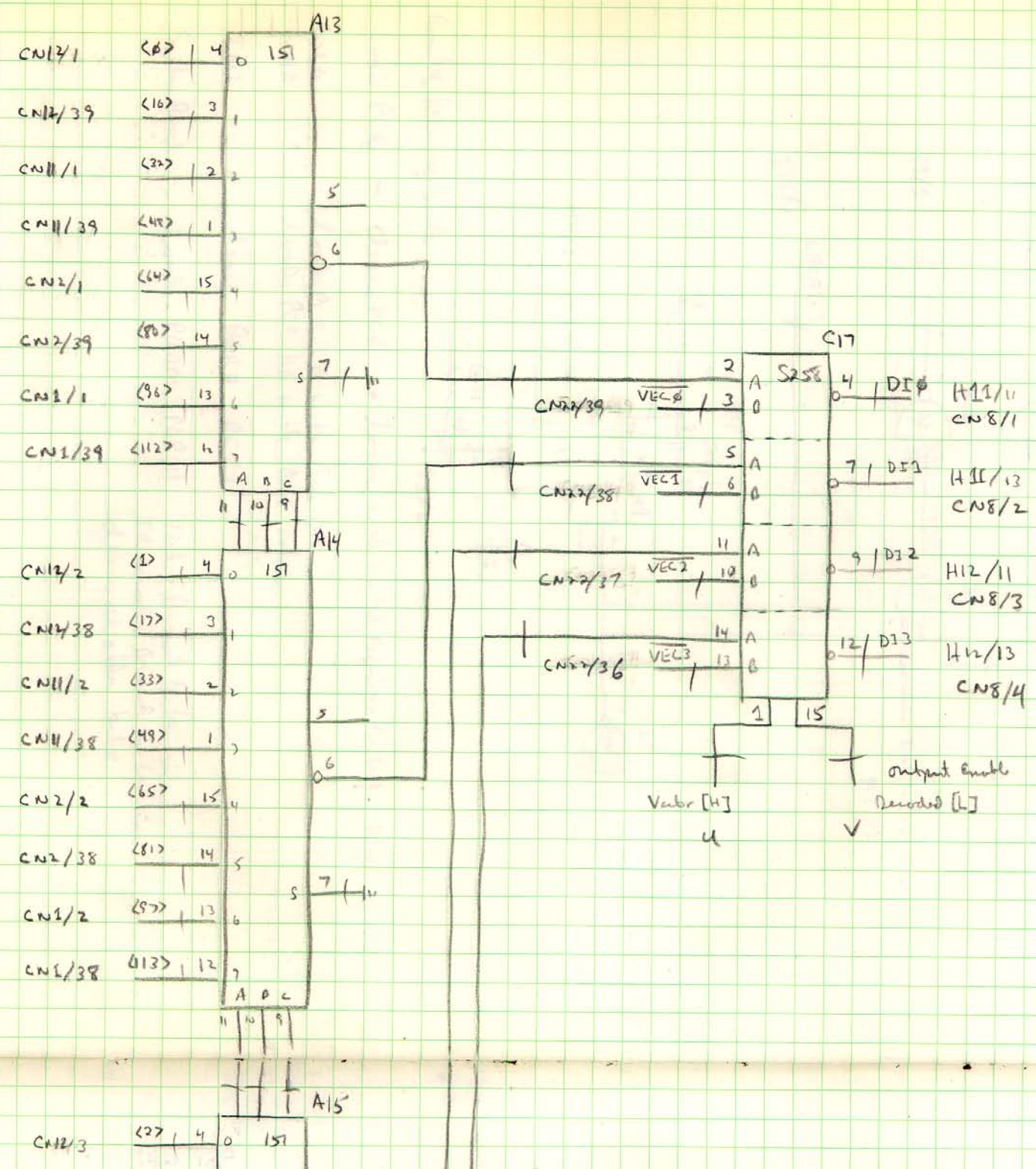
Results following Loads

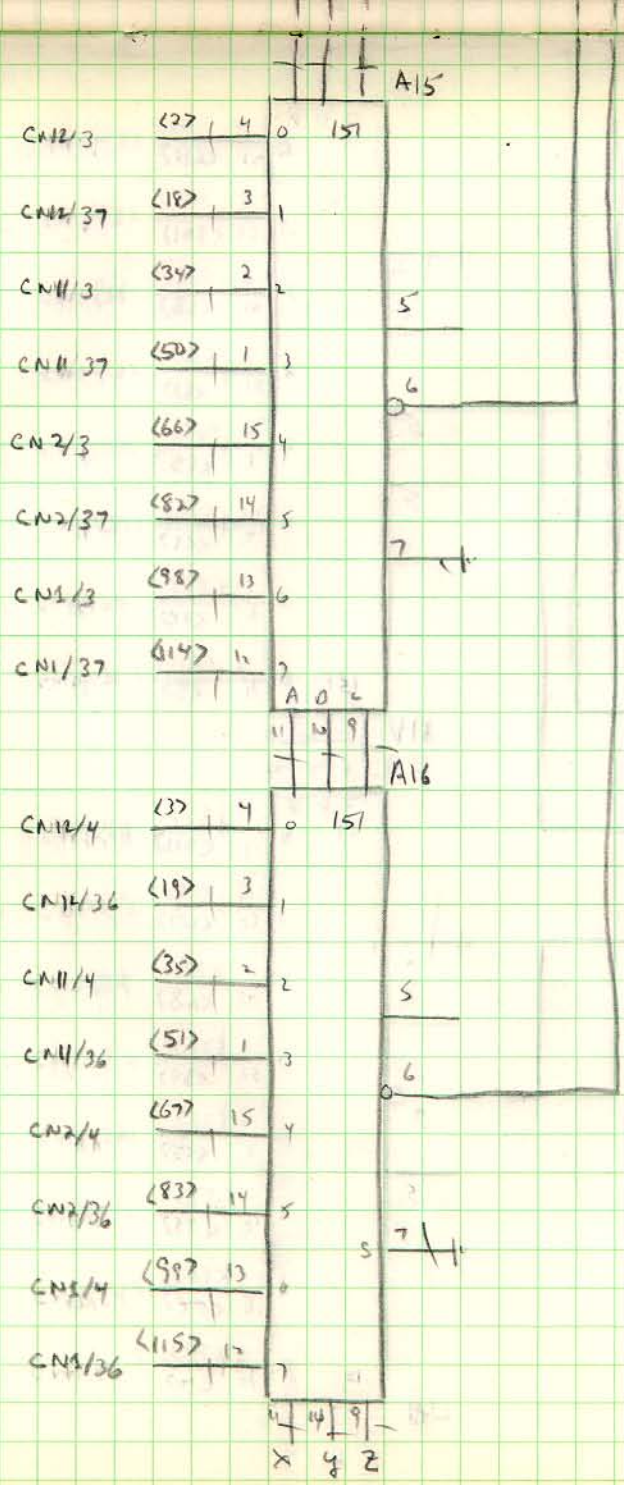
Load PCR – clears PCR → loads with switch Register Contents DSW0 - DSW15

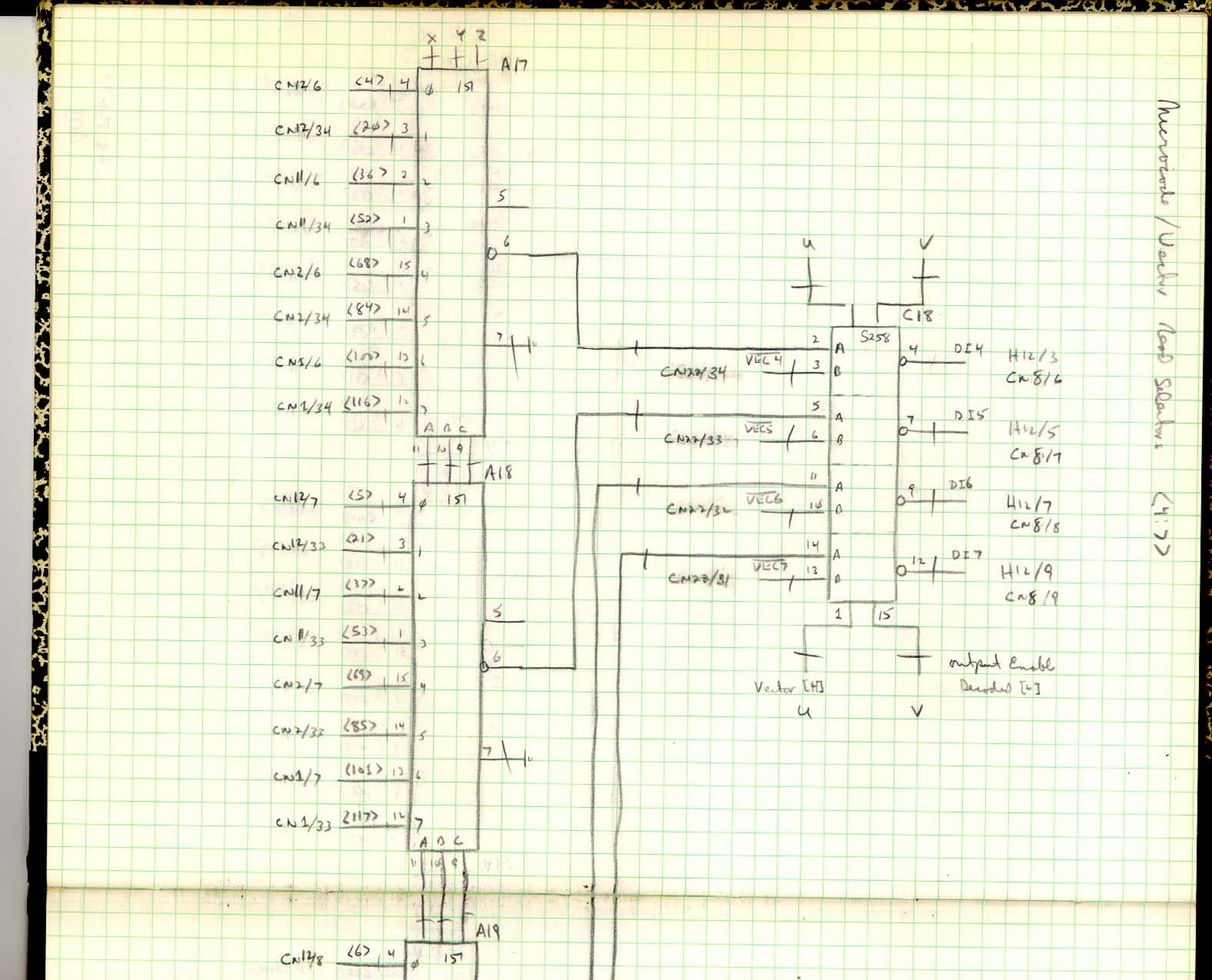
WLB – loads PCR LB with Bus Data
WHB loads PCR HB with Bus Data

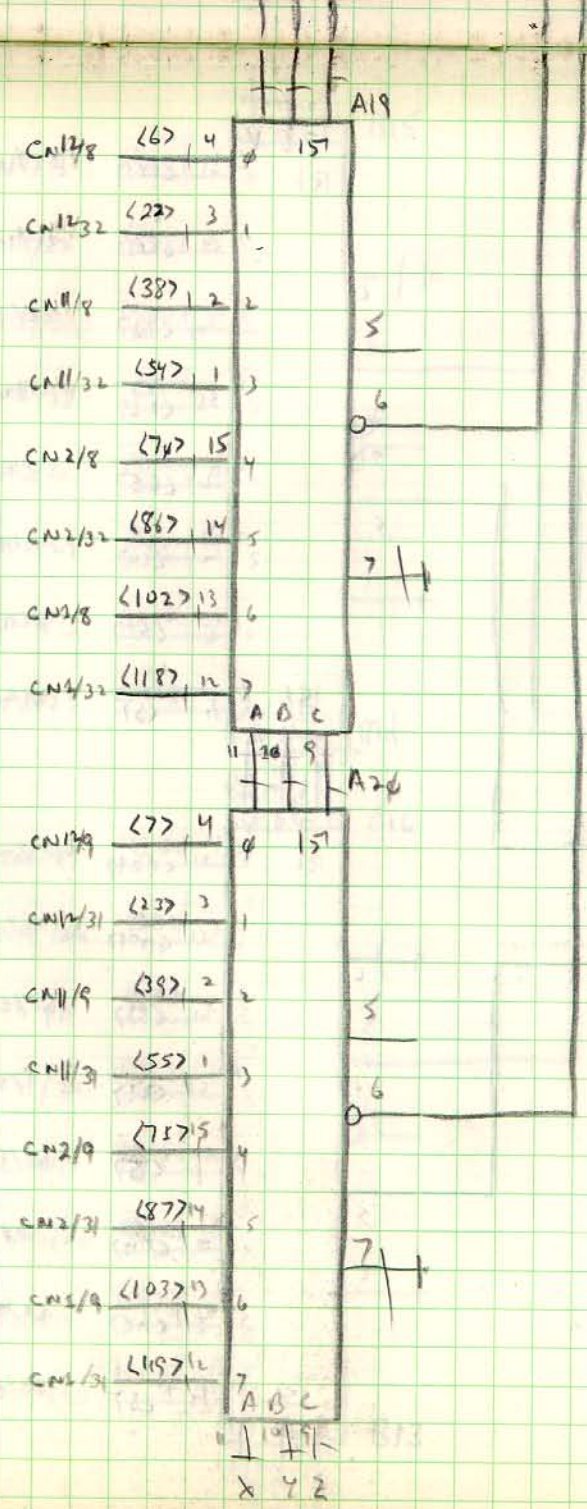
INIT – clears PCR0, PCR1

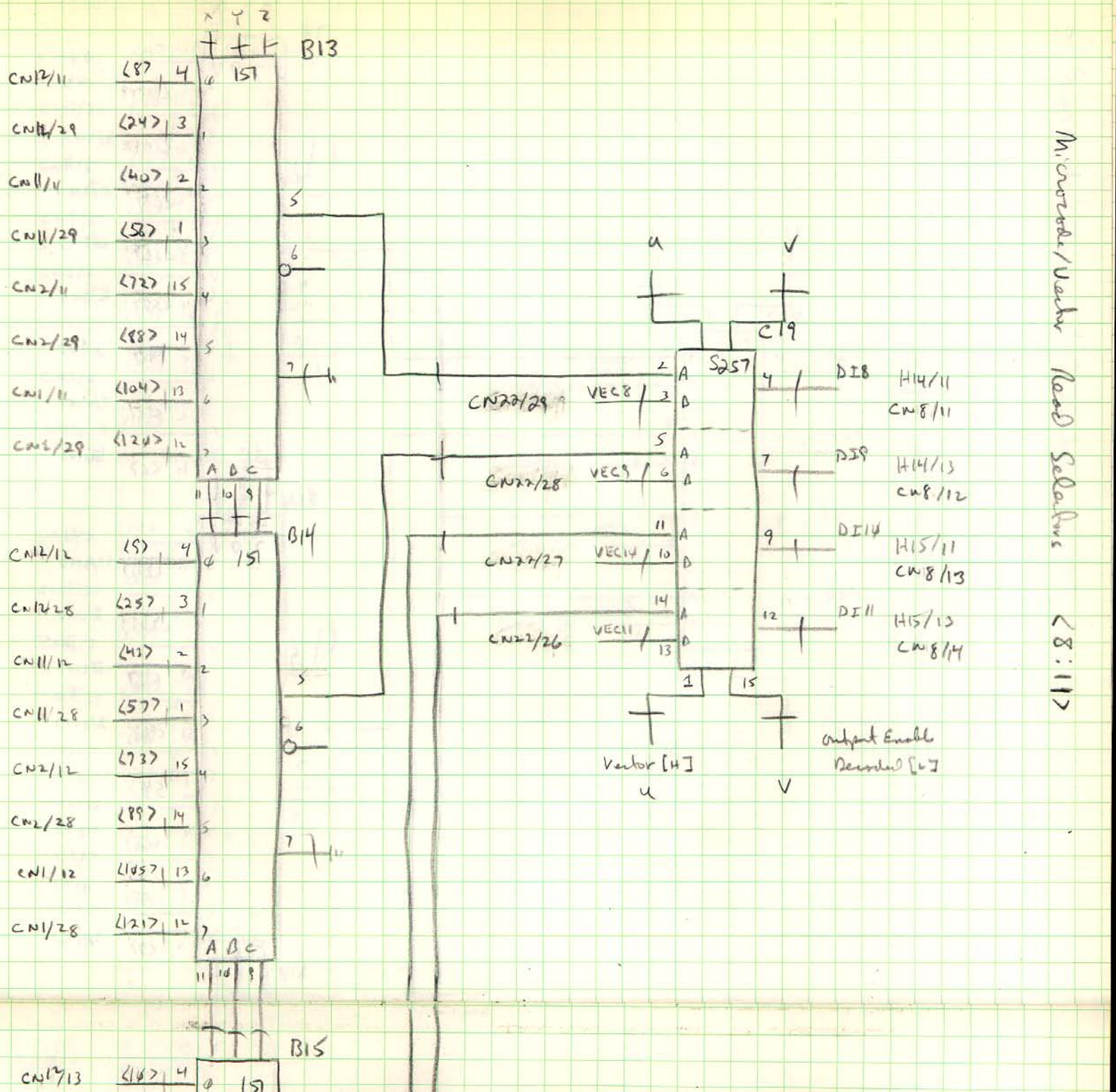
System Reset – loads PROM PDP-11 Vector Branch Extension
IR Decoder Branch Extension
clears all other bits

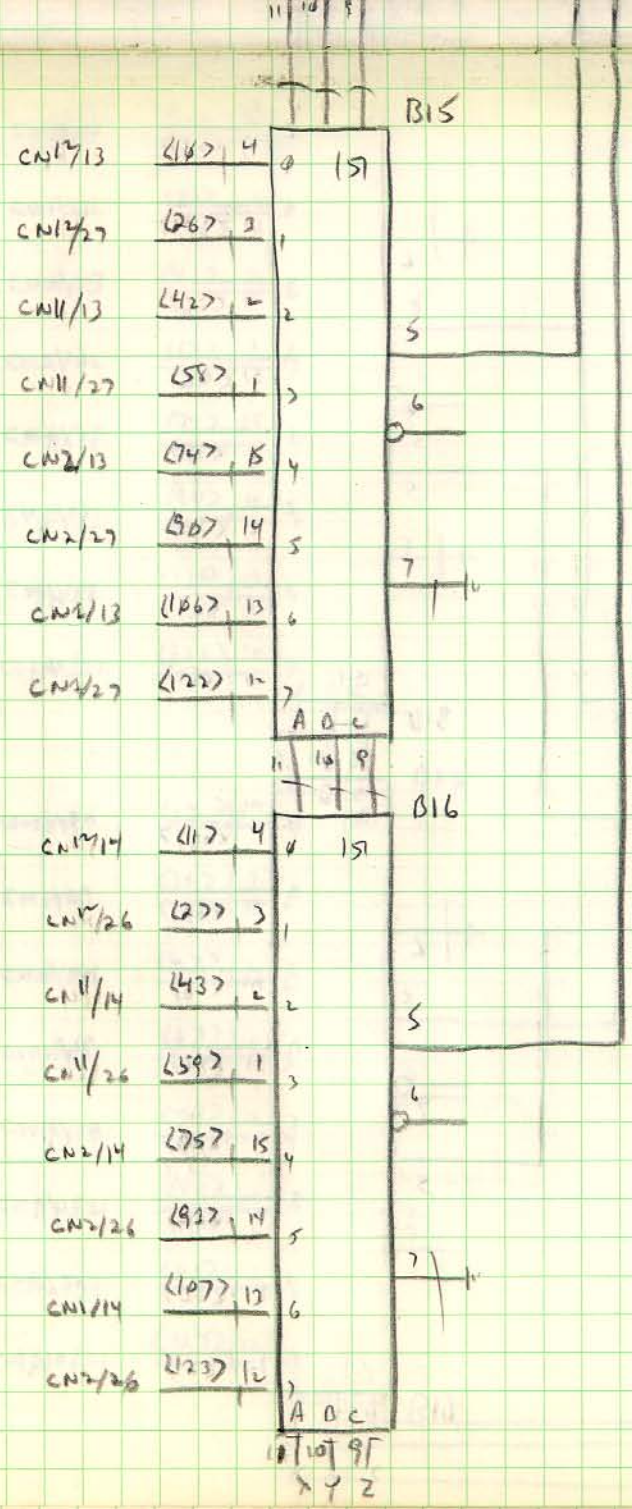

A13
A14
A15
C17
S256
CN12/1
CN12/39
CN11/1
CN11/39
CN2/1
CN2/39
CN1/1
CN1/39
CN12/2
CN12/38
CN11/2
CN11/38
CN2/2
CN2/38
CN1/2
CN1/38
CN12/3
CN22/39
CN22/38
CN22/37
CN22/36
VEC0
VEC1
VEC2
VEC3
DI0
DI1
DI2
DI3
H11/11
CN8/1
H11/13
CN8/2
H12/11
CN8/3
H12/13
CN8/4
Vector [H]
output Enable
Decoded [L]
M. controls / Vector Read Selectors <0:3>

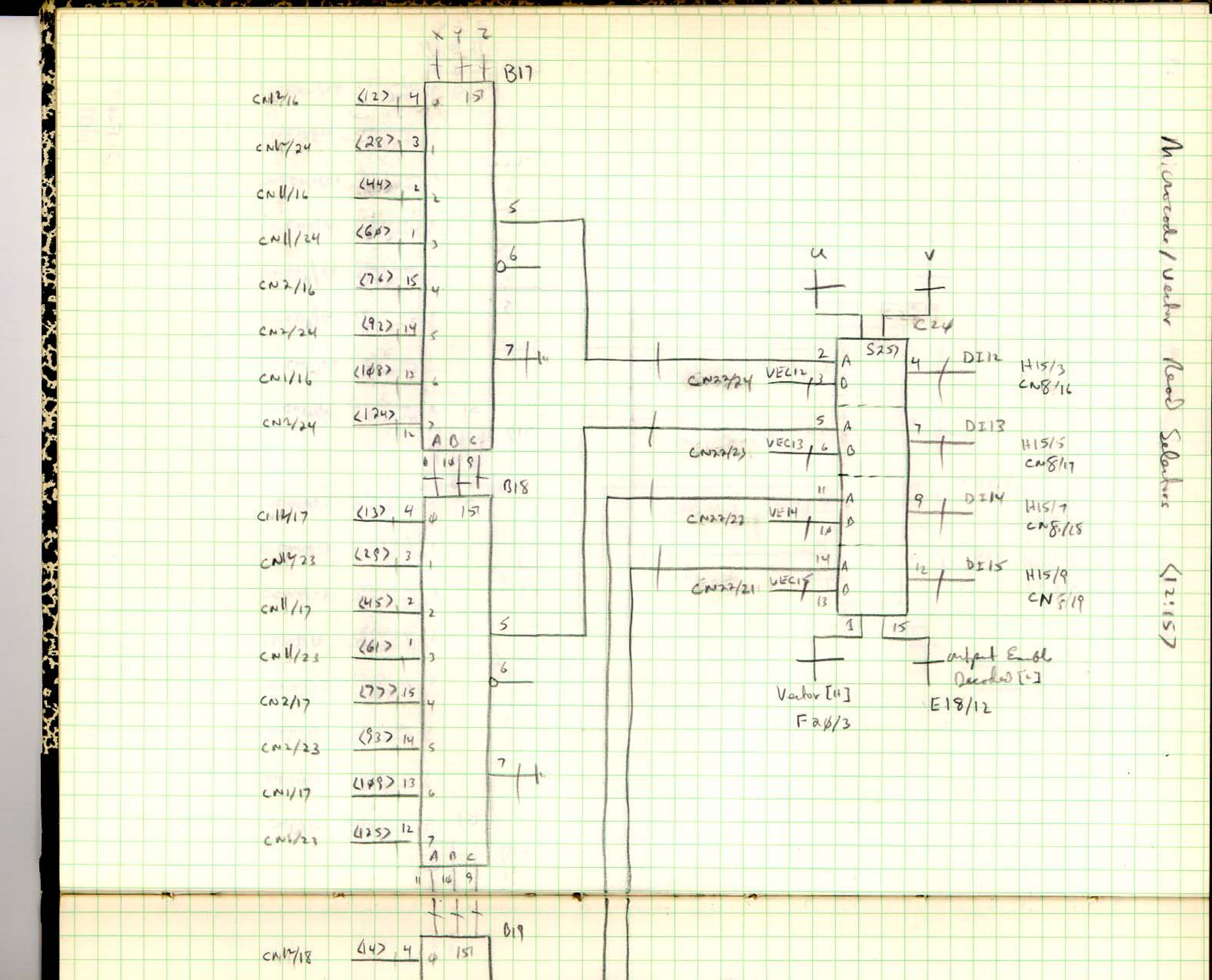

A15
CN12/3
CN2/37
CN11/3
CN1 37
CN2/3
CN2/37
CN1/3
CN1/37
A16
CN12/4
CN12/36
CN11/4
CN1/36
CN2/4
CN2/36
CN1/4
CN1/36
X
Y
Z

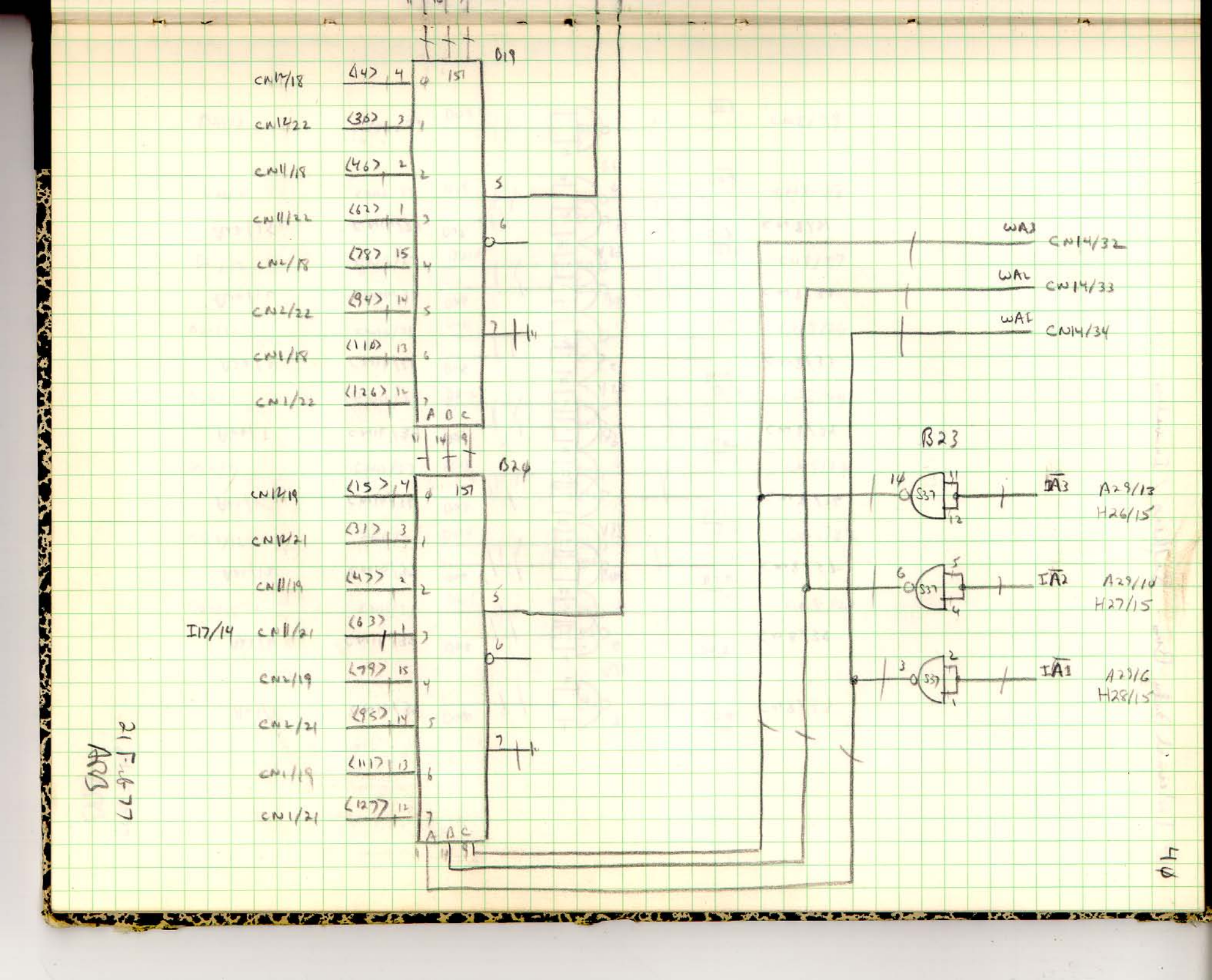

Memorandum / Vector Load Selectors <4:7>
X
Y
Z
A17
CN12/6
<47>
4
CN12/34
<20>
3
CN11/6
<36>
2
CN11/34
<52>
1
CN2/6
<68>
15
CN2/34
<84>
14
CN1/6
<100>
13
CN1/34
<116>
12
A B C
A18
CN12/7
<5>
4
CN12/33
<21>
3
CN11/7
<37>
2
CN11/33
<53>
1
CN2/7
<69>
15
CN2/33
<85>
14
CN1/7
<101>
13
CN1/33
<117>
12
A B C
A19
CN12/8
<6>
4
U
V
C18
S258
VEC4
CN20/34
VEC5
CN22/33
VEC6
CN22/32
VEC7
CN22/31
DI4
H12/3
CN8/6
DI5
H12/5
CN8/7
DI6
H12/7
CN8/8
DI7
H12/9
CN8/9
Vector [H]
output Enable
Decoded [4]


A19
CN12/8
CN12/32
CN11/8
CN11/32
CN2/8
CN2/32
CN1/8
CN1/32
A B C
A20
CN12/9
CN12/31
CN11/9
CN11/31
CN2/9
CN2/31
CN1/9
CN1/31
A B C
X Y Z

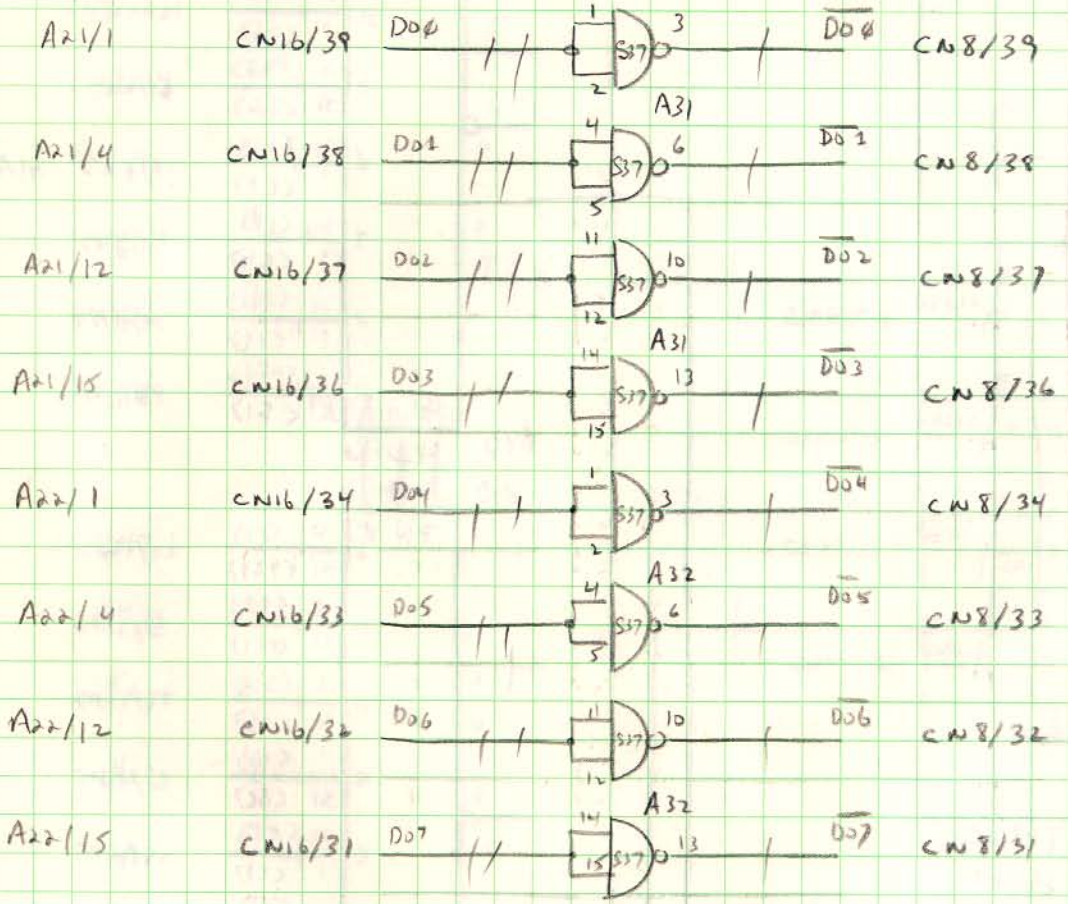

Microcontroller Vector Selection <8:11>
X Y Z
B13
CN12/11 <87> 4
CN11/29 <24> 3
CN11/11 <40> 2
CN11/29 <58> 1
CN2/11 <72> 15
CN2/29 <88> 14
CN1/11 <104> 13
CN1/29 <120> 12
A B C
B14
CN12/12 <9> 4
CN12/28 <25> 3
CN11/12 <41> 2
CN11/28 <57> 1
CN2/12 <73> 15
CN2/28 <89> 14
CN1/12 <105> 13
CN1/28 <121> 12
B15
CN12/13 <10> 4
U
V
C19
S257
CN22/29 VEC8 3
CN22/28 VEC9 6
CN22/27 VEC10 10
CN22/26 VEC11 13
DI8 H14/11 CN8/11
DI9 H14/13 CN8/12
DI10 H15/11 CN8/13
DI11 H15/13 CN8/14
Vector [H]
Output Enable Decoded [L]

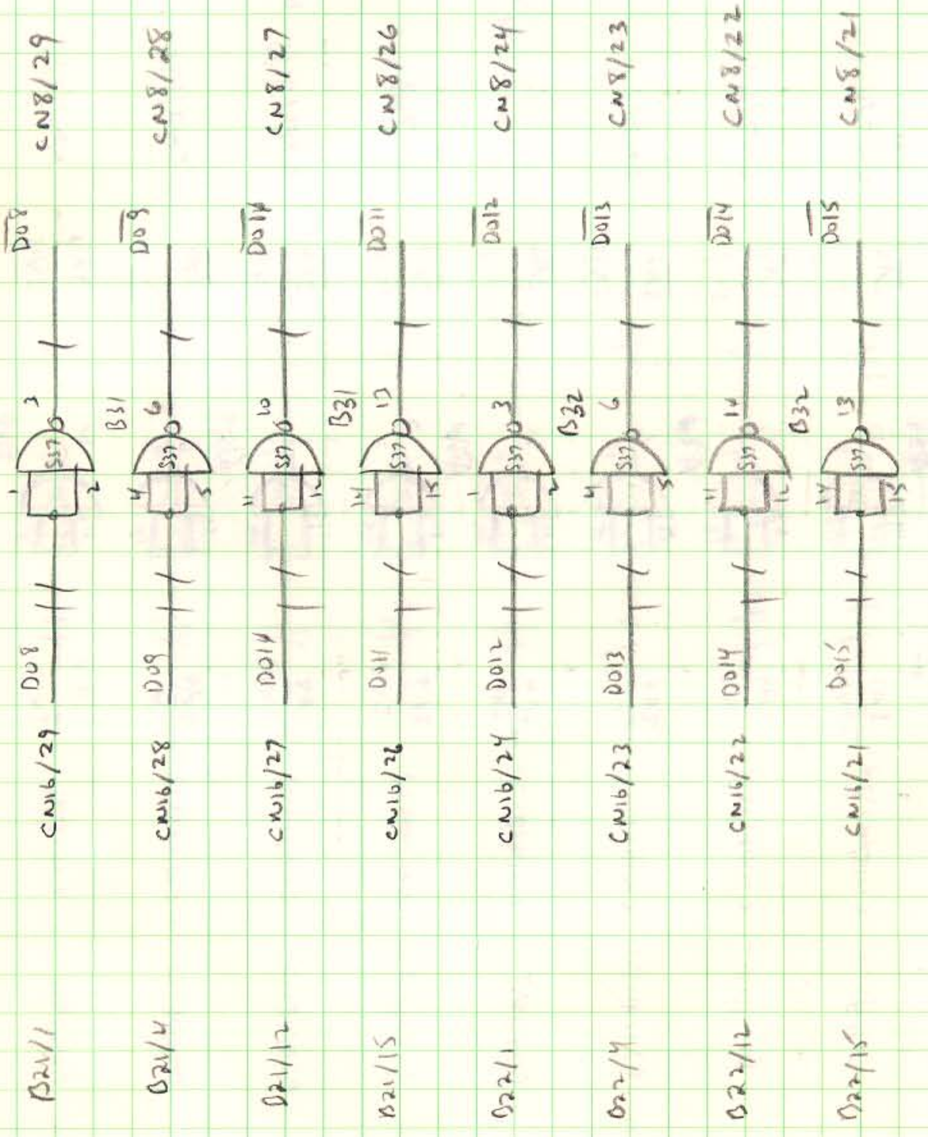

B15
CN12/13
CN12/27
CN11/13
CN11/27
CN2/13
CN2/27
CN1/13
CN1/27
B16
CN12/14
CN12/26
CN11/14
CN11/26
CN2/14
CN2/26
CN1/14
CN1/26
A B C
X Y Z


Microcode / Vector Load Selectors <12:15>
X Y Z
B17
CN2/16 <12> 4
CN2/24 <28> 3
CN1/16 <44> 2
CN1/24 <60> 1
CN2/16 <76> 15
CN2/24 <92> 14
CN1/16 <108> 13
CN1/24 <124> 12
A B C
B18
CN2/17 <13> 4
CN2/23 <29> 3
CN1/17 <45> 2
CN1/23 <61> 1
CN2/17 <77> 15
CN2/23 <93> 14
CN1/17 <109> 13
CN1/23 <125> 12
D19
CN2/18 <14> 4
U V
C24
S25J
CN27/24 VEC12
CN27/23 VEC13
CN27/22 VEC14
CN27/21 VEC15
DI12
DI13
DI14
DI15
H15/3 CN8/16
H15/5 CN8/17
H15/7 CN8/18
H15/9 CN5/19
Vector [4] F2B/3
output Enable Decoded [4]
E18/12


D19
CN17/18
CN12/22
CN11/18
CN11/22
CN2/18
CN2/22
CN1/18
CN1/22
B24
CN12/19
CN12/21
CN11/19
CN11/21
CN2/19
CN2/21
CN1/19
CN1/21
I17/14
WA3
CN14/32
WA2
CN14/33
WA1
CN14/34
B23
IA3
IA2
IA1
A29/13
H26/15
A29/14
H27/15
A29/16
H28/15

Internal Data Bus Buffers / Inverters





CN8/29
CN8/28
CN8/27
CN8/26
CN8/24
CN8/23
CN8/22
CN8/21
B31
B32
S37
CN16/29
CN16/28
CN16/27
CN16/26
CN16/24
CN16/23
CN16/22
CN16/21
B21/1
B21/4
B21/12
B21/15
B22/1
B22/4
B22/12
B22/15

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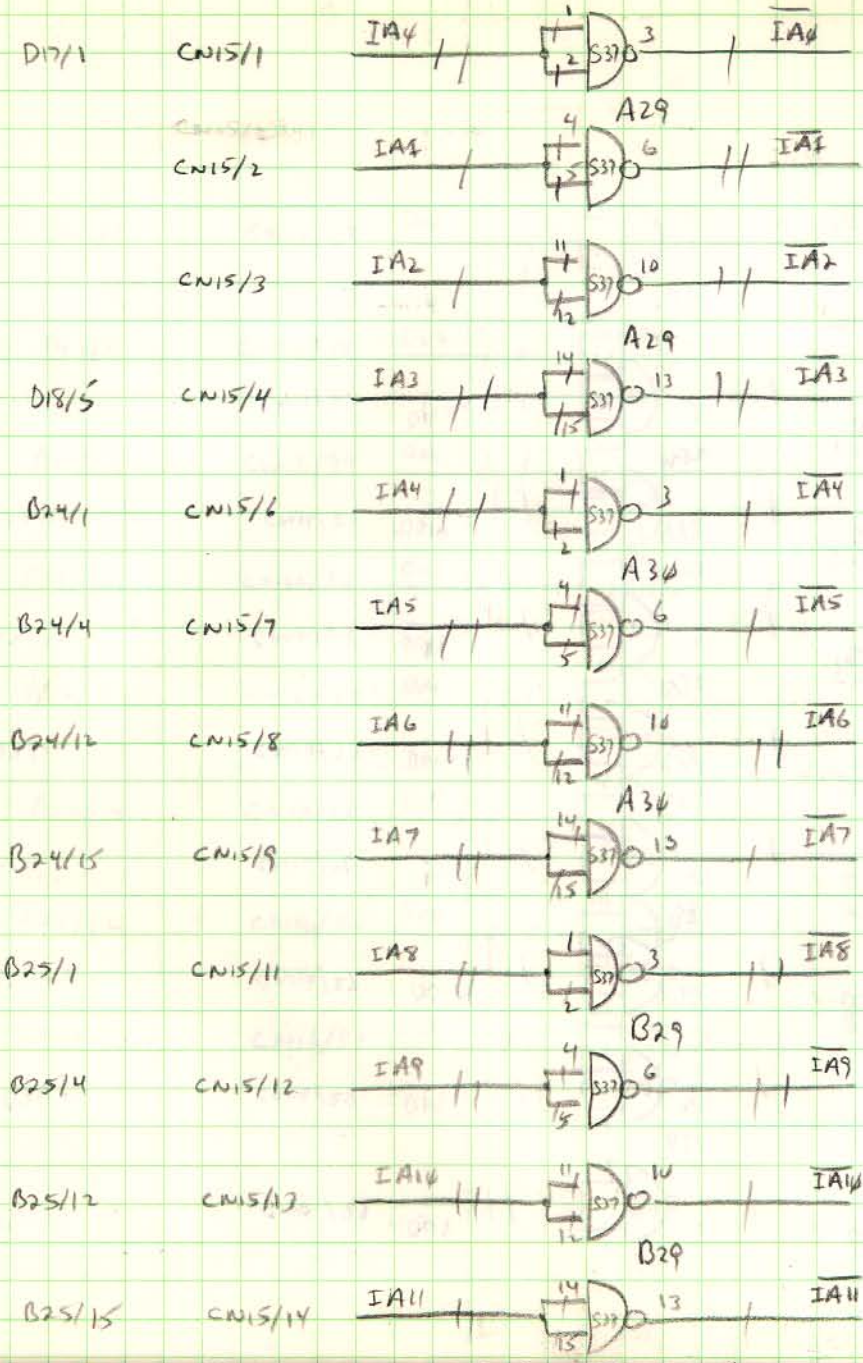
ARB

Inbound Address - Control Buffering - Inverting



D17/1	CN15/1	IA4	CN7/1	
	CN15/2	IA1	CN7/2	B23/2
	CN15/3	IA2	CN7/3	B23/5
D18/5	CN15/4	IA3	CN7/4	B23/11
B24/1	CN15/6	IA4	CN7/6	
B24/4	CN15/7	IA5	CN7/7	
B24/12	CN15/8	IA6	CN7/8	D23/14
B24/15	CN15/9	IA7	CN7/9	
B25/1	CN15/11	IA8	CN7/11	D22/12
B25/4	CN15/12	IA9	CN7/12	D21/11
B25/12	CN15/13	IA10	CN7/13	
B25/15	CN15/14	IA11	CN7/14	
B26/1	CN15/16	IA12	CN7/16	D21/6

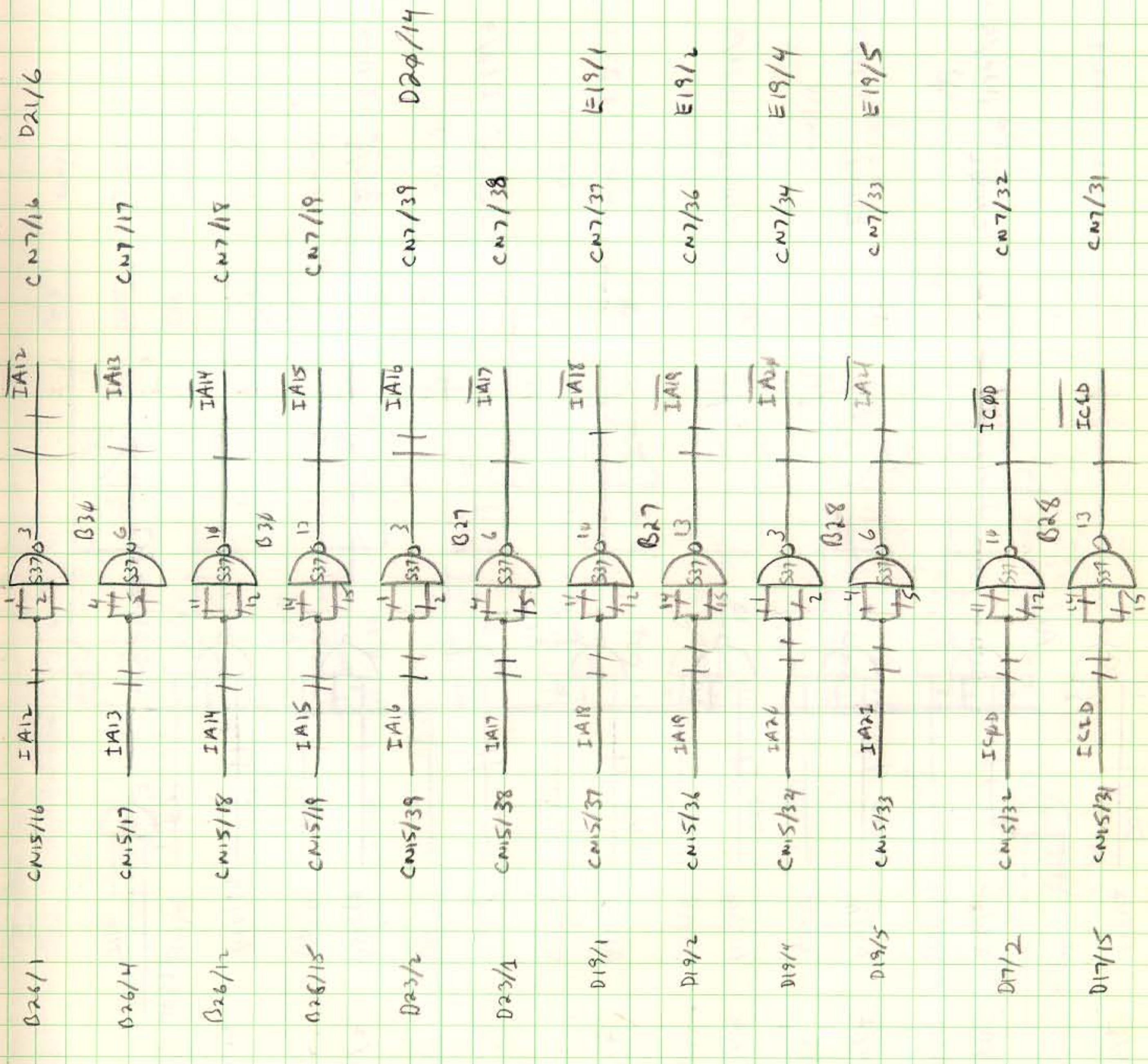

B26/1 CN15/16 IA12 S37 IA12 CN7/16 D21/6
B26/4 CN15/17 IA13 S37 B36 IA13 CN7/17
B26/12 CN15/18 IA14 S37 B36 IA14 CN7/18
B26/13 CN15/19 IA15 S37 IA15 CN7/19
D23/2 CN15/39 IA16 S37 IA16 CN7/39 D20/14
D23/1 CN15/38 IA17 S37 B27 IA17 CN7/38
D19/1 CN15/37 IA18 S37 IA18 CN7/37 E19/1
D19/2 CN15/36 IA19 S37 B27 IA19 CN7/36 E19/2
D19/4 CN15/34 IA20 S37 IA20 CN7/34 E19/4
D19/5 CN15/33 IA21 S37 B28 IA21 CN7/33 E19/5
D17/2 CN15/32 IC0D S37 B28 IC0D CN7/32
D17/15 CN15/31 IC1D S37 IC1D CN7/31

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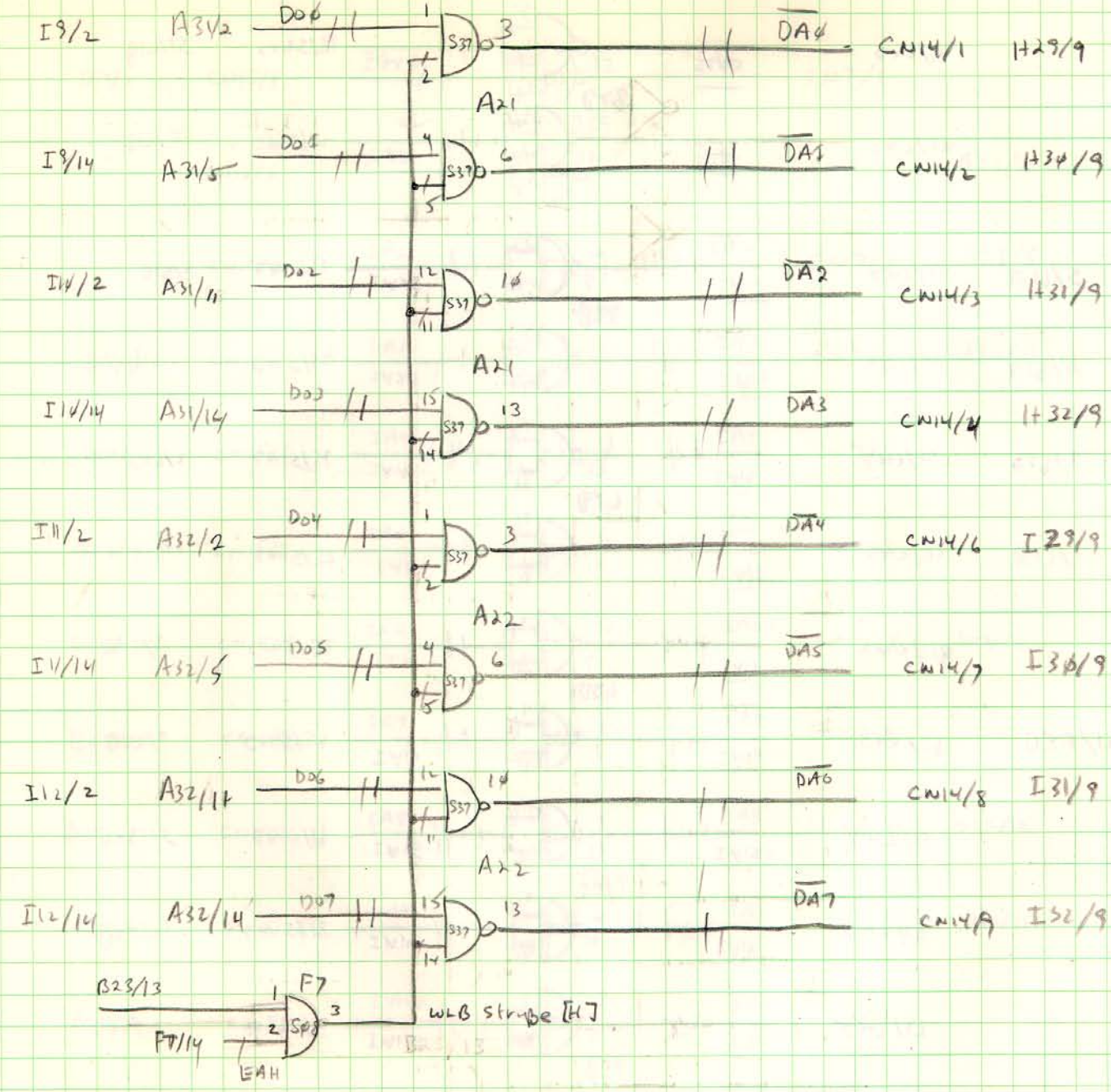
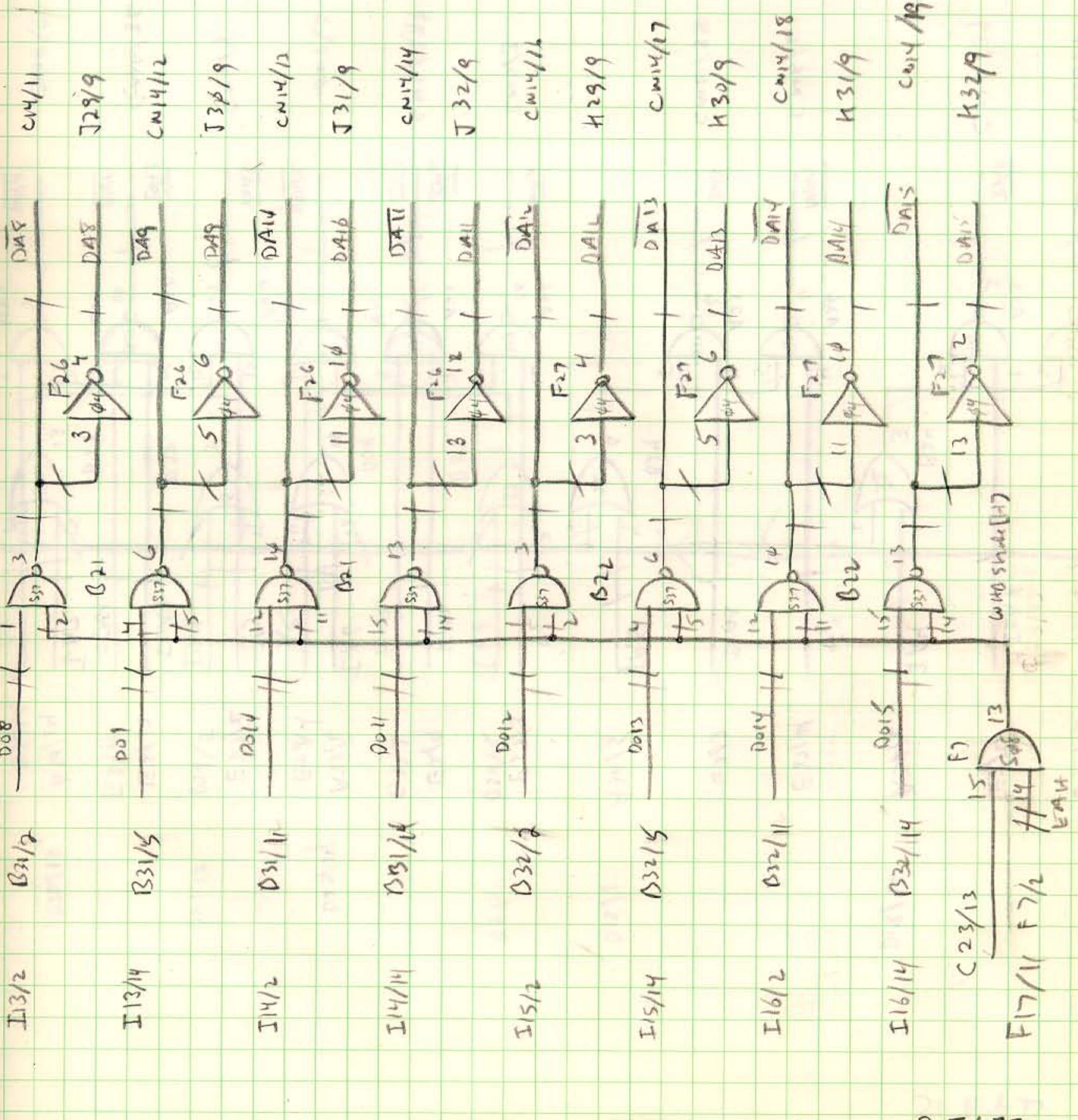
ABB



Microcode Write Data Amplifiers - Inverters


I13/2
I13/14
I14/2
I14/14
I15/2
I15/14
I16/2
I16/14
F17/11
C23/13
F7/2
B31/2
B31/5
B31/11
B31/14
B32/2
B32/5
B32/11
B32/14
CN14/11
J28/9
CN14/12
CN14/13
J31/9
CN14/14
J32/9
CN14/16
H29/9
CN14/17
H30/9
CN14/18
H31/9
H32/9
F26
F27
B21
B22

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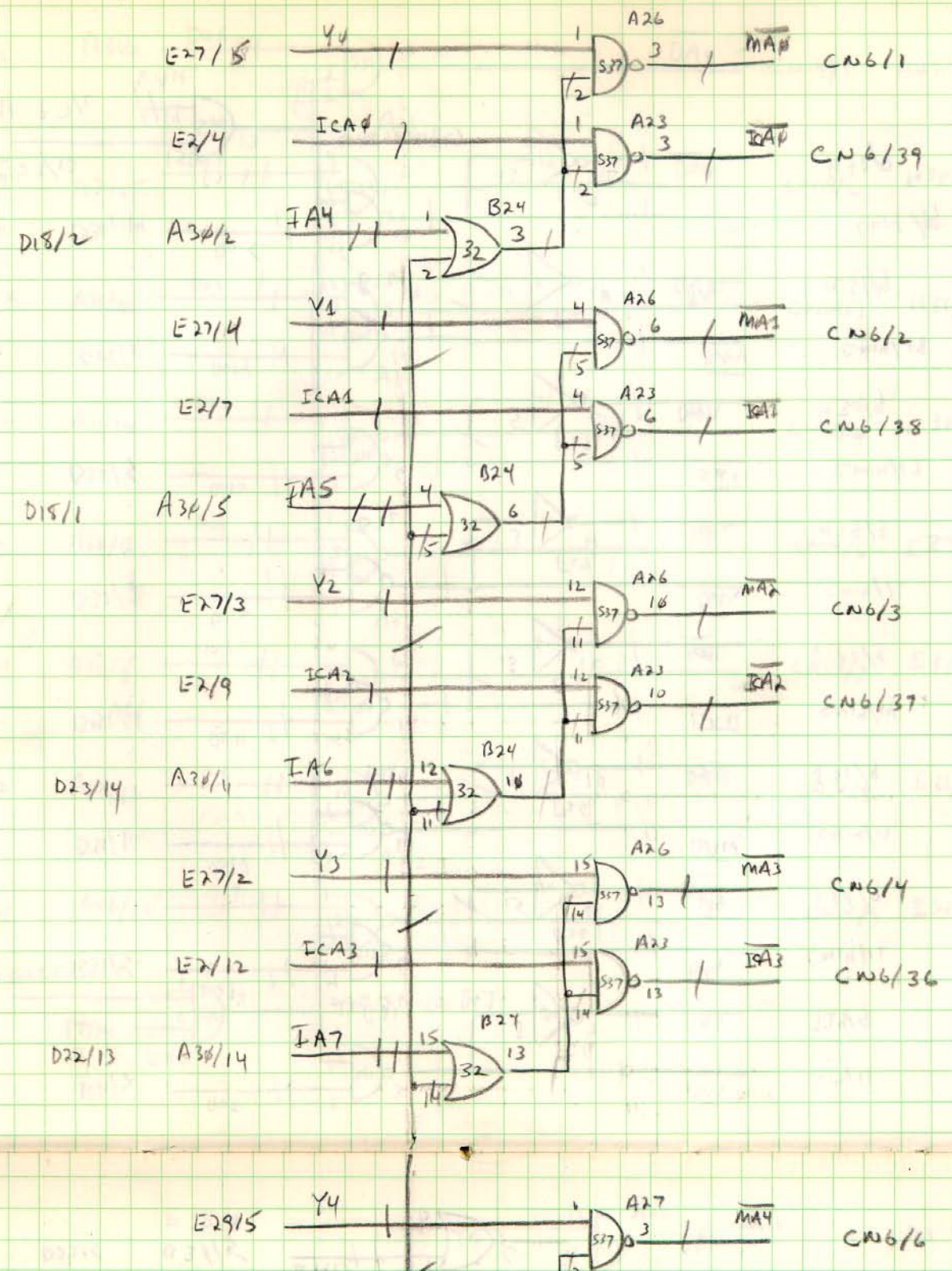
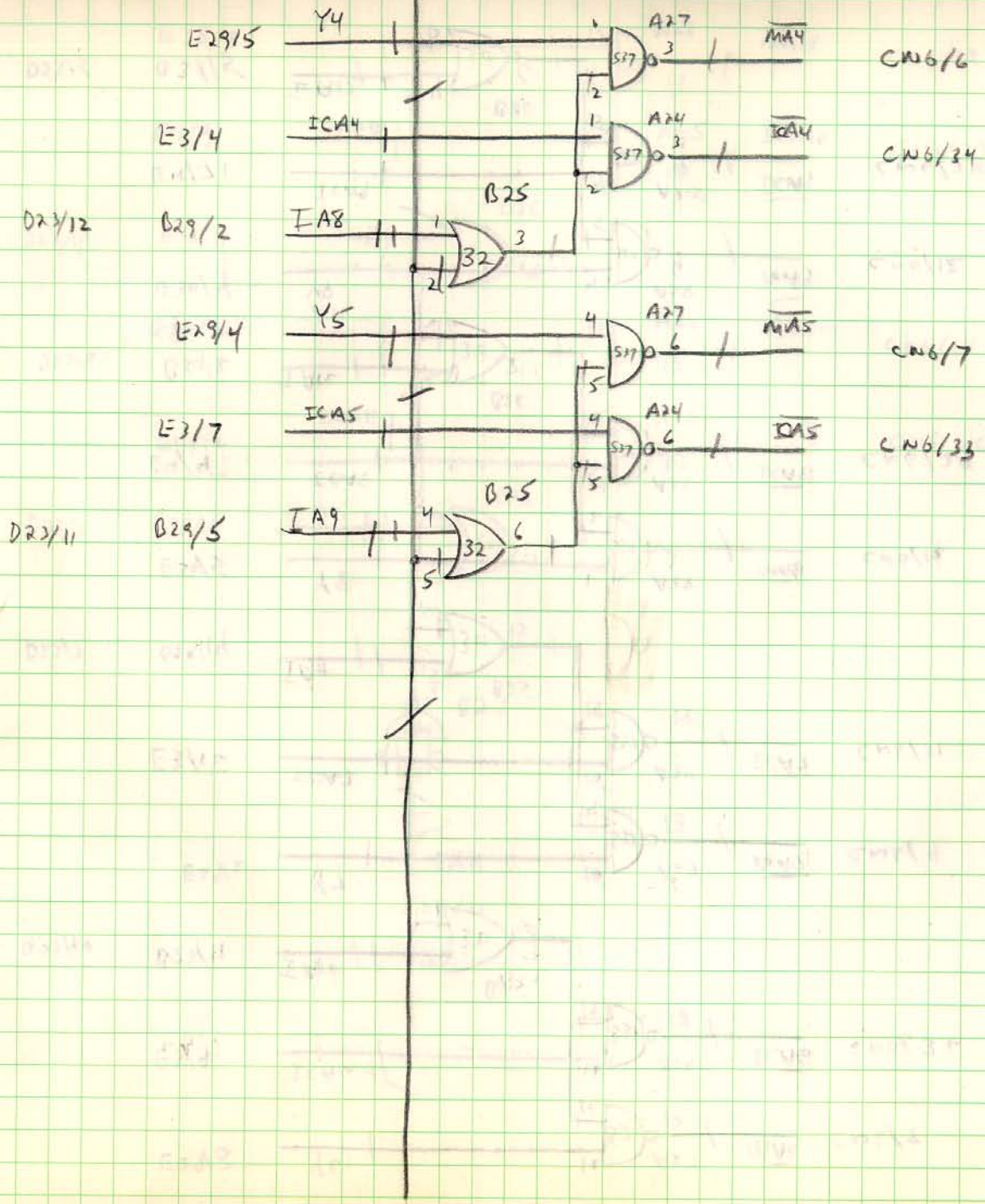
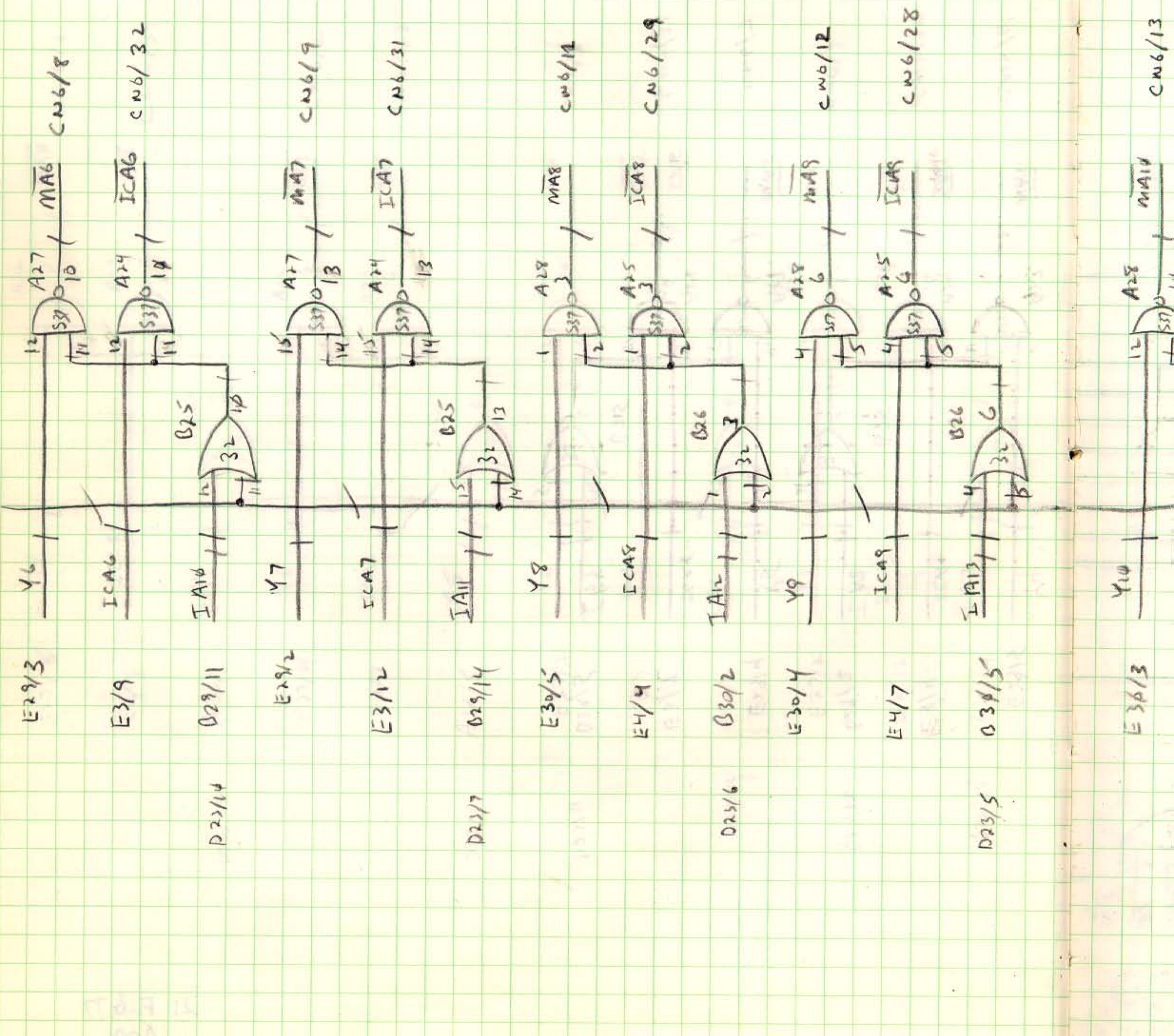
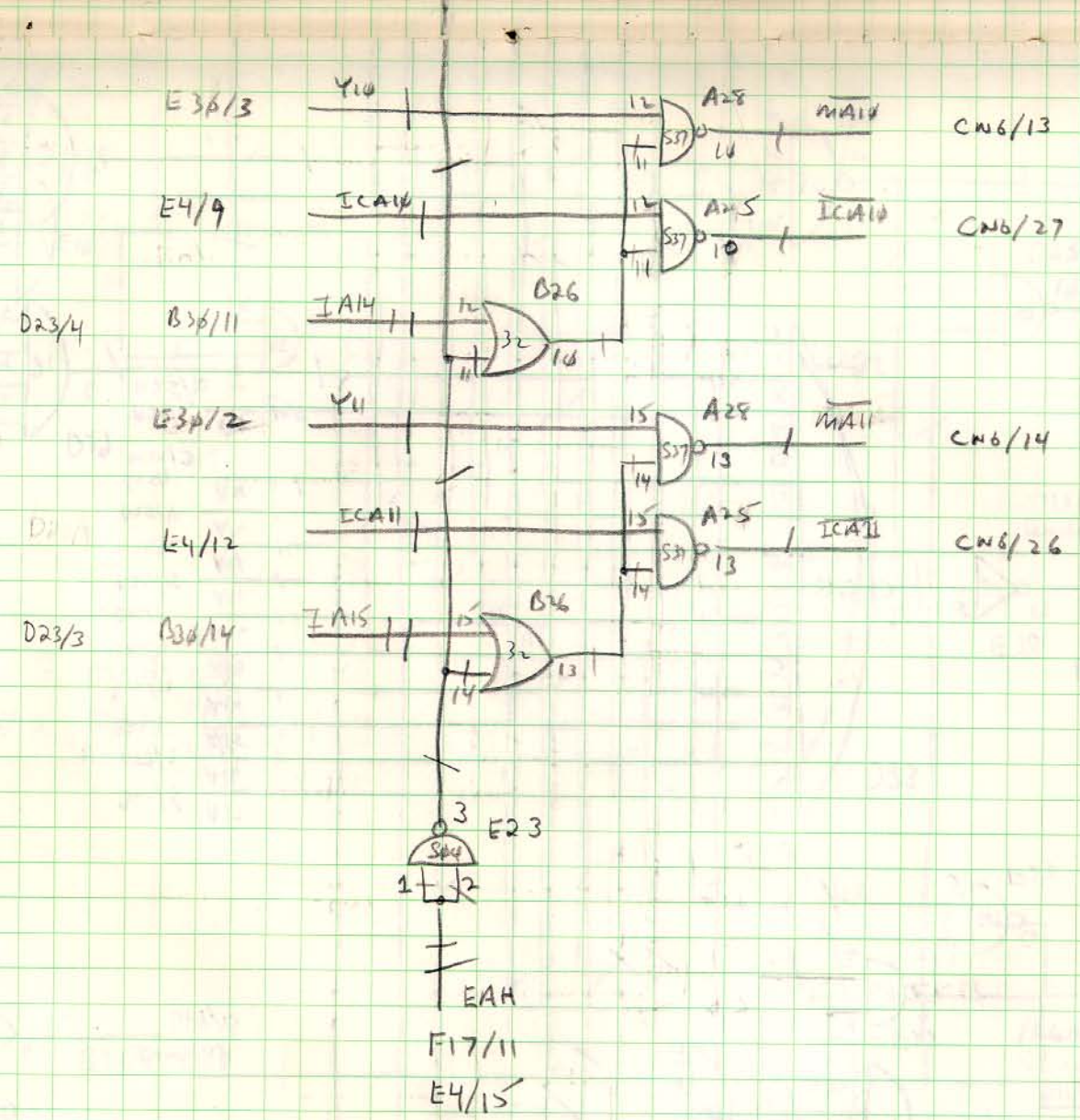
ABD


MCode & Icode Address Buffer - Drivers
<0:5>
E27/5
Y4
A26
S37
MA4
CN6/1
E2/4
ICA4
A23
IA4
CN6/39
D18/2
A3B/2
IA4
B24
32
E27/4
Y1
MA1
CN6/2
E2/7
ICA1
IA1
CN6/38
D15/1
A3B/5
IA5
E27/3
Y2
MA2
CN6/3
E2/9
ICA2
IA2
CN6/37
D23/14
A3B/4
IA6
E27/2
Y3
MA3
CN6/4
E2/12
ICA3
IA3
CN6/36
D22/13
A3B/14
IA7
E29/5
Y4
MA4
CN6/6

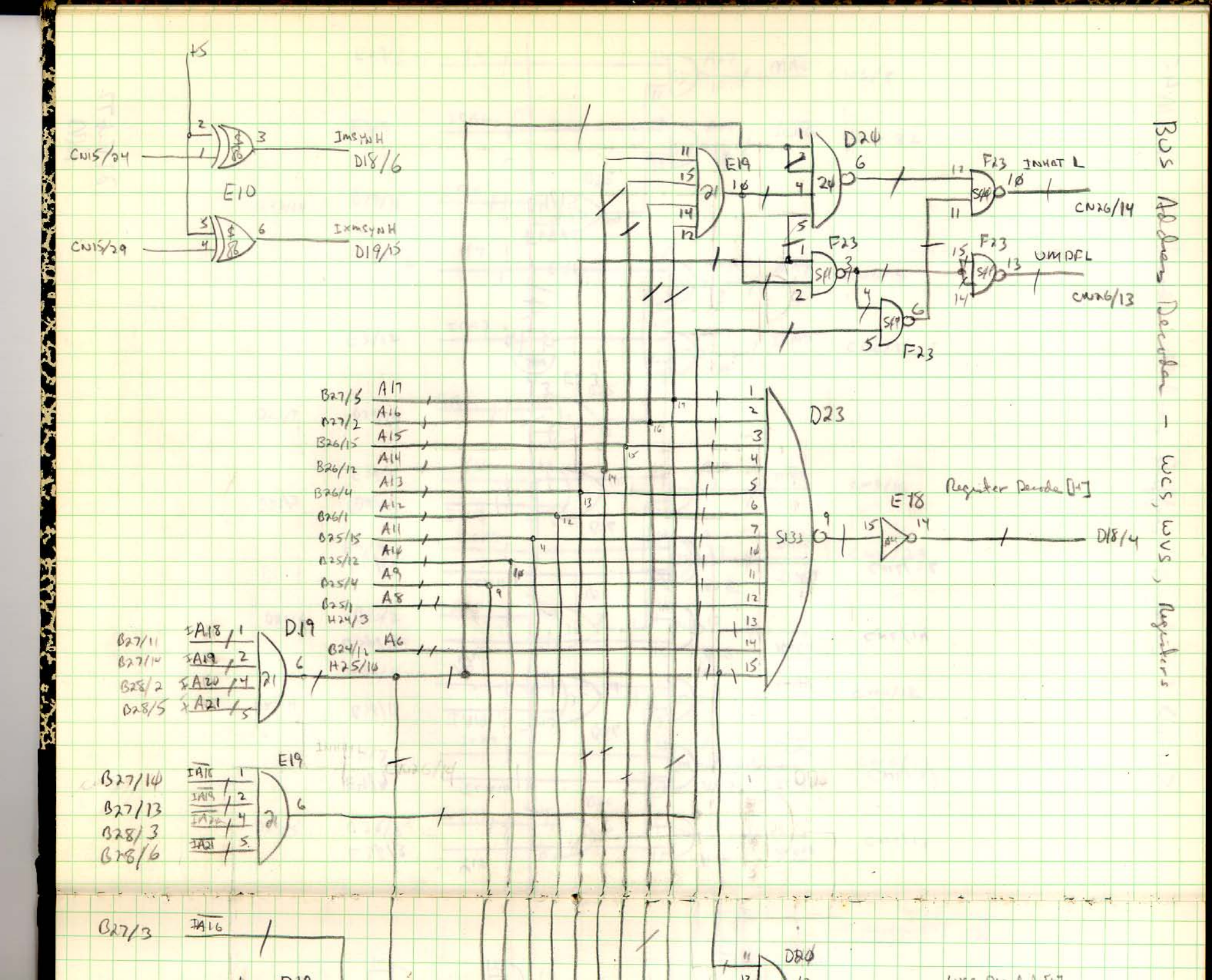

E29/5
Y4
A27
MA4
CN6/6
E3/4
ICA4
A24
ICA4
CN6/34
B25
D23/12
B29/2
IA8
32
E29/4
Y5
A27
MA5
CN6/7
E3/7
ICA5
A24
ICA5
CN6/33
B25
D23/11
B29/5
IA9
32

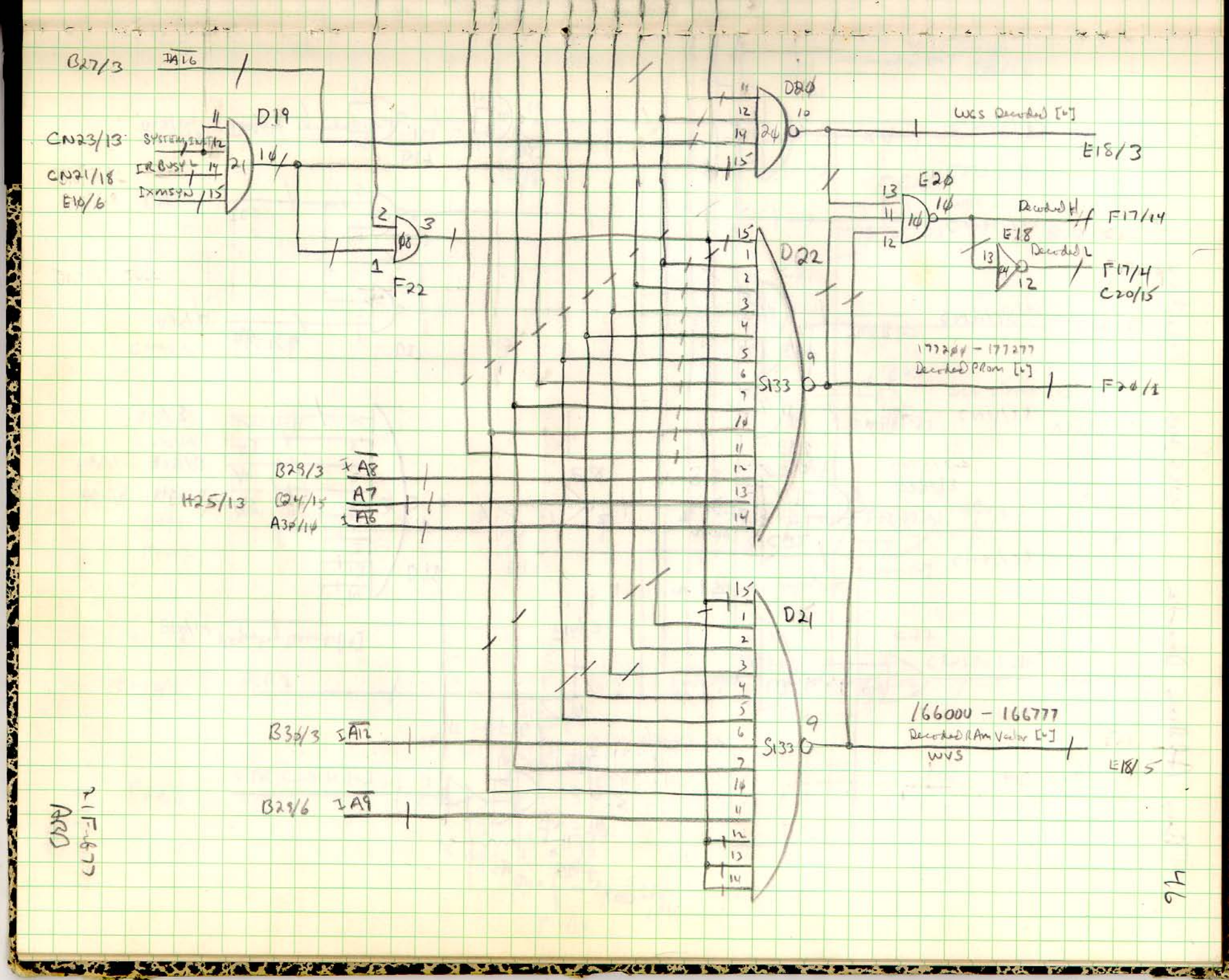
Mcode & Icode Address Buffers - Inverters <6:11>

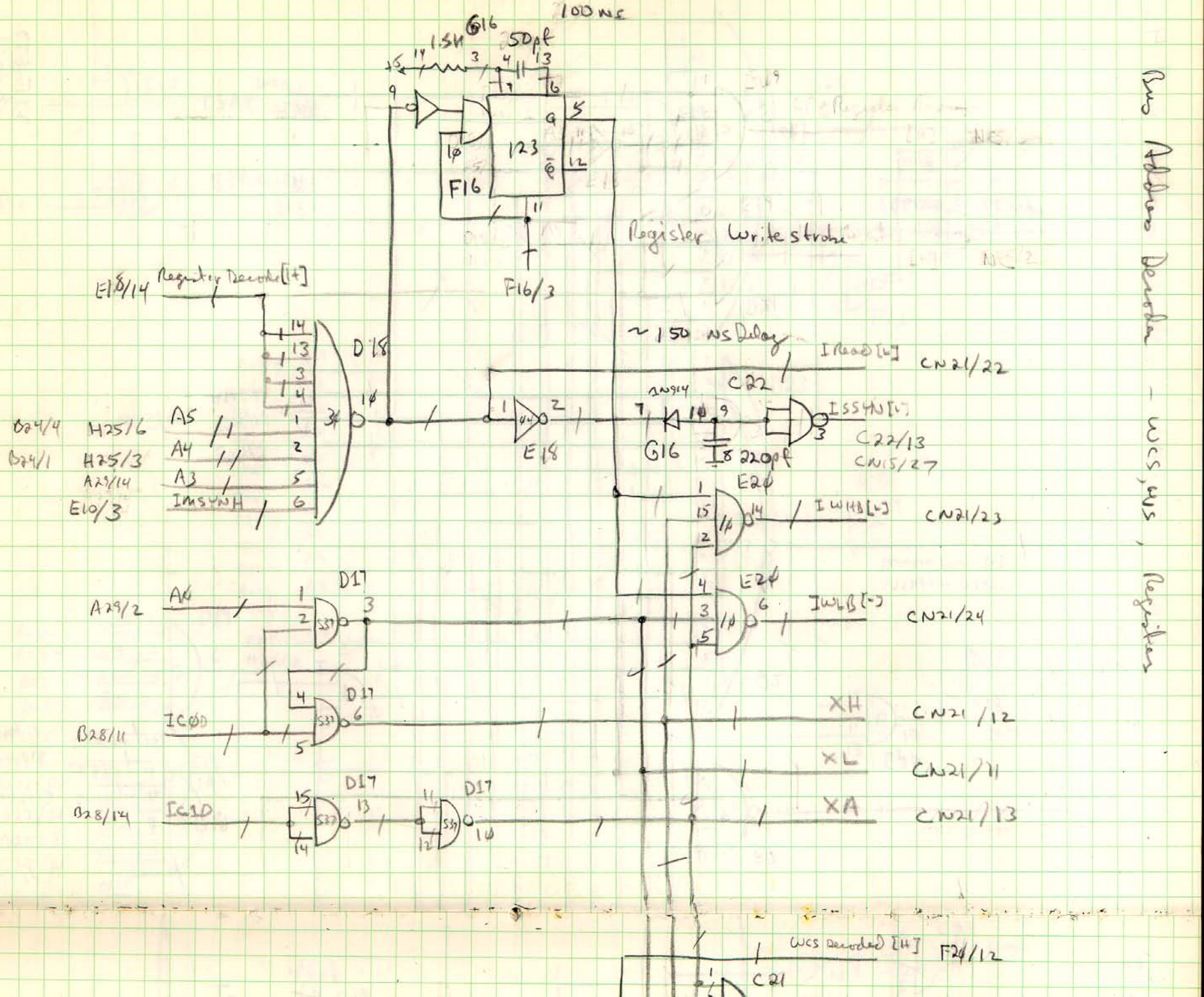


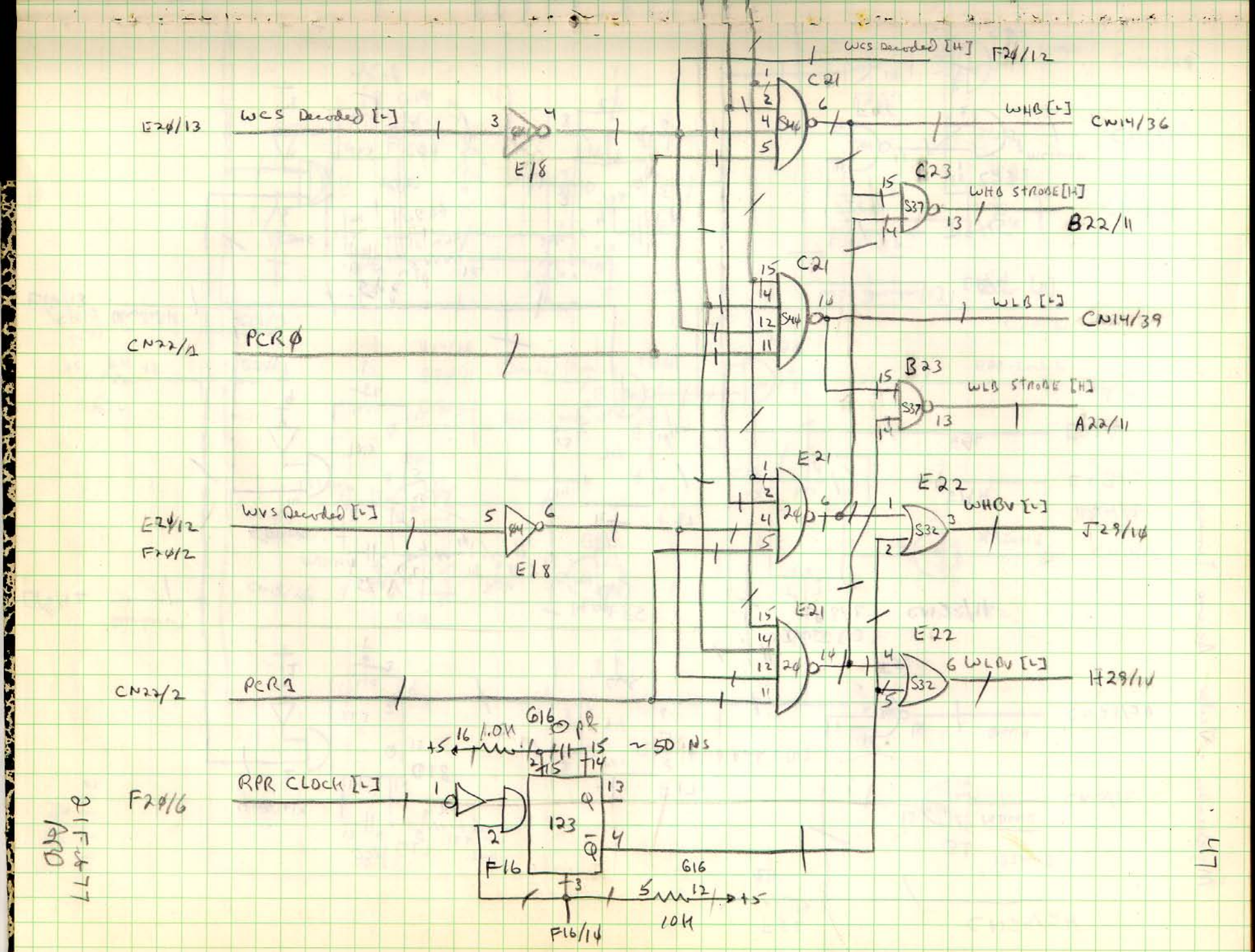

E3Φ/3
Y10
12
A28
S37
MA10
CN6/13
11
10
E4/9
ICA10
A25
ICA10
CN6/27
B26
D23/4
B3Φ/11
IA14
32
16
E3Φ/2
Y11
15
MA11
CN6/14
13
14
ECA11
E4/12
A25
ICA11
CN6/26
D23/3
B3Φ/14
IA15
B26
3
E23
S04
1
2
EAH
F17/11
E4/15

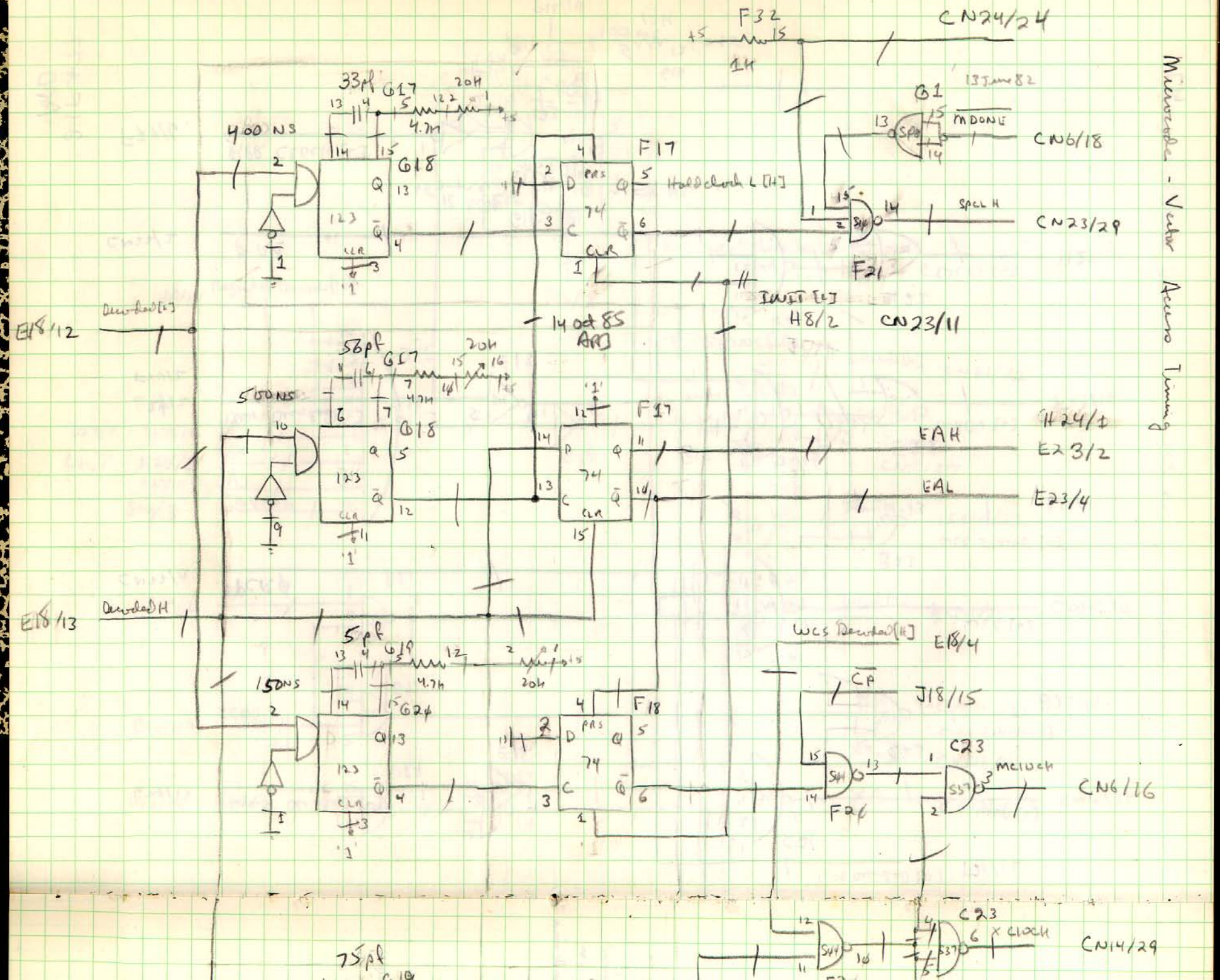
2 1F87 ADS

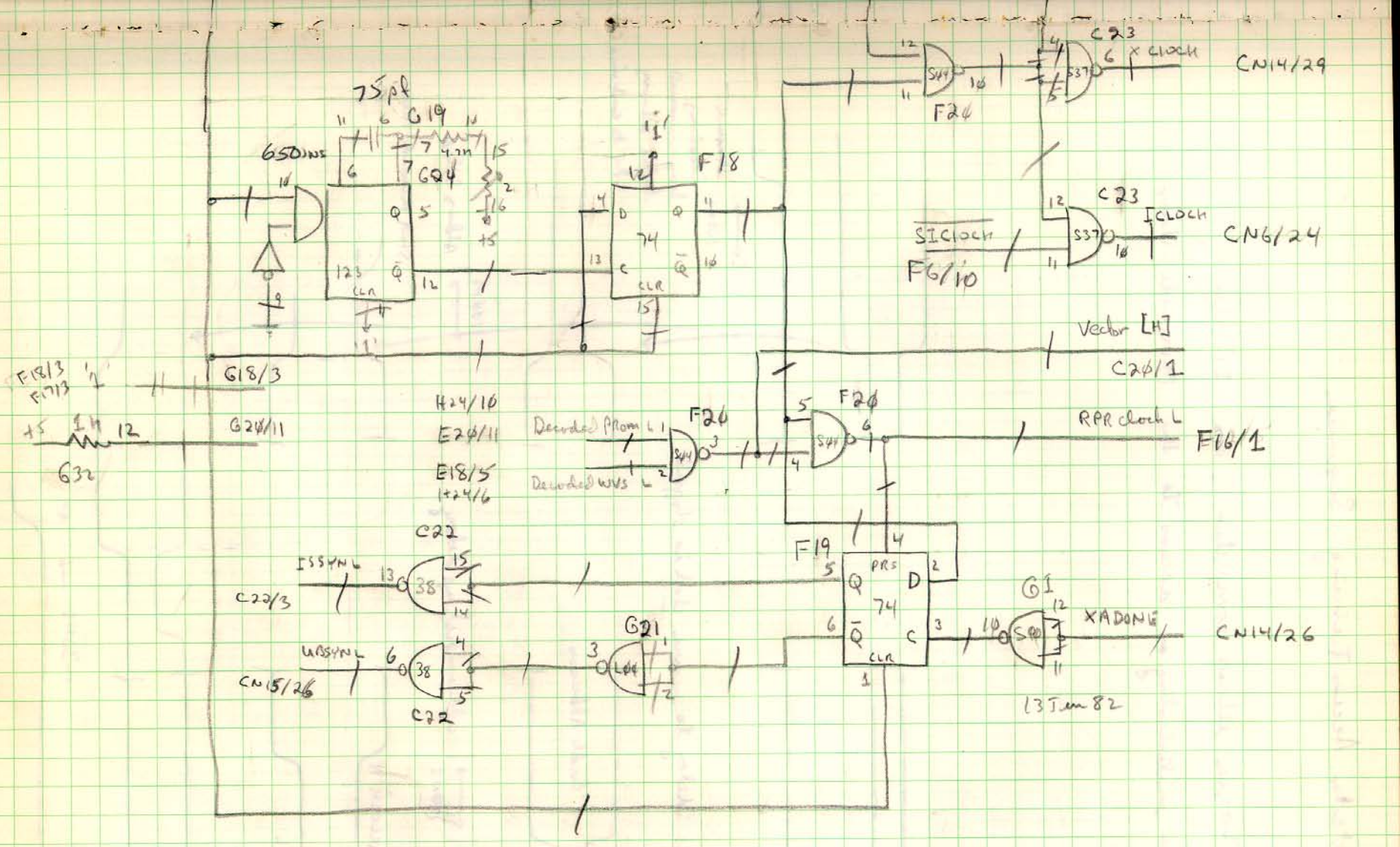

BUS Address Decoder - WCS, WVS, Registers
+5
CN15/24
CN15/29
E10
IMSYNH
D18/6
IXMSYNH
D19/15
E19
D24
F23
INHAT L
CN26/14
UMPFL
CN26/13
B27/5
B27/2
B26/15
B26/12
B26/4
B26/1
B25/15
B25/12
B25/4
B25/1
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
H24/3
D23
S133
E18
Register Decode [4]
D18/4
D19
B27/11
B27/14
B28/2
B28/5
IA18
IA19
IA20
IA21
B24/12
H25/16
A6
B27/10
B27/13
B28/3
B28/6
IA16
B27/3
D20


B27/3
IA16
D19
CN23/13
CN21/18
E10/6
SYSTEM SELECT 12
IRBUSY L 14
IXMSYN 15
21
10
2
3
08
1
F22
D20
24
11
12
14
15
10
WCS Decoded [L]
E18/3
E20
16
13
11
12
Decoded H
F17/4
E18
Decoded L
F17/4
C20/15
D22
S133
9
177200 - 177277
Decoded PROM [L]
F20/1
B29/3
H25/13
IA8
A7
IA6
D21
S133
9
166000 - 166777
Decoded IOAM Vector [L]
WVS
E18/5
B30/3
IA12
B29/6
IA9
94


Bus Address Decoder - WCS, WS, Registers
100 NS
G16
1.5K
50pf
F16
123
Register Write strobe
F16/3
E18/14
Register Decode [+]
D18
~150 NS Delay
IRead [L]
CN21/22
C22
E18
G16
220pf
ISSYN [L]
C22/13
CN15/27
E24
IWHB [L]
CN21/23
IWLB [L]
CN21/24
D17
A29/2
A0
B24/4
H25/6
A5
B24/1
H25/3
A4
A29/14
A3
E10/3
IMSYNH
B28/11
IC00
XH
CN21/12
XL
CN21/11
B28/14
IC10
XA
CN21/13
WCS Decoded [H]
F24/12
C21


WCS Decoded [H] F24/12
C21
WCS Decoded [L]
E24/13
E18
WHB [L]
CN14/36
C23
WHB STROBE [H]
B22/11
C21
WLB [L]
CN14/39
CN22/1
PCR0
B23
WLB STROBE [H]
A22/11
E21
E22
WCS Decoded [L]
E24/12
F24/12
E18
WHBV [L]
J29/10
E21
E22
WLBV [L]
H29/14
CN22/2
PCR1
G16
16 1.0K +5
~ 50 NS
RPR CLOCK [L]
F24/6
123
F16
G16
10K +5
F16/14


Microcode - Vector Access Timing
F32
CN24/24
33pf
G17
20H
400 NS
G18
F17
G1
MDONE
CN6/18
SPCL H
CN23/29
F21
Hold clock L [H]
INIT [L]
H8/2
CN23/11
14 oct 85
AM
E18/12
56pf
500NS
EAH
H24/1
E23/2
EAL
E23/4
E18/13
5pf
150NS
G24
F18
WCS Decoded [H]
E18/4
CP
J18/15
C23
MCLOCK
CN6/16
F24
75pf
X CLOCK
CN14/29


75pf
G19
650 NS
G24
F18
74
CLR
C23
X CLOCK
CN14/29
F24
SICLOCK
CLOCK
CN6/24
F6/10
Vector [H]
C24/1
F18/3
F17/3
'1'
G18/3
+5
1K
G24/11
G32
H24/16
E24/11
E18/5
H24/6
Decoded Prom L
Decoded WVS L
F26
F24
RPR clock L
F16/1
C22
ISSYN L
C22/3
USSYN L
CN15/26
G21
F19
PRS
G1
XADONE
CN14/26
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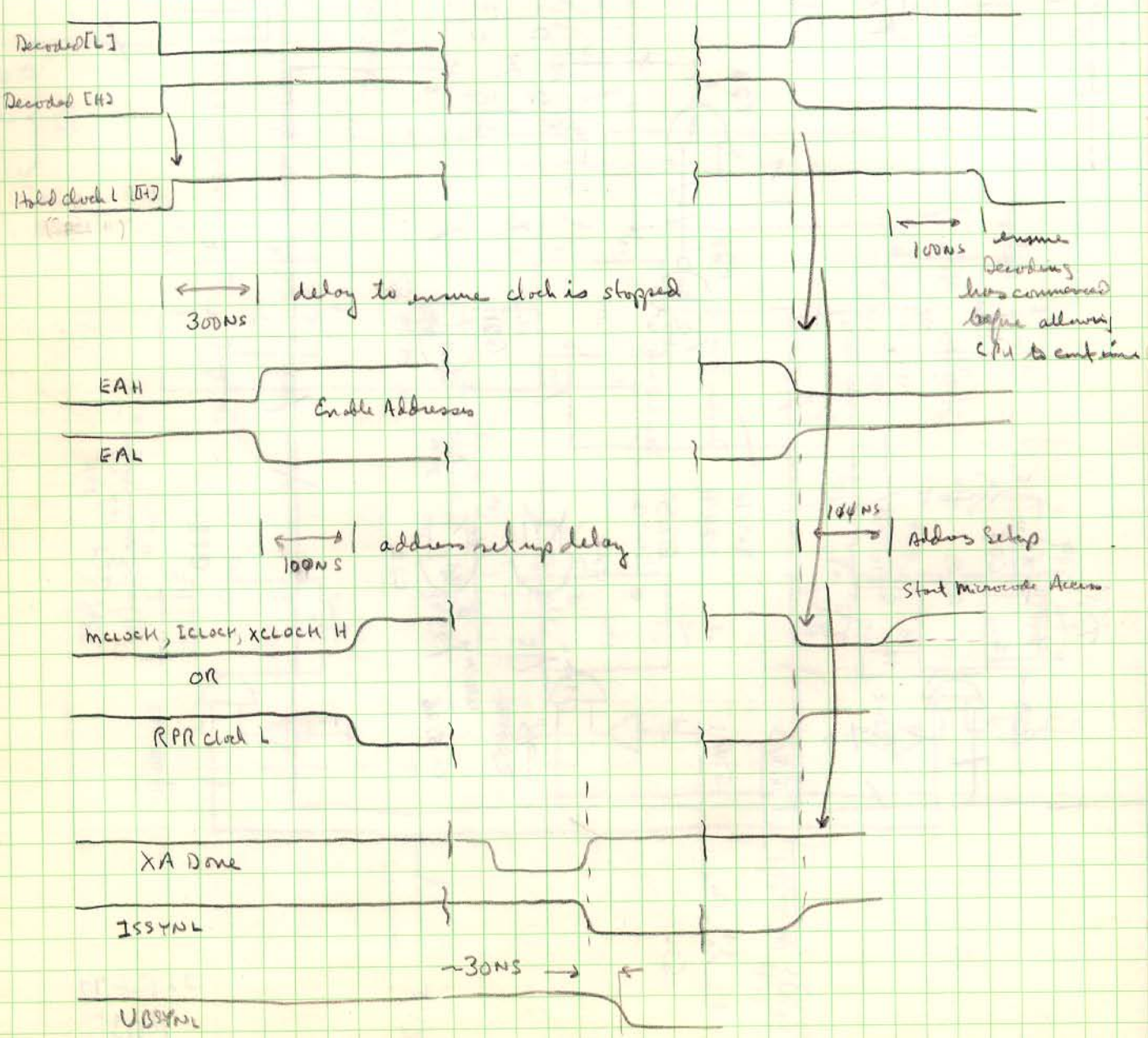
ADD
47

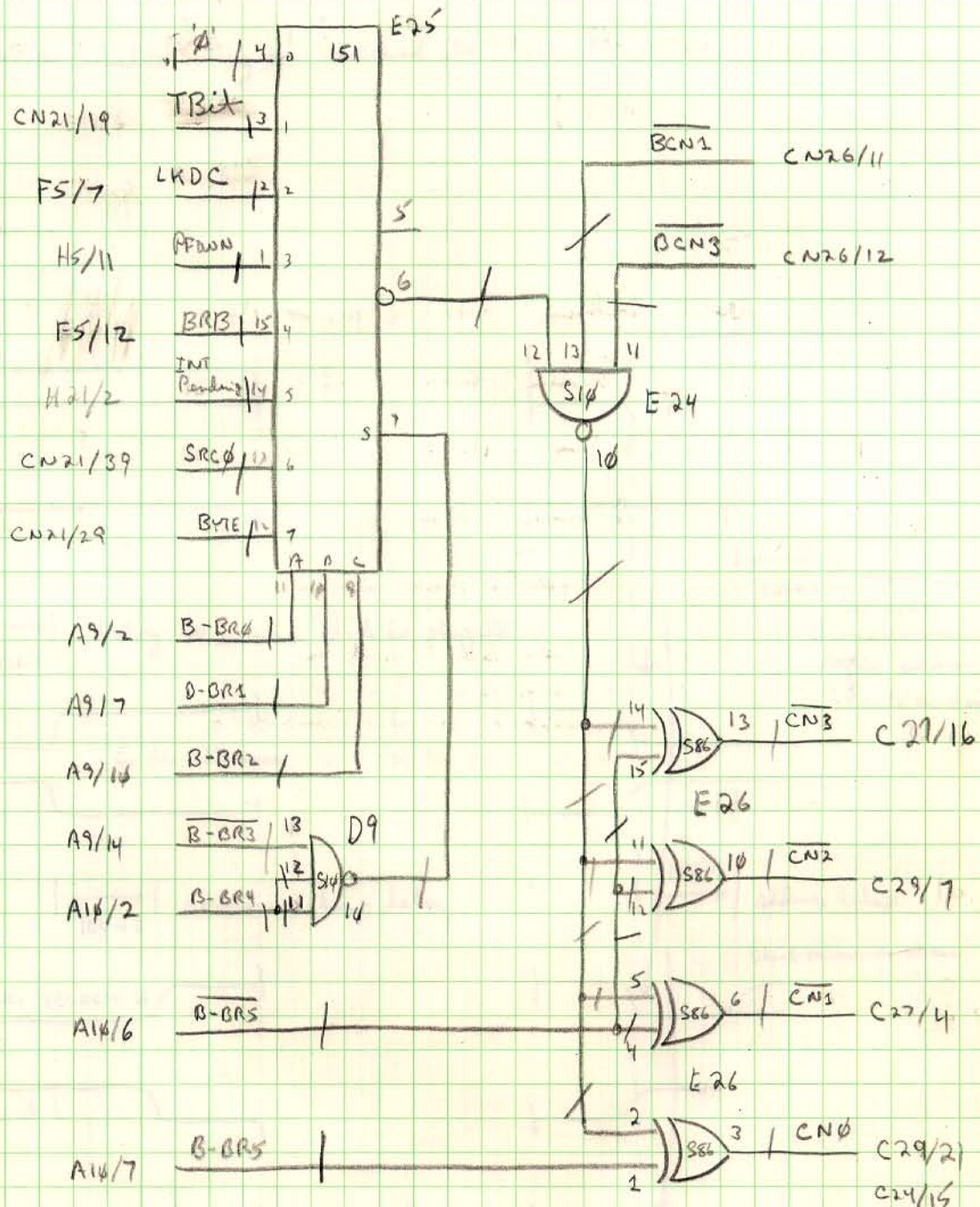
Microcode - Vector Access Timing Sequence

Decoding Logic allows completion of an IR decode sequence before initiating an access to the Microcode - Vector memories

Sequence



Branch Condition logic



16 Micro controlled Branching operations with 32 testable conditions (+32 more with the universe)

Notes:

Next Address from micro PC (S1=0; S0=0)

Repeat Address from AR (S1=0; S0=1)

Return Stack Address from STKO (S1=1; S0=0)

Branch Address from D (S1=1; S0=1)

Tristate Bussed:

1) Micro Start
2) Power fail Micro Address
3) Microcode Branch Address
4) Vector Branch Address
5) Scratch Register Branch Address
6) Internal Instruction Branch Address
7) External Instruction Branch Address

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ARD

Instruction Code

D	C	B	A	OPERATION (Notes)	Condition State	
ϕ	ϕ	ϕ	ϕ	Branch (Micro) V Condition (must use even Branch Address)	0	1
ϕ	ϕ	ϕ	1	Conditional Branch (Micro) V <C><N> ; Next	0	1
ϕ	ϕ	1	ϕ	Conditional Branch (Micro) V <V><Z> ; Next	0	1
ϕ	ϕ	1	1	Conditional Branch (Micro) V <C><V><Z><N> ; Next	0	1
ϕ	1	ϕ	ϕ	Conditional Branch (Micro) ; Repeat	0	1
ϕ	1	ϕ	1	Conditional Branch (Micro) ; Next	0	1
ϕ	1	1	ϕ	Conditional JSR (Micro) ; Repeat	0	1
ϕ	1	1	1	Conditional JSR (Micro) ; Next	0	1
1	ϕ	ϕ	ϕ	Conditional Next ; Repeat	0	1
1	ϕ	ϕ	1	Conditional PopStack ; Next always	0	1
1	ϕ	1	ϕ	Conditional RTS ; Repeat	0	1
1	ϕ	1	1	Conditional RTS ; Next	0	1
1	1	ϕ	ϕ	Conditional Branch Icode ; Next branches to current Icode level	0	1
1	1	ϕ	1	Conditional JSR Icode ; Next JSR's to current Icode level	0	1
1	1	1	ϕ	Conditional Branch Icode ; Next clocks priority, branches to next Icode level	0	1
1	1	1	1	Conditional JSR Icode ; Next clocks priority, JSR's to next Icode level	0	1

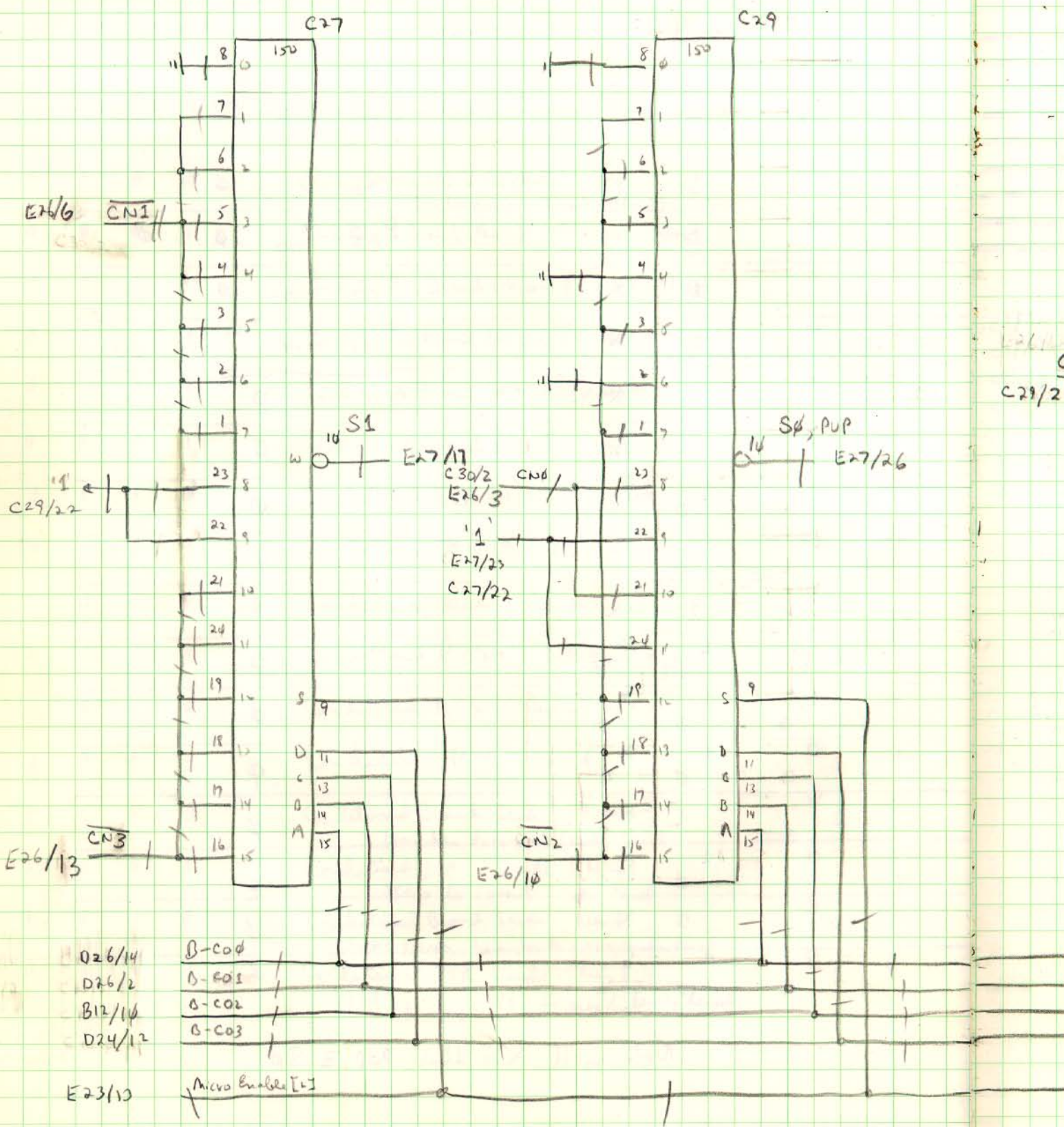
Micro controller Encoding

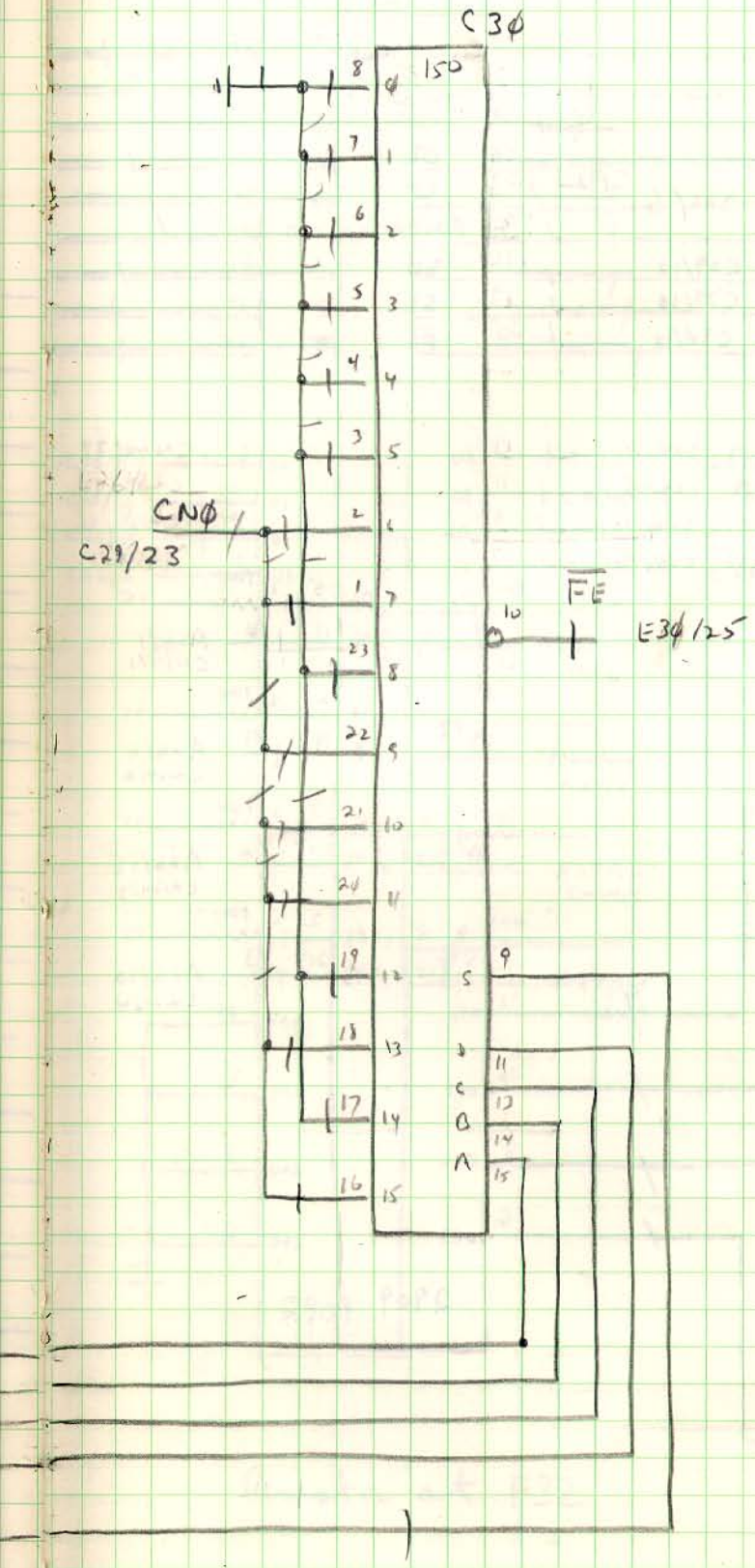
S1	SØ	$\overline{FE}$	PUP	ORØ	OR1	OR2	OR3
1	1	1	X	[CN]	Ø	Ø	Ø
0	0	1	X	Ø ⟨C⟩	Ø ⟨N⟩	Ø	Ø
0	0	1	X	Ø ⟨V⟩	Ø ⟨Z⟩	Ø	Ø
0	0	1	X	Ø ⟨C⟩	Ø ⟨V⟩	Ø ⟨Z⟩	Ø ⟨N⟩
0	1	1	X				Ø
0	0	1	X				Ø
0	1	1	X				Ø
0	0	1	X				Ø
Ø	1	1	X				Ø
Ø	Ø	1	X				Ø
Ø	1	1	X				Ø
0	0	1	X				Ø
0	0	1	X				Ø
0	0	1	X				Ø
0	0	1	X				Ø
0	0	1	X				Ø
0	0	1	X				Ø
0	0	1	X				Ø

Note with X's that PUP ≡ SØ

22 Feb 77
ARD

Control Signal Generation





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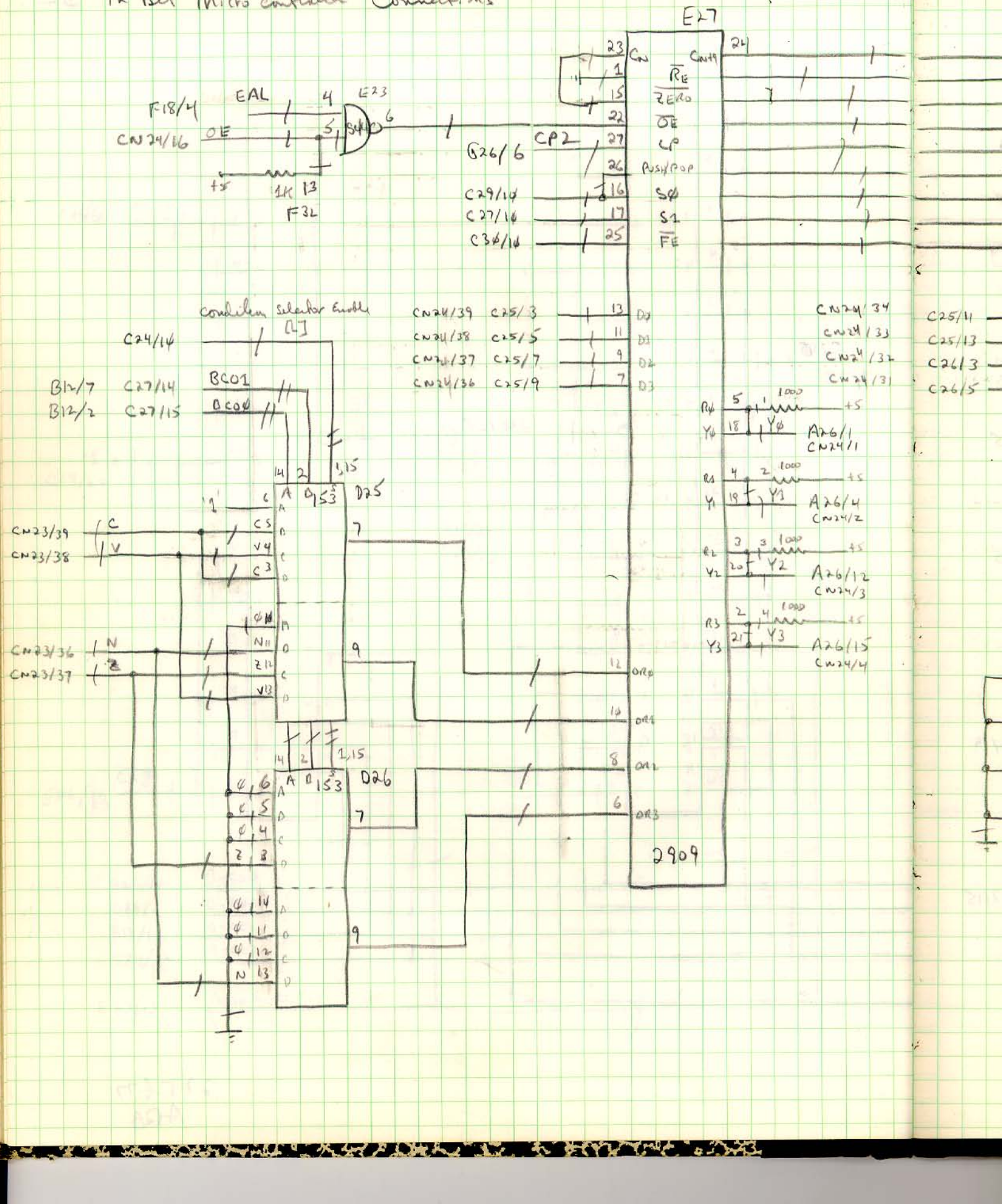
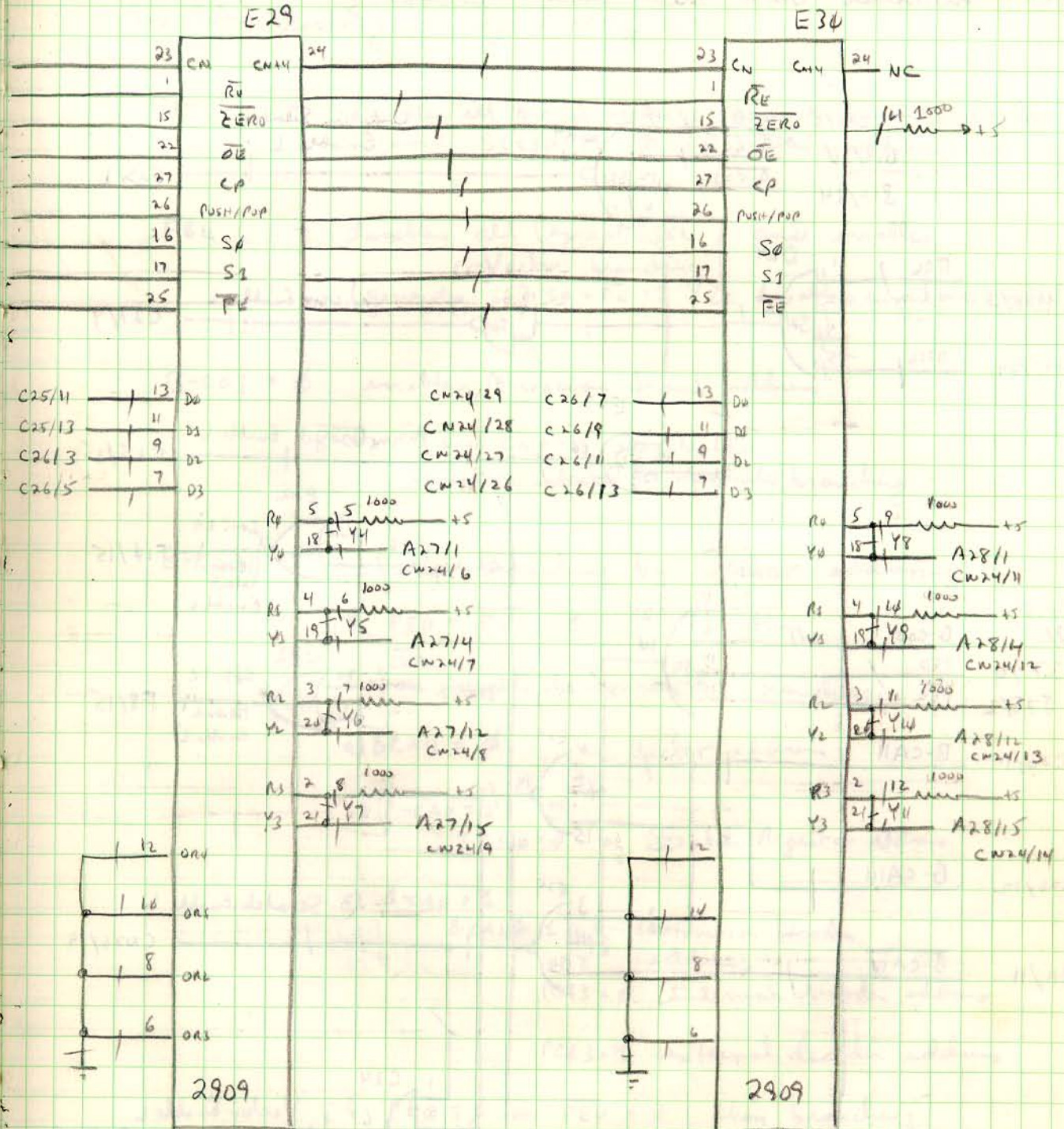
ARB

12 Bit Micro controller Connections





Resistor at F32

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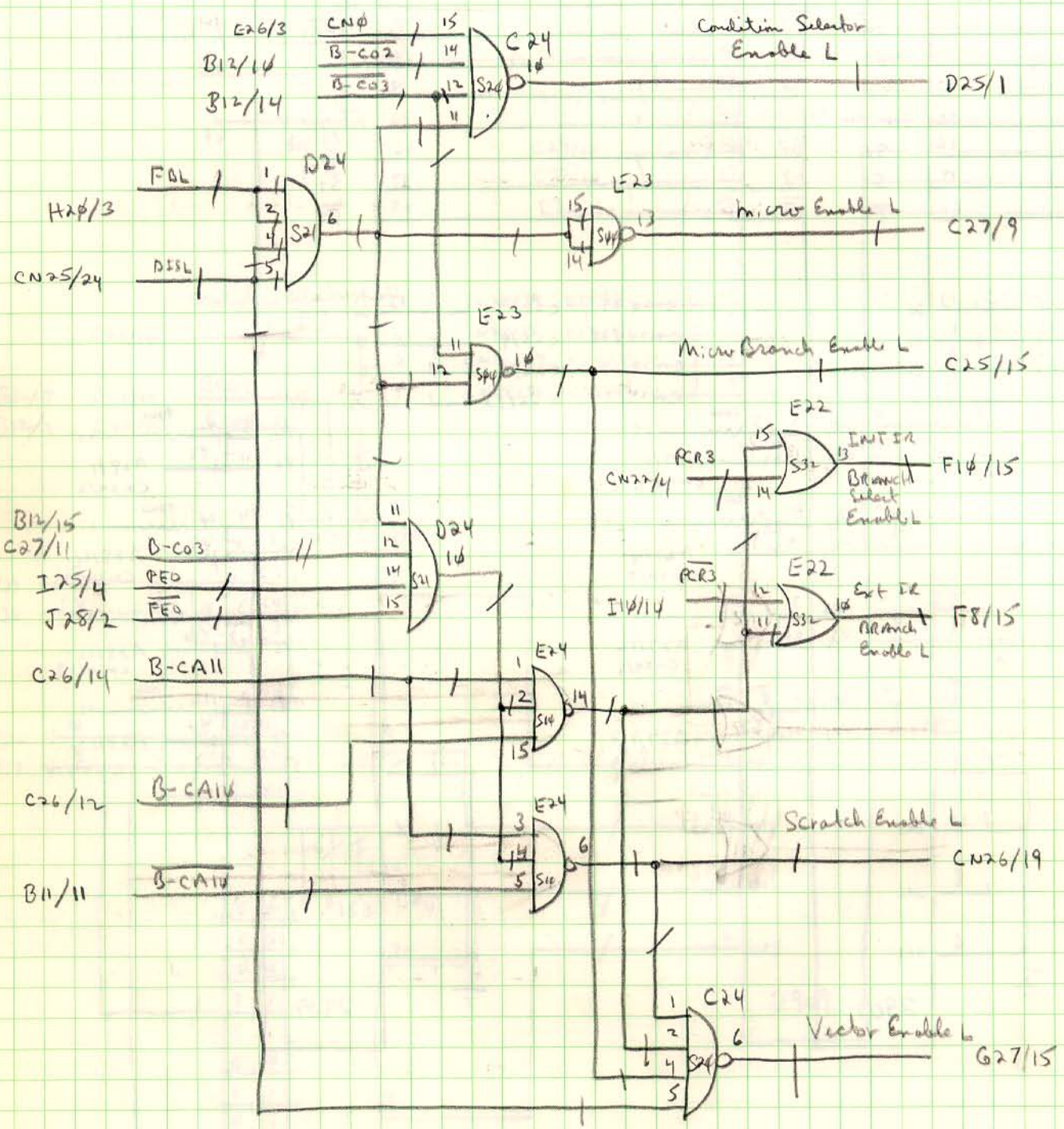
ARB

Microcontroller Data Bus Select Decoding



Bus Select Decoding - By Priority

DISL – disables all branch selects (except Console start & Power fail)
(generates S1 = SØ = FE = 1 ie disables current micro instruction)
Branching

FBL – disables all (except DISL) and enables Vector branching
(generates S1 = SØ = $\overline{FE}$ = 1 ie disables current micro instruction)
Branching

B-CO3 = Ø enables Microcode Branch address

$\overline{B\text{-}CO2}$ = 1 and CNØ = 1 enables the Condition Selector for multiple branching

B-CO3 = 1 enables branching by vector addressing

if PEO = $\overline{FEO}$ = 1 then

there are multiple sources for branching

a) BCA11 = Ø by Vector address

b) B-CA11 = 1
B-CA10 = Ø by Scratch Register address

c) B-CA11 = 1
B-CA10 = 1 by Instruction Decoder address
PCR3 = Ø internal decoder address
PCR3 = 1 external decoder address

if PEO = Ø or $\overline{FEO}$ = Ø then branching will be by Vector always

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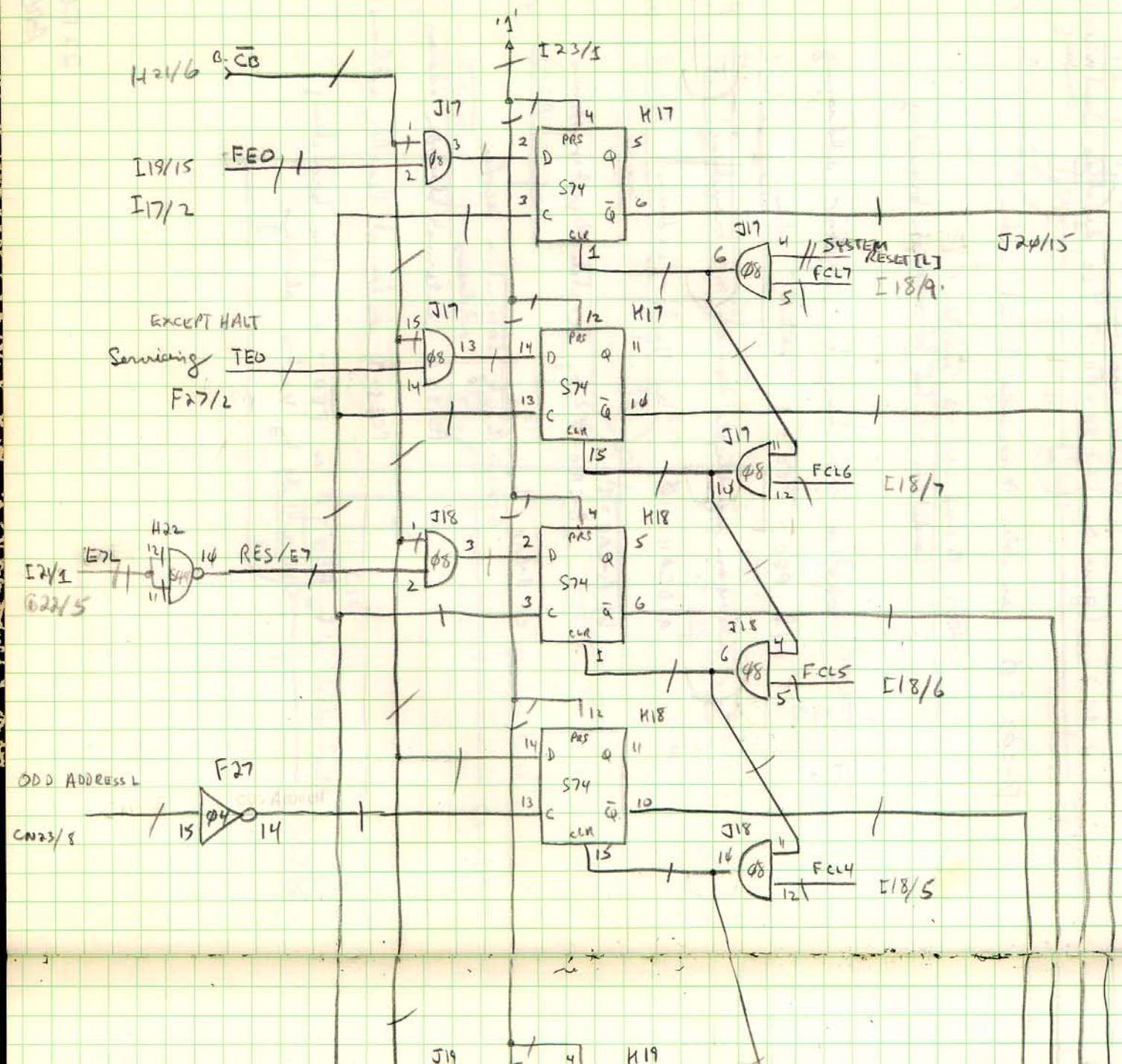
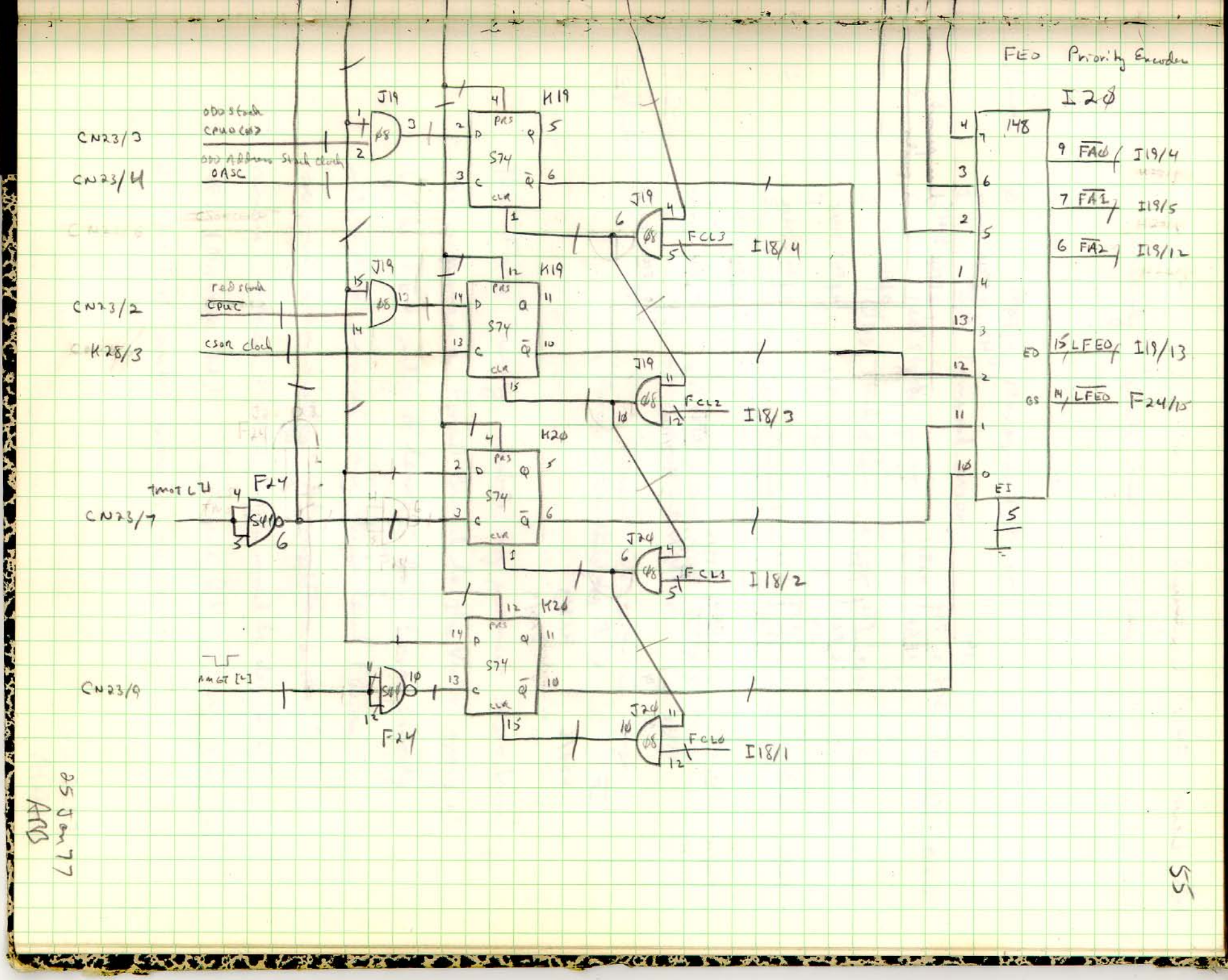
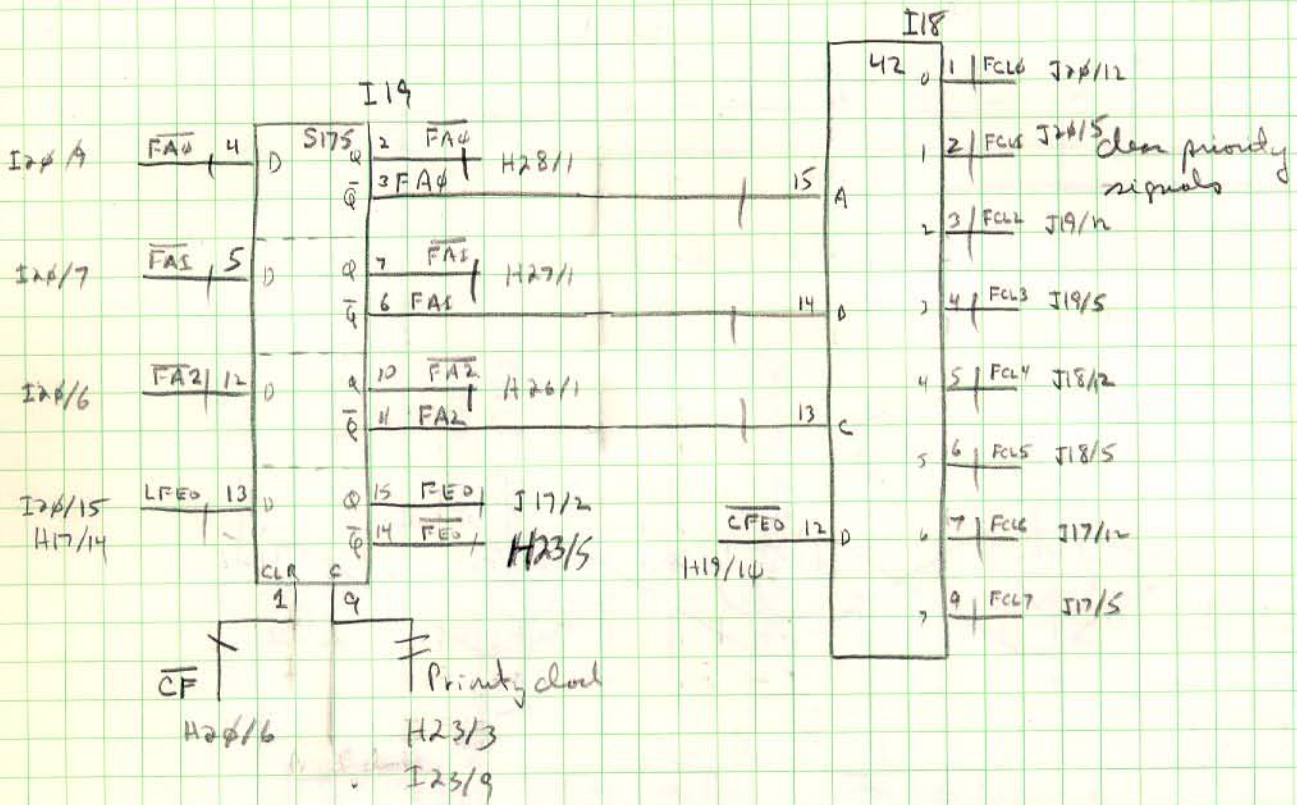
ARB

Control Priority Shutdown Logic Level FED (Force)




FED Priority Encoder
I20
148
CN23/3
CN23/4
CN23/2
K28/3
CN23/7
CN23/9
odd stack CPUA CLK
odd Address Stack clock
OASC
read stack CPUC
CSOA clock
TMOT LU
TMOT [-]
F24
J19
K19
J20
K20
S74
S40
FCL3
FCL2
FCL1
FCL0
I18/4
I18/3
I18/2
I18/1
9 FA0 I19/4
7 FA1 I19/5
6 FA2 I19/12
15 LFED I19/13
14 LFED F24/15
ED
GS
EI

Level FED Continued



Priority levels and conditions -

Lowest	∅	Memory Management Error
	1	BUS Timeout error
	2	Red stack error
	3	ODD stack Address error
	4	ODD Address for Word Input (DATI, P, IR)
	5	Timeout error while servicing a programmed EI level
	6	Timeout error while servicing a programmed interrupt or PF, YS, T-TRAP
Highest	7	Timeout error while servicing a Forced Interrupt (any FED)

The Force Priority inhibits any processor micro branching and sequences a Forced Branch to the Vector specified by the FED interrupt level. Any lower priority interrupt is ignored, any higher level FED is serviced immediately. At completion of the FED service routine the FED logic must be cleared by CFP (Microcode Bit). The console Bit $\overline{CB}$ can disable all FED Traps under microprogram control.

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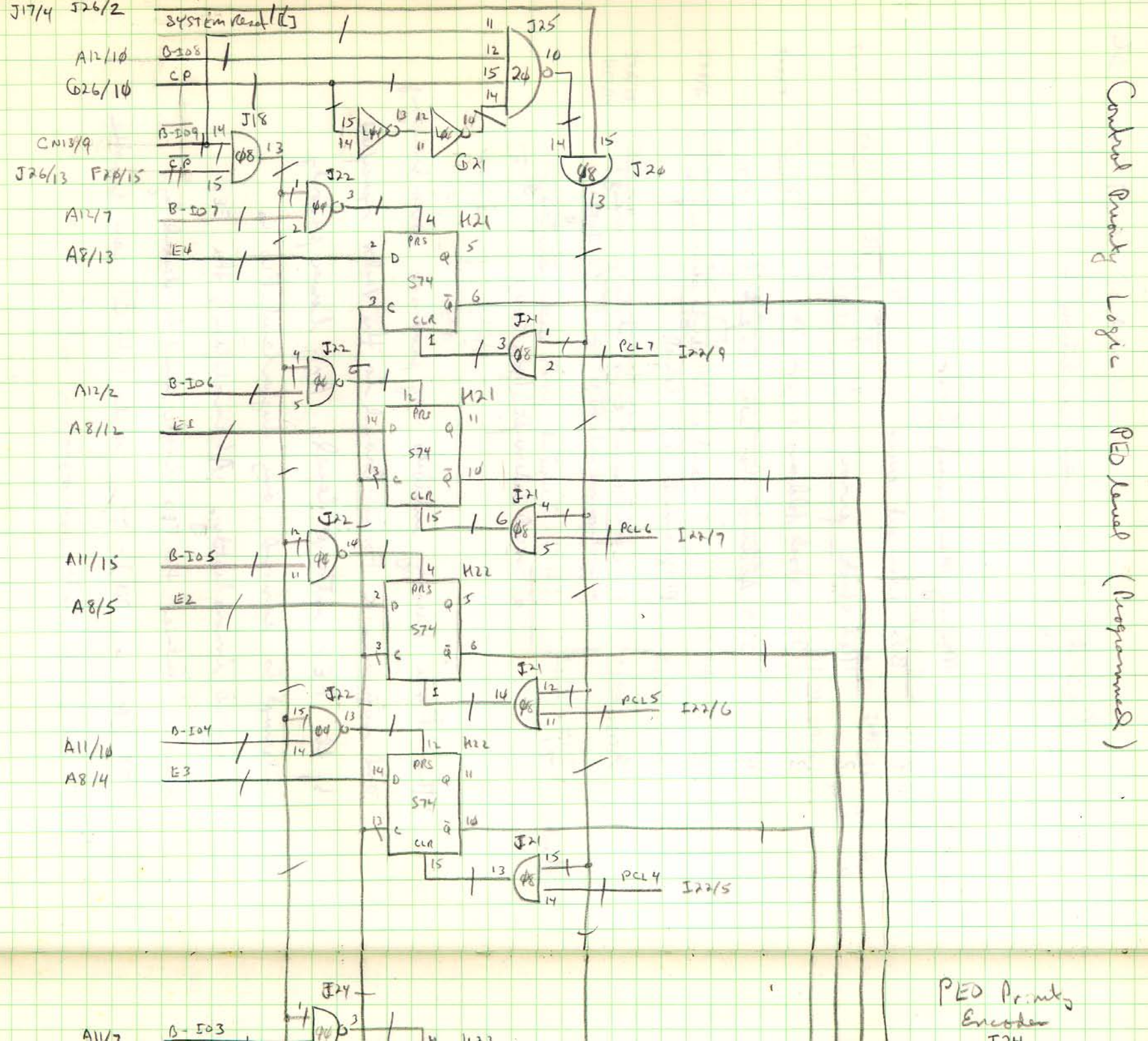
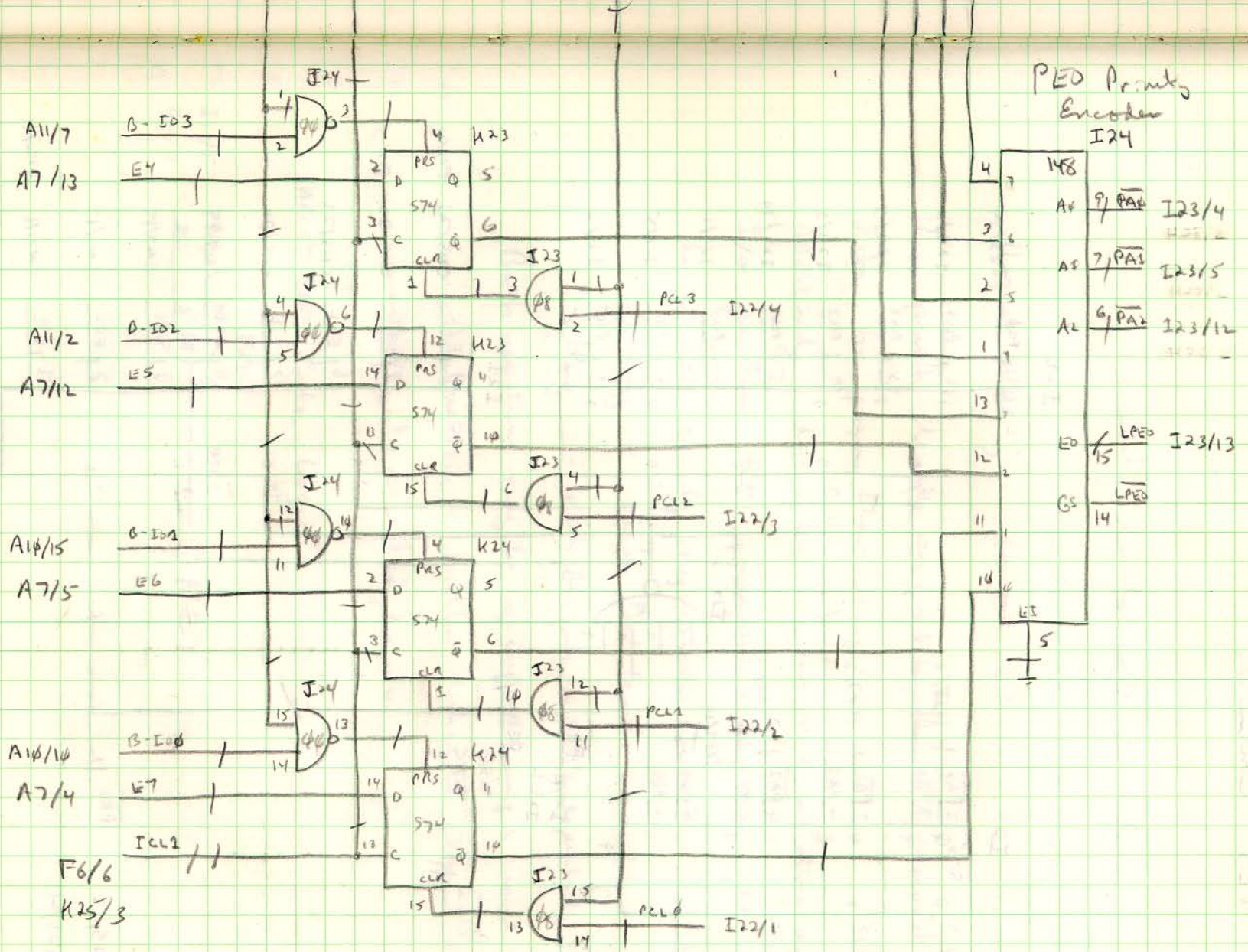
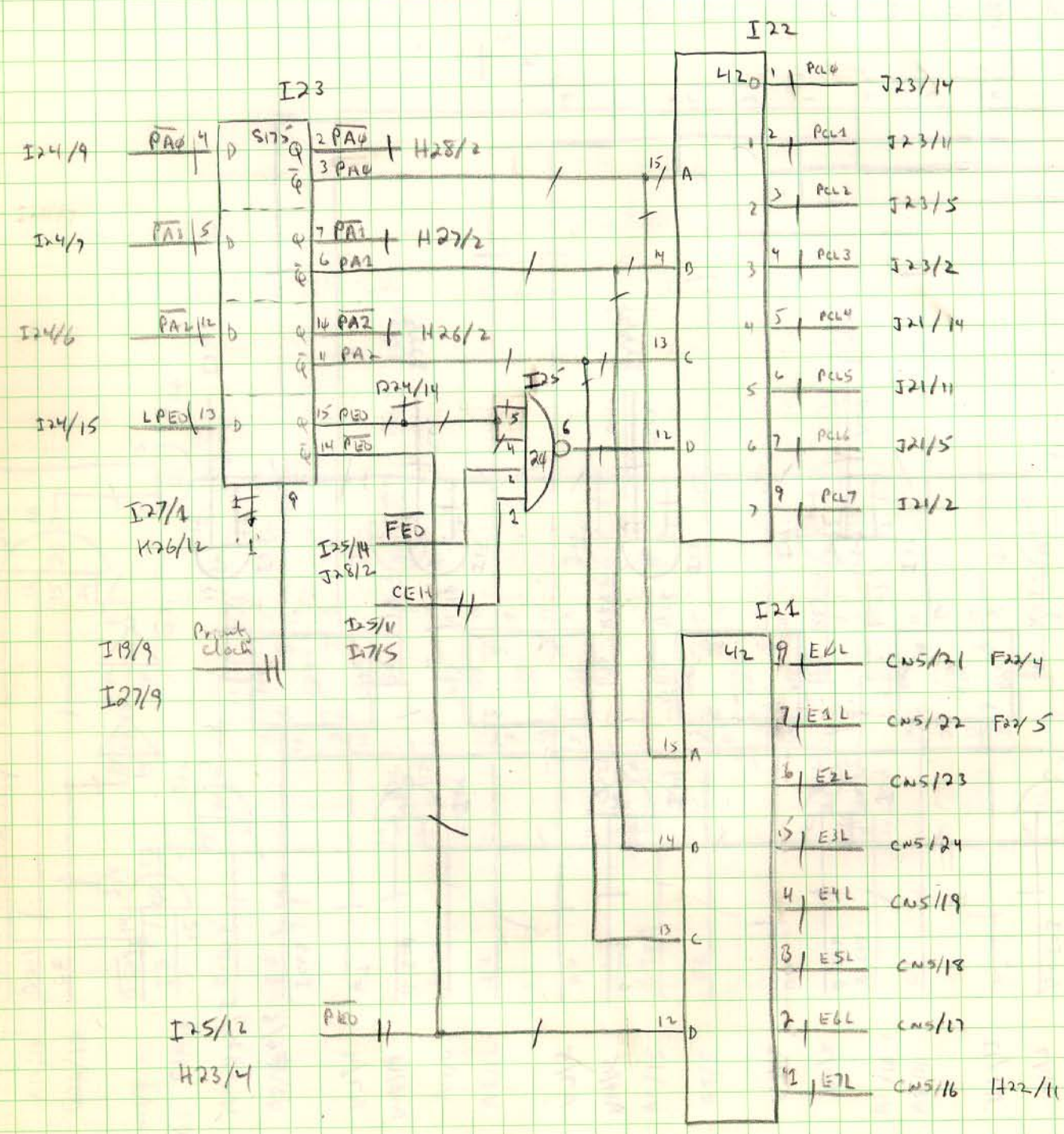
ABB


Control Priority Logic PED Panel (Programmed)
J17/4 J26/2
System Reset [L]
A12/10 D-IO8
G26/10 CP
CN13/9 B-IO9
J26/13 F2P/15 CP
J18
J25
J20
G21
A12/7 B-IO7
A8/13 E4
J22
H21
S74
PRS
D
C
CLR
Q
J21
PCL7
I22/9
A12/2 B-IO6
A8/12 E1
PCL6
I22/7
A11/15 B-IO5
A8/5 E2
H22
PCL5
I22/6
A11/10 B-IO4
A8/4 E3
PCL4
I22/5
PED Priority Encoder J24
A11/7 B-IO3


PLED Priority Encoder
I24
148
A11/7
B-ID3
A7/13
E4
A11/2
B-ID2
A7/12
E5
A10/15
B-ID1
A7/5
E6
A10/14
B-ID0
A7/4
E7
ICL1
F6/6
K25/3
K23
K24
S74
PRS
CLR
I23
PCL3
PCL2
PCL1
PCL0
I22/4
I22/3
I22/2
I22/1
A0 9 PA0 I23/4
A1 7 PA1 I23/5
A2 6 PA2 I23/12
EO 15 LPED I23/13
GS 14 LPED
EI 5

5

Level PED Continued



Priority levels and Conditions

Higest EØ , lowest E7

these priority levels are set by the IR decoded data for program flow coding

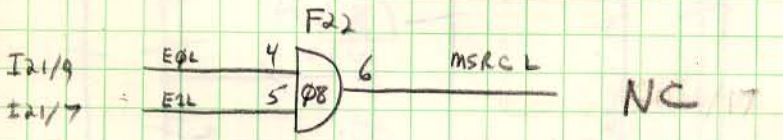
Additionaly - during microcycles not initiating an I/O operation the programmed levels may be cleared and set by microcode control

Clearing - clears all levels EØ-E7

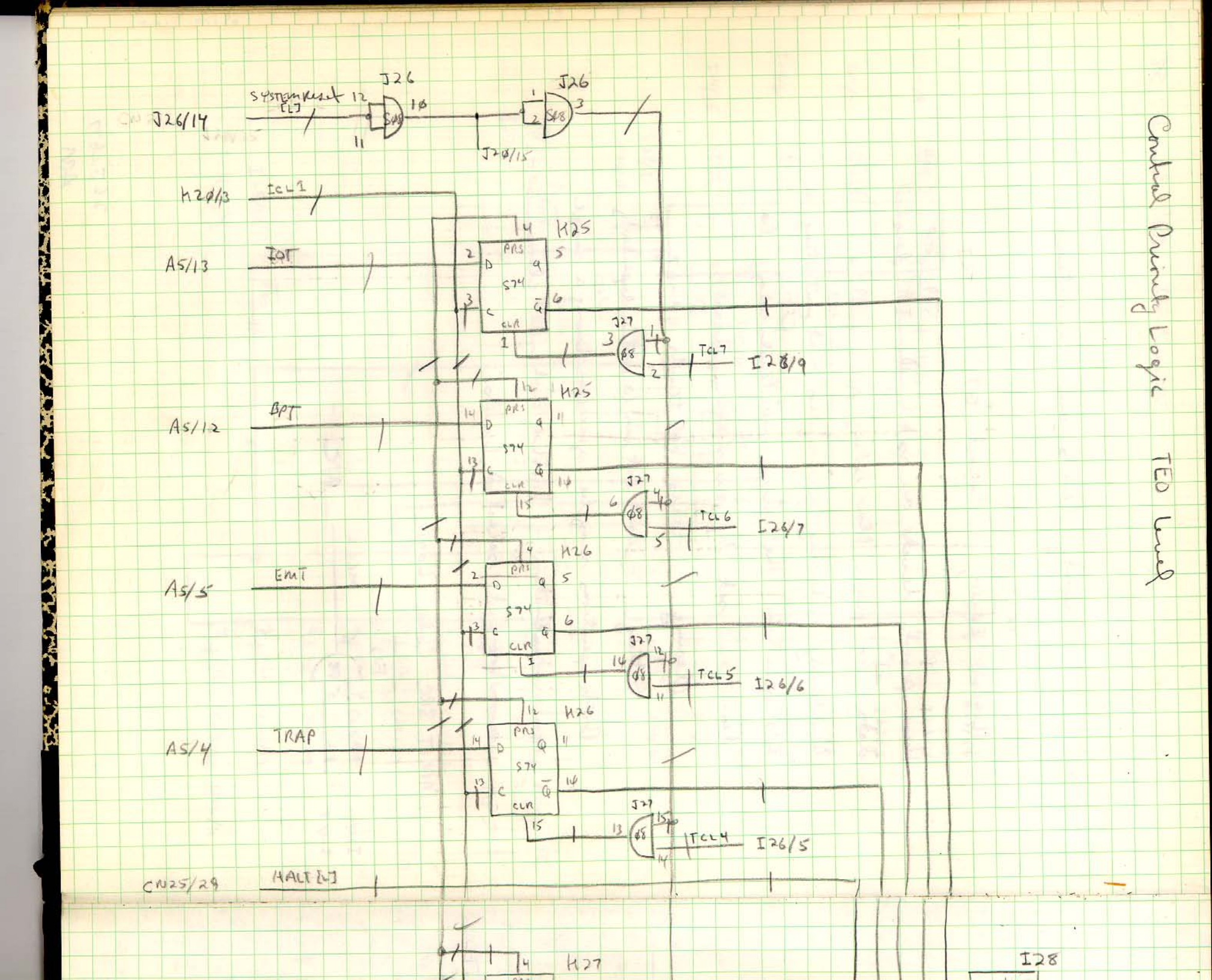
Setting - each bit may be set independently

Both operations may be specified during a single microinstruction - first half clock cycle clears EØ-E7 second half sets selected Levels.

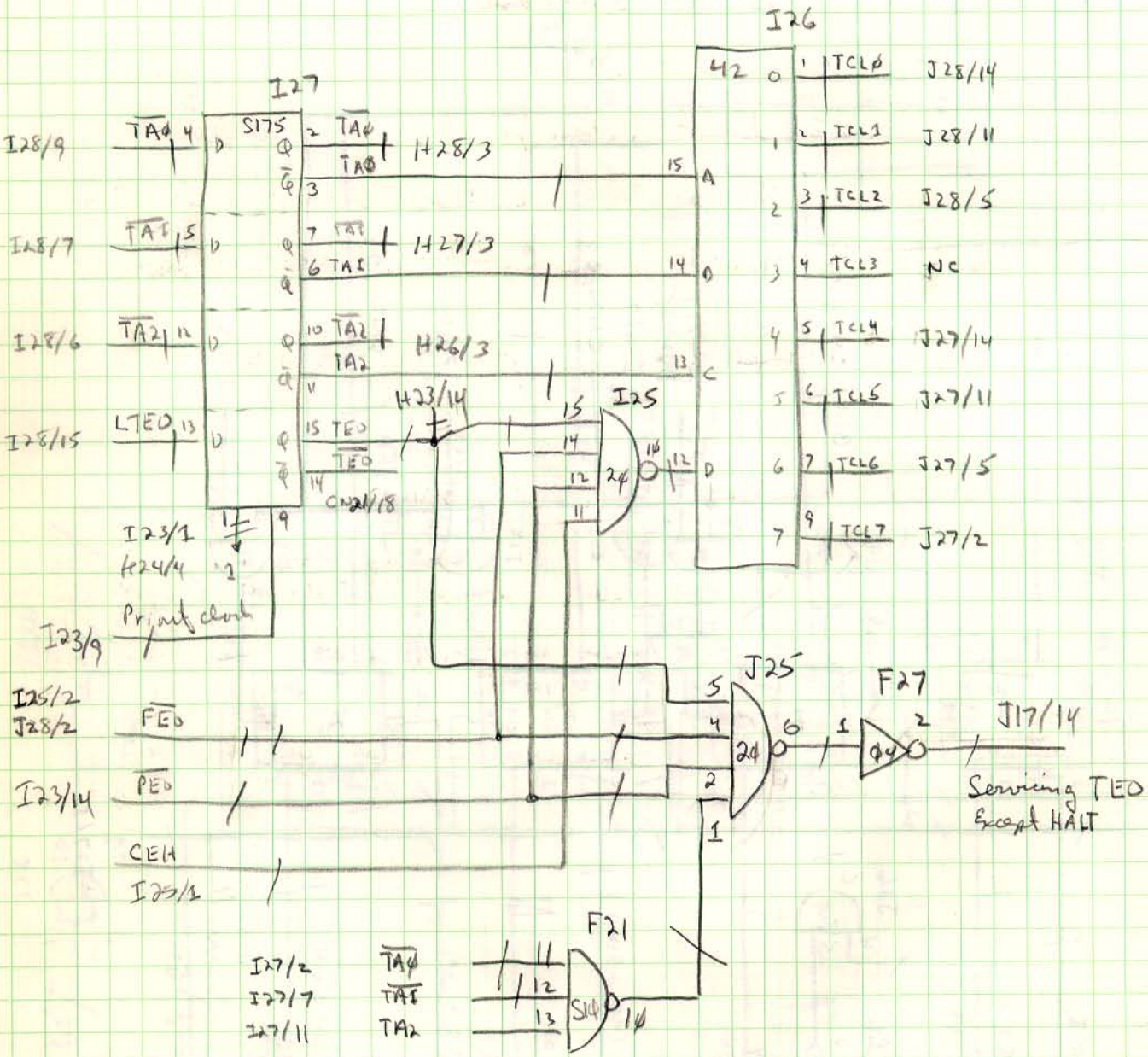
MM6T SRC Code Logic



26 Feb 77
ARB


Control Priority Logic TED Level
J26/14
SYSTEM RESET [L]
J26
J26
J20/15
H20/3
ICL1
H25
A5/13
IOT
J27
TCL7
I20/9
H25
A5/12
BPT
J27
TCL6
I26/7
H26
A5/5
EMT
J27
TCL5
I26/6
H26
A5/4
TRAP
J27
TCL4
I26/5
CN25/29
HALT [L]
H27
I28

Level TEO Continued



Priority levels and Conditions

The TEO level (Trap) has 4 programmed levels BPT, IOT, EMT, TRAP, a Trace level, Yellow Stack and Power fail level plus a Console controlled Halt level.

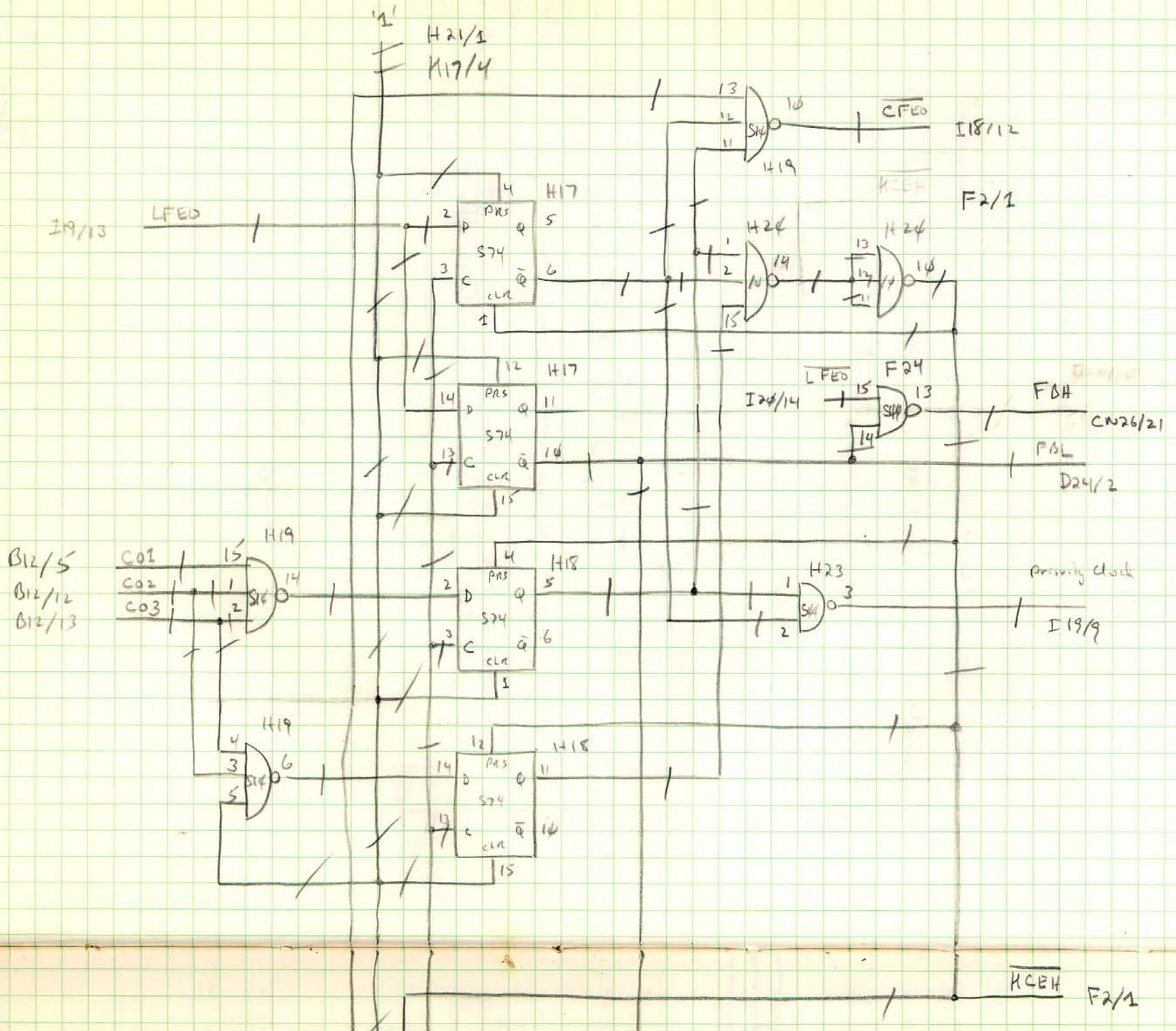
Any FEO trap clears the pending T Trap

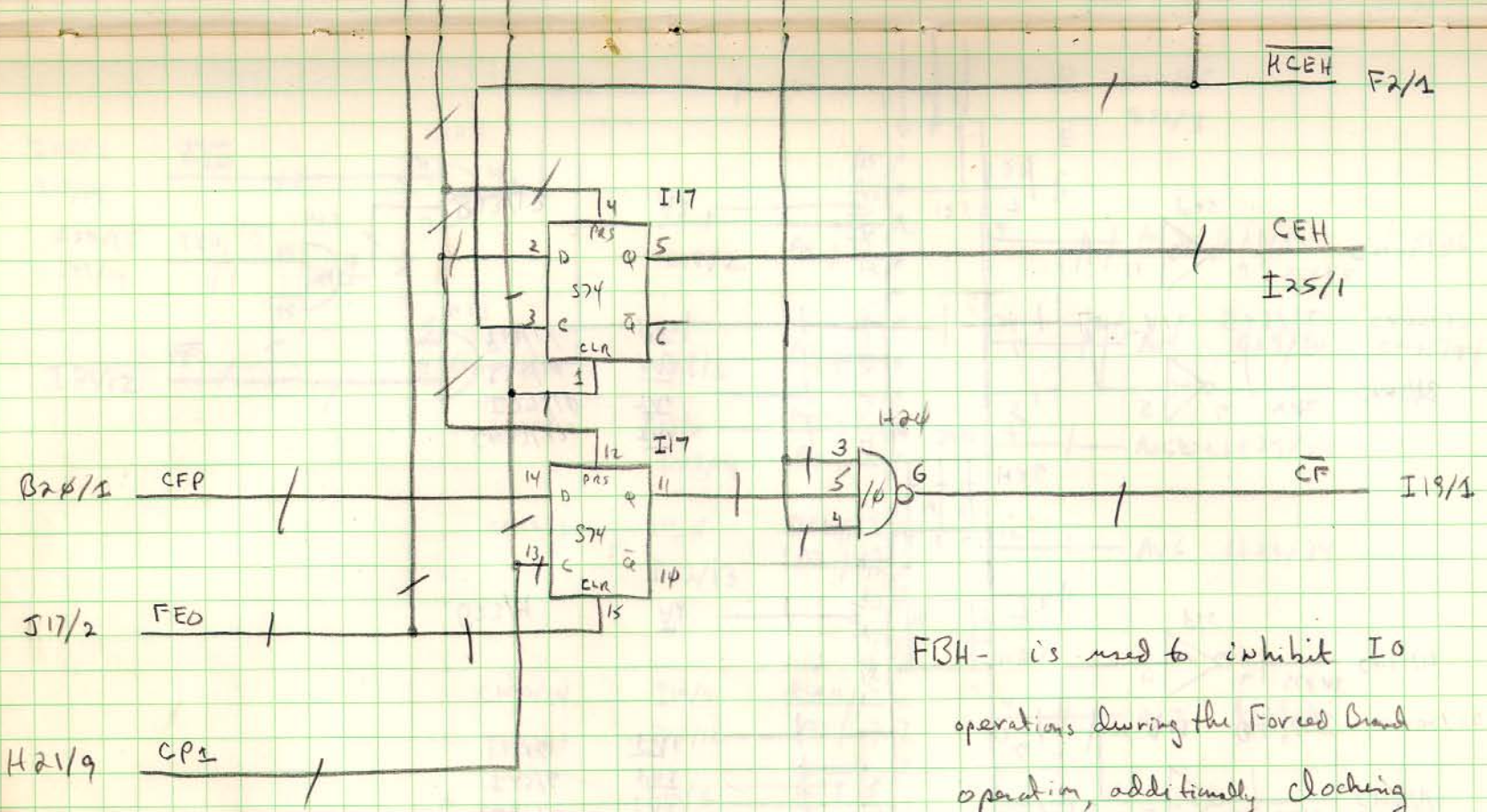
Note: Trace - Trap -

Coding: Trace enabled by IR coding then
a) Trap occurs at end of instruction if T was set before inst.
b) Trap occurs after next instruction if instruction sets T Bit

Special RTI, if T Bit is set during RTI then trap occurs immediately after the RTI

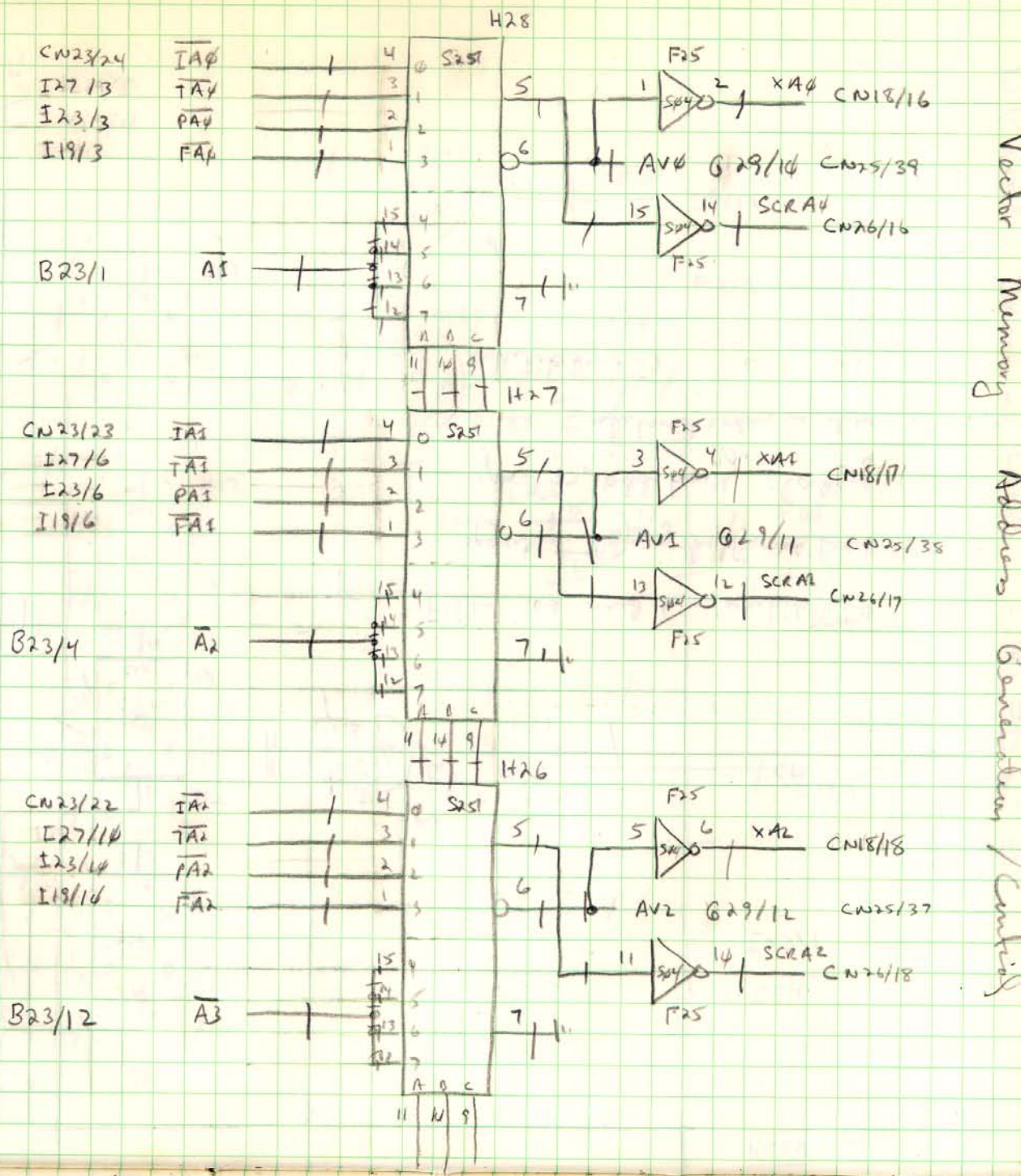
26 Feb 77
ABB


Priority Clocking Logic (FED, PED, and TED)
'1'
H21/1
H17/4
H17
H17
H19
H18
H19
H18
H24
H24
H23
F24
CFED
LFED
LFED
I18/12
F2/1
I9/13
I24/14
FDH
CN26/21
FDL
D24/2
B12/5
B12/12
B12/13
CO1
CO2
CO3
priority clock
I19/9
HCEH
F2/1
PRS
CLR
S74
S10
S11
S14

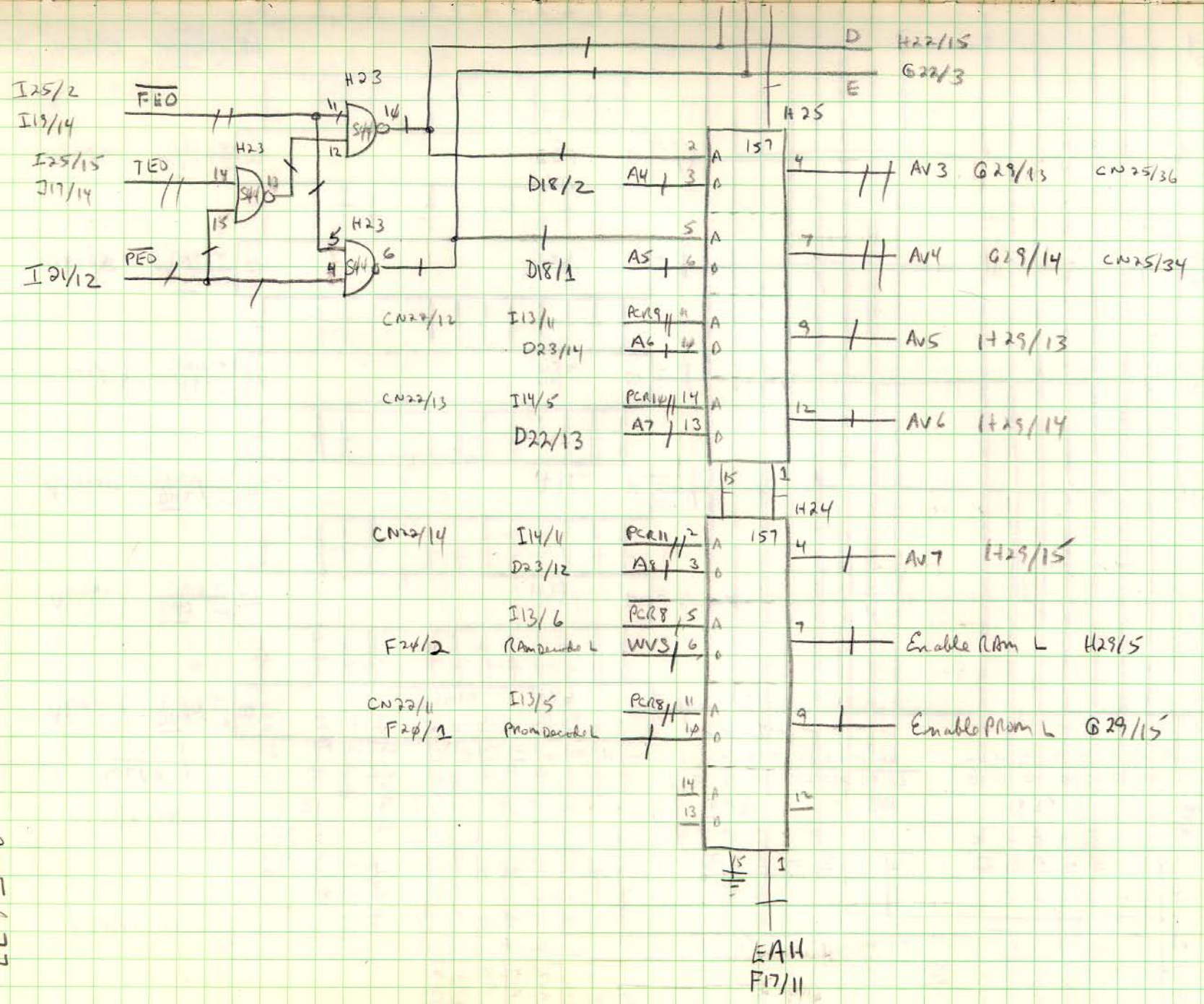


FBH- is used to inhibit IO operations during the Forced Branch operation, additionally clocking of the Conditional codes is also inhibited

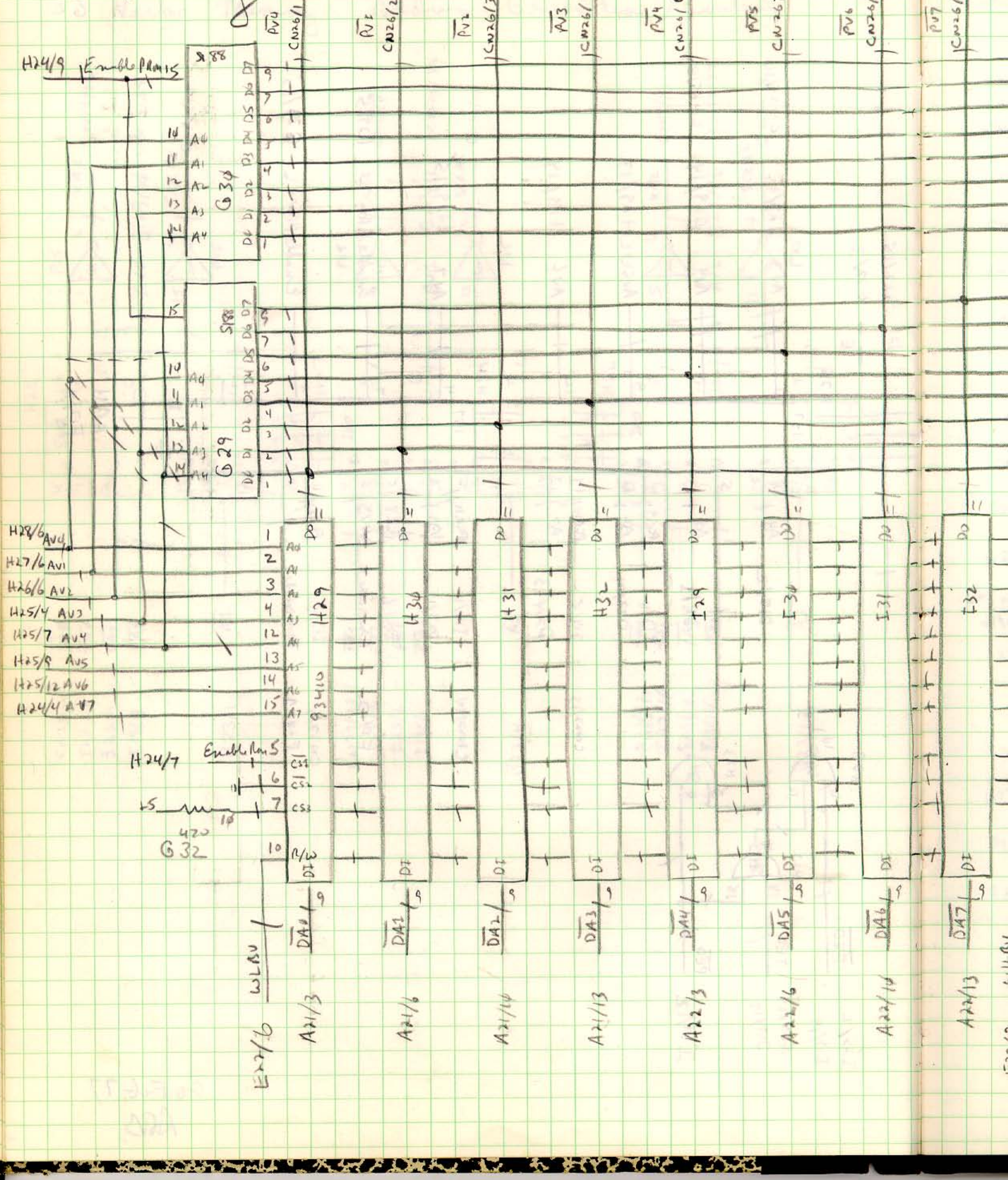
26 FEB 77
ARO

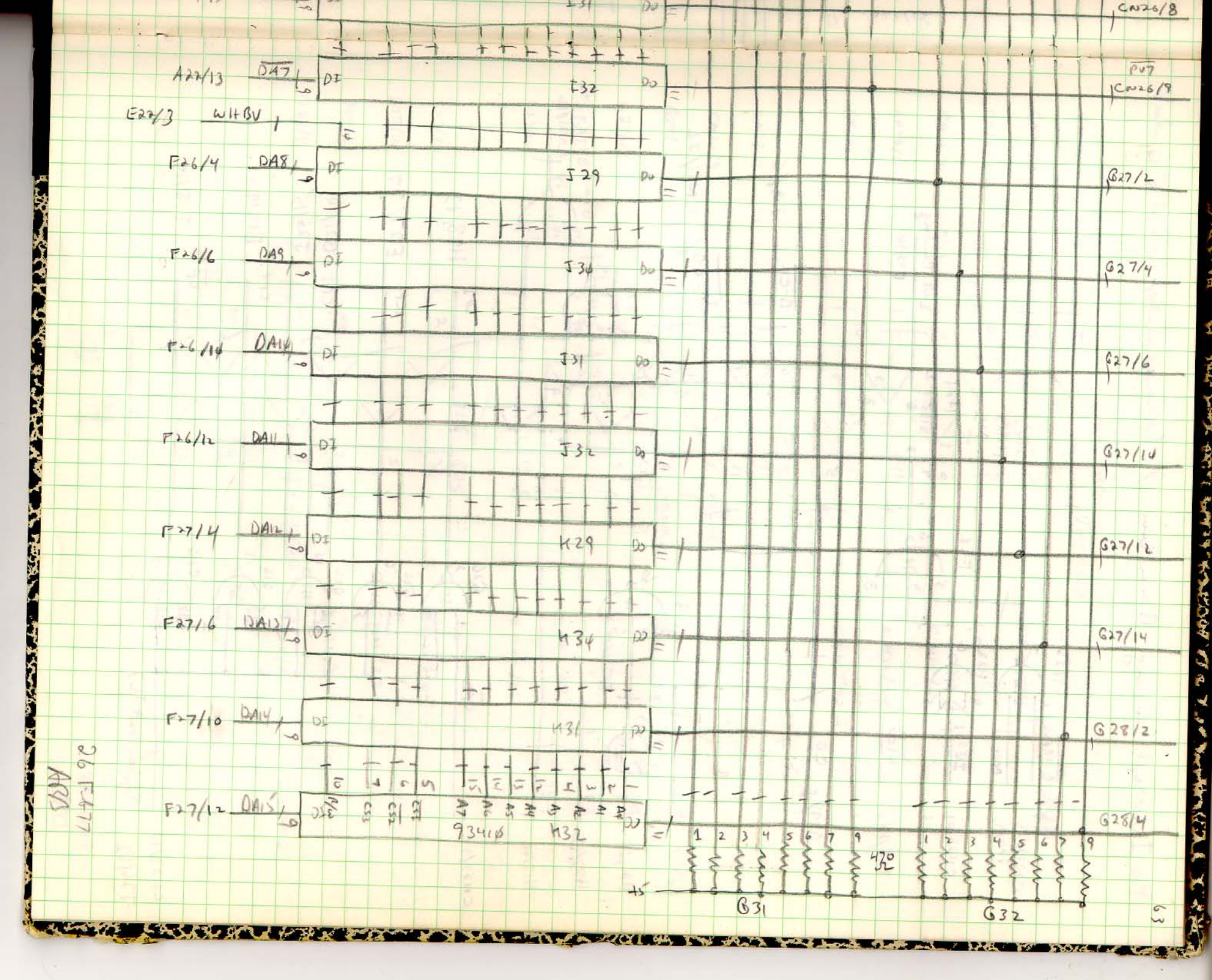


Vector Memory Address Generation / Control

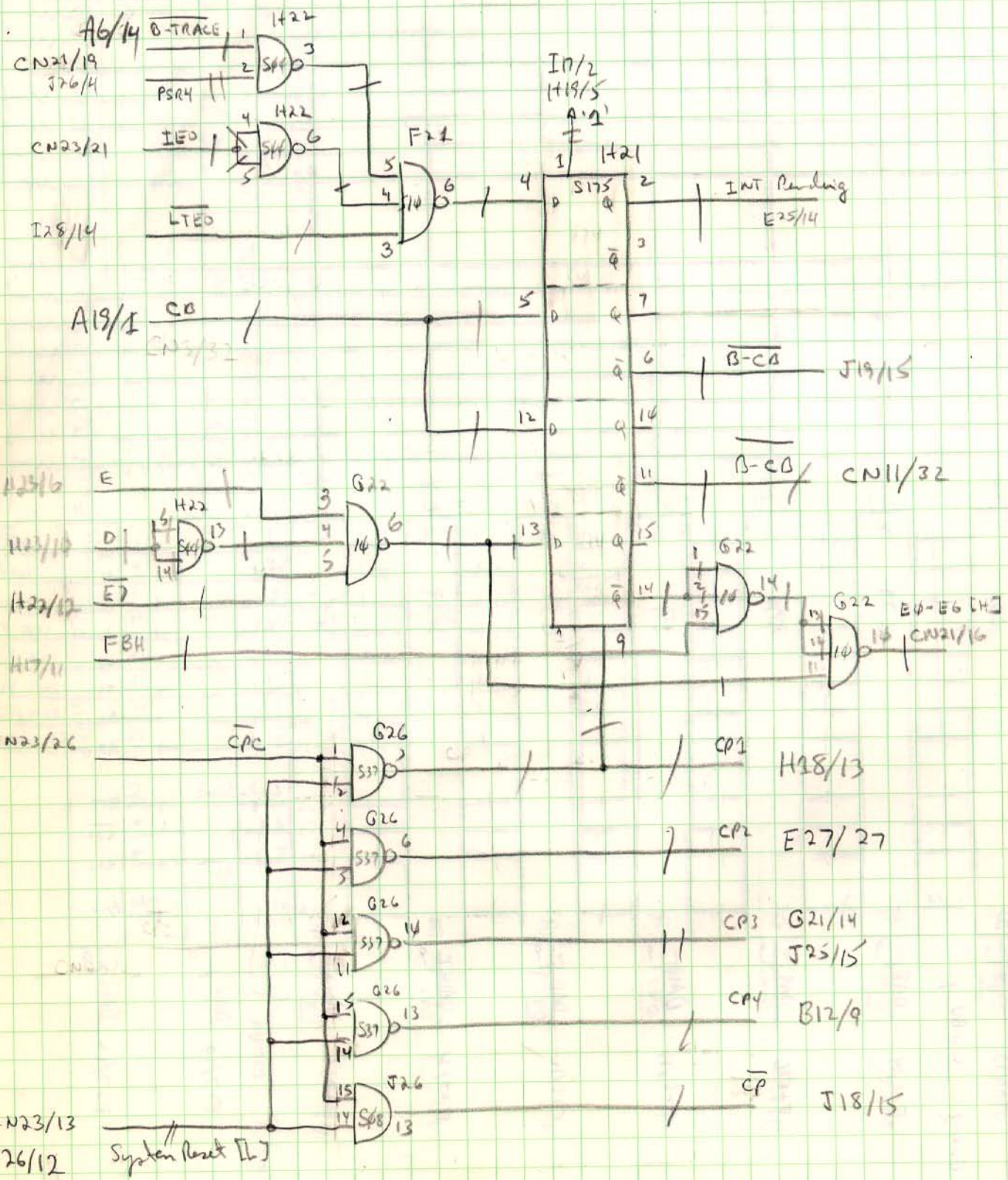

D
H22/15
E
G22/3
H25
H23
I25/2
I19/14
FEO
I25/15
J17/14
TEO
I21/12
PEO
H23
H23
157
A4
A5
A6
A7
A8
D18/2
D18/1
CN22/12
I13/11
D23/14
CN22/13
I14/5
D22/13
AV3
G29/13
CN25/36
AV4
G29/14
CN25/34
AV5
H29/13
AV6
H29/14
H24
CN22/14
I14/4
D23/12
AV7
H29/15
I13/6
F24/2
RAMDecode L
WV3
Enable RAM L
H29/5
CN22/11
F24/1
I13/5
PROMDecode L
Enable PROM L
G29/15
EAH
F17/11
A03
26-627
G2

Vector Memory

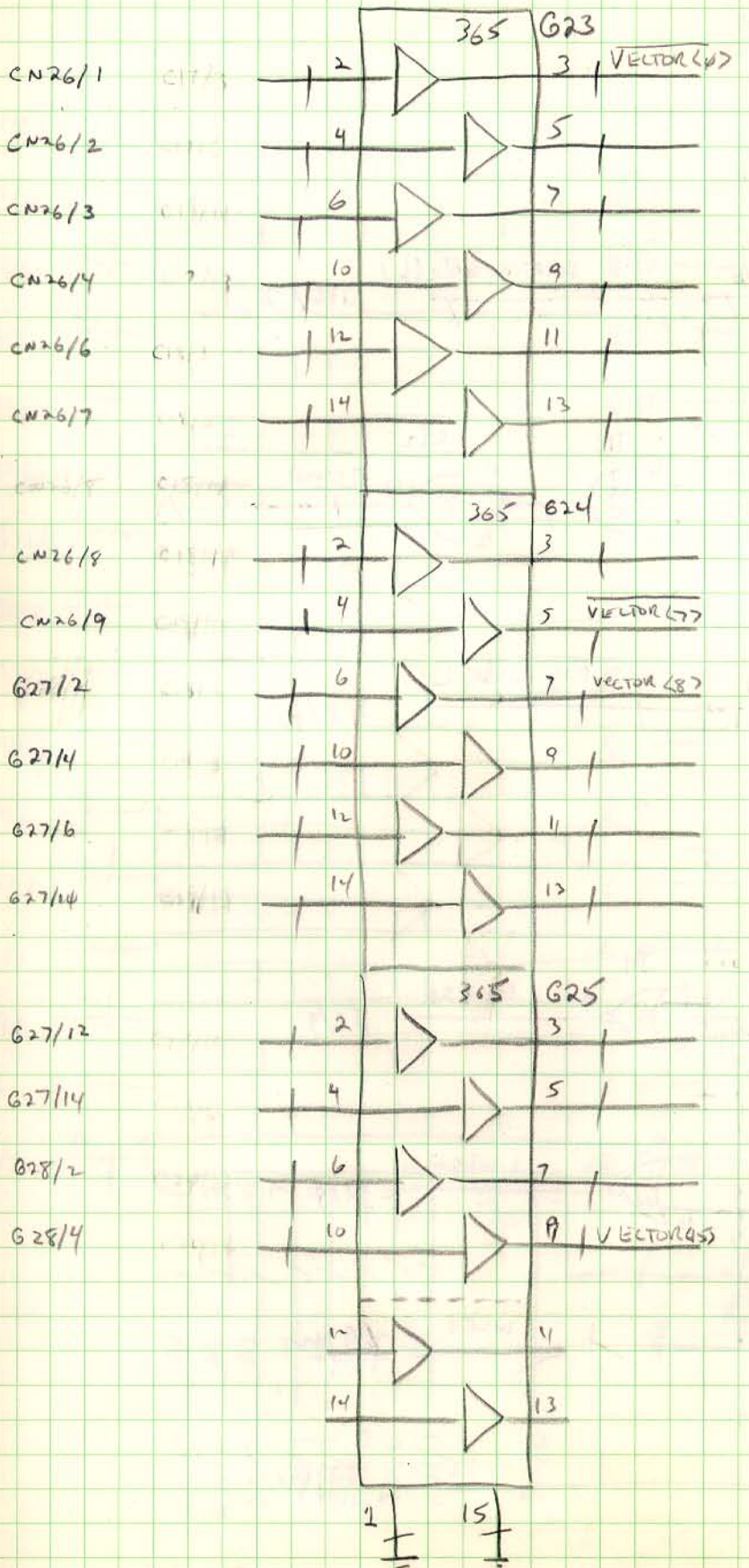



A22/13
DA7
E22/3
WITBV
F26/4
DA8
F26/6
DA9
F26/14
DA10
F26/12
DA11
F27/4
DA12
F27/6
DA13
F27/10
DA14
F27/12
DA15
DI
DO
I32
I29
I30
I31
I32
K29
K34
K31
K32
93410
CN26/8
CN26/9
G27/2
G27/4
G27/6
G27/10
G27/12
G27/14
G28/2
G28/4
470Ω
+5
G31
G32
G3

Interrupt Pending Generation / clock generator



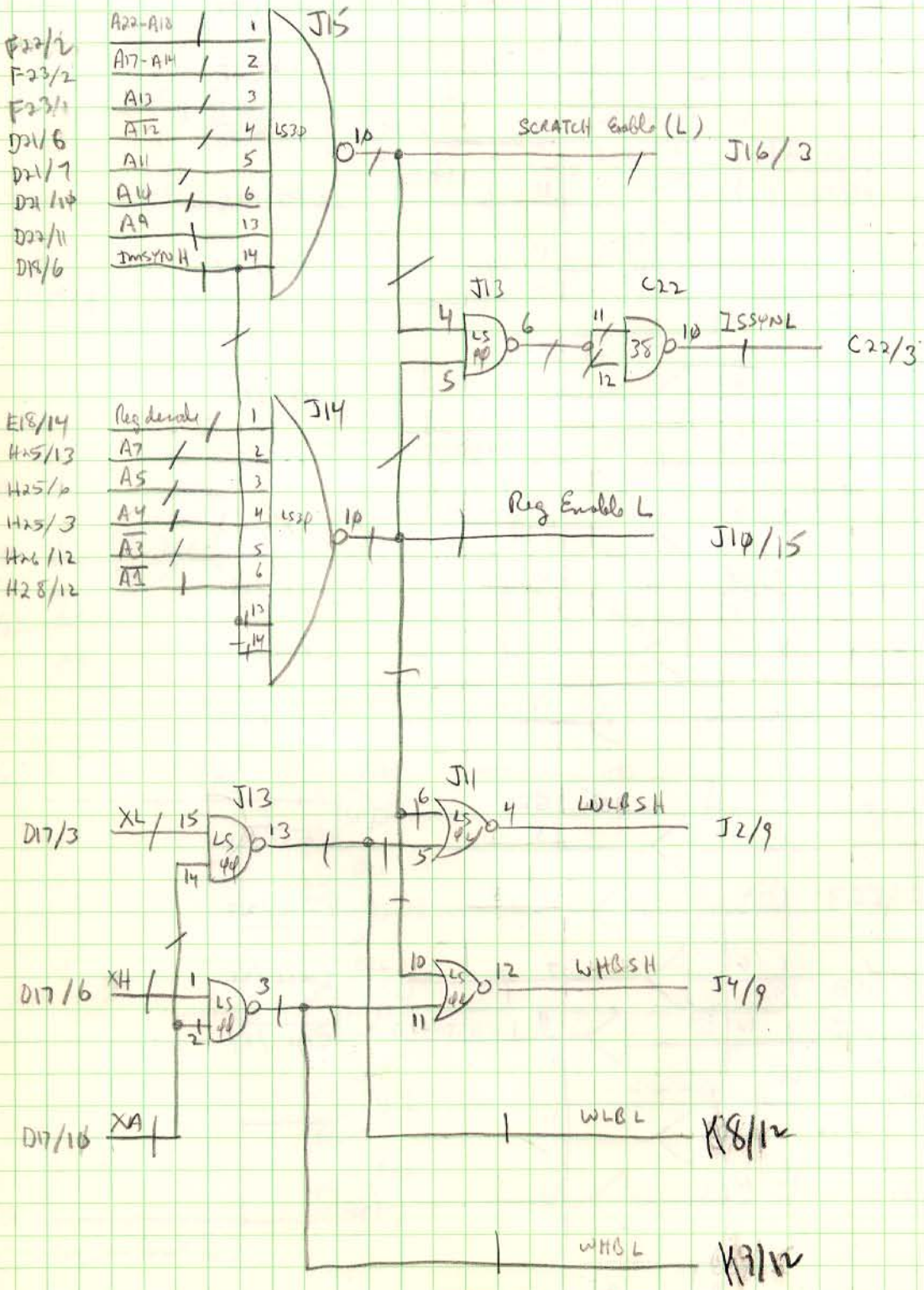
Vector Data Buffer → to Console



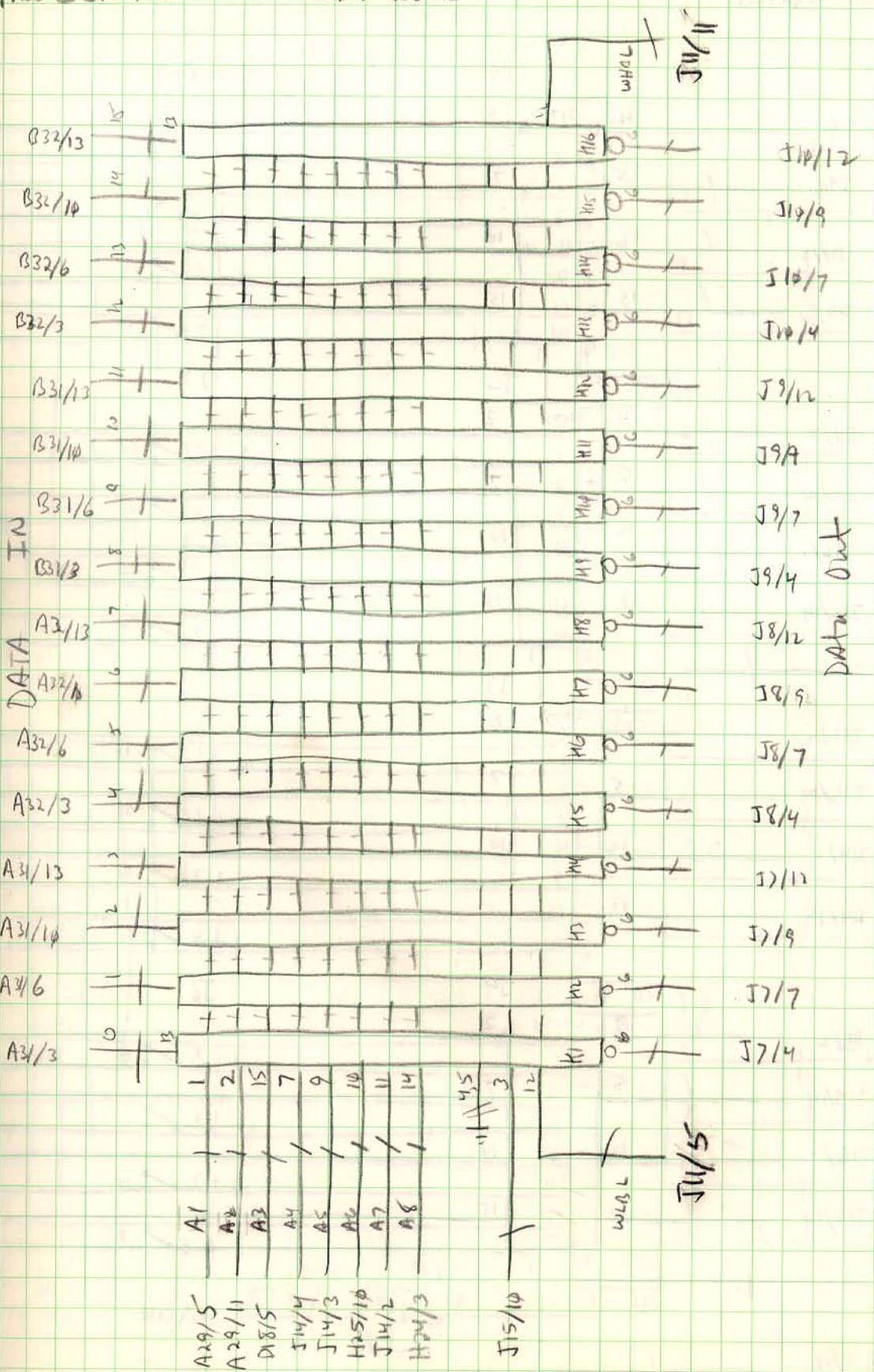
26 Feb 77
AMB

SYSTEM SIZE & MICRO TRAP Registers

FAST SCRATCH Decoding

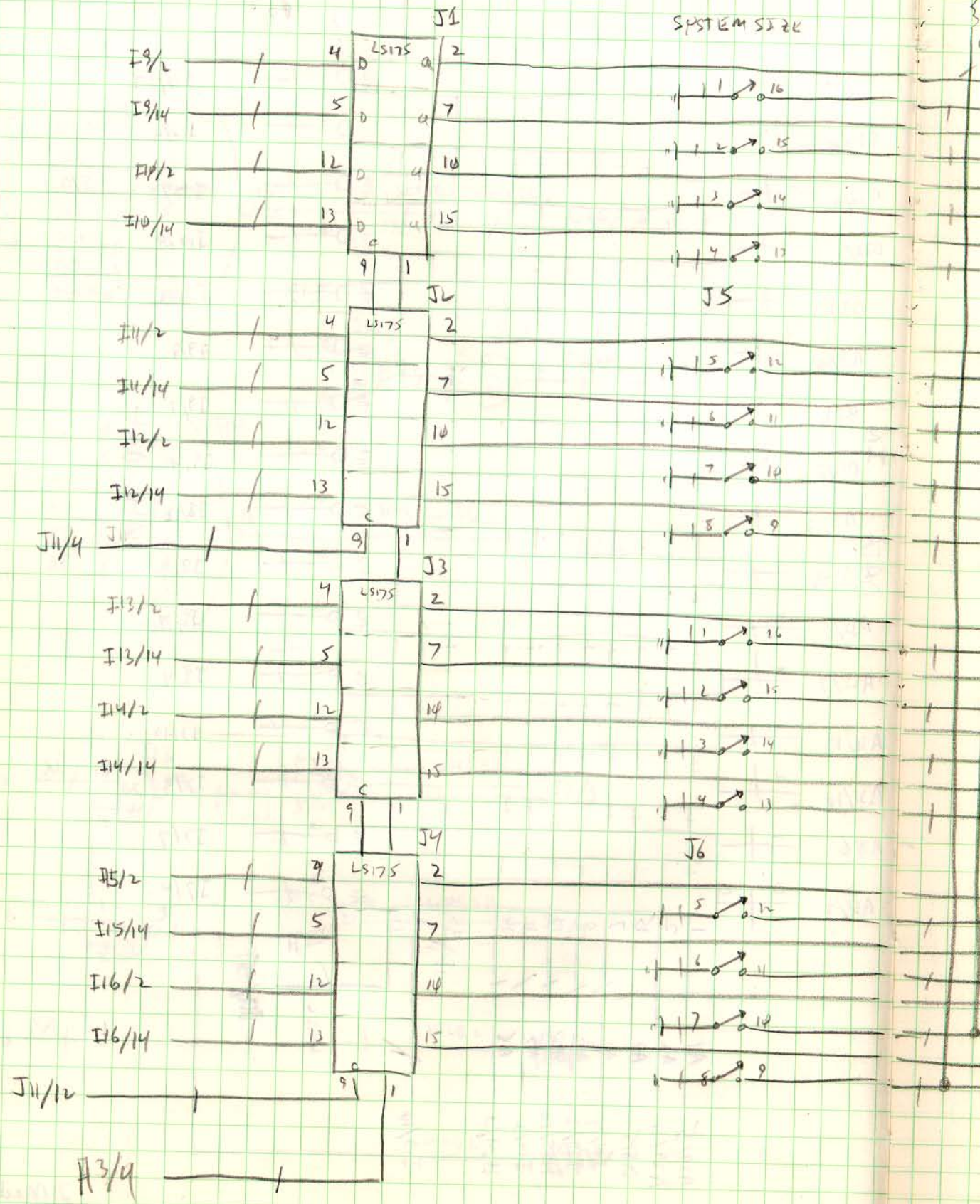


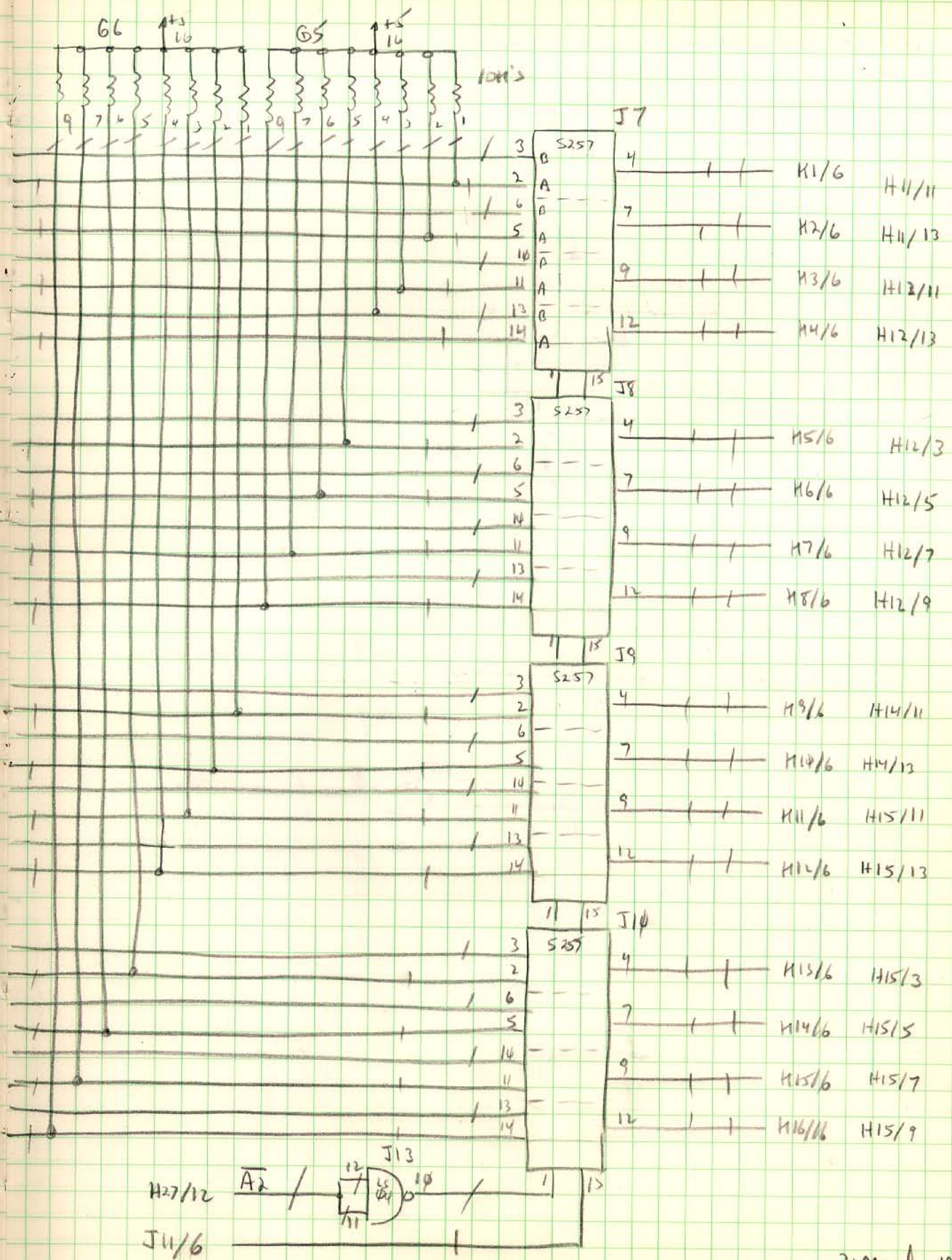
FABS Scratch 256 x16 bit words



21 March 1980
ABB

MICRO TRAP Register





21 March 1980
AAO

Location of integrated circuits by page of appearance

27 F-6-77
AGD

Circuit	Founding pages	Description
A1 (175)	25	
A2 (175)	25	
A3 (175)	25	
A4 (S175)	25	
A5 (175)	26	
A6 (S175)	26	
A7 (175)	26	
A8 (175)	26	
A9 (S175)	27	
A10 (S175)	27	
A11 (S175)	27	
A12 (S175)	27	
A13 (151)	37	
A14 (151)	37	
A15 (151)	37	
A16 (151)	37	

Circuit	found on pages	Description
A17 (151)	38	
A18 (151)	38	
A19 (151)	38	
A20 (151)	38	
A21 (S37)	43	
A22 (S37)	43	
A23 (S37)	44	
A24 (S37)	44, 45	
A25 (S37)	45	
A26 (S37)	44	
A27 (S37)	44, 45	
A28 (S37)	45	
A29 (S37)	42	
A30 (S37)	42	
A31 (S37)	41	
A32 (S37)	41	

27F-677
A50

Circuit		found on page	Description
B1	(150)	22	
B2	NONE		
B3	(150)	22	
B4	(150)	22	
B5	NONE		
B6	(150)	22	
B7	(S04)	19, 24	
B8	(S24)	19	
B9	(S175)	28	
B10	(S175)	28	
B11	(S175)	28	
B12	(S175)	28	
B13	(151)	39	
B14	(151)	39	
B15	(151)	39	
B16	(151)	39	

Circuit	found on page	Description
B17 (151)	40	
B18 (151)	40	
B19 (151)	40	
B20 (151)	40	
B21 (S37)	43	
B22 (S37)	43	
B23 (S37)	40, 47	
B24 (32)	44	
B25 (32)	44, 45	
B26 (32)	45	
B27 (S37)	42	
B28 (S37)	42	
B29 (S37)	42	
B30 (S37)	42	
B31 (S37)	41	
B32 (S37)	41	

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AOB

Circuit	found on page	Description
C1	NONE	
C2	NONE	
C3	NONE	
C4	NONE	
C5	NONE	
C6	NONE	
C7	(148)	24
C8	(S10)	19
C9	(S11)	19
C10	(S11)	19
C11	(S11)	19
C12	(S175)	13
C13	(S175)	13
C14	(S175)	13
C15	(S175)	13
C16	(S21)	19

Circuit		found on pages	Description
C17	(S258)	37	
C18	(S258)	38	
C19	(S257)	39	
C20	(S257)	40	
C21	(S40)	47	
C22	(38)	47, 48	
C23	(S37)	47, 48	
C24	(S24)	54	
C25	(365)	31	
C26	(365)	31	
C27	(150)	52	
C28	NONE		
C29	(150)	52	
C30	(150)	52	
C31	NONE		
C32	---		

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AMB

Circuit		Found on pages	Description
D1	(150)	21	
D2	NONE		
D3	(150)	21	
D4	(150)	21	
D5	NONE		
D6	(150)	21	
D7	(148)	26	
D8	(S16)	19	
D9	(S16)	19, 58	
D10	(S11)	19	
D11	(S11)	19	
D12	(157)	13	
D13	(157)	13	
D14	(157)	13	
D15	(157)	13	
D16	(S08)	13, 14	

Circuit		found in passes	Description
D17	(S37)	47	
D18	(34)	47	
D19	(21)	46	
D20	(20)	46	
D21	(S133)	46	
D22	(S133)	46	
D23	(S133)	46	
D24	(S21)	54	
D25	(153)	53	
D26	(153)	53	
D27	NONE		
D28	NONE		
D29	NONE		
D30	NONE		
D31	NONE		
D32	NONE		

27 F 477
ARB

Circuit		Found on pages	Description
E1	NONE		
E2	(S158)	23	
E3	(S158)	23	
E4	(S158)	23	
E5	(157)	23	
E6	(157)	23	
E7	(175)	24	
E8	(S44)	19	
E9	(S44)	19	
E10	(S86)	14, 46	
E11	(S151)	14	
E12	(175)	13	
E13	(175)	13	
E14	(175)	13	
E15	(175)	13	
E16	NONE		

Circuit		found on pages	Description
E17	NONE		
E18	(04)	46, 47	
E19	(21)	46	
E20	(10)	46, 47	
E21	(20)	47	
E22	(S32)	47, 54	
E23	(S40)	45, 53, 54	
E24	(S16)	50, 54	
E25	(151)	50	
E26	(S86)	50	
E27	(Am2909)	53	
E28	NONE		
E29	(Am2909)	53	
E30	(Am2909)	53	
E31	NONE		
E32	NONE		

27F-477
ARB

Circuit		found on pages	Description
F1	(S64)	24	
F2	(S74)	24	
F3	(Resistors)	24	
F4	(123)	24	
F5	(157)	24	
F6	(S37)	24	
F7	(S74)	24	
F8	(365)	36	
F9	(LS253)	29	
F10	(LS253)	29	
F11	(switches)	34	
F12	NONE		
F13	NONE		
F14	NONE		
F15	NONE		
F16	123	47	

Circuit		Found on pages	Description
F17	(74)	48	
F18	(74)	48	
F19	(04)	48	
F20	(S04)	48	
F21	(S10)	48, 64, 60	
F22	(08)	46	
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F29	NONE		
F30	NONE		
F31	NONE		
F32	(Resistors)	53	

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G8	(365)	34	
G9	(S257)	29	
G10	(S257)	29	
G11	(Switches)	34	
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G13	(S258)	34	
G14	(S258)	34	
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G16	RES	47	

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G17	(Resistors)	48	
G18	(123)	48	
G19	(Resistors)	48	
G20	(123)	48	
G21	(LØØ)	48, 57	
G22	— —		
G23	(365)	64	
G24	(365)	64	
G25	(365)	64	
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H3 (Transistors)	33	
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I11	(74)	35	
I12	(74)	35	
I13	(74)	34	
I14	(74)	34	
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I17	(S74)	61	
I18	(42)	56	
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Circuit	found on page	Description
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J16		

Circuit		found on pages	Description
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J18	(Ø8)	55, 57	
J19	(Ø8)	55	
J20	(Ø8)	55, 57	
J21	(Ø8)	57	
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J23	(Ø8)	57	
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J28	(Ø8)	59	
J29	(93414)	63	
J30	(93414)	63	
J31	(93416)	63	
J32	(93416)	63	

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Circuit	Found on pages	Description
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H3	---	
H4	---	
H5	---	
H6	---	
H7	---	
H8	---	
H9	---	
H10	---	
H11	---	
H12	---	
H13	---	
H14	---	
H15	---	
H16	---	

Circuit		found on page	Description
H17	(S74)	55	
H18	(S74)	55	
H19	(S74)	55	
H20	(S74)	55	
H21	(S74)	57	
H22	(S74)	57	
H23	(S74)	57	
H24	(S74)	57	
H25	(S74)	59	
H26	(S74)	59	
H27	(S74)	59	
H28	(74)	59	
H29	(93410)	63	
H30	(93410)	63	
H31	(93410)	63	
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Special Connector Patches For uninstalled Hardware

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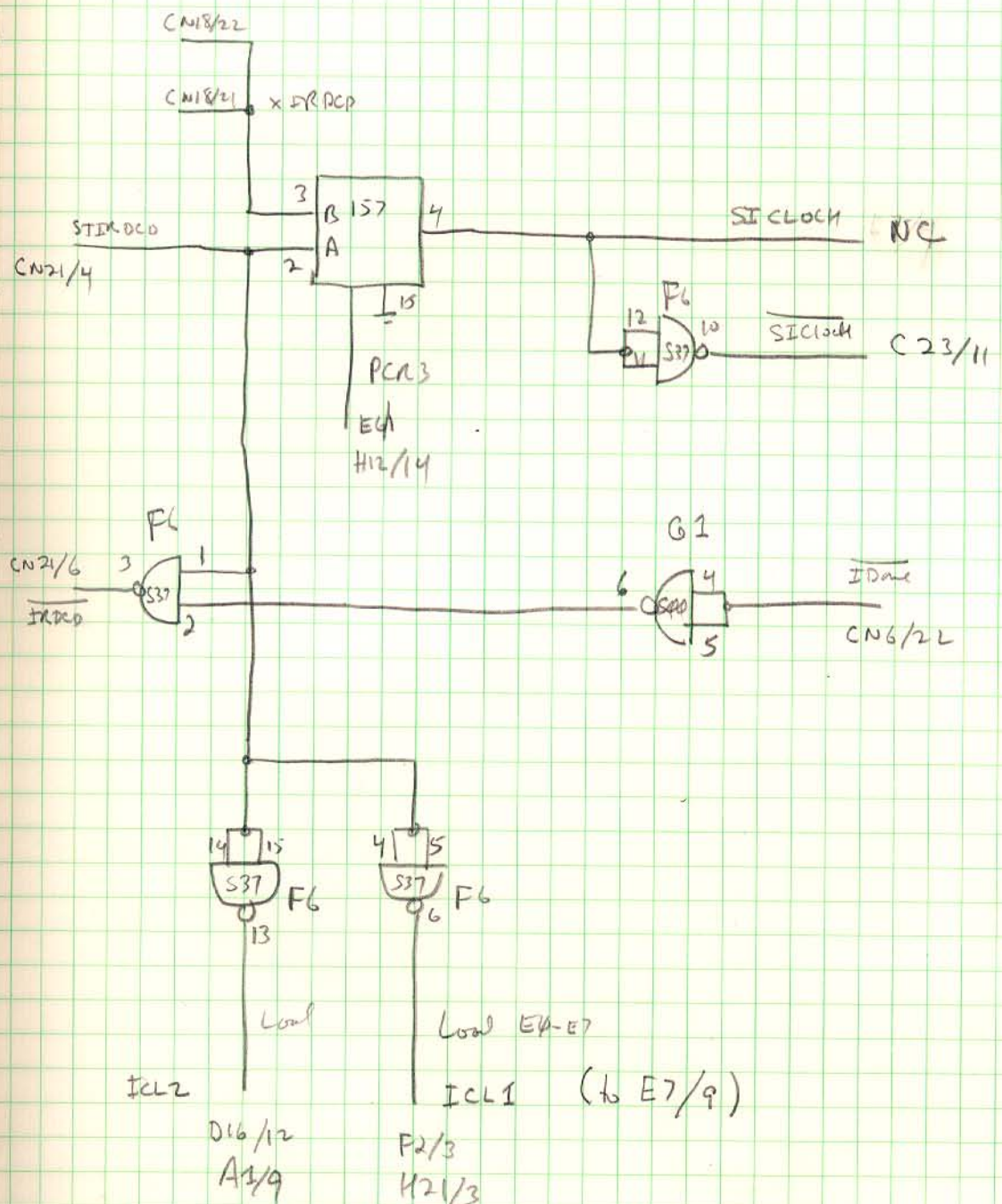
Instruction Address Encoding Timing



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