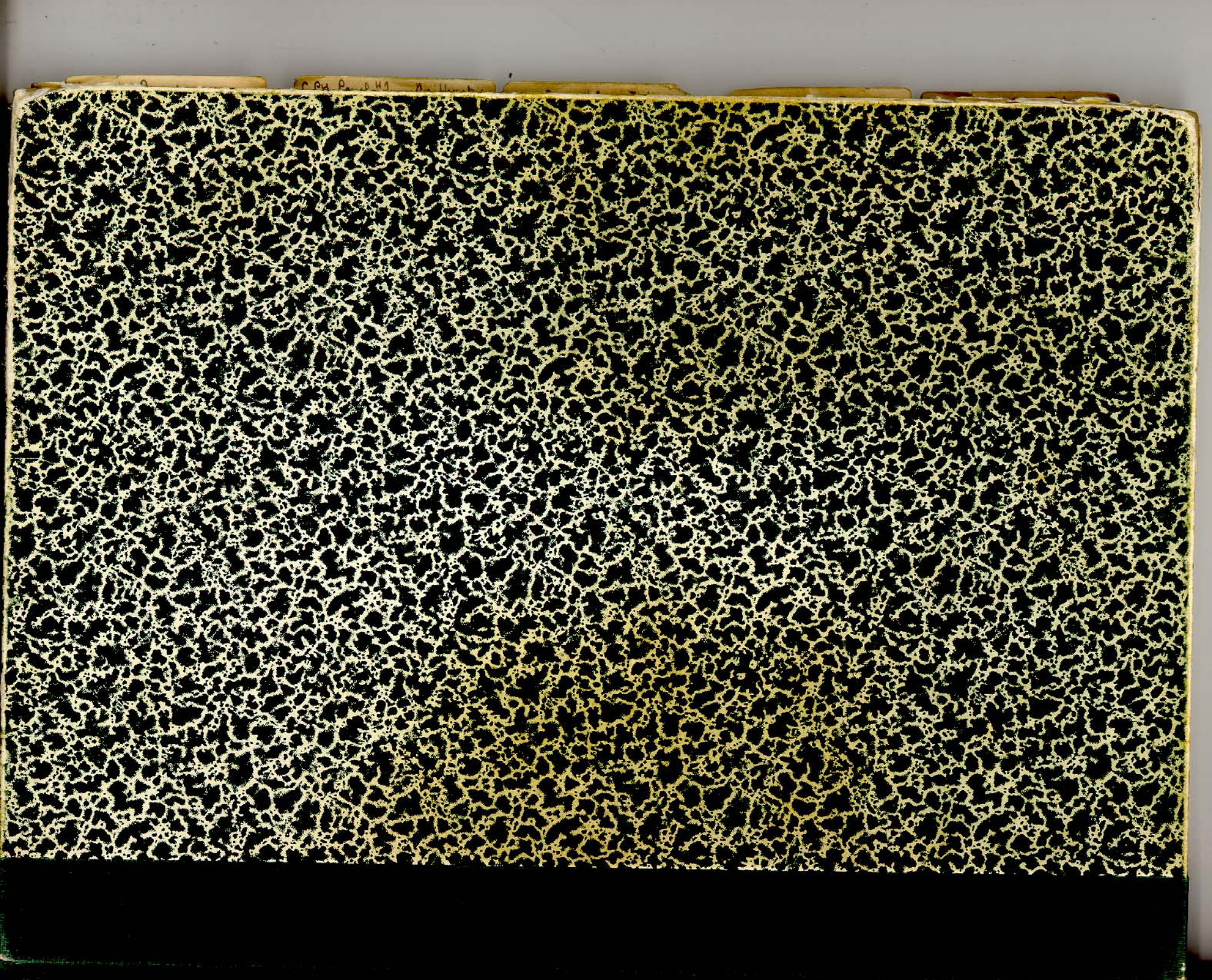
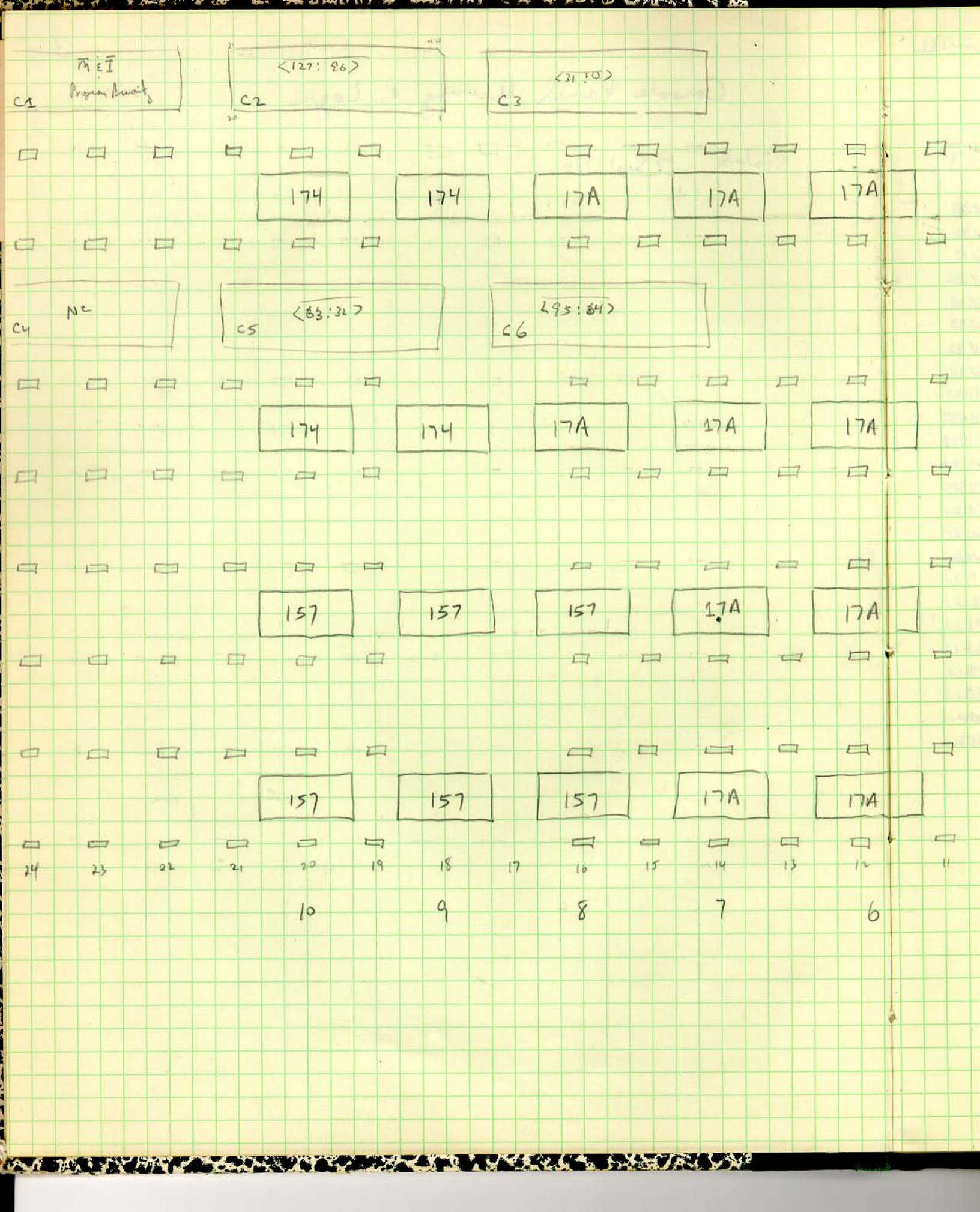


Computer Wiring & Logic

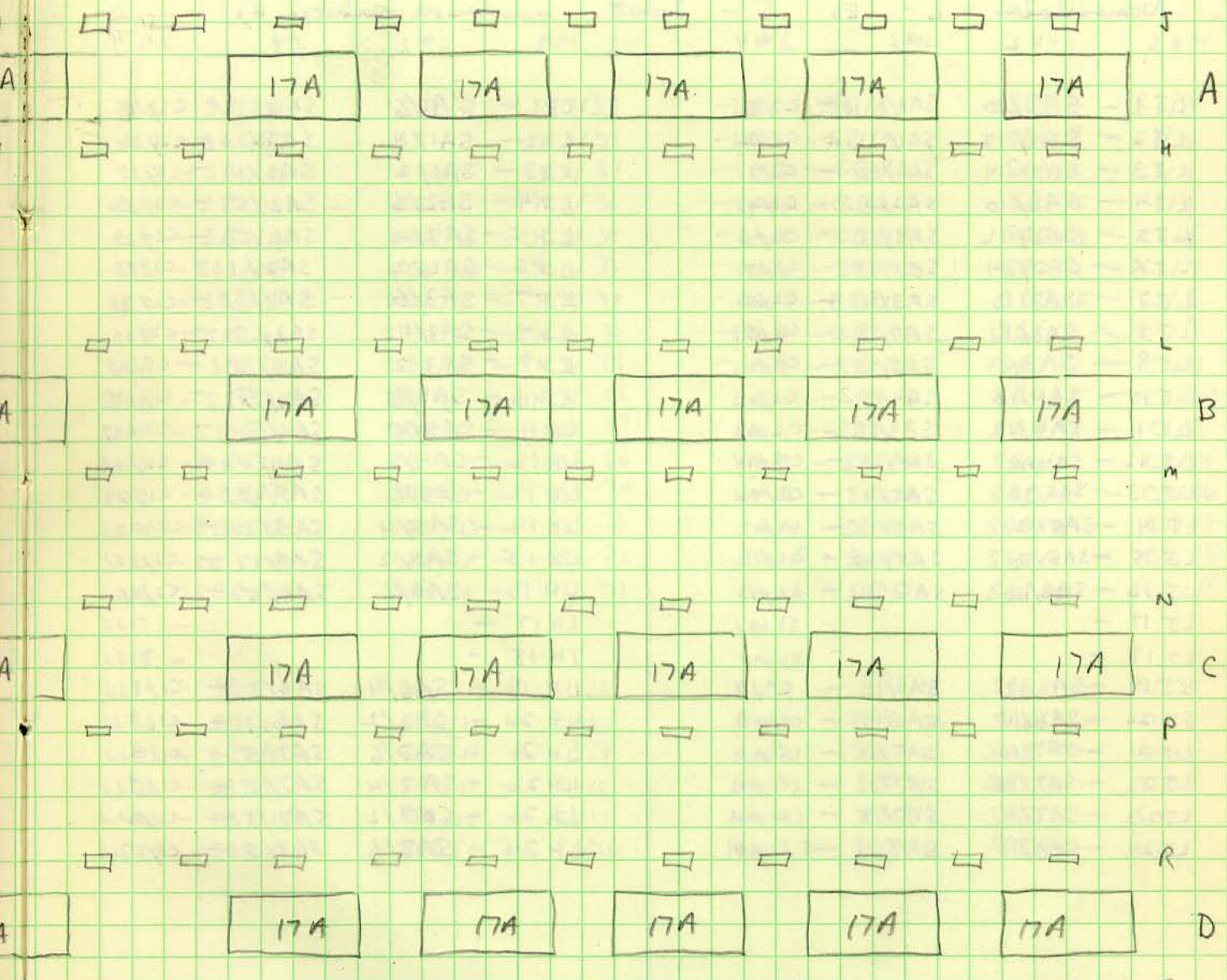
Console Panel Wiring & Logic

Stated 17 Sept 1976


C1
M E I
Program Security
C2
<127:96>
C3
<31:0>
174
174
17A
17A
17A
C4
NC
C5
<63:32>
C6
<95:64>
174
174
17A
17A
17A
157
157
157
17A
17A
157
157
157
17A
17A
24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6

Facing the Socket Side

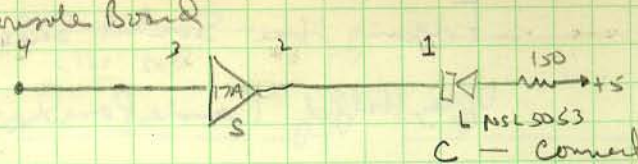
Upper Half of Console Panel



17 Sept 76

BRP

Wiring list



C — Connector #

Nomenclature L - LED ; S - Socket ; numbers are socket pin #'s

#1	#2	#3	#4	#1	#2	#3	#4
LJ1 -	SA1/10	SA1/11	- C2/1	LK1 -	SA1/6	SA1/5	- C2/39
LJ2 -	SA1/12	SA1/13	- C2/2	LK2 -	SA1/4	SA1/3	- C2/38
LJ3 -	SA1/14	SA1/15	- C2/3	LK3 -	SA1/2	SA1/1	- C2/37
LJ4 -	SA2/10	SA2/11	- C2/4	LK4 -	SA2/6	SA2/5	- C2/36
LJ5 -	SA2/12	SA2/13	- C2/6	LK5 -	SA2/4	SA2/3	- C2/34
LJ6 -	SA2/14	SA2/15	- C2/7	LK6 -	SA2/2	SA2/1	- C2/33
LJ7 -	SA3/10	SA3/11	- C2/8	LK7 -	SA3/6	SA3/5	- C2/32
LJ8 -	SA3/12	SA3/13	- C2/9	LK8 -	SA3/4	SA3/3	- C2/31
LJ9 -	SA3/14	SA3/15	- C2/11	LK9 -	SA3/2	SA3/1	- C2/29
LJ10 -	SA4/10	SA4/11	- C2/12	LK10 -	SA4/6	SA4/5	- C2/28
LJ11 -	SA4/12	SA4/13	- C2/13	LK11 -	SA4/4	SA4/3	- C2/27
LJ12 -	SA4/14	SA4/15	- C2/14	LK12 -	SA4/2	SA4/1	- C2/26
LJ13 -	SA5/10	SA5/11	- C2/16	LK13 -	SA5/6	SA5/5	- C2/24
LJ14 -	SA5/12	SA5/13	- C2/17	LK14 -	SA5/4	SA5/3	- C2/23
LJ15 -	SA5/14	SA5/15	- C2/18	LK15 -	SA5/2	SA5/1	- C2/22
LJ16 -	SA6/10	SA6/11	- C2/19	LK16	SA6/6	SA6/5	- C2/21
LJ17 -				LK17 -			
LJ18 -				LK18 -			
LJ19 -	SA6/12	SA6/13	- C1/8	LK19 -	SA6/4	SA6/3	- C1/1
LJ20 -	SA6/14	SA6/15	- C1/9	LK20 -	SA6/2	SA6/1	- C1/2
LJ21 -	SA7/10	SA7/11	- C1/11	LK21 -	SA7/6	SA7/5	- C1/3
LJ22 -	SA7/12	SA7/13	- C1/12	LK22 -	SA7/4	SA7/3	- C1/4
LJ23 -	SA7/14	SA7/15	- C1/13	LK23 -	SA7/2	SA7/1	- C1/6
LJ24 -	SA8/10	SA8/11	- C1/14	LK24 -	SA8/6	SA8/5	- C1/7

Wiring List Console Board

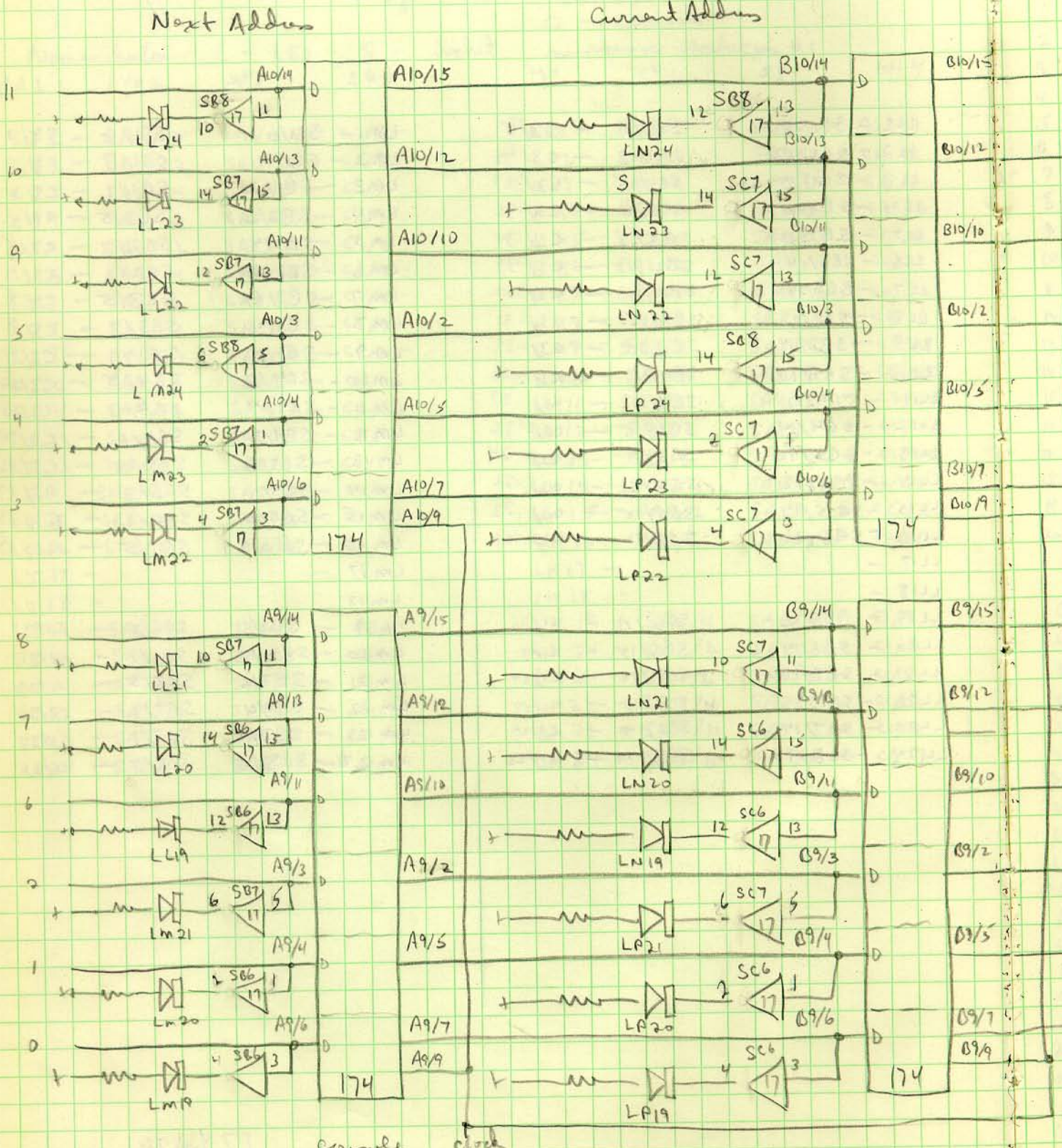
W1	W2	W3	W4
LL1	SB1/10	SB1/11	C3/39
LL2	SB1/12	SB1/13	C3/38
LL3	SB1/14	SB1/15	C3/37
LL4	SB2/10	SB2/11	C3/36
LL5	SB2/12	SB2/13	C3/34
LL6	SB2/14	SB2/15	C3/33
LL7	SB3/10	SB3/11	C3/32
LL8	SB3/12	SB3/13	C3/31
LL9	SB3/14	SB3/15	C3/29
LL10	SB4/10	SB4/11	C3/28
LL11	SB4/12	SB4/13	C3/27
LL12	SB4/14	SB4/15	C3/26
LL13	SB5/10	SB5/11	C3/24
LL14	SB5/12	SB5/13	C3/23
LL15	SB5/14	SB5/15	C3/22
LL16	SB6/10	SB6/11	C3/21
LL17	—		
LL18	—		
LL19	SB6/12	SB6/13	C1/32
LL20	SB6/14	SB6/15	C1/31
LL21	SB7/10	SB7/11	C1/29
LL22	SB7/12	SB7/13	C1/28
LL23	SB7/14	SB7/15	C1/27
LL24	SB8/10	SB8/11	C1/26

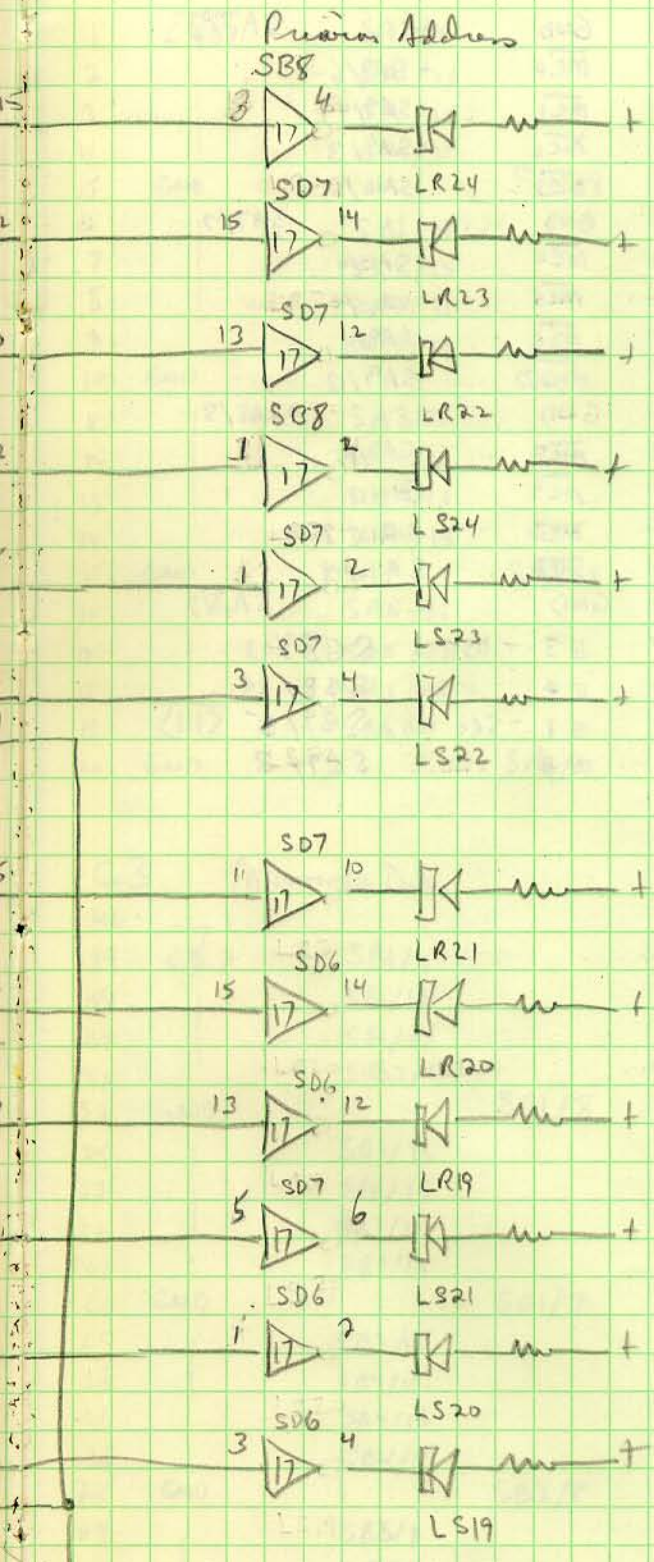
W1	W2	W3	W4
LM1	SB1/6	SB1/5	C3/1
LM2	SB1/4	SB1/3	C3/2
LM3	SB1/2	SB1/1	C3/3
LM4	SB2/6	SB2/5	C3/4
LM5	SB2/4	SB2/3	C3/6
LM6	SB2/2	SB2/1	C3/7
LM7	SB3/6	SB3/5	C3/8
LM8	SB3/4	SB3/3	C3/9
LM9	SB3/2	SB3/1	C3/11
LM10	SB4/6	SB4/5	C3/12
LM11	SB4/4	SB4/3	C3/10
LM12	SB4/2	SB4/1	C3/14
LM13	SB5/6	SB5/5	C3/16
LM14	SB5/4	SB5/3	C3/17
LM15	SB5/2	SB5/1	C3/18
LM16	SB6/6	SB6/5	C3/19
LM17	—		
LM18	—		
LM19	SB6/4	SB6/3	C1/39
LM20	SB6/2	SB6/1	C1/38
LM21	SB7/6	SB7/5	C1/37
LM22	SB7/4	SB7/3	C1/36
LM23	SB7/2	SB7/1	C1/34
LM24	SB8/6	SB8/5	C1/33

17 Sept 76
ABD

CPU Panel #1 Arithmetic
CPU Panel #1 I/O
CPU Panel #1 Selectors
CPU Panel #1 I/O Control

Micro Code Address Display Wiring Console





Resistors 150 ohm
Diods NSL 5053

18 Sept 76
ARD

40 Pin Connectors wiring list

C1

1	$\overline{IC0}$	-	SA6/3
2	$\overline{IC1}$		SA6/1
3	$\overline{IC2}$		SA7/5
4	$\overline{IC3}$		SA7/3
5	GND		SA5/8
6	$\overline{IC4}$		SA7/1
7	$\overline{IC5}$		SA8/5
8	$\overline{IC6}$		SA6/13
9	$\overline{IC7}$		SA6/15
10	GND		SA5/7
11	$\overline{IC8}$		SA7/11
12	$\overline{IC9}$		SA7/13
13	$\overline{IC10}$		SA7/15
14	$\overline{IC11}$		SA8/11
15	GND		SA6/8
16	E7	- RED	SG7/1
17	E6		SG8/5
18	E5	- EX	SG8/3
19	E4		SG8/1
20	GND		SA6/7

40	GND	-	SA7/8
39	$\overline{MC0}$	-	SA9/6
38	$\overline{MC1}$		SA9/4
37	$\overline{MC2}$		SA9/3
36	$\overline{MC3}$		SA10/6
35	GND		SA7/7
34	$\overline{MC4}$		SA10/4
33	$\overline{MC5}$		SA10/3
32	$\overline{MC6}$		SA9/1
31	$\overline{MC7}$		SA9/13
30	GND		SA8/8
29	$\overline{MC8}$		SA9/14
28	$\overline{MC9}$		SA10/11
27	$\overline{MC10}$		SA10/13
26	$\overline{MC11}$		SA10/14
25	GND		SA8/7
24	E3	- DST	SG8/13
23	E2		SG8/15
22	E1	- Sec	SG7/5
21	E0		SG7/3

C2

1	$\overline{C}$
2	
3	
4	
5	GN
6	
7	
8	
9	
10	GN
11	
12	
13	
14	
15	GN
16	
17	
18	
19	$\overline{C}$
20	GN

C3

40	
39	
38	
37	
36	
35	G
34	
33	
32	
31	
30	G
29	
28	
27	
26	
25	
24	
23	
22	
21	
20	

1982 Sept 26
ABJ

C2 I Decode Data

1	<967>	– SA1/11	
2		– SA1/13	
3		SA1/15	
4		SA2/11	
5	GND		SA1/8
6		SA2/13	
7		SA2/15	
8		SA3/11	
9		SA3/13	
10	GND		SA1/7
11		SA3/15	
12		SA4/11	
13		SA4/13	
14		SA4/15	
15	GND		SA2/8
16		SA5/11	
17		SA5/13	
18		SA5/15	
19	<111>	SA6/11	
20	GND		SA2/7
40	GND		SA3/8
39	<112>	– SA1/5	
38		SA1/3	
37		SA1/1	
36		SA2/5	
35	GND		SA3/7
34		SA2/3	
33		SA2/1	
32		SA3/5	
31		SA3/3	
30	GND		SA4/8
29		SA3/1	
28		SA4/5	
27		SA4/3	
26		SA4/1	
25	GND		SA4/7
24		SA5/5	
23		SA5/3	
22		SA5/1	
21	<127>	SA6/5	

C3 Microcode Data

(Jumpers 8-14, 15-31)

40			
39	<ϕ>	– SB1/11	
38		SB1/13	
37		SB1/15	
36		SB2/11	
35	GND		SB1/8
34		SB2/13	
33		SB2/15	
32		SB3/11	
31		SB3/13	
30	GND		SB1/7
29		SB3/15	
28		SB4/11	
27		SB4/13	
26		SB4/15	
25	GND		SB2/8
24		SB5/11	
23		SB5/13	
22		SB5/15	
21	<159>	SB6/11	
20	GND		SB2/7
1	<16	SB1/5	
2		SB1/3	
3		SB1/1	
4		SB2/5	
5	GND		SB3/8
6		SB2/3	
7		SB2/1	
8		SB3/5	
9		SB3/3	
10	GND		SB3/7
11		SB3/1	
12		SB4/5	
13		SB4/3	
14		SB4/1	
15	GND		SB4/8
16		SB5/5	
17		SB5/3	
18		SB5/1	
19	<81>	SB6/5	
20	GND		SB4/7

CPU Panel #1 Arithmetic
CPU Panel #1 I/O
CPU Panel #1 Selectors
CPU Panel #1 I/O Control

Wiring list Cradle Board

#1	#2	#3	#4	#1	#2	#3	#4
LN1	– SC1/10	SC1/11 –	C5/1	LP1	– SC1/6	SC1/5 –	C5/39
LN2	– SC1/12	SC1/13 –	C5/2	LP2	– SC1/4	SC1/3 –	C5/38
LN3	– SC1/14	SC1/15 –	C5/3	LP3	– SC1/2	SC1/1 –	C5/37
LN4	– SC2/10	SC2/11 –	C5/4	LP4	– SC2/6	SC2/5 –	C5/36
LN5	– SC2/12	SC2/13 –	C5/6	LP5	– SC2/4	SC2/3 –	C5/34
LN6	– SC2/14	SC2/15 –	C5/7	LP6	– SC2/2	SC2/1 –	C5/33
LN7	– SC3/10	SC3/11 –	C5/8	LP7	– SC3/6	SC3/5 –	C5/32
LN8	– SC3/12	SC3/13 –	C5/9	LP8	– SC3/4	SC3/3 –	C5/31
LN9	– SC3/14	SC3/15 –	C5/11	LP9	– SC3/2	SC3/1 –	C5/29
LN10	– SC4/10	SC4/11 –	C5/12	LP10	– SC4/6	SC4/5 –	C5/28
LN11	– SC4/12	SC4/13 –	C5/13	LP11	– SC4/4	SC4/3 –	C5/27
LN12	– SC4/14	SC4/15 –	C5/14	LP12	– SC4/2	SC4/1 –	C5/26
LN13	– SC5/10	SC5/11 –	C5/16	LP13	– SC5/6	SC5/5 –	C5/24
LN14	– SC5/12	SC5/13 –	C5/17	LP14	– SC5/4	SC5/3 –	C5/23
LN15	– SC5/14	SC5/15 –	C5/18	LP15	– SC5/2	SC5/1 –	C5/22
LN16	– SC6/10	SC6/11 –	C5/19	LP16	– SC6/6	SC6/5 –	C5/21
LN17	– /			LP17	– /		
LN18	– /			LP18	– /		
LN19	– SC6/12	SC6/13 –	SB9/11	LP19	– SC6/4	SC6/3 –	SB9/6
LN20	– SC6/14	SC6/15 –	SB9/13	LP20	– SC6/2	SC6/1 –	SB9/4
LN21	– SC7/10	SC7/11 –	SB9/14	LP21	– SC7/6	SC7/5 –	SB9/3
LN22	– SC7/12	SC7/13 –	SB10/11	LP22	– SC7/4	SC7/3 –	SB10/6
LN23	– SC7/14	SC7/15 –	SB10/13	LP23	– SC7/2	SC7/1 –	SB10/4
LN24	– SB8/12	SB8/13 –	SB10/14	LP24	– SB8/14	SB8/15 –	SB10/3

Wiring List Console Board

LR1	—	SD1/10	SD1/11	—	C6/1	LS1	—	SD1/6	SD1/5	—	C6/39
LR2	—	SD1/12	SD1/13	—	C6/2	LS2	—	SD1/4	SD1/3	—	C6/38
LR3	—	SD1/14	SD1/15	—	C6/3	LS3	—	SD1/2	SD1/1	—	C6/37
LR4	—	SD2/10	SD2/11	—	C6/4	LS4	—	SD2/6	SD2/5	—	C6/36
LR5	—	SD2/12	SD2/13	—	C6/6	LS5	—	SD2/4	SD2/3	—	C6/34
LR6	—	SD2/14	SD2/15	—	C6/7	LS6	—	SD2/2	SD2/1	—	C6/33
LR7	—	SD3/10	SD3/11	—	C6/8	LS7	—	SD3/6	SD3/5	—	C6/32
LR8	—	SD3/12	SD3/13	—	C6/9	LS8	—	SD3/4	SD3/3	—	C6/31
LR9	—	SD3/14	SD3/15	—	C6/11	LS9	—	SD3/2	SD3/1	—	C6/29
LR10	—	SD4/10	SD4/11	—	C6/12	LS10	—	SD4/6	SD4/5	—	C6/28
LR11	—	SD4/12	SD4/13	—	C6/13	LS11	—	SD4/4	SD4/3	—	C6/27
LR12	—	SD4/14	SD4/15	—	C6/14	LS12	—	SD4/2	SD4/1	—	C6/26
LR13	—	SD5/10	SD5/11	—	C6/16	LS13	—	SD5/6	SD5/5	—	C6/24
LR14	—	SD5/12	SD5/13	—	C6/17	LS14	—	SD5/4	SD5/3	—	C6/23
LR15	—	SD5/14	SD5/15	—	C6/18	LS15	—	SD5/2	SD5/1	—	C6/22
LR16	—	SD6/10	SD6/11	—	C6/19	LS16	—	SD6/6	SD6/5	—	C6/21
LR17	/					LS17	/				
LR18	/					LS18	/				
LR19	—	SD6/12	SD6/13	—	SB9/10	LS19	—	SD6/4	SD6/3	—	SB9/7
LR20	—	SD6/14	SD6/15	—	SB9/12	LS20	—	SD6/2	SD6/1	—	SB9/5
LR21	—	SD7/10	SD7/11	—	SB9/15	LS21	—	SD7/6	SD7/5	—	SB9/2
LR22	—	SD7/12	SD7/13	—	SB10/10	LS22	—	SD7/4	SD7/3	—	SB10/7
LR23	—	SD7/14	SD7/15	—	SB10/12	LS23	—	SD7/2	SD7/1	—	SB10/5
LR24	—	SB8/4	SB8/3	—	SB10/15	LS24	—	SB8/2	SB8/1	—	SB10/2

20 Sept 26
ARD

CPU Panel #1 Arithmetic

CPU Panel #1 I/O

CPU Panel #1 Selectors

CPU Panel #1 I/O Control

C5 Buffered Microcode <63:32>

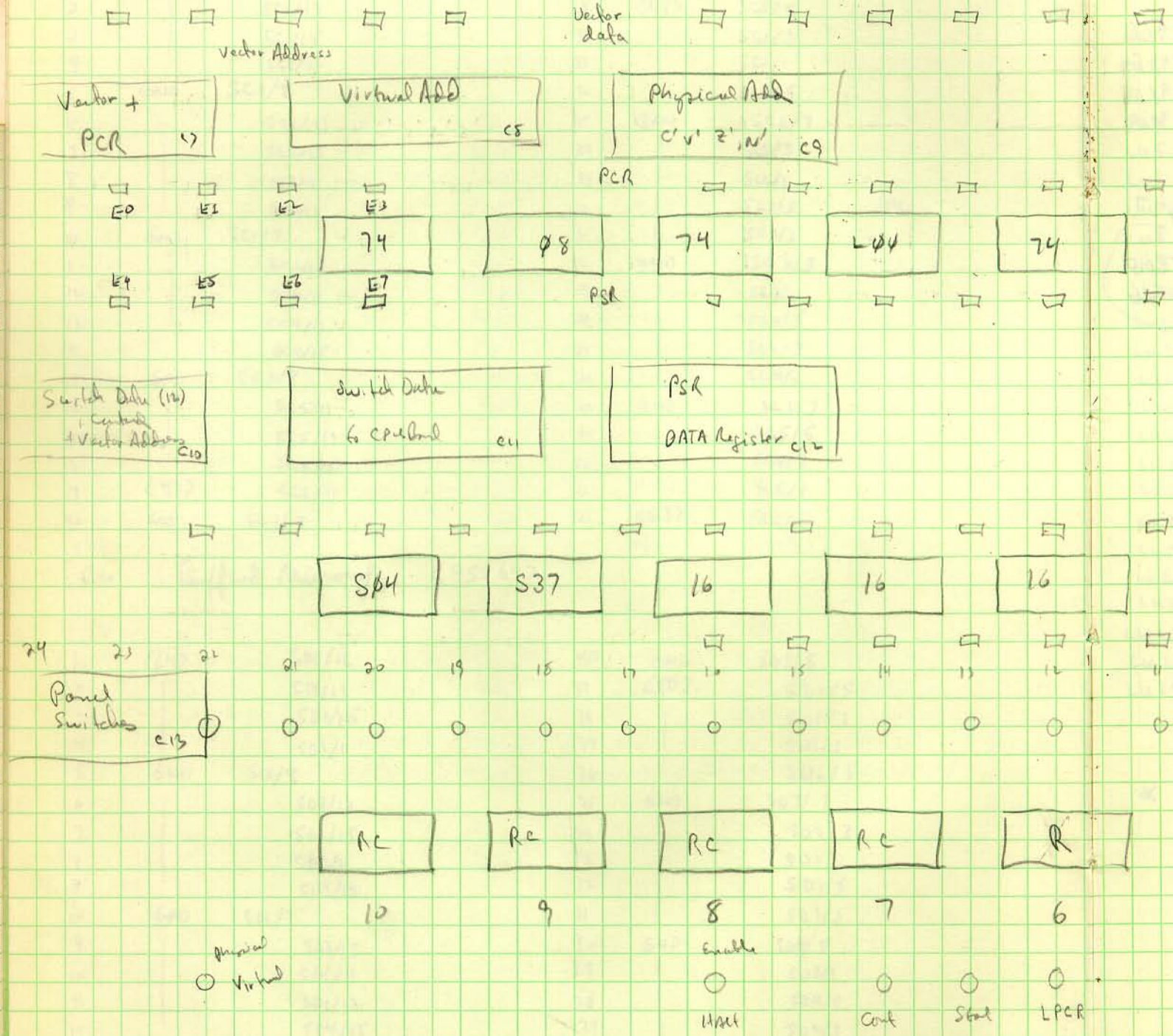
1	<32>	SC1/11
2		SC1/13
3		SC1/15
4		SC2/11
5	GND	SC1/8
6		SC2/13
7		SC2/15
8		SC3/11
9		SC3/13
10	GND	SC1/7
11		SC3/15
12		SC4/11
13		SC4/13
14		SC4/15
15	GND	SC3/8
16		SC5/11
17		SC5/13
18		SC5/15
19	<47>	SC6/11
20	GND	SC3/7
40	GND	SC2/8
39	<48>	SC1/5
38		SC1/3
37		SC1/1
36		SC2/5
35	GND	SC2/7
34		SC2/3
33		SC2/1
32		SC3/5
31		SC3/3
30	GND	SC2/8
29		SC3/1
28		SC4/5
27		SC4/3
26		SC4/1
25	GND	SC2/7
24		SC5/5
23		SC5/3
22		SC5/1
21	<63>	SC6/5

54

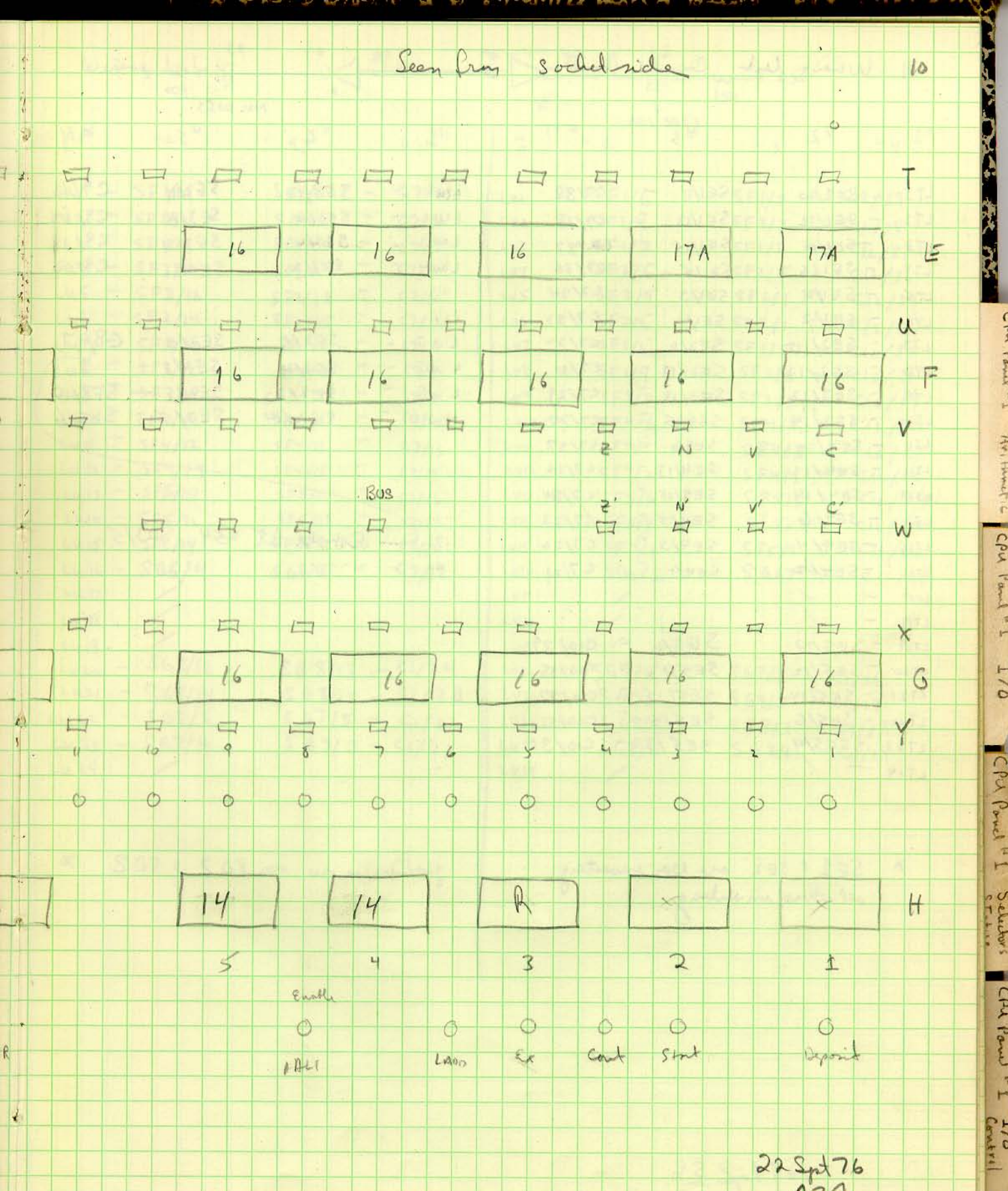
C6 Buffered Microcode <95:64>

1	<64>	SD1/11
2		SD1/13
3		SD1/15
4		SD2/11
5	GND	SD1/8
6		SD2/13
7		SD2/15
8		SD3/11
9		SD3/13
10	GND	SD1/7
11		SD3/15
12		SD4/11
13		SD4/13
14		SD4/15
15	GND	SD2/8
16		SD5/11
17		SD5/13
18		SD5/15
19	<79>	SD6/11
20	GND	SD2/7
40	GND	SD3/8
39	<80>	SD1/5
38		SD1/3
37		SD1/1
36		SD2/5
35	GND	SD3/7
34		SD2/3
33		SD2/1
32		SD3/5
31		SD3/3
30	GND	SD4/8
29		SD3/1
28		SD4/5
27		SD4/3
26		SD4/1
25	GND	SD4/7
24		SD5/5
23		SD5/3
22		SD5/1
21	<95>	SD6/5

Console Panel Lower Half



Seen from socket side



22 Sept 76
ABD

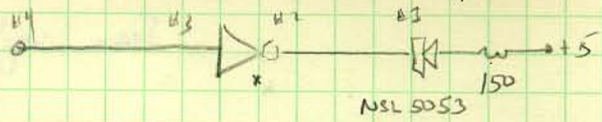
CPU Panel #1 Arithmetic

CPU Panel #1 I/O

CPU Panel #1 Selectors Status

CPU Panel #1 I/O Control

Wiring list Console Board



#1	#2	#3	#4
LT1	– SE1/10	SE1/11 –	C7/39
LT2	– SE1/12	SE1/13 –	C7/38
LT3	– SE1/14	SE1/15 –	C7/37
LT4	– SE1/6	SE1/5 –	C7/36
LT5	– SE1/4	SE1/3 –	C7/34
LT6	– SE1/2	SE1/1 –	C7/33
LT7	– SE2/10	SE2/11 –	C7/32
LT8	– SE2/12	SE2/13 –	C7/31
LT9	– SE3/12	SE3/13 –	C7/29
LT10	– SE3/14	SE3/15 –	C7/28
LT11	– SE4/10	SE4/11	C7/27
LT12	– SE4/12	SE4/13 –	C7/26
LT13	– SE4/14	SE4/15 –	C7/24
LT14	– SE4/6	SE4/5 –	C7/23
LT15	– SE4/4	SE4/3 –	C7/22
LT16	– SE4/2	SE4/1 –	C7/21
LT17	– /		
LT18	– /		
LT19	– SE5/10	SE5/11 –	C10/39
LT20	– SE5/12	SE5/13 –	C10/38
LT21	– SE5/14	SE5/15 –	C10/37
LT22	– SE5/6	SE5/5 –	C10/36
LT23	– SE5/4	SE5/3 –	C10/34
LT24	– /		

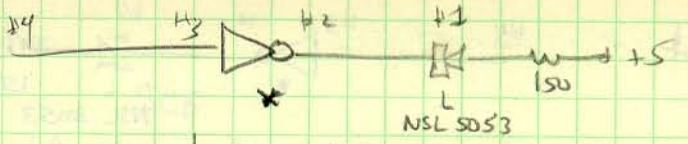
#1	#2	#3	#4
LW1 –	SE3/10	SE3/11	C9/16
LW2 –	SE3/6	SE3/5	C9/17
LW3 –	SE3/4	SE3/3	C9/18
LW4 –	SE3/2	SE3/1	C9/19
LW7 –	SE2/6	SE2/5 –	C8/17
LW8 –	SE2/4	SE2/3 –	
LW9 –	SE2/2	SE2/1 –	SF8/10
LW10 –	SE2/14	SE2/15 –	SH5/6

(SE2/3 –) Console list #54 SC3/5

#1
Lu1
Lu2
Lu3
Lu4
Lu5
Lu6
Lu7
Lu8
Lu9

* SE1 & SE2 are Non inverting
all others inverting

Wiring List



#1	#2	#3	#4
LU1	SF1/10	SF1/11	C7/1
LU2	SF1/12	SF1/13	C7/2
LU3	SF1/14	SF1/15	C7/3
LU4	SF2/10	SF2/11	C7/4
LU5	SF2/12	SF2/13	C7/6
LU6	SF2/14	SF2/15	C7/7
LU7	SF3/10	SF3/11	C7/8
LU8	SF3/12	SF3/13	C7/9
LU9	SF3/14	SF3/15	C7/11
LU10	SF4/10	SF4/11	C7/12
LU11	SF4/12	SF4/13	C7/13
LU12	SF4/14	SF4/15	C7/14
LU13	SF5/10	SF5/11	C7/16
LU14	SF5/12	SF5/13	C7/17
LU15	SF5/14	SF5/15	C7/18
LU16	SG6/4	SG6/3	C7/19
LU17	/		
LU18	/		
LU19	/		
LU20	SG8/12	SG8/13	C1/24
LU21	SG8/14	SG8/15	C1/23
LU22	SG7/6	SG7/5	C1/22
LU23	SG7/4	SG7/3	C1/21
LU24	/		

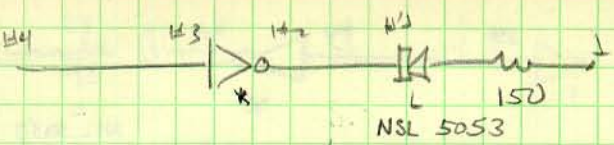
#1	#2	#3	#4
LV1	SF1/6	SF1/5	C12/39
LV2	SF1/4	SF1/3	C12/38
LV3	SF1/2	SF1/1	C12/37
LV4	SF2/6	SF2/5	C12/36
LV5	SF2/4	SF2/3	C12/34
LV6	SF2/2	SF2/1	C12/33
LV7	SF3/6	SF3/5	C12/32
LV8	SF3/4	SF3/3	C12/31
LV9	SF3/2	SF3/1	C12/29
LV10	SF4/6	SF4/5	C12/28
LV11	SF4/4	SF4/3	C12/27
LV12	SF4/2	SF4/1	C12/26
LV13	SF5/6	SF5/5	C12/24
LV14	SF5/4	SF5/3	C12/23
LV15	SF5/2	SF5/1	C12/22
LV16	SG6/2	SG6/1	C12/21
LV17	/		
LV18	/		
LV19	/		
LV20	SG7/2	SG7/1	C1/16
LV21	SG8/6	SG8/5	C1/17
LV22	SG8/4	SG8/3	C1/18
LV23	SG8/2	SG8/1	C1/19
LV24	/		

* SG7 & SG8 are non inverting

23 Sept 76
ABB

CPU Panel #1 Arithmetic
CPU Panel #1 I/O
CPU Panel #1 Selectors
CPU Panel #1 I/O Control

Wiring list



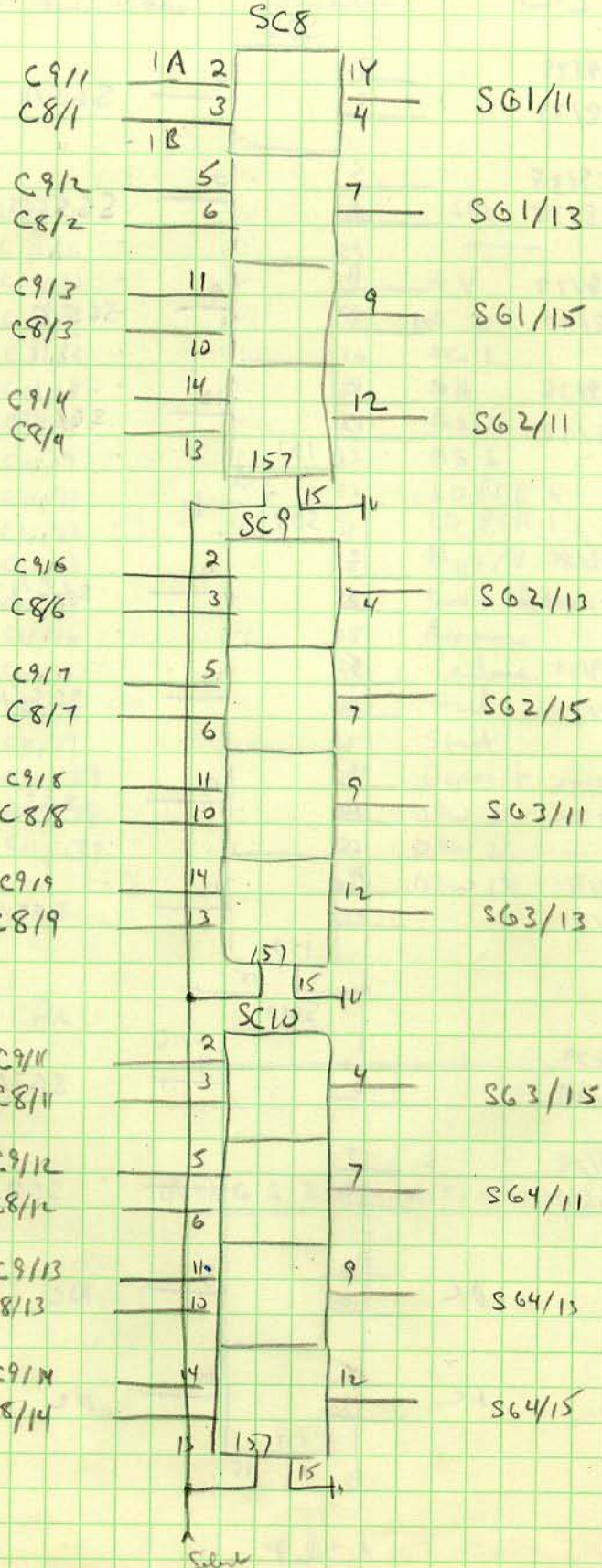
#1	#2	#3	#4
Lx1	SG1/10	SG1/11	SC8/4
Lx2	SG1/12	SG1/13	SC8/7
Lx3	SG1/14	SG1/15	SC8/9
Lx4	SG2/10	SG2/11	SC8/12
Lx5	SG2/12	SG2/13	SC9/4
Lx6	SG2/14	SG2/15	SC9/7
Lx7	SG3/10	SG3/11	SC9/9
Lx8	SG3/12	SG3/13	SC9/12
Lx9	SG3/14	SG3/15	SC10/4
Lx10	SG4/10	SG4/11	SC10/7
Lx11	SG4/12	SG4/13	SC10/9
Lx12	SG4/14	SG4/15	SC10/12
Lx13	SG5/10	SG5/11	SD8/4
Lx14	SG5/12	SG5/13	SD8/7
Lx15	SG5/14	SG5/15	SD8/9
Lx16	SG6/10	SG6/11	SD8/12
Lx17	SG6/12	SG6/13	SD9/4
Lx18	SG6/14	SG6/15	SD9/7
* Lx19	SG7/10	SG7/11	SH1/2
* Lx20	SG7/12	SG7/13	SH1/4
* Lx21	SG7/14	SG7/15	SH1/6
* Lx22	SG8/10	SG8/11	SH1/10
Lx23	/		
Lx24	/		

#1	#2	#3	#4
Ly1	SG1/6	SG1/5	C12/1
Ly2	SG1/4	SG1/3	C12/2
Ly3	SG1/2	SG1/1	C12/3
Ly4	SG2/6	SG2/5	C12/4
Ly5	SG2/4	SG2/3	C12/6
Ly6	SG2/2	SG2/1	C12/7
Ly7	SG3/6	SG3/5	C12/8
Ly8	SG3/4	SG3/3	C12/9
Ly9	SG3/2	SG3/1	C12/11
Ly10	SG4/6	SG4/5	C12/12
Ly11	SG4/4	SG4/3	C12/13
Ly12	SG4/2	SG4/1	C12/14
Ly13	SG5/6	SG5/5	C12/16
Ly14	SG5/4	SG5/3	C12/17
Ly15	SG5/2	SG5/1	C12/18
Ly16	SG6/6	SG6/5	C12/19
Ly17	/		
Ly18	/		
Ly19	/		
Ly20	/		
Ly21	/		
Ly22	/		
Ly23	/		
Ly24	/		

* these are as follows

	#6	#5
Lx19	SD9/9	SH1/1
Lx20	SD9/12	SH1/3
Lx21	SD10/4	SH1/5
Lx22	SD10/7	SH1/11

Virtual/Physical Selector



24 Sept 76
ARA

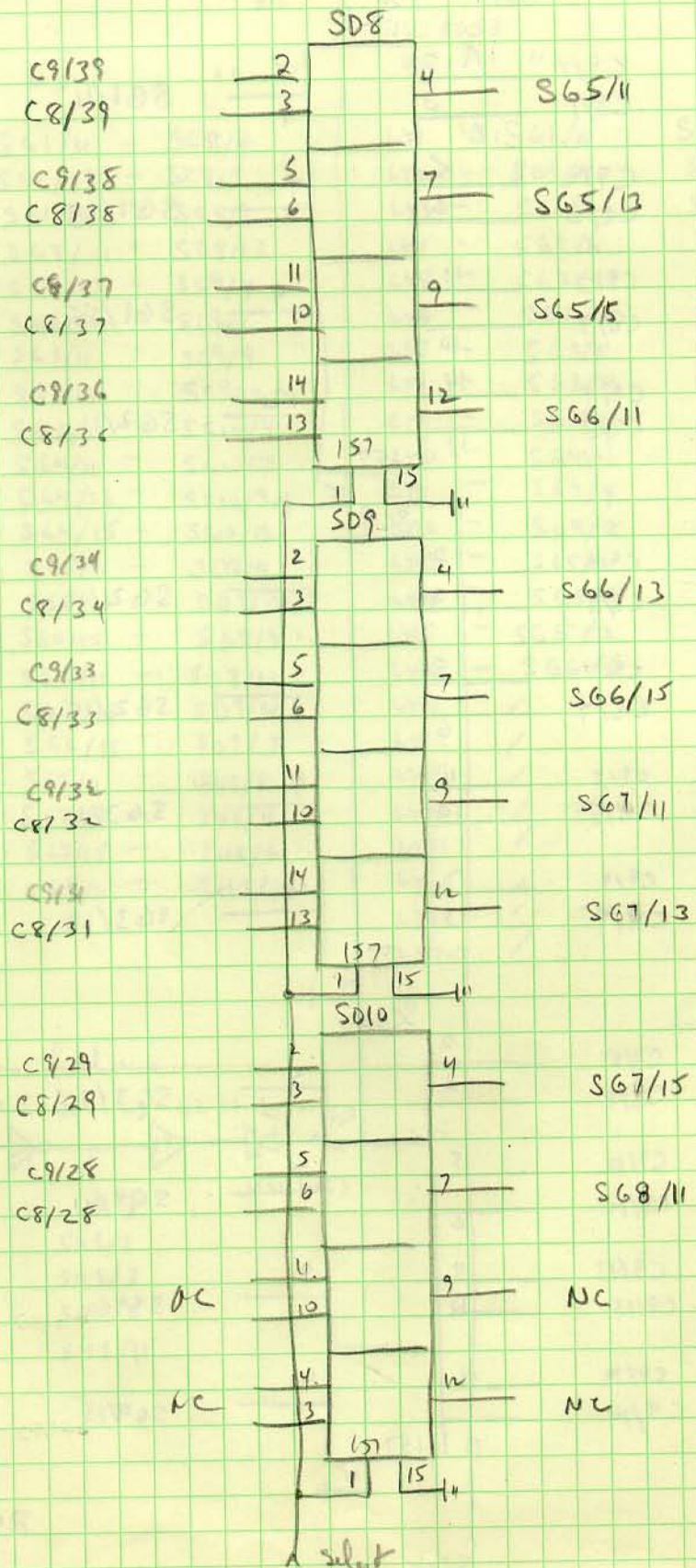
CPU Panel #1 Arithmetic

CPU Panel #1 I/O

CPU Panel #1 Selectors Status

CPU Panel #1 I/O Control

Virtual/Physical Selector



Console to Switches Connector C13

1	DSW 0	— C11/1		40	GND		
2	DSW 1	— C11/2		39			
3	DSW 2	— C11/3		38	+V	—	SH10/15
4	DSW 3	— C11/4		37	MC 2	—	SF10/10
5	DSW 4	— C11/6		36	MC 1	—	SH7/12
6	DSW 5	— C11/7		35	MH	—	SH7/14
7	DSW 6	— C11/8		34	MS 2	—	SF6/10
8	DSW 7	— C11/9		33	MS 1	—	SH8/10
9	DSW 8	— C11/11		32	LD PCR 2	—	SF8/11
10	DSW 9	— C11/12		31	LD PCR 1	—	SH8/12
11	DSW 10	— C11/13		30	Phys / V. int	—	SH8/14
12	DSW 11	— C11/14		29	Load Address	—	SH9/10
13	DSW 12	— C11/16		28	Examine	—	SH9/12
14	DSW 13	— C11/17		27	Continue	—	SH9/14
15	DSW 14	— C11/18		26	Halt	—	SH10/10
16	DSW 15	— C11/19		25	Start	—	SH10/12
17	DSW 16	— C11/39		24	Deposit	—	SH10/14
18	DSW 17	— C11/38		23	DSW 21	— C11/33	
19	DSW 18	— C11/37		22	DSW 20	— C11/34	
20	GND			21	DSW 19	— C11/36	

Console words to CPU

#1

DSW

15												2	1	0

#2

DSW

LA	EX	C	S	D	H	X	X	X	X	21	20	19	18	17	16

25 Sept 76
ARD

C7

PCR & Vector Data

1	PCR <0>	SF1/11
2	|	SF1/13
3	|	SF1/15
4	|	SF2/11
5	GND – SF1/8	
6	|	SF2/13
7	|	SF2/15
8	|	SF3/11
9	|	SF3/13
10	GND – SF1/7	
11	|	SF3/15
12	|	SF4/11
13	|	SF4/13
14	|	SF4/15
15	GND – SF2/8	
16	|	SF5/11
17	|	SF5/13
18	|	SF5/15
19	PCR <15>	SG6/3
20	GND – SF2/7	

40	GND – SE1/8	
39	Vector <0>	SE1/11
38	|	SE1/13
37	|	SE1/15
36	|	SE1/5
35	GND SE1/7	
34	|	SE1/3
33	|	SE1/1
32	|	SE2/11
31	Vector <7>	SE1/13
30	GND SE2/8	
29	Vector <8>	SE3/13
28	|	SE3/15
27	|	SE4/11
26	|	SE4/13
25	GND SE2/7	
24	|	SE4/15
23	|	SE4/5
22	|	SE4/3
21	Vector <15>	SE4/1

C8

C9

C8 Virtual Addres

1	VA <0>	SC8/3
2	|	SC8/6
3	|	SC8/10
4	|	SC8/13
5	GND — SE3/8	
6	|	SC9/3
7	|	SC9/6
8	|	SC9/10
9	|	SC9/13
10	GND — SE3/7	
11	|	SC10/3
12	|	SC10/6
13	|	SC10/10
14	VA <11>	SC10/13
15	GND — SE4/8	
16		
17	BUS [L] — SE2/5	
18		
19	CP CLOCK — SG10/15	
20	GND — SE4/7	

40	GND — SC8/8	
39	VA <12>	SD8/3
38	|	SD8/6
37	|	SD8/10
36	|	SD8/13
35	GND — SD7/8	
34	|	SD9/3
33	|	SD9/6
32	|	SD9/10
31	|	SD9/13
30	GND — SC9/8	
29	|	SD10/3
28	VA <21>	SD10/6
27		
26		
25	GND — SD6/8	
24	HALT [L] —	SG9/13
23	HALT [H] —	SG9/3
22		
21		

C9 Physical Addres + C', V', N', Z' + WIO's + MHCL [H]

1	PA <0>	SC8/2
2	|	SC8/5
3	|	SC8/11
4	|	SC8/14
5	GND — SC10/8	
6	|	SC9/2
7	|	SC9/5
8	|	SC9/11
9	|	SC9/14
10	GND — SD5/7	
11	|	SC10/2
12	|	SC10/5
13	|	SC10/11
14	PA <11>	SC10/14
15	GND — SD8/8	
16	C'	SE3/11
17	V'	SE3/5
18	N'	SE3/3
19	Z'	SE3/1
20	GND — SD7/7	

40	GND — SD9/8	
39	PA <12>	SD8/2
38	|	SD8/5
37	|	SD8/11
36	|	SD8/14
35	GND — SD6/7	
34	|	SD9/2
33	|	SD9/5
32	|	SD9/11
31	|	SD9/14
30	GND — SD10/8	
29	|	SD10/2
28	PA <21>	SD10/5
27		
26		
25	GND —	SD5/7
24	MME [H] —	SF7/4
23		
22		
21	MHCL [H] — SF8/11	

25 Sept 76
AMB

CPU Panel #1 Arithmetic
CPU Panel #1 I/O
CPU Panel #1 Selectors Status
CPU Panel #1 I/O Control

C10 SW Data + Vector Addr

1	DSW0	C11/1
2	|	C11/2
3	|	C11/3
4	|	C11/4
5	GND	- C11/5
6	|	C11/6
7	|	C11/7
8	|	C11/8
9	|	C11/9
10	GND	- C11/10
11		C11/11
12	|	C11/12
13	|	C11/13
14	|	C11/14
15	GND	- C11/15
16		C11/16
17	|	C11/17
18	|	C11/18
19	DSW15	C11/19
20	GND	- C11/20

to Control Board

40	GND - C11/40	
39	VCTA<0>	- SE5/1
38	|	SE5/13
37	|	SE5/15
36	|	SE5/5
35	GND - C11/35	
34	VCTA<4>	SE5/3
33		
32		
31		
30	GND - C11/30	
29	HALT [L]	— SG9/10
28	HALT [H]	— SG9/6
27		
26	LD PCR	— SH4/4
25	GND - C11/25	
24	DIS [L]	— SF10/6
23	DIS [H]	— SF10/5
22	PFS [H]	— SF6/5
21	PANEL Reset [L]	— SF9/1

C11 SW Data

1	DSW0	C10/1 + C13/1
2	|	C10/2 + C13/2
3	|	C10/3 + C13/3
4	|	C10/4 + C13/4
5	GND	- SG3/8 + C10/5
6	|	C10/6 + C13/5
7	|	C10/7 + C13/6
8	|	C10/8 + C13/7
9	|	C10/9 + C13/8
10	GND	- SG3/7 + C10/10
11		C10/11 + C13/9
12		C10/12 + C13/10
13		C10/13 + C13/11
14		C10/14 + C13/12
15	GND	- SG4/8 + C10/15
16		C13/13 + C10/16
17		C13/14 + C10/17
18		C13/15 + C10/18
19	DSW15	C13/16 + C10/19
20	GND	- SG4/7 + C10/20

to CPU Board

40	GND - SG5/8 + C10/40	
39	DSW16	C13/17
38	|	C13/18
37	|	C13/19
36	|	C13/21
35	GND - SG5/7 + C10/35	
34		C13/22
33	DSW24	C13/23
32		
31		
30	GND - SG6/8 + C10/30	
29		
28		
27	H	- SH5/6
26	D	- SH5/2
25	GND - SG6/7 + C10/25	
24	S	- SH5/4
23	C	- SH5/14
22	EX	- SH5/12
21	LA	- SH5/10

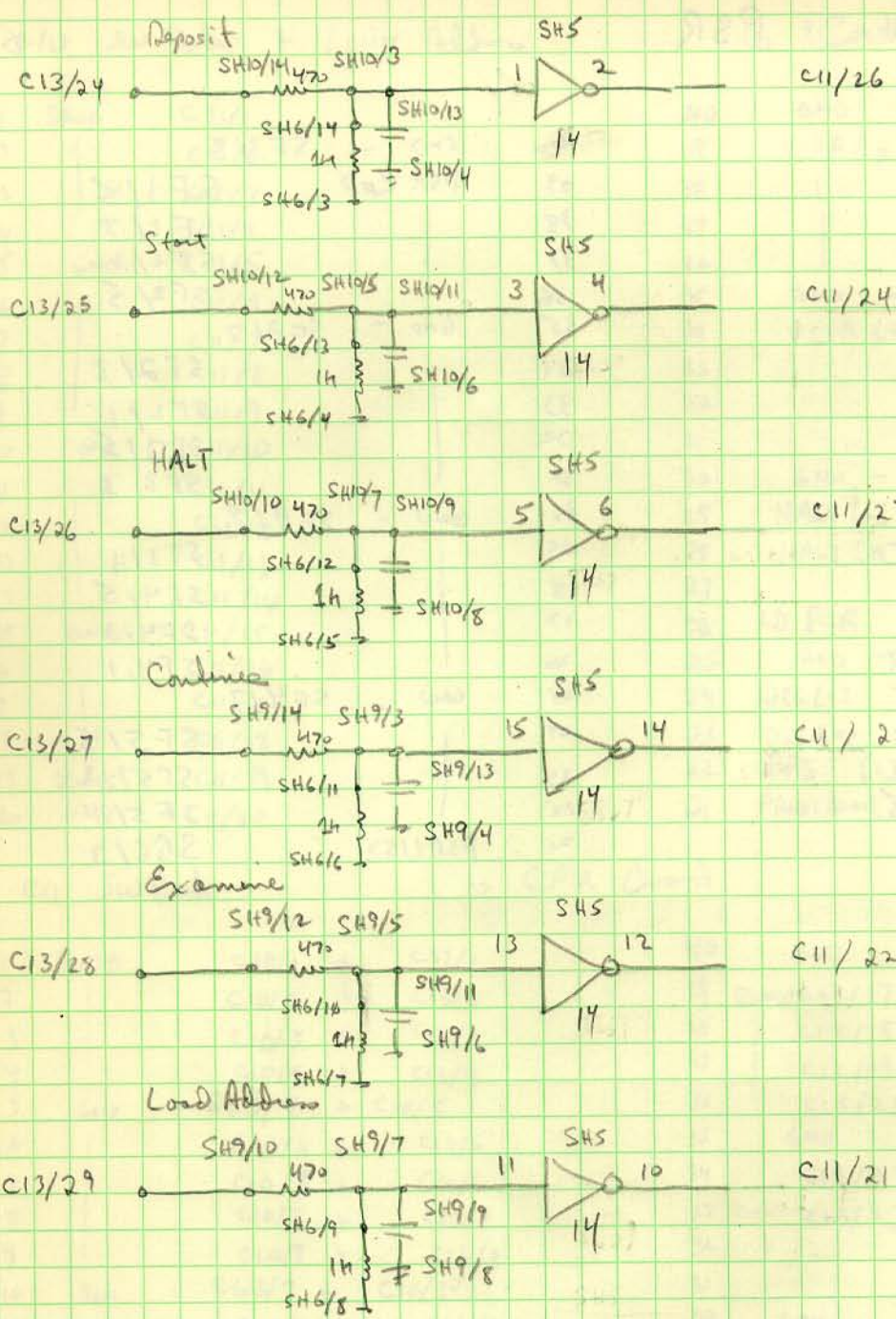
C12 Data Register & PSR

1	D(0)	- SG1/5
2		SG1/3
3		SG1/1
4		SG2/5
5	GND	- SG1/8
6		SG2/3
7		SG2/1
8		SG3/5
9		SG3/3
10	GND	- SG1/7
11		SG3/1
12		SG4/5
13		SG4/3
14		SG4/1
15	GND	- SG2/8
16		SG5/5
17		SG5/3
18		SG5/1
19	D(15)	SG6/5
20	GND	- SG2/7

40	GND	- SF3/8
39	PSR(0)	SF1/5
38		SF1/3
37		SF1/1
36		SF2/5
35	GND	- SF3/7
34		SF2/3
33		SF2/1
32		SF3/5
31		SF3/3
30	GND	- SF4/8
29		SF3/1
28		SF4/5
27		SF4/3
26		SF4/1
25	GND	- SF4/7
24		SF5/5
23		SF5/3
22		SF5/1
21	PSR(15)	SG6/3

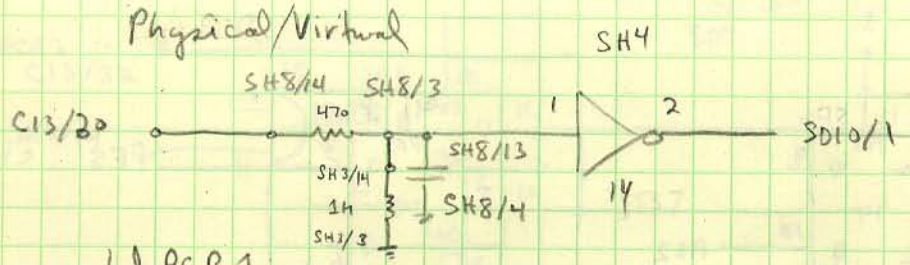
25 Sept 1976
ARO

CPU Panel #1 Arithmetic
CPU Panel #1 I/O
CPU Panel #1 Selectors Status
CPU Panel #1 I/O Control

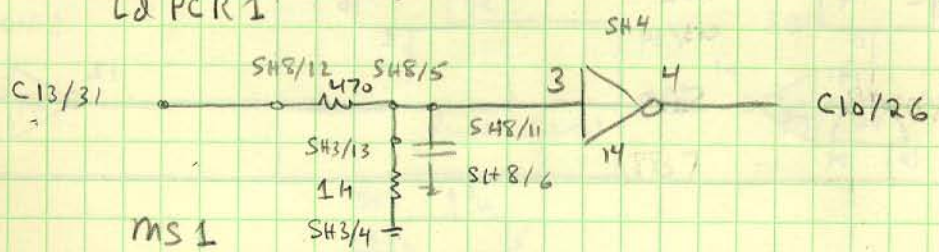


Caps = 10mf @ 25VDC

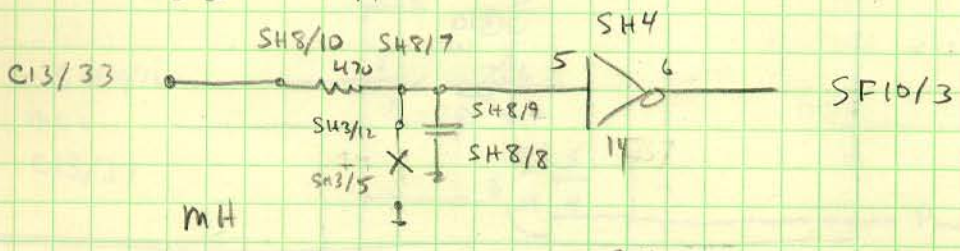
Physical/Virtual



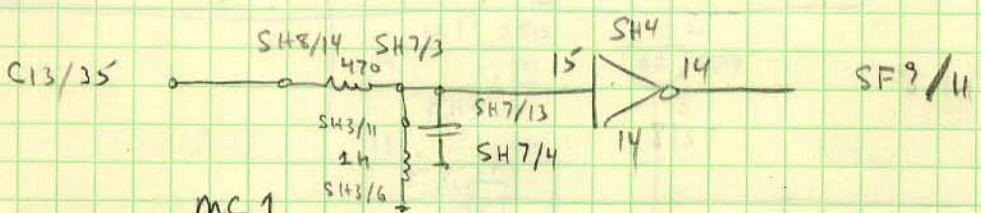
Ld PCR 1



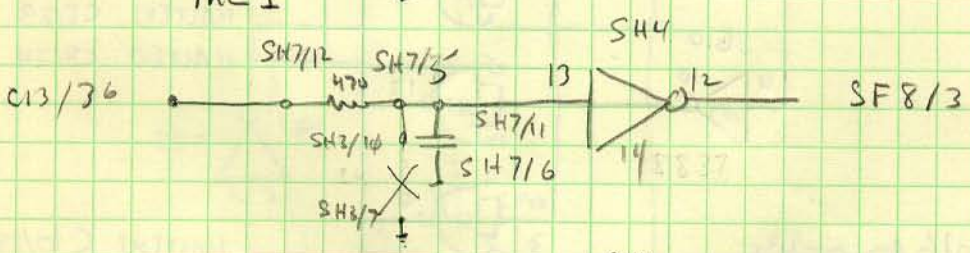
ms 1

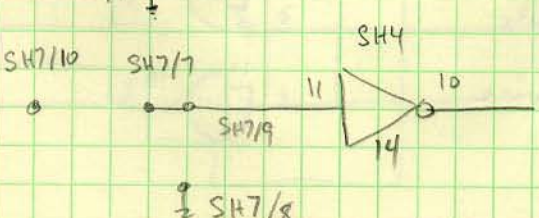


mH



mC 1

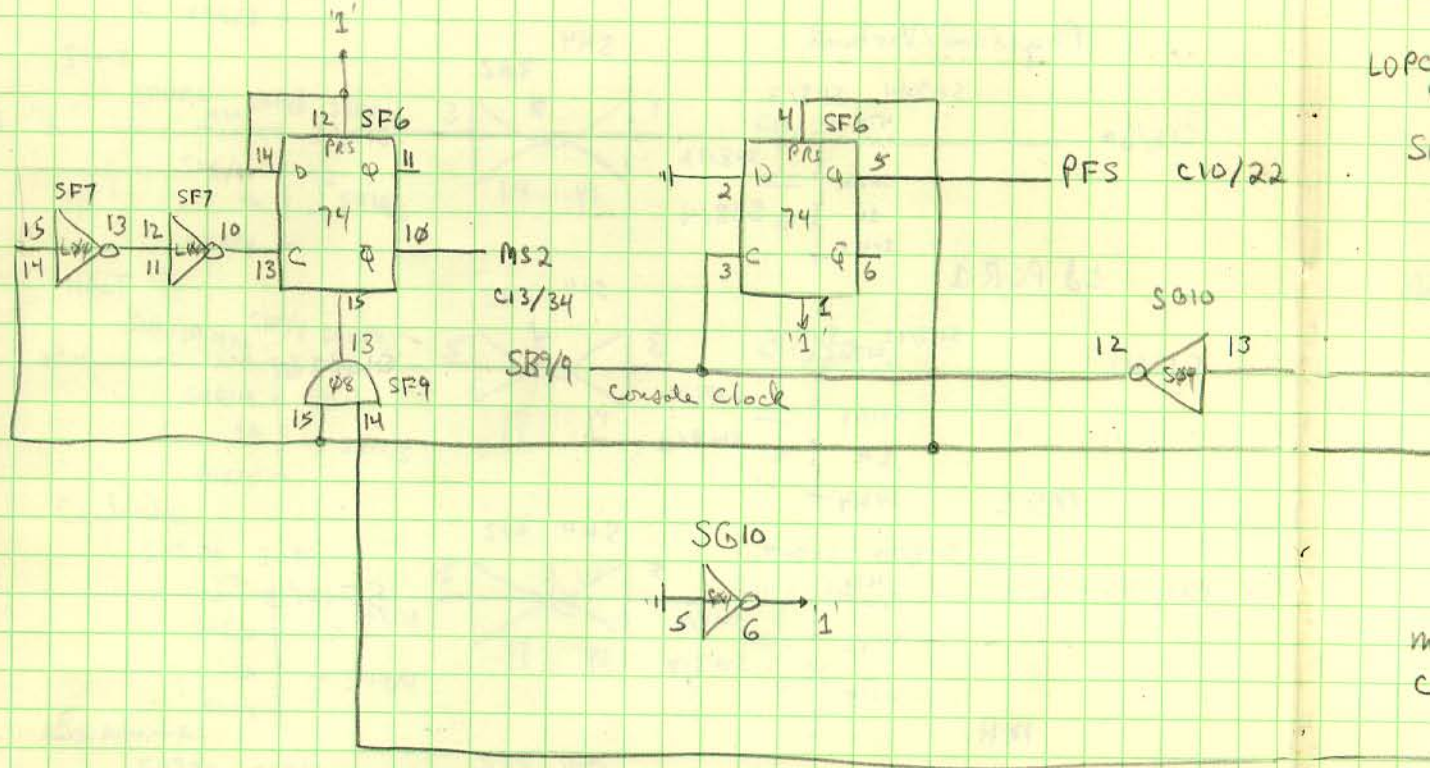


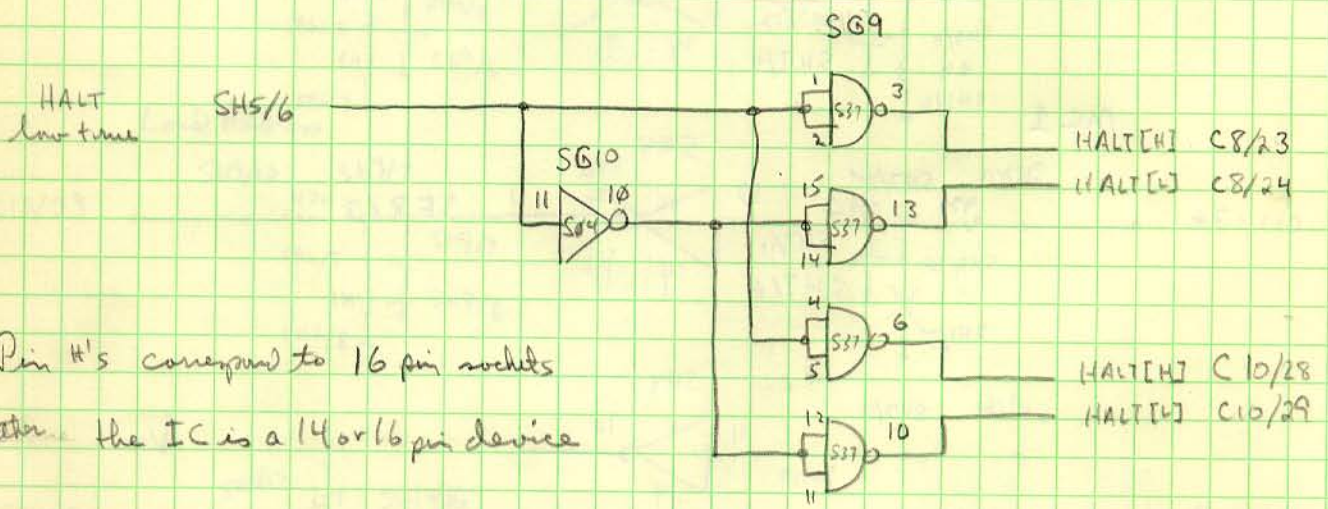


25 Sept 1976
ARO

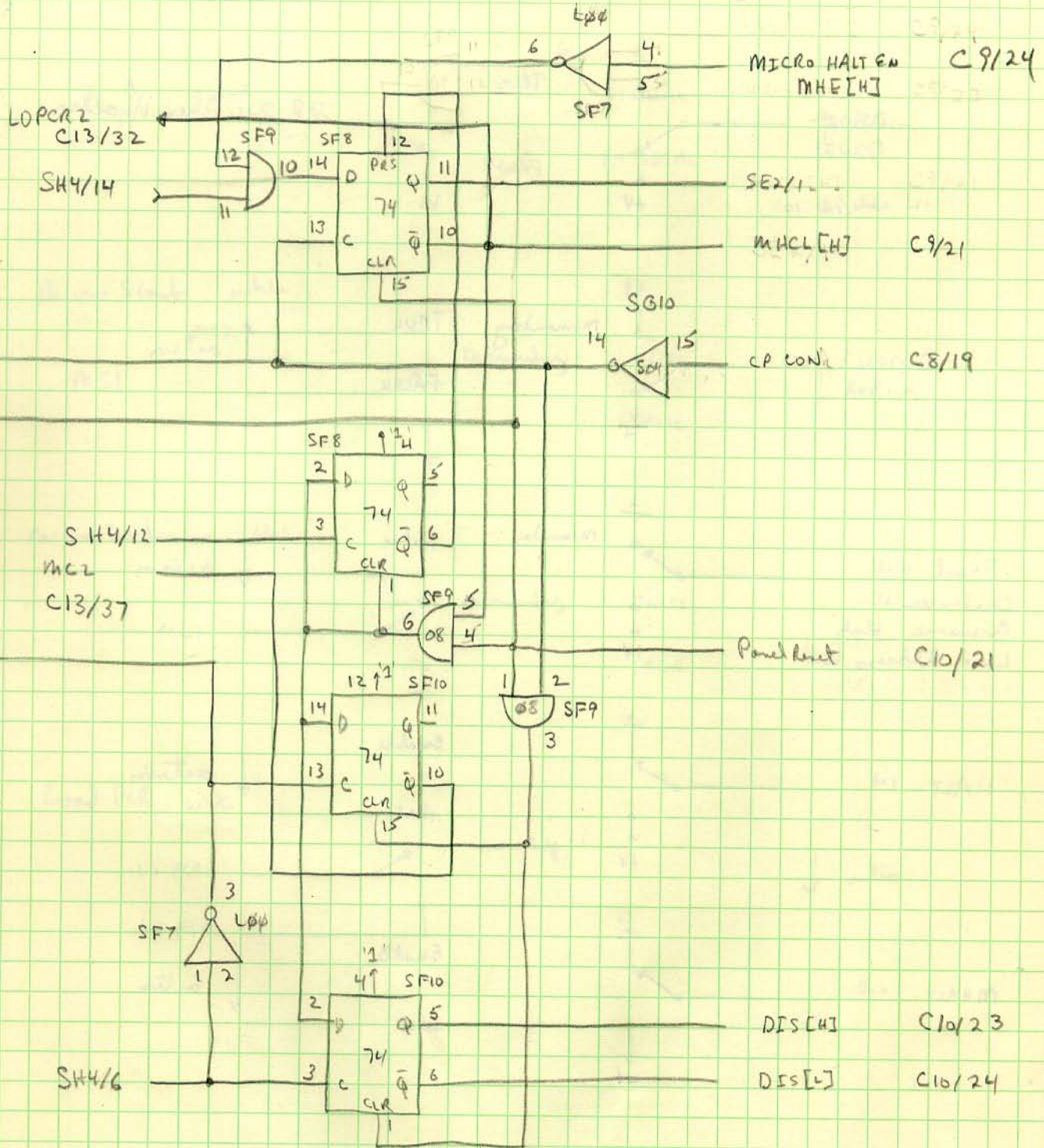
CPU Panel #1 Arithmetic
CPU Panel #1 I/O
CPU Panel #1 Selectors
CPU Panel #1 I/O Control

Control Panel Logic





Pin #'s correspond to 16 pin sockets whether the IC is a 14 or 16 pin device

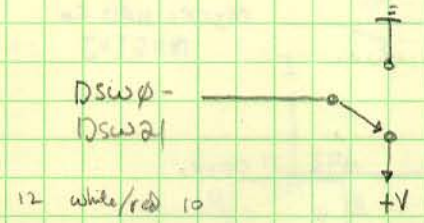


26 Sept 76
ARD

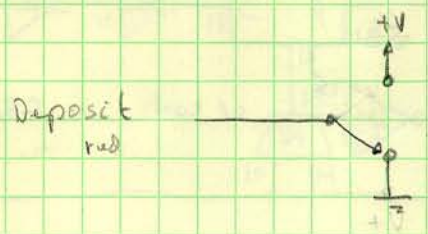
CPU Panel #1 Arithmetic
CPU Panel #1 I/O
CPU Panel #1 Selectors Status
CPU Panel #1 I/O Control

Switch Wiring

(Data to CPU cond must be low true

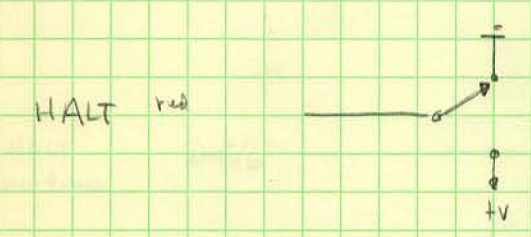


22 switches ↑ action



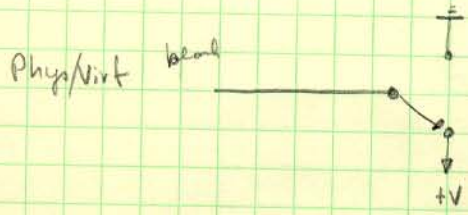
↑ action

↓ action



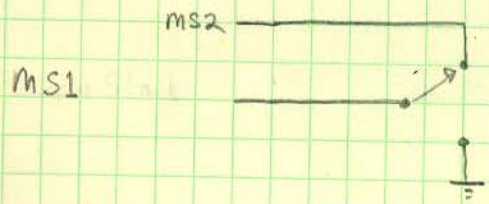
↓ action

↓ action



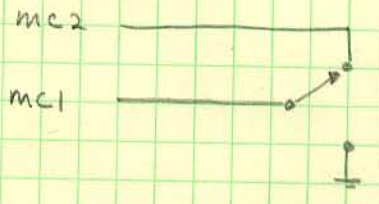
↑ Action

Micro Start white



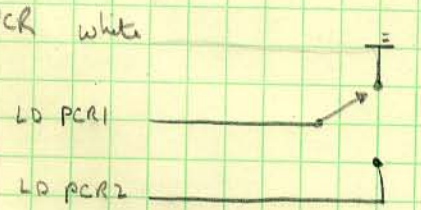
↓ Action

Micro Continue white



↓ Action

Load PCR white



↓ action

26 Sept 76
ARD

CPU Panel #1 Arithmetic

CPU Panel #1 I/O

CPU Panel #1 Selectors

CPU Panel #1 I/O Control

3/CN4 - CN21 (3) (24") SRC/DST

2/CN8 - CN24 (3) (24") INST

1/CN4 - CN23 (3) (32") I/O Ch

1) CN7 - CN26 (3) (31") SCRATCH

2) 15½" yellow -

Control Processor Unit Board #3

Control Memory Unit Board # 3

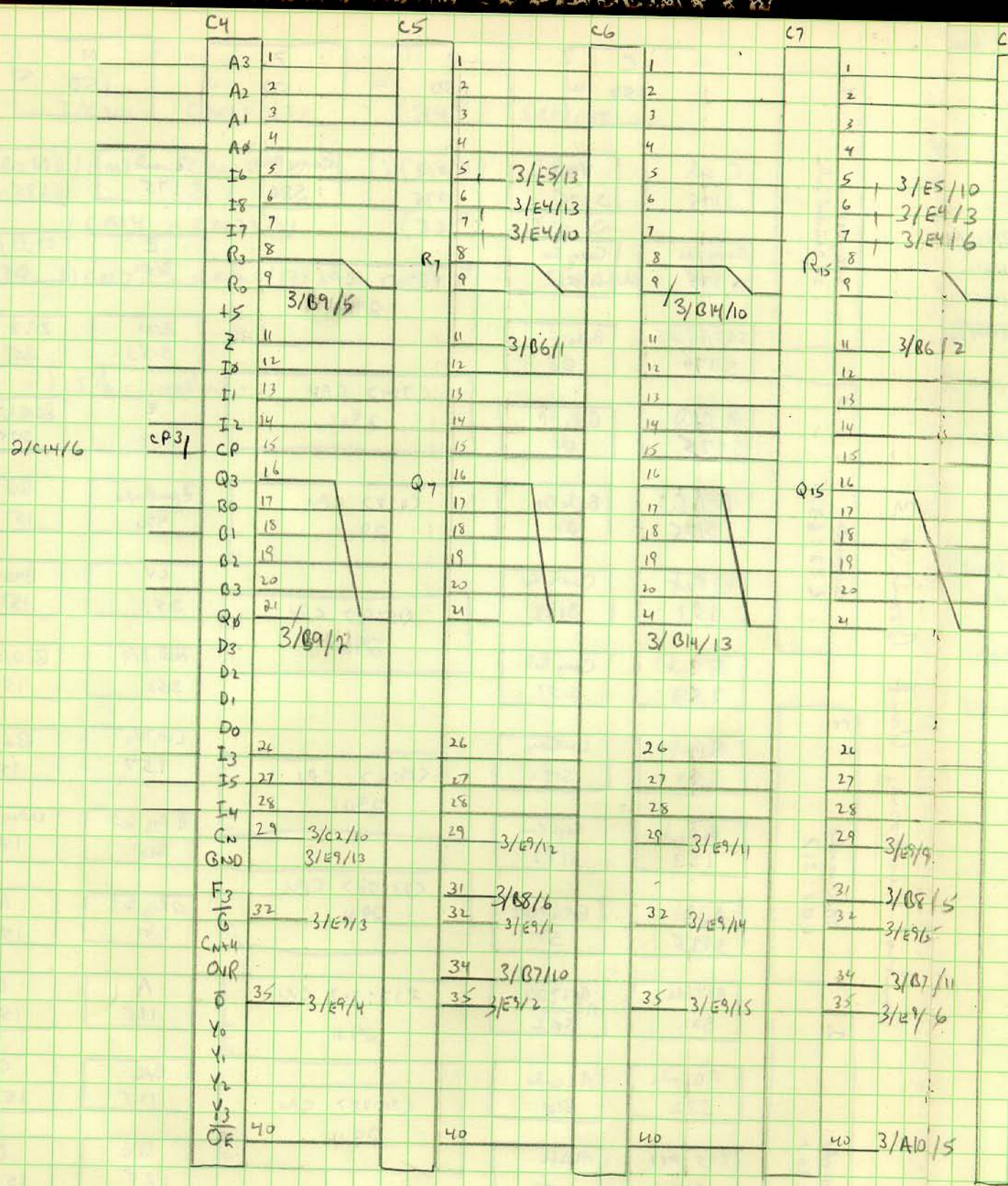
	C 150	V 150	Z 150	N 150		1
4 SRC, DST IR Decoder Path	C sel S175	V sel S175	C', V', Z', N' 175	Carry PSW S86	Z sel S175	N sel S175	2
	Carry IN S175	Carry IN 151	<3:0> CPU 2901 C4		Z S151	I7, $\overline{I7}$, BAI7 Ø8	3
	I6,7,8/SRS S175	Byte OP Ø8			Z/N S153	Z∧Z SØ8	4
3 Microcode <32:63>	B Add S175	Byte OP Øf	<7:4> CPU 2901 C5		Z SØ8	BCØ,1,2/SR4 S175	5
	A;B Sel S175	Byte OP Ø8	<11:8> CPU 2901 C6		Zpulldn 470	SØ 151	6
	B Port 153	Carry Ex S182	<15:12> CPU 2901 C7		CV S153	B4D 151	7
	B Port 153	Carry Sel S157			MSB R/Q S153	B3D/S1 151	8
2 Microcode <Ø:31>	A Port 153	Low Carry S182	<19:16> CPU 2901 C10		LSB R/Q 157	B2D 151	9
	A Port 153	High Carry S182			R Reg Sel S151	uPwr/BID 151	10
	Add S175	BR67D/S 51	<23:20> CPU 2901 C11		Q Reg Sel S151	A 151	11
1 Microcode <64:95>	AB Code S21	BR67D/S AB Code SØ2	<27:24> CPU 2901 C12		A 125	B 151	12
	AB Code S32	AB Code SIØ	<31:28> CPU 2901 C13		B/C 125	C 151	13
	I4,5; M@1 S175	MATH 153			D/E 125	D 151	14
	I Ø,1,2,3 S175	Parity S280	SOR SØ5	SOR SØ5	SRØ,1,2,3 S175	E 151	15
K	H	E	D	J	Q	A	

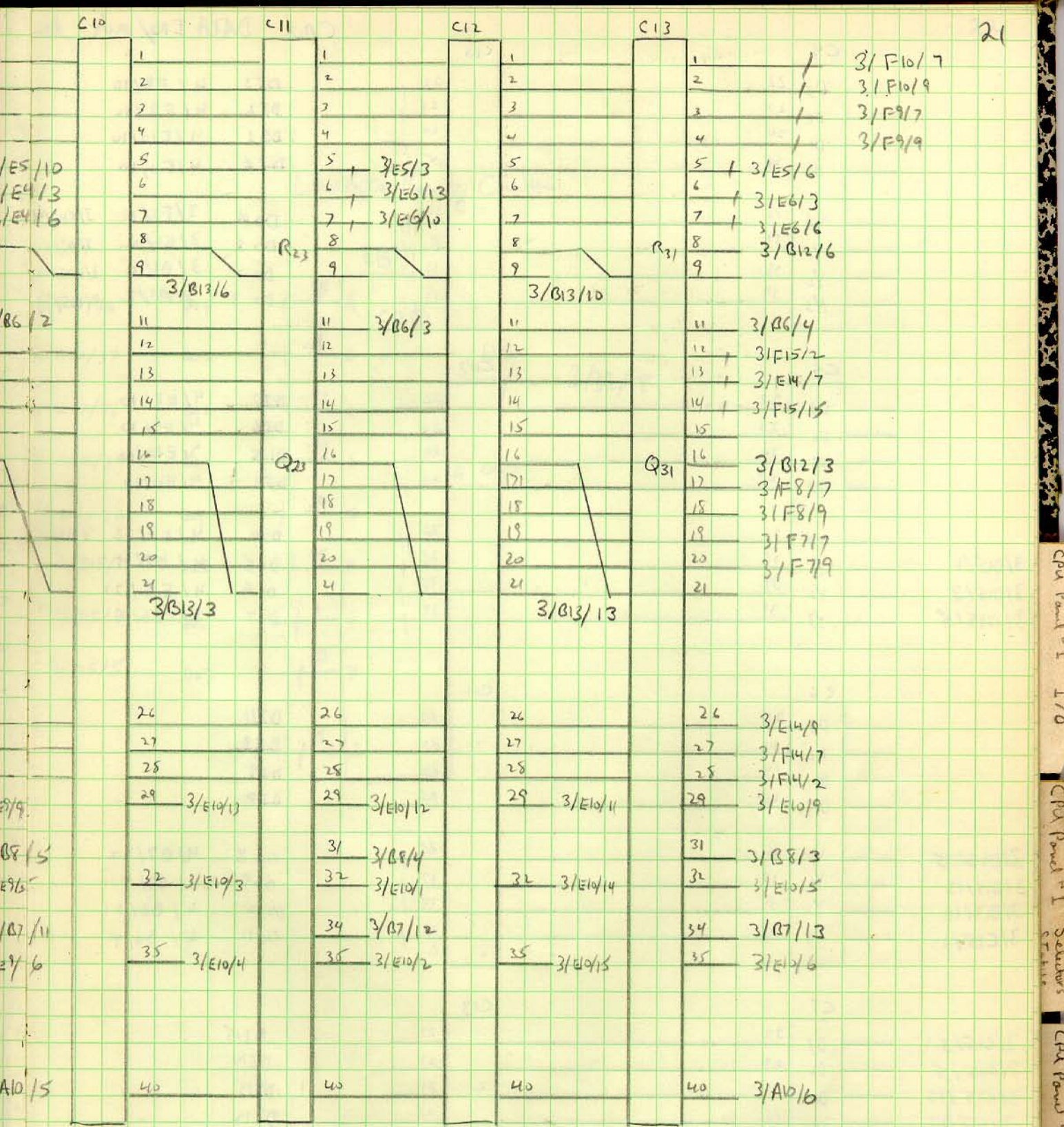
80ct76 APB

CPU Panel #1 I/O

CPU Panel #1 Selectors

CPU Panel #1 I/O Control

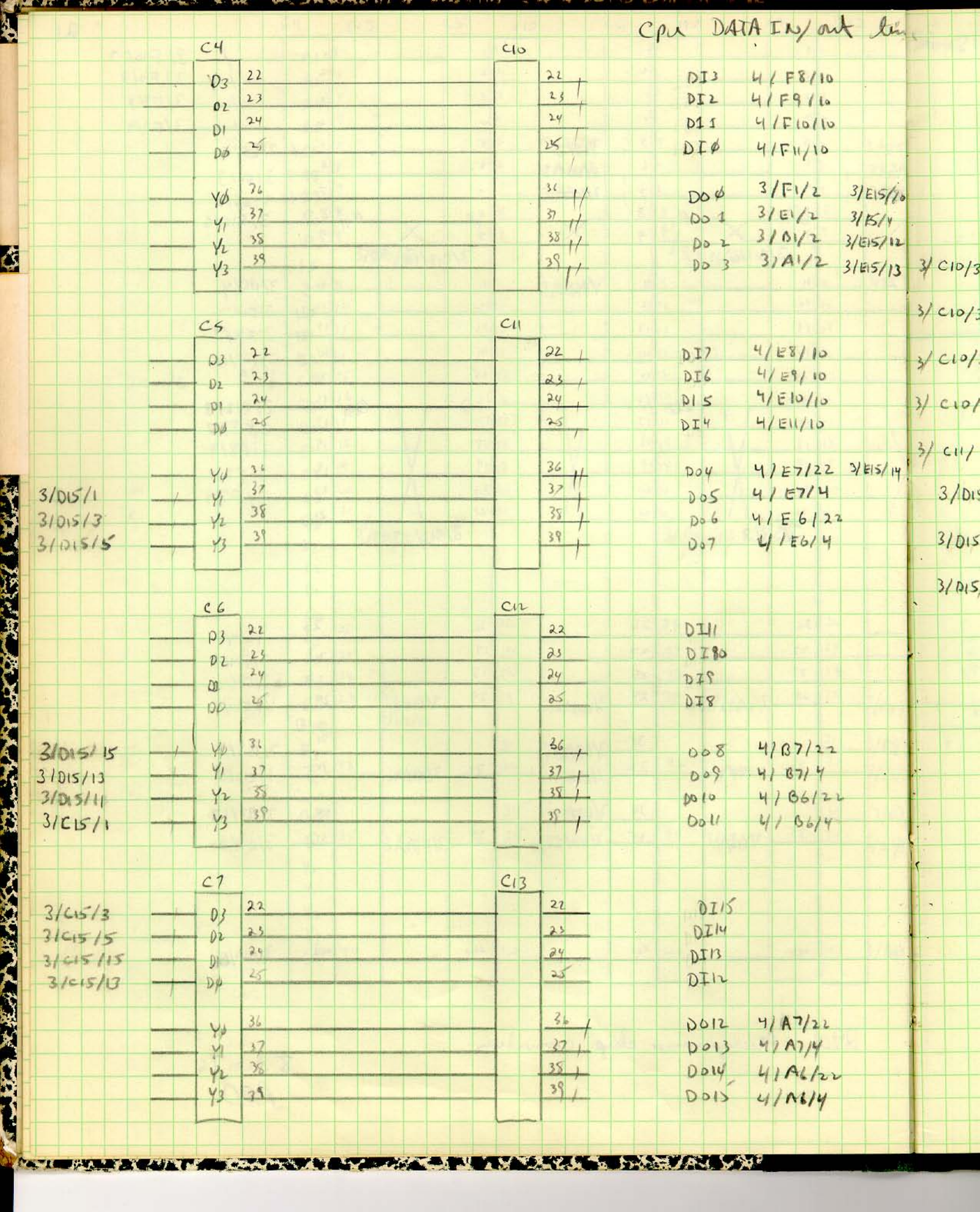

C4
C5
C6
C7
A3
A2
A1
A0
I6
I8
I7
R3
R0
+5
Z
I0
I1
I2
CP
Q3
B0
B1
B2
B3
Q0
D3
D2
D1
D0
I3
I5
I4
CN
GND
F3
G
CN+4
OVR
0
Y0
Y1
Y2
Y3
OE
3/B9/5
3/B9/7
3/C2/10
3/E9/13
3/E9/13
3/E9/4
3/E5/13
3/E4/13
3/E4/10
3/B6/1
3/B8/6
3/E9/1
3/B7/10
3/E3/2
3/B14/10
3/B14/13
3/E9/12
3/E9/11
3/E9/14
3/E9/15
3/E5/10
3/E4/3
3/E4/6
3/B6/2
3/E9/9
3/B8/5
3/E9/5
3/B7/11
3/E9/6
3/A10/5
R7
Q7
R15
Q15
2/C14/6
CP3



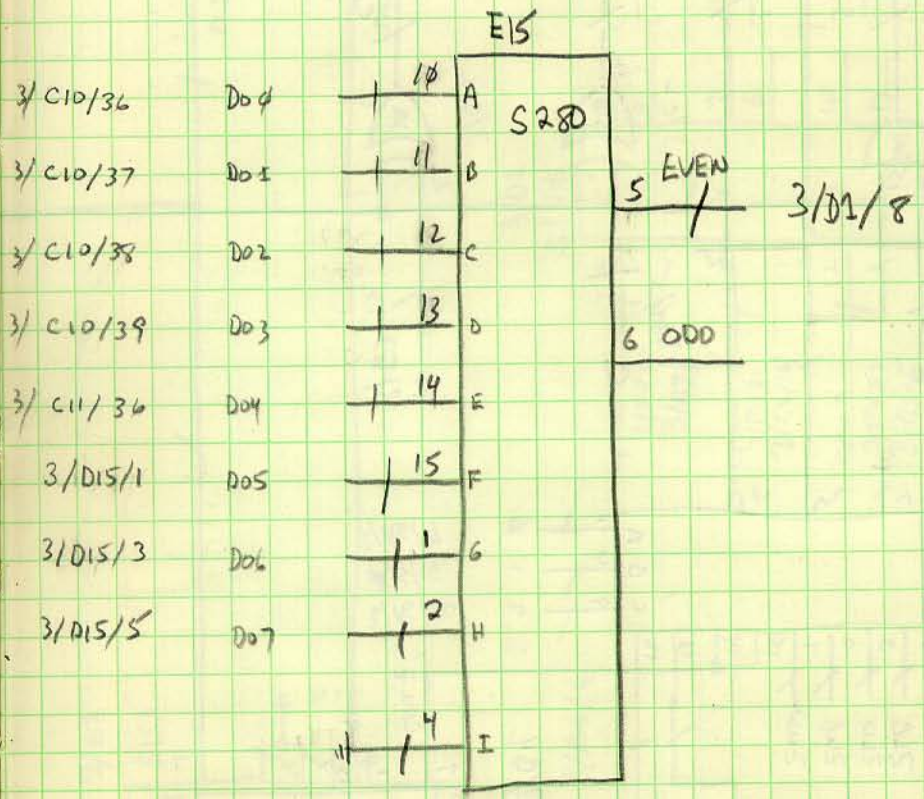
2901 Microprocessor chip connections

8 Oct 76
ARD

CPU Panel #1 I/O
CPU Panel #1 Selectors
CPU Panel #1 I/O Control


CPU DATA IN/out lines
C4
C10
D3 22
D2 23
D1 24
D0 25
Y0 36
Y1 37
Y2 38
Y3 39
DI3 4/F8/10
DI2 4/F9/10
DI1 4/F10/10
DI0 4/F11/10
DO0 3/F1/2 3/E15/10
DO1 3/E1/2 3/E5/4
DO2 3/D1/2 3/E15/12
DO3 3/A1/2 3/E15/13 3/C10/3
C5
C11
DI7 4/E8/10
DI6 4/E9/10
DI5 4/E10/10
DI4 4/E11/10
DO4 4/E7/22 3/E15/14
DO5 4/E7/4
DO6 4/E6/22
DO7 4/E6/4
3/D15/1
3/D15/3
3/D15/5
C6
C12
DI11
DI10
DI9
DI8
DO8 4/B7/22
DO9 4/B7/4
DO10 4/B6/22
DO11 4/B6/4
3/D15/15
3/D15/13
3/D15/11
3/C15/1
C7
C13
DI15
DI14
DI13
DI12
DO12 4/A7/22
DO13 4/A7/4
DO14 4/A6/22
DO15 4/A6/4
3/C15/3
3/C15/5
3/C15/15
3/C15/13

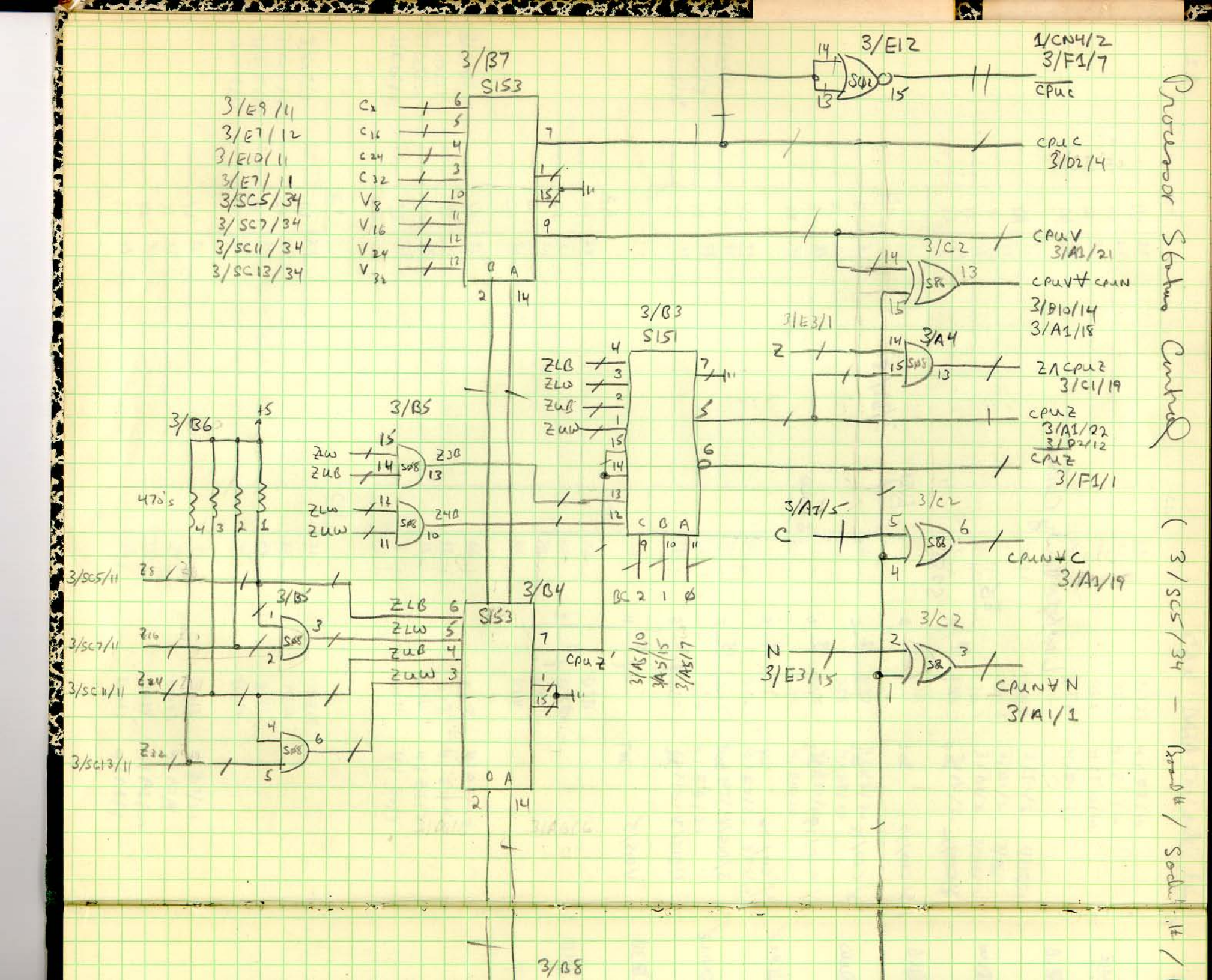
Low Byte Parity Checker

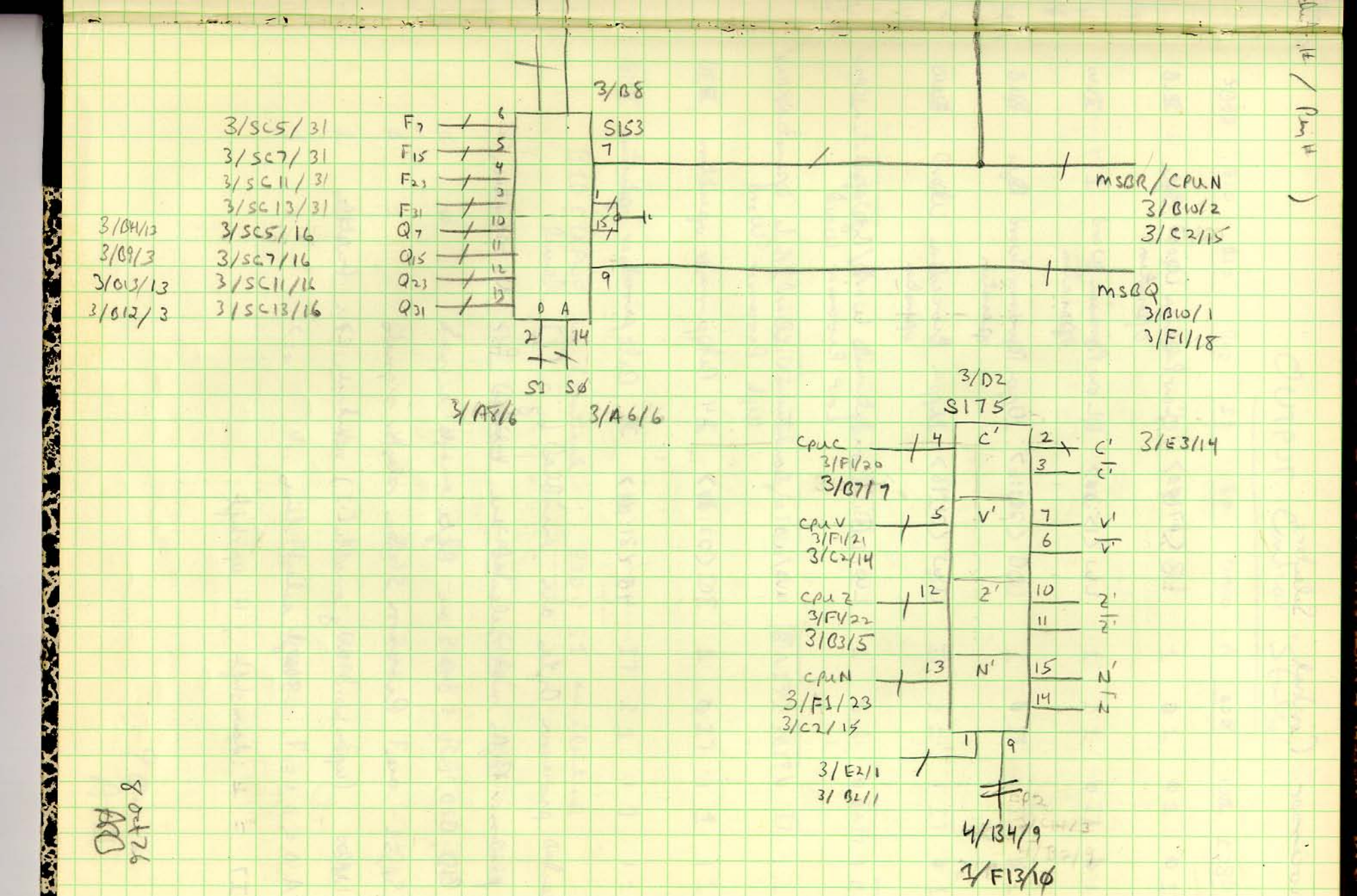


CPU Panel #1 I/O

CPU Panel #1 Selectors Status

CPU Panel #1 I/O Control


Processor Status Control (3/SC5/34 – Board 4 / Sock
3/B7
S153
3/E9/14
3/E7/12
3/E10/11
3/E7/11
3/SC5/34
3/SC7/34
3/SC11/34
3/SC13/34
C2
C16
C24
C32
V8
V16
V24
V32
3/E12
1/CN4/2
3/F1/7
CPUC
CPUC
3/D2/4
CPUV
3/A1/21
3/C2
CPUV ∀ CPUN
3/B10/14
3/A1/18
3/B3
S151
ZLB
ZLO
ZUB
ZUW
3/E3/1
Z
3/A4
Z∧CPUZ
3/C1/19
CPUZ
3/A1/22
3/D2/12
CPUZ
3/F1/1
3/B6
+5
470's
3/B5
ZUW
ZUB
ZLW
ZLB
Z3B
Z4B
3/A1/5
C
3/C2
CPUN∀C
3/A1/19
3/SC5/11
3/SC7/11
3/SC11/11
3/SC13/11
Z8
Z16
Z24
Z32
3/B5
3/B4
S153
ZLB
ZLW
ZUB
ZUW
CPUZ'
3/A5/10
3/A5/15
3/A5/7
N
3/E3/15
3/C2
CPUN∀N
3/A1/1
3/B8



CPU Panel #1 I/O

CPU Panel #1 Switches

CPU Panel #1 I/O

23

Processor Control Selectors

State	BC2	BC1	BC0			CPUZ	B1
0	0	0	0	LB <07:00>	Low Processor Word Byte operation	ZLB	1
1	0	0	1	LW <15:00>	Low Processor Word operation	ZLW	1
2	0	1	0	UB <23:16>	Upper Processor Word Byte operation	ZUB	0
3	0	1	1	UW <31:16>	Upper Processor Word operation	ZUW	0
4	1	0	0	LW/LB	Conditional Word/Byte operation CPUZ' Low Processor Word		1
5	1	0	1	UW/UB	Conditional Word/Byte operation CPUZ' High Processor Word		0
6	1	1	0	3B <23:00>	24 Bit processor operation	Z3B	1
7	1	1	1	4B <31:00>	32 Bit processor operation	Z4B	1

Selected processor Bytes are enabled by a [H] level
processor Bytes not selected are coded for No operation
B1D, B2D, B3D, & B4D are Byte enable signals
S0, S1 are Processor Status selector signals
UPWD (upper word only enable [L]) control CPU tristate
A, B, C, D, & E Shift select lines
I7 = L (down shift ; H up shift

OUTPUT Control States

B1D	B2D	B3D	B4D	S1	S0	UPWD	A	B	C	D	E
1	0	0	0	0	0	1	1	1	1	I7	$\overline{I7}$
1	1	0	0	0	1	1	1	1	I7	1	$\overline{I7}$
0	0	1	0	1	0	0	1	I7	$\overline{I7}$	1	1
0	0	1	1	1	1	0	I7	1	$\overline{I7}$	1	1
1	$\overline{Byte[4]}$	0	0	0	$\overline{Byte[4]}$	1	1	1	$\overline{B \wedge I7}$	$\overline{B \wedge I7}$	$\overline{I7}$
0	0	1	$\overline{Byte[4]}$	1	$\overline{Byte[4]}$	0	$\overline{B \wedge I7}$	$\overline{B \wedge I7}$	$\overline{I7}$	1	1
1	1	1	0	1	0	1	1	I7	1	1	$\overline{I7}$
1	1	1	1	1	1	1	I7	1	1	1	$\overline{I7}$

B1D & UPWD are identical ; B3D & S1 are identical

S1	S0	CARC	CPUV	CPUN	CPUZ'	MSBR	MSBQ
0	0	C_8	V_8	F_7	ZLB	F_7	Q_7
0	1	C_{16}	V_{16}	F_{15}	ZLW	F_{15}	Q_{15}
1	0	C_{24}	V_{24}	F_{23}	ZUB	F_{23}	Q_{23}
1	1	C_{32}	V_{32}	F_{31}	ZUW	F_{31}	Q_{31}

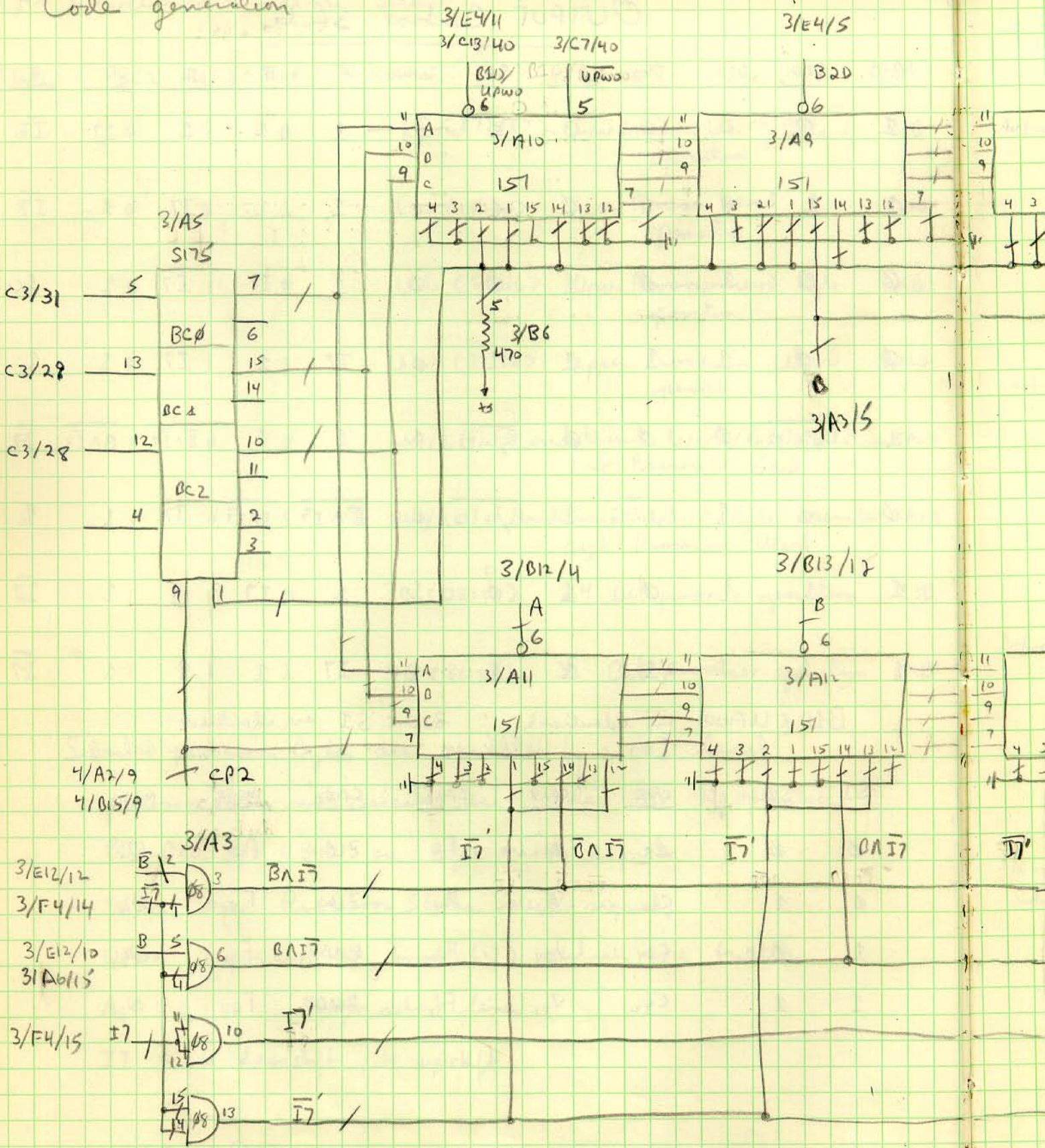
90d76
ARD

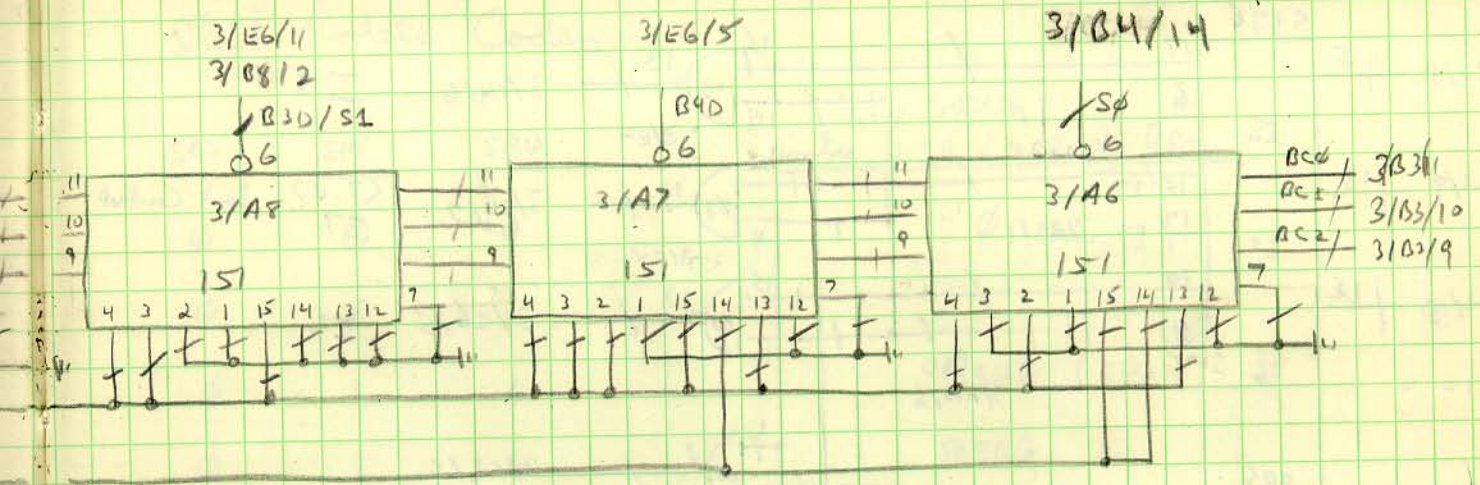
CPU Panel #1 I/O

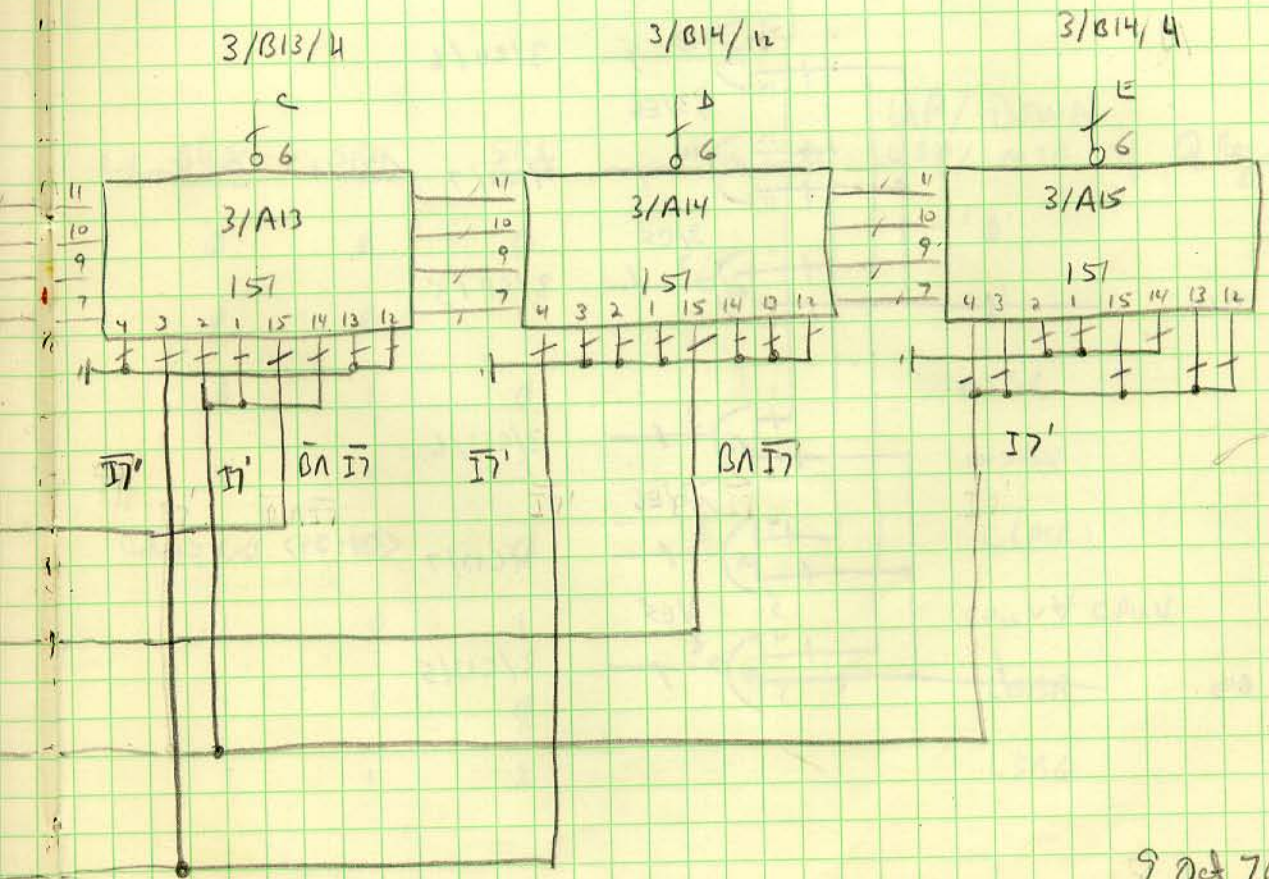
CPU Panel #1 Selectors Status

CPU Panel #1 I/O Control

Code generation







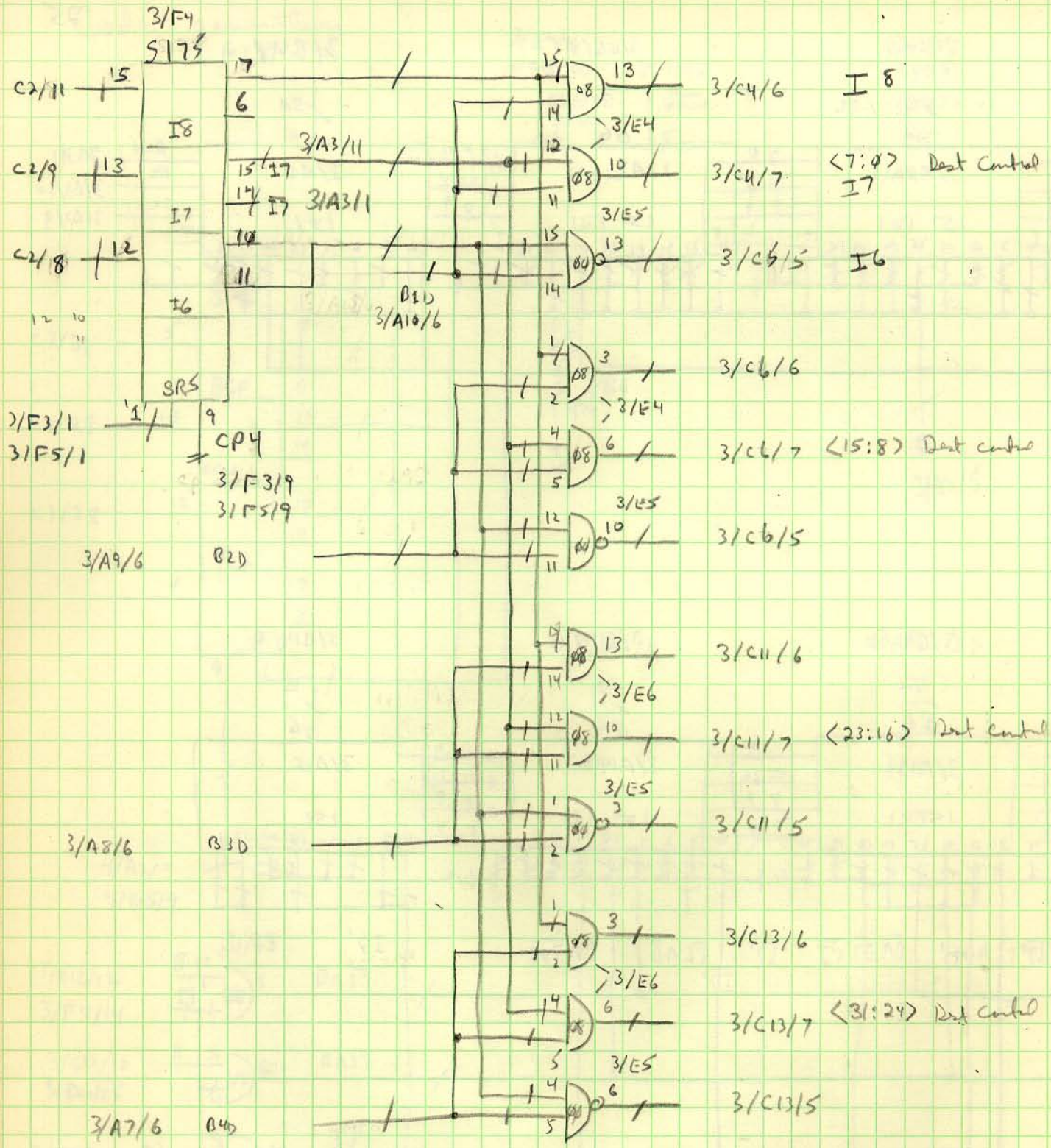
9 Oct 76

ARB

CPU Panel #1 I/O

CPU Panel #1 Selectors

CPU Panel #1 I/O Control


3/F4
S175
C2/11
C2/9
C2/8
I8
I7
I6
SRS
3/F3/1
3/F5/1
CP4
3/F3/9
3/F5/9
3/A3/11
3/A3/1
B1D
3/A10/6
3/A9/6
B2D
3/A8/6
B3D
3/A7/6
B4D
3/C4/6
3/C4/7
3/C5/5
3/C6/6
3/C6/7
3/C6/5
3/C11/6
3/C11/7
3/C11/5
3/C13/6
3/C13/7
3/C13/5
3/E4
3/E5
3/E6
I 8
I7
I6
<7:0> Dest Control
<15:8> Dest control
<23:16> Dest control
<31:24> Dest control

Shift Rotate Codes

UP/DOWN into LSB/MSB of RAM

SR2	SR1	SR0	
0	0	0	'0'
0	0	1	'1'
0	1	0	MSBR (CPUN)
0	1	1	MSBQ
1	0	0	C (PSR)
1	0	1	CPUN ≠ CPUV
1	1	0	LSBR
1	1	1	LSBQ

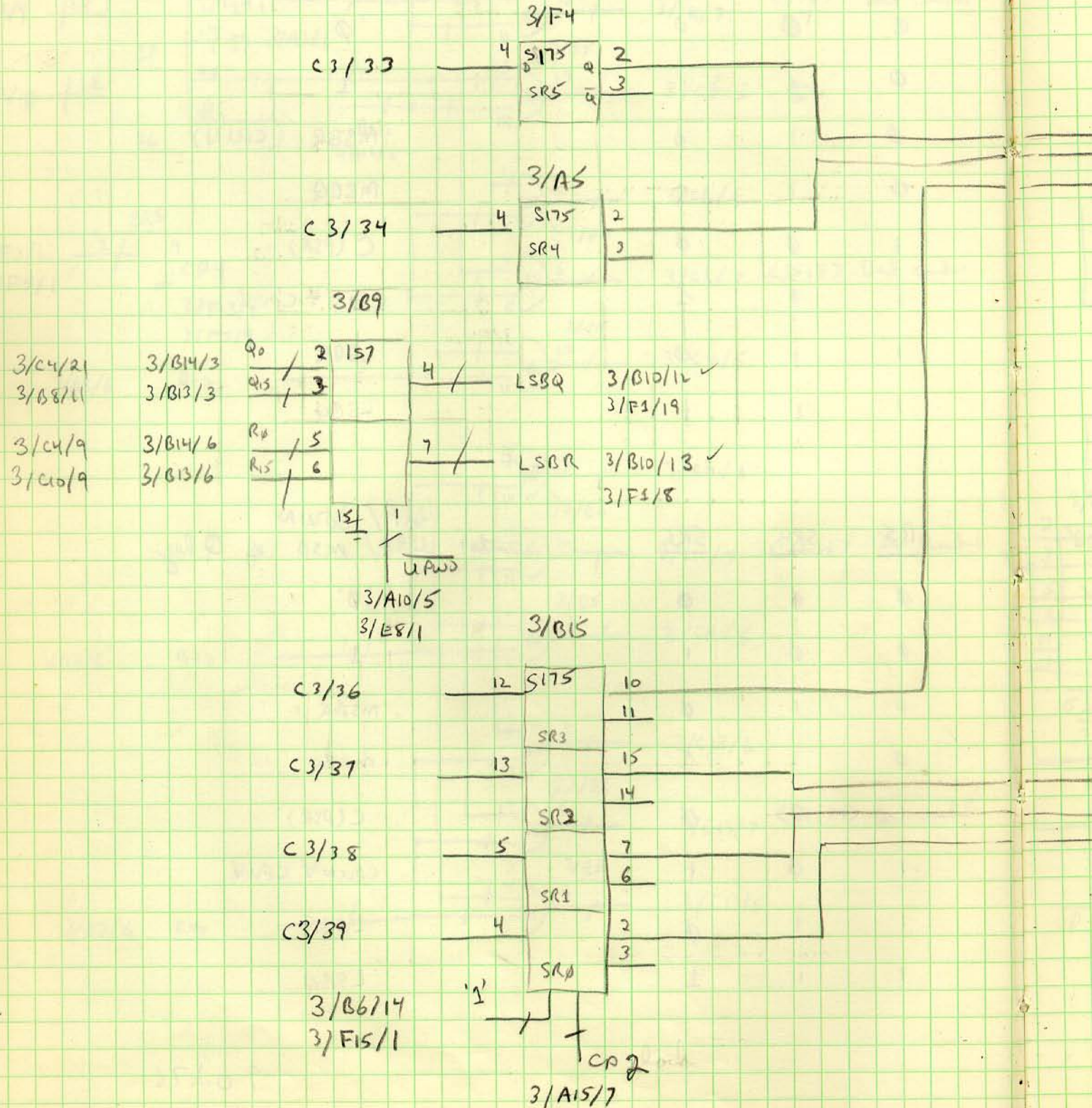
UP/DOWN into LSB/MSB of Q Reg

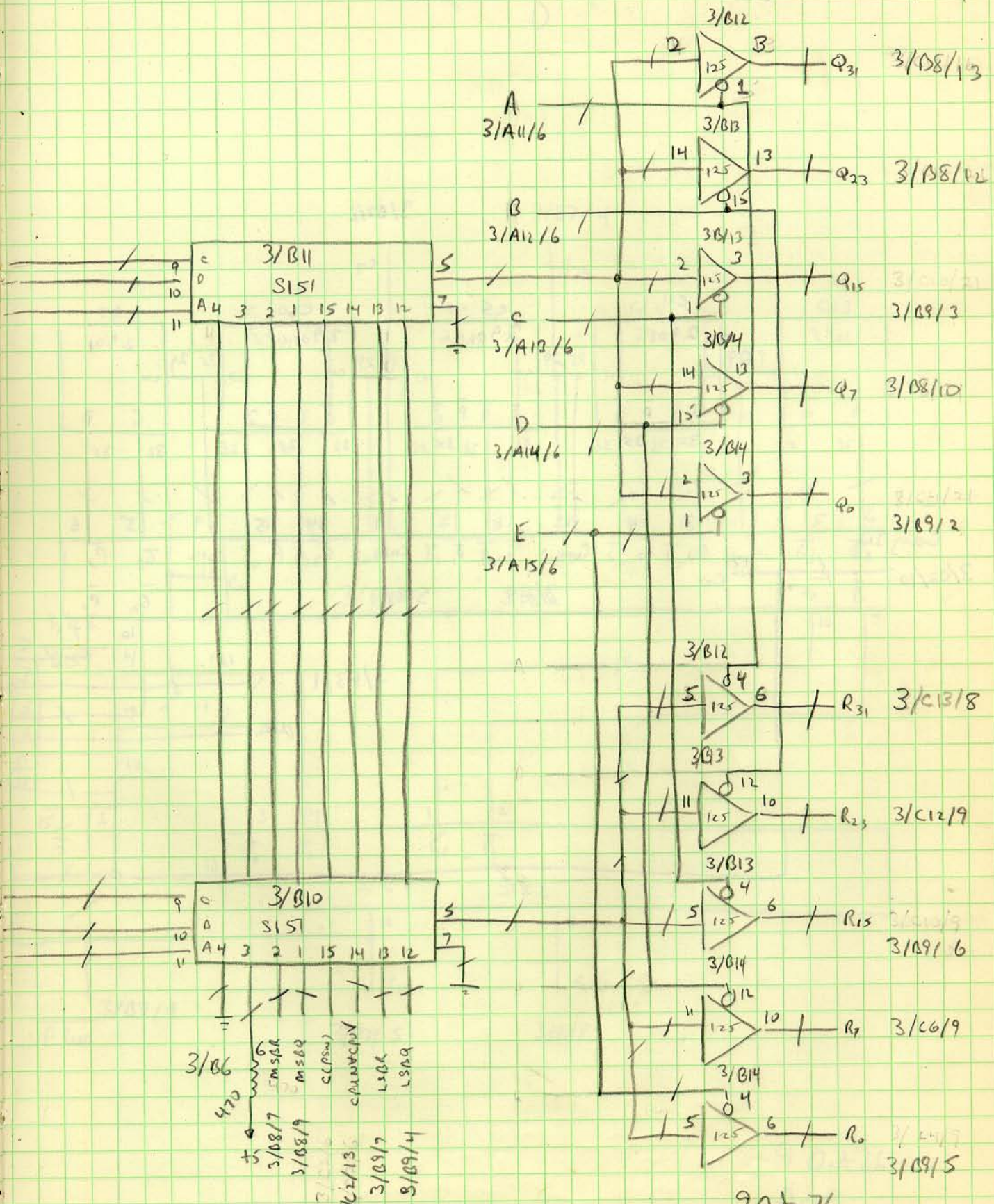
SR5	SR4	SR3	
0	0	0	'0'
0	0	1	'1'
0	1	0	MSBR
0	1	1	MSBQ
1	0	0	C(PSR)
1	0	1	CPUN ≠ CPUV
1	1	0	LSBR
1	1	1	LSBQ

9 Oct 76
ARB

CPU Panel #1 I/O
CPU Panel #1 Selectors Status
CPU Panel #1 I/O Control

Shift Rotate Selects





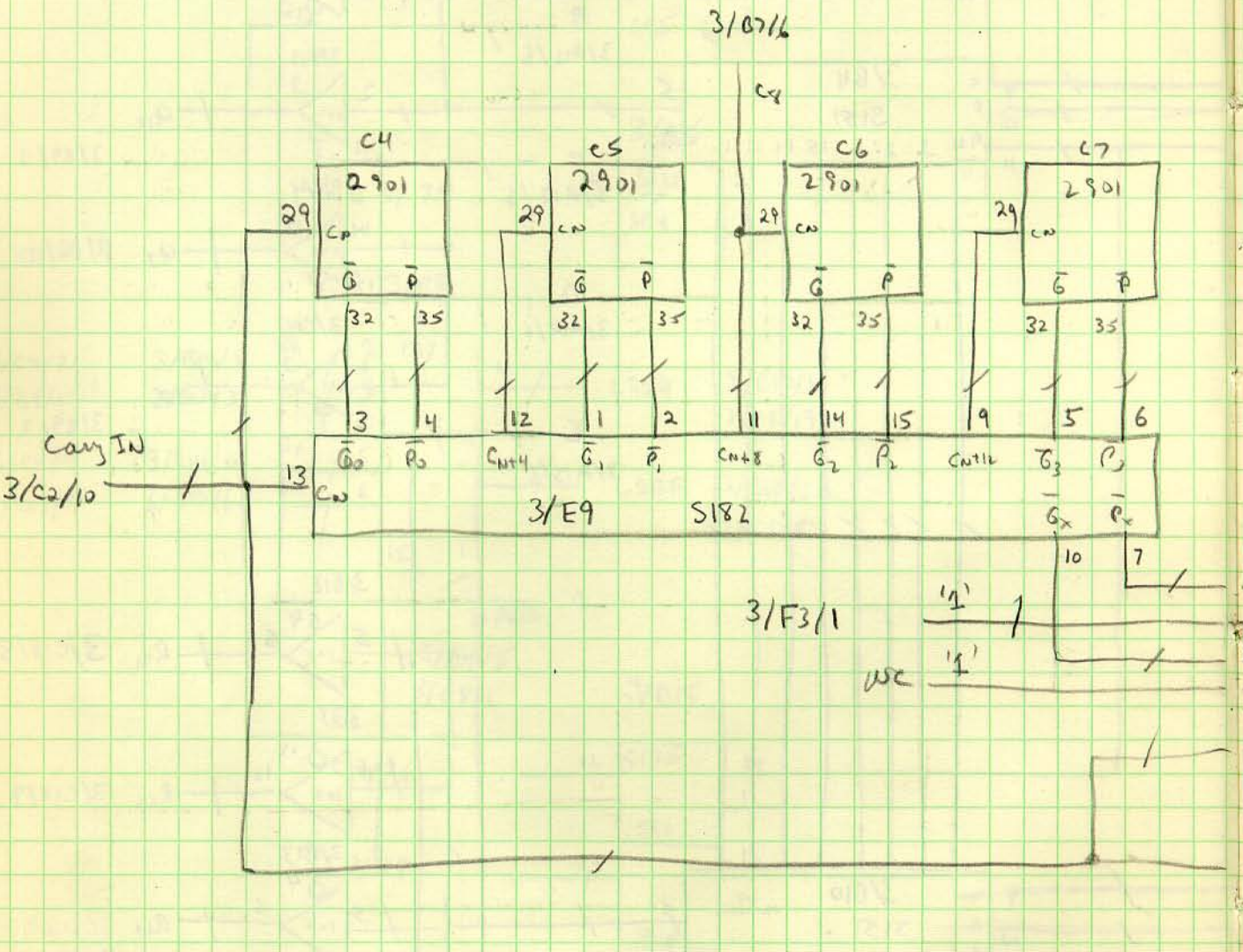
90+ 76
ARD

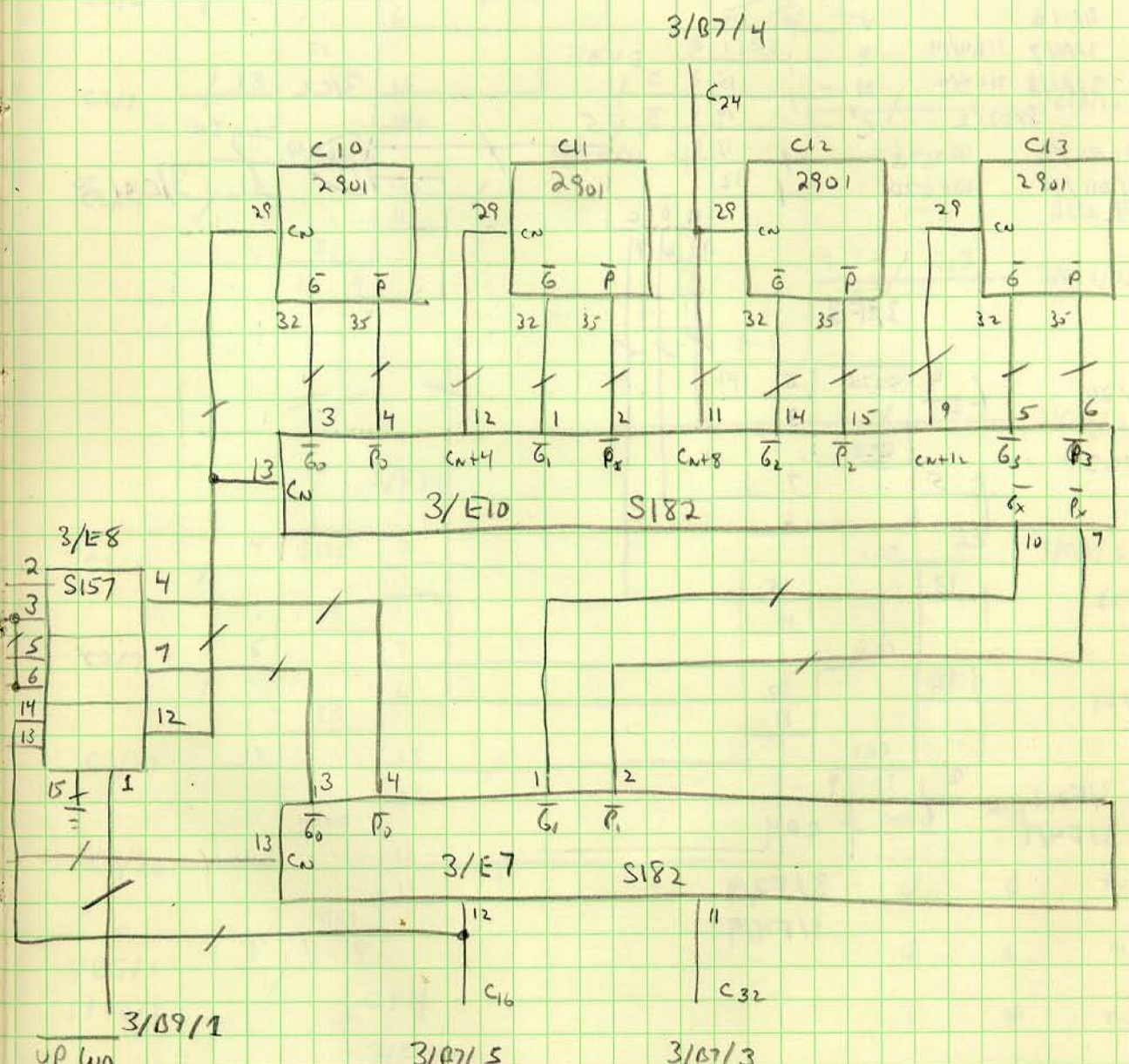
CPU Panel #1 I/O

CPU Panel #1 Selectors Status

CPU Panel #1 I/O Control

Processor Lookahead Carry Logic





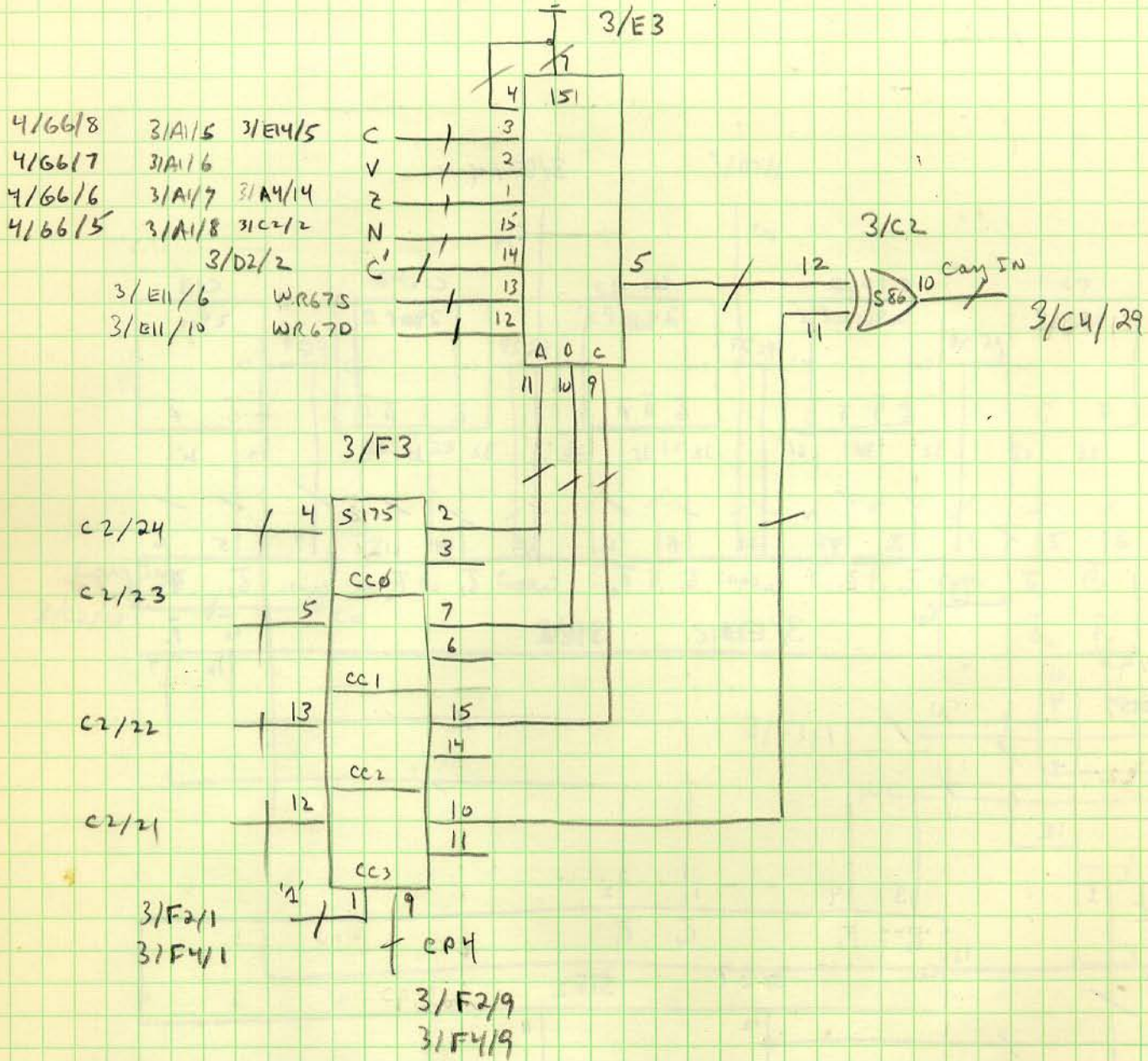
90476
ARB

CPU Panel #1 I/O

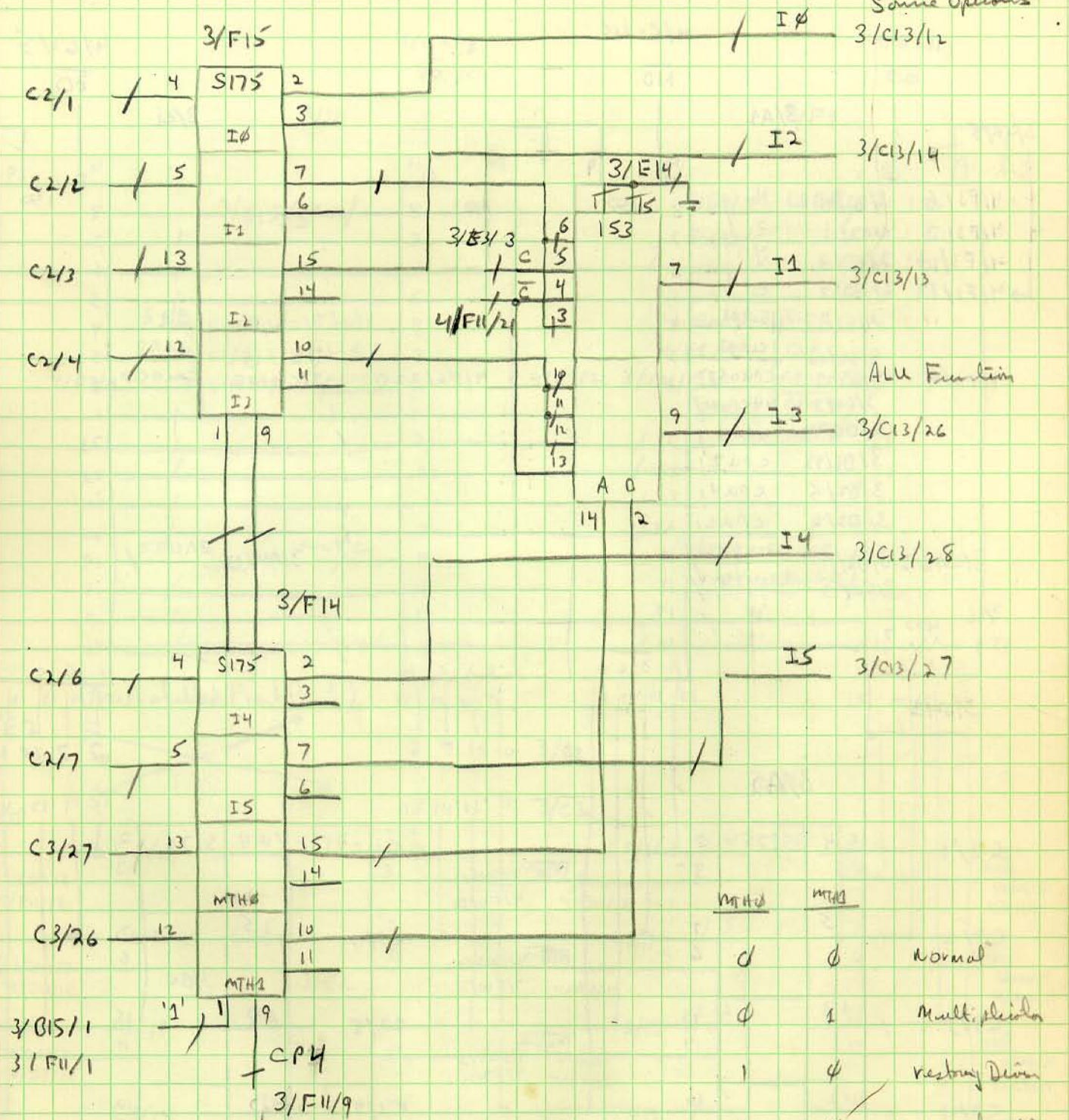
CPU Panel #1 Selectors Status

CPU Panel #1 I/O Control

Carry IN Logic



CPU Source & Operation Coding with Conditional Math control.



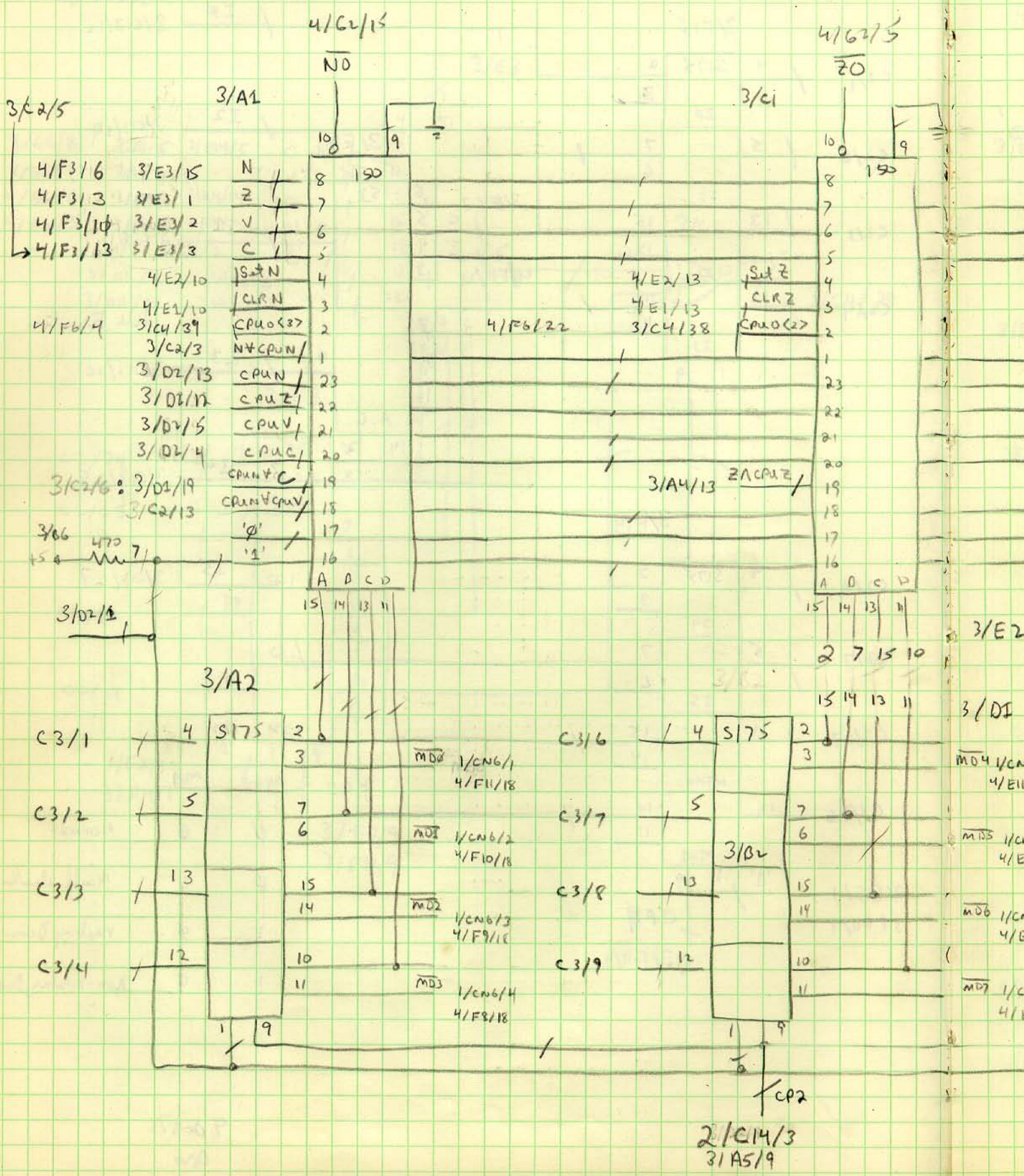
9 Oct 75
AGM

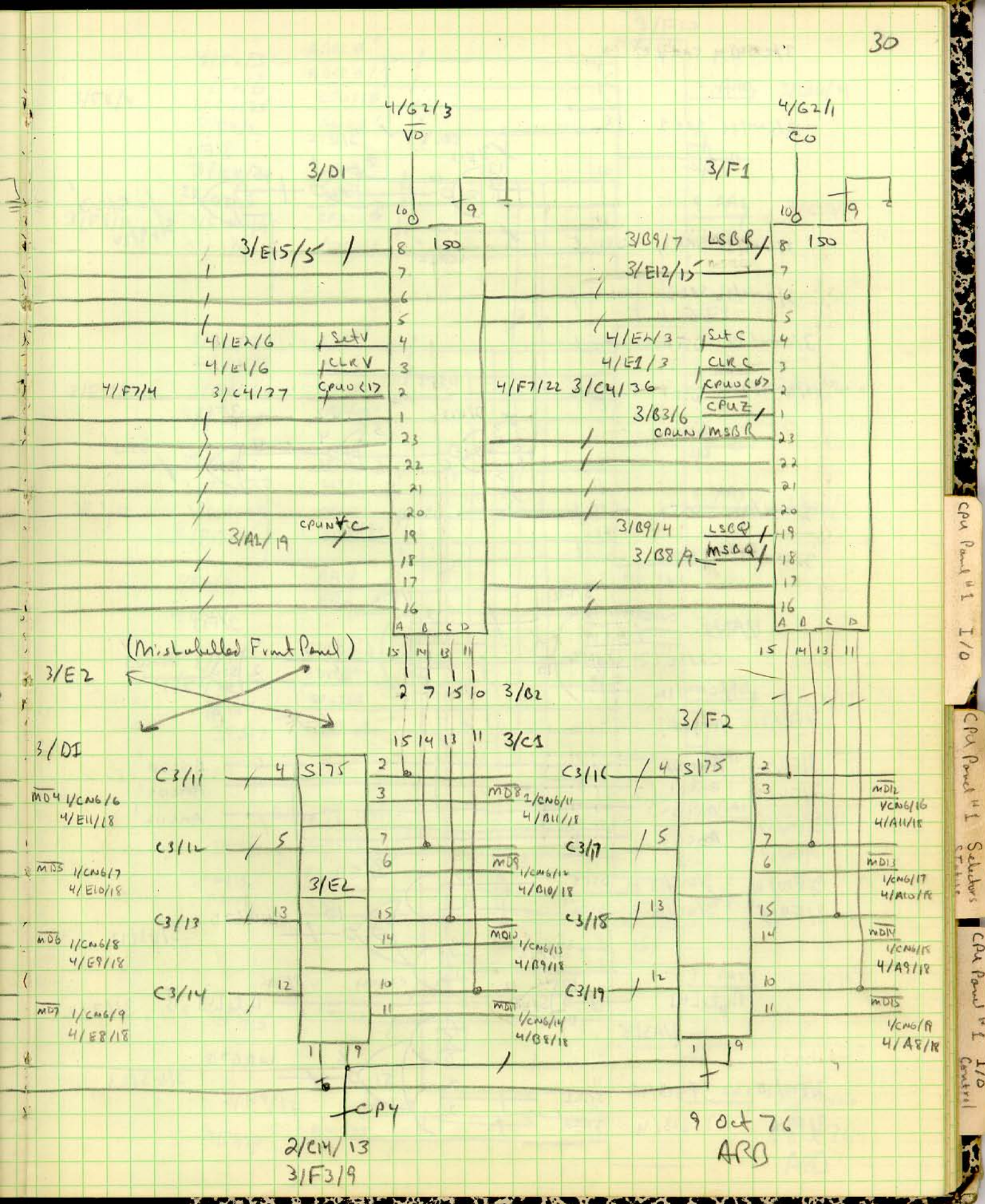
CPU Panel #1 I/O

CPU Panel #1 Selectors Status

CPU Panel #1 I/O Control

Processor Status Selection

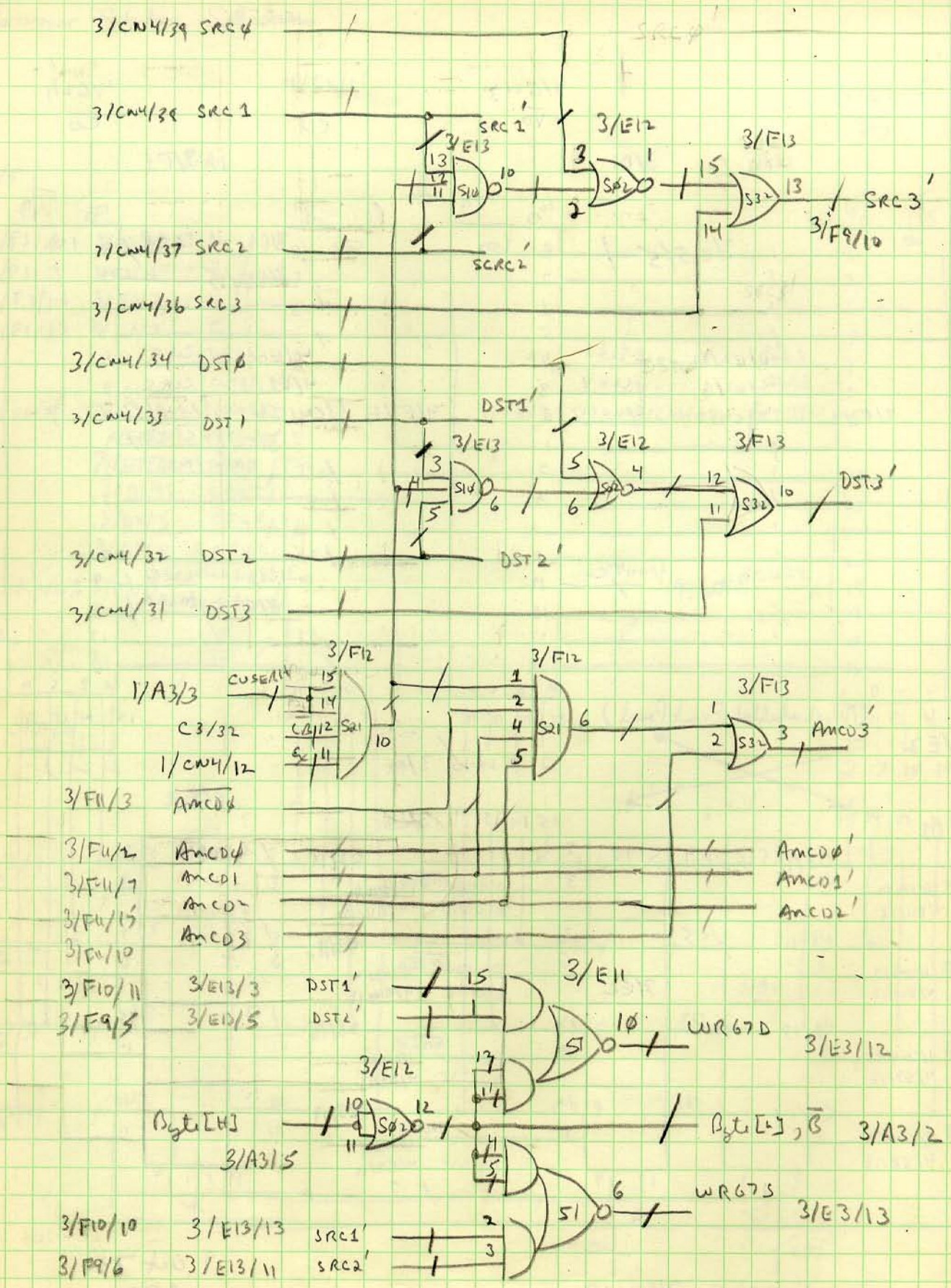


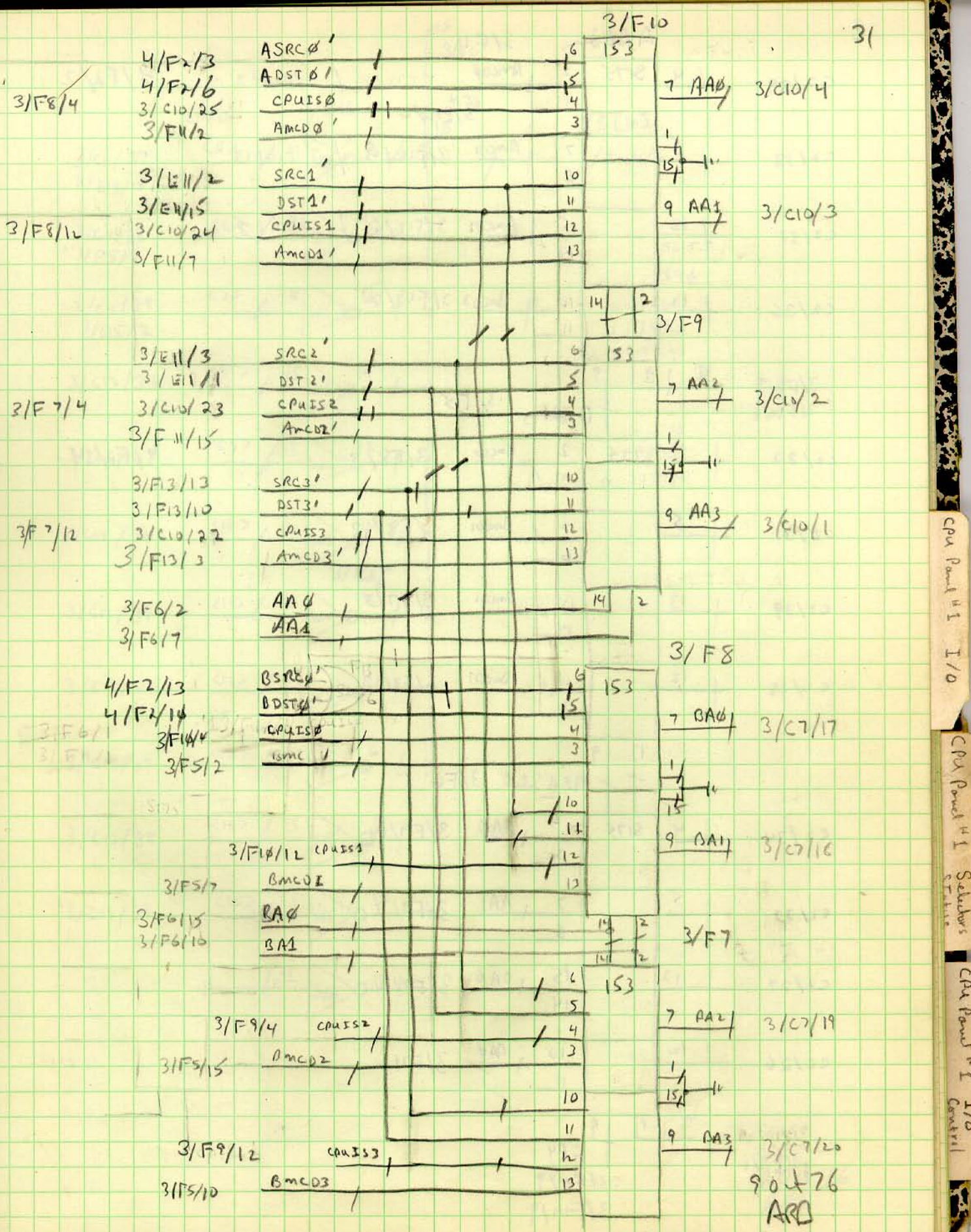


CPU Panel #1 I/O

CPU Panel #1 Selectors

CPU Panel #1 I/O Control

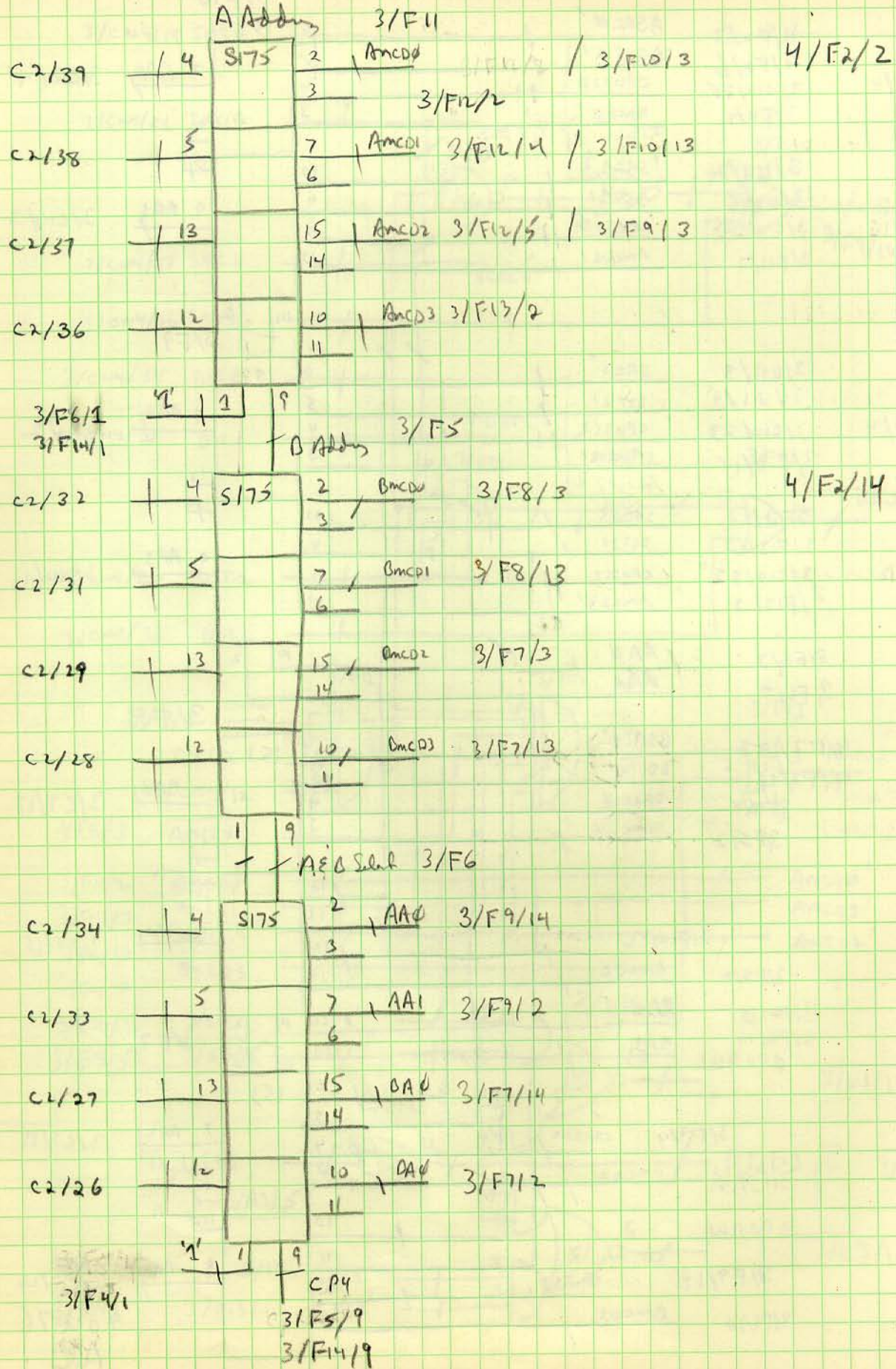

3/CN4/39 SRC4
3/CN4/38 SRC1
SRC1'
3/E13
3/E12
3/F13
SRC3'
3/F9/10
7/CN4/37 SRC2
SCRC2'
3/CN4/36 SRC3
3/CN4/34 DST0
3/CN4/33 DST1
DST1'
3/E13
3/E12
3/F13
DST3'
3/CN4/32 DST2
DST2'
3/CN4/31 DST3
3/F12
3/F12
3/F13
1/A3/3
CUSERIN
C3/32
1/CN4/12
AMCO3'
3/F11/3 AMCO0
3/F11/2 AMCO0
3/F11/7 AMCO1
3/F11/15 AMCO2
3/F11/10 AMCO3
AMCO0'
AMCO1'
AMCO2'
3/F10/11 3/E13/3 DST1'
3/F9/5 3/E10/5 DST2'
3/E11
WRG7D
3/E3/12
3/E12
Byte[H]
3/A3/5
Byte[L], B̄
3/A3/2
WRG7S
3/E3/13
3/F10/10 3/E13/13 SRC1'
3/F9/6 3/E13/11 SRC2'

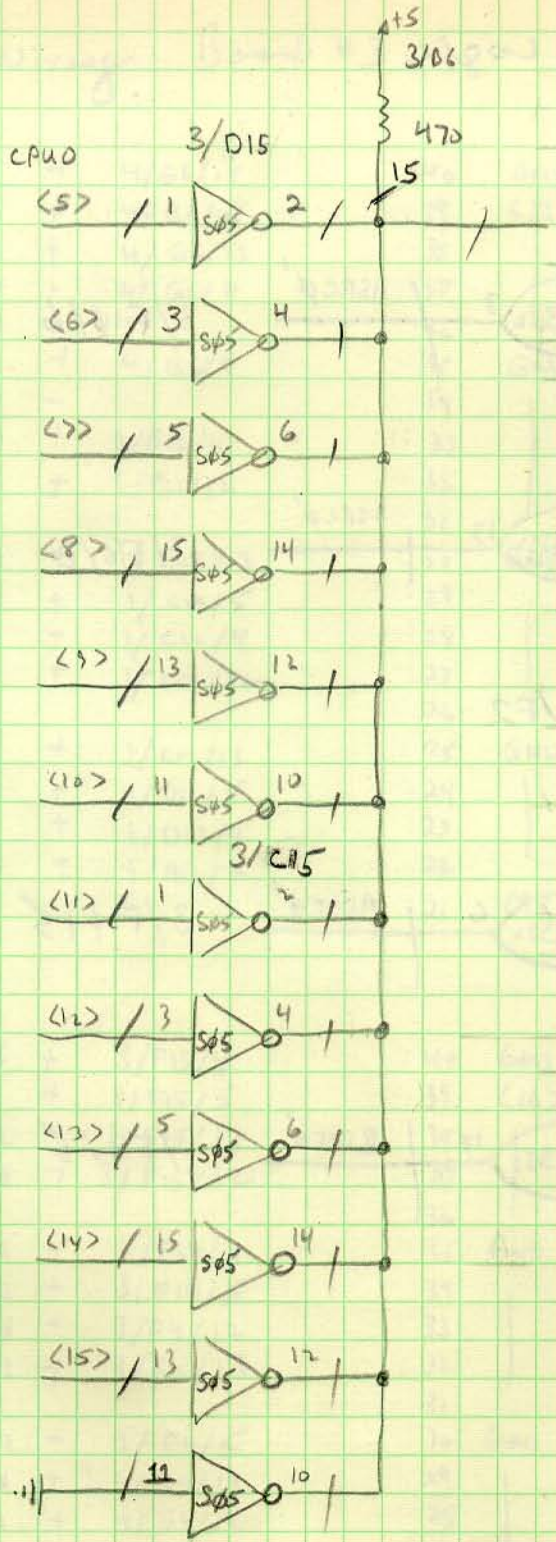


CPU Panel #1 I/O

CPU Panel #1 Selectors

CPU Panel #1 I/O Control


A Addrs
3/F11
C2/39
4
S175
2
AmCD0
3/F10/3
4/F2/2
3
3/F12/2
C2/38
5
7
AmCD1
3/F12/4
3/F10/13
6
C2/37
13
15
AmCD2
3/F12/5
3/F9/3
14
C2/36
12
10
AmCD3
3/F13/2
11
'1'
1
9
3/F6/1
3/F14/1
B Addrs
3/F5
C2/32
4
S175
2
BmCD0
3/F8/3
4/F2/14
3
C2/31
5
7
BmCD1
3/F8/13
6
C2/29
13
15
BmCD2
3/F7/3
14
C2/28
12
10
BmCD3
3/F7/13
11
1
9
A Eb Sel
3/F6
C2/34
4
S175
2
AA0
3/F9/14
3
C2/33
5
7
AA1
3/F9/2
6
C2/27
13
15
BA0
3/F7/14
14
C2/26
12
10
BA1
3/F7/2
11
'1'
1
9
CP4
3/F4/1
3/F5/9
3/F14/9



360
346
000360
177440
1 000020

330
177440
0 177770

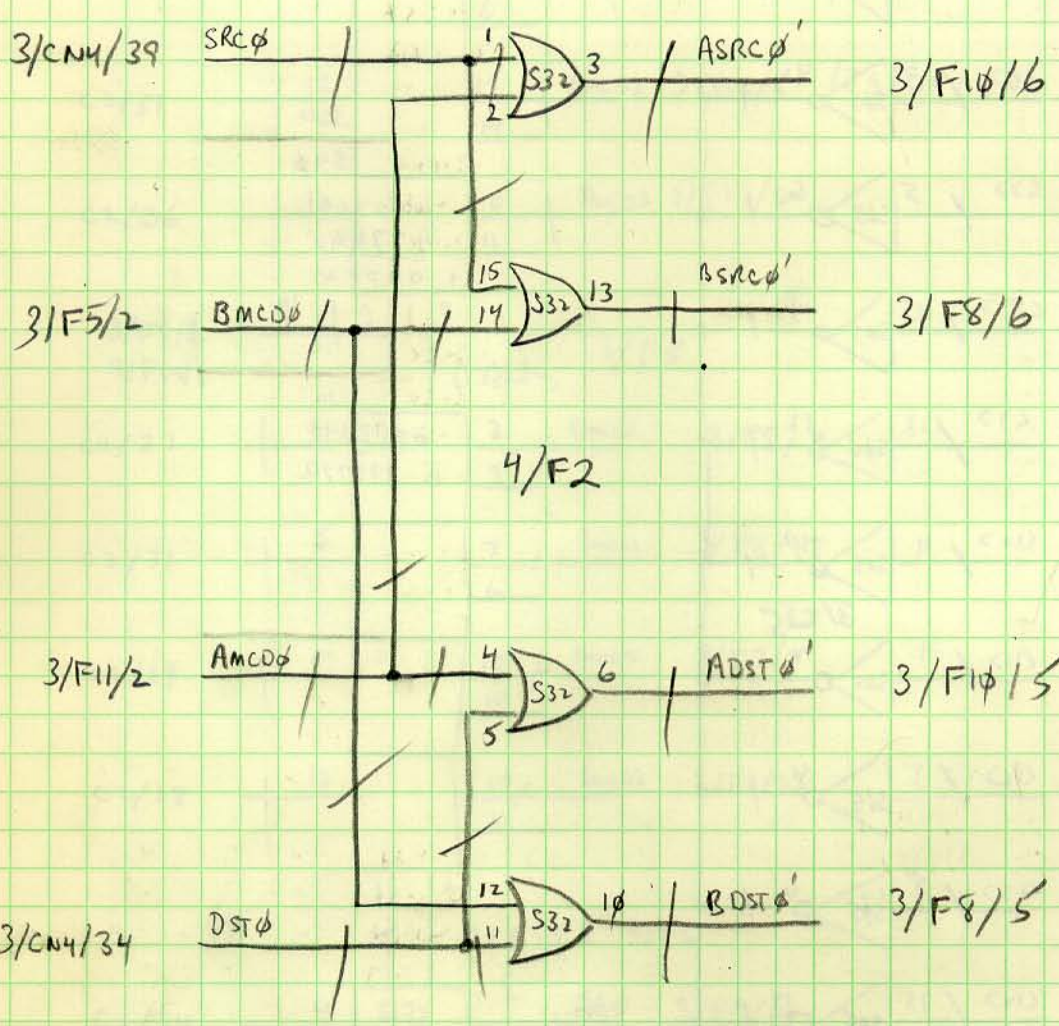
CPU Panel #1 I/O

CPU Panel #1 Selectors

CPU Panel #1 I/O Control

12 Oct 76
AM

SRC & DST ORING Logic



Added

6 May 78

AB

Connector Wiring Board #3

#1 (IN)

1	<64>	B-BR0	+	4/G6/15
2		B-BR1	+	4/G6/14
3		B-BR2	+	4/G6/13
4		B-BR3	+	4/G6/11
5	GND			
6		B-BR4	+	4/G6/9
7		B-BR5	-	
8		D-IO0	+	1/B12/4
9		D-IO1	+	1/B12/12
10	GND			
11		D-IO2	+	1/B12/13
12		D-IO3	+	1/C12/5
13		D-IO4	+	1/C12/4
14		D-IO5	+	1/C12/12
15	GND			
16		D-IO6	+	1/C12/13
17		D-IO7	+	1/D12/5
18		D-IO8	+	1/D12/4
19	<79>	D-IO9	+	1/B12/5
20	GND			

40	GND			
39	<80>	B-CA0	+	4/F7/9
38		B-CA1	+	4/F7/8
37		B-CA2	+	4/F7/7
36		B-CA3	+	4/F7/2
35	GND			
34		B-CA4	+	4/F7/1
33		B-CA5	+	4/F7/23
32		B-CA6	+	4/B2/11
31		B-CA7	-	1/B3/4
30	GND			
29		B-CA8	-	1/B3/2
28		B-CA9	-	1/B3/11
27		B-CA10	-	
26		B-CA11	-	
25	GND			
24		B-CO0	-	4/G11
23		B-CO1	-	4/G12
22		B-CO2	+	4
21	<95>	B-CO3	+	1/A5/11

#2 (IN)

1	<0>	D-S0	+	3/F15/4
2		D-S1	+	3/F15/5
3		D-S2	+	3/F15/13
4		D-F0	+	3/F15/12
5	GND			
6		D-F1	+	3/F14/4
7		D-F2	+	3/F14/5
8		D-D0	+	3/F4/12
9		D-D1	+	3/F4/13
10	GND			
11		D-D2	+	3/F4/5
12		D-A0	+	4/G4/13
13		D-A1	+	4/G4/12
14		D-A2	+	4/G4/4
15	GND			
16		D-DS0	+	4/G5/13
17		D-DS1	+	4/G5/12
18		D-DS2	+	4/G5/4
19	<157>	D-DS3	+	4/G5/5
20	GND			

40	GND			
39	<16>	D-AD0	+	3/F11/4
38		D-AD1	+	3/F11/5
37		D-AD2	+	3/F11/13
36		D-AD3	+	3/F11/12
35	GND			
34		D-AS0	+	3/F6/4
33		D-AS1	+	3/F6/5
32		D-BD0	+	3/F5/4
31		D-BD1	+	3/F5/5
30	GND			
29		D-BD2	+	3/F5/13
28		D-BD3	+	3/F5/12
27		D-BS0	+	3/F6/13
26		D-BS1	+	3/F6/12
25	GND			
24		D-CC0	+	3/F3/4
23		D-CC1	+	3/F3/5
22		D-CC2	+	3/F3/13
21	<317>	D-CC3	+	3/F3/12

Connector Wiring Board #3

#3

1	<32>	D-N0	+3/A2/4
2		D-N1	+3/A2/5
3		D-N2	+3/A2/13
4		D-N3	+3/A2/12
5	GND		
6		D-Z0	+ 3/B2/4
7		D-Z1	+ 3/B2/5
8		D-Z2	+ 3/B2/13
9		D-Z3	+ 3/B2/12
10	GND		
11		D-V0	+ 3/E2/4
12		D-V1	+ 3/E2/5
13		D-V2	+ 3/E2/13
14		D-V3	+ 3/E2/12
15	GND		
16		D-C0	+ 3/F2/4
17		D-C1	+ 3/F2/5
18		D-C2	+ 3/F2/13
19	<47>	D-C3	+ 3/F2/12
20	GND		

40	GND		
39	<48>	D-SR0	+ 3/B15/4
38		D-SR1	+ 3/B15/5
37		D-SR2	+ 3/B15/13
36		D-SR3	+ 3/B15/12
35	GND		
34		D-SR4	+ 3/A5/4
33		D-SR5	+ 3/F4/4 // 1/CN6/32
32		B-$\overline{CB}$	+ 3/F12/12 // 1/A7/14
31		D-BC0	+ 3/A5/5
30	GND		
29		D-BC1	+ 3/A5/13
28		D-BC2	+ 3/A5/12
27		D-MA0	+ 3/F14/13
26		D-MA1	+ 3/F14/12
25	GND		
24		D-CL0	+ 2/A15/14
23		D-CL1	+ 2/A15/2
22		D-CCL	+ 4/A1/2
21	<63>	D-CFP	+ 4/G4/5

#4

1	LD IR	+	4/G3/9
2	LB IR	+	2/C12/13
3	HB IR	+	2/C12/10
4	ST IR DCD	+	2/C11/10
5	GND		
6	IR DCD	+	2/C10/1
7	PCR WLB	+	4/G13/6
8	PCR WHB	+	4/G14/6
9	PCR READ	+	4/G15/6
10	GND		
11	XL	+	2/CN2/28
12	XH	+	2/CN2/27
13	XA	+	2/CN2/26
14	WAIT H	+	2/C11/2
15	GND		
16	EP-E6 [1]	+	4/C1/12
17		—	
18	IR BUSY L	+	2/C9/14
19	PSR4	—	
20	GND		

40	GND			
39	SRC0	+		3/F10/6
38	SRC1	+		3/F8/10
37	SRC2	+		3/F7/6
36	SRC3	+		3/F13/14
35	GND			
34	DST0	+		3/F8/5
33	DST1	+		3/F8/11
32	DST2	+		3/F7/5
31	DST3	+		3/F13/11
30	GND			
29	Byte	+		3/E12/11
28	Special	+		1/C18/5
27	UDA	+		1/D8/13
26	$\overline{LHHD}$	+		1/D12/12
25	GND			
24	WLB	Strobe	+	4/G13/12
23	WHB	Strobe	+	4/G14/12
22	Read	Strobe	+	4/G15/12
21				

Connector Wiring Board # 1

14 Oct 76 34

#4

1	YS[H]	+	3/D15/2
2	$\overline{\text{CPUC}}$	+	3/E12/15
3	CPUOØ	+	3/C10/36
4	OASC	+	4/G3/7
5	GND		
6	CSOR	+	4/G12/13
7	TMOT L	+	1/C1/4
8	ODDADD L	+	1/D9/10
9	MMGTER L	+	1/C1/6
10	GND		
11	INIT CLEAR L	+	1/A10/2 + 1/G14/5
12	EX	+	3/F12/11
13	SYSTEM RESET [L]	+	2/B14/2 + 4/G1/15
14	INIT TRIGGER [L]	+	1/D4/2
15	GND		
16	TDC LO	+	1/E4/14
17	RDC LO	+	1/E4/13
18	TAC LO	T	1/E4/11
19	RAC LO	+	1/E4/10
20	GND		

40	GND		
39	C	+	1/A2/2
38	V	+	1/A2/14
37	Z	+	1/A1/1
36	N	+	1/A2/1
35	GND		
34	CVZ	+	1/A1/13
33	C+N	+	1/A2/3
32	V+N	+	1/A2/13
31	(V+N)VZ	+	1/A1/3
30	GND		
29	SPCLH	+	2/C15/2
28			
27			
26	$\overline{\text{CPL}}$	+	2/A14/6
25	GND		
24	$\overline{\text{IA}}'$	+	1/E9/9
23	$\overline{\text{IB}}'$	+	1/E9/7
22	$\overline{\text{IC}}'$	+	1/E9/6
21	IEO	−	1/E9/15

#5 (OUT)

1	<16>	B - $\overline{\text{ADØ}}$	+	3/F11/3
2	|	B - $\overline{\text{AD1}}$	+	3/F11/6
3	|	B - $\overline{\text{AD2}}$	+	3/F11/14
4	|	B - $\overline{\text{AD3}}$	+	3/F11/11
5	GND			
6	|	B - $\overline{\text{ASØ}}$	+	3/F6/3
7	|	B - $\overline{\text{AS1}}$	+	3/F6/6
8	|	B - $\overline{\text{BDØ}}$	+	3/F5/3
9	|	B - $\overline{\text{BD1}}$	+	3/F5/6
10	GND			
11	|	B - $\overline{\text{BD2}}$	+	3/F5/14
12	|	B - $\overline{\text{BD3}}$	+	3/F5/11
13	|	B - $\overline{\text{BSØ}}$	+	3/F6/14
14	|	B - $\overline{\text{BS1}}$	+	3/F6/11
15	GND			
16	|	B - $\overline{\text{CCØ}}$	+	3/F3/3
17	|	B - $\overline{\text{CC1}}$	+	3/F3/6
18	|	B - $\overline{\text{CC2}}$	+	3/F3/14
19	<31>	B - $\overline{\text{CC3}}$	+	3/F3/11
20	GND			

40	GND			
39	<Ø>	B - $\overline{\text{SØ}}$	+	3/F15/3
38	|	B - $\overline{\text{S1}}$	+	3/F15/6
37	|	B - $\overline{\text{S2}}$	+	3/F15/14
36	|	B - $\overline{\text{FØ}}$	+	3/F15/11
35	GND			
34	|	B - $\overline{\text{F1}}$	+	3/F14/3
33	|	B - $\overline{\text{F2}}$	+	3/F14/6
32	|	B - $\overline{\text{DØ}}$	+	3/F4/11
31	|	B - $\overline{\text{D1}}$	+	3/F4/14
30	GND			
29	|	B - $\overline{\text{D2}}$	+	3/F4/6
28	|	B - $\overline{\text{AØ}}$	+	4/G4/14
27	|	B - $\overline{\text{A1}}$	+	4/G4/11
26	|	B - $\overline{\text{A2}}$	+	4/G4/3
25	GND			
24	|	B - $\overline{\text{DSØ}}$	+	4/G5/14
23	|	B - $\overline{\text{DS1}}$	+	4/G5/11
22	|	B - $\overline{\text{DS2}}$	+	4/G5/3
21	<15>	B - $\overline{\text{DS3}}$	+	4/G5/6

CPU Panel #1 I/O

CPU Panel #1 Selectors Status

CPU Panel #1 I/O Control

Connector wiring Board # 1

#6 (out)

1	<32>	B-$\overline{N0}$	+	3/A2/3	40	GND		
2	|	B-$\overline{N1}$	+	3/A2/6	39	<48>	B-$\overline{SR0}$	+ 3/B15/3
3	|	B-$\overline{N2}$	+	3/A2/14	38	|	B-$\overline{SR1}$	+ 3/B15/6
4		B-$\overline{N3}$	+	3/A2/11	37	|	B-$\overline{SR2}$	+ 3/B15/14
5	GND				36		B-$\overline{SR3}$	+ 3/B15/11
6	|	B-$\overline{Z0}$	+	3/B2/3	35	GND		
7	|	B-$\overline{Z1}$	+	3/B2/6	34	|	B-$\overline{SR4}$	+ 3/A5/3
8	|	B-$\overline{Z2}$	+	3/B2/14	33	|	B-$\overline{SR5}$	+ 3/F4/3
9		B-$\overline{Z2}$	+	3/B2/11	32	|	B-$\overline{CB}$	+ 1/A7/14
10	GND				31	|	B-$\overline{BC0}$	+ 3/A5/6
11	|	B-$\overline{V0}$	+	3/E2/3	30	GND		
12	|	B-$\overline{V1}$	+	3/E2/6	29	|	B-$\overline{BC1}$	+ 3/A5/14
13	|	B-$\overline{V2}$	+	3/E2/14	28	|	B-$\overline{BC2}$	+ 3 A5/11
14	|	B-$\overline{V3}$	+	3/E2/11	27	|	B-$\overline{MA0}$	+ 3/F14/14
15	GND				26	|	B-$\overline{MA1}$	+ 3/F14/11
16	|	B-$\overline{C0}$	+	3/F2/3	25	GND		
17	|	B-$\overline{C1}$	+	3/F2/6	24	|	B-$\overline{CLO}$	+ 2/A15/10
18	|	B-$\overline{C2}$	+	3/F2/14	23	|	B-$\overline{CL1}$	+ 4/G1/6
19	<47>	B-$\overline{C3}$	+	3/F2/11	22	|	B-$\overline{CCL}$	+ 4/A1/6
20	GND				21	<63>	B-$\overline{CTP}$	+

#7

1	$\overline{PV0}$	+	4/F11/22
2	$\overline{PV1}$	+	4/F10/22
3	$\overline{PV2}$	+	4/F9/22
4	$\overline{PV3}$	+	4/F8/22
5	GND	+	
6	$\overline{PV4}$	+	4/E11/22
7	$\overline{PV5}$	+	4/E10/22
8	$\overline{PV6}$	+	4/E9/22
9	$\overline{PV7}$	+	4/E8/22
10	GND		
11	$\overline{BCN1}$	+	4/G6/10
12	$\overline{BCN3}$	+	1/A3/6
13	UMDF[H]	−	1/CN2/5
14	INHBTL	+	1/D7/12
15	GND		
16	SCRA0	+	4/F7/17
17	SCRA1	+	4/F7/18
18	SCRA2	+	4/F7/19
19	SCRB Read Enable	+	4/F7/16
20	GND		

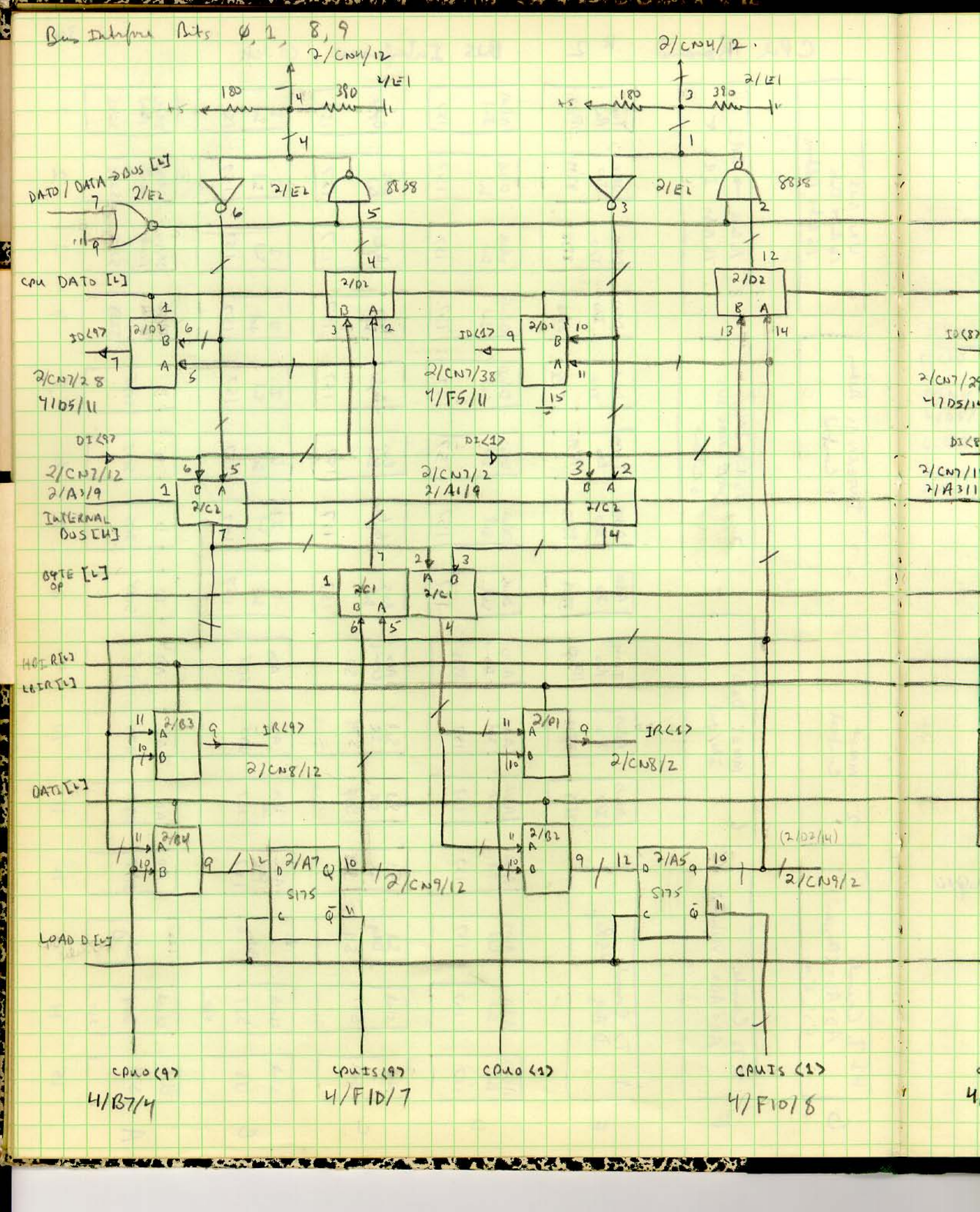
40	GND		
39	SCRB0	+	4/F7/13
38	SCRB1	+	4/F7/11
37	SCRB2	+	4/F6/13
36	SCRB3	+	4/F6/11
35	GND	+	
34	SCRB4		4/E7/13
33	SCRB5	+	4/E7/11
32	SCRB6	+	4/E6/13
31	SCRB7	+	4/E6/11
30	GND		
29	SCRB8	+	4/B7/13
28	SCRB9	+	4/B7/11
27	SCRB10	+	4/B6/13
26	SCRB11	+	4/B6/11
25	GND		
24	TBitH	+	1/A7/11
23	YSH	+	1/A7/3
22	PFH	+	1/A7/6
21	FDH	+	1/C7/15 + 4/G12/11

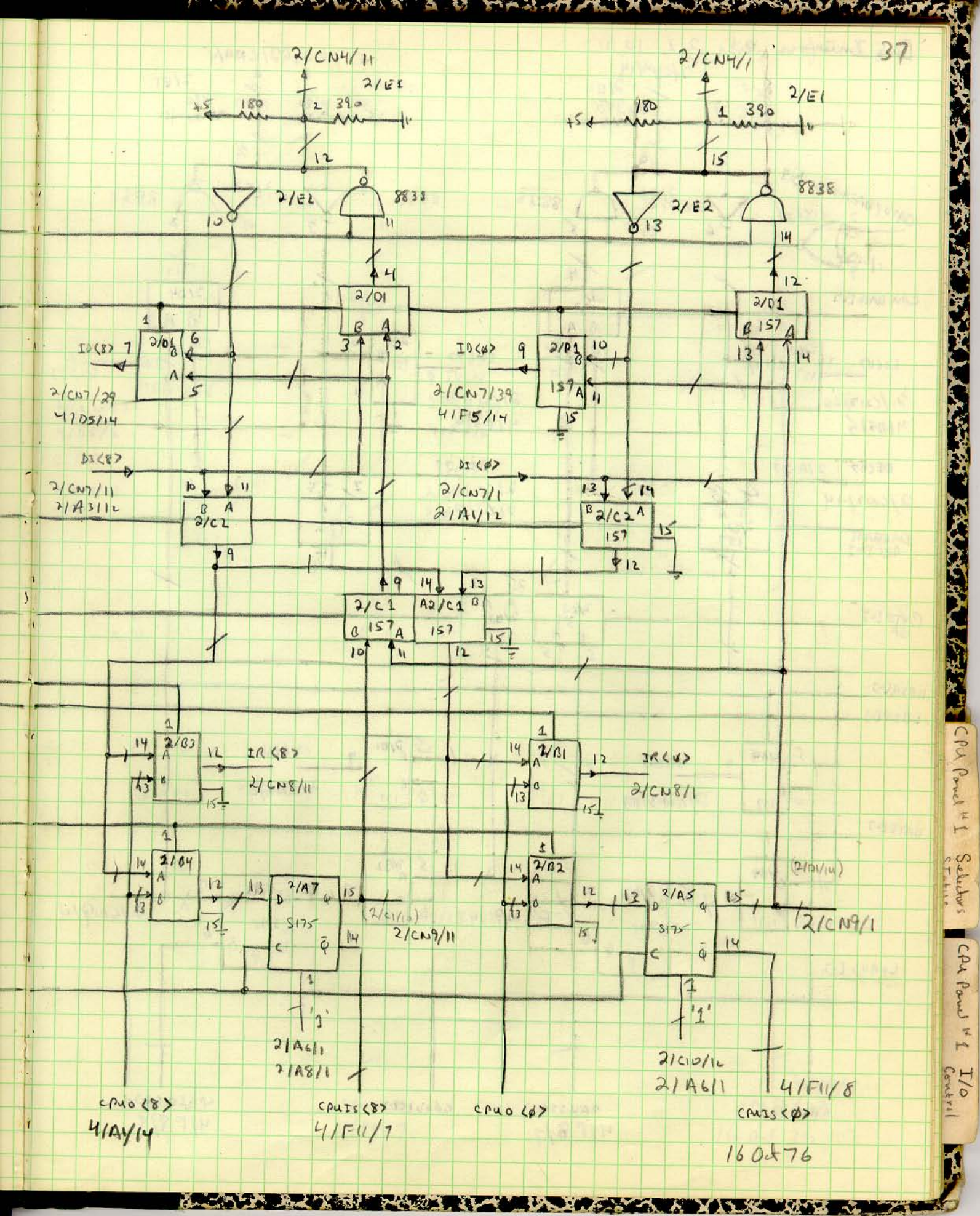
CPU Board # 2 BUS Interface / Clock

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
G	#1 To Console AD & ADx (Physical) C'v', 2', N'		2 MMGT Control				3 INTERNAL Addrs + Control					4 UNIBUS 16 Bits Data 18 Bits Address			
F	5 To Console AD & ADx (Virtual)						6 MMGT Data IN/out					7 16 Bits IN INTERNAL BUS 16 Bit out			8 16 Bits → IR1 16 Bits IR2 ←
E	9 To Console DReg, PSReg.				ABUS I/O 8838	ABUS I/O 8838	Term Res 180/390	ABUS I/O 8838	ABUS I/O 8838	Term Res 180/390	DBUS I/O 8838	DBUS I/O 8838	DBUS I/O 8838	DBUS I/O 8838	Term Res 180/390
D	ABUS Sel 157	ABUS Sel 157	ABUS Sel 157	ABUS Sel 157	ABUS Sel 157	ABUS Sel 157	ABUS I/O 8838	OBUS Sel 157	OBUS Sel 157	OBUS Sel 157	OBUS Sel 157	OBUS Sel 157	OBUS Sel 157	OBUS Sel 157	OBUS Sel 157
C	Clock S32	Clock S37	Sel DReg S11	Sel IR S08	Sel IR S04 clock	Sel IR S74	ADx Conds S11	BUS Sel 157	Byte 157	BUS Sel 157	Byte 157	Bus Sel 157	Byte 157	BUS Sel 157	Byte 157
B	clock 08	clock S37 560	120 Delay	ADx Sel 157	ADx Sel 157	ADx S175	ADx S175	D Sel 157	I Sel 157	D Sel 157	I Sel 157	D sel 157	I Sel 157	D Sel 157	I Sel 157
A	Clock S74	Clock S04 560	120 Delay	AD S175	AD S175	AD S175	AD S175	D S175	D S175	D S175	D S175	IR/SW Read S258	IR/SW Read S258	IR/SW Read S258	IR/SW Read S258

CPU Panel #1 Switches

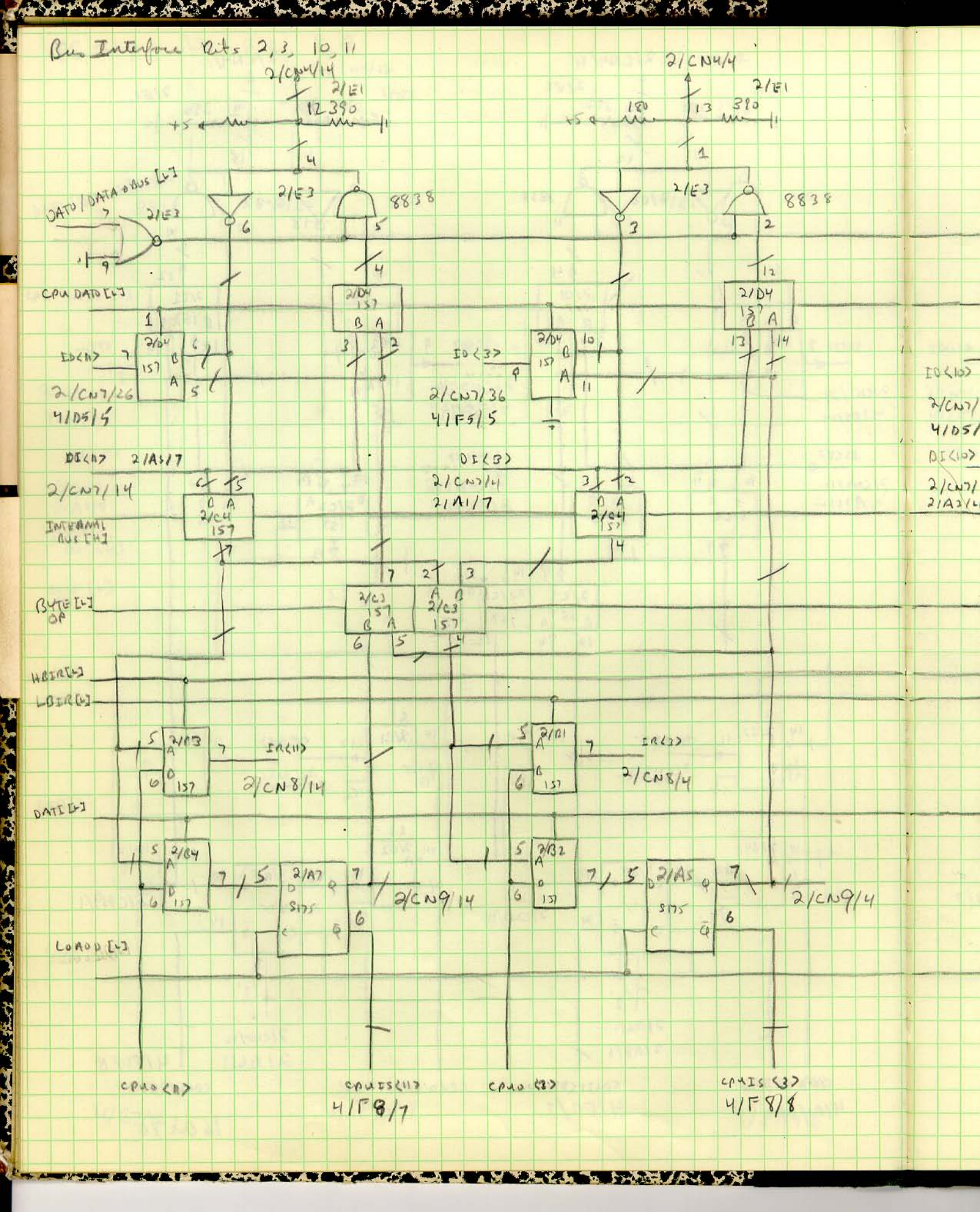
CPU Panel #1 I/O Control

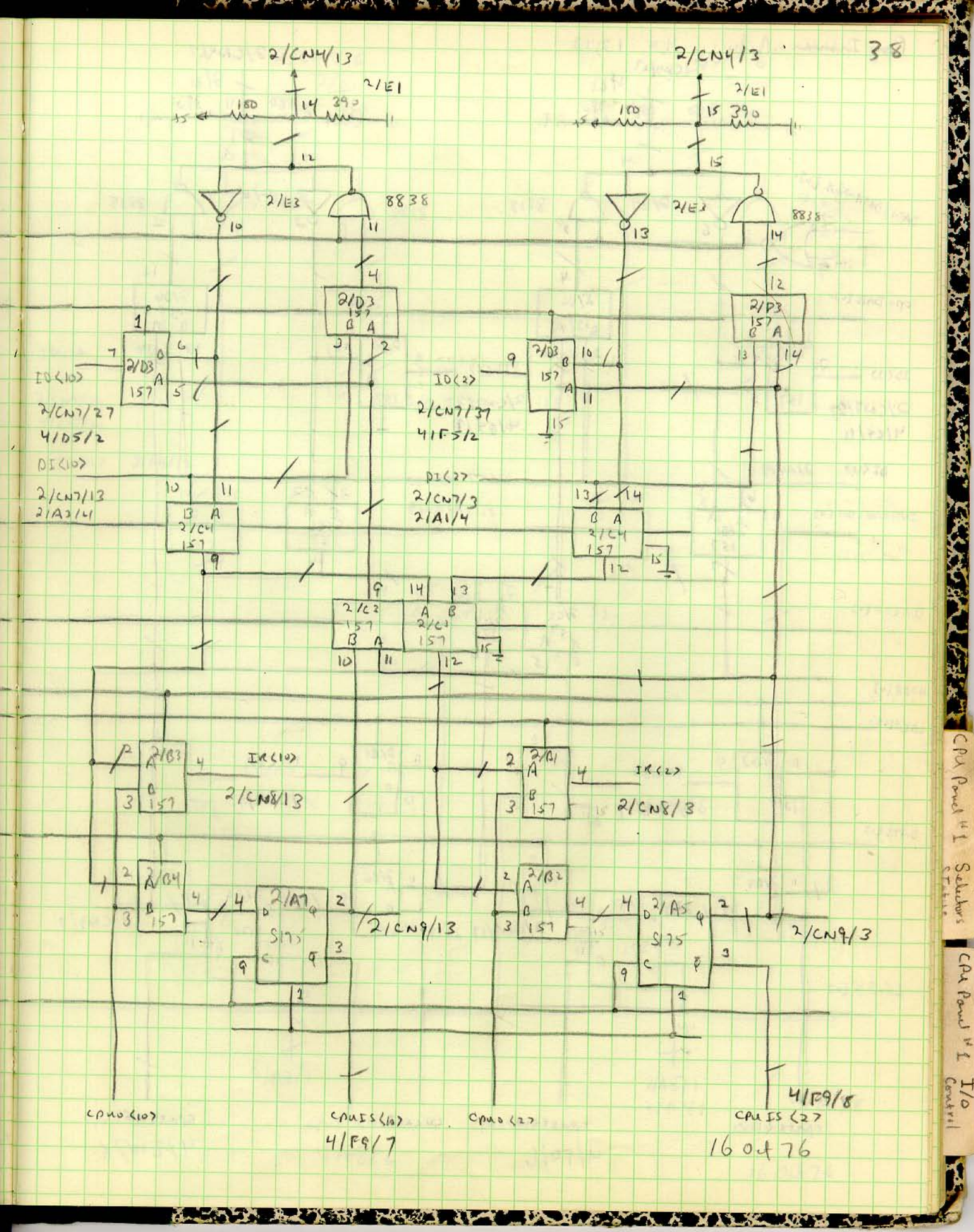

Bus Interface Bits 0, 1, 8, 9
2/CN4/12
2/CN4/2
2/LE1
180
390
+5
DATO / DATA → BUS [L]
2/E2
2/LE2
8838
CPU DATO [L]
2/D2
2/CN7/28
4/D5/11
2/CN7/38
4/F5/11
DI<9>
DI<1>
2/CN7/12
2/A3/9
2/CN7/2
2/A1/9
INTERNAL BUS [H]
2/C2
2/C1
BYTE OP [L]
HOLD [H]
LOIR [L]
2/B3
2/B1
IR<9>
IR<1>
2/CN8/12
2/CN8/2
DATO [L]
2/B4
2/B2
2/A7
2/A5
S175
2/CN9/12
(2/D2/14)
LOAD D [L]
CPUO<9>
4/B7/4
CPUIS<9>
4/F10/7
CPUO<1>
CPUIS<1>
4/F10/8

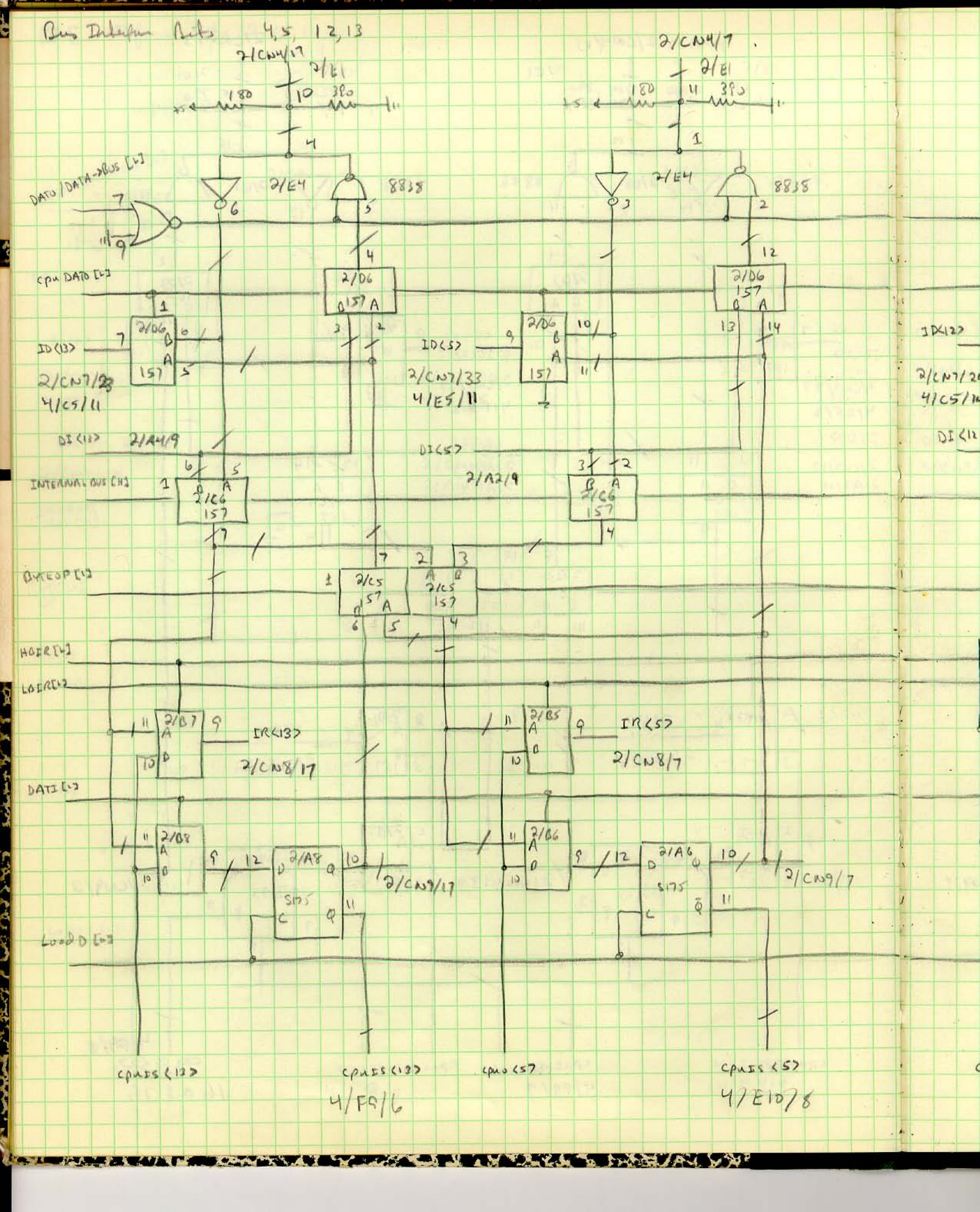


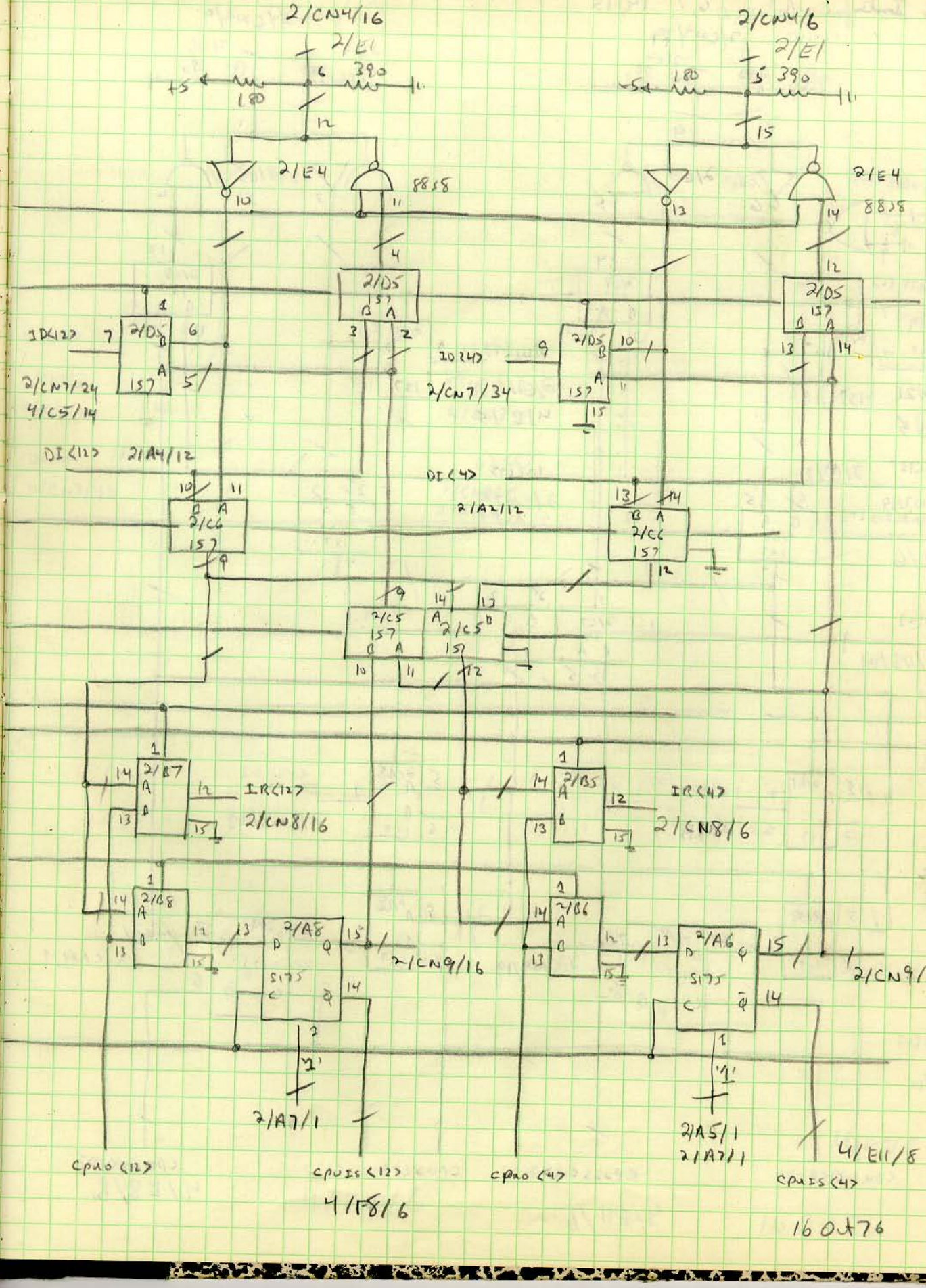
CPU Panel #1 Selectors

CPU Panel #1 I/O Control


Bus Interface Bits 2, 3, 10, 11
2/CN4/14
2/E1
12390
+5
4
2/E3
8838
DATO/DATA BUS [L]
DATO
2/E3
9
CPU DATO [L]
2/D4
157
ID<11>
2/CN7/26
4/D5/5
DI<11>
2/A3/7
2/CN7/14
INTERNAL BUS [H]
2/C4
157
BYTE [L] OP
2/C3
157
HOIR[H]
LOIR[L]
2/B3
IR<11>
2/CN8/14
DATI [L]
2/C4
2/A7
S175
LOAD [L]
2/CN9/14
CPUO<8>
CPUIS<11>
4/F8/7
2/CN4/4
180
390
2/CN7/36
4/F5/5
ID<3>
DI<3>
2/CN7/4
2/A1/7
2/B1
IR<3>
2/CN8/4
2/B2
2/A5
CPUO<3>
CPUIS<3>
4/F8/8
ID<10>
2/CN7/
4/D5/
DI<10>
2/CN7/
2/A3/4

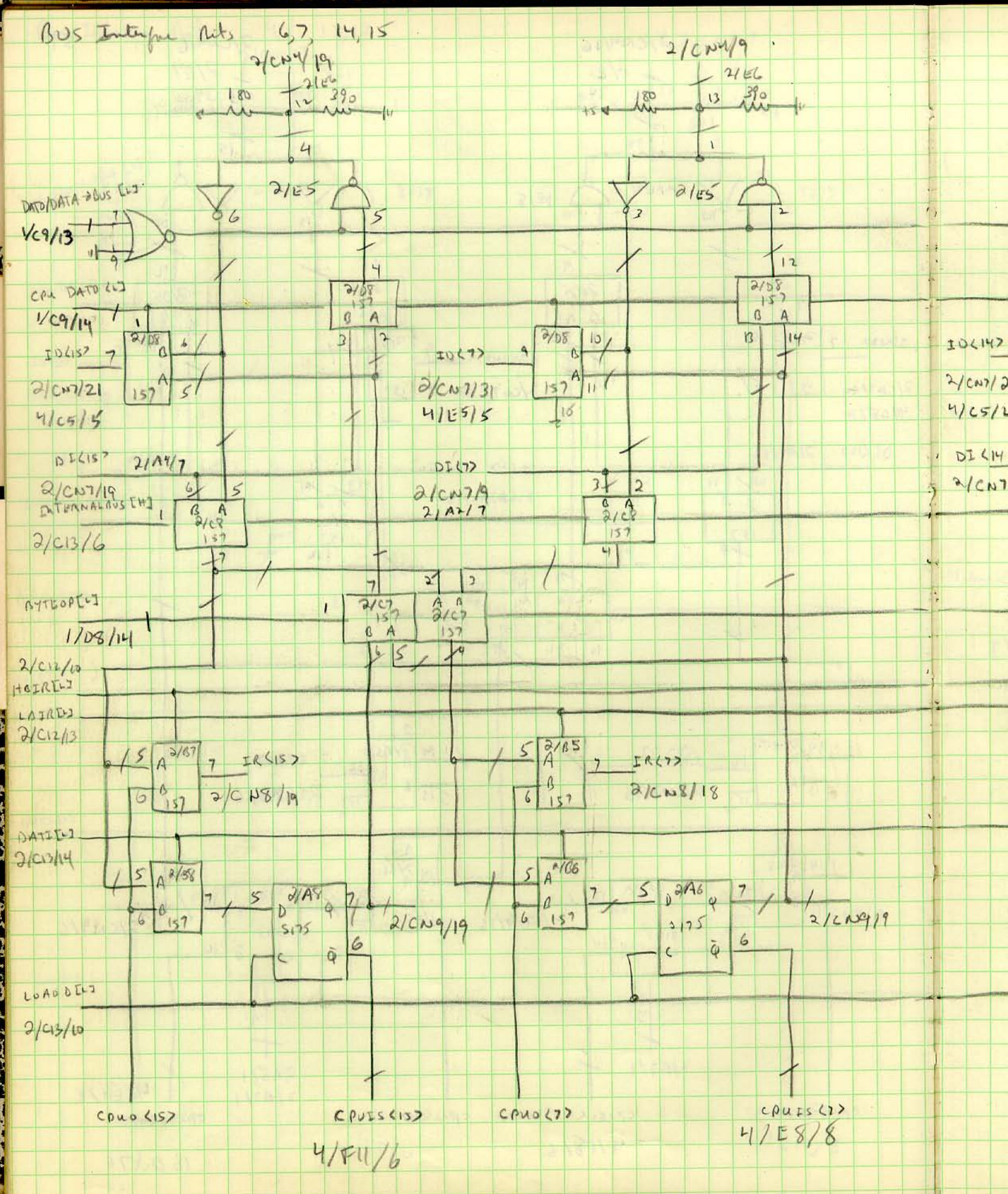

2/CN4/13
2/E1
180
390
2/E3
8838
2/D3
157
2/C4
157
2/C2
157
2/C1
157
2/B3
157
2/B4
157
2/B2
157
2/B1
157
2/A7
S175
2/A5
S175
ID<10>
2/CN7/27
4/D5/2
DI<10>
2/CN7/13
2/A3/4
ID<2>
2/CN7/37
4/F5/2
DI<2>
2/CN7/3
2/A1/4
IR<10>
2/CN8/13
IR<2>
2/CN8/3
2/CN9/13
2/CN9/3
CPUO<10>
CPUIS<10>
4/F9/7
CPUO<2>
CPUIS<2>
4/F9/8
16 of 76
CPU Panel #1 Selectors
CPU Panel #1 I/O Control

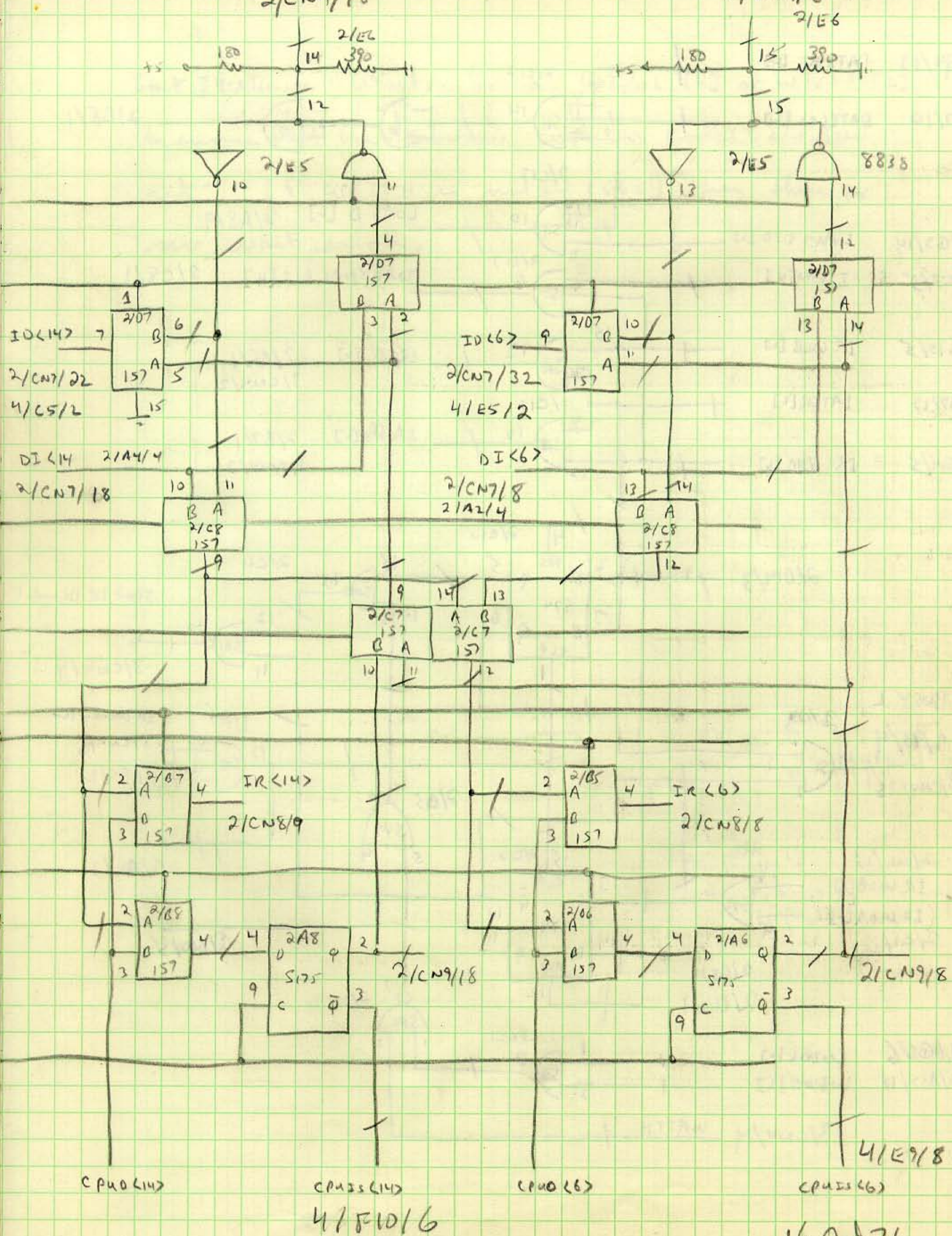

Bus Interface Auto 4,5, 12,13
2/CN4/17
2/E1
180
10
390
4
DATO/DATA→BUS [L]
2/E4
8838
7
6
5
9
CPU DATO [L]
2/D6
157
A
B
1
3
2
ID<13>
2/CN7/23
4/C5/11
DI<13>
2/A4/9
INTERNAL BUS [H]
2/C6
157
6
5
7
BYTEOP [L]
2/C5
157
HOIR [H]
LOIR [L]
2/B7
IR<13>
2/CN8/17
DATI [L]
2/B8
SN75
Load D [L]
cpuIS<13>
2/CN9/17
4/F9/6
ID<5>
2/CN7/33
4/E5/11
DI<5>
2/A2/9
2/B5
IR<5>
2/CN8/7
2/B6
2/A6
2/CN9/7
cpu<5>
cpuIS<5>
4/E10/8
IR<12>
DI<12>



CPU Panel #1 Selectors

CPU Panel #1 I/O Control

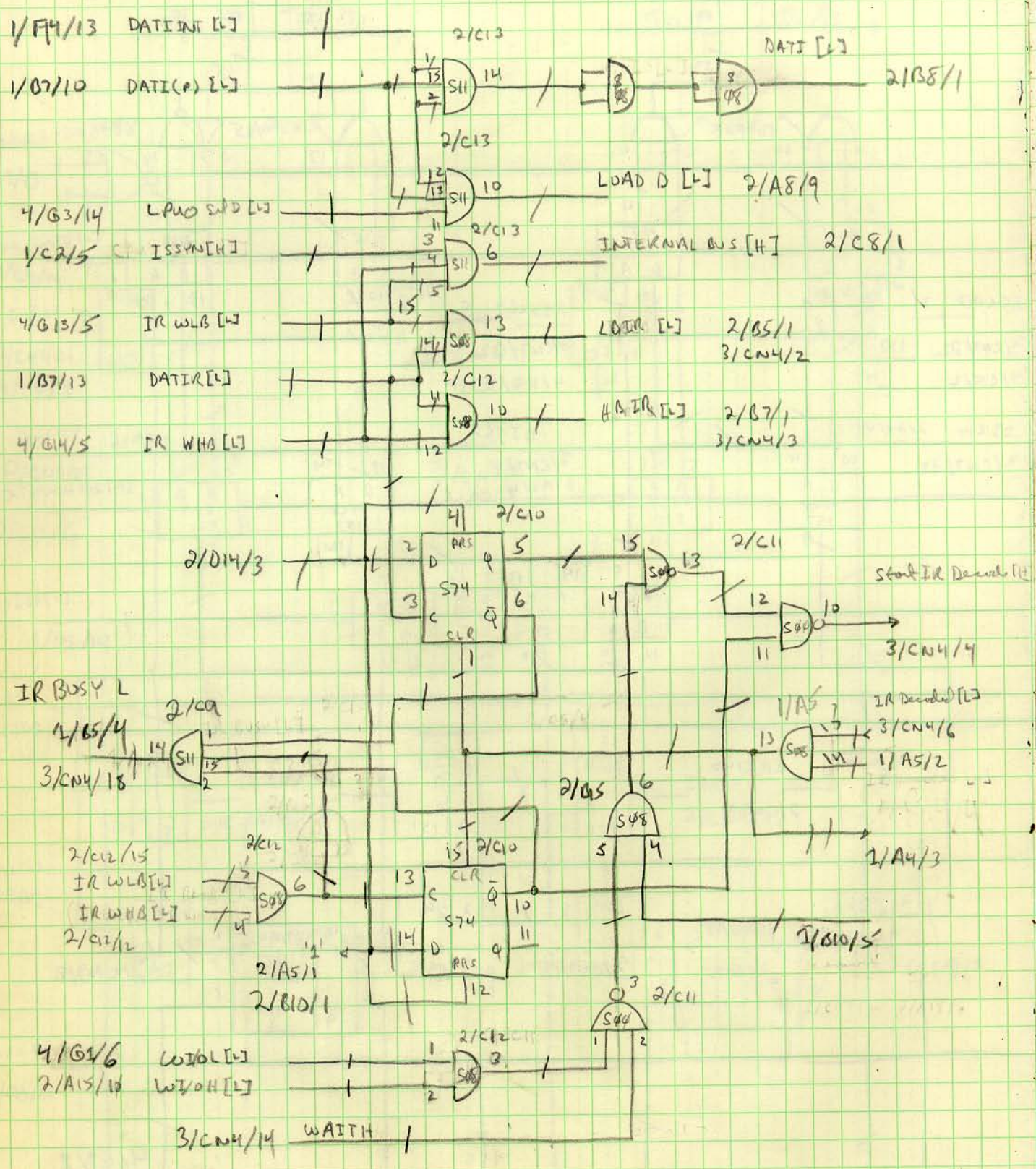

BUS Interface Bits 6, 7, 14, 15
2/CN4/19
2/CN4/9
180
390
2/E6
2/E5
DATO/DATA→BUS [L]
1/C9/13
CPU DATO [L]
1/C9/14
IO<15>
2/CN7/21
4/C5/5
IO<7>
2/CN7/31
4/E5/5
DI<15>
2/A4/7
DI<7>
2/CN7/19
INTERNALBUS [H]
2/C13/6
2/CN7/9
2/A7/7
BYTEOP [L]
1/D8/14
2/C12/10
HOIR [L]
LOIR [L]
2/C12/13
IR<15>
2/CN8/19
IR<7>
2/CN8/18
DATI [L]
2/C13/14
2/CN9/19
LOAD 0 [L]
2/C13/10
CPU0<15>
CPU15<15>
CPU0<7>
CPU15<7>
4/F11/6
4/E8/8



16 Oct 76

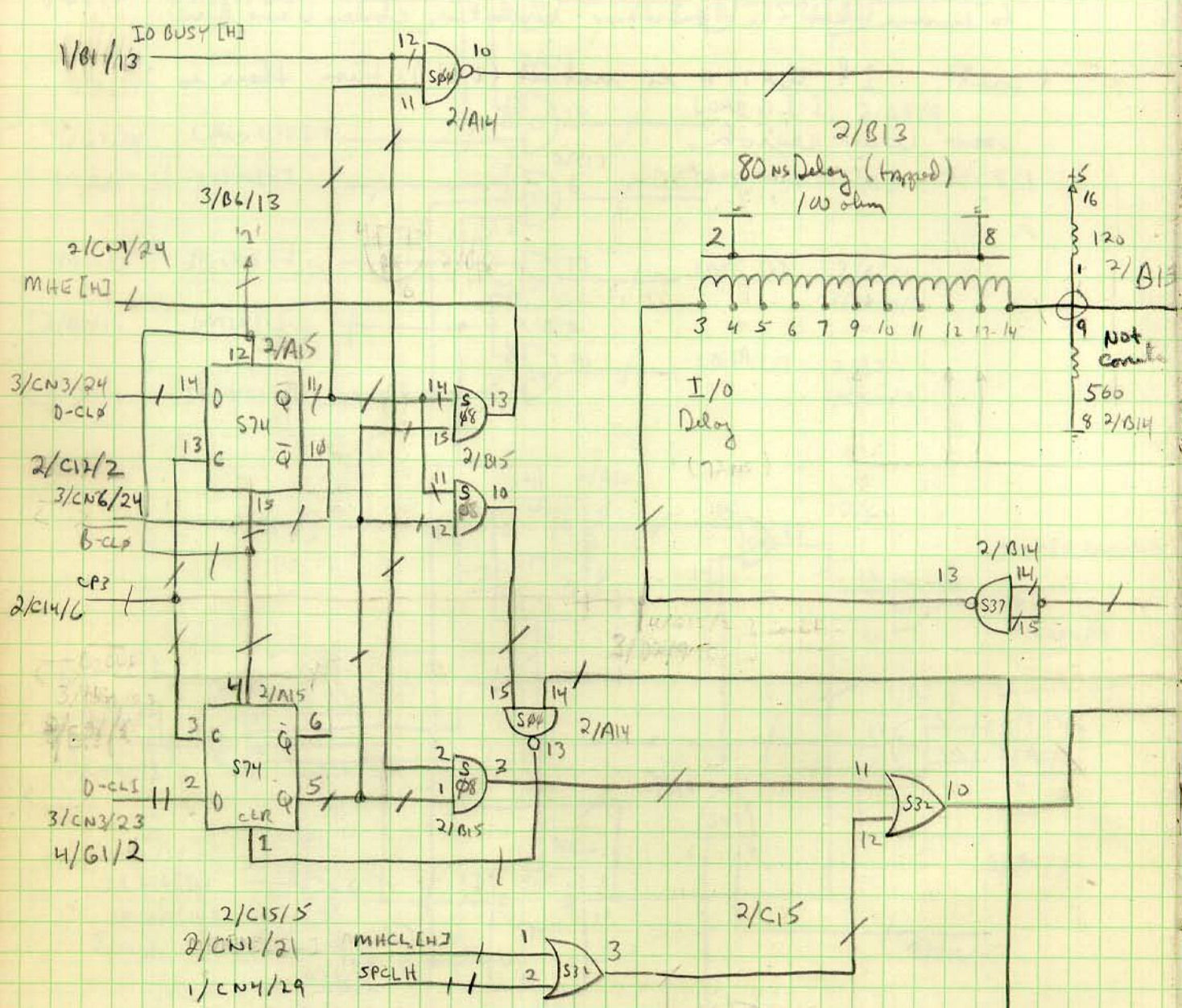
CPU Panel #1 Selectors Status

CPU Panel #1 I/O Control


1/F14/13 DATI INT [L]
1/B7/10 DATI(P) [L]
2/C13
DATI [L]
2/B8/1
LOAD D [L]
2/A8/9
4/G3/14 LPHO SW D [L]
1/C2/5 ISSYN [H]
INTERNAL BUS [H]
2/C8/1
4/G13/5 IR WLB [L]
LOIR [L]
2/B5/1
3/CN4/2
1/B7/13 DATIR [L]
2/C12
4/G14/5 IR WHB [L]
HAIR [L]
2/B7/1
3/CN4/3
2/C10
2/D14/3
2/C11
Start IR Decode [H]
3/CN4/4
IR BUSY L
2/C9
4/G5/4
3/CN4/18
IR Decoded [L]
3/CN4/6
1/A5/2
1/A4/3
2/C12/15
IR WLB [L]
IR WHB [L]
2/C12/12
2/A5/1
2/B10/1
2/B5
I/D10/5'
4/G4/6 LOIOL [L]
2/A15/10 LOIOH [L]
3/CN4/14 WAITH

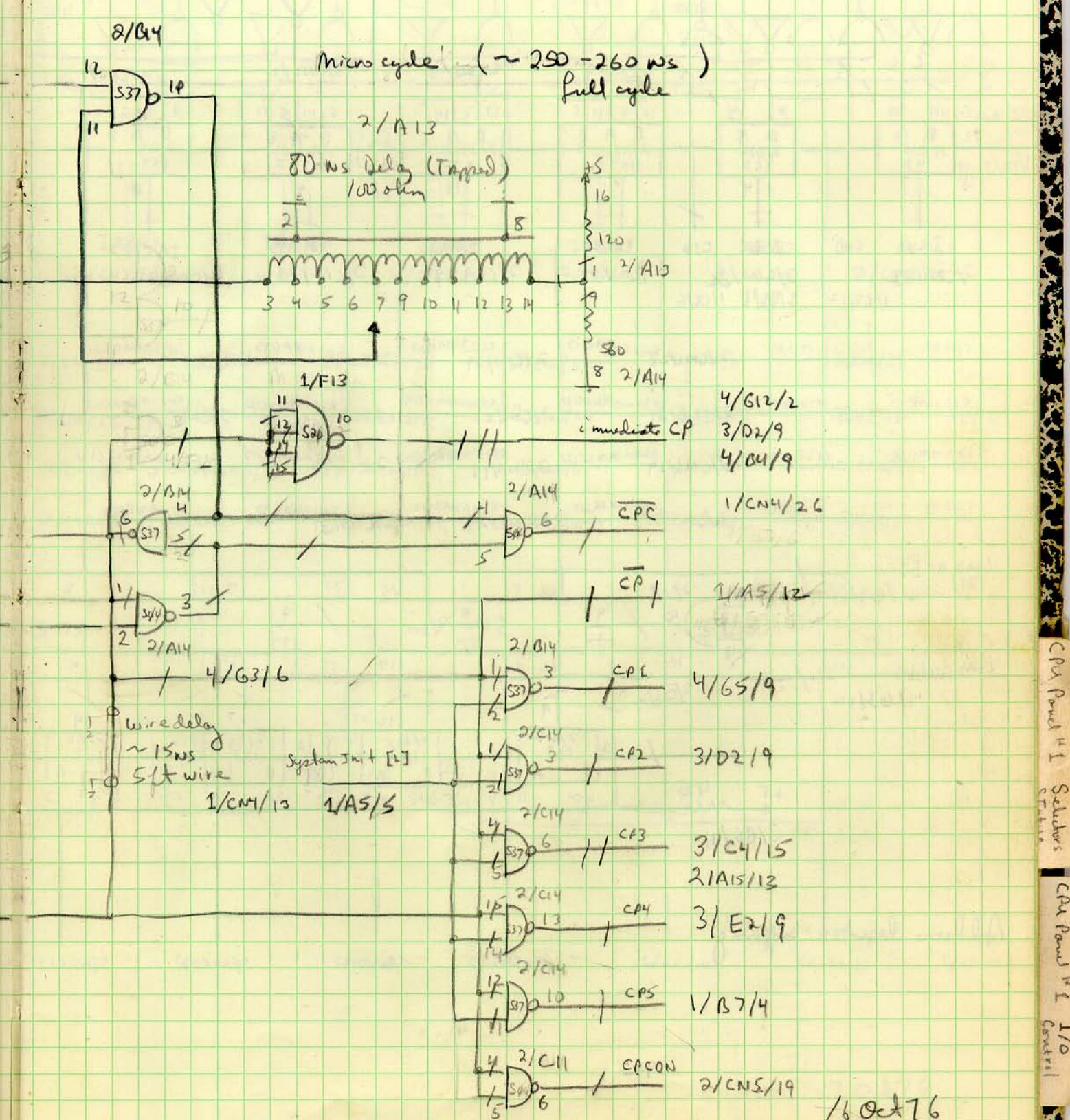
Stat IR Decode Waits for a WI/OL [L] or WI/OH [L] to ensure that the processor condition codes have been set. If WAITH is not set (i.e. L) then there is no wait period.

CP Clock



See page 76 for Buffered CL1

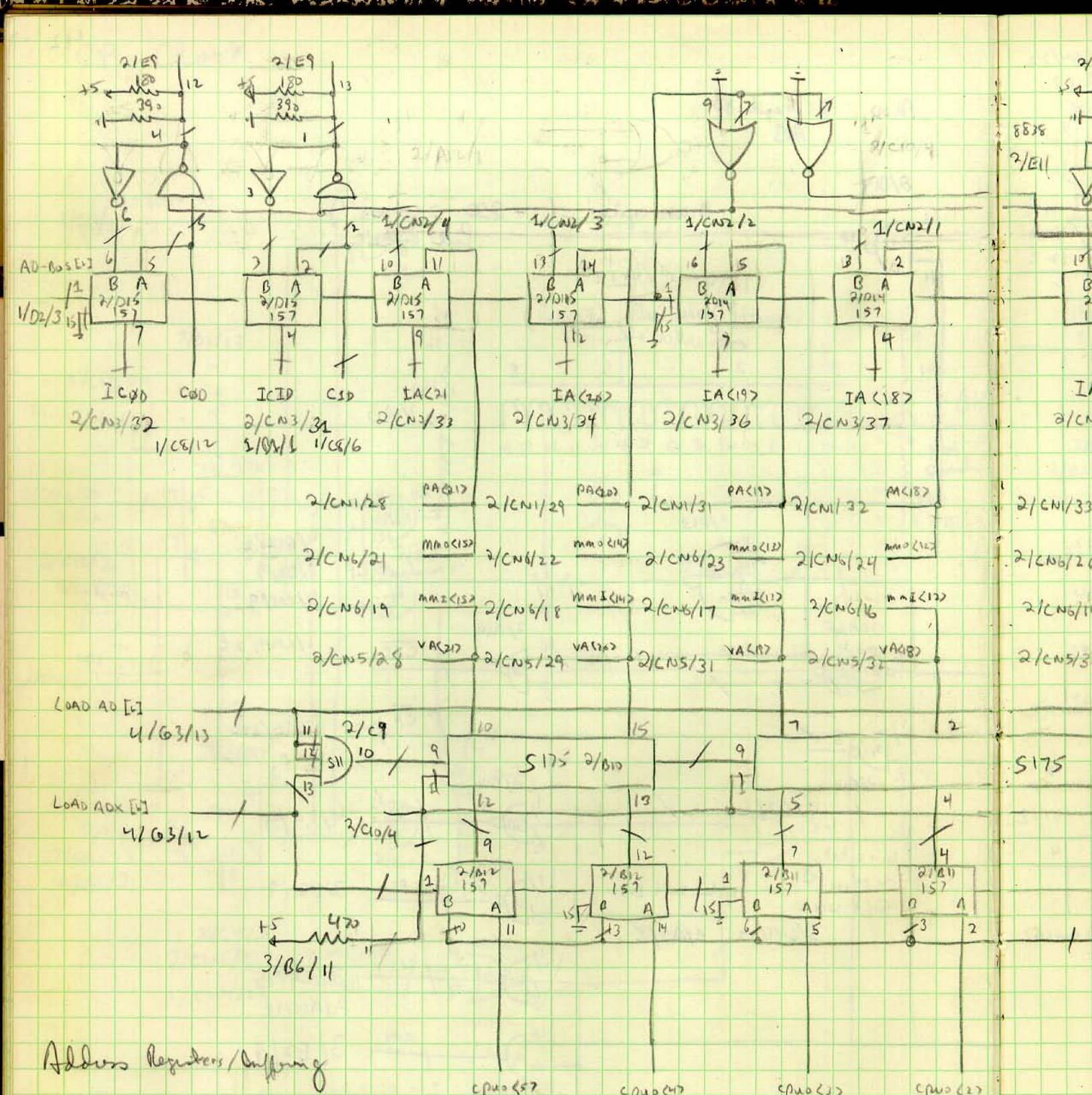
MOD 23 March 80
ARS



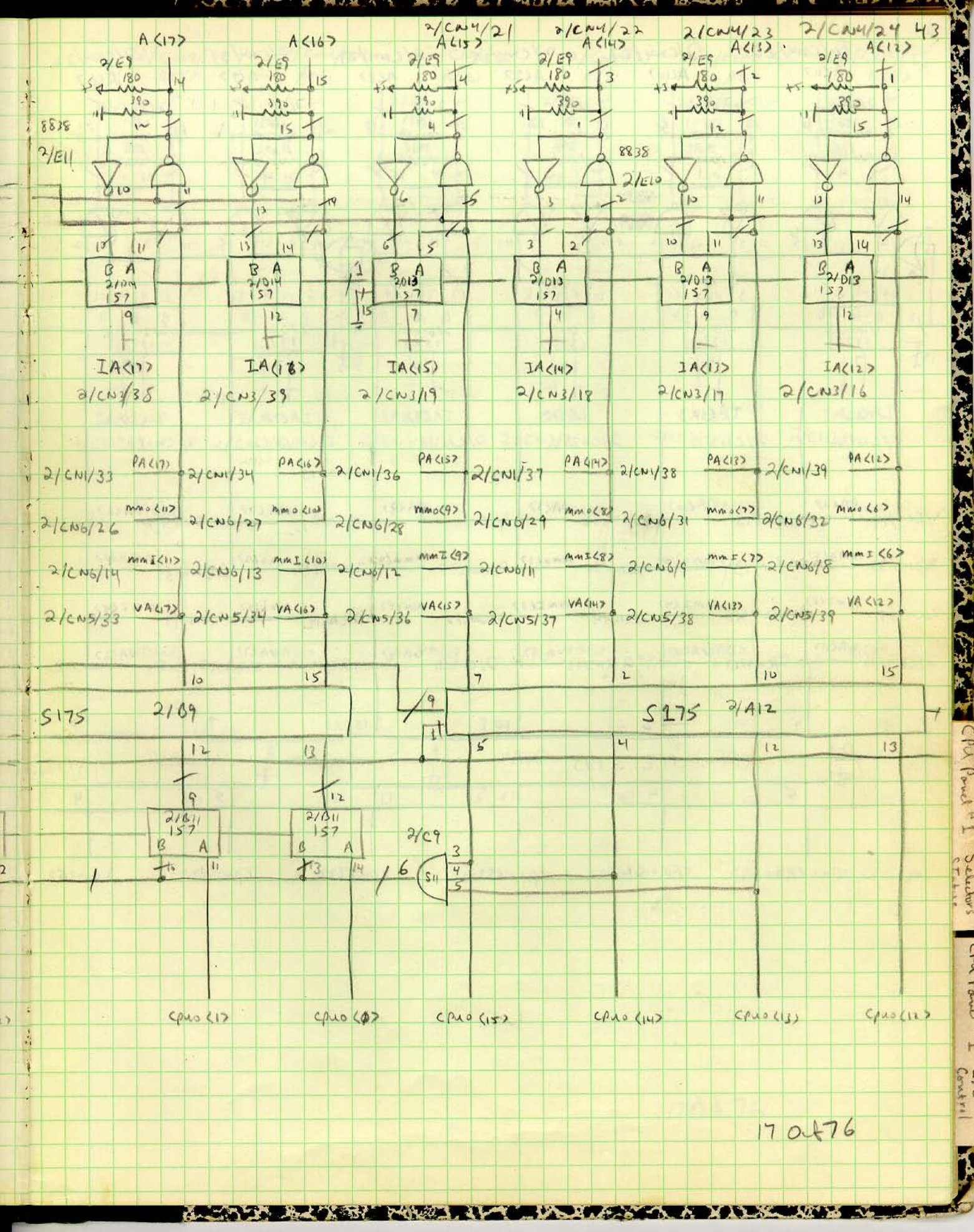
CPU Panel #1 Selectors Status

CPU Panel #1 I/O Control

16 Oct 76

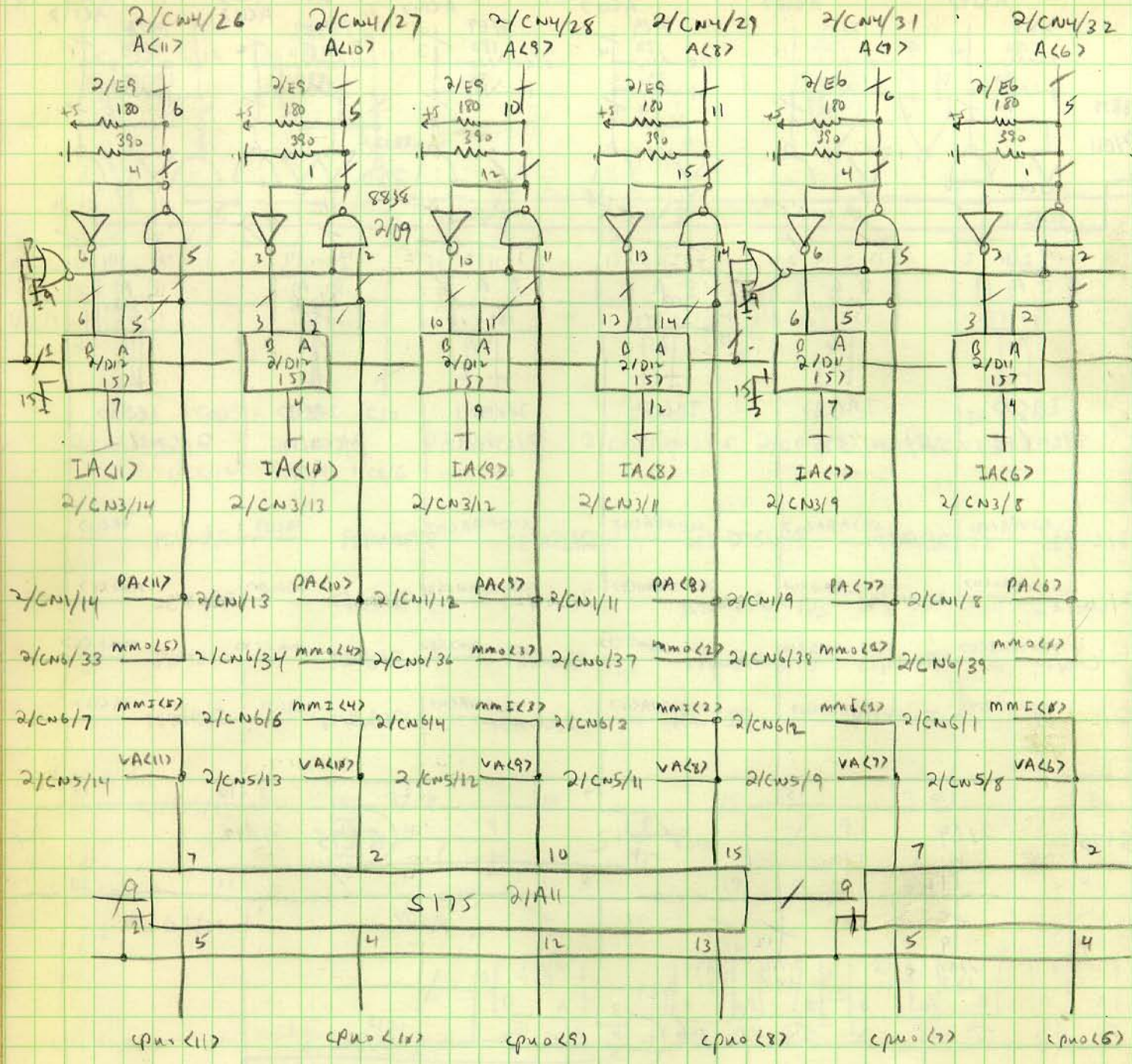


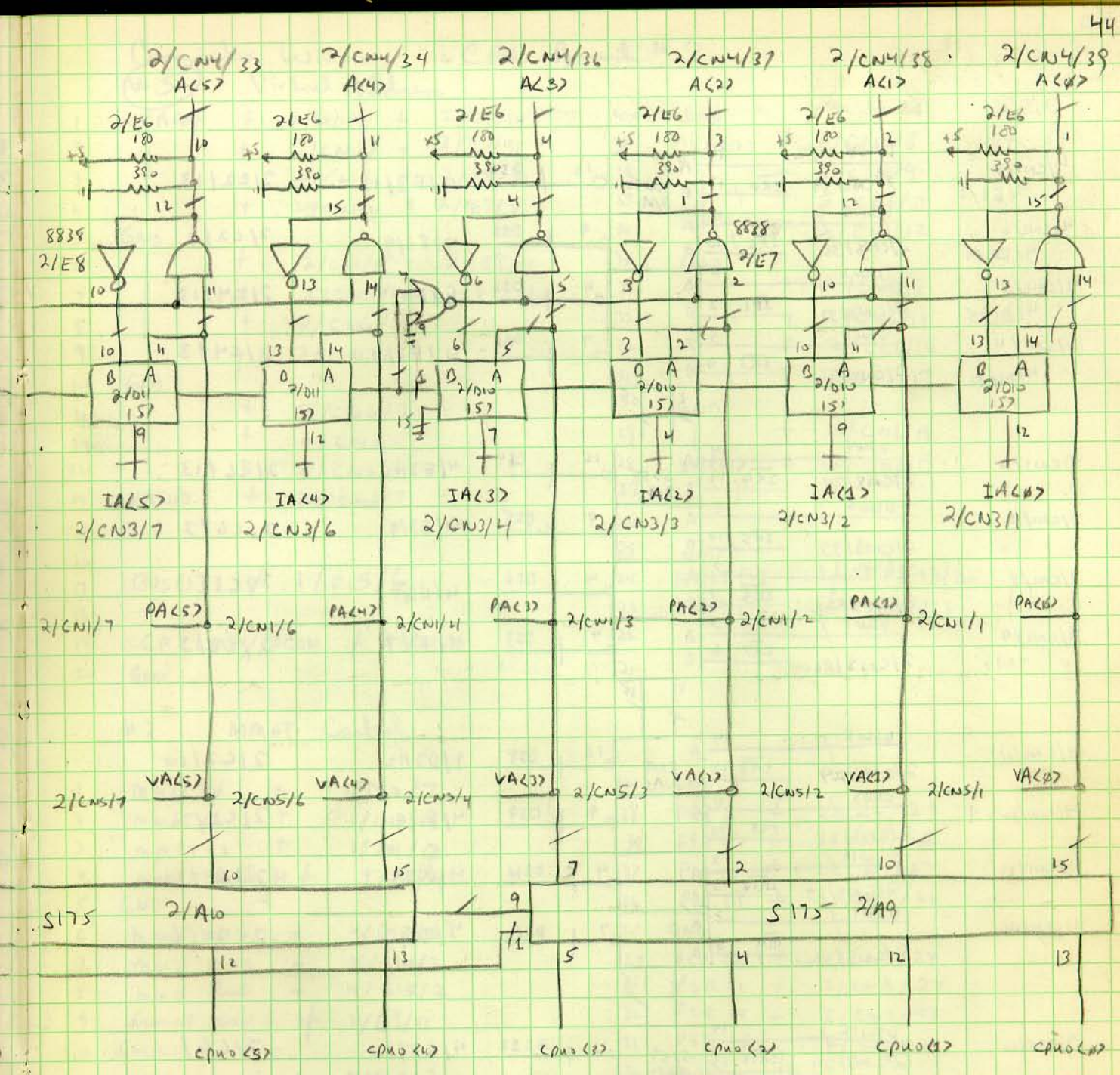
Address Registers / buffering



CPU Panel #1 Selectors

CPU Panel #1 I/O Control

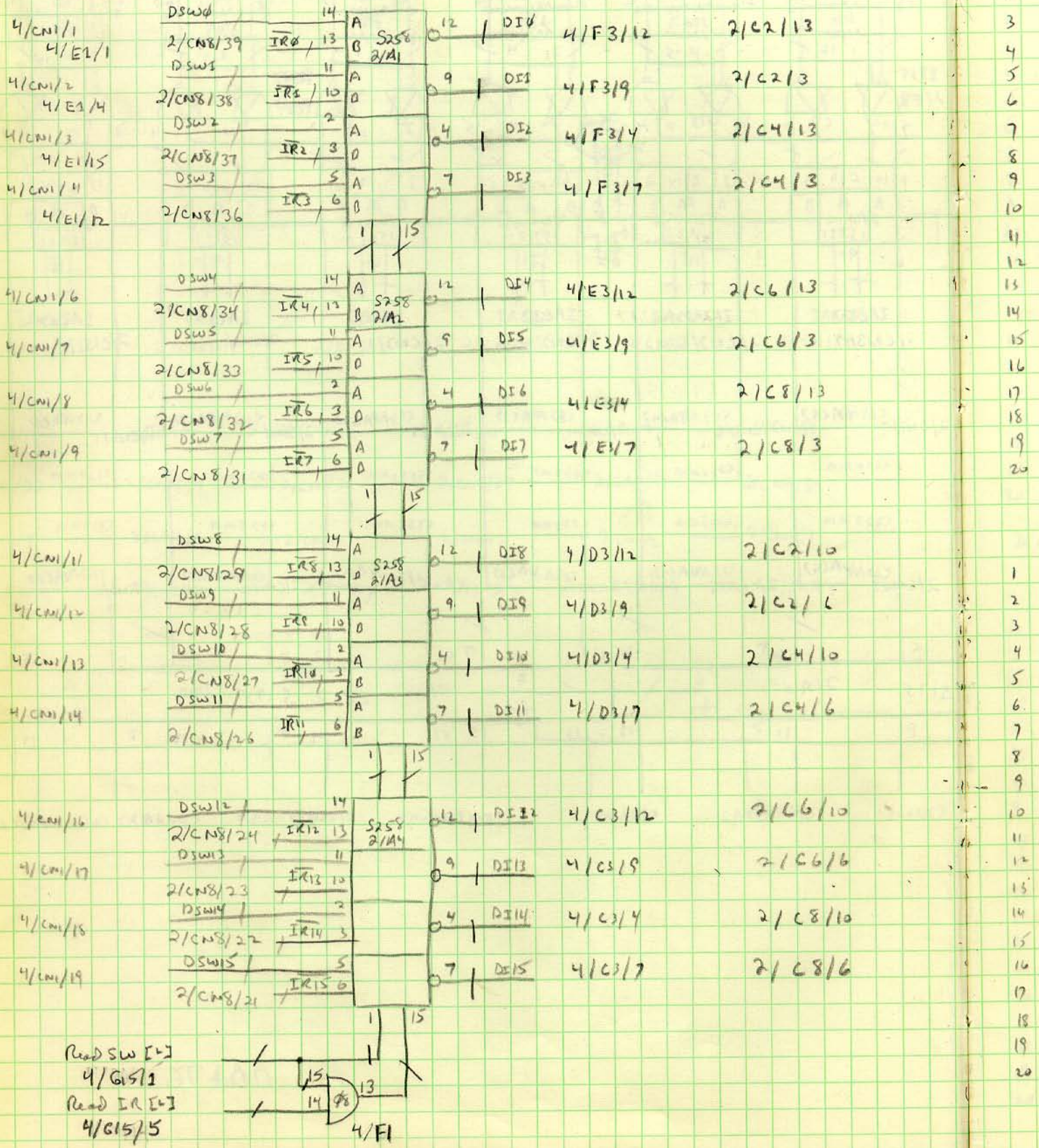

2/CN4/26
A<11>
2/CN4/27
A<10>
2/CN4/28
A<9>
2/CN4/29
A<8>
2/CN4/31
A<7>
2/CN4/32
A<6>
2/E9
2/E6
180
390
8838
2/D9
2/D12
2/D11
IA<11>
IA<10>
IA<9>
IA<8>
IA<7>
IA<6>
2/CN3/14
2/CN3/13
2/CN3/12
2/CN3/11
2/CN3/9
2/CN3/8
PA<11>
PA<10>
PA<9>
PA<8>
PA<7>
PA<6>
2/CN1/14
2/CN1/13
2/CN1/12
2/CN1/11
2/CN1/9
2/CN1/8
MM0<5>
MM0<4>
MM0<3>
MM0<2>
MM0<1>
MM0<0>
2/CN6/33
2/CN6/34
2/CN6/36
2/CN6/37
2/CN6/38
2/CN6/39
MMI<5>
MMI<4>
MMI<3>
MMI<2>
MMI<1>
MMI<0>
2/CN6/7
2/CN6/6
2/CN6/4
2/CN6/2
2/CN6/1
VA<11>
VA<10>
VA<9>
VA<8>
VA<7>
VA<6>
2/CN5/14
2/CN5/13
2/CN5/12
2/CN5/11
2/CN5/9
2/CN5/8
S175
2/A11
cpu<11>
cpu<10>
cpu<9>
cpu<8>
cpu<7>
cpu<6>
2/CN8
2/CN1/7
S175



17Oct76

CPU Panel #1 Selectors

CPU Panel #1 I/O Control


DSW0
DSW1
DSW2
DSW3
DSW4
DSW5
DSW6
DSW7
DSW8
DSW9
DSW10
DSW11
DSW12
DSW13
DSW14
DSW15
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
IR8
IR9
IR10
IR11
IR12
IR13
IR14
IR15
S258 2/A1
S258 2/A2
S258 2/A3
S258 2/A4
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
DI8
DI9
DI10
DI11
DI12
DI13
DI14
DI15
4/F3/12
4/F3/9
4/F3/4
4/F3/7
4/E3/12
4/E3/9
4/E3/4
4/E1/7
4/D3/12
4/D3/9
4/D3/4
4/D3/7
4/C3/12
4/C3/9
4/C3/4
4/C3/7
2/C2/13
2/C2/3
2/C4/13
2/C4/3
2/C6/13
2/C6/3
2/C8/13
2/C8/3
2/C2/10
2/C2/6
2/C4/10
2/C4/6
2/C6/10
2/C6/6
2/C8/10
2/C8/6
4/CN1/1
4/E2/1
4/CN1/2
4/E2/4
4/CN1/3
4/E1/15
4/CN1/4
4/E1/12
4/CN1/6
4/CN1/7
4/CN1/8
4/CN1/9
4/CN1/11
4/CN1/12
4/CN1/13
4/CN1/14
4/CN1/16
4/CN1/17
4/CN1/18
4/CN1/19
2/CN8/39
2/CN8/38
2/CN8/37
2/CN8/36
2/CN8/34
2/CN8/33
2/CN8/32
2/CN8/31
2/CN8/29
2/CN8/28
2/CN8/27
2/CN8/26
2/CN8/24
2/CN8/23
2/CN8/22
2/CN8/21
Read SW [L]
4/G15/1
Read IR [L]
4/G15/5
4/F1

Connector Wiring CPU Board # 2

#5 Virtual Address

1	VA<0>	+	2/CN1/1	+	2/E7/14		
2	|	+	2/CN1/2	+	2/E7/11		
3	|	+	2/CN1/3	+	2/E7/2		
4	|	+	2/CN1/4	+	2/E7/5		
5	GND						
6	|	+	2/CN1/6	+	2/E8/14		
7	|	+	2/CN1/7	+	2/E8/11		
8	|	+	2/CN6/1				
9	|	+	2/CN6/2				
10	GND						
11	|	+	2/CN6/3				
12	|	+	2/CN6/4				
13	|	+	2/CN6/6				
14	VA<11>	+	2/CN6/7				
15	GND						
16							
17	BUS [L]	+	1/F15/6				
18							
19	CP CLOCH/CPCON	+	2/C11/6				
20	GND						

40	GND						
39	VA<12>	+	2/CN6/8				
38	|	+	2/CN6/9				
37	|	+	2/CN6/11				
36	|	+	2/CN6/12				
35	GND						
34	|	+	2/CN6/13				
33	|	+	2/CN6/14				
32	|	+	2/CN6/16				
31	|	+	2/CN6/17				
30	GND						
29	|	+	2/CN6/18				
28	VA<21>	+	2/CN6/19				
27							
26							
25	GND						
24	HALT [L]	+	1/F13/2				
23	HALT [H]	+	1/A7/13				
22							
21							

#2 MM6T Control

1	mm6T C0	+	1/D10/7				
2	mm6T C1	+	1/D10/9				
3	mm6T C3	+	1/D11/2				
4	mm6T Ready H	+	1/06/4				
5	GND						
6	mm0 WLB	+	4/G13/2				
7	mm0 WHB	+	4/G14/2				
8	mm0 Read	+	4/G15/2				
9	MM6T GOH	+	1/D9/11				
10	GND						
11	mm1 WLB	+	4/G13/3				
12	mm1 WHB	+	4/G14/3				
13	mm1 Read	+	4/G15/3				
14	mm6T GRL	+	1/C1/6				
15	GND						
16	mm2 WLB	+	4/G13/4				
17	mm2 WHB	+	4/G14/4				
18	mm2 Read	+	4/G15/4				
19	GOL	+	2/C15/15				
20	GND						

40	GND						
39	PSR 8	+	2/CN9/29				
38	PSR 9	+	2/CN9/28				
37	PSR 10	+	2/CN9/27				
36	PSR 11	+	2/CN9/26				
35	GND						
34	PSR 12	+	2/CN9/24				
33	PSR 13	+	2/CN9/23				
32	PSR 14	+	2/CN9/22				
31	PSR 15	+	2/CN9/21				
30	GND						
29	INIT CLEAR	/	1/04/6	+	4/C2/1		
28	XL	+	3/CN4/11				
27	XH	+	3/CN4/12				
26	XA	+	3/CN4/13				
25	GND						
24	MM6T EN [H]	+	4/D1/11				
23							
22							
21	MM6T INIT						

17 Oct 76

CPU Panel #1 Selectors

CPU Panel #1 I/O Control

Connector Wiring — CPU Board #2

#3 INTERNAL Address Plus Control

1	IA0	+	2/D10/12		40	GND		
2	IA1	+	2/D10/9	- 4/G15/15	39	IA16	+	2/D14/12
3	IA2	+	2/D10/4	+ 4/G15/14	38	IA17	+	2/D14/9
4	IA3	+	2/D10/7		37	|	+	2/D14/4
5	GND				36	|	+	2/D14/7
6	|	+	2/D11/12		35	GND		
7	|	+	2/D11/9		34	IA20	+	2/D15/12
8	|	+	2/D11/4		33	IA21	+	2/D15/9
9	|	+	2/D11/7	+ 4/G15/13	32	IC0D	+	2/D15/7
10	GND				31	IC1D	+	2/D15/4
11	|	+	2/D12/12		30	GND		
12	|	+	2/D12/9		29	IXMSYNL	+	1/B4/6
13	|	+	2/D12/4		28			1/E2/6
14	|	+	2/D12/7		27	ISSYNL	+	1/E2/10
15	GND				26	UBSYNL	-	
16	|	+	2/D13/12		25	GND		
17	|	+	2/D13/9		24	IMSYNL	-	1/B4/16
18	|	+	2/D13/4		23			
19	IAIS	+	2/D13/7		22			
20	GND				21	INIT CLEAR H	+	1/E3/14

#4 UNIBUS Data Plus Address

1	BD0 [L]	+	2/E1/1		40	GND		
2	|	+	2/E1/3		39	BA0 [L]	+	2/E6/1
3	|	+	2/E1/15		38	|	+	2/E6/2
4	|	+	2/E1/13		37	|	+	2/E6/3
5	GND				36	|	+	2/E6/4
6	|	+	2/E1/5		35	GND		
7	|	+	2/E1/11		34	|	+	2/E6/14
8	|	+	2/E6/15		33	|	+	2/E6/10
9	|	+	2/E6/13		32	|	+	2/E6/5
10	GND				31	|	+	2/E6/6
11	|	+	2/E1/2		30	GND		
12	|	+	2/E1/4		29	|	+	2/E9/11
13	|	+	2/E1/14		28	|	+	2/E9/10
14	|	+	2/E1/12		27	|	+	2/E9/5
15	GND				26	|	+	2/E9/6
16	|	+	2/E1/6		25	GND		
17	|	+	2/E1/10		24	|	+	2/E9/1
18	|	+	2/E6/14		23	|	+	2/E9/2
19	BD1S [L]	+	2/E6/12		22	|	+	2/E9/3
20	GND				21	BA1S [L]	+	2/E9/4

Connector Wiring — CPU Board #2

#1 Physical Address + C' V' Z' N'

1	PAØ	+	2/CN5/1 – 1/108/15
2		+	2/CN5/2
3		+	2/CN5/3
4		+	2/CN5/4
5	GND		
6		+	2/CN5/6
7		+	2/CN5/7
8		+	2/CN6/39
9		+	2/CN6/38
10	GND		
11		+	2/CN6/37
12		+	2/CN6/36
13		+	2/CN6/34
14	PA11	+	2/CN6/33
15	GND		
16	C'	+	4/G6/23
17	V'	+	4/G6/22
18	Z'	+	4/G6/21
19	N'	+	4/G6/20
20	GND		
40	GND		
39	PA12	+	2/CN6/32
38		+	2/CN6/31
37		+	2/CN6/29
36		+	2/CN6/28
35	GND		
34		+	2/CN6/27
33		+	2/CN6/26
32		+	2/CN6/24
31		+	2/CN6/23
30	GND		
29	PA20	+	2/CN6/22
28	PA21	+	2/CN6/21
27			
26			
25	GND		
24	MHE[H]	+	2/B15/13
23			
22			
21	MHCL[H]	+	2/C15/1

#6 Memory Management Data

1	MMIØ	+	2/CN5/8
2		+	2/CN5/9
3		+	2/CN5/11
4		+	2/CN5/12
5	GND		
6		+	2/CN5/13
7		+	2/CN5/14
8		+	2/CN5/39
9		+	2/CN5/38
10	GND		
11		+	2/CN5/37
12		+	2/CN5/36
13		+	2/CN5/34
14		+	2/CN5/33
15	GND		
16		+	2/CN5/32
17		+	2/CN5/31
18		+	2/CN5/29
19	MMI15	+	2/CN5/28
20	GND		
40	GND		
39	MMOØ	+	2/CN1/8
38		+	2/CN1/9
37		+	2/CN1/11
36		+	2/CN1/12
35	GND		
34		+	2/CN1/13
33		+	2/CN1/14
32		+	2/CN1/39
31		+	2/CN1/38
30	GND		
29		+	2/CN1/37
28		+	2/CN1/36
27		+	2/CN1/34
26		+	2/CN1/33
25	GND		
24		+	2/CN1/32
23		+	2/CN1/31
22		+	2/CN1/29
21	MMO15	+	2/CN1/28

17 Oct 76

CPU Panel #1 Selectors

CPU Panel #1 I/O Control

Connector Wiring CPU Board #2

#7 INTERNAL DATA BUS

1	DI Ø	T	2/D1/13	40	GND		
2	|	+	2/D2/13	39	DO Ø	T	2/D1/9
3	|	+	2/D3/13	38	|	+	2/D2/9
4	|	T	2/D4/13	37	|	+	2/D3/9
5	GND			36	|	T	2/D4/9
6	|	T	2/D5/13	35	GND		
7	|	L	2/D6/13	34	|	+	2/D5/9
8	|	+	2/D7/13	33	|	T	2/D6/9
9	|	+	2/D8/13	32	|	+	2/D7/9
10	GND			31	|	+	2/D8/9
11	|	T	2/D1/3	30	GND		
12	|	+	2/D2/3	29	|	+	2/D1/7
13	|	T	2/D3/3	28	|	+	2/D2/7
14	|	L	2/D4/3	27	|	+	2/D3/7
15	GND			26	|	T	2/D4/7
16	|	T	2/D5/3	25	GND		
17	|	+	2/D6/3	24	|	+	2/D5/7
18	|	+	2/D7/3	23	|	+	2/D6/7
19	DI15	+	2/D8/3	22	|	T	2/D7/7
20	GND			21	DO15	+	2/D8/7

#8 INSTRUCTION Register Data

1	IR Ø	+	2/B1/12	40	GND		
2	|	+	2/B1/9	39	$\overline{\text{DIR Ø}}$	+	2/A1/13
3	|	+	2/B1/4	38	|	+	2/A1/10
4	|	+	2/B1/7	37	|	+	2/A1/3
5	GND			36	|	+	2/A1/6
6	|	+	2/B5/12	35	GND		
7	|	+	2/B5/9	34	|	+	2/A2/13
8	|	+	2/B5/4	33	|	+	2/A2/10
9	|	+	2/B5/7	32	|	+	2/A2/3
10	GND			31	|	+	2/A2/6
11	|	+	2/B3/12	30	GND		
12	|	+	2/B3/9	29	|	+	2/A3/13
13	|	+	2/B3/4	28	|	+	2/A3/10
14	|	+	2/B3/7	27	|	+	2/A3/3
15	GND			26	|	+	2/A3/6
16	|	+	2/B7/12	25	GND		
17	|	+	2/B7/9	24	|	+	2/A4/13
18	|	+	2/B7/4	23	|	+	2/A4/10
19	IR15	+	2/B7/7	22	|	+	2/A4/3
20	GND			21	$\overline{\text{DIR15}}$	+	2/A4/6

Connector Wiring CPU Board # 2

#9 Data Register & PSR

1	DØ	+	2/D1/14	40	GND			
2	|	+	2/D2/14	39	PSRØ	+		4/E1/2
3	|	+	2/D3/14	38	|	+		4/E1/5
4	|	+	2/D4/14	37	|	+		4/E1/14
5	GND			36	|	+		4/E1/11
6	|	+	2/D5/14	35	GND			
7	|	+	2/D6/14	34	|	+		4/E3/13
8	|	+	2/D7/14	33	|	+		4/E3/10
9	|	+	2/D8/14	32	|	+		4/E3/3
10	GND			31	|	+		4/E3/6
11	|	+	2/D1/2	30	GND			
12	|	+	2/D2/2	29	|	+	2/CN2/39	4/D3/13
13	|	+	2/D3/2	28	|	+	2/CN2/38	4/D3/10
14	|	+	2/D4/2	27	|	+	2/CN2/37	4/D3/7
15	GND			26	|	+	2/CN2/36	4/D3/6
16	|	+	2/D5/2	25	GND			
17	|	+	2/D6/2	24	|	+	2/CN2/34	4/D1/4
18	|	+	2/D7/2	23	|	+	2/CN2/33	4/D1/5
19	D15	+	2/D8/2	22	|	+	2/CN2/32	4/D1/15
20	GND			21	PSR15	+	2/CN2/31	4/D1/14

17 Oct 76

CPU Panel #1 Selectors Status

CPU Panel #1 I/O Control

Connector Wiring CPU Board #4

H1 Switch Data

1	DSW0	+	2/A1/14	4/F11/17	40	GND		
2	|	-	2/A1/11	4/F10/17	39	DSW16	+	4/F11/16
3	|	+	2/A1/2	4/F9/17	38	|	+	4/F10/16
4	|	-	2/A1/5	4/F8/17	37	|	-	4/F9/16
5	GND				36	|	+	4/F8/16
6	|	+	2/A2/14	4/E11/17	35	GND		
7	|	+	2/A2/11	4/E10/17	34	|	+	4/E11/16
8	|	+	2/A2/2	4/E9/17	33	DSW21	+	4/E10/16
9	|	+	2/A2/5	4/E8/17	32		+	4/E9/16
10	GND				31		+	4/E8/16
11	|	+	2/A3/14	4/B11/17	30	GND		
12	|	+	2/A3/11	4/B10/17	29		+	4/B11/16
13	|	+	2/A3/2	4/B9/17	28		+	4/B10/16
14	|	-	2/A3/5	4/B8/17	27	H	+	4/B9/16
15	GND				26	D	+	4/B8/16
16	|	+	2/A4/14	4/A11/17	25	GND		
17	|	-	2/A4/11	4/A10/17	24	S	+	4/A11/16
18		+	2/A4/2	4/A9/17	23	C	+	4/A10/16
19	DSW15	+	2/A4/5	4/A8/17	22	Ex	+	4/A9/16
20	GND				21	LA	+	4/A8/16

MM6T Connector Jumpers for MM6T Not installed

CN2

CN2/4 – CN2/9

CN2/21 – CN2/29

CN6

CN6/1 – CN6/39
CN6/2 – CN6/38
CN6/3 – CN6/37
CN6/4 – CN6/36

CN6/6 – CN6/34
CN6/7 – CN6/33
CN6/8 – CN6/32
CN6/9 – CN6/31

CN6/11 – CN6/29
CN6/12 – CN6/28
CN6/13 – CN6/27
CN6/14 – CN6/26

CN6/16 – CN6/24
CN6/17 – CN6/23
CN6/18 – CN6/22
CN6/19 – CN6/21

CPU Board #4 Select / PSR / CNTR / SLR / SCR

	G15	G14	G13	G12	G11	G10	G9	G8	G7
	ADD 42	ADD 42	ADD 42	PSR/SCR S32	SCR INV SØ4	SCR INV SØ4	CNTR S133	CNTR S133	CNTR S133

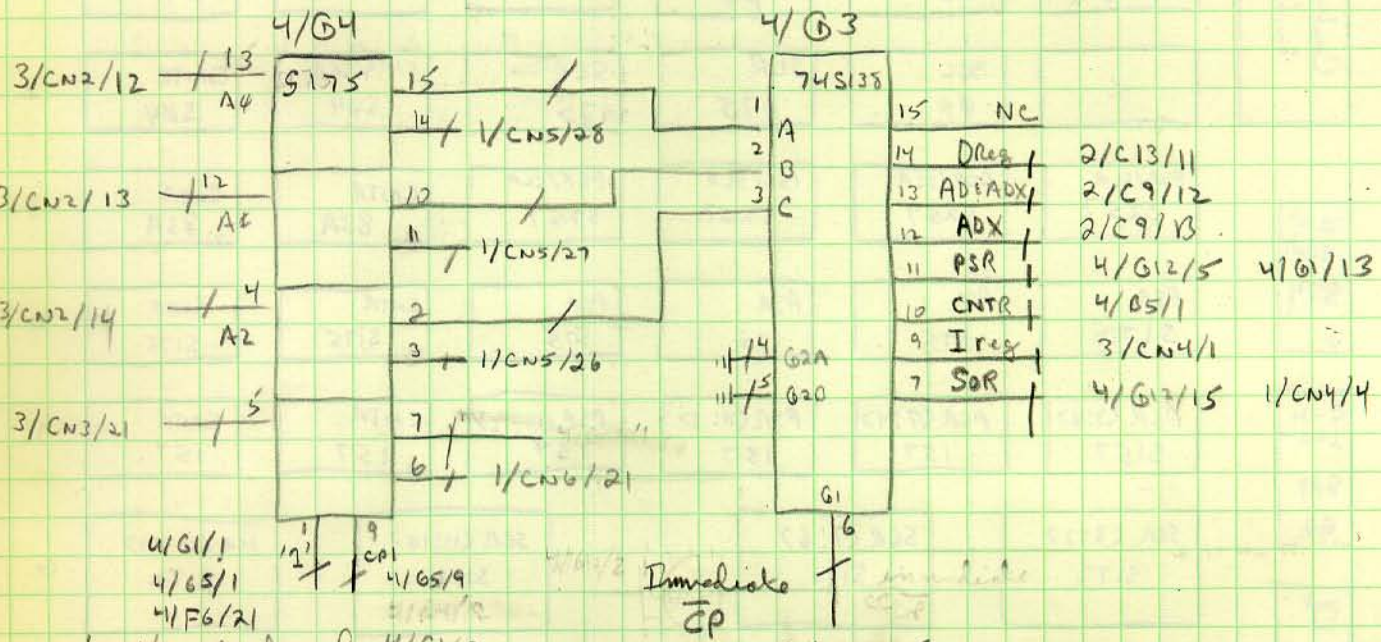
H — Control Panel Switch & Lines

	F	E	D	C	B	A	
	IR/SW ØB	CLC ØB	PSR ØB	PSR SØB	CNTR S11	CNTR S74	1
	X	SEC ØØ	SLR 175	SLR 175	CNTR/SCR SØ4	CNTR SØ4	2
	PSR/SLR S257	PSR/SLR S257	PSR/SLR S257	PSR/SLR S257	CNTR 83A	CNTR 83A	3
CLOCK TEST S74 G1	PSR S175	PSR 175	PSR 175	PSR 175	CNTR S175	CNTR S175	4
C-N INV SØ4 G2	PSR ⟨3:0⟩ S157	PSR ⟨7:4⟩ 157	PSR ⟨11:8⟩ 157	PSR ⟨15:12⟩ 157	CNTR 157	CNTR 157	5
	SCR ⟨3:2⟩ S172	SCR ⟨7:6⟩ S172		SCR ⟨11:10⟩ S172		SCR ⟨15:14⟩ S172	6
DEST SEL S138 G3	SCR ⟨1:0⟩ S172	SCR ⟨5:4⟩ S172		SCR ⟨9:8⟩ S172		SCR ⟨13:12⟩ S172	7
DEST MICRO S175 G4	CPUIS ⟨3⟩ 150	CPUIS ⟨7⟩ 150		CPUIS ⟨11⟩ 150		CPUIS ⟨15⟩ 150	8
CPUIS CODE S175 G5	CPUIS ⟨2⟩ 150	CPUIS ⟨6⟩ 150		CPUIS ⟨10⟩ 150		CPUIS ⟨14⟩ 150	9
	CPUIS ⟨1⟩ 150	CPUIS ⟨5⟩ 150		CPUIS ⟨9⟩ 150		CPUIS ⟨13⟩ 150	10
COND GROUND 150 G6	CPUIS ⟨Ø⟩ 150	CPUIS ⟨4⟩ 150		CPUIS ⟨8⟩ 150		CPUIS ⟨12⟩ 150	11

220476

CPU Board #1 I/O Control

CPU output Destination Select

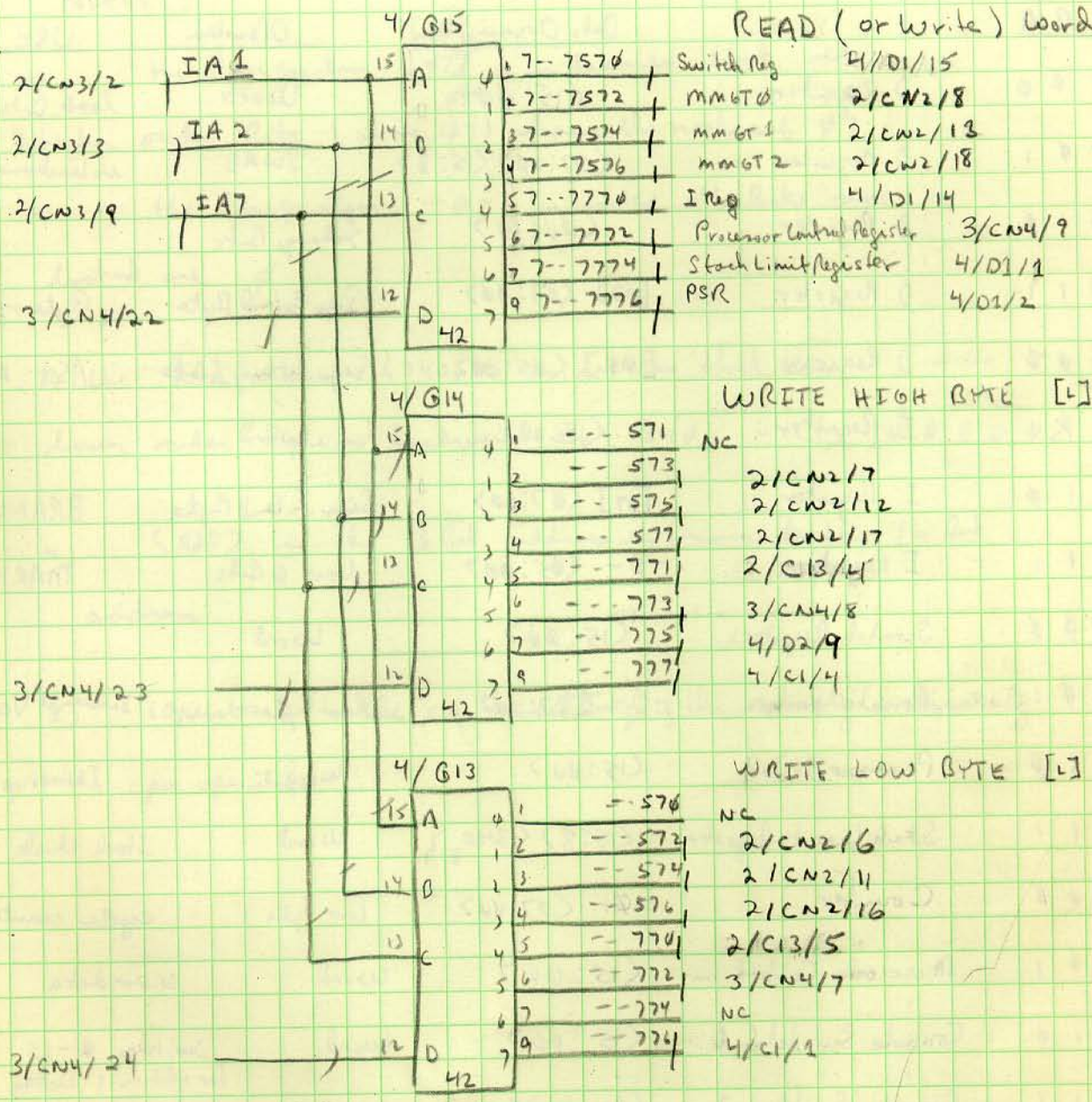


Write clocks for 4/G1/3

- 0 – NONE
- 1 – D Register
- 2 – Address Register + Address Extension
- 3 – Address Extension
- 4 – Processor Status Register
- 5 – Cycle Counter
- 6 – instruction Register
- 7 – Stack overflow Register

clocks go high at approximately the same time as the CP clock

Address Decoders for internal Registers



220476

CPU Panel #1 I/O Control

CPU INPUT Selector Listing (Sixteen inputs selectable)

Selector D C B A		Data Organization	Operation	USE
0 0 0 0	D Register	<15:00>	Word	load Data
0 0 0 1	D Register	<07:00> <15:8>	SWAB	interchange Bytes
0 0 1 0	D Register	<00:15>	Exchange Bits	
0 0 1 1	D Register	[07] <07:00>	Sign Exland Byte	Byte ops
0 1 0 0	D Register	[05] <05:00>	Sign Exland 6 Bits	ASH, ASHC
0 1 0 1	I Register	<15:00>	Word	
0 1 1 0	I Register	[07] <07:00>	Sign Exland Byte	BRANCHES
0 1 1 1	I Register	-0- <05:00>	low 6 Bits	MARK
1 0 0 0	Scratch Registers	<15:00>	Word	
1 0 0 1	Priority Vectors	-0- <07:00>	low Byte	Interrupt Vectors
1 0 1 0	Processor Status	<15:00>	Word	Interrupts
1 0 1 1	Stack Limit Register	<15:8> <340_8>	Word	Stack check
1 1 0 0	Counter	-0- <07:00>	Low Byte	cycle counting
1 1 0 1	Microcode Constant	<15:00>	Word	Micro data
1 1 1 0	Console Switches 1	<15:00>	Word	Switches 0-15 for address & Data
1 1 1 1	Console Switches 2	(operation) (ADD)	Word	contain high order address plus console operation

Notes :

1) the designation [Ø5 / Ø7] indicates that all higher order Bits (above Ø5 / Ø7) have the value Ø

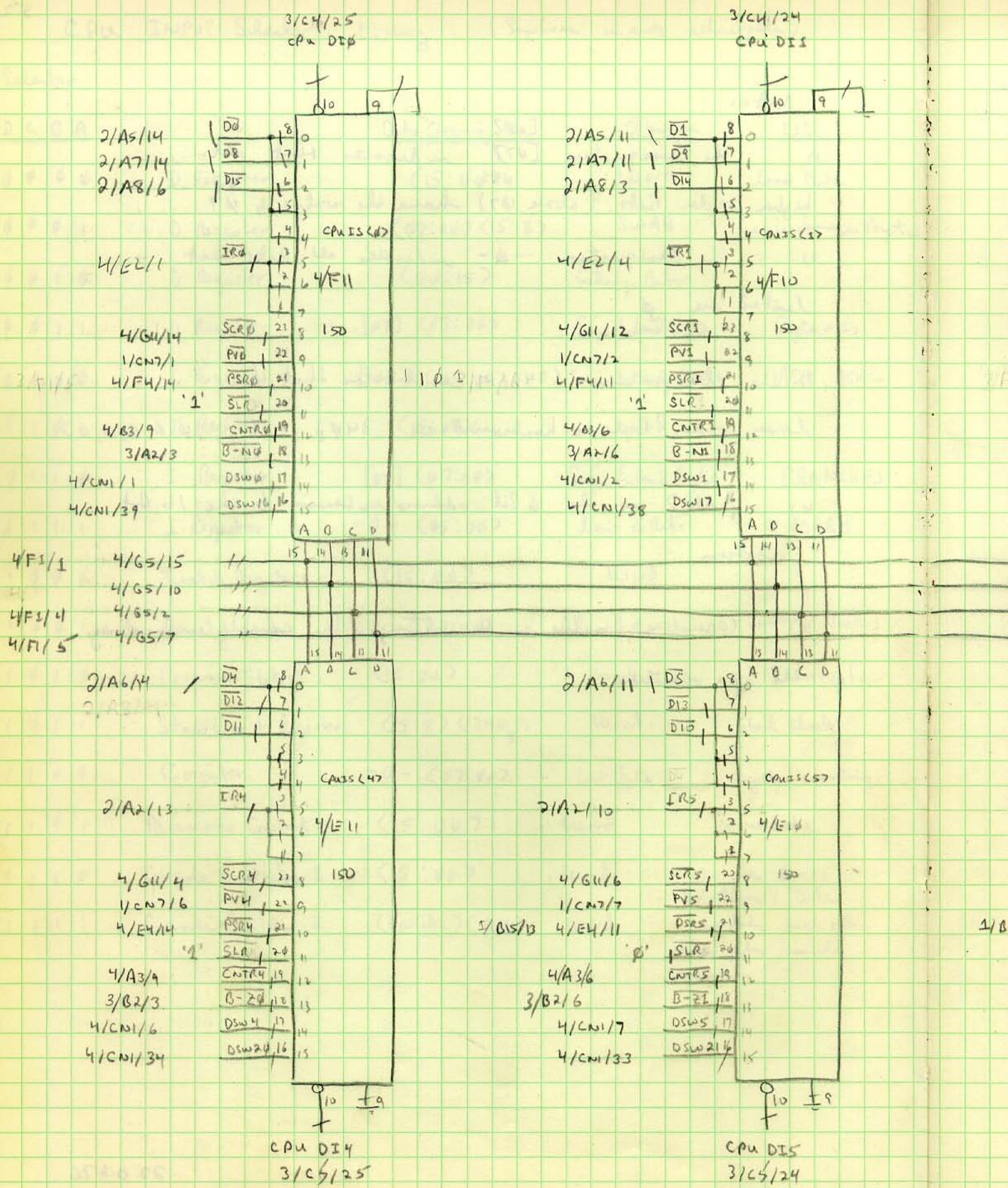
2) the designation —Ø— indicates all Bits not listed are Ø

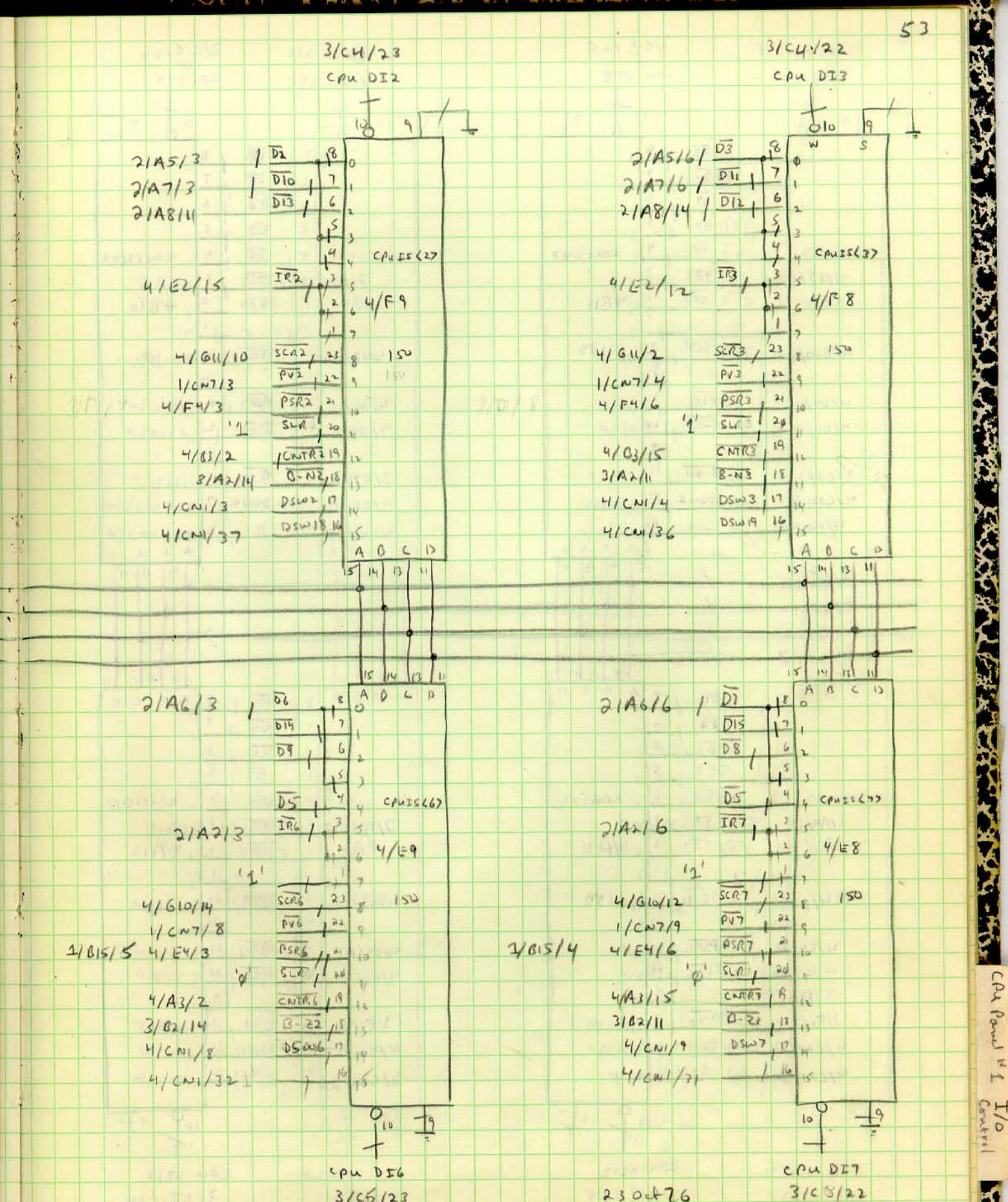
3) the designation $\langle 340_8 \rangle$ indicates that the lower order Byte is hardwired as $340_8 = \langle 1,1,1,0,0,0,0,0 \rangle$

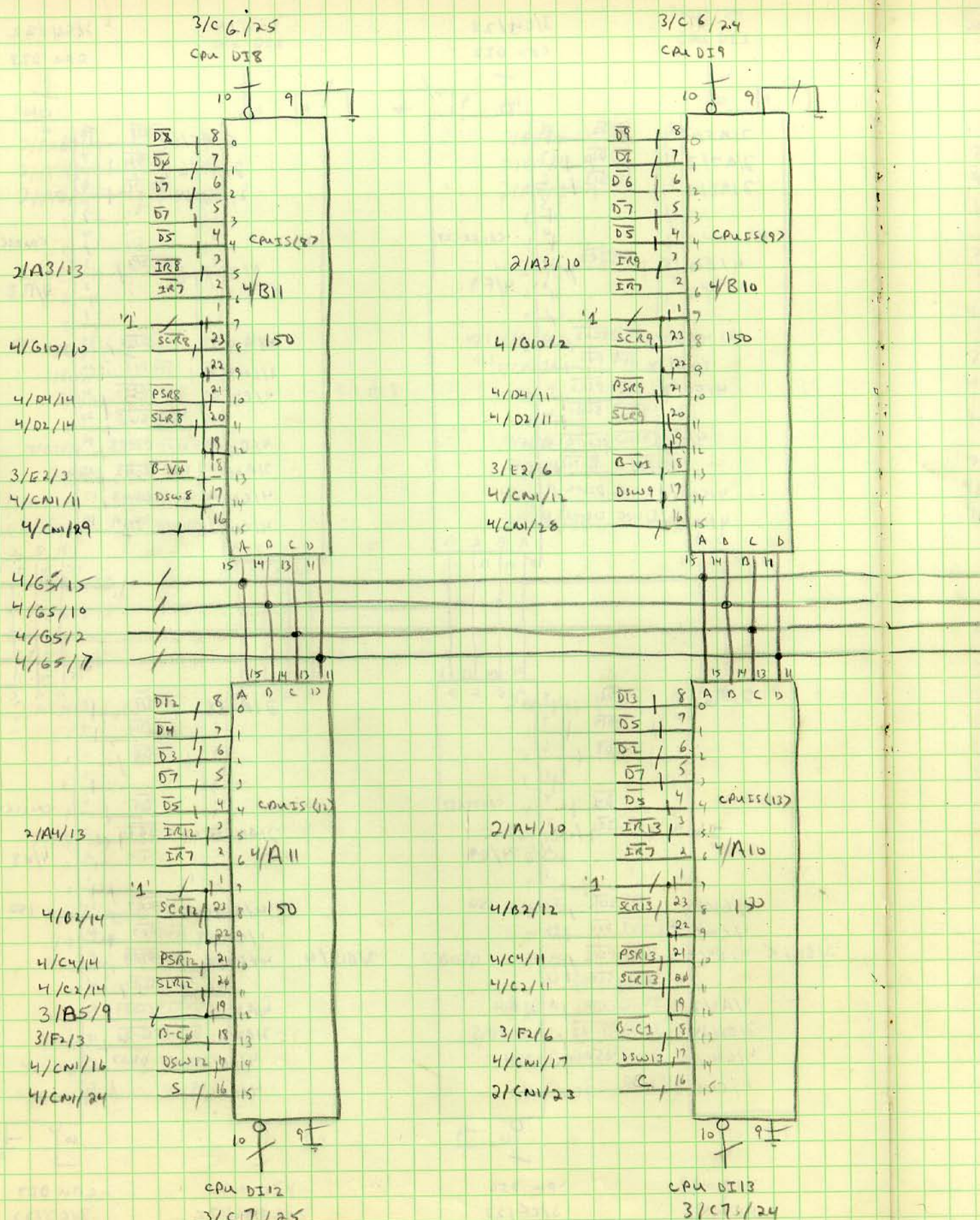
4) $\langle$Add$\rangle$ is the 6 Bit address extension to the 16 Bit address

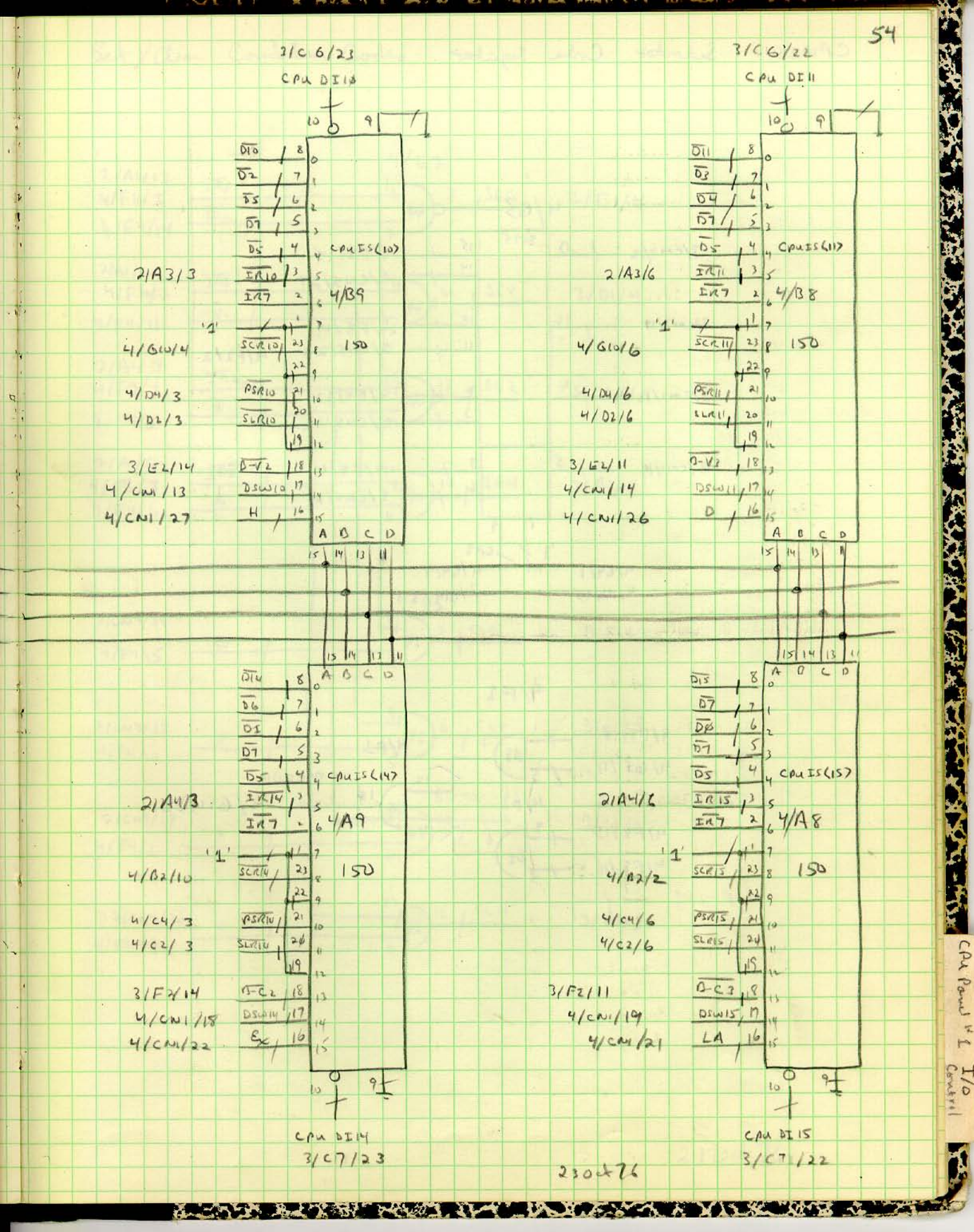
5) $\langle$Operation$\rangle$ is the switch settings of the console indicating the cpu operation

22 Oct 76

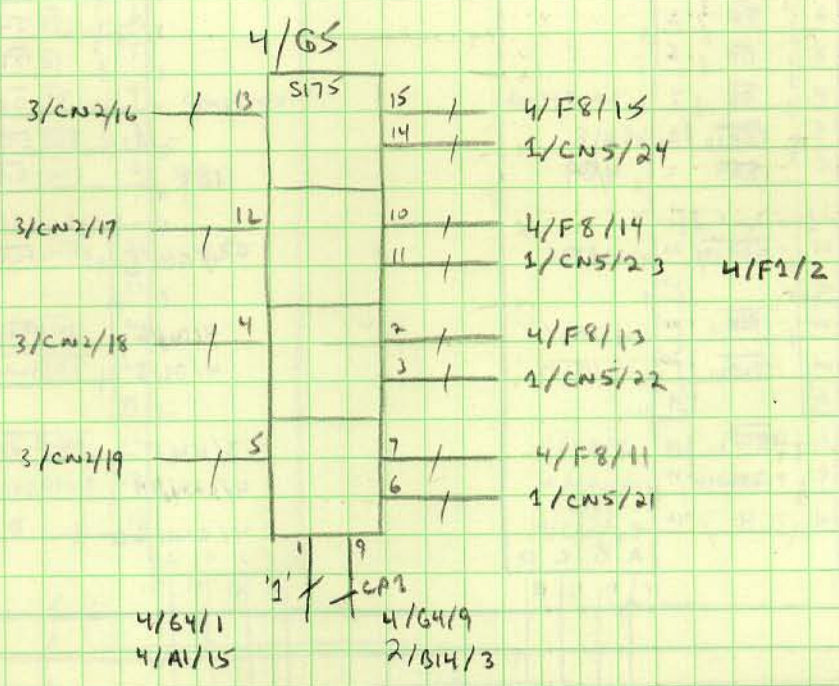

3/C4/25
CPU DI0
3/C4/24
CPU DI1
2/A5/14
2/A7/14
2/A8/6
2/A5/11
2/A7/11
2/A8/3
4/E2/1
4/E2/4
4/F11
4/F10
4/G11/14
1/CN7/1
4/F4/14
4/G11/12
1/CN7/2
4/F4/11
4/B3/9
3/A2/3
4/CN1/1
4/CN1/39
4/B3/6
3/A2/6
4/CN1/2
4/CN1/38
4/F1/1
4/F1/4
4/F1/5
4/G5/15
4/G5/10
4/G5/2
4/G5/7
2/A6/4
2/A6/11
2/A2/13
2/A2/10
4/G11/4
1/CN7/6
4/E4/14
4/G11/6
1/CN7/7
4/E4/11
4/A3/9
3/B2/3
4/CN1/6
4/CN1/34
4/A3/6
3/B2/6
4/CN1/7
4/CN1/33
CPU DI4
3/C5/25
CPU DI5
3/C5/24

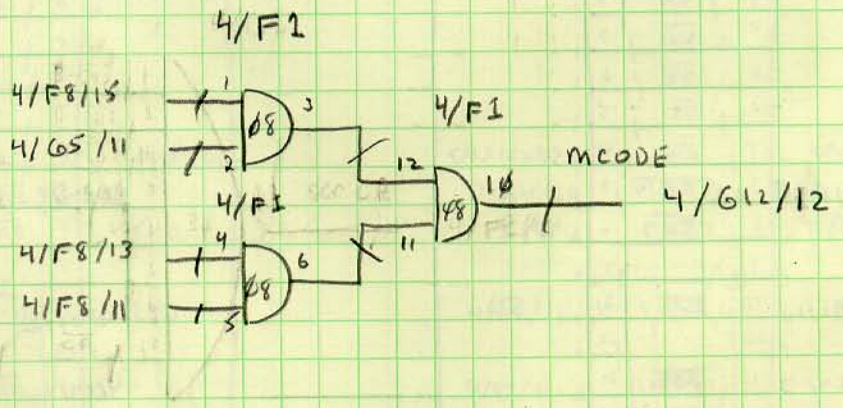

3/C4/23
CPU DI2
2/A5/3
2/A7/3
2/A8/11
4/E2/15
4/G11/10
1/CN7/3
4/F4/3
'1'
4/B3/2
3/A2/14
4/CN1/3
4/CN1/37
4/F9
3/C4/22
CPU DI3
2/A5/6
2/A7/6
2/A8/14
4/E2/12
4/G11/2
1/CN7/4
4/F4/6
'1'
4/B3/15
3/A2/11
4/CN1/4
4/CN1/36
4/F8
2/A6/3
2/A7/3
1/B15/5
4/E4/3
'0'
4/A3/2
3/B2/14
4/CN1/8
4/CN1/32
4/E9
4/G10/14
1/CN7/8
CPU DI6
3/C5/23
2/A6/6
2/A2/6
1/B15/4
4/E4/6
'0'
4/A3/15
3/B2/11
4/CN1/9
4/CN1/71
4/E8
4/G10/12
1/CN7/9
CPU DI7
3/C5/22
23 Oct 76
CPU Panel #1 I/O Control


3/C 6/25
CPU DI8
CPU IS(8)
4/B11
150
2/A3/13
4/G10/10
4/D4/14
4/D2/14
3/E2/3
4/CN1/11
4/CN1/29
3/C 6/24
CPU DI9
CPU IS(9)
4/B10
150
2/A3/10
4/G10/2
4/D4/11
4/D2/11
3/E2/6
4/CN1/12
4/CN1/28
4/G5/15
4/G5/10
4/G5/2
4/G5/7
CPU IS(12)
4/A11
150
2/A4/13
4/B2/14
4/C4/14
4/C2/14
3/B5/9
3/F2/3
4/CN1/16
4/CN1/24
CPU DI12
3/C7/25
CPU IS(13)
4/A10
150
2/A4/10
4/B2/12
4/C4/11
4/C2/11
3/F2/6
4/CN1/17
2/CN1/23
CPU DI13
3/C7/24

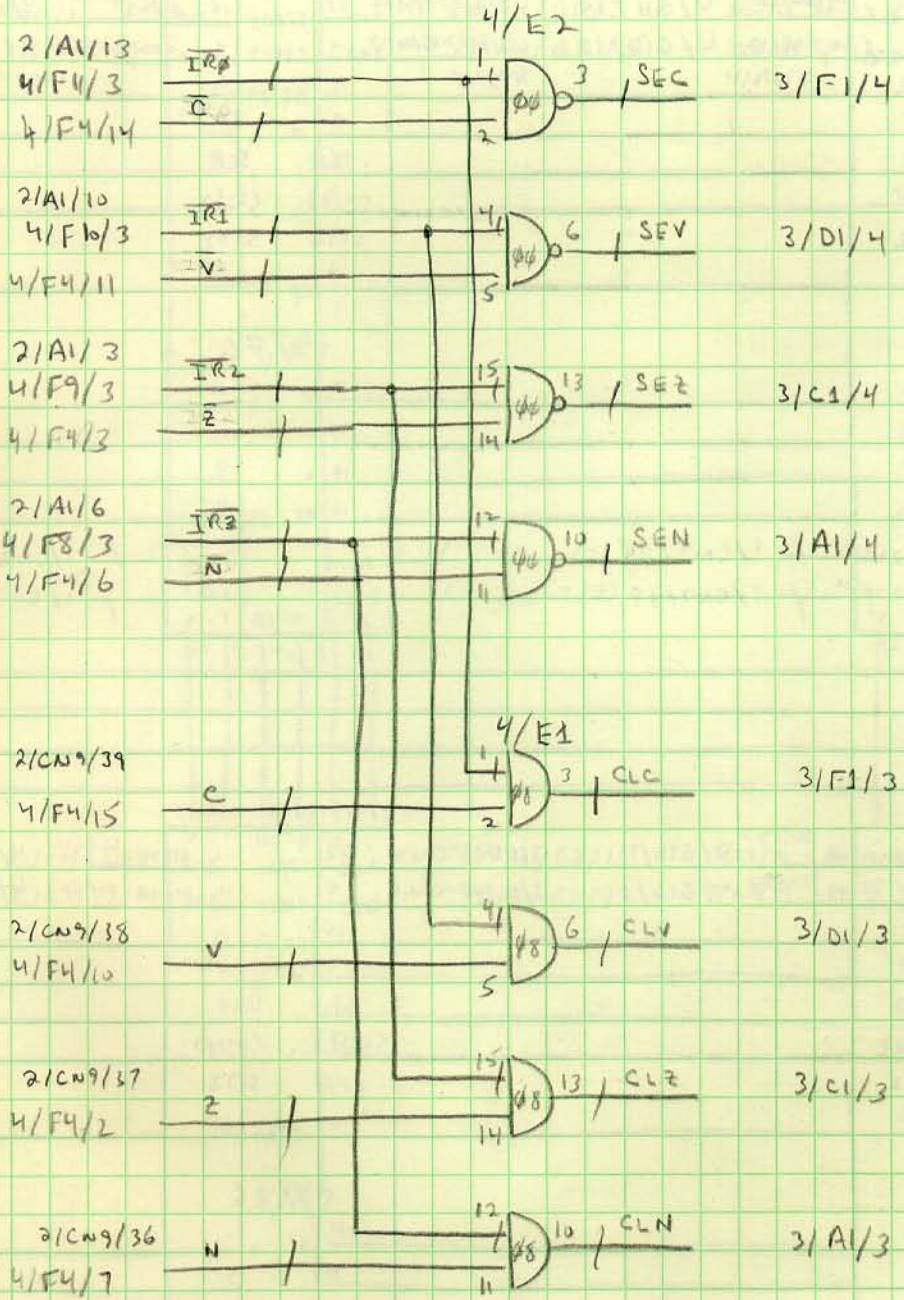

3/C 6/23
CPU DI10
2/A3/3
4/G10/4
4/D4/3
4/D2/3
3/E2/14
4/CN1/13
4/CN1/27
4/B9
150
CPUIS(10)
3/C 6/22
CPU DI11
2/A3/6
4/G10/6
4/D4/6
4/D2/6
3/E2/11
4/CN1/14
4/CN1/26
4/B8
150
CPUIS(11)
2/A4/3
4/B2/10
4/C4/3
4/C2/3
3/F2/14
4/CN1/18
4/CN1/22
4/A9
150
CPUIS(14)
CPU DI14
3/C7/23
2/A4/6
4/B2/2
4/C4/6
4/C2/6
3/F2/11
4/CN1/19
4/CN1/21
4/A8
150
CPUIS(15)
CPU DI15
3/C7/22
230ct76
CPU Panel #1 I/O Control

CPU IS Selector Code Register





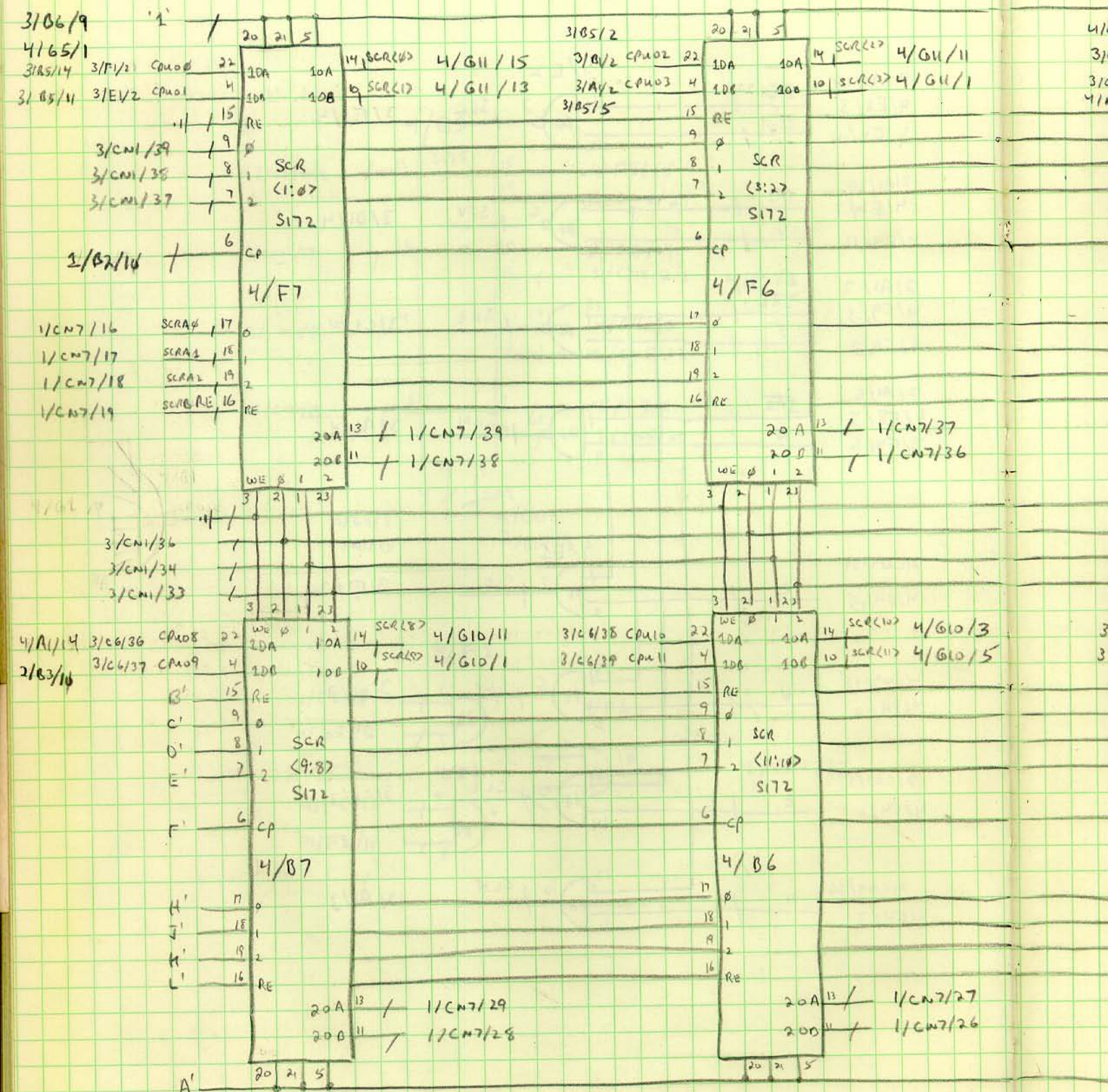
Set/Clear Condition Codes

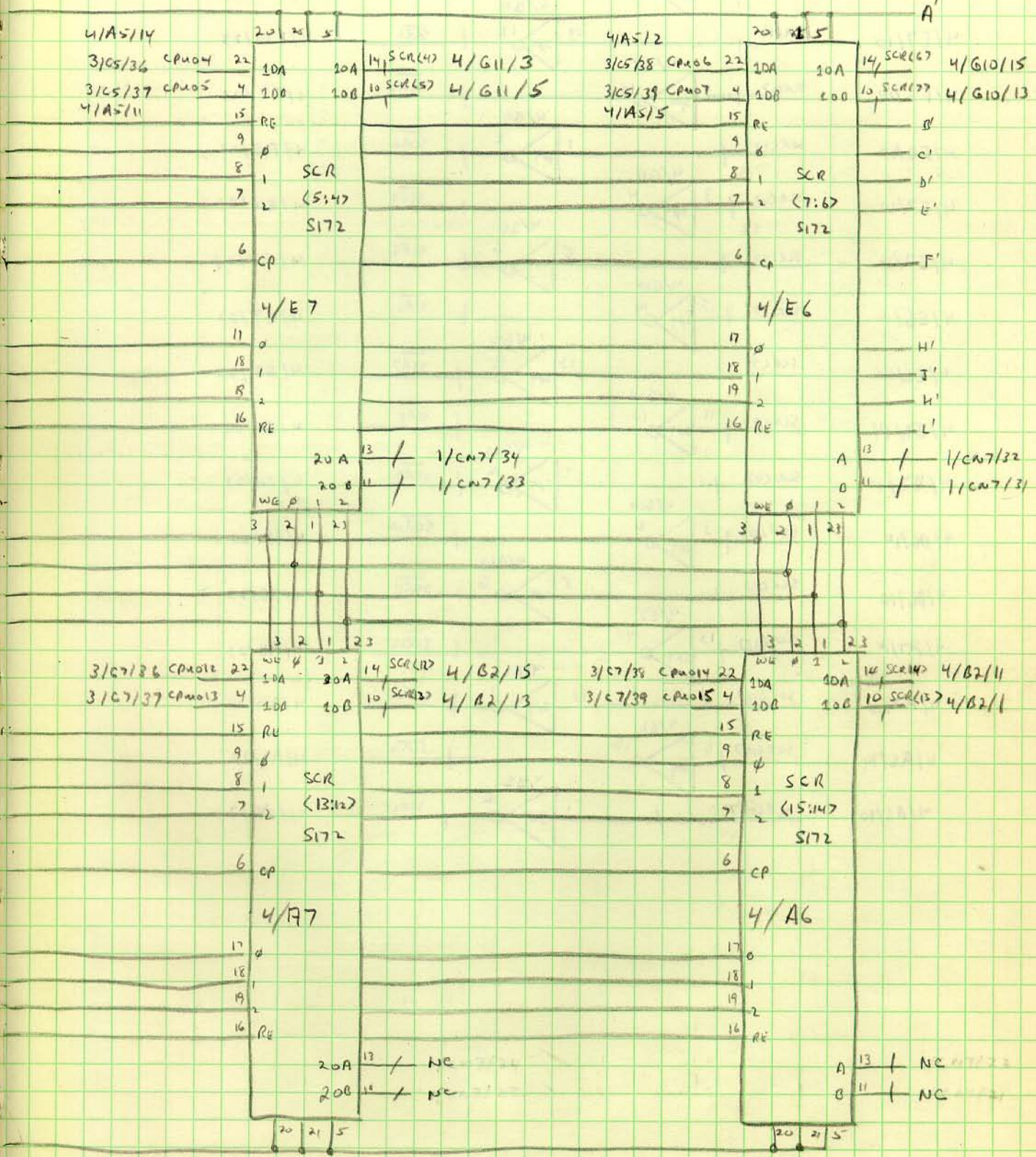


23 Oct 76

CAR Panel #1 I/O Control

Scratch Register logic

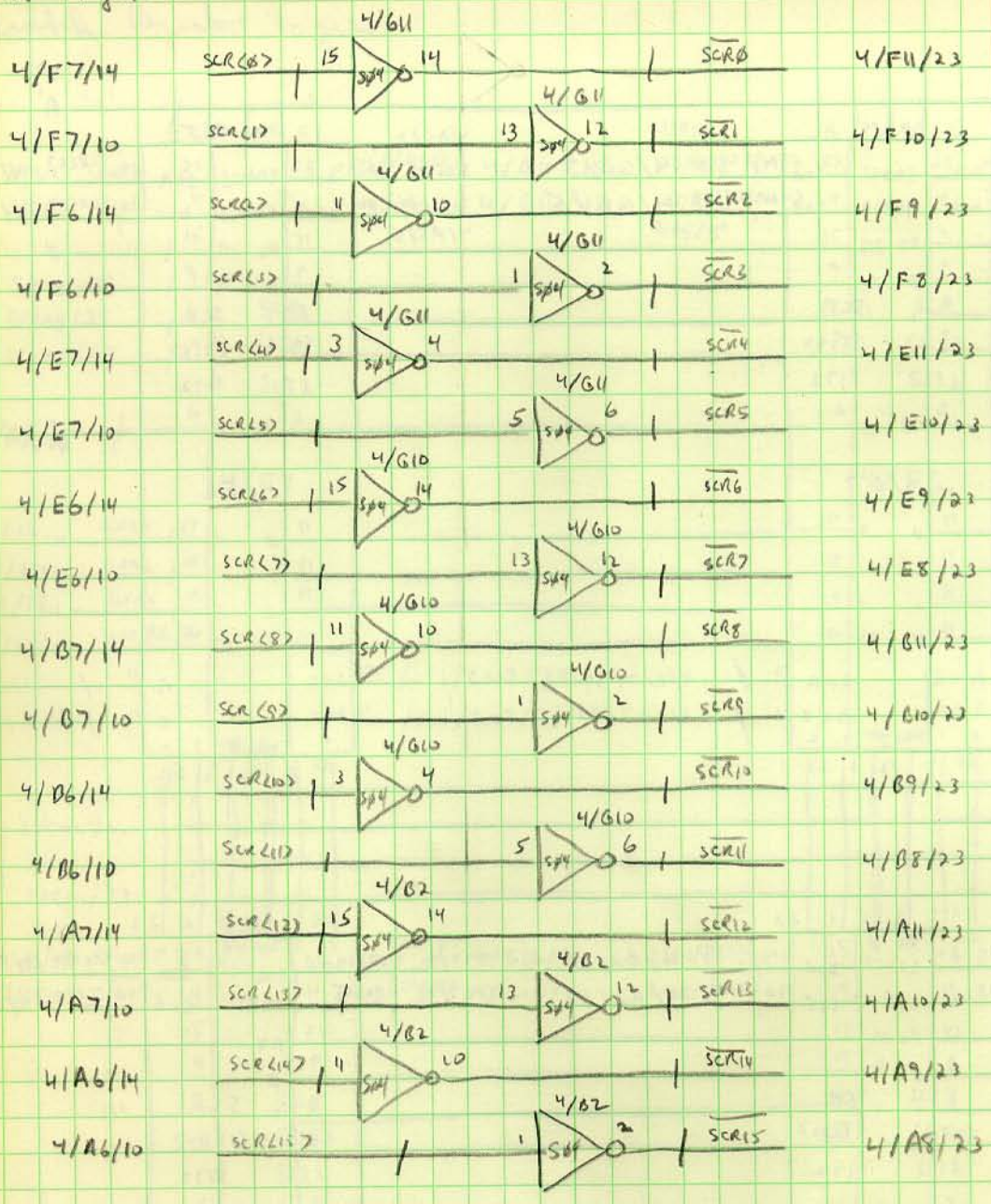




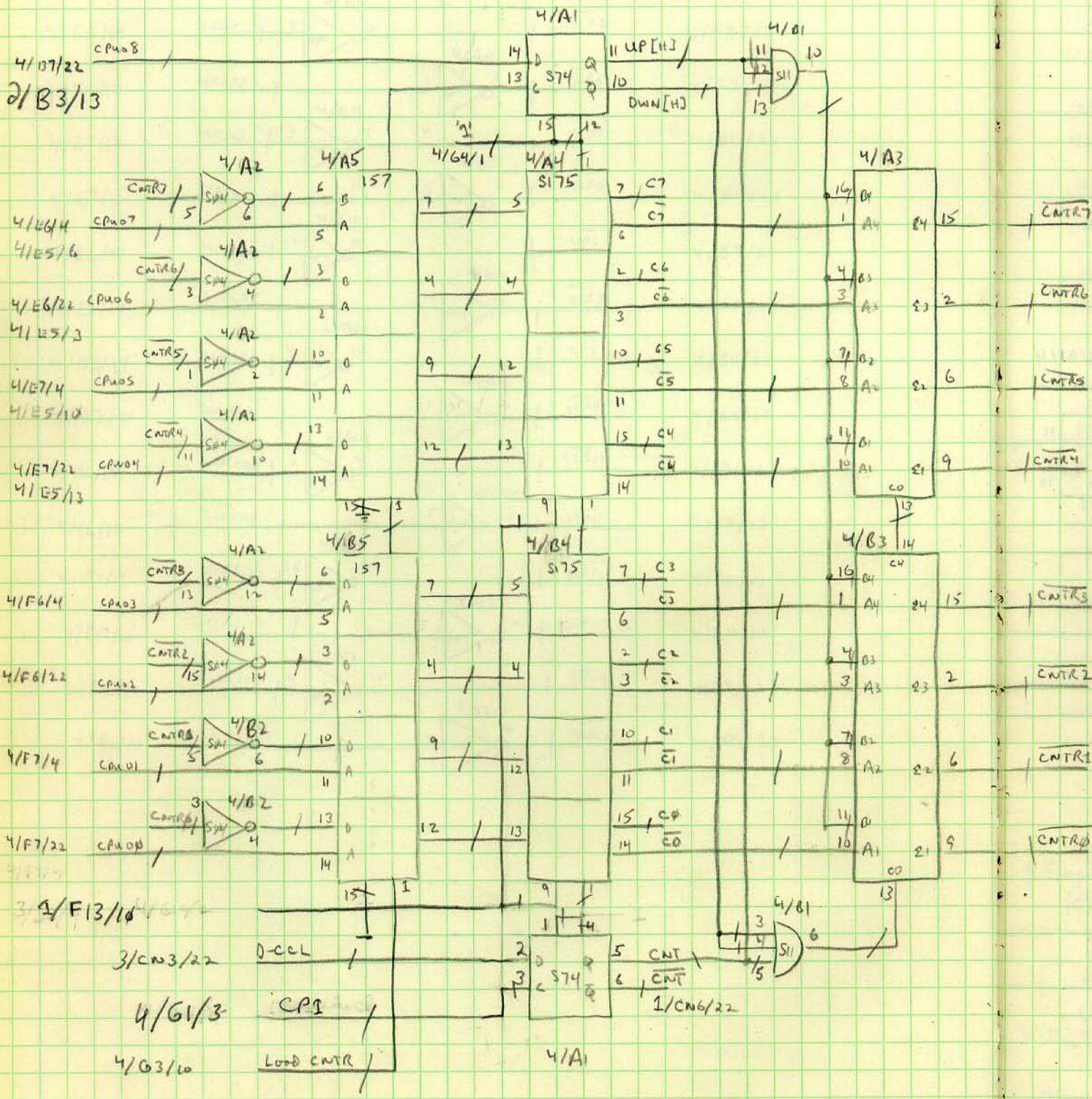
240476

CPA Panel #1 I/O Control

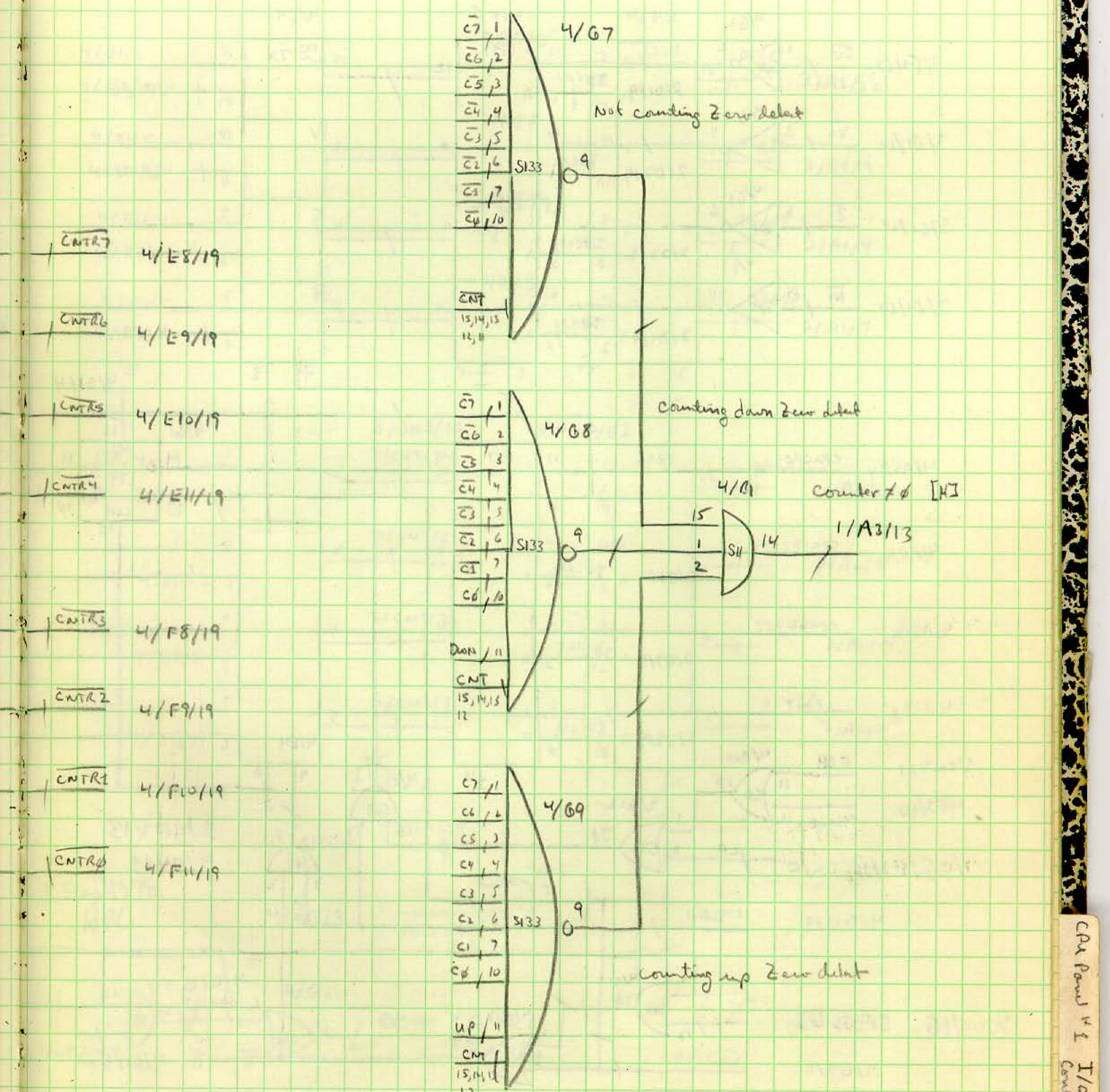
SCRATCH Register Inverters



CNTR Logic


4/A1
S74
UP [H]
DWN [H]
4/B1
S11
4/A2
S04
4/A5
157
4/B5
157
4/A4
S175
4/B4
S175
4/A3
4/B3
CNTR7
CNTR6
CNTR5
CNTR4
CNTR3
CNTR2
CNTR1
CNTR0
CPH07
CPH06
CPH05
CPH04
CPH03
CPH02
CPH01
CPH00
D-CCL
CPI
LOAD CNTR
CNT
4/64/1
4/61/3
4/G3/10
3/CN3/22
1/CN6/22
4/F13/10

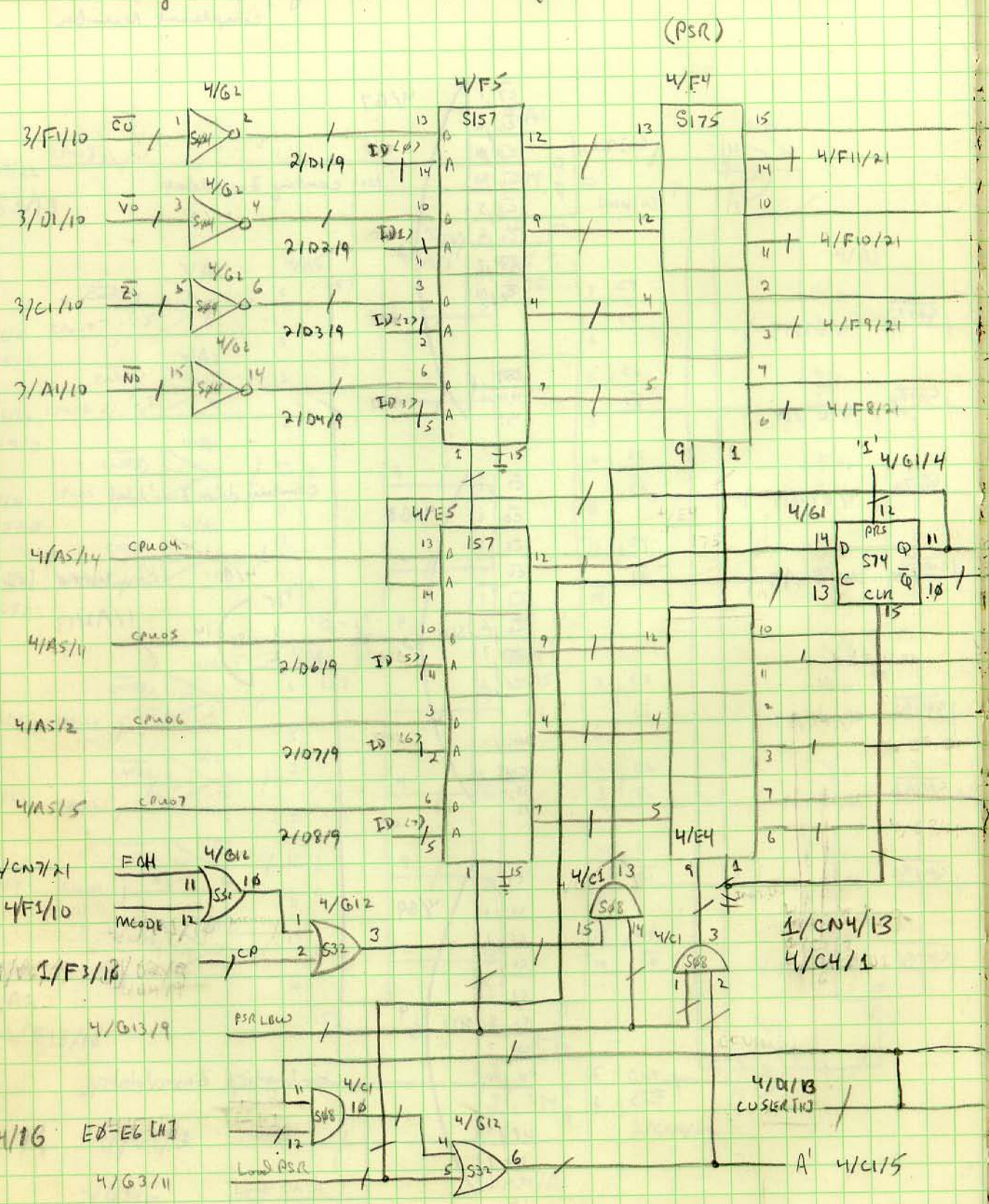
Counting performed on a two's complement Number

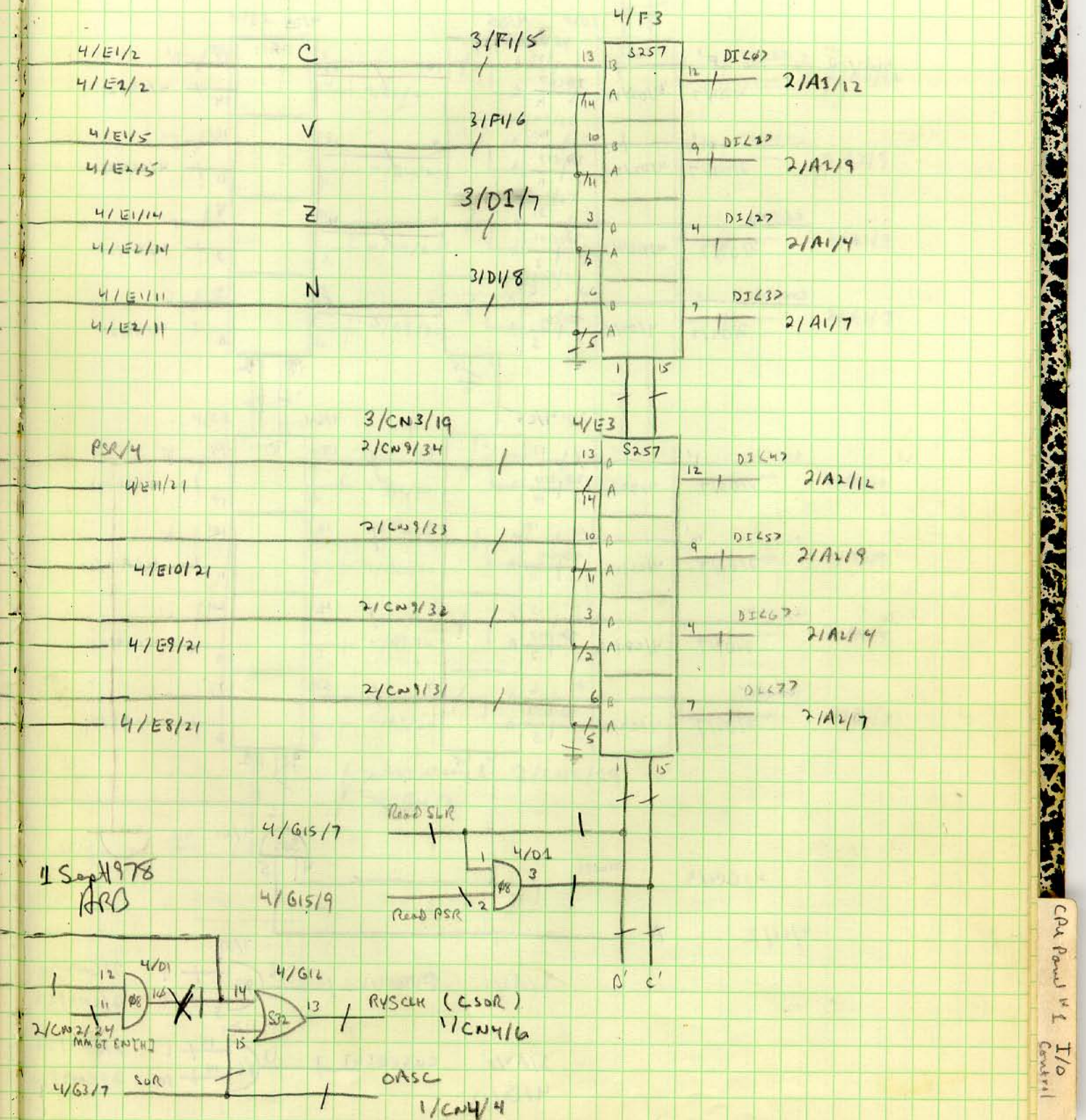


24 0476

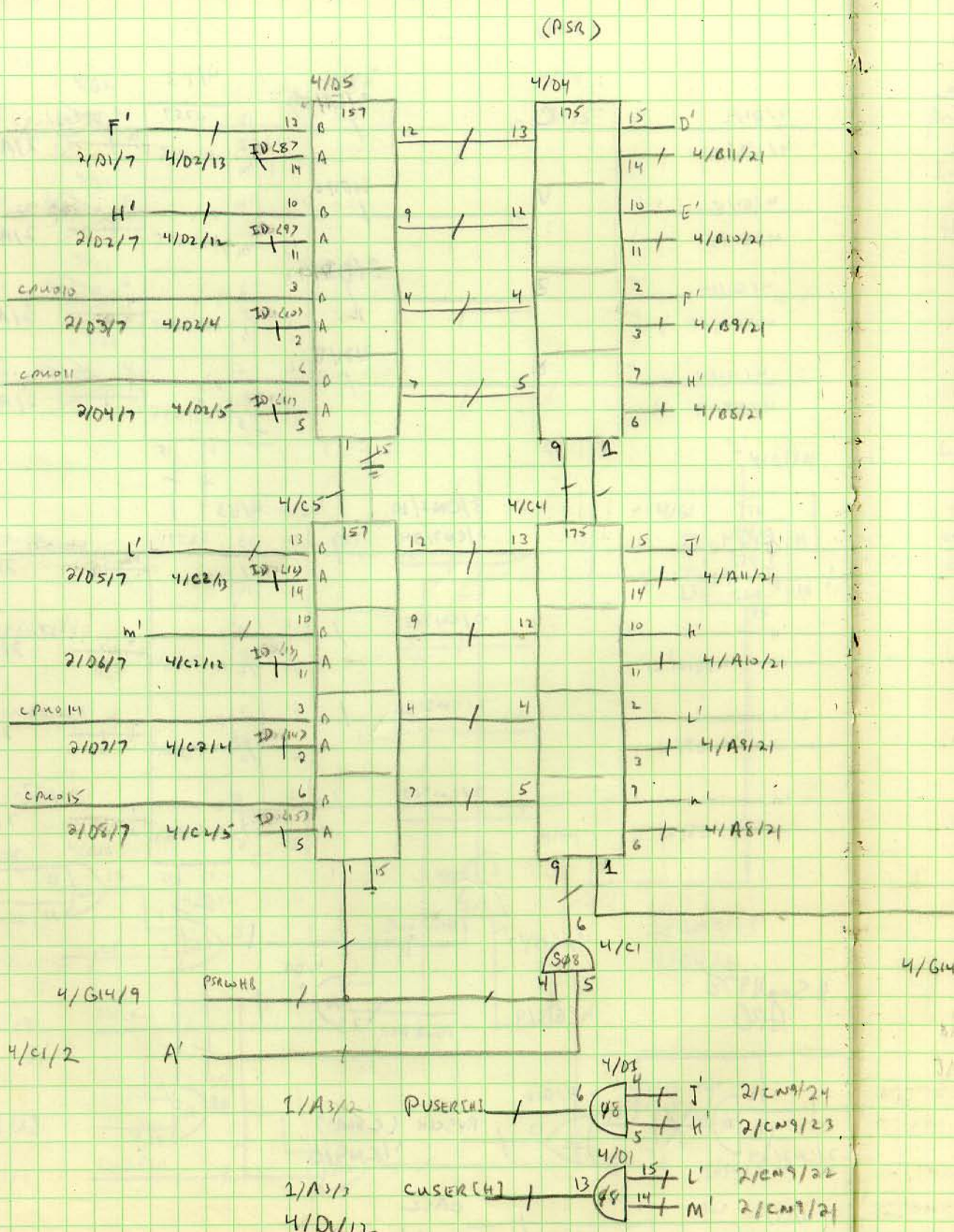
CPA Panel #1 I/O Control

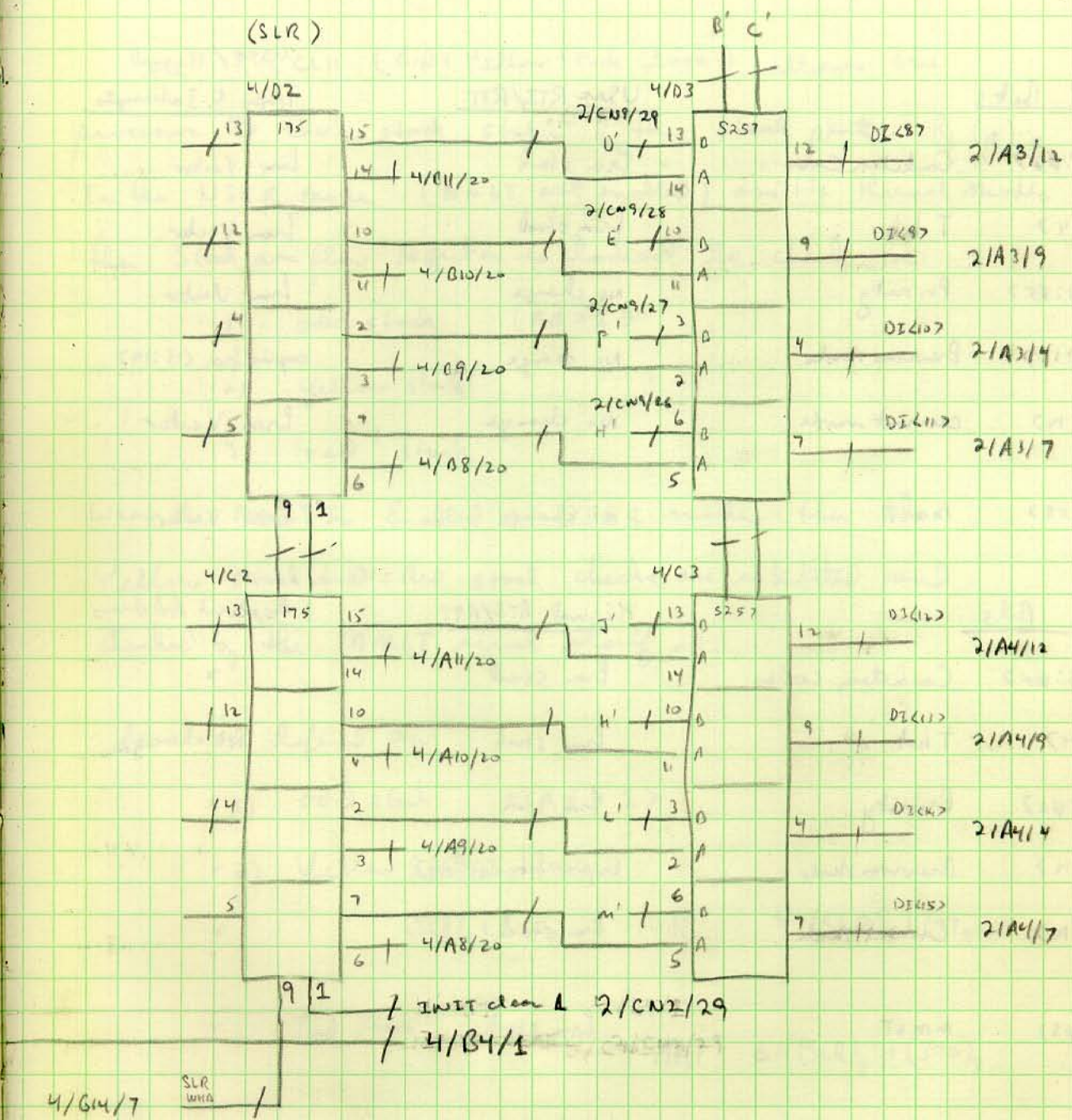
PSR / SLR Logic C, V, Z N, T, Priority Bits




4/F3
3/F1/5
S257
4/E1/2
C
4/E2/2
DI<0>
2/A3/12
4/E1/5
V
3/F1/6
4/E2/5
DI<1>
2/A2/9
3/D1/7
4/E1/14
Z
4/E2/14
DI<2>
2/A1/4
4/E1/11
N
3/D1/8
4/E2/11
DI<3>
2/A1/7
3/CN3/19
4/E3
PSR/4
2/CN9/34
S257
4/E11/21
DI<4>
2/A2/12
2/CN9/33
4/E10/21
DI<5>
2/A2/9
2/CN9/32
4/E9/21
DI<6>
2/A2/4
2/CN9/31
4/E8/21
DI<7>
2/A2/7
Read SLR
4/G15/7
4/D1
Read PSR
4/G15/9
1 Sept 1978
ARD
4/D1
4/G12
RYSCLK (CSOR)
1/CN4/6
2/CN2/24
MMBT ENTH
SOR
4/G3/7
ORSC
1/CN4/4
D'
C'
240476
CAM Panel #1 I/O Control

PSR / SLR Logic SLR <15:08> PSR <15:08>




(SLR)
4/D2
4/D3
B' C'
2/CN9/29
2/CN9/28
2/CN9/27
2/CN9/26
4/B11/20
4/B10/20
4/B9/20
4/B8/20
DI<8>
DI<9>
DI<10>
DI<11>
2/A3/12
2/A3/9
2/A3/4
2/A3/7
4/C2
4/C3
4/A11/20
4/A10/20
4/A9/20
4/A8/20
DI<12>
DI<13>
DI<14>
DI<15>
2/A4/12
2/A4/9
2/A4/4
2/A4/7
INIT clear L
2/CN2/29
4/B4/1
SLR WHA
4/G14/7

Notes on PSR operation (Hardware

PSR Bits		User RTI/RTT	User/Kernel Traps & Interrupts
<03:00>	Condition Codes	from stack	from Vector
<04>	T bit	from stack	from Vector
<07:05>	Priority	No change	from Vector
<13:12>	Previous Mode	No change	copied from <15:14>
<15:14>	current mode	No change	from Vector
<11:08>	MMGT	No change	from Vector

PSR Bits		Kernel RTI/RTT	Explicit Address
<03:00>	Condition codes	from stack	*
<04>	T bit	from stack	No change
<07:05>	Priority	from stack	*
<13:12>	Previous Mode	copied from <15:14>	*
<15:14>	Current Mode	from stack	*
<11:08>	MMGT	from stack	*

* changed by Kernel access or User access if PSR is mapped into user space

Stack Overflow codings

the RYS CLK (Red & Yellow Stack Clock) allows the processor to check ~~stack~~ status of the stack pointer R_6 (16). In the USER mode (MMGT not enabled) and the Kernel Mode the Stack overflow Register is checked to check for

1) odd stack (A∅ = 1)
2) yellow stack
3) red stack

When the MMGT is Enabled in USER mode than the Yellow stack and Red stack checks are inhibited and checked by the MMGT unit itself.

levels are defined as

1) odd stack <A∅ = 1>
2) Yellow Stack

$$(SLR)_8 + 340_8 \leq R_s \leq (SLR)_8 + 377_8$$

3) Red Stack

$$R_s \leq (SLR)_8 + (340)_8$$

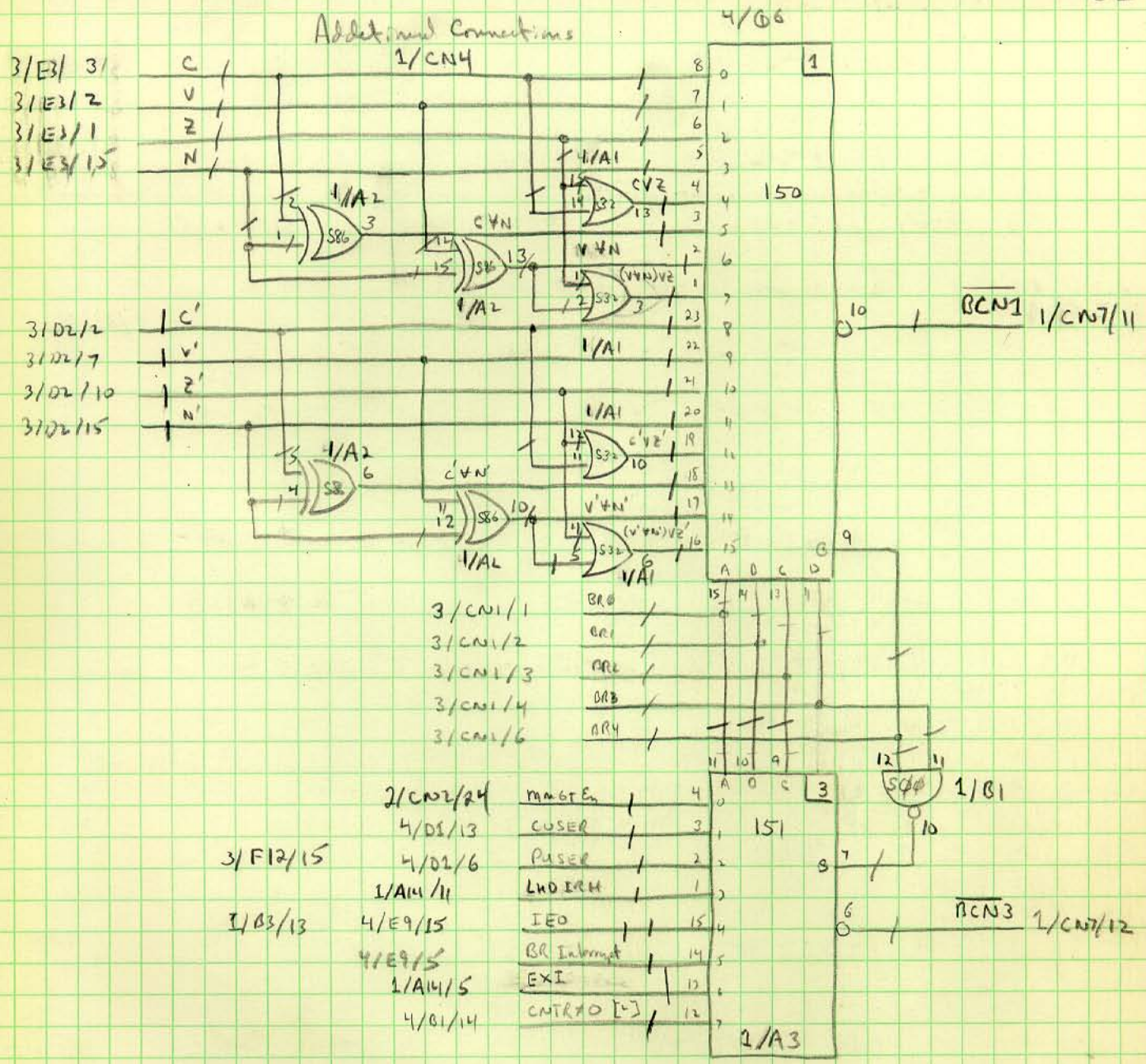
Computed by $R_S - SLR \rightarrow SOR$
all three checked simultaneously

24 of 76

Branch Selector Logic -

32 Branch conditions and their inverses

	Bit 4 = 0 Conditions (inverses selectable) (logical)		1	2	Bit 4 = 1 Conditions (inverses selectable) (machine)
0	C	BCS / BCC			0
1	V	BVS / BCC			T Bit
2	Z	BEQ / BNE			NC
3	N	BMI / BPL			PFDWN
4	CVZ	BLOS / BHI			BR (IR Decoder)
5	C ⊻ N				INT PENDING
6	V ⊻ N	BLT / BGE			SRC 0 (DIR6)
7	(V ⊻ N) V Z	BLE / BGT			BYTE
8	C'			3	MMGT En
9	V'				CUSER
10	Z'				PUSER
11	N'				Lookahead in Progress
12	C'VZ'				IEO
13	C' ⊻ N'				BR INTERRUPT
14	V' ⊻ N'				External I line
15	(V' ⊻ N') V Z'				CNTR ≠ 0



250+76

CPU Panel #1 I/O Control

CPU Board #1 I/O

UNIBUS 3	RES 180/390	I/O S04	I/O S30	BR S00	BR S32	1	Vector / Scratch Data 7
	RES 180/390	I/O S00	I/O S10	ØØ	BR S86	2	
	I/O 8838	I/O Res	I/O S30	1Ø	BR 157	3	
	I/O 8838	I/O 122	I/O L00	I/O S21	INT S74	4	
2	RES TMOT	I/O L20	I/O L00	I/O S00	I/O S08	5	<32:63> and to Console 6
	REC 8837	I/O L00	I/O S30	I/O L00	I/O S20	6	
	REC 8837	I/O S10	I/O 1Ø	I/O S32	I/O S64	7	
INTERNAL INTERRUPT 1	IPL 42	I/O 1Ø	I/O ØØ	I/O L00	I/O 30	8	
	IPL 148	I/O 20	I/O S08	I/O S74	I/O 20	9	<0:31> and to Console 5
NPR TMOT	RES 180	NPR S00	I/O S04	I/O S74	I/O S30	10	
NPR 38	ISL 33	I/O S175	I/O S175	I/O S175	I/O S00	11	
NPR S20	ISL S 33	I/O S175	I/O S175	I/O S175	I/O S10	12	
NPR S20	ISL S10	IPL S70	IPL S10	IPL S11	IPL S11	13	I/O Errors / Conditions 4 INTerrupt Data
ISL ØØ	ISL S00	IPL S00	IPL S04	IPL S00	IPL S74	14	
ISL L00	ISL S00	IPL 174	IPL S175	IPL S175	X	15	
H	G	F	E	D	A		250476

Connector Wiring (Board #1)

#1 INTERNAL INTERRUPT control

1	CLOCK	← 1/C15/12 + 1/CN3/32	24	GND	
2	INT0	← 1/D15/3	23	CCLOCK	→ 1/E811
3	INT1	← 1/D15/4	22	CINT0	→ 1/E812
4	INT2	← 1/D15/6	21	CINT1	→ 1/E813
5	INT3	← 1/D15/14	20	CINT2	→ 1/E814
6	GND		19	CINT3	→ 1/E815
7	INT4	← 1/D15/13	18	GND	
8	INT5	← 1/D15/11	17	CINT4	→ 1/E816
9	EX ILINE	← 1/E9/10	16	CINT5	→ 1/E817
10			15	C EX ILINE	→ 1/E819
11			14		
12	GND		13		

#2 UNIBUS MAP / MMGT Extra's

1	UBA18	← 2/D14/3	24	GND	
2	UBA19	← 2/D14/6	23		
3	UBA20	← 2/D15/13	22		
4	UBA21	← 2/D15/14	21		
5	UMDF [H]	← 1/CN7/13	20		
6	GND		19		
7	AD-BUS L	← 1/C4/14	18	GND	
8	MSRC L	— 2/CN4/17	17		
9	C1D (DATO(B))	← 1/C8/3	16		
10	DATIR H	← 1/A7/12	15		
11	DATIP L	← 2/B9/2	14		
12	GND		13		

#3

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

H3 UNIBUS Connections

32
10
10
52
3
55

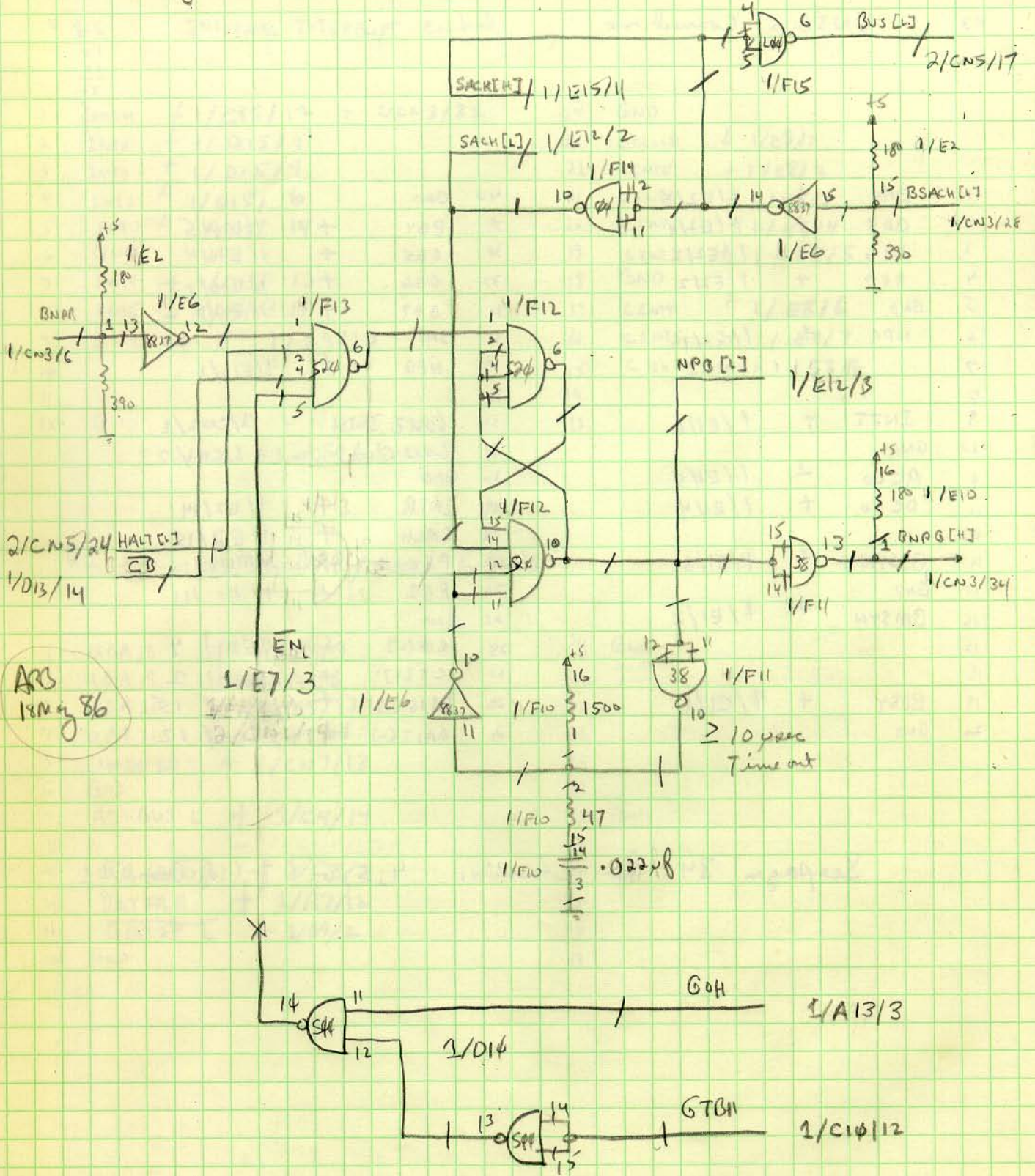
1	BR4	+	1/E2/5
2	BR5	+	1/E2/4
3	BR6	+	1/E2/3
4	BR7	+	1/E2/2
5	GND		
6	NPR	+	1/E2/1
7			
8			
9	INIT	+	1/E1/6
10	GND		
11	AC LO	+	1/E1/5
12	DC LO	+	1/E1/4
13			
14	BSSYN	+	1/E1/3
15	GND		
16	BMSYN	+	1/E1/2
17			
18			
19	BUSY	+	1/E1/1
20	GND		

40	GND		
39	BG4	+	1/E10/5
38	BG5	+	1/E10/4
37	BG6	+	1/E10/3
36	BG7	+	1/E10/2
35	GND		
34	NPG	+	1/E10/1
33			
32	60HZ INTH	+	1/CN1/1
31	60Hz Clock Clear L	+	1/CN1/23
30	GND		
29	INTR	+	1/E2/14
28	SACK	+	1/E2/15
27	PC0	+	1/E1/10
26	PC1	+	1/E1/11
25	GND		
24	C0 [L]	+	2/E11/4
23	C1 [L]	+	2/E11/1
22	BA16 [L]	+	2/E11/15
21	BA17 [L]	+	2/E11/12

See page 34 for Connectors 4, 5, 6, & 7 of Board H1

25 Oct 76

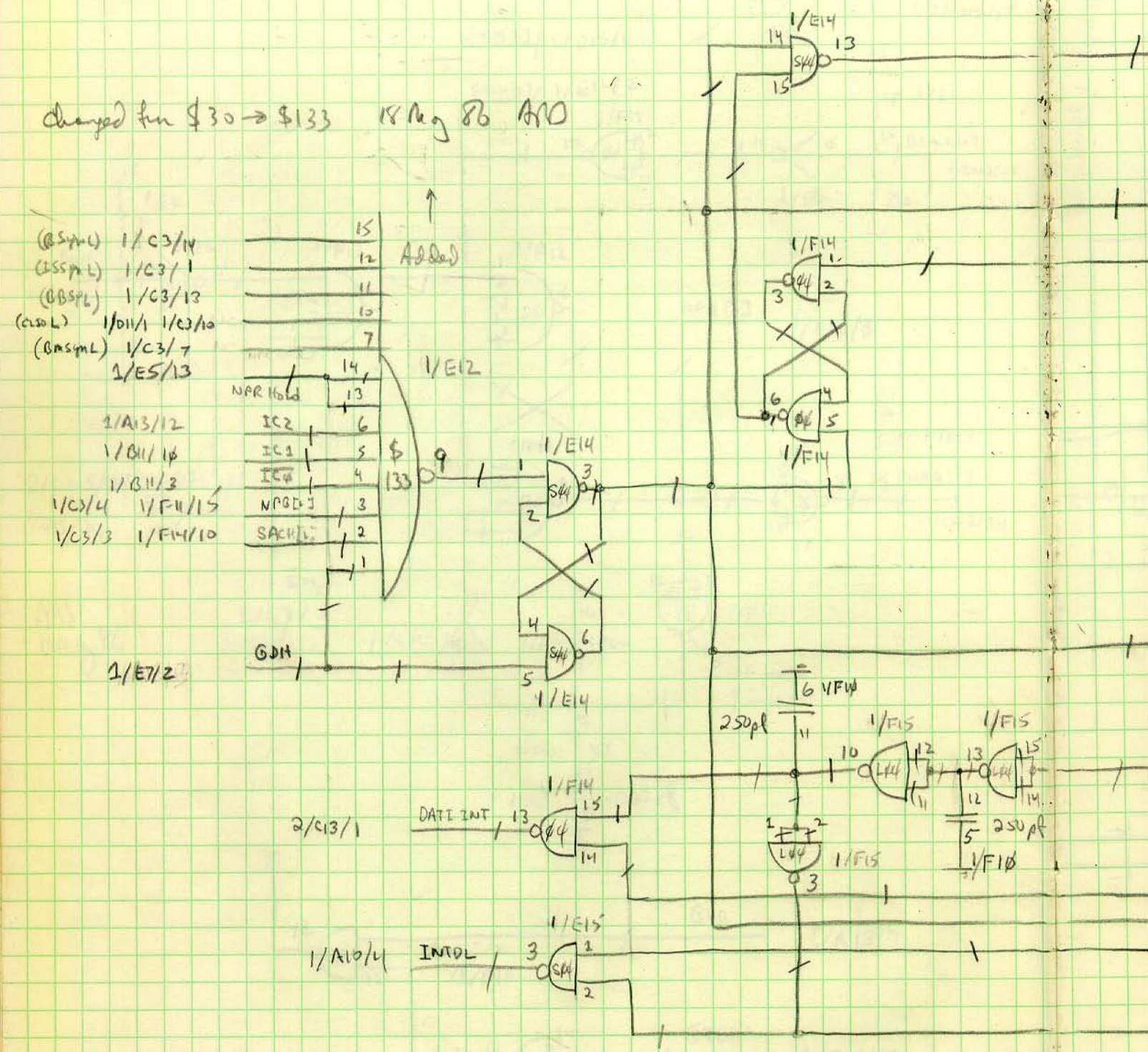
NPR Logic

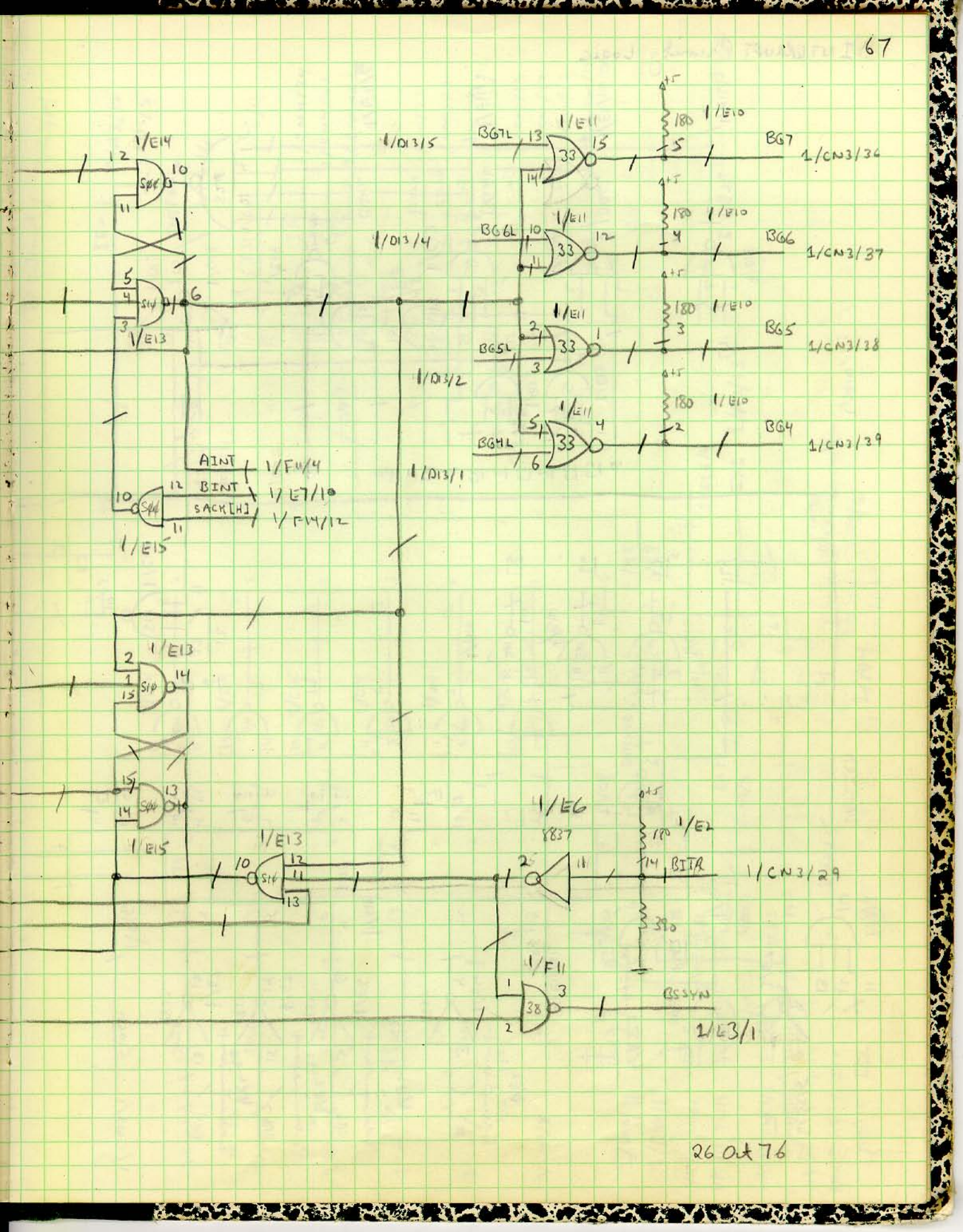


ARB
18 May 76

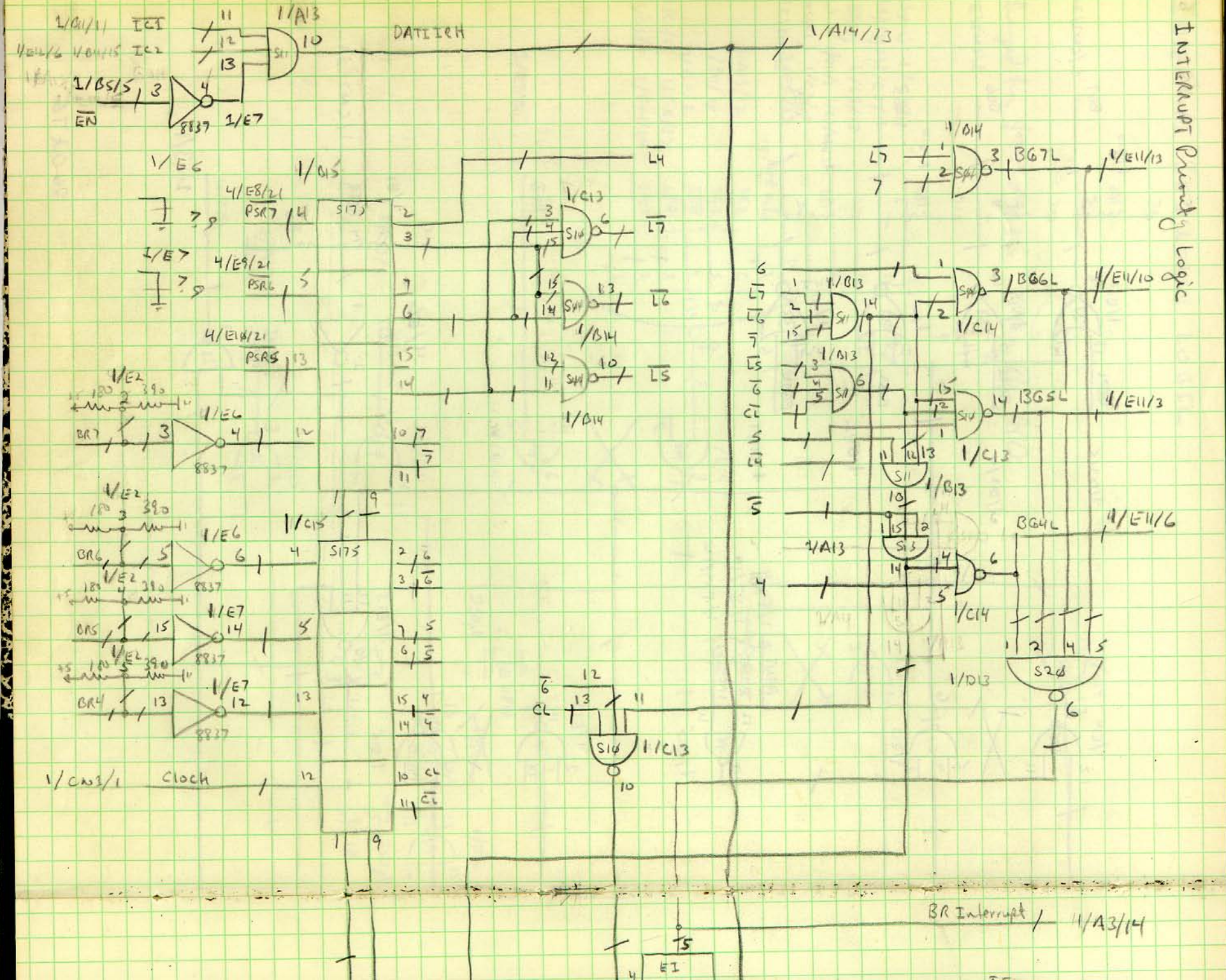
26 Oct 76

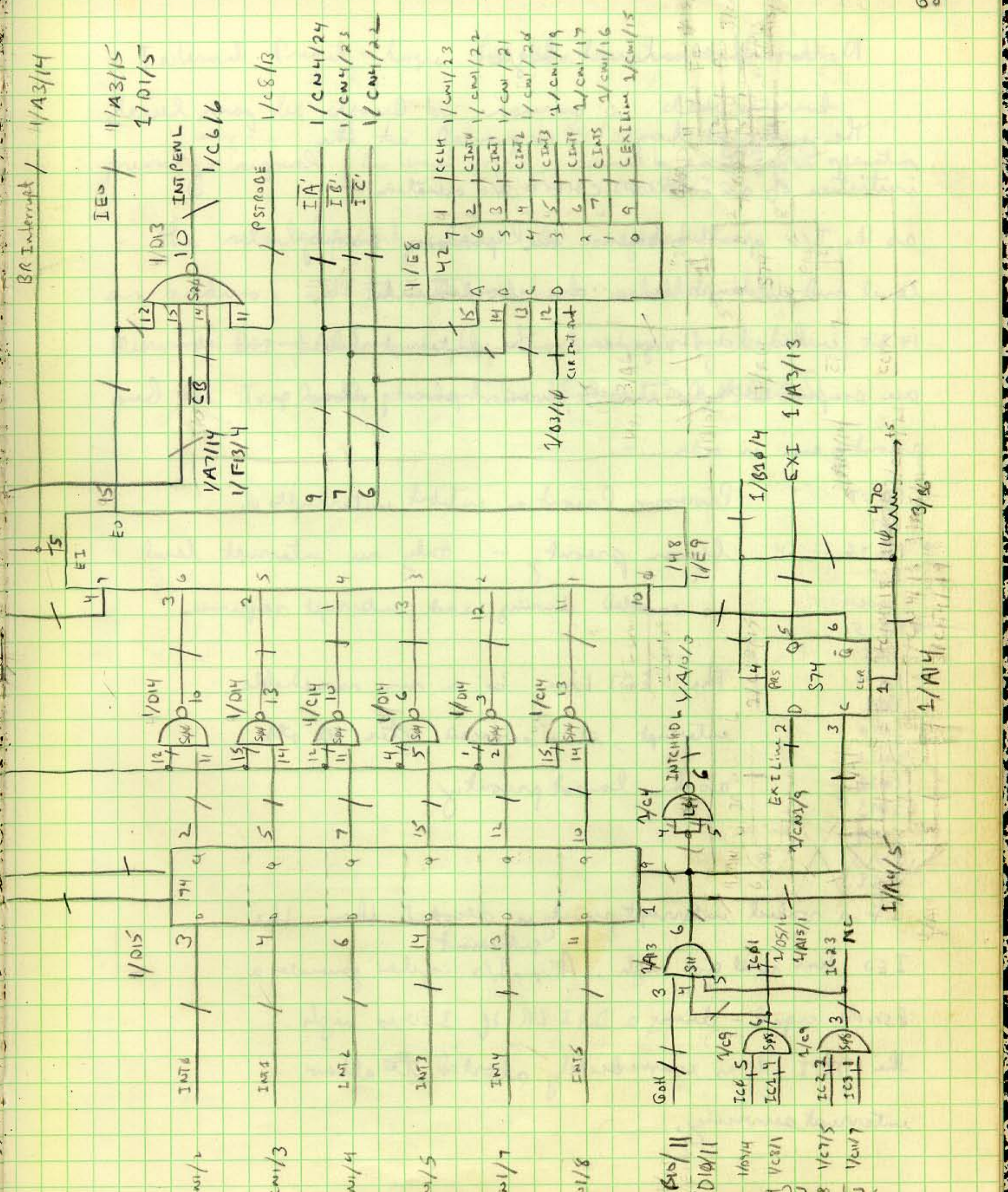
INTERRUPT SEQUENCE LOGIC




1/E14
1/D13/5
BG7L
1/E11
33
180
1/E10
BG7
1/CN3/36
1/D13/4
BG6L
BG6
1/CN3/37
1/E13
BG5L
BG5
1/CN3/38
1/D13/2
BG4L
BG4
1/CN3/39
1/D13/1
AINT
1/F14/4
BINT
1/E7/10
SACK[H]
1/F14/12
1/E15
1/E6
8837
BIIR
1/CN3/29
390
1/F11
BSSYN
1/E3/1

26 Oct 76


INTERRUPT Priority Logic
DATI IRH
BR Interrupt
CLOCK
BG7L
BG6L
BG5L
BG4L
EI
S11
S14
S175
S20
8837
390
180


BR Interrupt
1/A3/14
IEO
1/A3/15
1/D1/5
INTPENL
1/C6/6
PSTROBE
1/C8/13
1/CN4/24
1/CN4/25
1/CN4/22
1/E8
EXI
1/A3/13
1/B10/4
S74
EXI Line 2
INTCHDL
INT0
INT1
INT2
INT3
INT4
INT5
1/D15
1/A4/5
1/A14
1/D10/11
NC

Notes on the interrupt logic

The interrupt logic is sequenced at the initiation of an INTERRUPT CHECH I/O operation - as the I/O operation begins the processor priority level and interrupt lines are loaded into the 14 bit current status register. The interrupt lines are compared with the current processor priority level - priorities are in order -

→ PSR=7
BR7
→ PSR=6
BR6
CLOCH
→ PSR=5
BR5
→ PSR=4
BR4
INT0
INT1
INT2
INT3
INT4
INT5
EXI

Processor Priorities inhibit interrupts of lesser priority - only one interrupt level is enabled during each interrupt sequence.

The EXI Line is a non maskable interrupt, it is serviced after all others as the lowest priority

If a valid interrupt priority is decoded then the IED line will go high. A subsequent I/O cycle generates a Pstrobe signal - during a DATI IR if IED is high the DATI IR is immediately aborted to allow interrupt servicing.

Internal Priority logic for the serviced priority level may be cleared by issuing a clear current priority signal, Ex Internal logic is cleared by an INTERRUPT ENPUT operation.

The selected priority level is encoded to an address $\overline{IA}'$, $\overline{IB}'$, $\overline{IC}'$ which selects the Microcode Branch Address for the machine priority level and the Trap vector constant for that interrupt level

BUS Controller Coding

The Bus controller is programmed by 10 bits of control data from the Microprogram with the following designations

1 bit	ENABLE I/O Cycle	IO9
4 bits	I/O function & timing	IOØ, IO1, IO2, IO3
1 bit	Byte operation enable	IO4
1 bit	Special/NDA Enable	IO5
3 bits	Memory management Control	IO6, IO7, IO8

to initiate an I/O operation the Enable bit must be asserted, else the I/O controller ignores the data on the other I/O lines

The I/O functions and timing are defined on the next page –

delayed I/O's start at the beginning of the next microinstruction

immediate I/O's start at the beginning of the current microinstruction

IO3 I

Ø
Ø
Ø
Ø
Ø
Ø
Ø
Ø
1
1
1
1
1
1
1
1
1

IO3	IO2	IO1	IO0	
0	0	0	0	DATI (delayed) [Byte/Special/NDA/MMGT]
0	0	0	1	DATIP (delayed) [Byte/Special/NDA/MMGT]
0	0	1	0	DATO (delayed) [Byte/Special/NDA/MMGT]
0	0	1	1	DATOB (delayed) [Special/NDA/MMGT]
0	1	0	0	DATI IR (delayed) [Byte/Special/NDA/MMGT]
0	1	0	1	Lookahead DATI IR (delayed) [Byte/Special/NDA/MMGT]
0	1	1	0	INTERRUPT INPUT (delayed)
0	1	1	1	INIT (delayed)
1	0	0	0	DATI (immediate)
1	0	0	1	DATIP (immediate)
1	0	1	0	DATO (immediate)
1	0	1	1	DATOB (immediate)
1	1	0	0	DATI IR (immediate)
1	1	0	1	Lookahead DATI IR (immediate)
1	1	1	0	INTERRUPT INPUT (immediate)
1	1	1	1	INTERRUPT CLOCK (immediate)

28 OCT 76

BUS Controller Coding

I04 Byte Enable Bit - if Byte bit of IR decoded data is set then during - DATI (P, IR) operations Byte operations may be specified by setting the Byte Enable Bit of the I/O control, else word operations are performed

DATO may also be conditionally a byte operation

The assertion of a byte operation on an odd address location will cause the BUS I/O hardware to transfer low byte CPU data to high Byte Bus data lines or transfer high Byte Bus data to the low Byte CPU input lines - automatically performing the Byte swapping operations for odd Byte operations

I05

3 MM6T Control Bits - I06, I07, I08

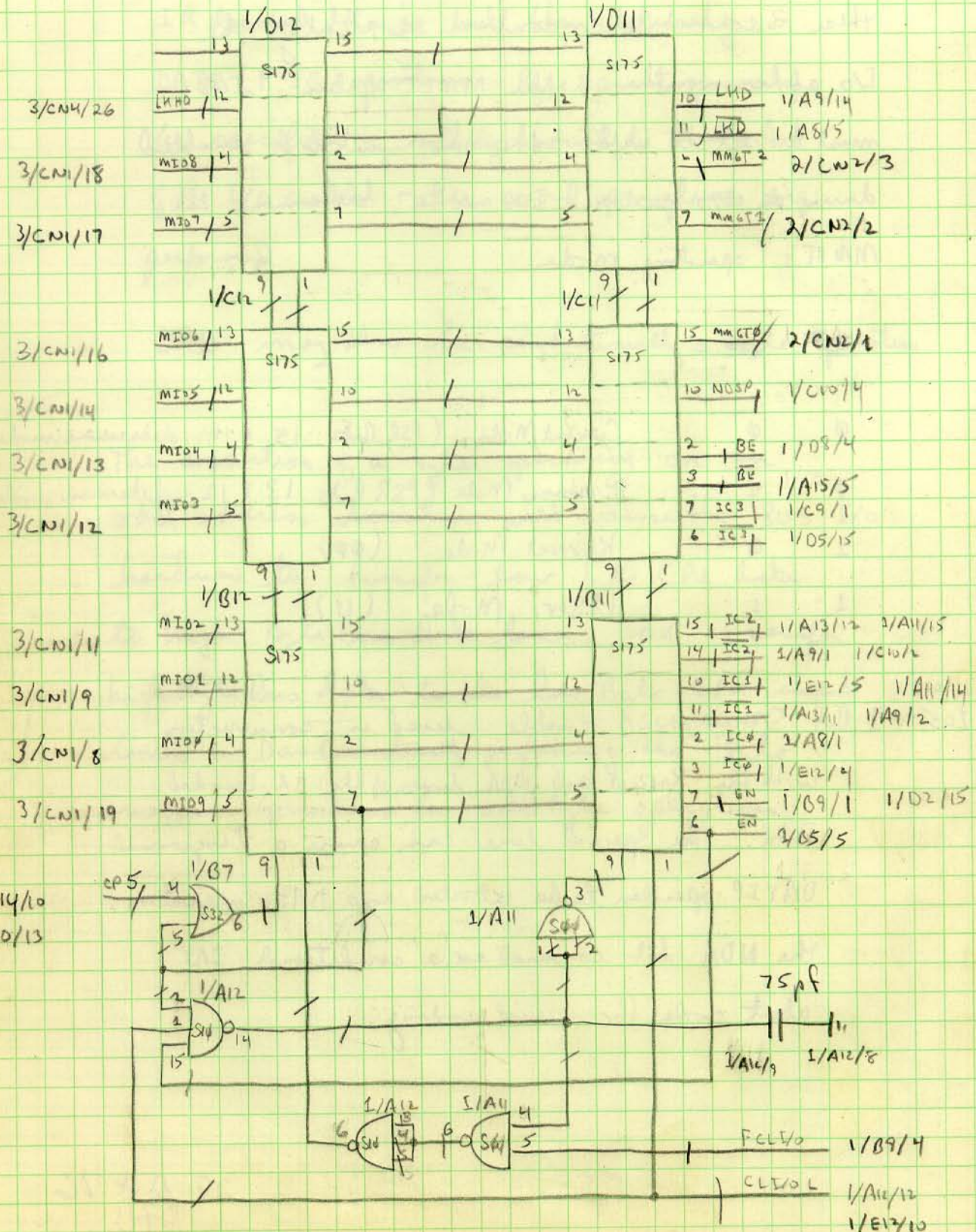
These 3 control bits control explicitly the I/O addressing through the MM6T system. I08 must be set to allow the MM6T unit to be enabled during an I/O operation. I06 and I07 determine the MM6T's operating mode

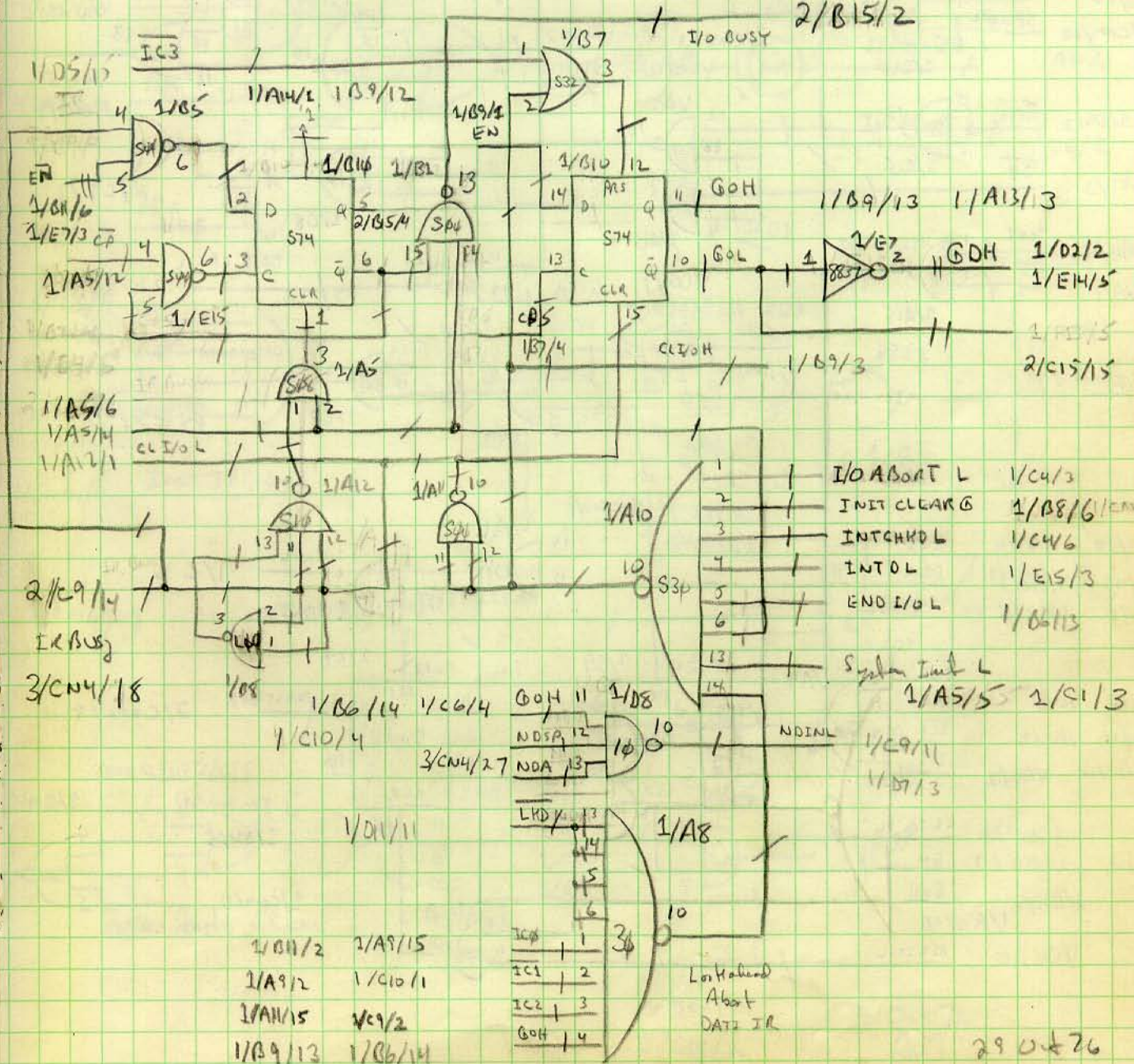
I07	I06	
0	0	Current Mode (PSR Bits 15 & 14 determine mode)
0	1	Previous Mode (PSR Bits 13 & 12 determine mode)
1	0	Kernel Mode (00)
1	1	User Mode (11)

I05 1 Bit Special/NDA Enable used in conjunction with the Special and NDA lines of the IR Decoded Data. The Special line can cause a Programmed DATIP operation to be aborted as a DATI operation. The NDA bit is used as a conditional I/O abort code for special coding.

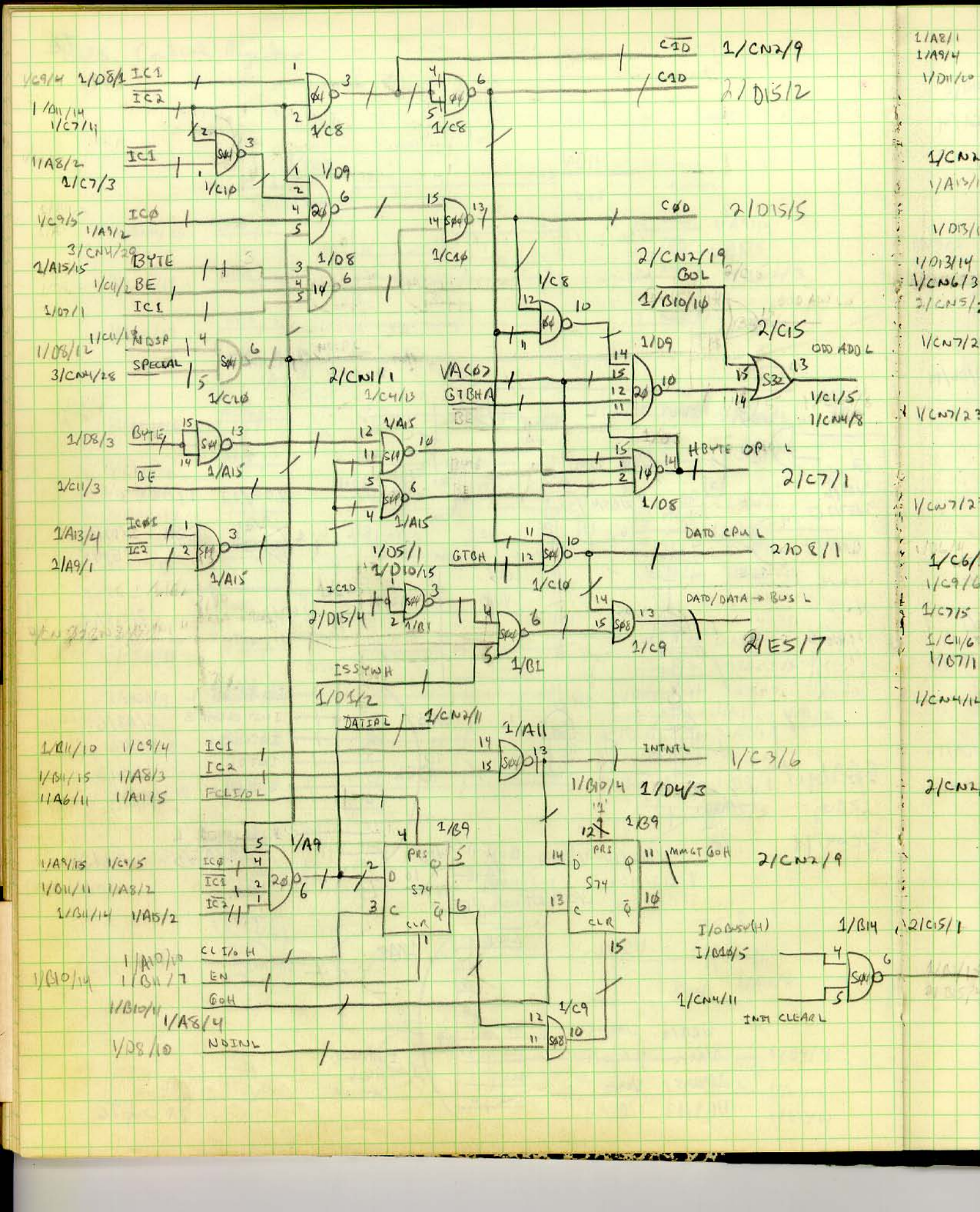
28 Oct 76
KRB

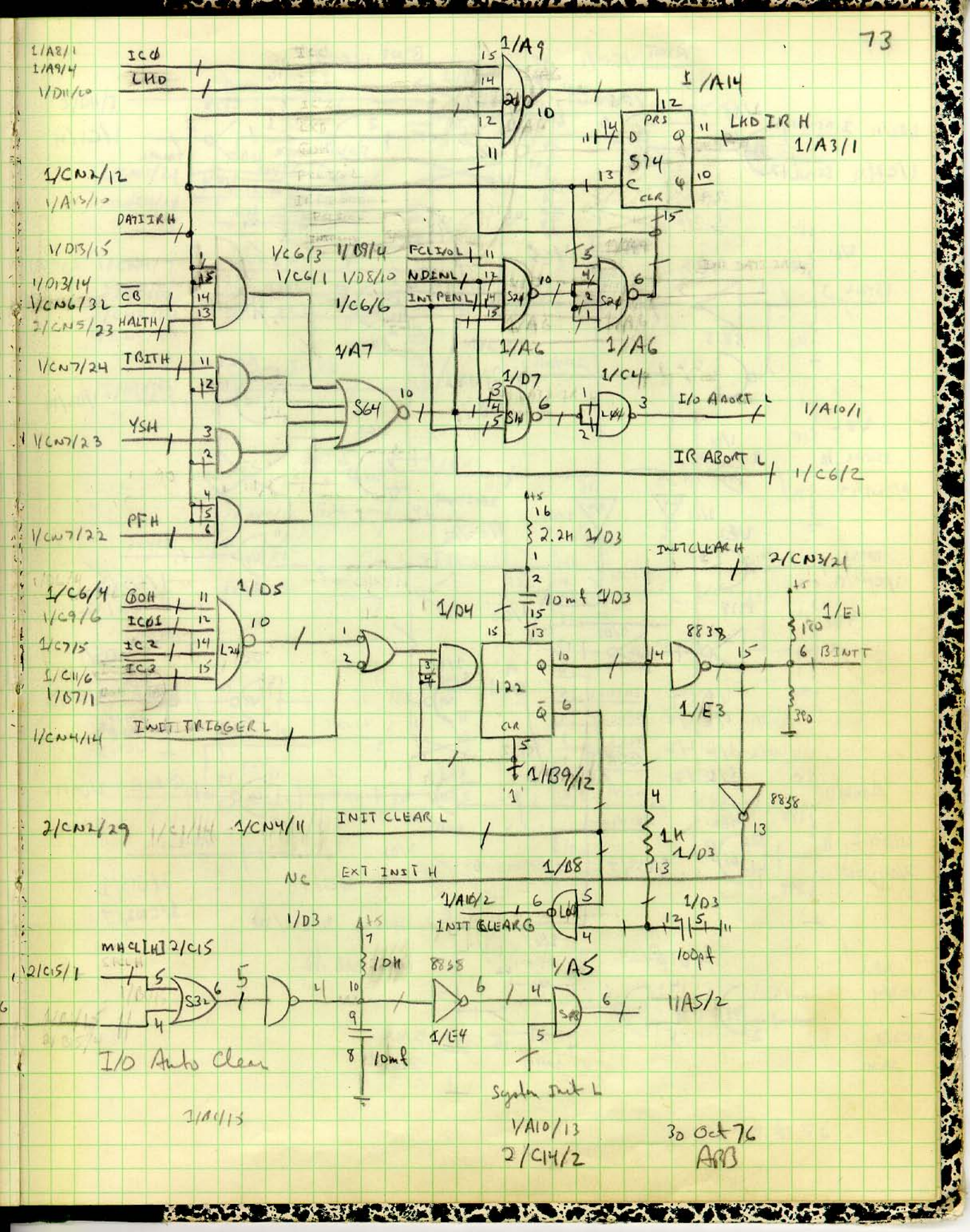
BUS Control Register

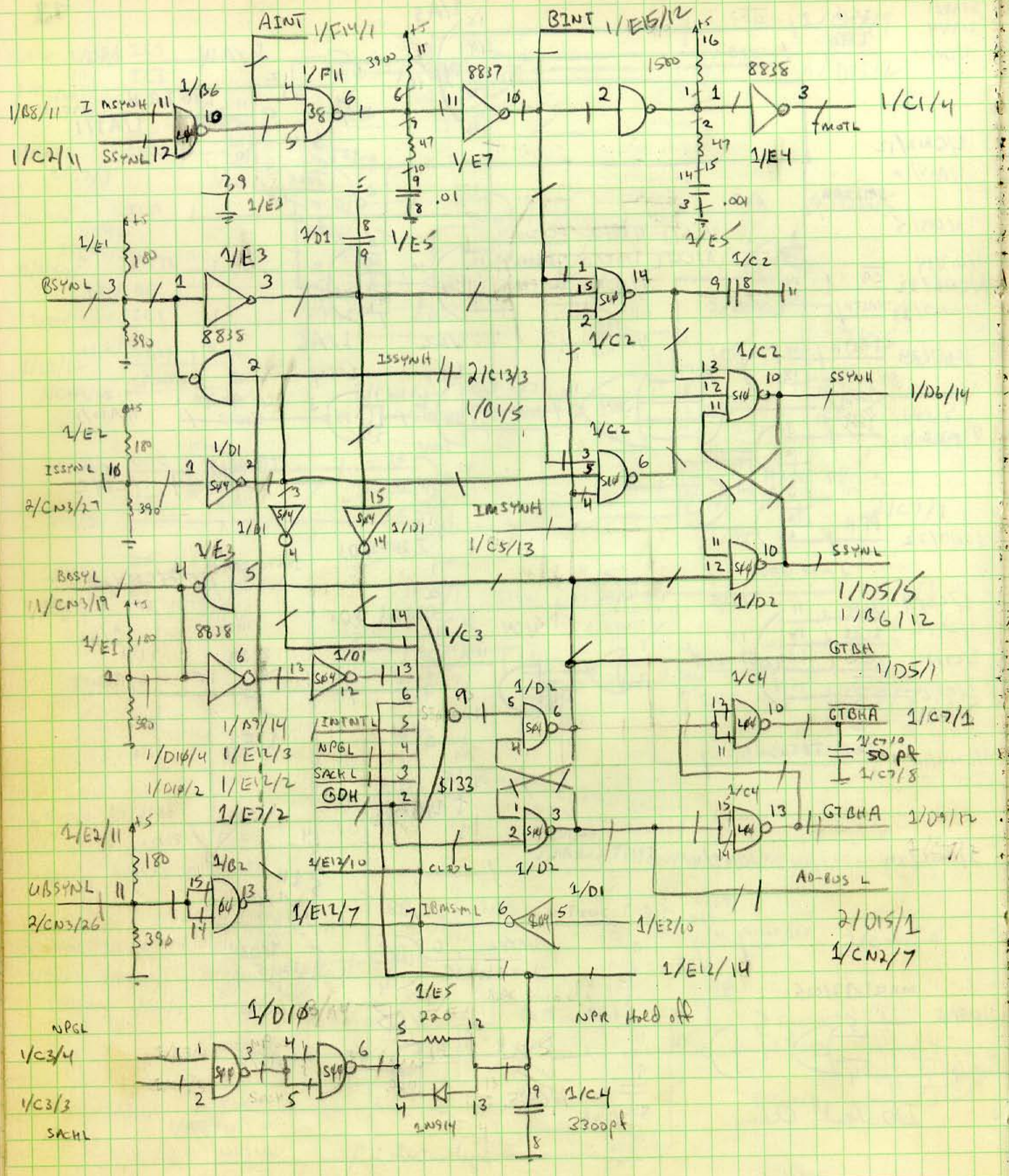


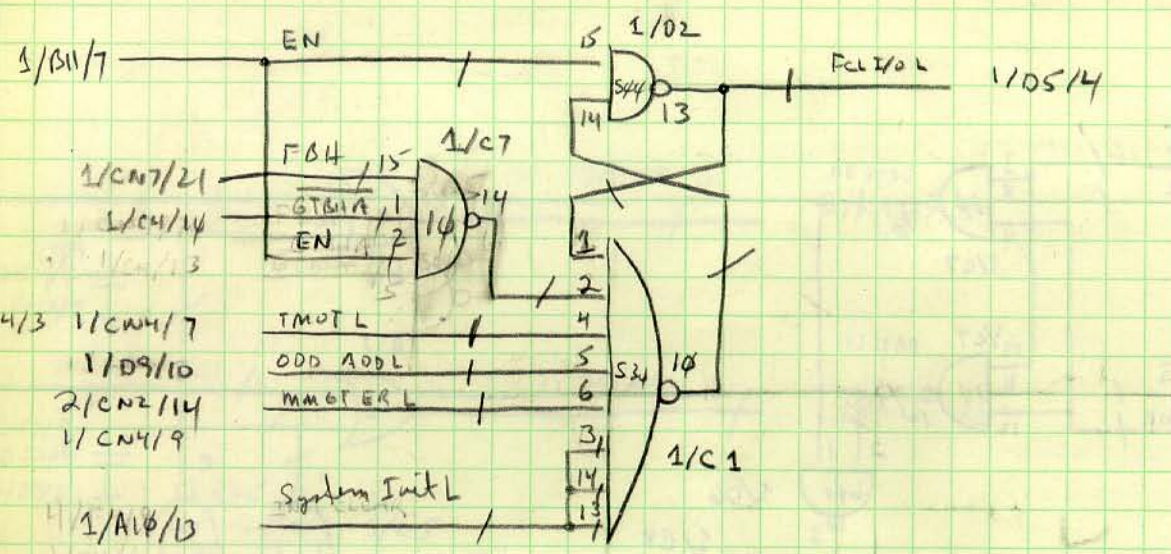

2/B15/2
I/O BUSY
IC3
1/D5/15
1/A14/2
1/B9/12
1/B7
S32
1/B9/1
EN
1/B5
1/B14
1/B2
1/B10
S74
PRE
CLR
GOH
GOL
1/B9/13
1/A13/3
1/E7
8837
1/D2/2
1/E14/5
2/C15/15
2/B5/4
1/B7/4
CLI/OH
1/B9/3
1/A5
1/A5/6
1/A5/14
1/A2/1
CL I/O L
1/A12
1/A11
S10
S20
S30
1/A10
I/O ABORT L
1/C4/3
INIT CLEAR G
1/B8/6
INTCHKD L
1/C4/6
INT O L
1/E15/3
END I/O L
1/B6/13
System Init L
1/A5/5
1/C1/3
2/C9/14
IR BUSY
3/CN4/18
1/D8
1/B6/14
1/C6/4
1/C10/4
GOH
NDSA
NDA
3/CN4/27
NDINL
1/C9/11
1/B7/3
1/D11/11
LKD
1/A8
IC0
IC1
IC2
GOH
Lockout and Abort DATA IR
1/B11/2
2/A9/15
1/A9/2
1/C10/1
1/A11/15
1/C9/2
1/B9/13
1/B6/14

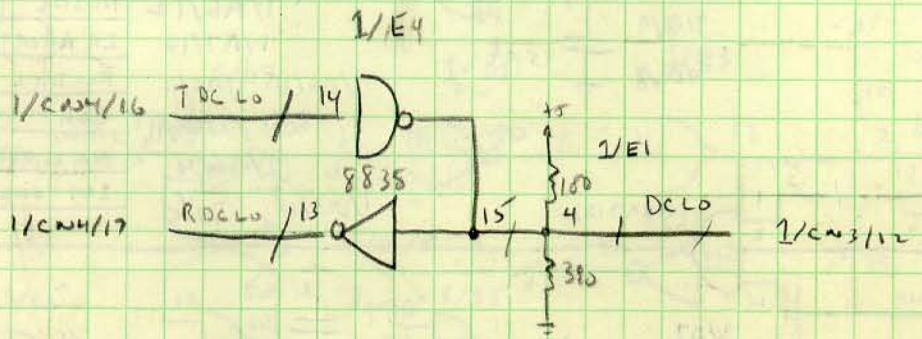
29 of 76

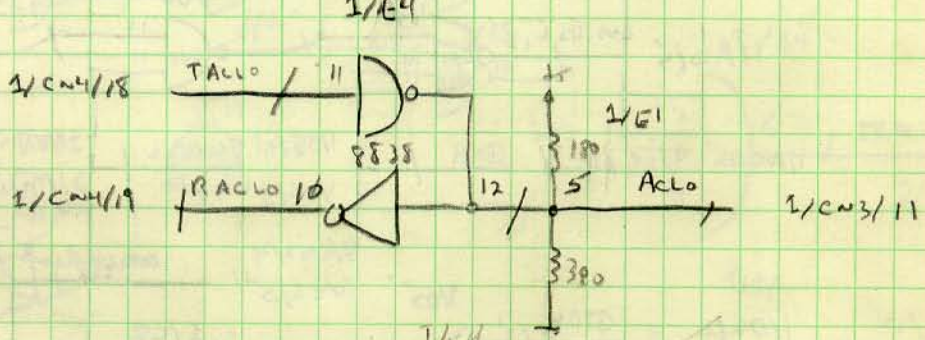

C1D
1/CN2/9
C1D
2/D15/2
IC1
IC2
1/C8
IC1
1/C10
1/C9
IC0
BYTE
BE
IC1
1/D8
NDSP
SPECIAL
1/C10
C0D
2/D15/5
1/C14
2/CN2/19
GOL
1/B10/10
1/C8
1/D9
2/C15
ODD ADD L
2/CN1/1
VAC07
GTBHA
1/C1/5
1/CN4/8
HBYTE OP L
2/C7/1
1/D8
1/A15
DATO CPU L
2/D8/1
GTBH
1/C10
1/D5/1
1/D10/15
IC1D
2/D15/4
1/B1
DATO/DATA → BUS L
2/E5/7
1/C9
ISSYWH
1/D5/2
1/B1
DATIAL
1/CN2/11
1/A11
INTNTL
1/C3/6
1/B10/4
1/D4/3
1/B9
MMGT GOH
2/CN2/9
1/A9
PRS
S74
CLR
I/O BUSY(H)
1/B14
2/C15/1
I/O BSY/5
1/CN4/11
INH CLEAR L
CL I/O H
EN
GOH
NDINL
1/C9
1/A8/4


1/A8/1
1/A9/4
1/D11/10
ICØ
LHD
1/A9
1/A14
LHD IR H
1/A3/1
1/CN2/12
1/A13/10
DATIRH
1/D13/15
1/C6/3
1/C6/1
1/D8/4
1/D8/10
1/D13/14
1/CN6/32
2/CN5/23
CB
HALTH
1/C6/6
1/A7
1/A6
1/A6
1/CN7/24
TRITH
1/D7
1/C4
I/O ABORT L
1/A10/1
1/CN7/23
YSH
IR ABORT L
1/C6/2
1/CN7/22
PFH
2.2H 1/D3
INITCLEAR H
2/CN3/21
1/C6/4
1/C9/6
1/C7/5
1/C11/6
1/D7/1
GOH
ICØ1
IC2
IC3
1/D5
1/D4
10mf 1/D3
1/E1
8838
BINIT
1/E3
1/CN4/14
INIT TRIGGER L
1/B9/12
2/CN2/29
1/CN4/11
INIT CLEAR L
8838
1K 1/D3
NC
EXT INIT H
1/B8
1/A10/2
INIT CLEAR G
1/D3
100pf
MH C[H] 2/C15
2/C15/1
1/D3
10H
8838
1/A5
1/A5/2
1/E4
I/O Auto Clear
System Init L
1/A10/13
2/C14/2
1/A4/13
30 Oct 76
ARB


AINT 1/F14/1
BINT 1/E15/12
1/B6
1/F11
8837
1/E7
8838
1/E4
1/C1/4
1/B8/11
1/C7/11
SSYNL
1/E3
1/D1
1/E5
1/E1
BSYNL
1/C2
ISSYNH
2/C13/3
1/D1/5
1/E2
ISSYNL
2/CN3/27
IMSYNH
1/C5/13
SSYNH
1/D6/14
SSYNL
BOSYL
1/CN3/19
1/D2
1/D5/5
1/B6/12
GTBH
1/D5/1
1/C3
$133
INTNTL
NPGL
SACKL
GDH
1/C4
GTBHA 1/C7/1
50 pf
GTBHA 1/D9/12
AD-BUS L
2/D15/1
1/CN2/7
1/D14/4
1/E12/3
1/D14/2
1/E12/2
1/E7/2
1/E2/11
1/B2
UBSYNL
2/CN3/26
1/E12/10
CLRDL
1/E12/7
IBMSYNL
1/E3/10
1/E12/14
1/E5
1/D10
NPR Hold off
NPGL 1/C3/4
1/C3/3 SACKL
220
1N914
3300pf

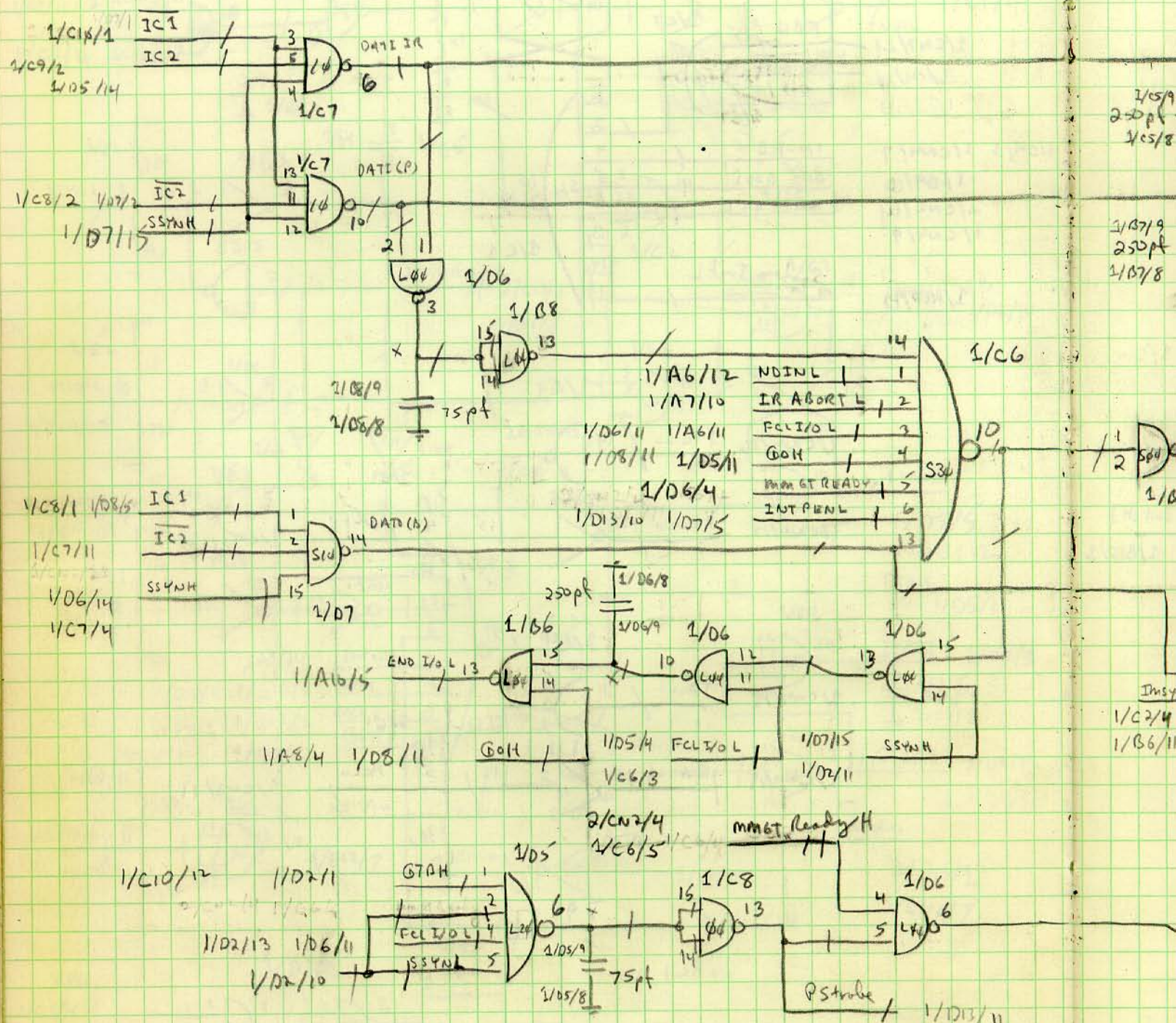


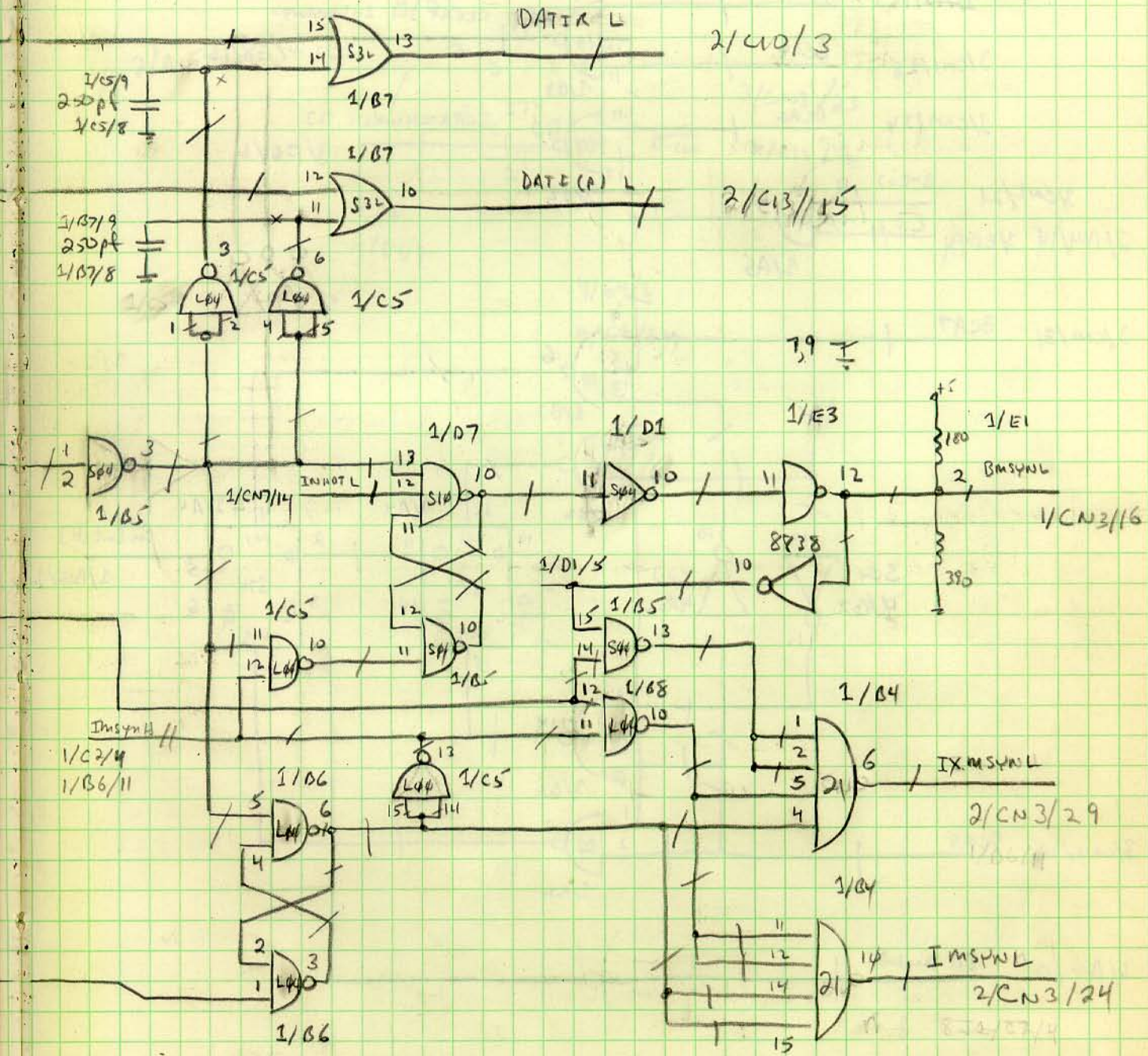




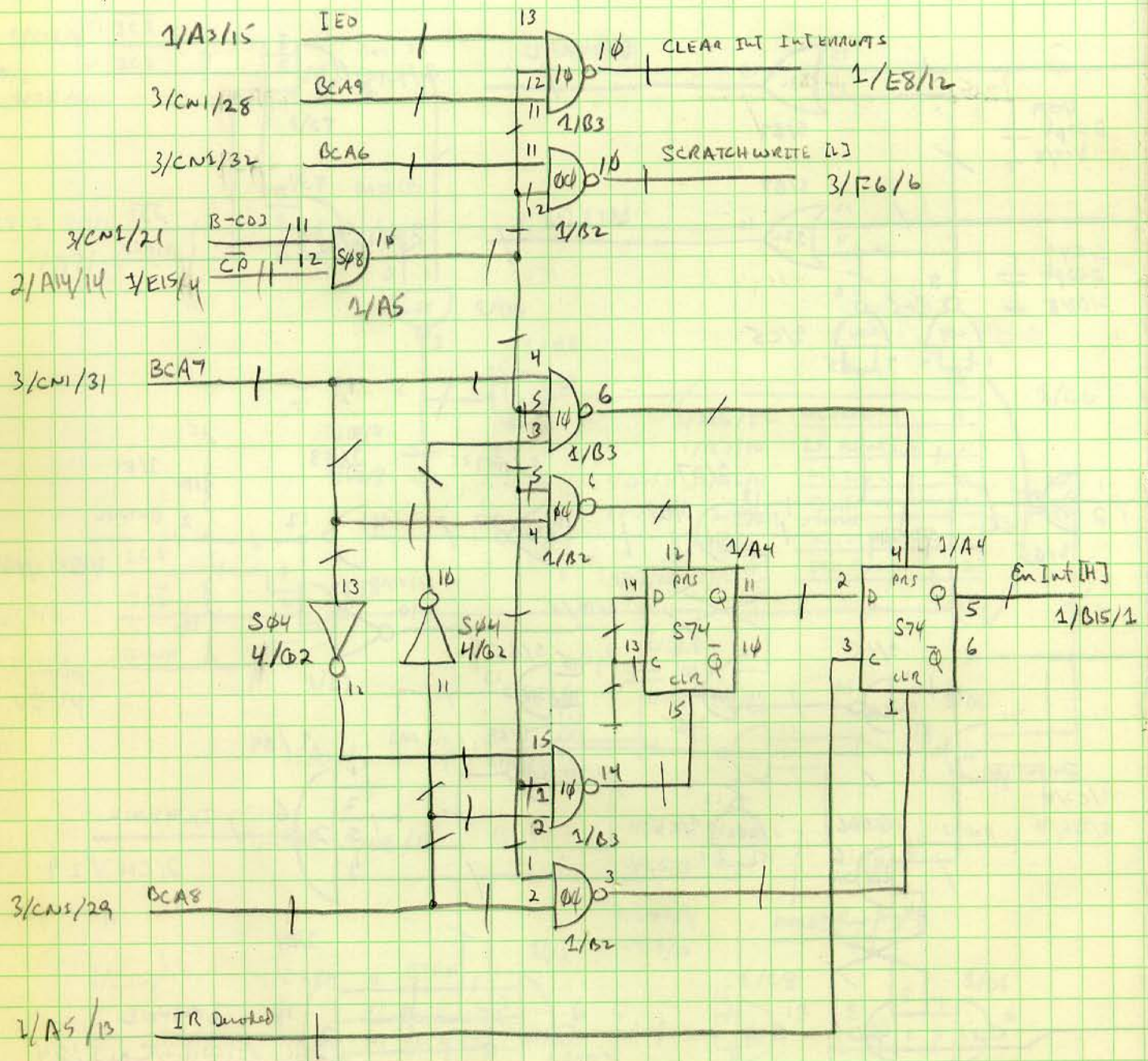
1/E4
7,9

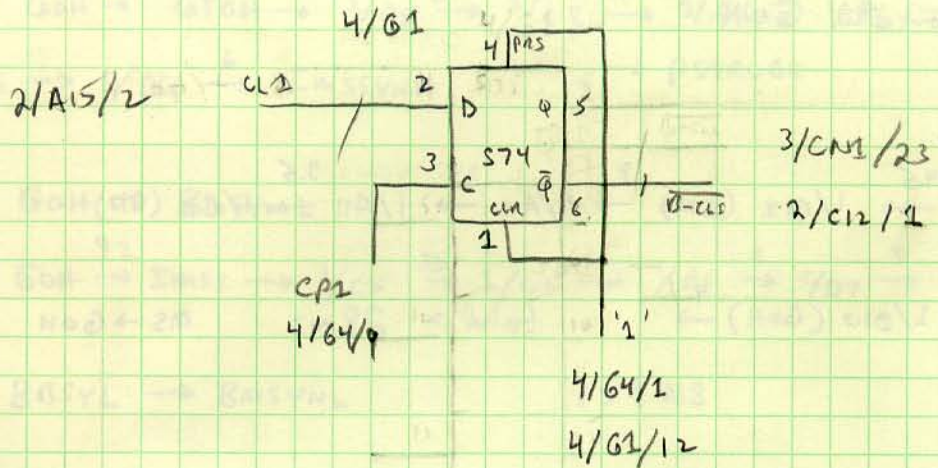
30 Oct 76


1/C10/1
IC1
IC2
1/C9/2
1/D5/14
1/C7
DATI IR
1/C8/2 1/D7/2
SSYNH
1/D7/15
DATI (P)
1/D6
1/B8
1/D8/9
2/D8/8
75pf
1/A6/12
1/A7/10
1/D6/11 1/A6/11
1/D8/11 1/D5/11
1/D6/4
1/D13/10 1/D7/5
NDINL
IR ABORT L
FCLI/O L
GOH
MMGT READY
INTPENL
S34
1/C6
1/C8/1 1/D8/5
1/C7/11
1/D6/14
1/C7/4
DATO (A)
1/D7
250pf
1/D6/8
1/D6/9
1/B6
1/D6
END I/O L
1/A10/5
1/A8/4 1/D8/11
1/D5/4
FCLI/O L
1/D7/15
SSYNH
1/D2/11
1/C6/3
2/CN7/4
1/C6/5
MMGT Ready H
1/D5
1/C10/12
1/D2/11
GTAH
1/C8
1/D2/13 1/D6/11
1/D2/10
1/D5/9
75pf
1/D5/8
PStrobe
1/D13/11


DATIR L
2/C10/3
1/B7
1/C5/9
250pf
1/C5/8
DATI(A) L
2/C13/15
1/B7/9
250pf
1/B7/8
1/C5
7,9
1/E3
1/E1
180
390
BMSYNL
1/CN3/16
1/D7
1/D1
1/B5
IN NOT L
1/CN7/14
8838
1/D1/5
1/B5
1/B4
IMSYN H
1/C2/4
1/B6/11
IXMSYNL
2/CN3/29
1/D6
1/B6
IMSYNL
2/CN3/24

300-471


1/A3/15
IED
3/CN1/28
BCA9
3/CN1/32
BCA6
CLEAR INT INTERRUPTS
1/E8/12
SCRATCH WRITE [L]
3/F6/6
1/B3
1/B2
3/CN1/21
B-COJ
CP
2/A14/14
1/E15/4
S08
1/A5
3/CN1/31
BCA7
1/B3
1/B2
S04
4/G2
S04
4/G2
S74
1/A4
S74
1/A4
En Int [H]
1/B15/1
1/B3
3/CN1/29
BCA8
1/B2
1/A5/13
IR Decoded



16 March 77
ARM

I/O Timing

Microcycle start to GOH

Immediate:

CP → 1/B7 —4.5→ 1/B12 (EN) —8→ 1/A12 —3.5→ 1/A11 —3.5→ 1/B11 (EN)

—8→ 1/B7 —4.5→ 1/B10 (GOH) —4→ total = 28 NS. MS → GOH

Delayed

CP → 1/B10 (GOH) —6→ total = 6 NS CP → GOH

Times from GOH to GTBH (ie GO TO BUS H)

for DATI (P, IR) DATO (A)

assuming BSYNL, ISSYNL, BOSYL, NPGL, SACKL clear

GOH → 1/C3 —3.5→ 1/D2 —3.5→ GTBH 7 NS

→ 1/C4 —31→ GTBHA 38 NS

→ 1/D2 —3.5→ AD-BUS L 10.5 NS

→ 1/C4 —35→ GTBHA 45.5 NS

GOH → BBSYL 16 NS

—7→ GTBH → 1/E3 —9→ BOSYL

GOH → IMSSYNH

GOH → GTBH → 1/D5 $\xrightarrow{31}$ 1/C8 $\xrightarrow{11}$ 1/D6 $\xrightarrow{31}$ 1/B6 $\xrightarrow{3}$ 1/B6 $\xrightarrow{3}$ IMSS

IMSS $\xrightarrow{3}$ 1/B4 $\xrightarrow{6}$ IMSSYNH

GOH → PSTROBE

92 NS

GOH $\xrightarrow{92}$ IMSS → 1/C5 $\xrightarrow{35}$ 1/C5 $\xrightarrow{31}$ 1/B5 $\xrightarrow{3}$ 1/D7 $\xrightarrow{3}$ 1/D1 $\xrightarrow{3}$ 1/E3 $\xrightarrow{9}$ BMSYNL

175 NS

BBSYL → BMSYNL

159 NS

ISSYNL → SSYNH

→ 1/D2 $\xrightarrow{3}$ 1/C2 $\xrightarrow{3}$ 1/C2 $\xrightarrow{3}$ SSYNH

9 NS.

BSYNL → SSYNH

→ 1/E3 $\xrightarrow{26}$ 1/C2 $\xrightarrow{3}$ 1/C2 $\xrightarrow{3}$ SSYNH

26 NS

SSYNH → DATIRL / DATI(P) L

SSYNH → 1/C7 $\xrightarrow{7}$ 1/B7 $\xrightarrow{4.5}$ DATI

11.5 NS

→ 1/C7 $\xrightarrow{7}$ 1/D6 $\xrightarrow{31}$ 1/D8 $\xrightarrow{7}$ 1/C6 $\xrightarrow{3}$ 1/B5 $\xrightarrow{3}$ 1/C5 $\xrightarrow{35}$ 1/B7 $\xrightarrow{4.5}$ DATI

90.5

90.5

Load pulse = 90.5 - 11.5 = 79 NS

SSYNH → END I/O L

→ 1/C7 $\xrightarrow{7}$ 1/D6 $\xrightarrow{31}$ 1/D8 $\xrightarrow{7}$ 1/C6 $\xrightarrow{3}$ 1/D6 $\xrightarrow{31}$ 1/D6 $\xrightarrow{35}$ 1/B6 $\xrightarrow{3}$ END I/O L

SSYNH ↗ FCLI/O L ↗ GOH ↗

117 NS.

END I/O L → IRBUSY 25 NS

→ 1/A10 $\xrightarrow{3}$ 1/A11 $\xrightarrow{3}$ 1/B10 $\xrightarrow{7}$ 1/B6 $\xrightarrow{3}$ 1/A10 $\xrightarrow{3}$ 1/A11 $\xrightarrow{3}$ 1/A12 $\xrightarrow{3}$ IRBUSY

END I/O L → BBSYL 36 NS

→ 1/A10 $\xrightarrow{3}$ 1/A11 $\xrightarrow{3}$ 1/B10 $\xrightarrow{7}$ 1/C3 $\xrightarrow{3}$ 1/D2 $\xrightarrow{3}$ 1/E3 $\xrightarrow{17}$ BBSYL

SSYNH → BMSYNL (DATI) 73 NS

→ 1/C7 $\xrightarrow{3}$ 1/D6 $\xrightarrow{31}$ 1/B8 $\xrightarrow{7}$ 1/C6 $\xrightarrow{3}$ 1/B5 $\xrightarrow{3}$ 1/D7 $\xrightarrow{3}$ 1/D8 $\xrightarrow{3}$ 1/E3 $\xrightarrow{20}$ Asynch

SSYNH → BBSYL 153 NS

BBSYL − BMSYNL = 80 NS

SSYNH → IMSYNL (DATI) 96 NS

→ 1/C7 $\xrightarrow{3}$ 1/D6 $\xrightarrow{31}$ 1/B8 $\xrightarrow{7}$ 1/C6 $\xrightarrow{3}$ 1/B5 $\xrightarrow{3}$ 1/B6 $\xrightarrow{3}$ 1/C5

$\xrightarrow{31}$ 1/B8 $\xrightarrow{11}$ 1/B4 $\xrightarrow{4}$ IMSYNL

DATO (D)

SSYNH → ENDIOL 75NS

→ 1/D7 —3→ 1/C6 —3→ 1/D6 —31→ 1/D6 —35→ 1/B6 —3→ ENDIOL

SSYNH → IMSSYNH 18NS.

→ 1/D7 —3→ 1/C6 —3→ 1/B5 —3→ 1/B6 —3→ 1/D4 —4→ IMSYNH
1/D7 —3→ 1/B8 —11→ 1/B6

SSYNH → BMSSYNH 35NS

→ 1/D7 —3→ 1/C6 —3→ 1/B5 —3→ 1/D7 —3→ 1/D1 —3→ 1/E3 —2φ→ BMSSYNH

INOV 1976
ARB

Component Location Index CPU Board

Board # 1 Layout pg 64

	Circuit	Logic or Pages	Description
1/A1	S32	62	
1/A2	S86	62	
1/A3	151	62	
1/A4	S74	76	
1/A5	Sø8	41, 72, 73, 76	
1/A6	S2ø	73	
1/A7	S64	73	
1/A8	3ø	72	
1/A9	2ø	73	
1/A10	S3ø	72	
1/A11	Søø	72	
1/A12	S1ø	72	
1/A13	S11	68	
1/A14	S74	68, 73	
1/A15	Søø	73	

Board # 1

	Circuit	Logic on Pages	Description
1/B1	S00	62, 72, 73	
1/B2	00	74, 76	
1/B3	10	76	
1/B4	21	75	
1/B5	S00	72, 75	
1/B6	L00	74, 75	
1/B7	S32	72, 75	
1/B8	L00	72, 75	
1/B9	S74	73	
1/B10	S74	72	
1/B11	S175	72	
1/B12	S175	72	
1/B13	S11	68	
1/B14	S00	68, 73	
1/B15	S175	68	

Board #1

	Circuit	Logic on Page	Description
1/C1	S3ϕ	74	
1/C2	S1ϕ	74	
1/C3	S3ϕ	74	
1/C4	Lϕϕϕϕϕϕϕϕϕϕϕϕϕϕϕϕ	68, 73, 74	
1/C5	Lϕϕϕϕϕϕϕϕϕϕϕϕϕϕϕϕ	75	
1/C6	S3ϕ	75	
1/C7	1ϕ	75	
1/C8	ϕϕ	73, 75	
1/C9	Sϕ8	68, 73	
1/C10	Sϕϕ	73	
1/C11	S175	72	
1/C12	S175	72	
1/C13	S1ϕ	68	
1/C14	Sϕϕ	68	
1/C15	S175	68	

Board # 1

	Circuit	Logic on Pass	Description
1/D1	S04	74	
1/D2	S04	74	
1/D3	Resistors		
1/D4	122	73	
1/D5	L20	73, 75	
1/D6	L04	75	
1/D7	S10	73, 75	
1/D8	10	72, 73	
1/D9	20	73	
1/D10	S00	72	
1/D11	S175	72	
1/D12	S175	72	
1/D13	S20	68	
1/D14	S04	68	
1/D15	174	68	

Board # 1

	Circuit	Logic on Page	Description
1/E1	Resistors	74, 75	
1/E2	Resistors	66, 67, 68	
1/E3	8838	73, 74, 75	
1/E4	8838	73, 74	
1/E5	Resistors	74	
1/E6	8837	66, 67, 68	
1/E7	8837	68, 74	
1/E8	42	68	
1/E9	148	68	
1/E10	Resistors	66, 67	
1/E11	33	67	
1/E12	S133	67	
1/E13	S10	67	
1/E14	S00	67	
1/E15	S40	67, 72	

Board #1

	Circuit	Logic on Page	Description
1/F10	Resistors	66	
1/F11	38	66, 67, 74	
1/F12	S20	66	
1/F13	S20	66, 42	
1/F14	00	66, 67	
1/F15	L00	66, 67	

Component Location Index CPU Board

Board #2 Layout pg 36

	Circuit	Logic on Page	Description
2/A1	S258	45	
2/A2	S258	45	
2/A3	S258	45	
2/A4	S258	45	
2/A5	S175	37, 38	
2/A6	S175	39, 40	
2/A7	S175	37, 38	
2/A8	S175	39, 40	
2/A9	175	44	
2/A10	175	44	
2/A11	175	44	
2/A12	175	43	
2/A13	Delay Line	42	
2/A14	S04	42	
2/A15	S74	42	

Board V2

	Circuit	Logicon Page	Description
2/B1	157	37, 38	
2/B2	157	37, 38	
2/B3	157	37, 38	
2/B4	157	37, 38	
2/B5	157	39, 40	
2/B6	157	39, 40	
2/B7	157	39, 40	
2/B8	157	39, 40	
2/B9	175	43	
2/B10	175	43	
2/B11	157	43	
2/B12	157	43	
2/B13	Delay Line	42	
2/B14	S37	42	
2/B15	S08	41, 42	

Board

2/C1
2/C2
2/C3
2/C4
2/C5
2/C6
2/C7
2/C8
2/C9
2/C1
2/C1
2/C1
2/C
2/C

Board # 2

	Circuit	Logic on Pages	Description
2/C1	157	37	
2/C2	157	37	
2/C3	157	38	
2/C4	157	38	
2/C5	157	39	
2/C6	157	39	
2/C7	157	40	
2/C8	157	40	
2/C9	S11	41, 43	
2/C10	S74	41	
2/C11	S00	41, 42	
2/C12	S08	41	
2/C13	S11	41	
2/C14	S37	42	
2/C15	S32	42, 73	

Board #2

	Circuit	Logicon Pages	Description
2/01	157	37	
2/02	157	37	
2/03	157	38	
2/04	157	38	
2/05	157	39	
2/06	157	39	
2/07	157	40	
2/08	157	40	
2/09	8838	44	
2/010	157	44	
2/011	157	44	
2/012	157	44	
2/013	157	43	
2/014	157	43	
2/015	157	43	

Board #2

	Circuit	Logic on Pages	Description
2/E1	Resistors	37, 38, 39	
2/E2	8838	37	
2/E3	8838	38	
2/E4	8838	39	
2/E5	8838	40	
2/E6	Resistors	40, 44	
2/E7	8838	44	
2/E8	8838	44	
2/E9	Resistors	43, 44	
2/E10	8838	43	
2/E11	8838	43	

Logic Component Index CPU Board

Board # 3 Layout pg 20

	Circuit	Logic on Pages	Description
3/A1	150	30	
3/A2	175	30	
3/A3	Φ8	25	
3/A4	SΦ8	23	
3/A5	S175	25, 27	
3/A6	151	25	
3/A7	151	25	
3/A8	151	25	
3/A9	151	25	
3/A10	151	25	
3/A11	151	25	
3/A12	151	25	
3/A13	151	25	
3/A14	151	25	
3/A15	151	25	

Board #3

	Circuit	Logicon Page	Description
3/B1	— No designation		
3/B2	175	30	
3/B3	S151	23	
3/B4	S153	23	
3/B5	S08	23	
3/B6	Resistors	23, 25, 32, 43	
3/B7	S153	23	
3/B8	S153	23	
3/B9	157	27	
3/B10	S151	27	
3/B11	S151	27	
3/B12	125	27	
3/B13	125	27	
3/B14	125	27	
3/B15	175	27	

Board # 3

	Circuit	Logic on Pages	Description
3/C1	150	30	
3/C2	S86	23, 29	
3/C3	— — —		
3/C4	Am2901	21, 22, 28	
3/C5	Am2901	21, 22, 28	
3/C6	Am2901	21, 22, 28	
3/C7	Am2901	21, 22, 28	
3/C8	— — —		
3/C9	— — —		
3/C10	Am2901	21, 22, 28	
3/C11	Am2901	21, 22, 28	
3/C12	Am2901	21, 22, 28	
3/C13	Am2901	21, 22, 28	
3/C14	— — —		
3/C15	S05	32	

Board # 3

	Circuit	Logic on Page	Description
3/D1	150	30	
3/D2	175	23	
3/D15	505	32	

Board # 3

	Circuit	Logic on Page	Description
3/E1	— ——		
3/E2	175	30	
3/E3	151	29	
3/E4	Ø8	26	
3/E5	ØØ	26	
3/E6	Ø8	26	
3/E7	S182	28	
3/E8	S157	28	
3/E9	S182	28	
3/E10	S182	28	
3/E11	51	31	
3/E12	SØ2	31	
3/E13	S1Ø	31	
3/E14	153	29	
3/E15	not used		

Board # 3

	Circuit	Logic on Page	Description
3/F1	150	30	
3/F2	175	30	
3/F3	175	29	
3/F4	175	26, 27	
3/F5	175	32	
3/F6	S175	32	
3/F7	153	31	
3/F8	153	31	
3/F9	153	31	
3/F10	153	31	
3/F11	S175	32	
3/F12	S21	31	
3/F13	S32	31	
3/F14	S175	29	
3/F15	175	29	

Logic Component Index CPU Panel

Board # 4 Layout - pg 50

	Circuit	Logic on Pages	Description
4/A1	S74	58	
4/A2	Sφ4	58	
4/A3	83A	58	
4/A4	S175	58	
4/A5	157	58	
4/A6	S172	56	
4/A7	S172	56	
4/A8	150	54	
4/A9	150	54	
4/A10	150	54	
4/A11	150	54	

Board #4

	Circuit	Logic on Pages	Description
4/B1	S11	58	
4/B2	S04	57, 58	
4/B3	83A	58	
4/B4	S175	58	
4/B5	157	58	
4/B6	S172	56	
4/B7	S172	56	
4/B8	150	54	
4/B9	150	54	
4/B10	150	54	
4/B11	150	54	

Board #4

	Circuit	Logic on Pages	- Description
4/C1	S08	59, 60	
4/C2	175	60	
4/C3	S257	60	
4/C4	175	60	
4/C5	157	60	
4/D1	08	59, 60	
4/D2	175	60	
4/D3	S257	60	
4/D4	175	60	
4/D5	157	60	

Board 44

	Circuit	Logic on Pages	Description
4/E1	Ø8	55	
4/E2	ØØ	55	
4/E3	S257	59	
4/E4	175	59	
4/E5	157	59	
4/E6	S172	56	
4/E7	S172	56	
4/E8	150	53	
4/E9	150	53	
4/E10	150	53	
4/E11	150	53	

Board 4

	Circuit	Logic on Pages	Description
4/F1	Ø8	45, 55	
4/F2	S32	33	
4/F3	S257	59	
4/F4	S175	59	
4/F5	S157	59	
4/F6	S172	56	
4/F7	S172	56	
4/F8	150	53	
4/F9	150	53	
4/F10	150	53	
4/F11	150	53	

Board #4

	Circuit	Logic an Pres	Description
4/G1	S74	59, 76	
4/G2	S04	59	
4/G3	S138	51	
4/G4	175	51	
4/G5	S175	55	
4/G6	150	62	
4/G7	S133	58	
4/G8	S133	58	
4/G9	S133	58	
4/G10	S04	57	
4/G11	S04	57	
4/G12	S32	59	
4/G13	42	51	
4/G14	42	51	
4/G15	42	51	