Hardware Systems Manual

Alan R. Baldwin

96 SHEETS • 5 x 5 QUAD
10⅛ x 7⅞ • 53-110

NATIONAL

NATIONAL BLANK BOOK COMPANY, INC.
Holyoke, Massachusetts 01040•Made in USA

ARB Computer

Hardware Systems Manual

Index

Processor Registers

PROCESSOR STATUS WORD 17777776 $(177776)_8$

MODE				group select				Priority			Trace	Status			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
											T	N	Z	V	C
CM		PM													

Bits

15-14	Current mode of memory management (See MMGT)
13-12	Previous mode of memory management (See MMGT)
11-8	Memory management group select Bits (See MMGT)
7-5	Processor priority level (Hardware levels 4-7 implemented)
4	Trace bit
3-0	Processor status bits N - sign Z - zero V - arithmetic overflow C - carry flag

21 Dec 80
AOD

Notes on PSR operation (Hardware & Microcoding)

PSR Bits		USER RTI/RTT	Kernel RTI/RTT
<03:00>	Condition Codes	from stack	from stack
<04>	Trace Bit	from stack	from stack
<07:05>	Priority level	No change	from stack
<09:08>	Previous MMGT	No change	from stack (M) from <11:10> (H)
<11:10>	current MMGT	No change	from stack
<13:12>	Previous Mode	No change	from stack (M) from <15:14> (H)
<15:14>	Current Mode	No change	from stack

* changed by Kernel or User Access if PSR is Mapped.

USER/KERNEL TRAPS & Interrupts	Explicit Address
from Vector	*
from Vector	no change
from Vector	*
copied from <11:10>	*
from Vector	*
copied from <15:14>	*
from Vector	*

22 Dec 80
ARO

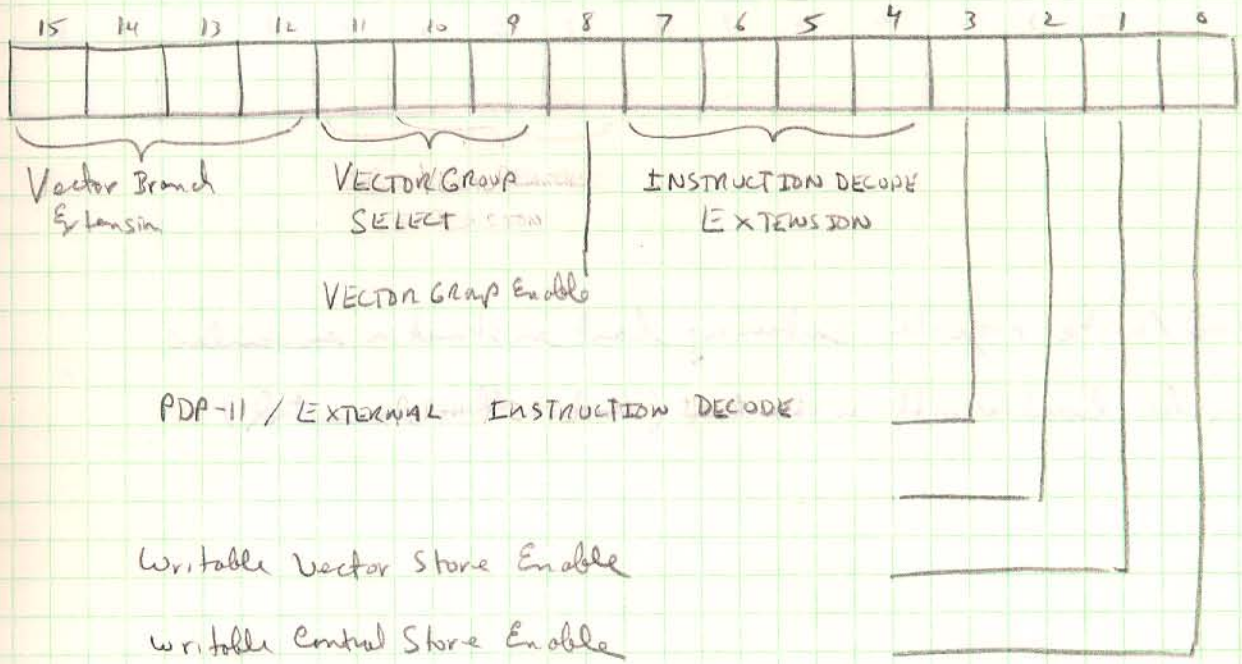
Stack Limit Register 17777774 $(177774)_8$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								X	X	X	X	X	X	X	X

Modulo 256 limit value

The normal stack limit is 377_8. The stack limit register allows the limit to be increased in steps of 400_8 in the Kernel mode.

Processor Control Register 17777772 $(177772)_8$



Vector Branch Extension – 4 Bit extension of internal Vector Address

Instruction Decode Extension – 4 Bit extension Address for Instruction Decoder

Vector Group – 1 PROM, 8 RAM Vector Groups for internal Vector levels

17 Jan 81
ARD

INSTRUCTION REGISTER 17777770 $(177770)_8$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ø

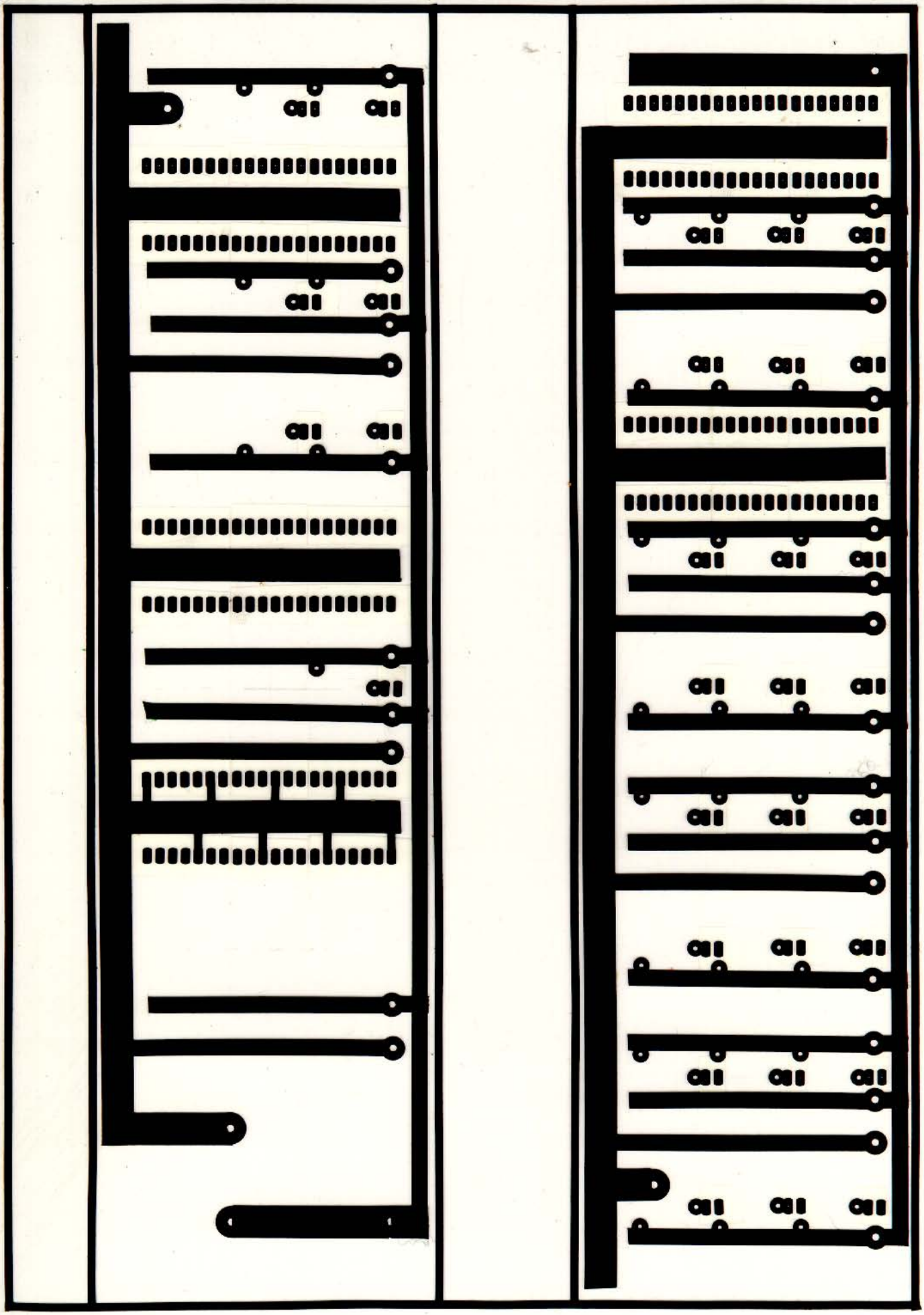
Read/write register containing last instruction executed - may be loaded with instruction (which is then executed)

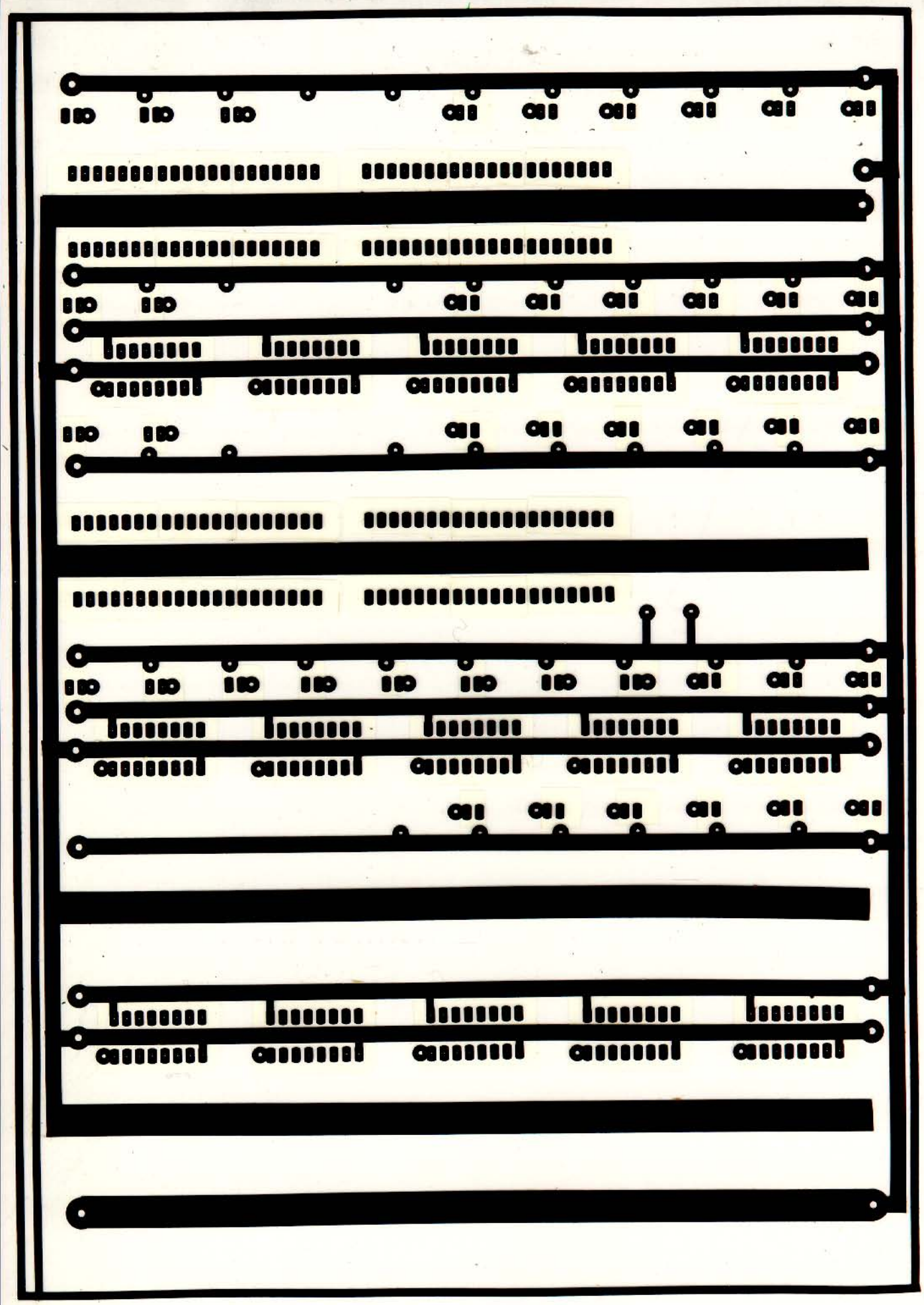
ARB System I/O & Vectors

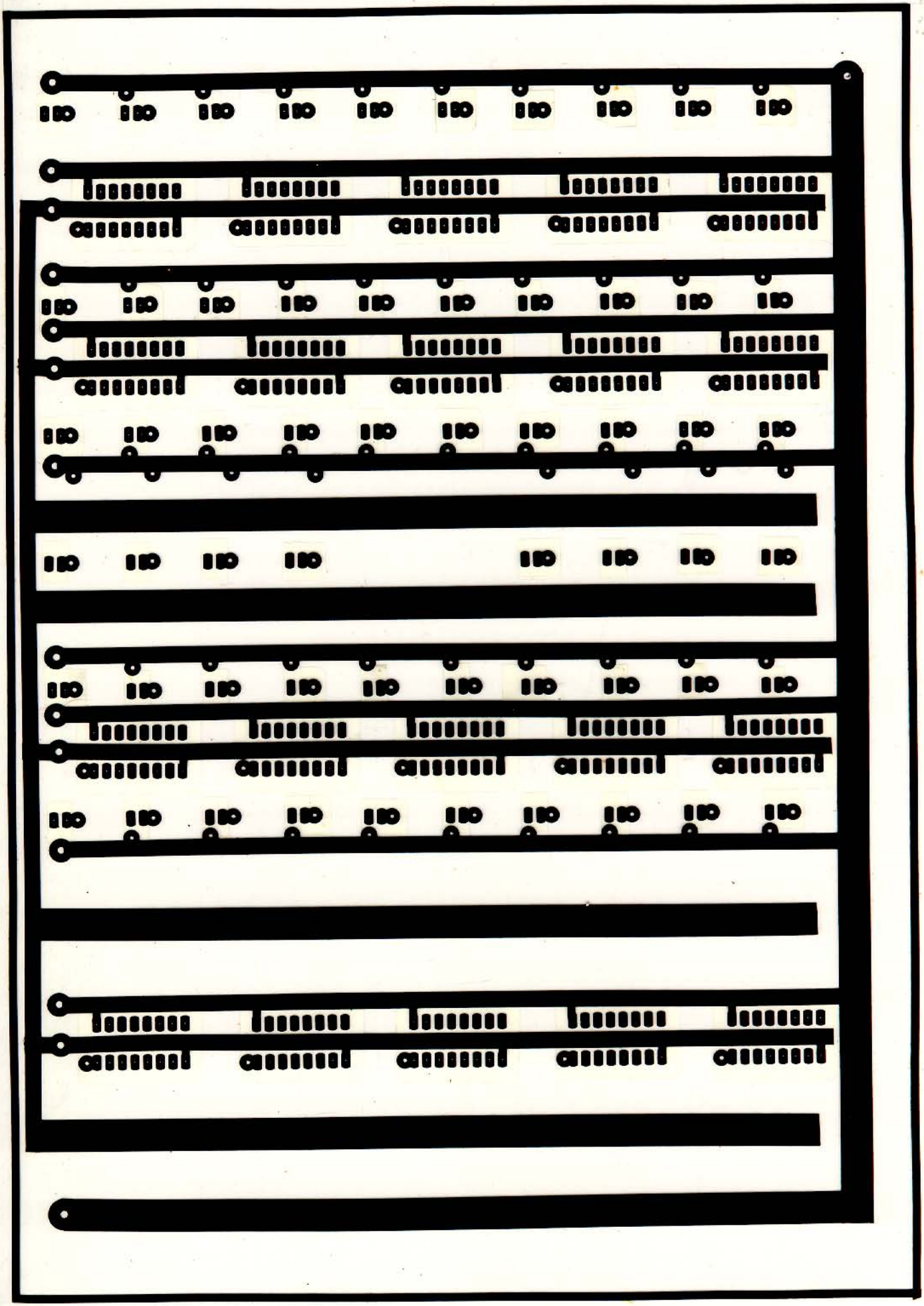
	Address	Vector	Interrupt
RX01	177170-2	264	
Cassette (TA11)	177500-6	260	
Keyboard	177560-2	60	level 6
Printer	177564-6	64	lev 5
Clock	177546	100	level 7
Floating Point Error	———	244	
MMGT	status ~~177572-6~~ ~~172200-172376~~	250	
Console switches	177570	———	
~~PSW Processor STATUS WORD~~	~~177776~~	———	
~~Stack limit Register~~	~~177774~~	———	
~~Processor Control Register~~	~~177772~~	———	
~~Destination Register~~	~~177770~~	———	
CPU Registers	177700-737	———	
Floating Point RAM	256 words Scratch- 77 67000-777 000-103 used by FPP	———	
MICRO TRAP Register ~~Microcode option word~~	777760	———	
SYSTEM SIZE WORD	777764	———	
Permanent MICROCODE	740000-777777	———	
Permanent ~~Arb~~ Internal VECTORS	177200-277	———	
Writable Microcode	760000-773777	———	
Writable ~~Arb~~ Internal Vectors	166000-166777	———	
GRAPHICS ~~Print~~ Keyboard	176670-2	170	level 4
GRAPHICS Printer	176674-6	174	lev 3

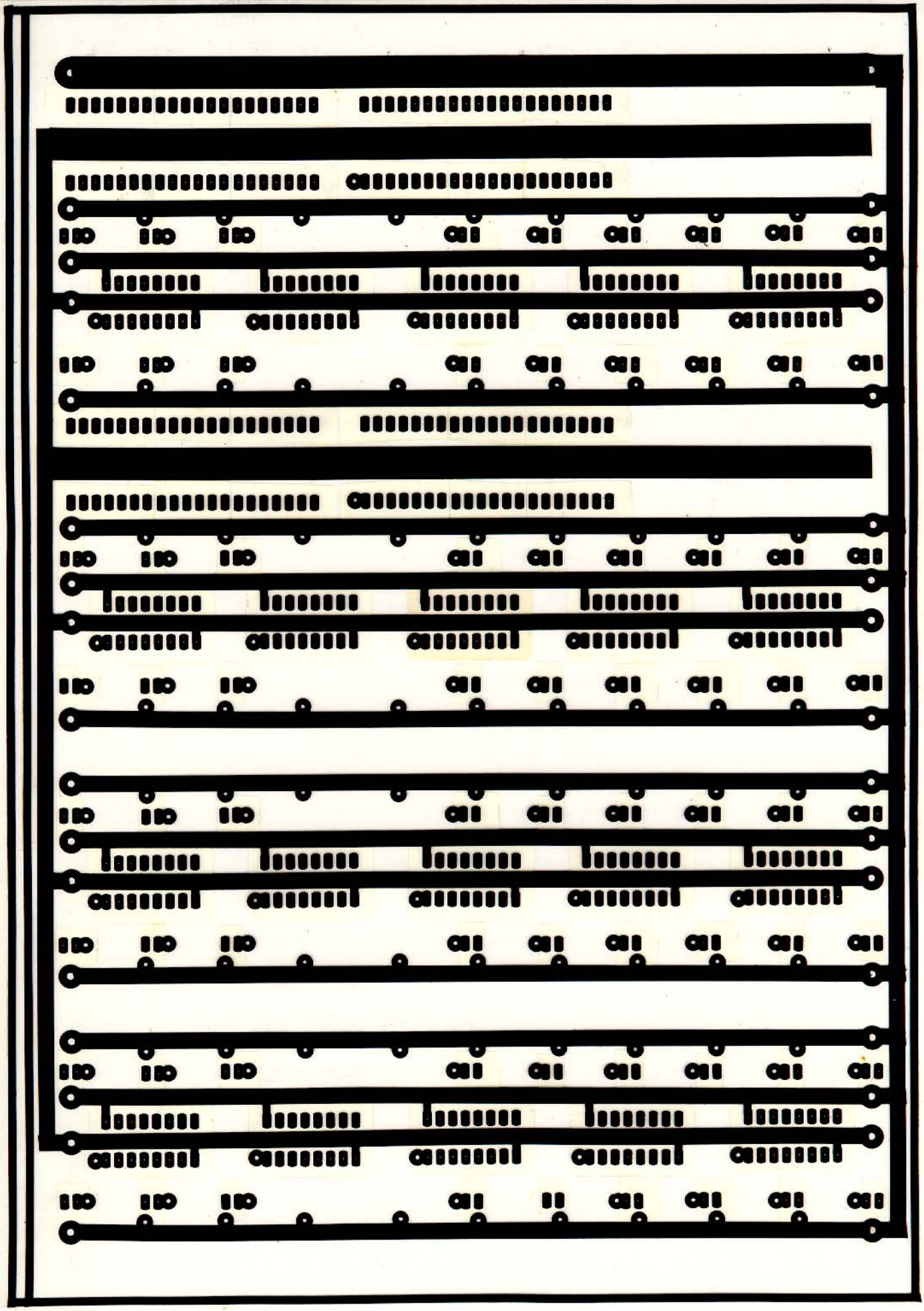
others assigned by Hardware

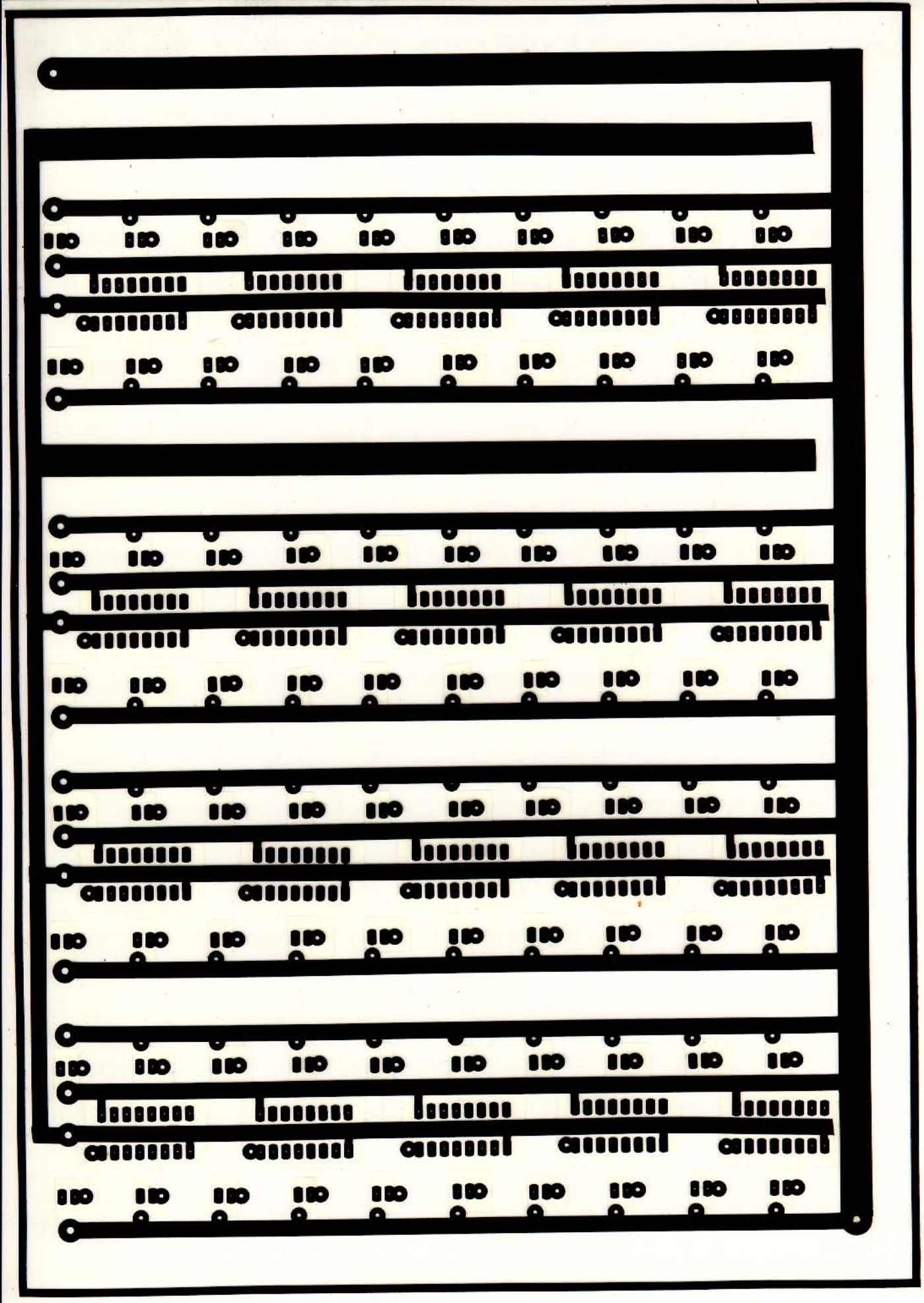
	Address	Vector	interrupt
FD-11P	177160	230	
Prom Programer	177110-117	—	
~~BUS~~ secondary BUS Logic	177100-104	—	
	177700-200		
UNIBUS MAP	770200-367		
		~~170~~	
		~~174~~	
~~Reserved~~		270	level 6
Reserved		274	level 1
Reserved		240	level 0

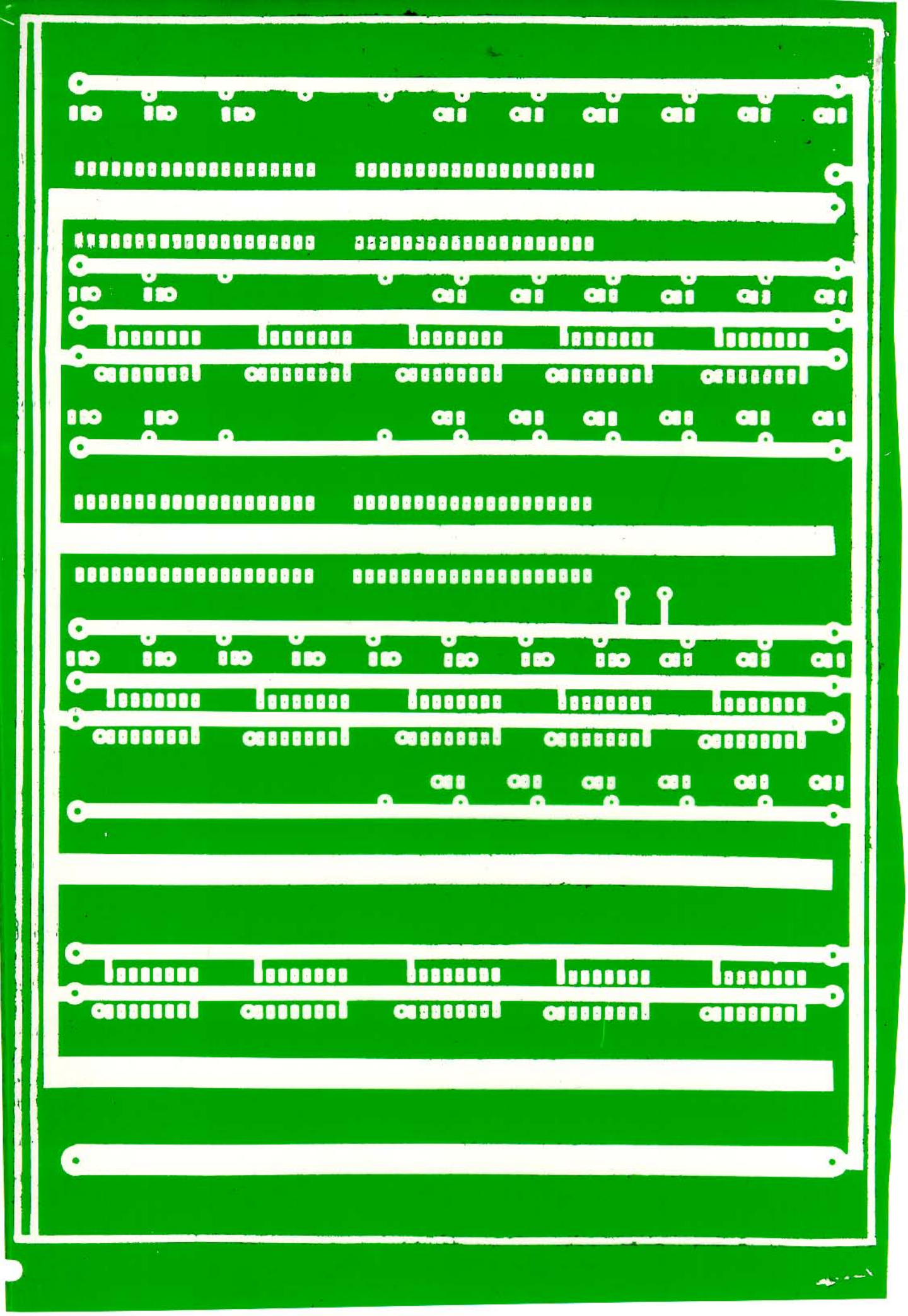


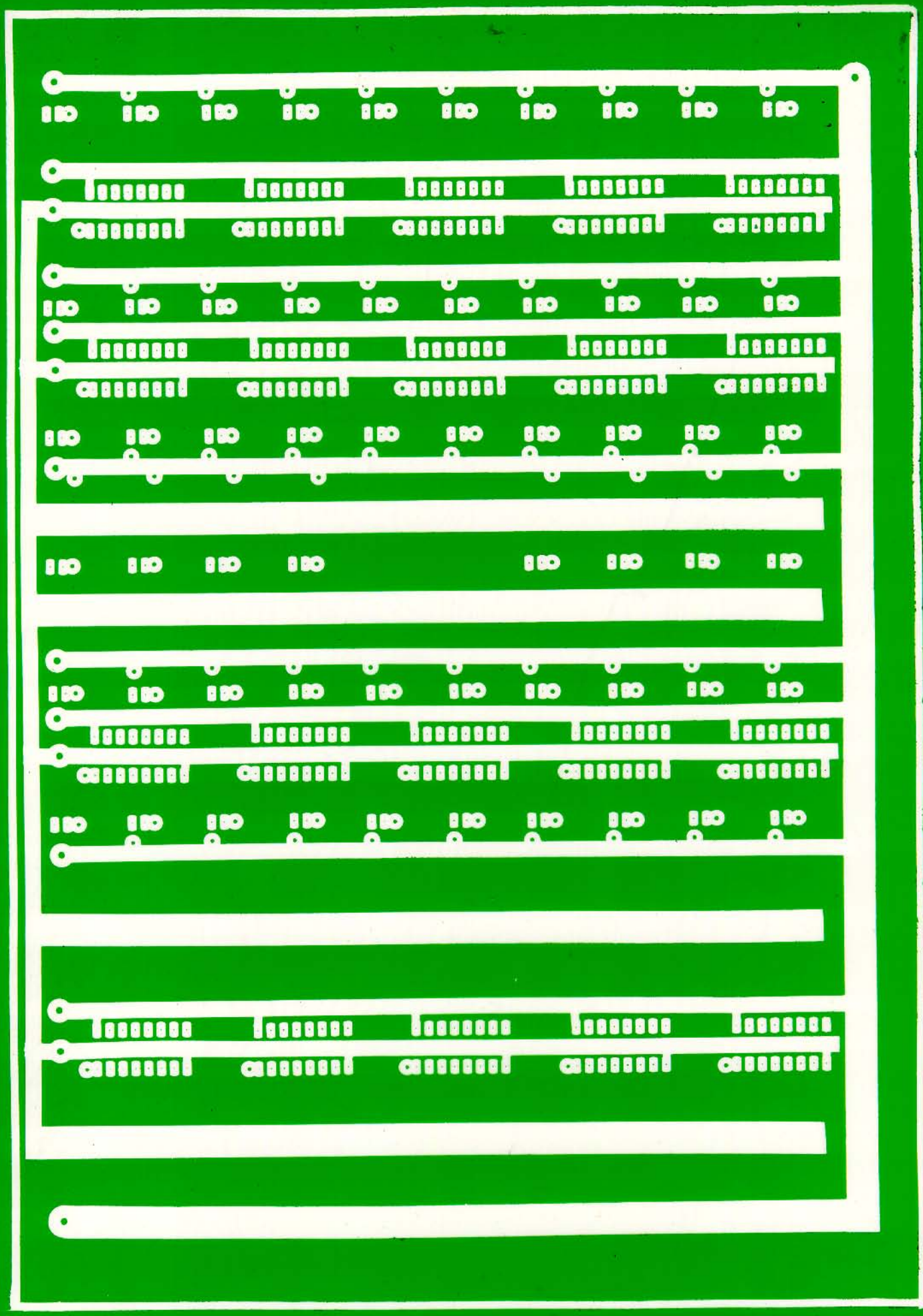


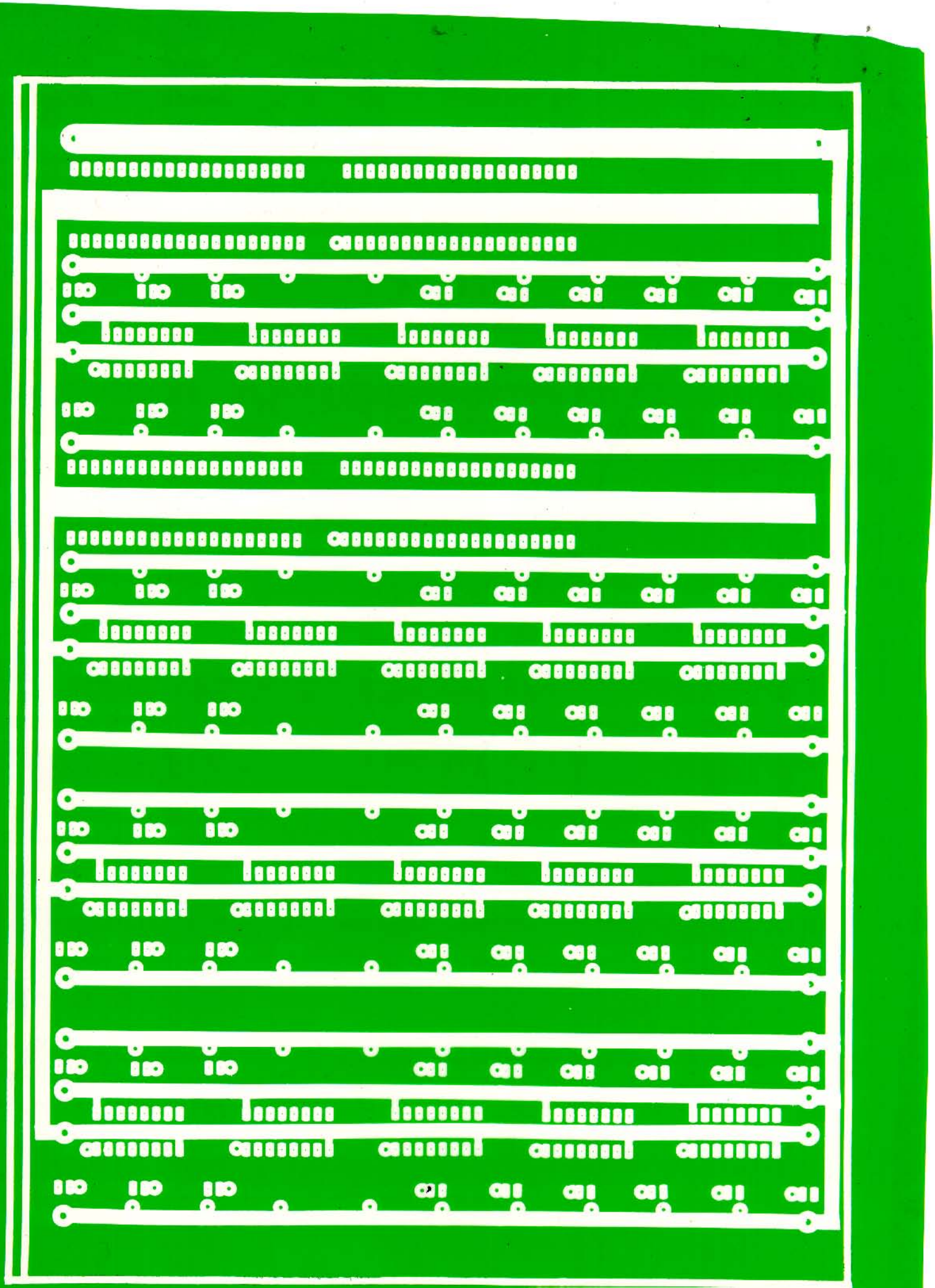


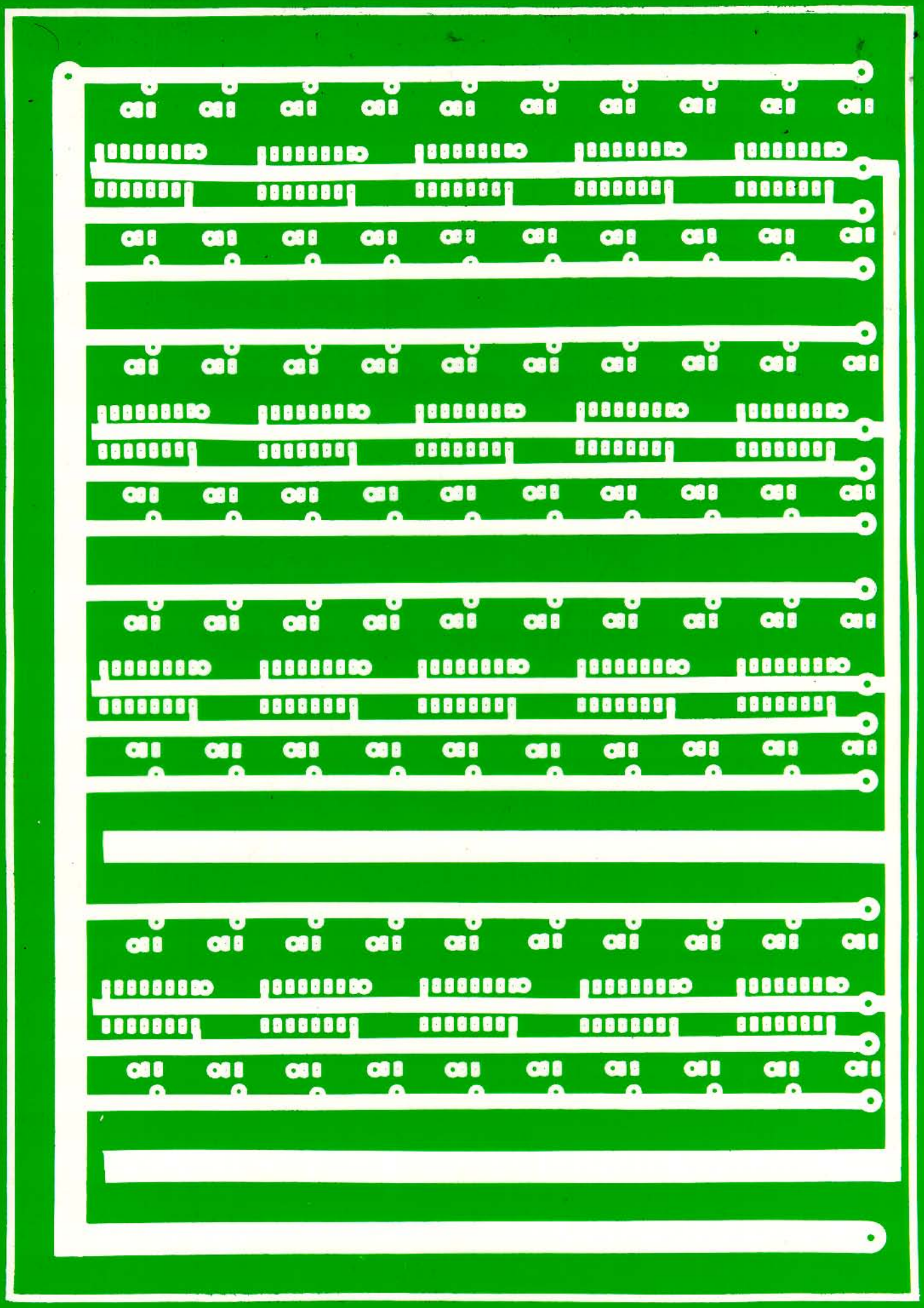


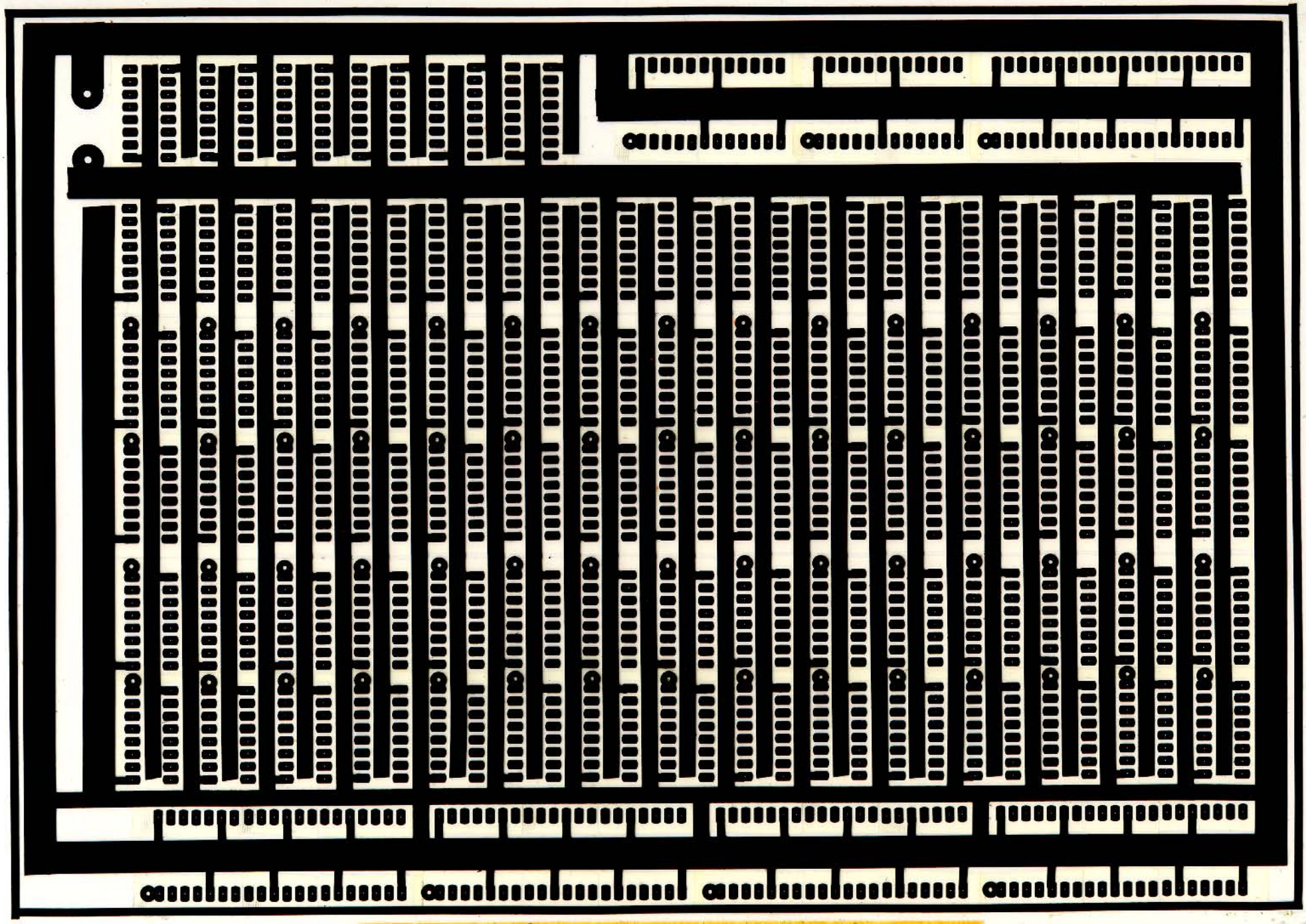






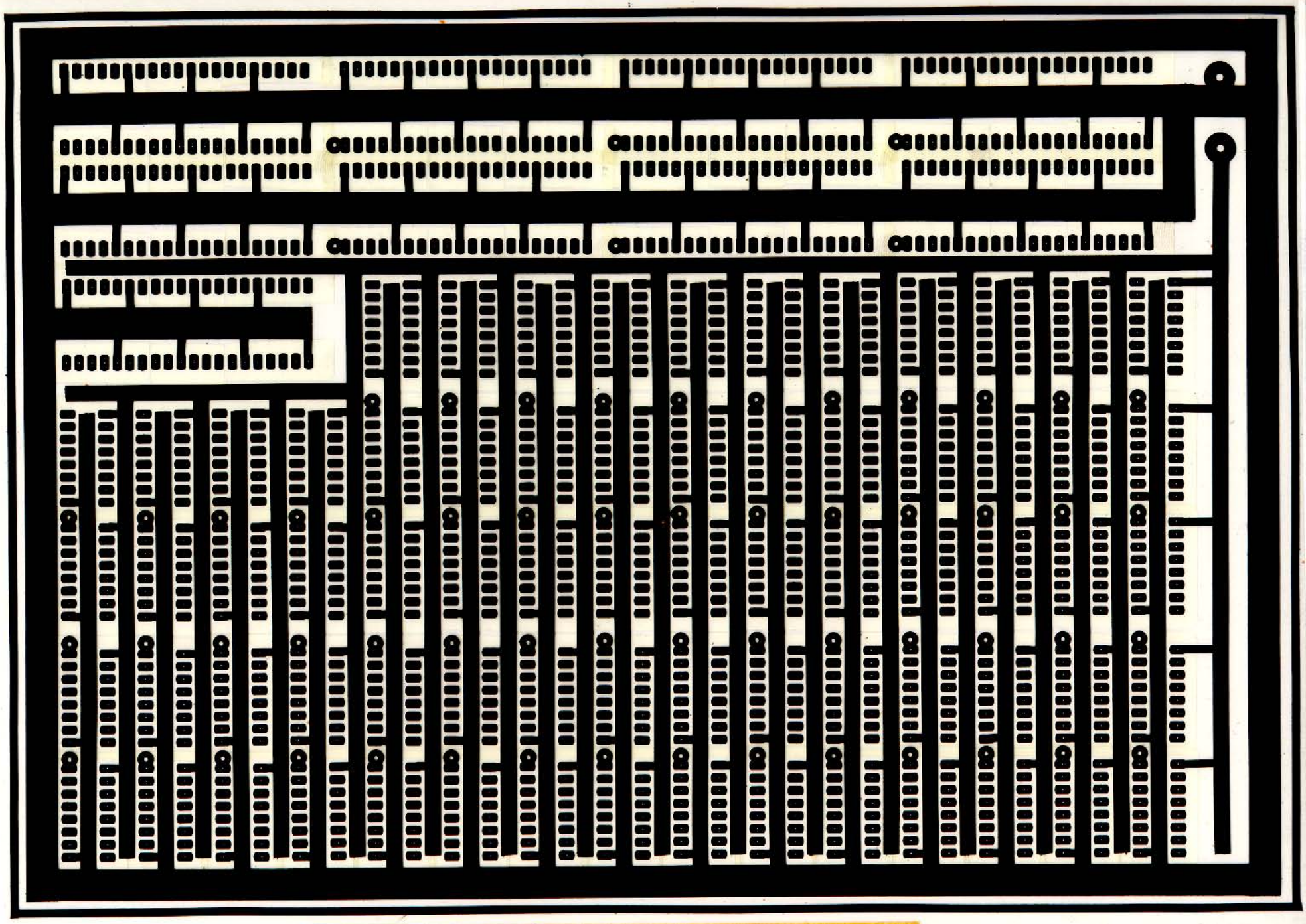




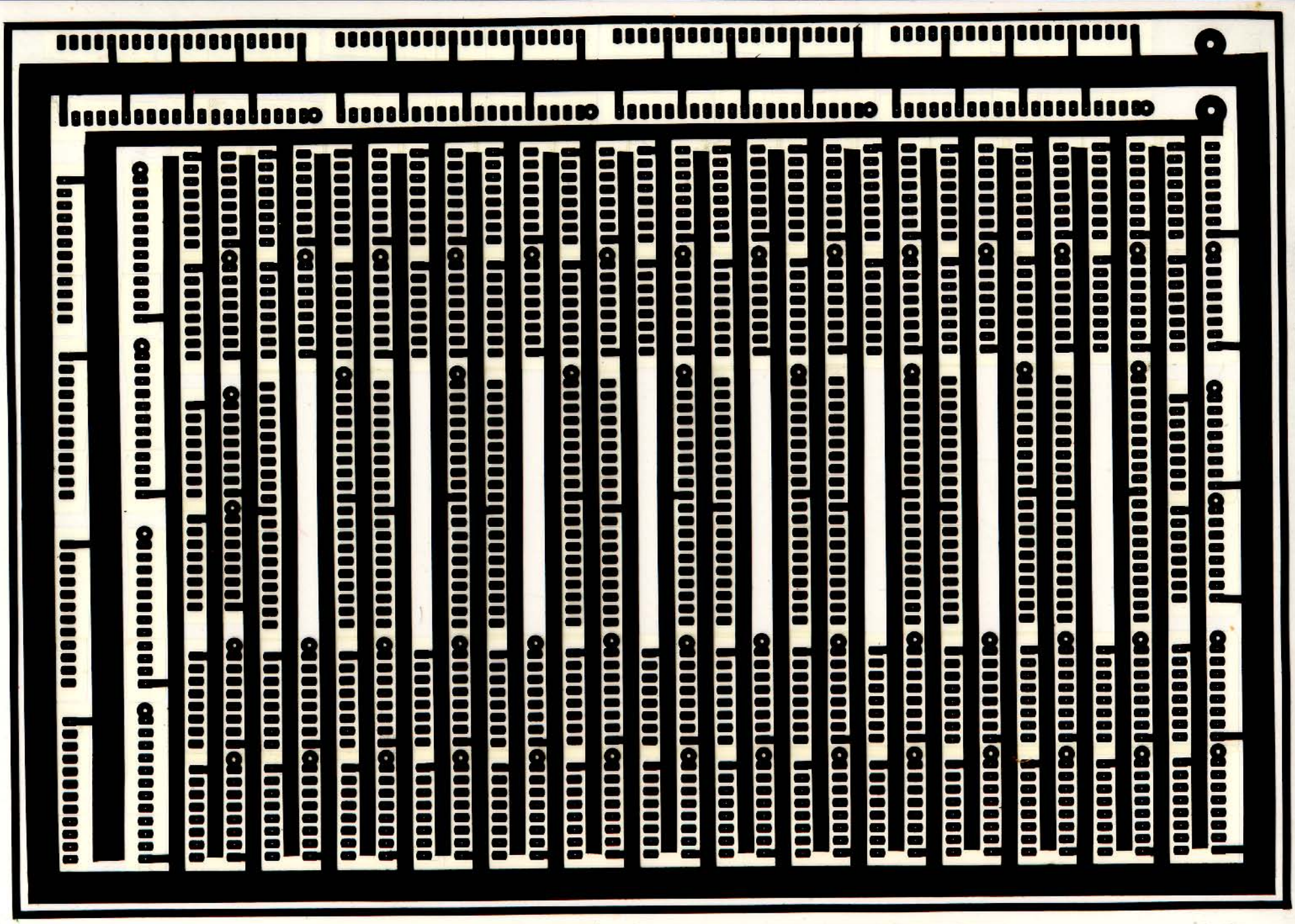


I/O Control BUS Request Logic / CP Clock
Top & Bottom
Prototype

20 June 70
(1880)

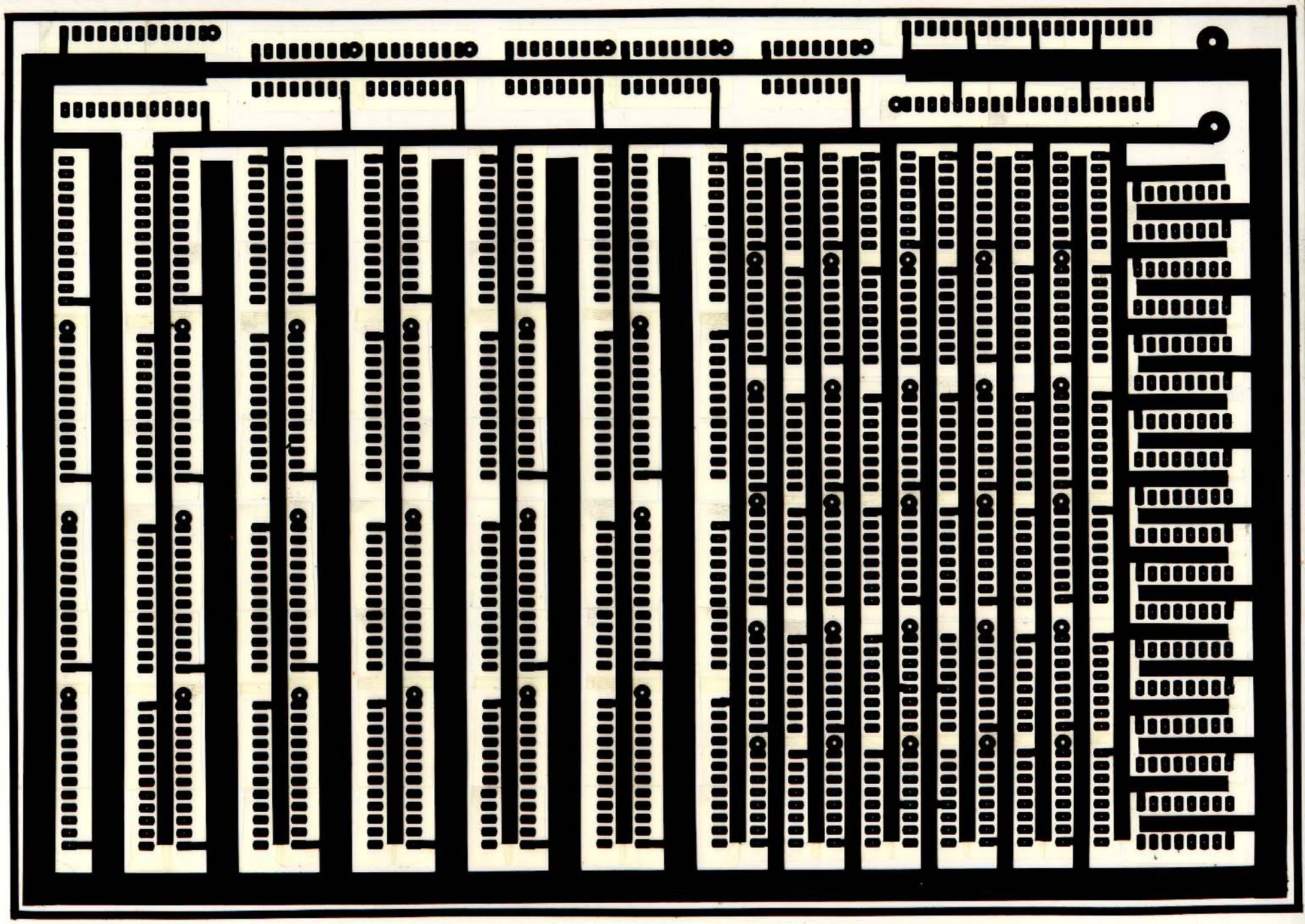


BUS Interface / AD, ADx, D, I Registers
MMOT Port
Top of Bottom
Positive
20 Jun 76
ABD



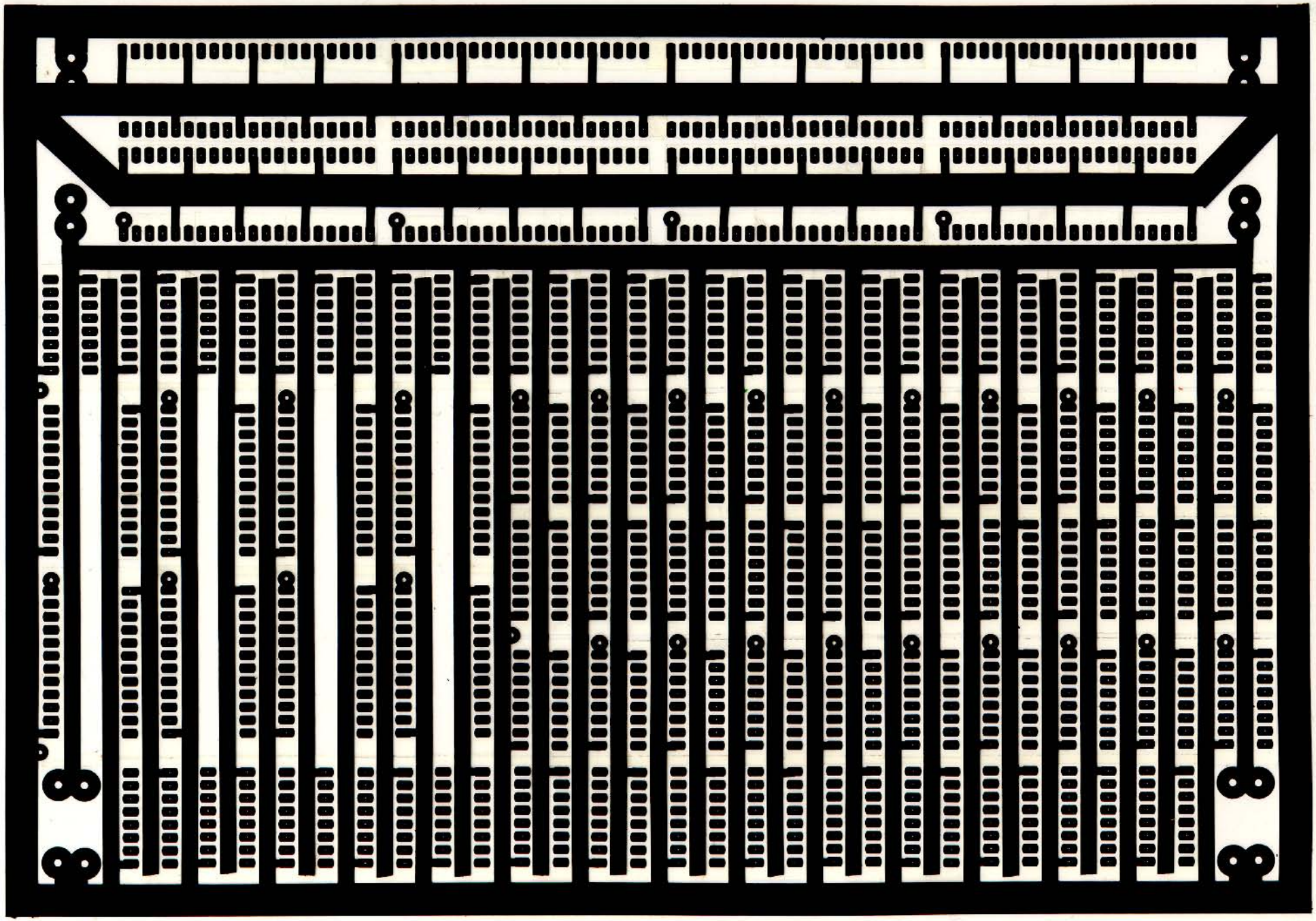
32 Bit CPU Board
Bottom of Bottom
Positive

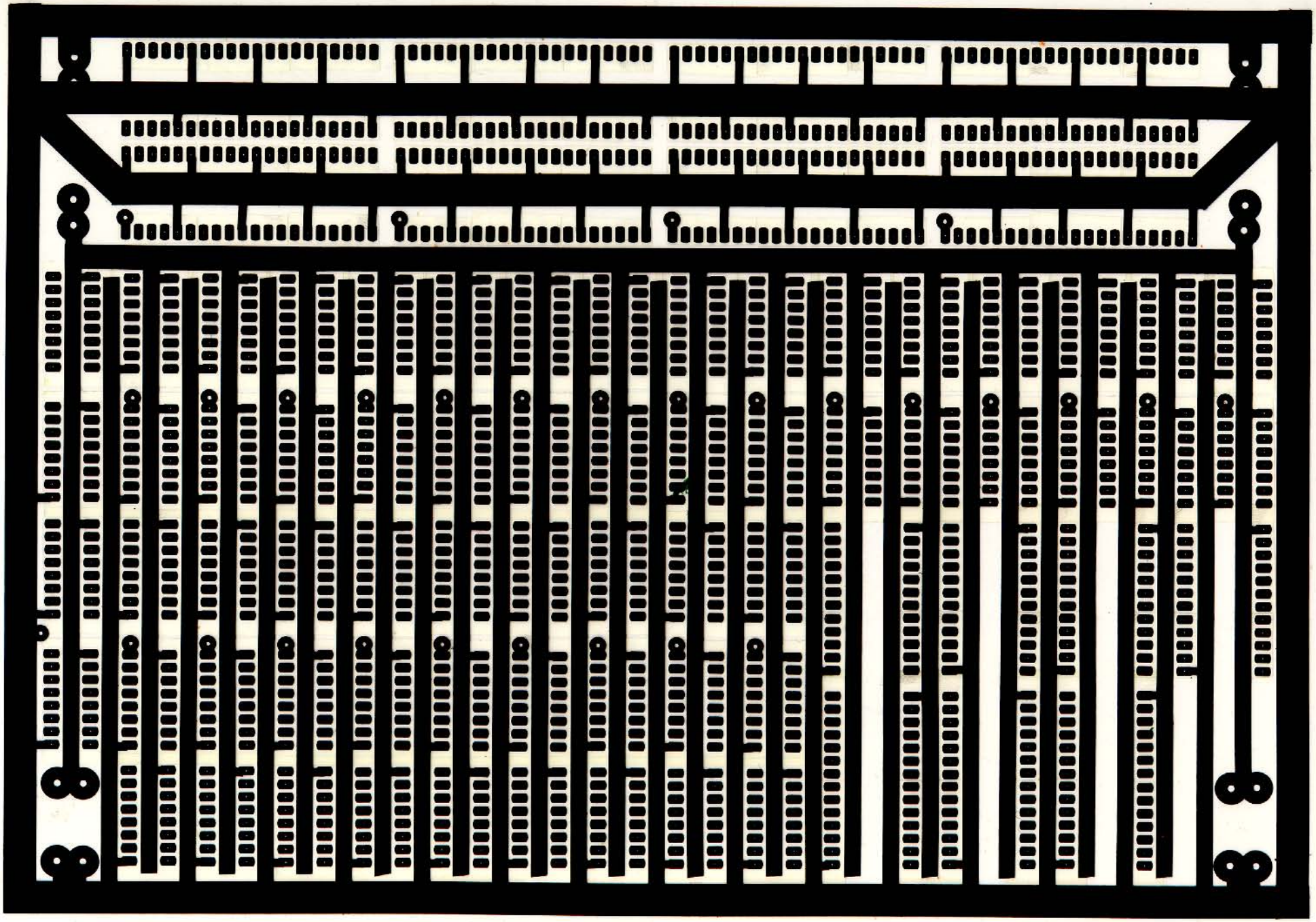
18 June 76
ARB

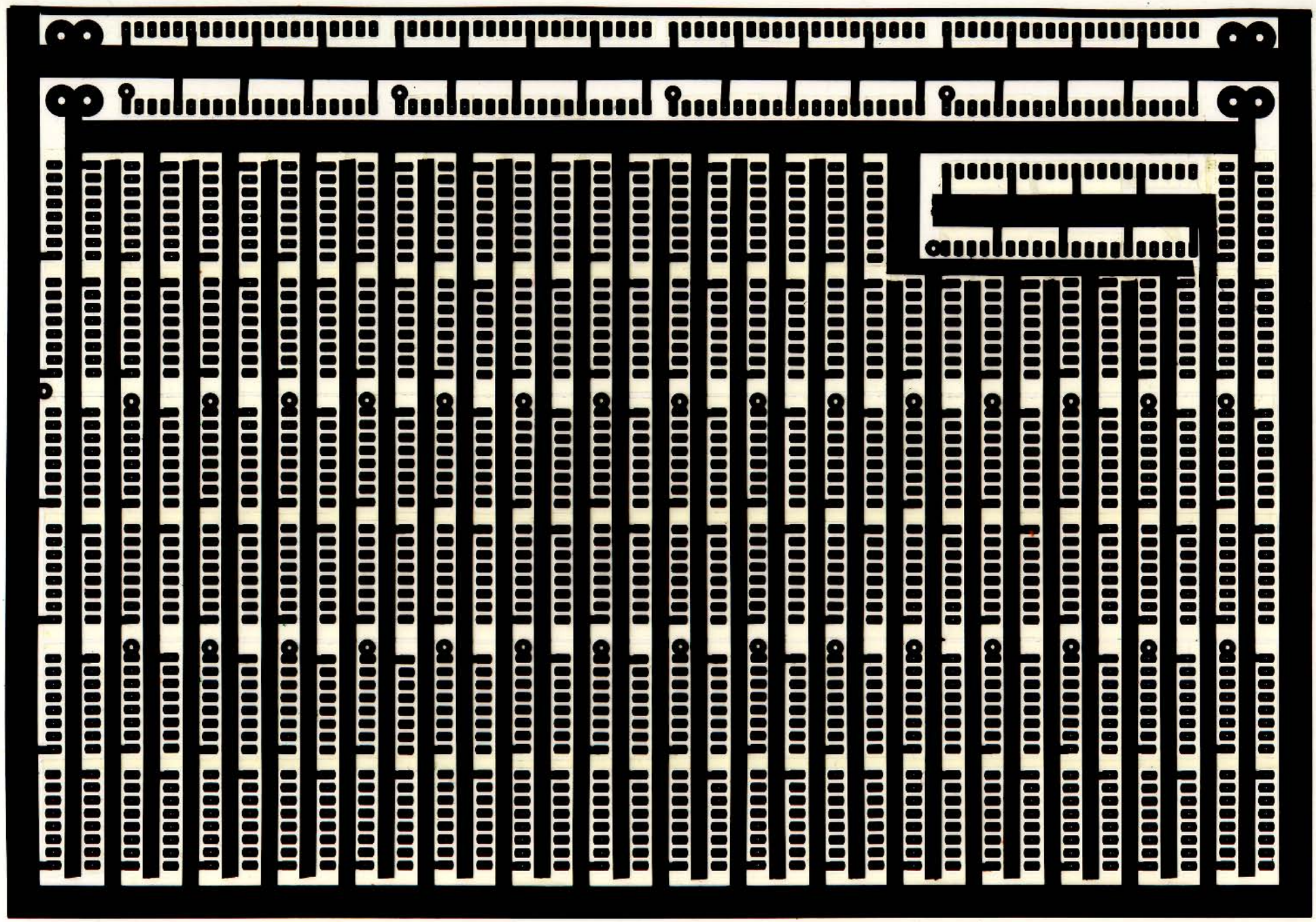


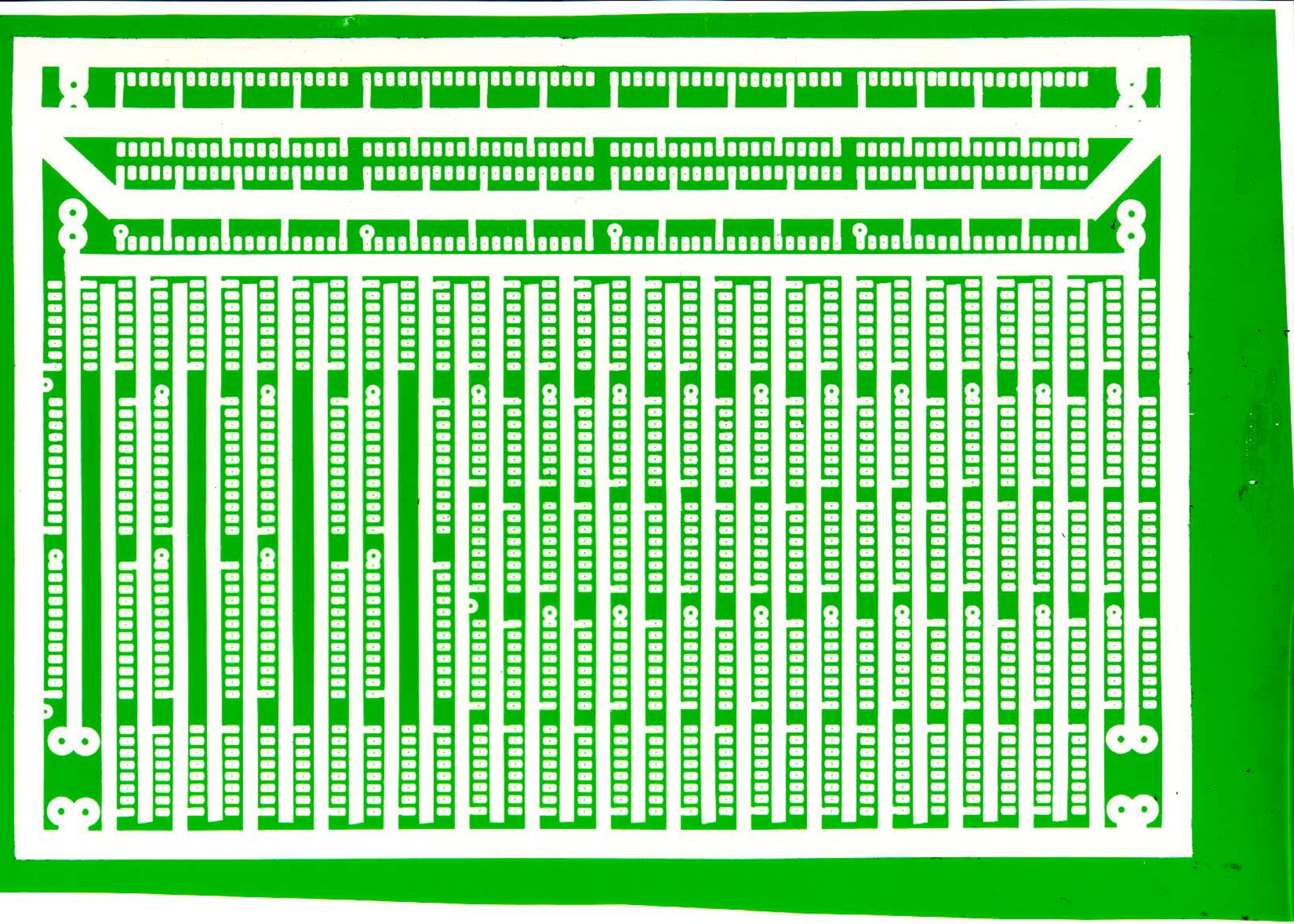
CPUES/ PSW/ SLR/ CP Counter/ OR Cmd Board
Top & Bottom
Positive

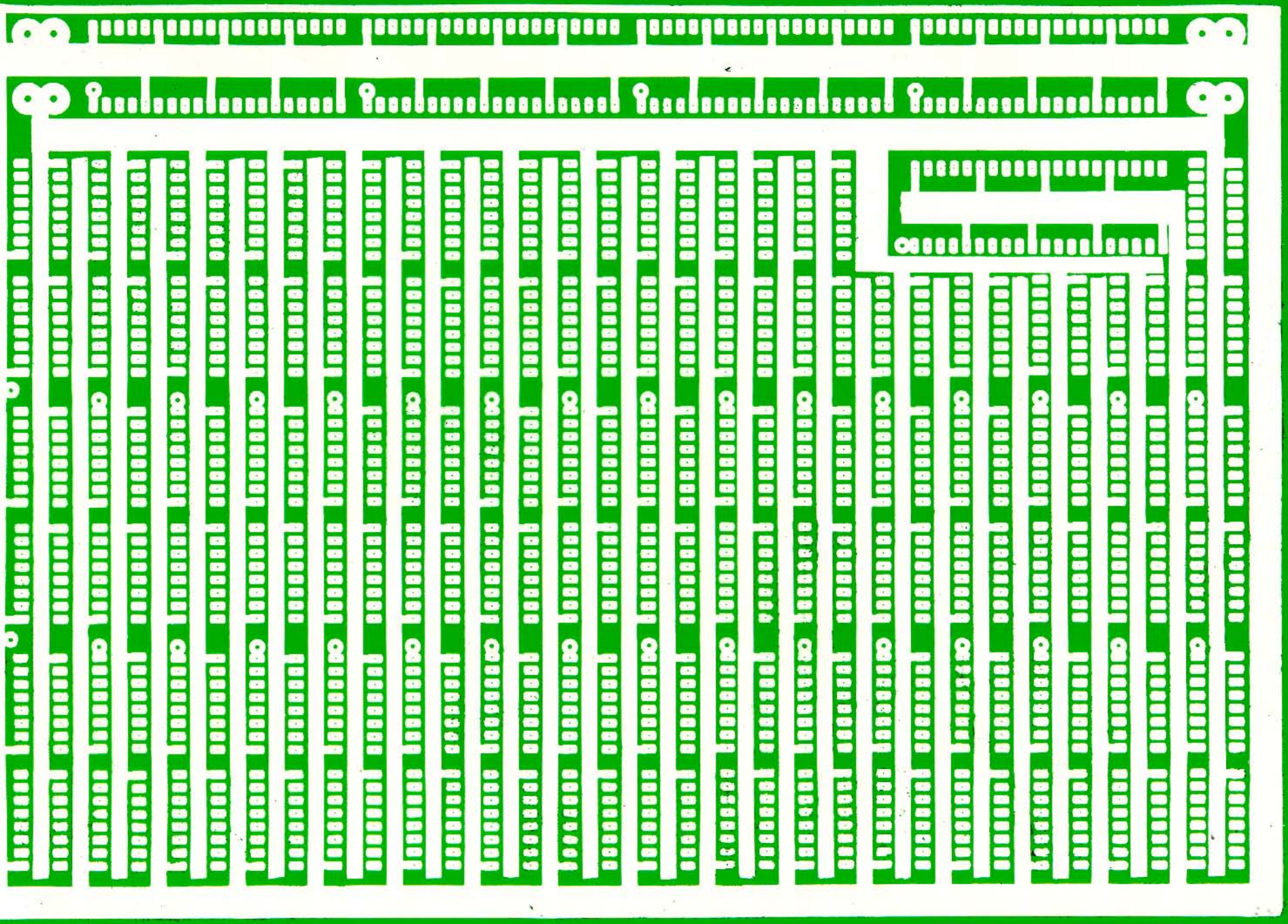
19 June 76
ARD

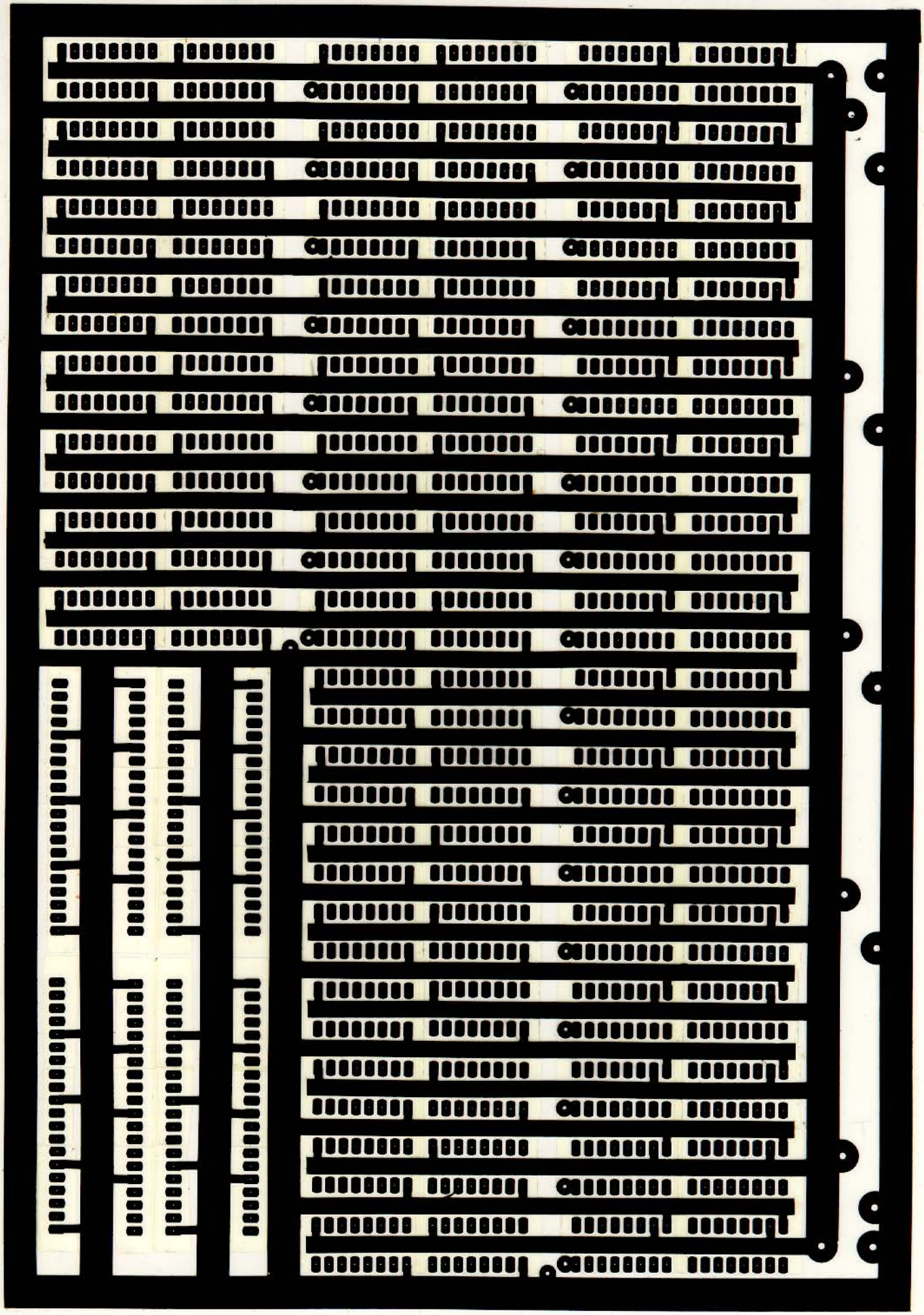


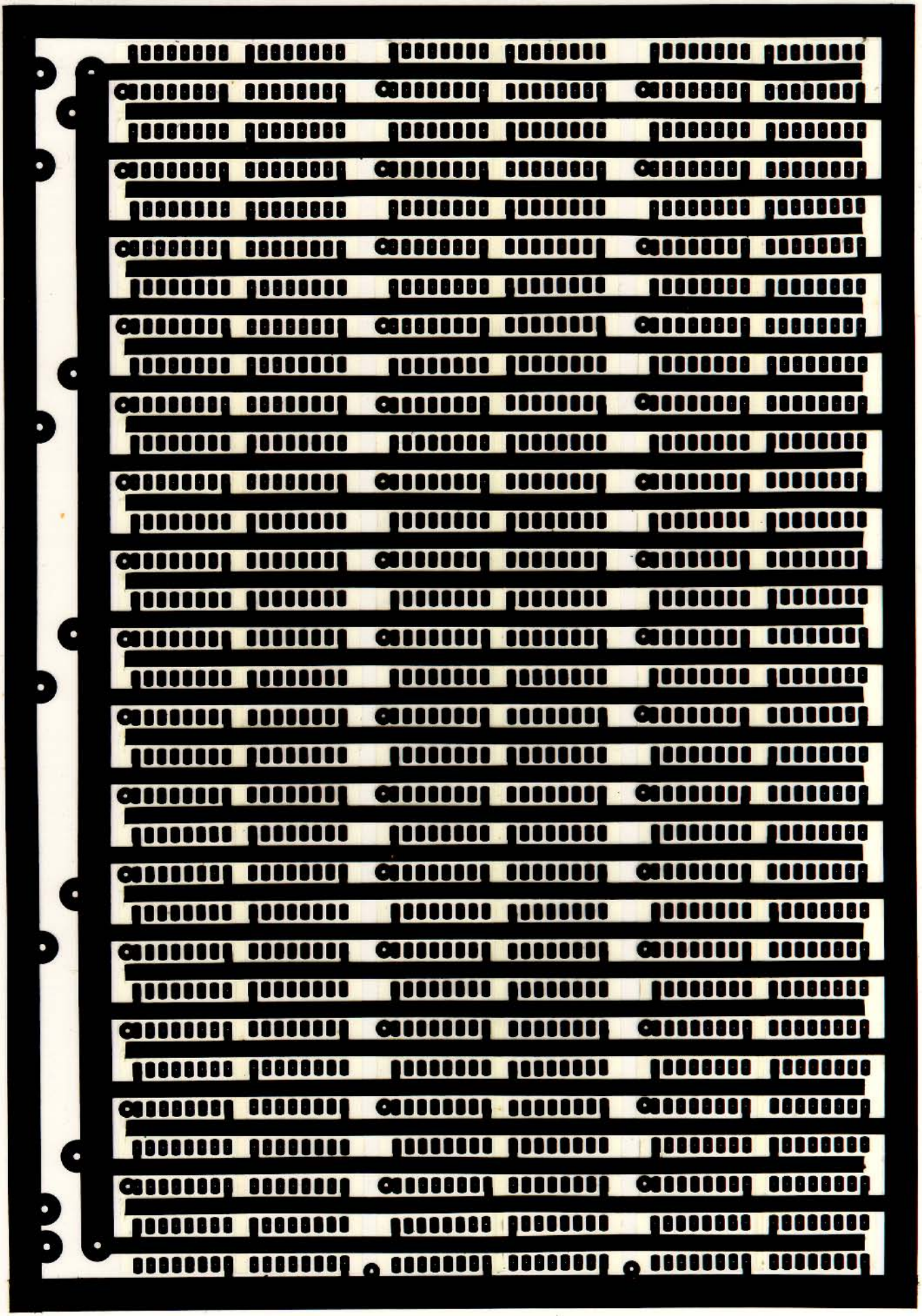


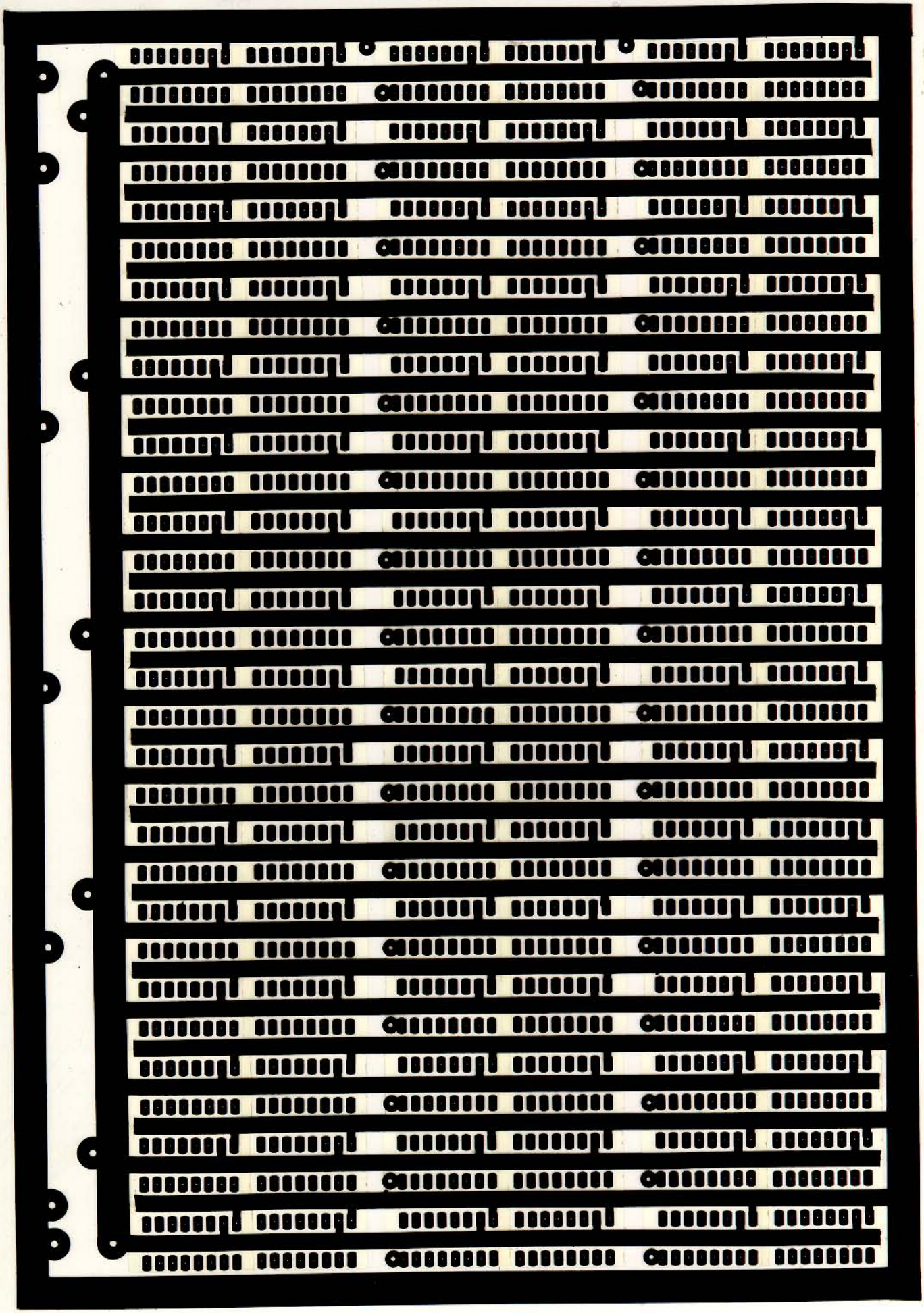


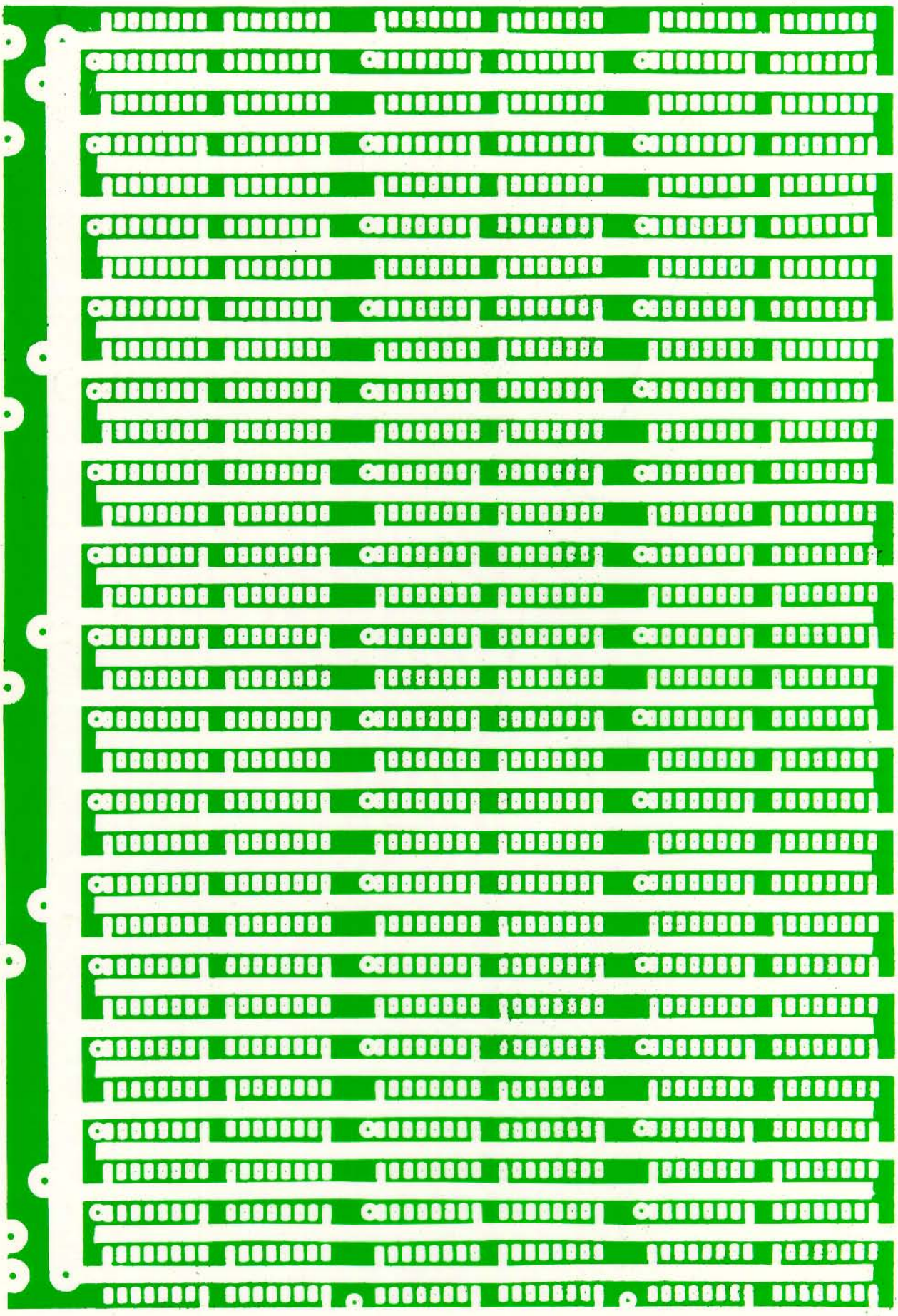


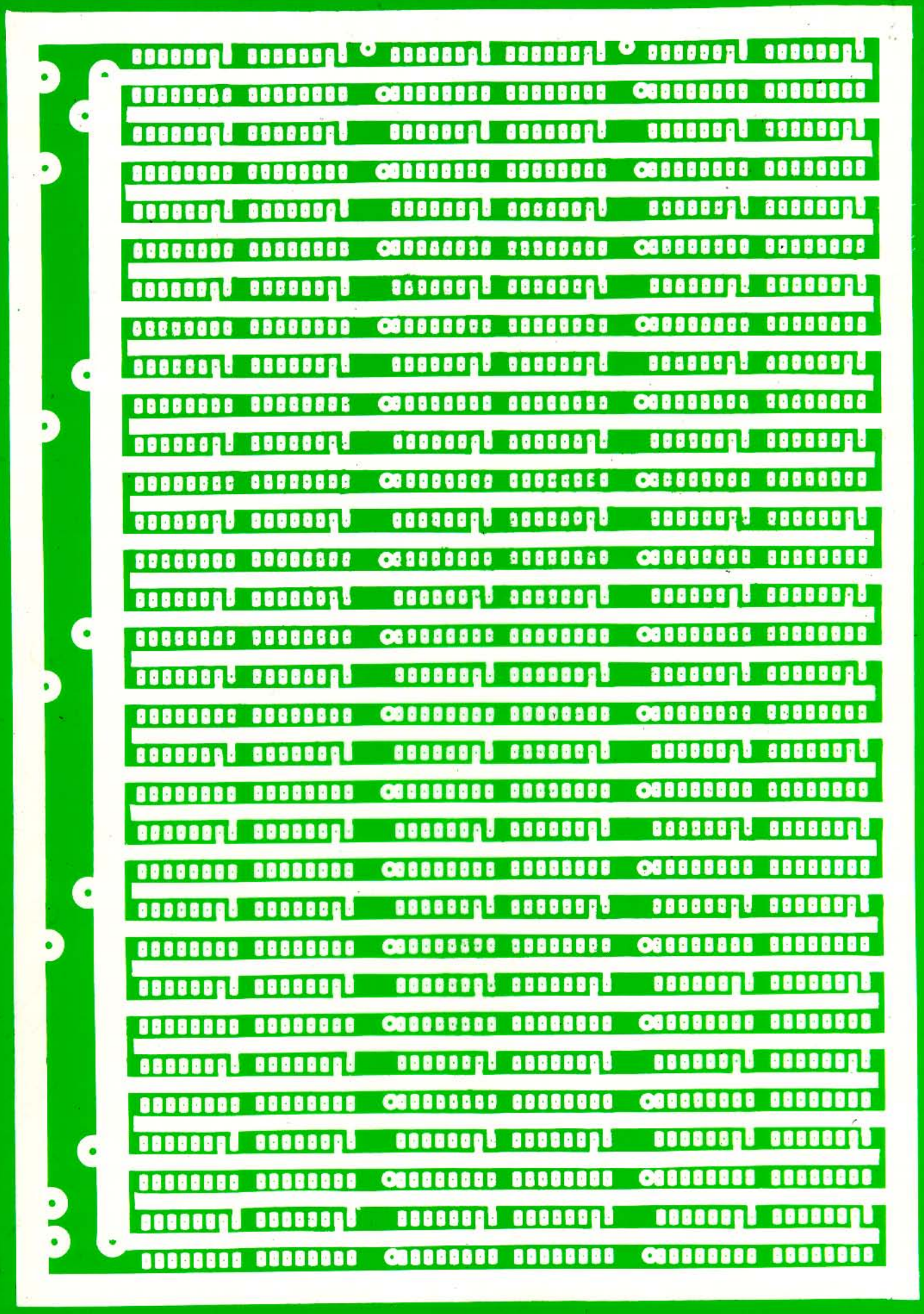


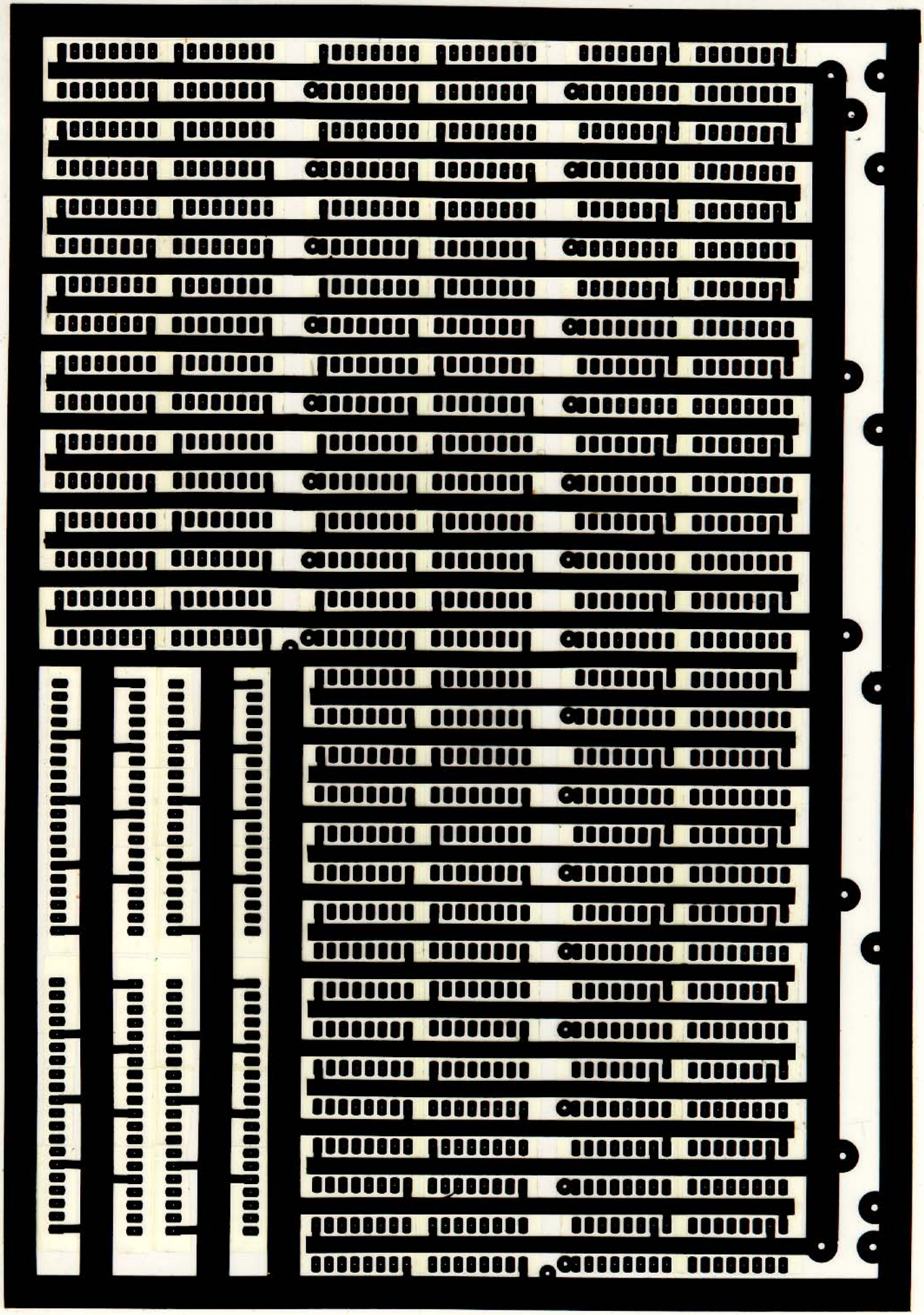


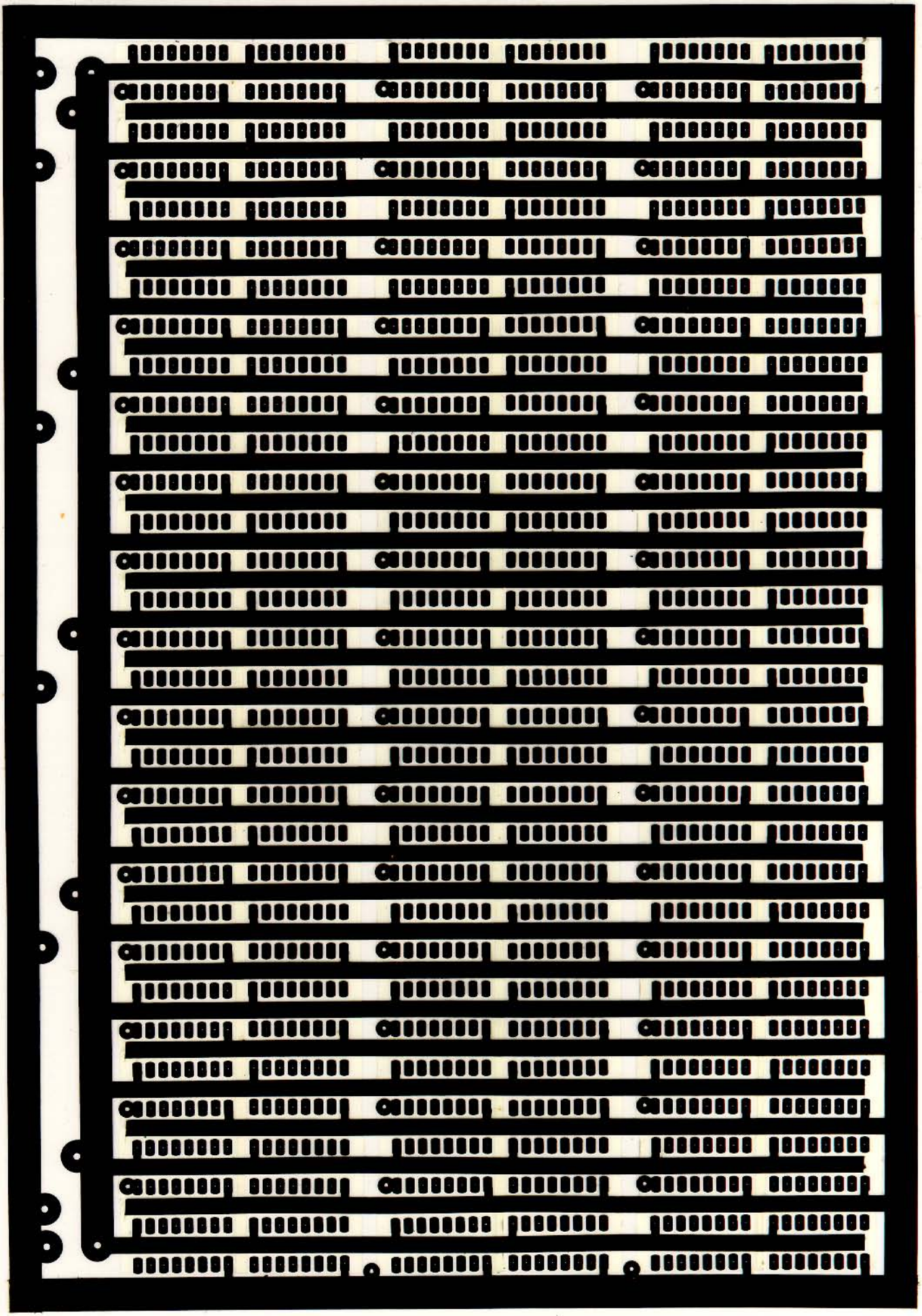


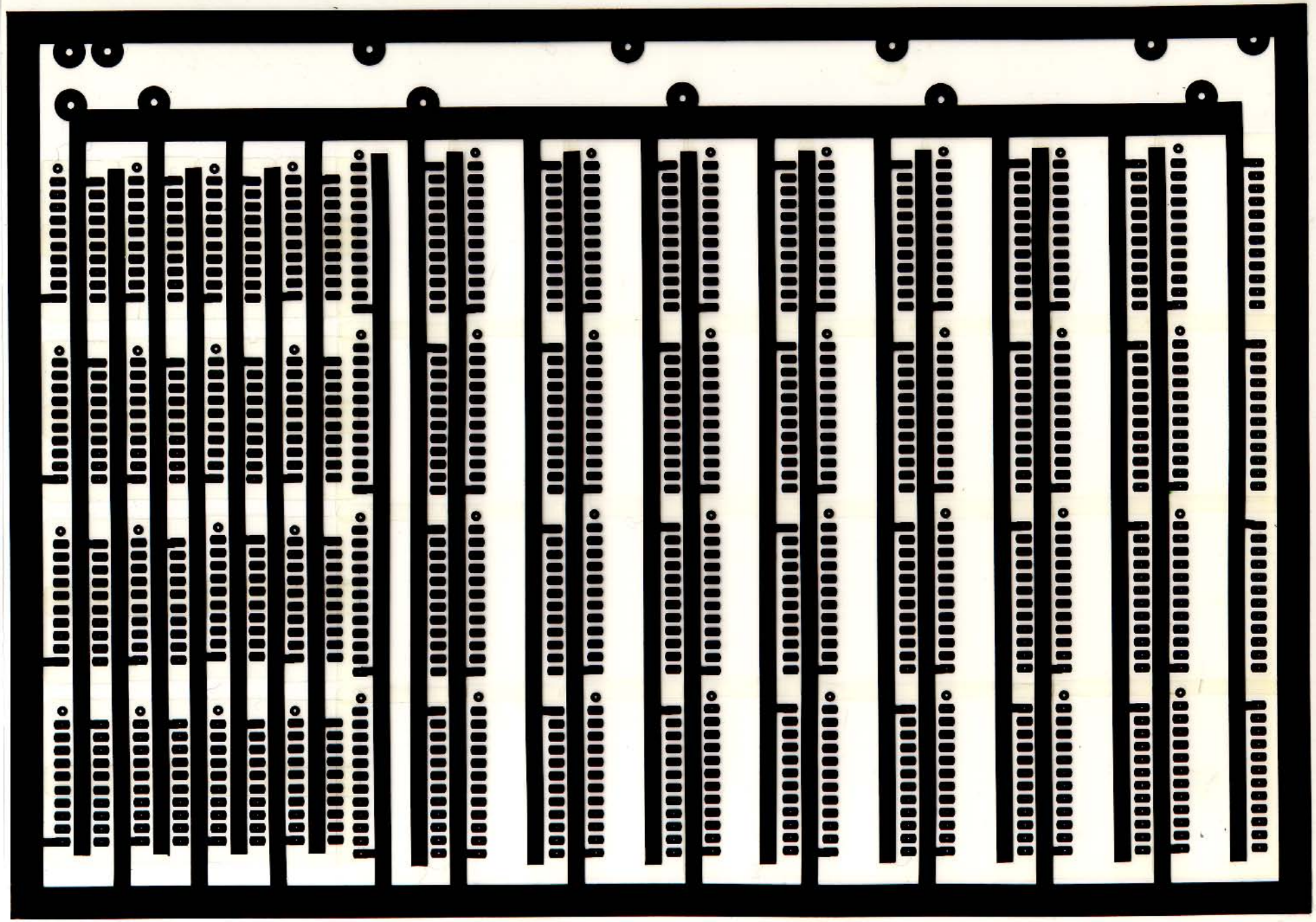




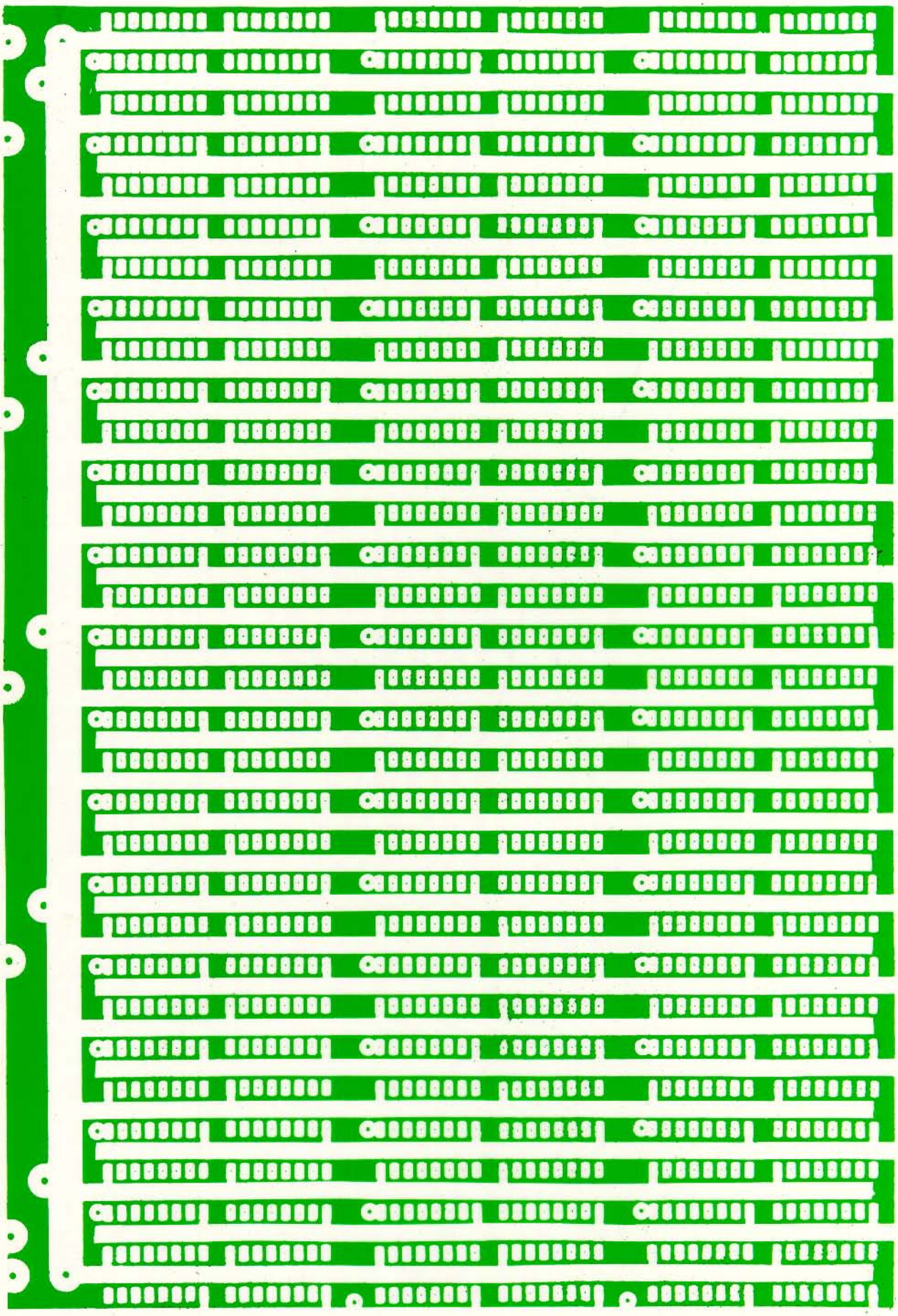


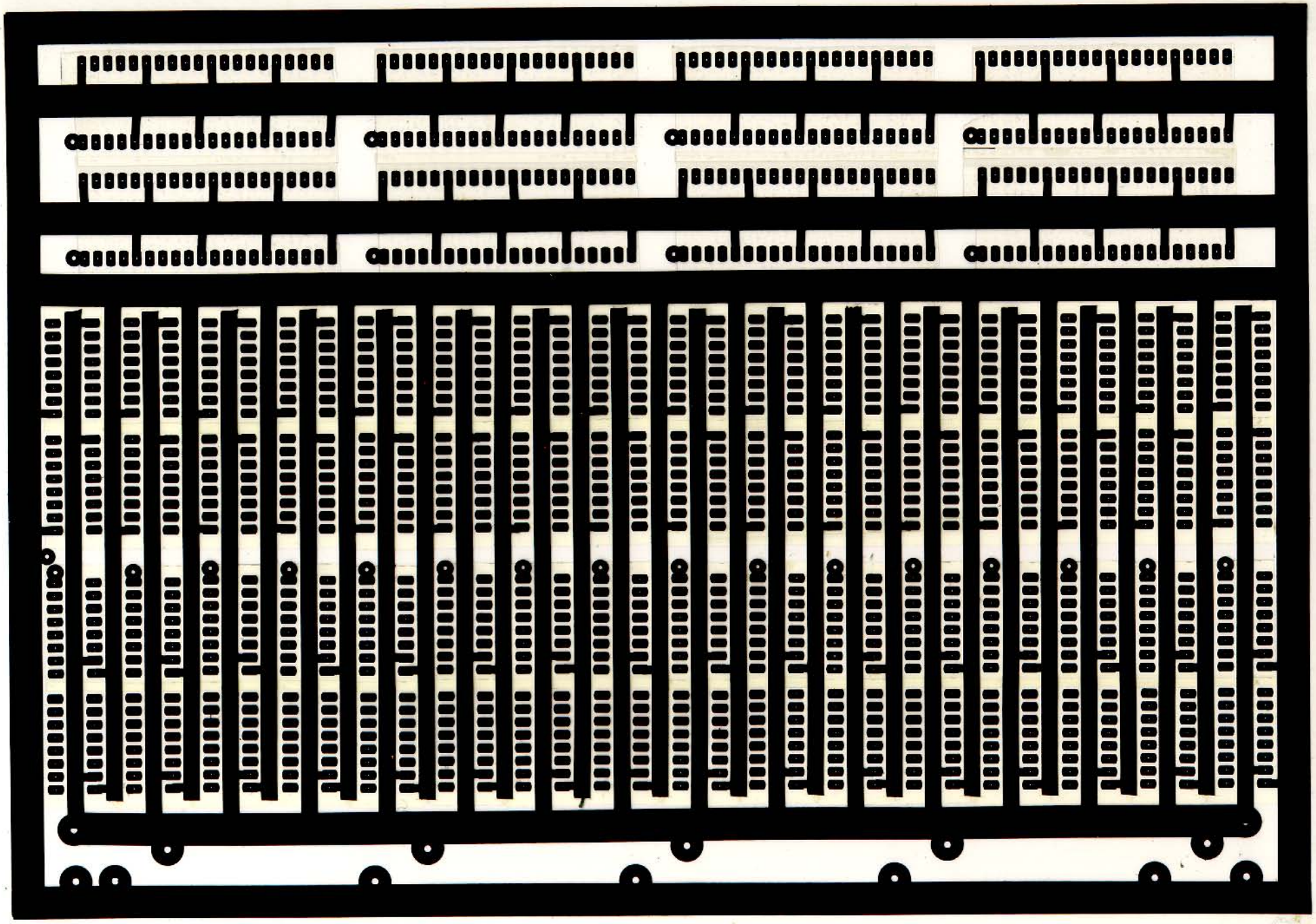


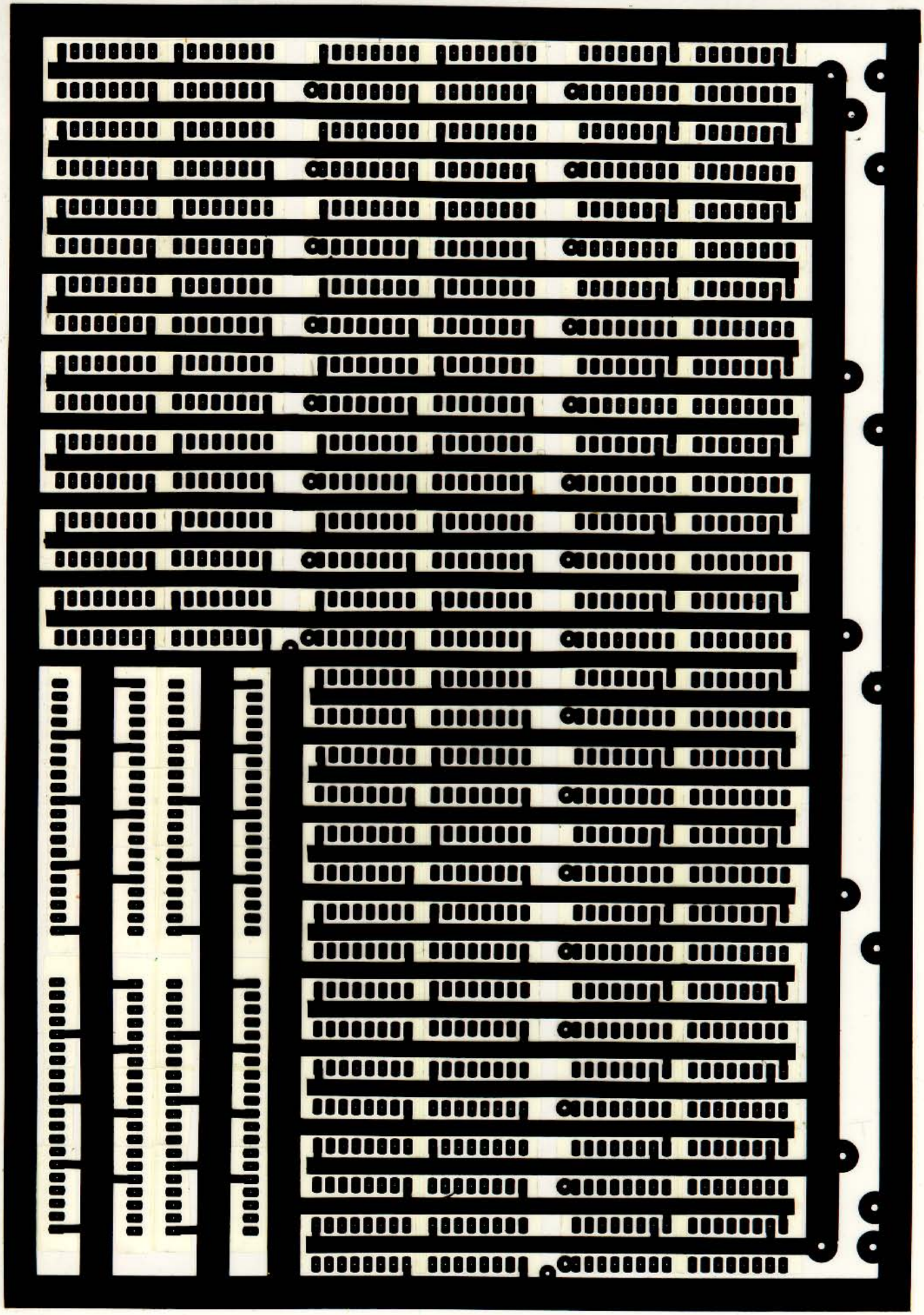


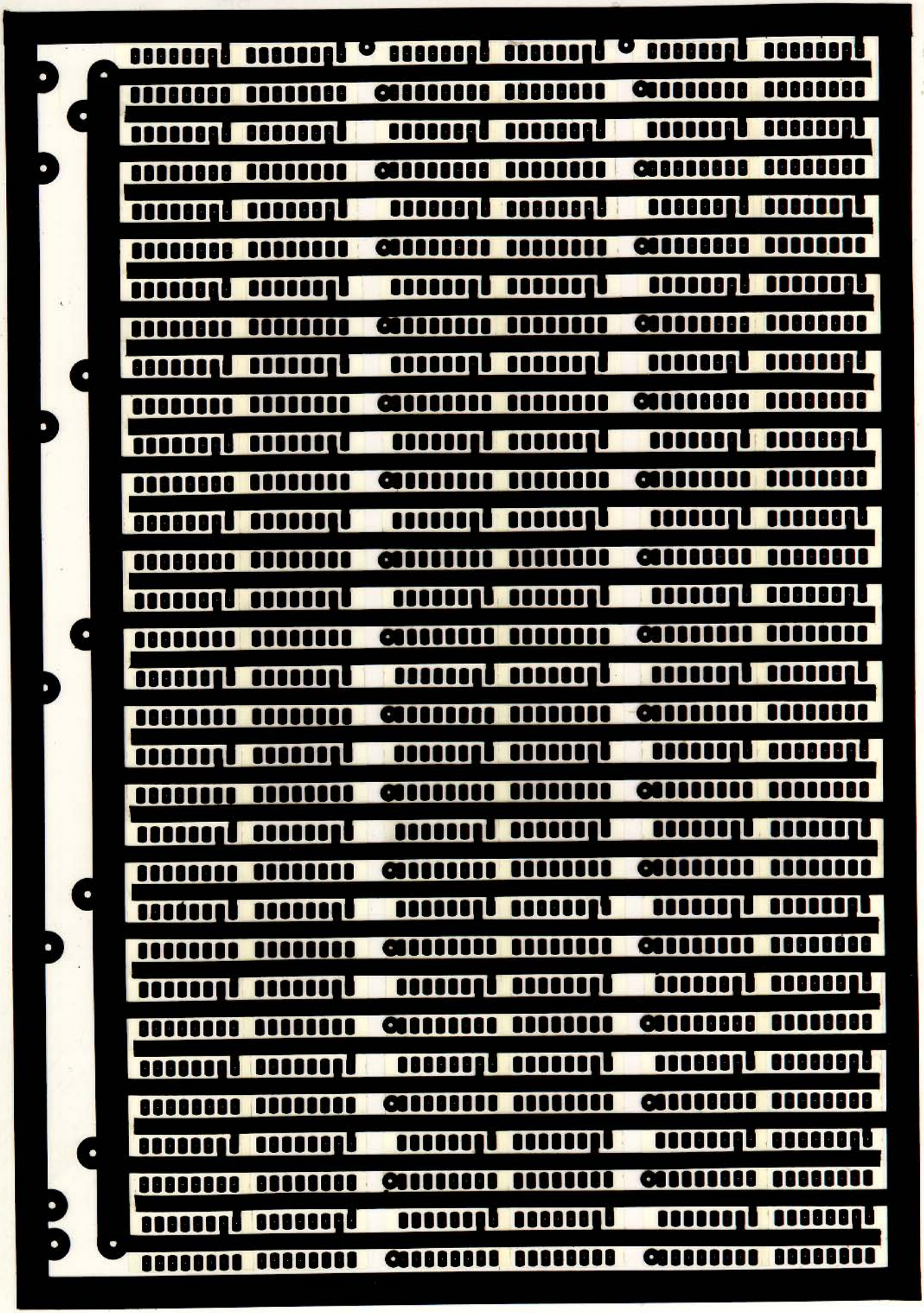


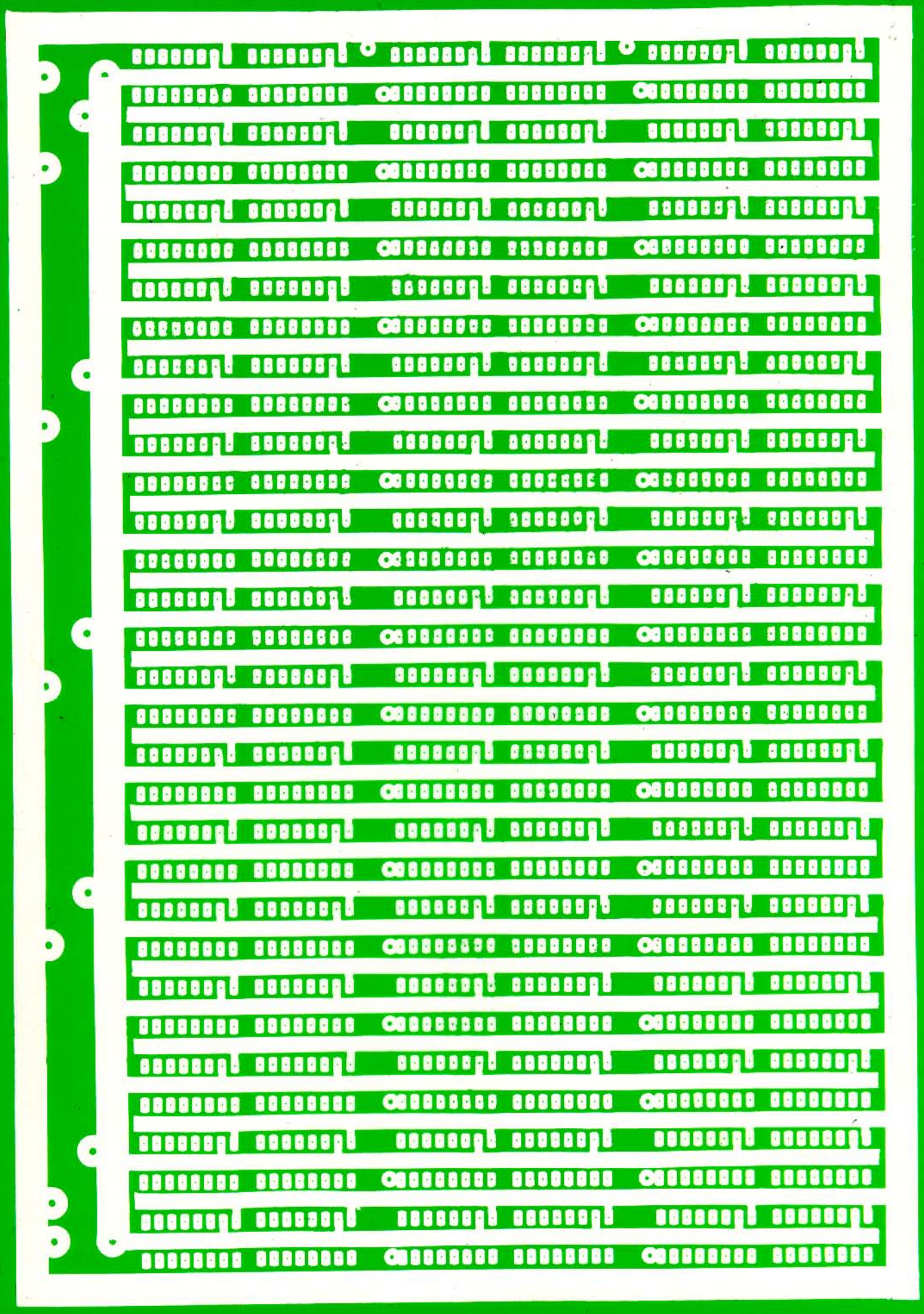
ARB Processor Microcode Replacement Board

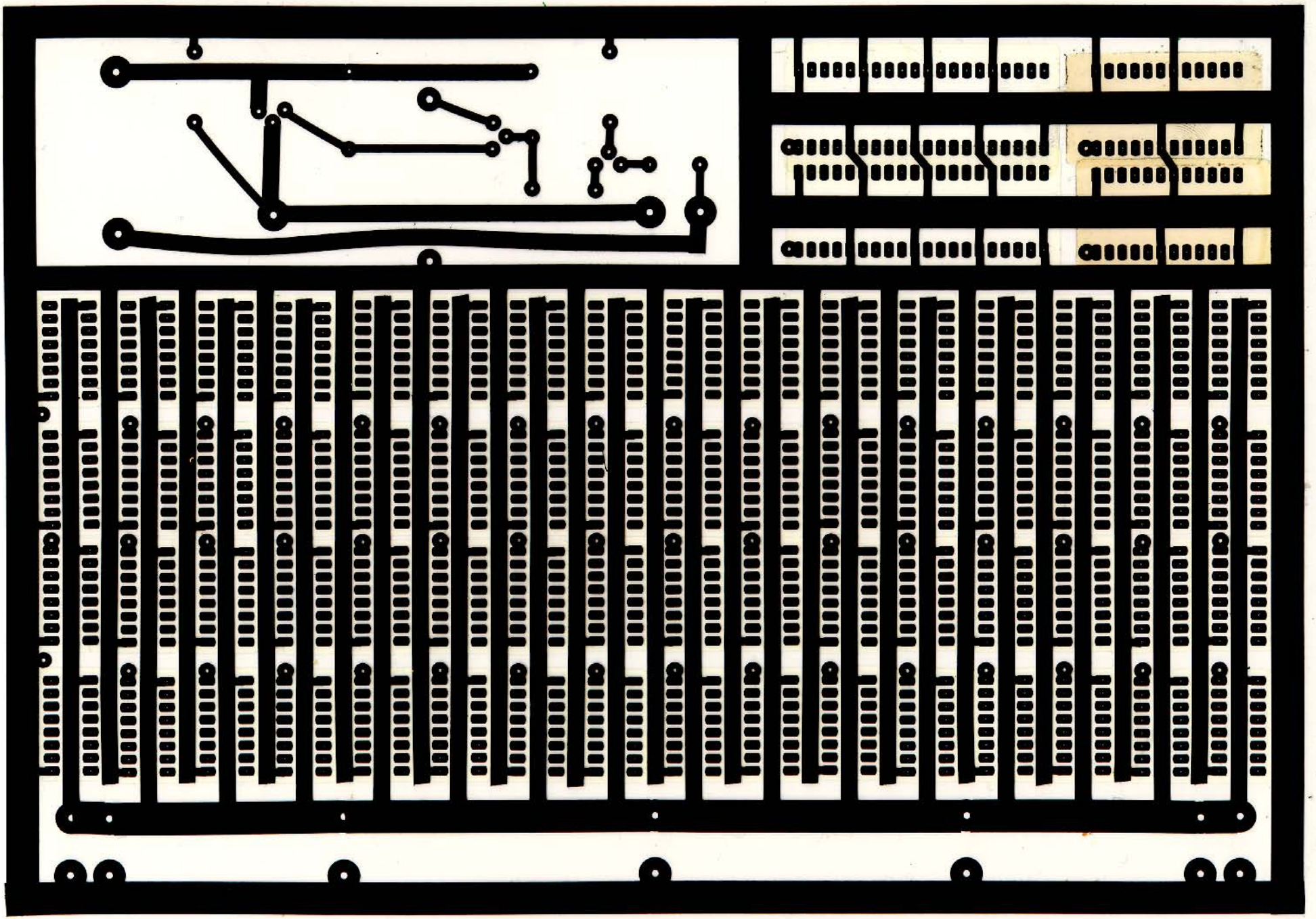


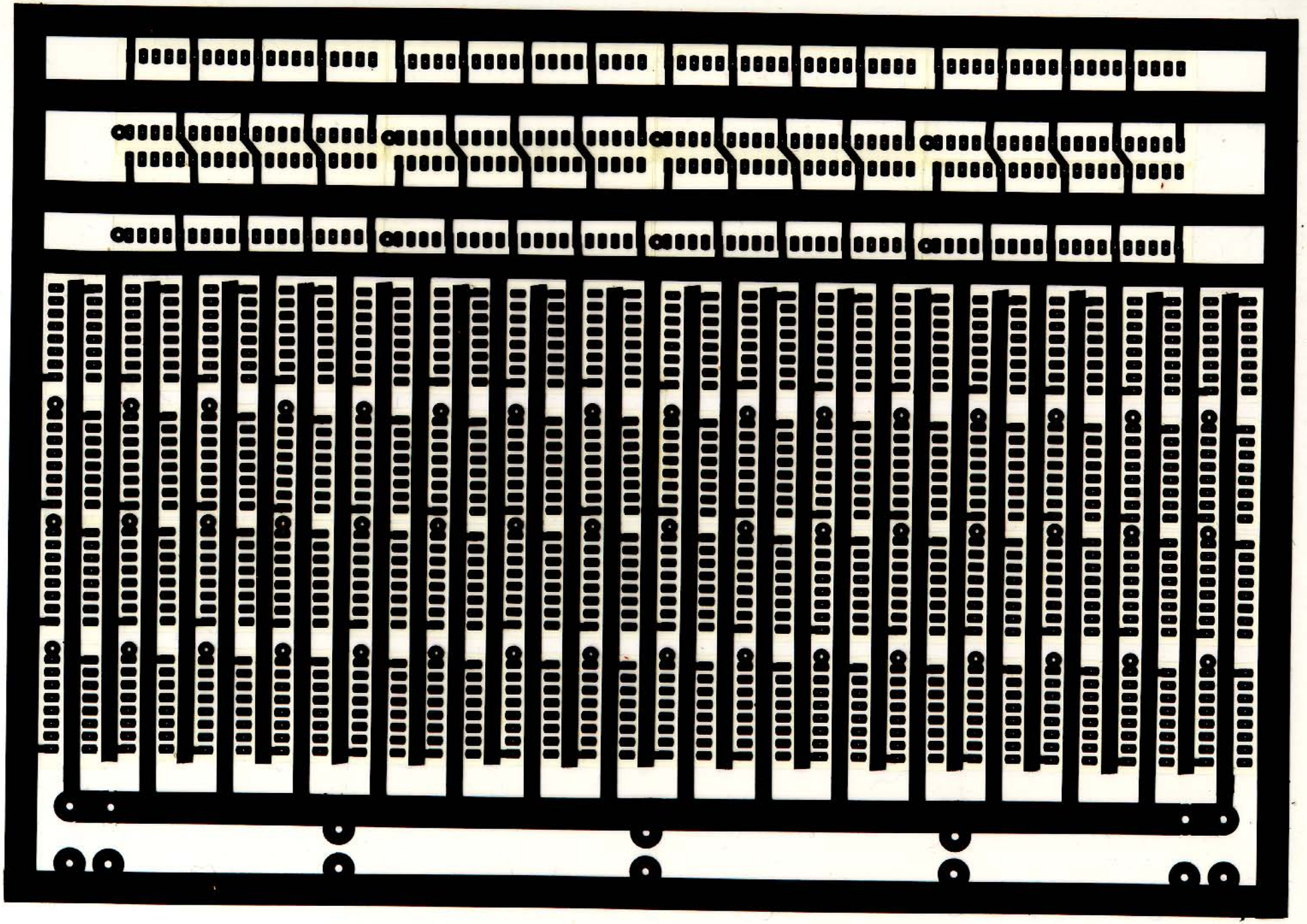




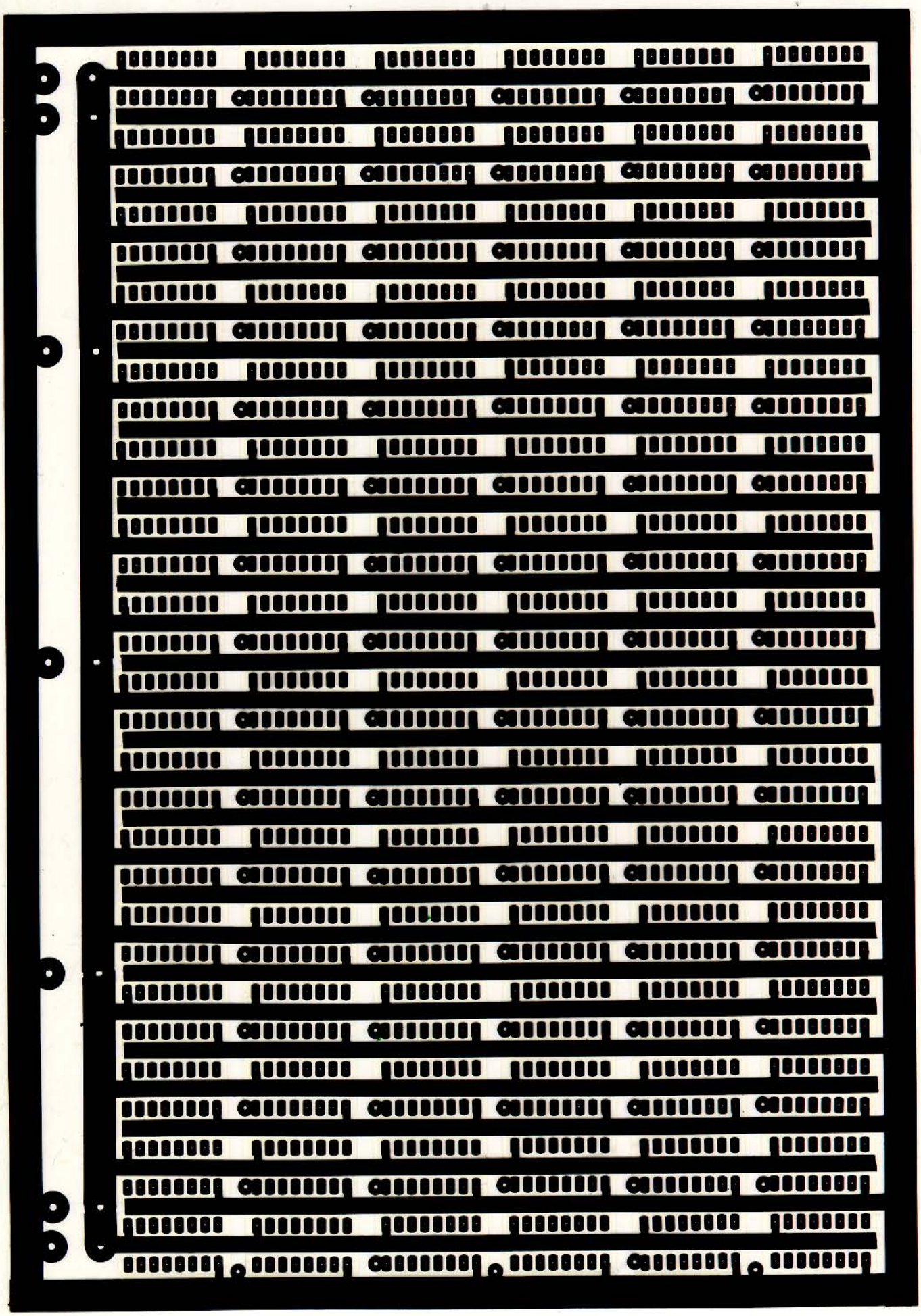


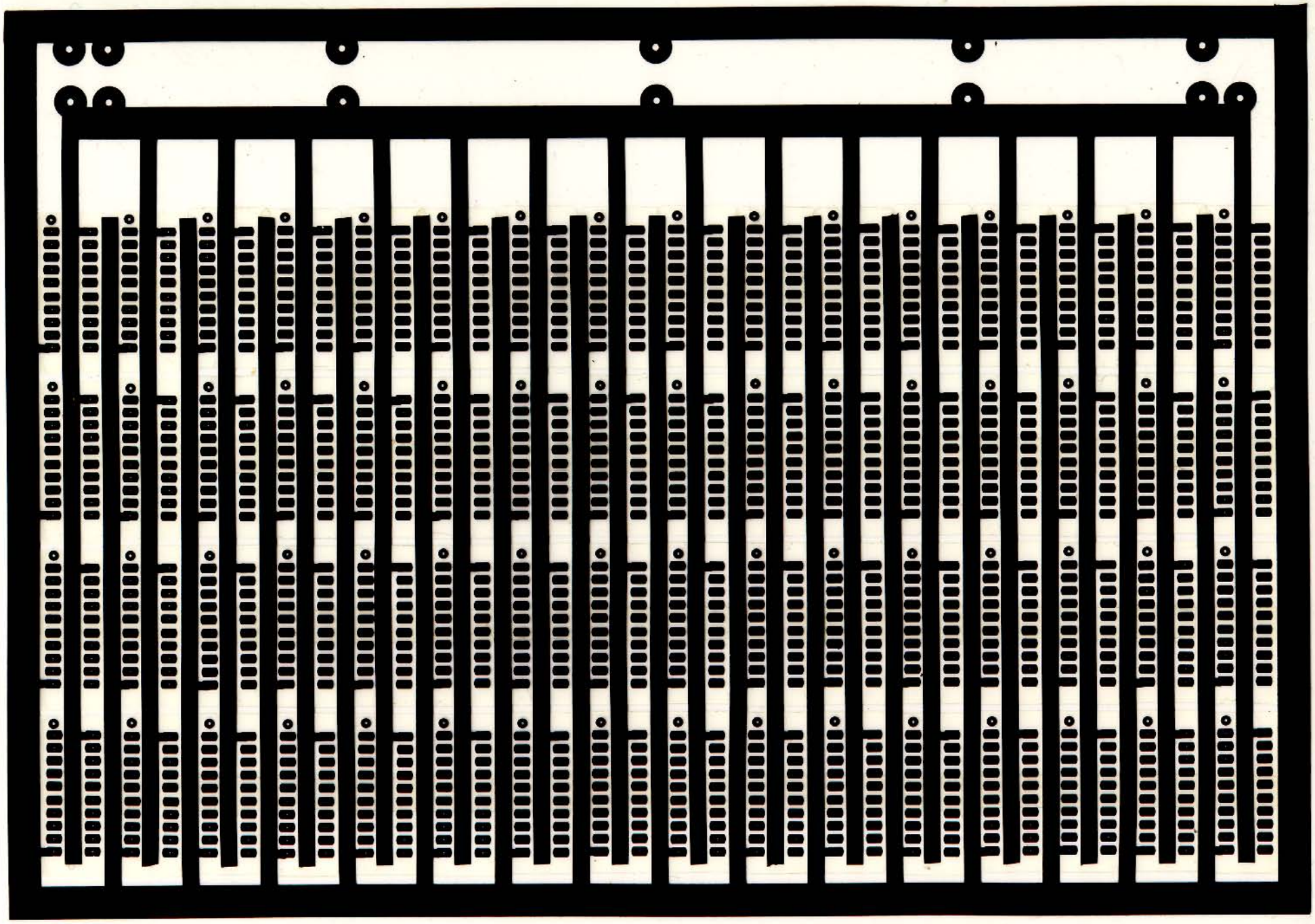




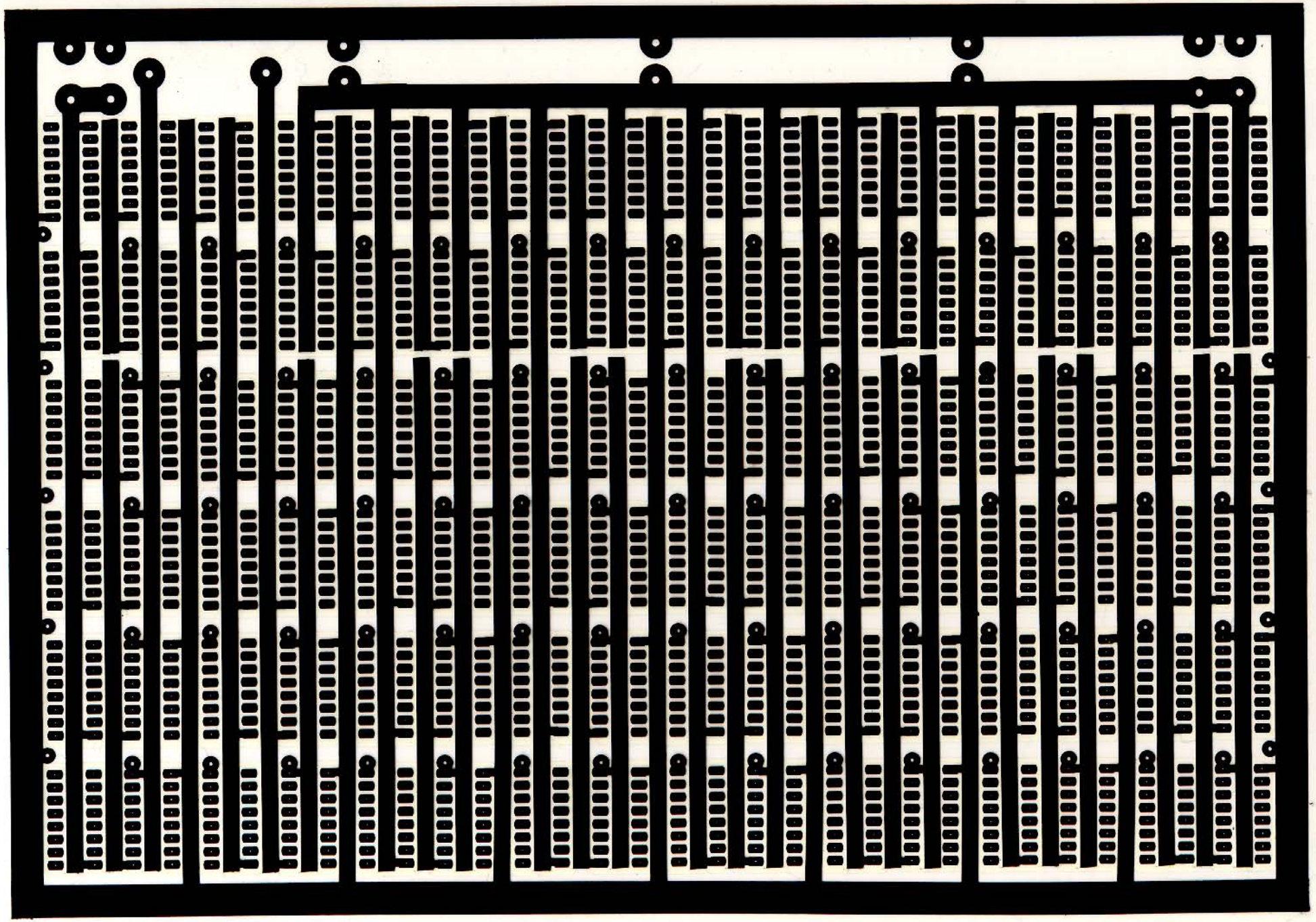


MAP

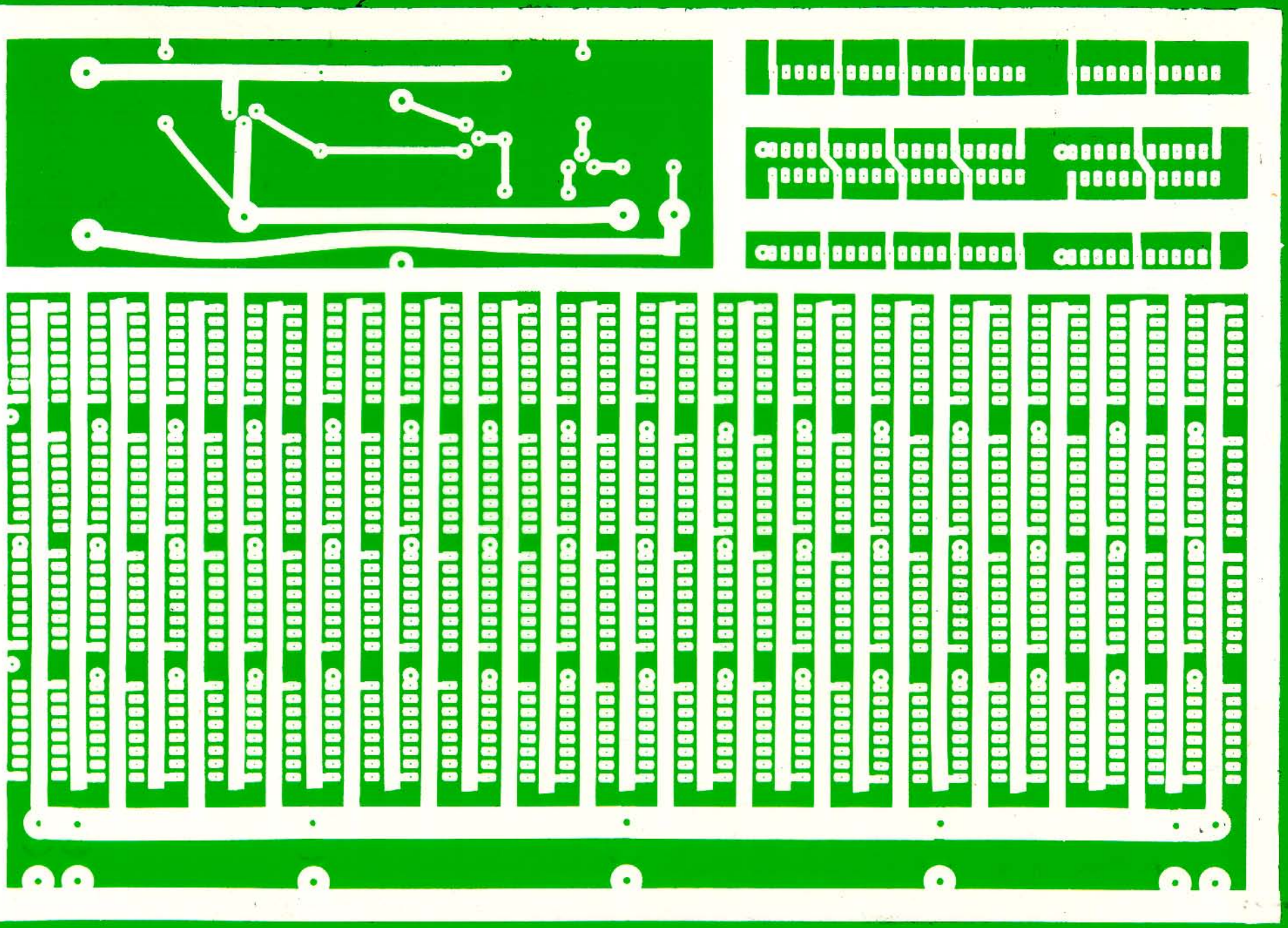


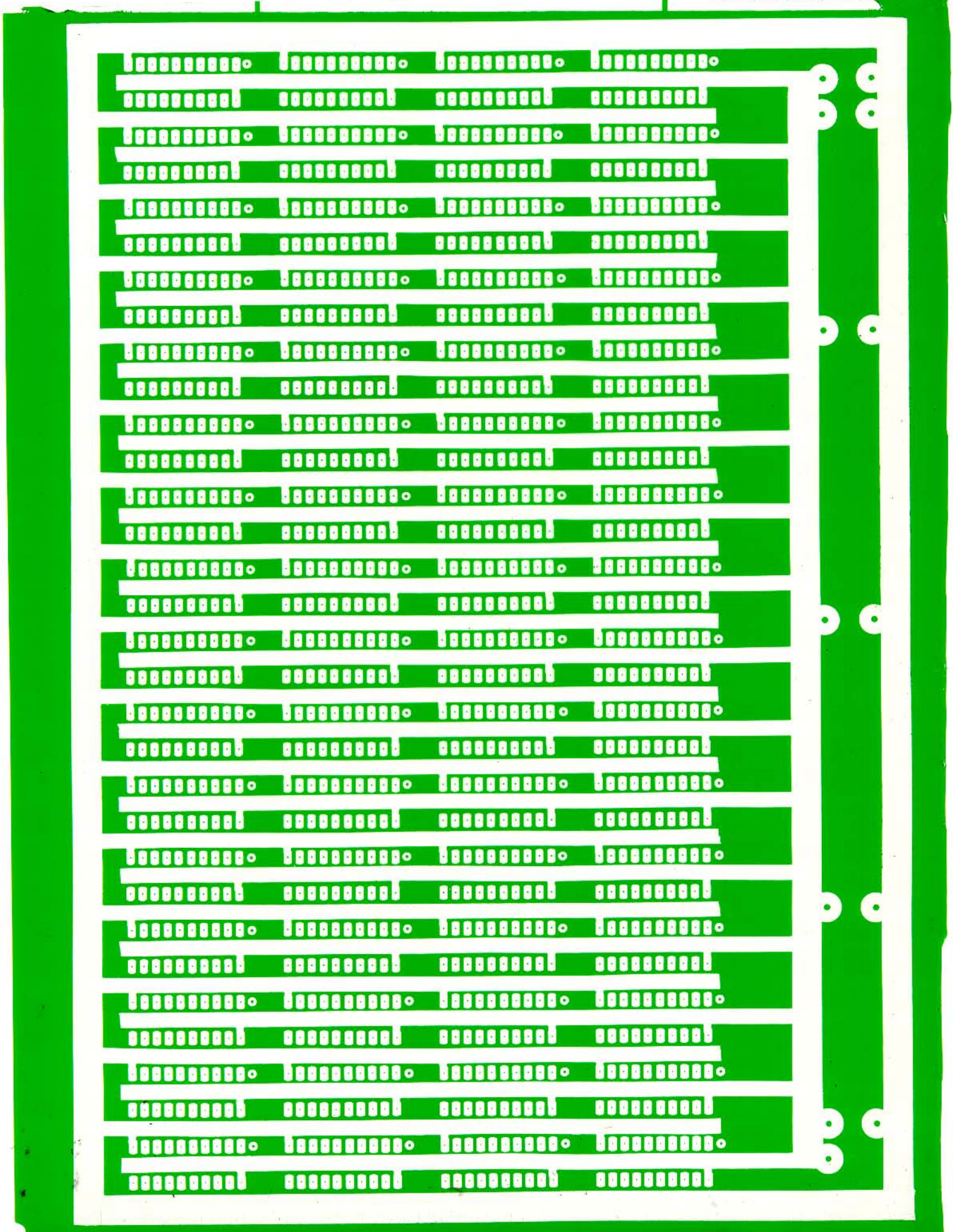


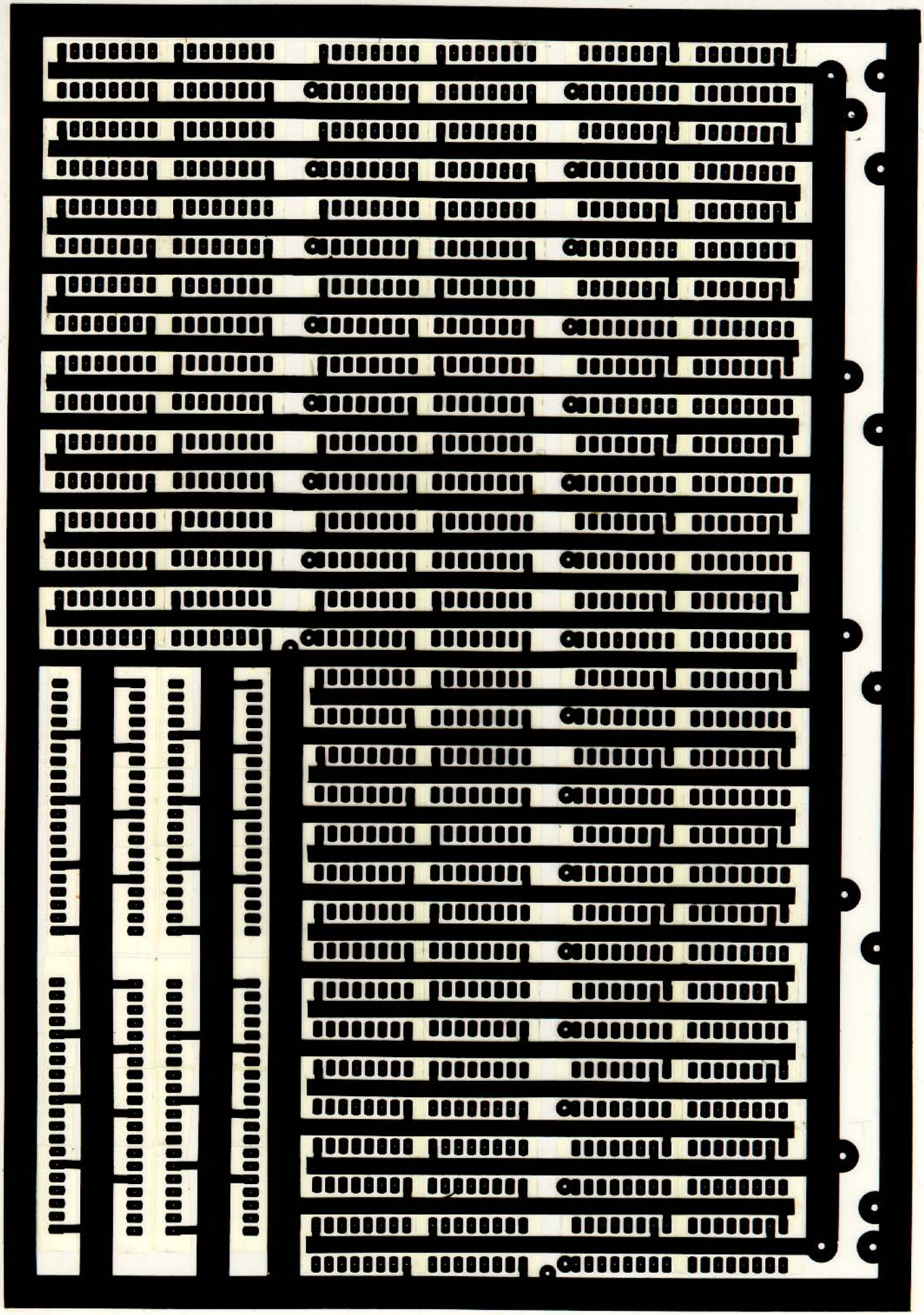
64KW FAST Memory Replacement MMOT Panel

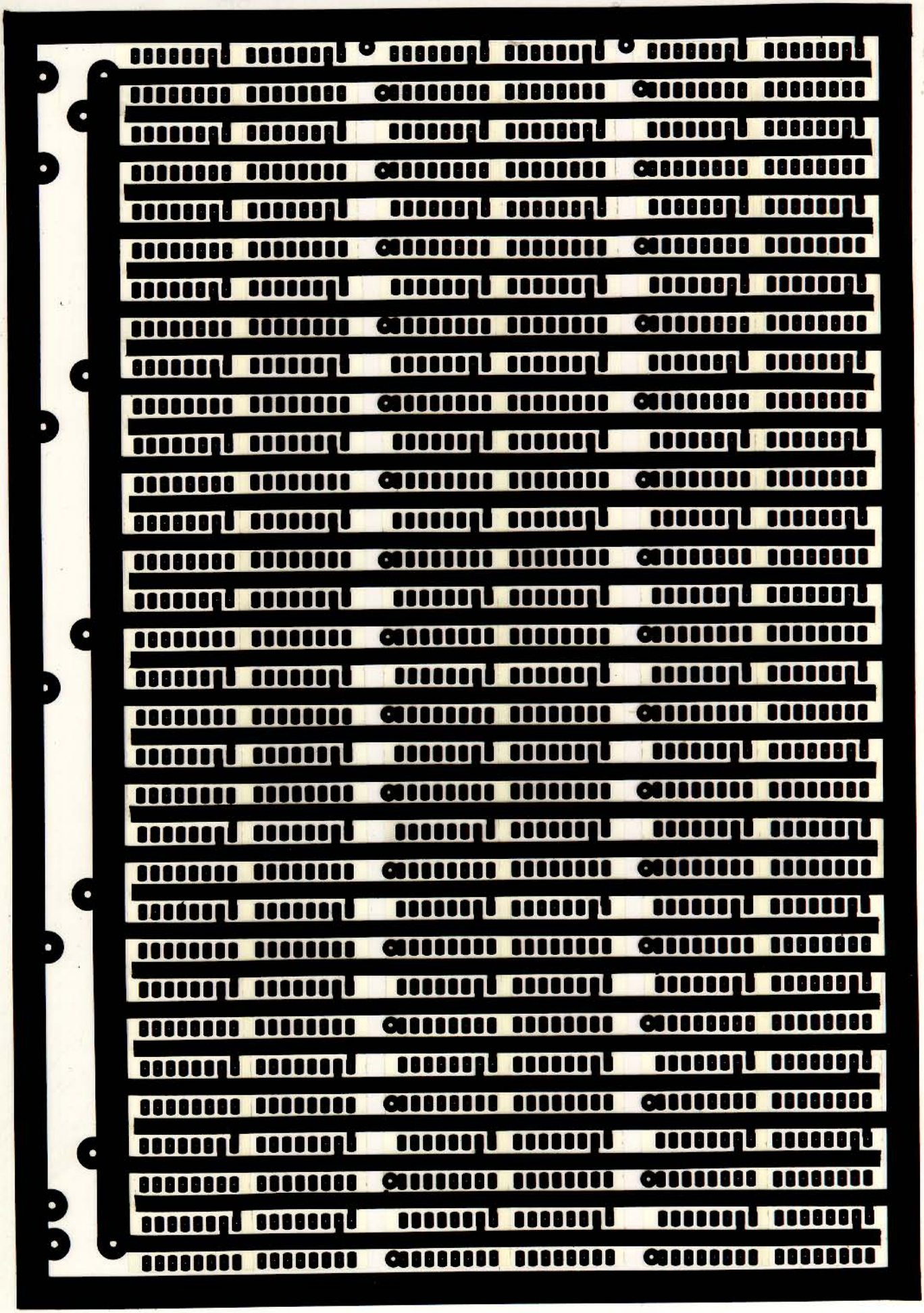


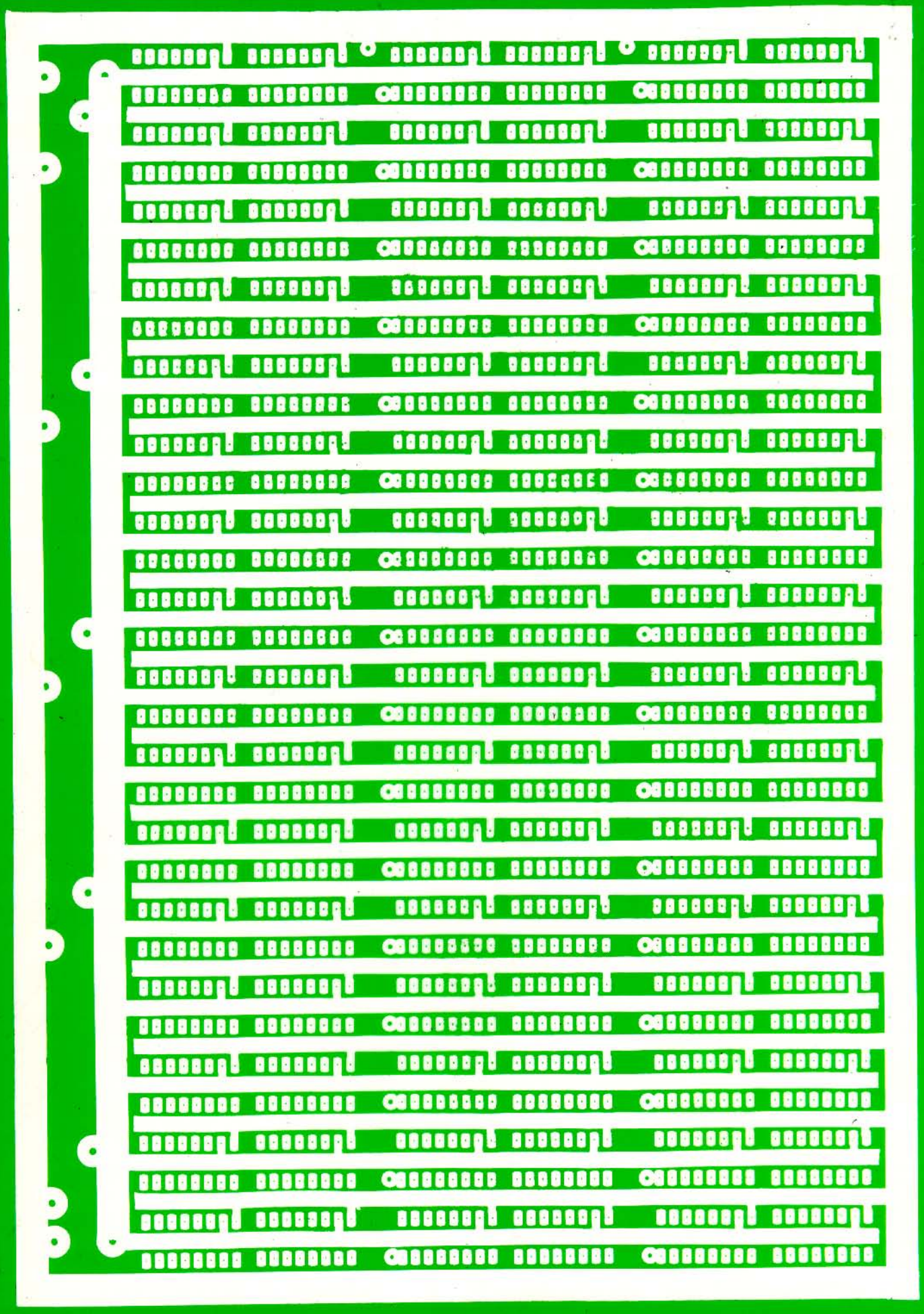
MROT / 16K Memory

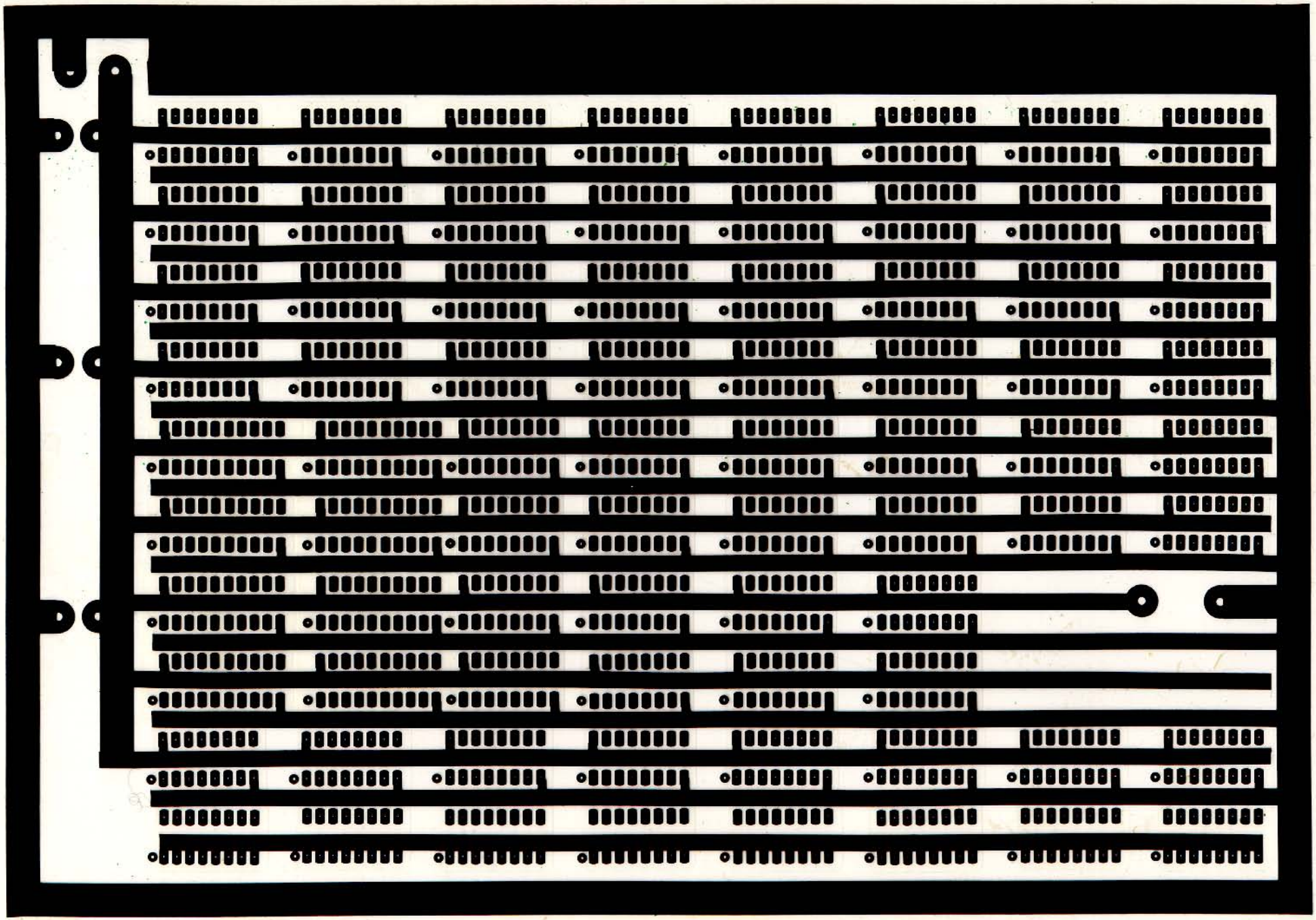




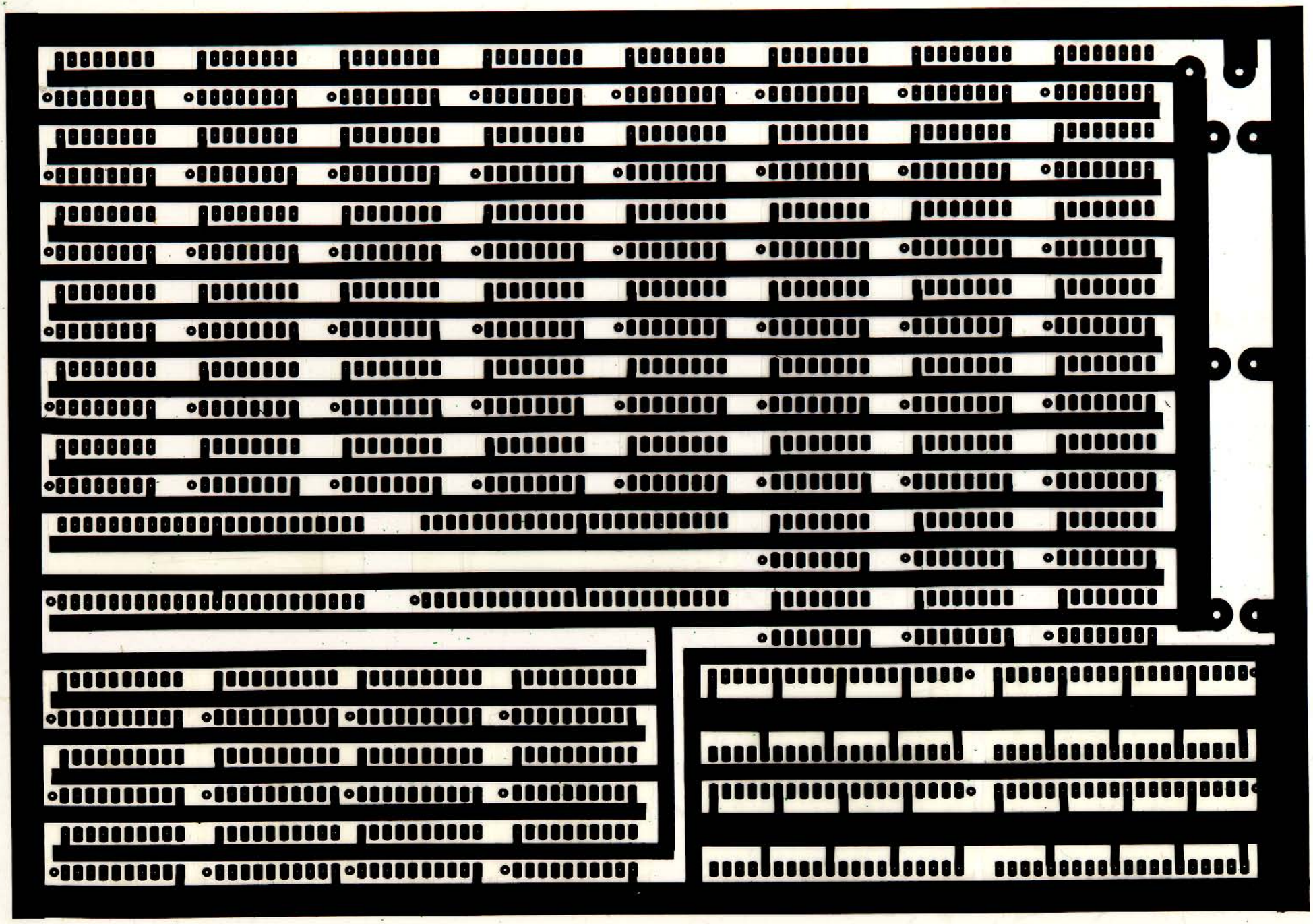




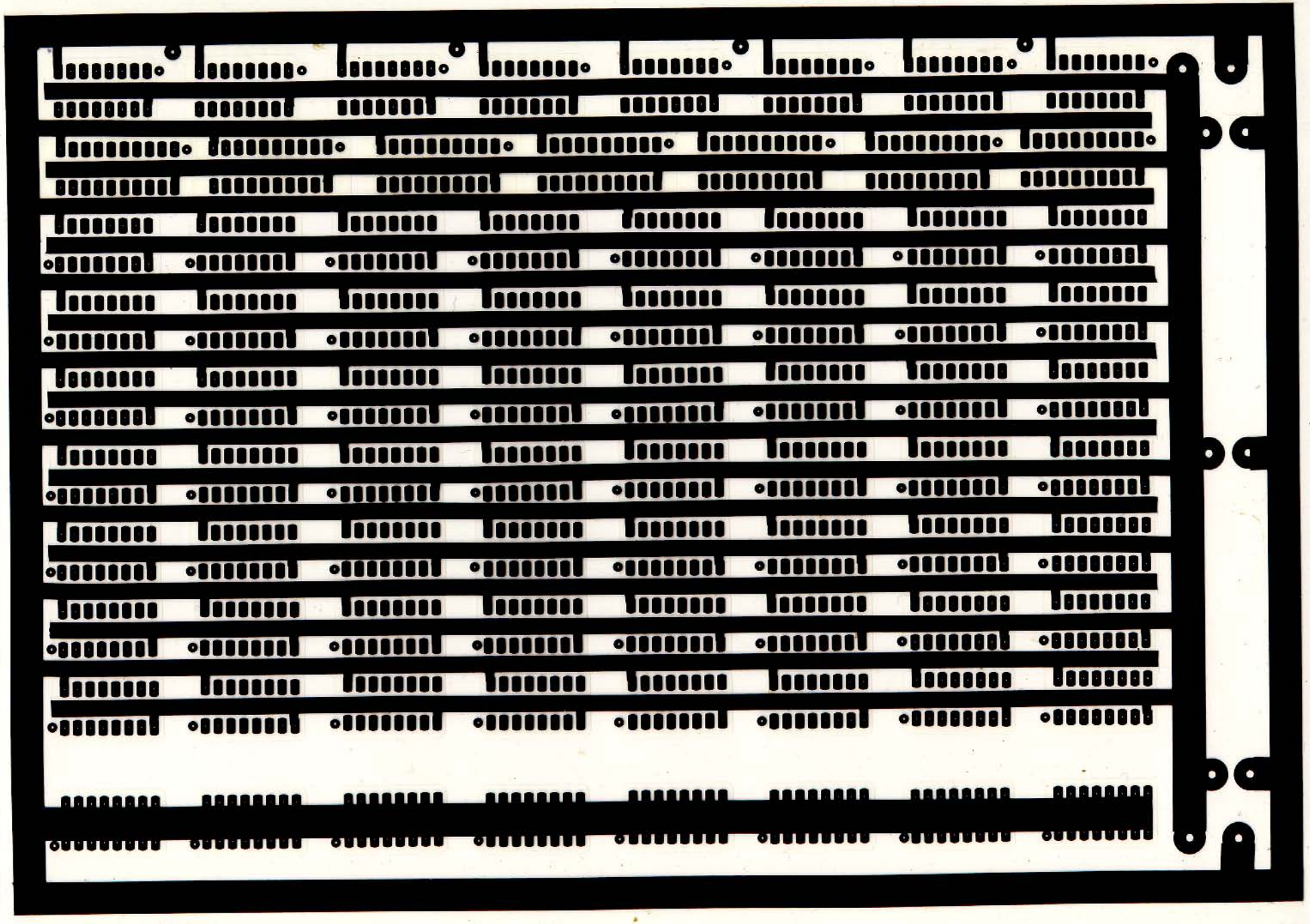




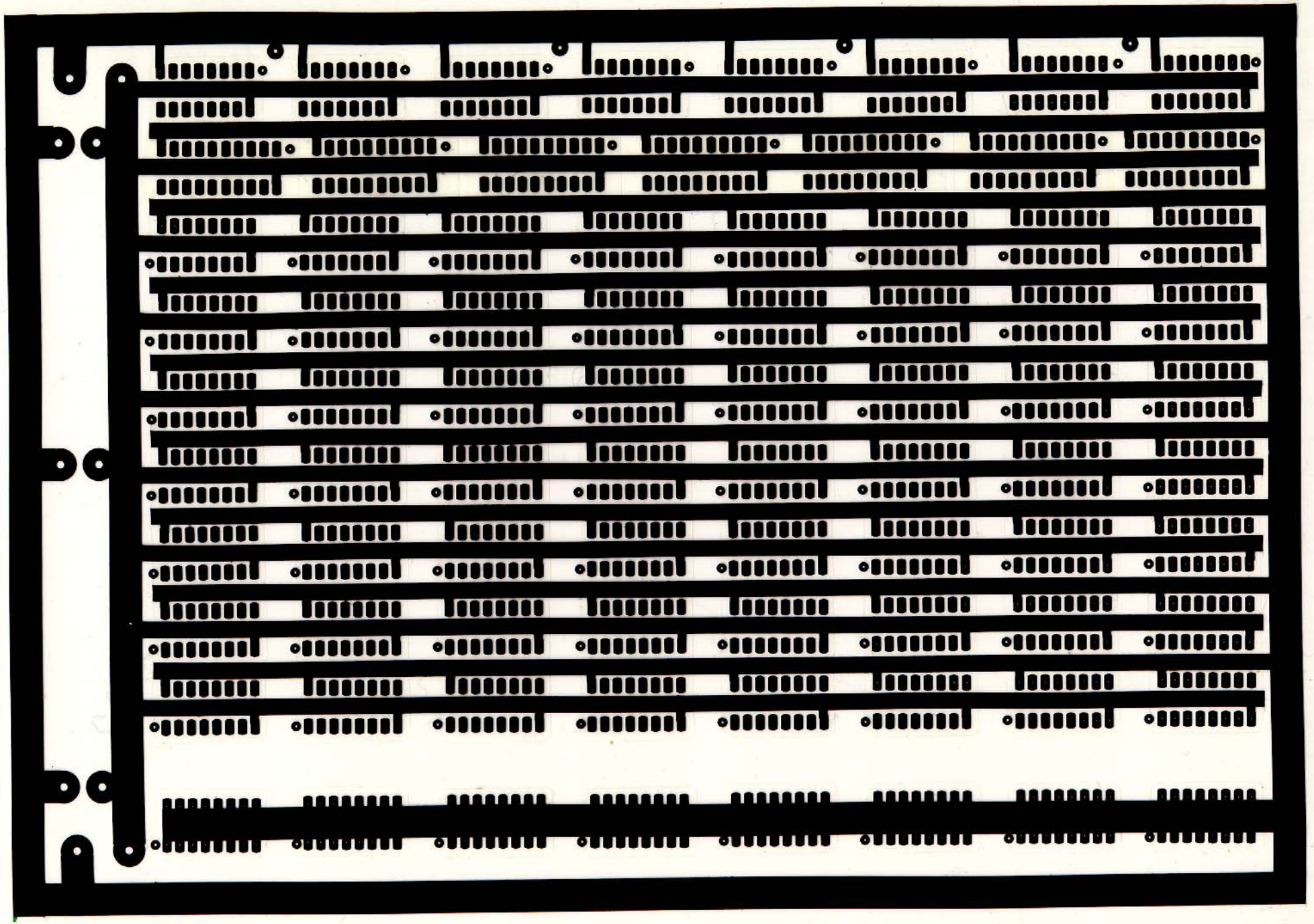
Memory Controller/ECC Bottom / Left
27-Nov-82 ASD



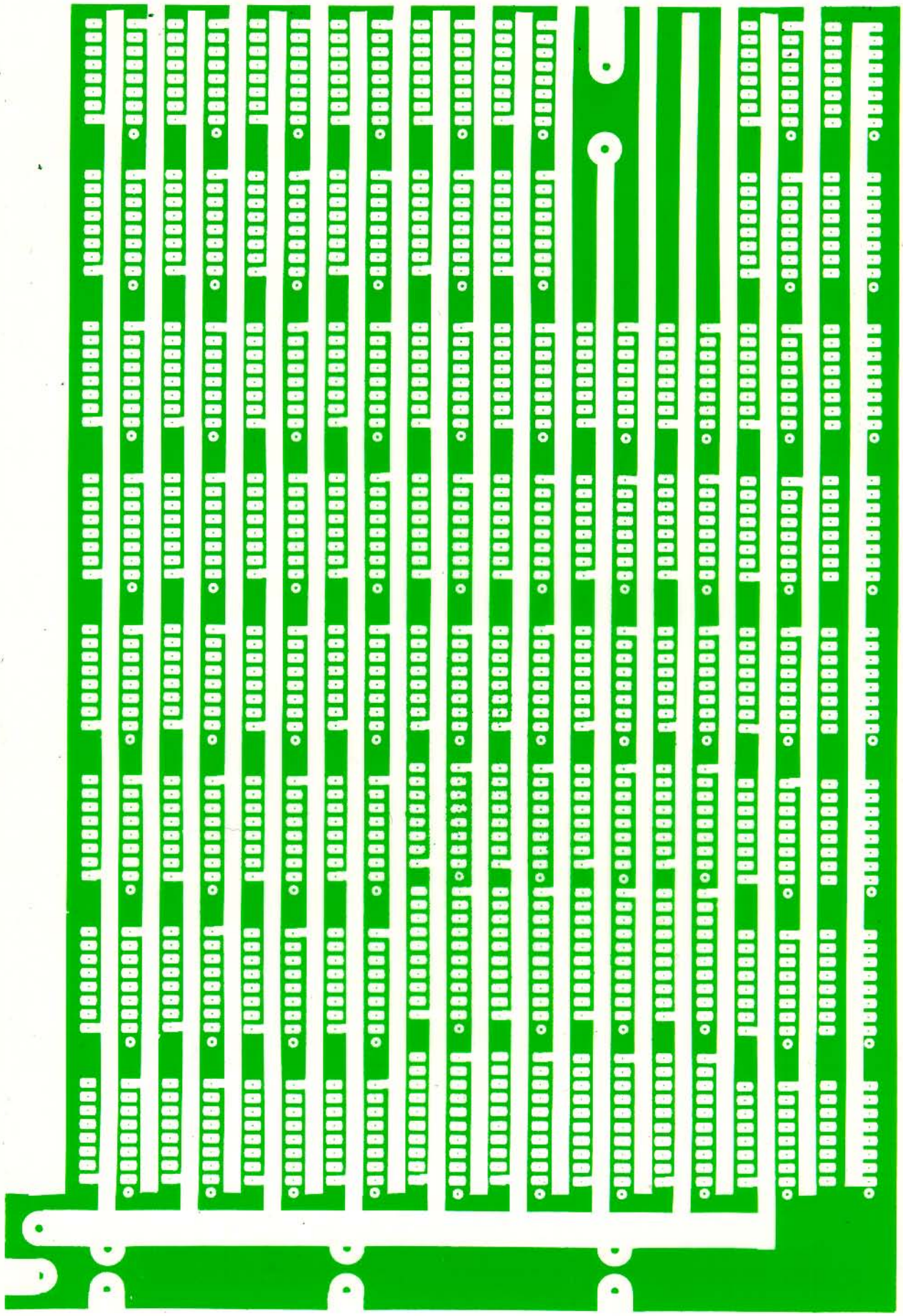
Memory Control/ECC Top/Left 25-Nov-82 ABO

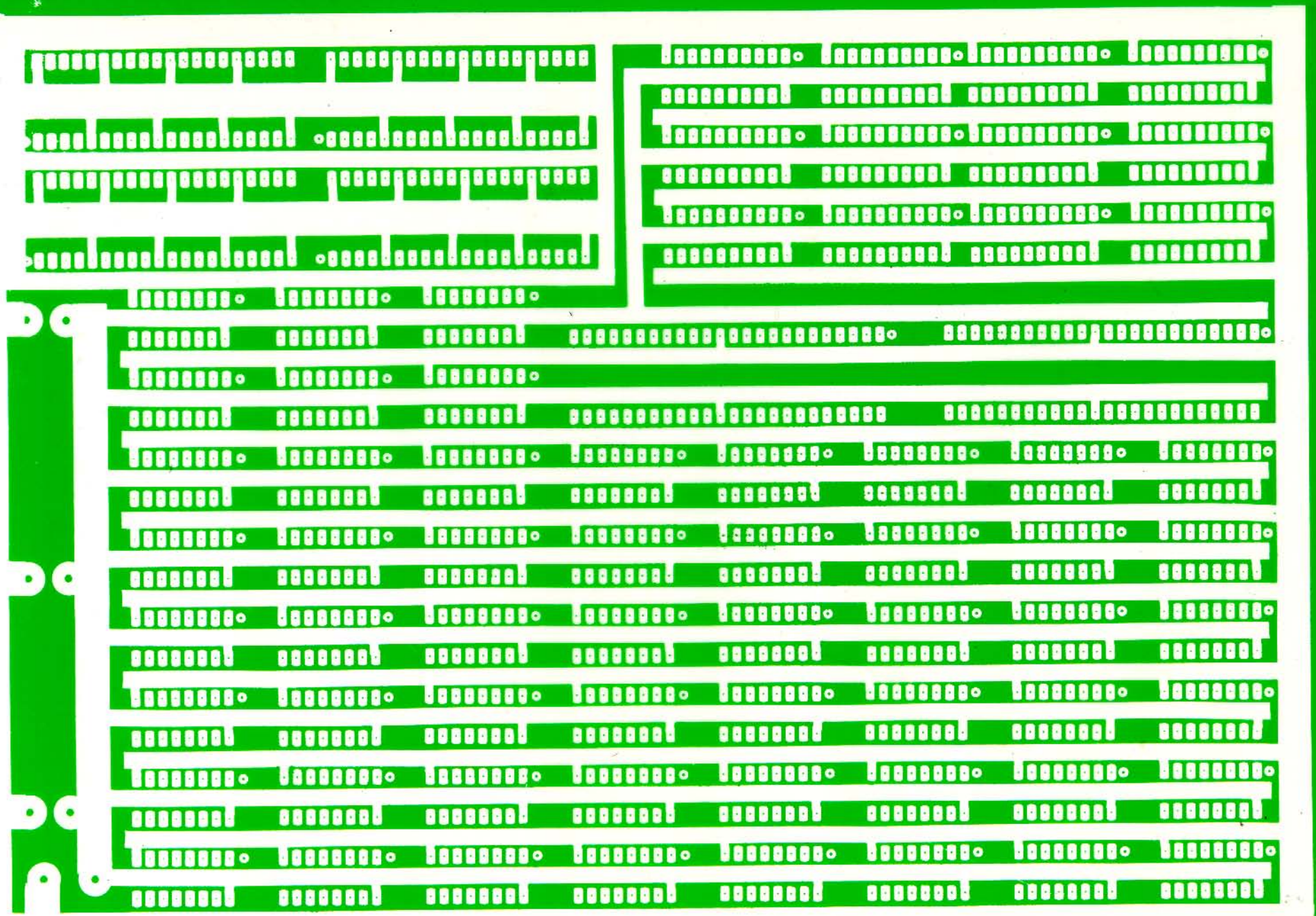


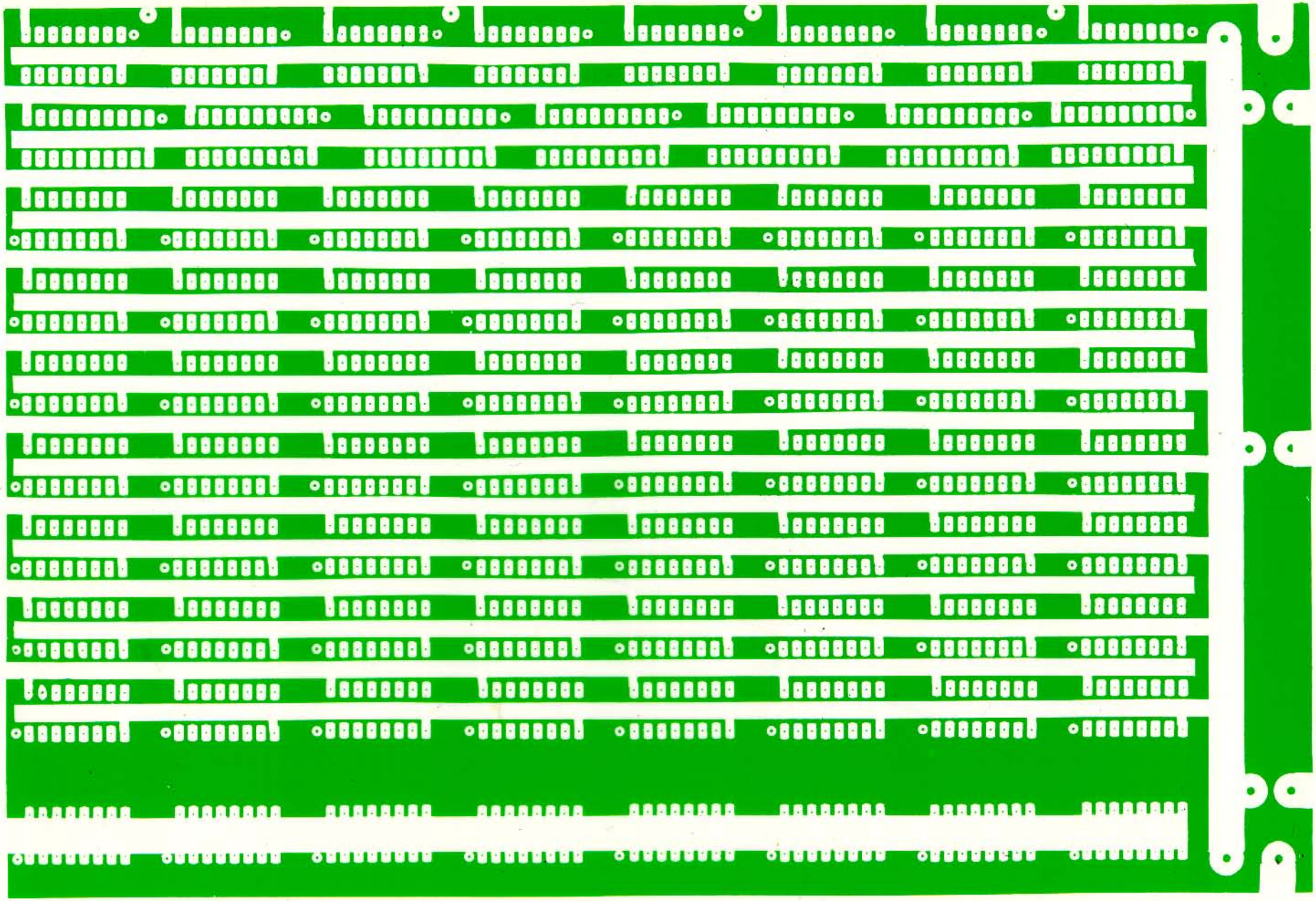
Memory Control/ECC Bottom/Right
25-Nov-82 ARD

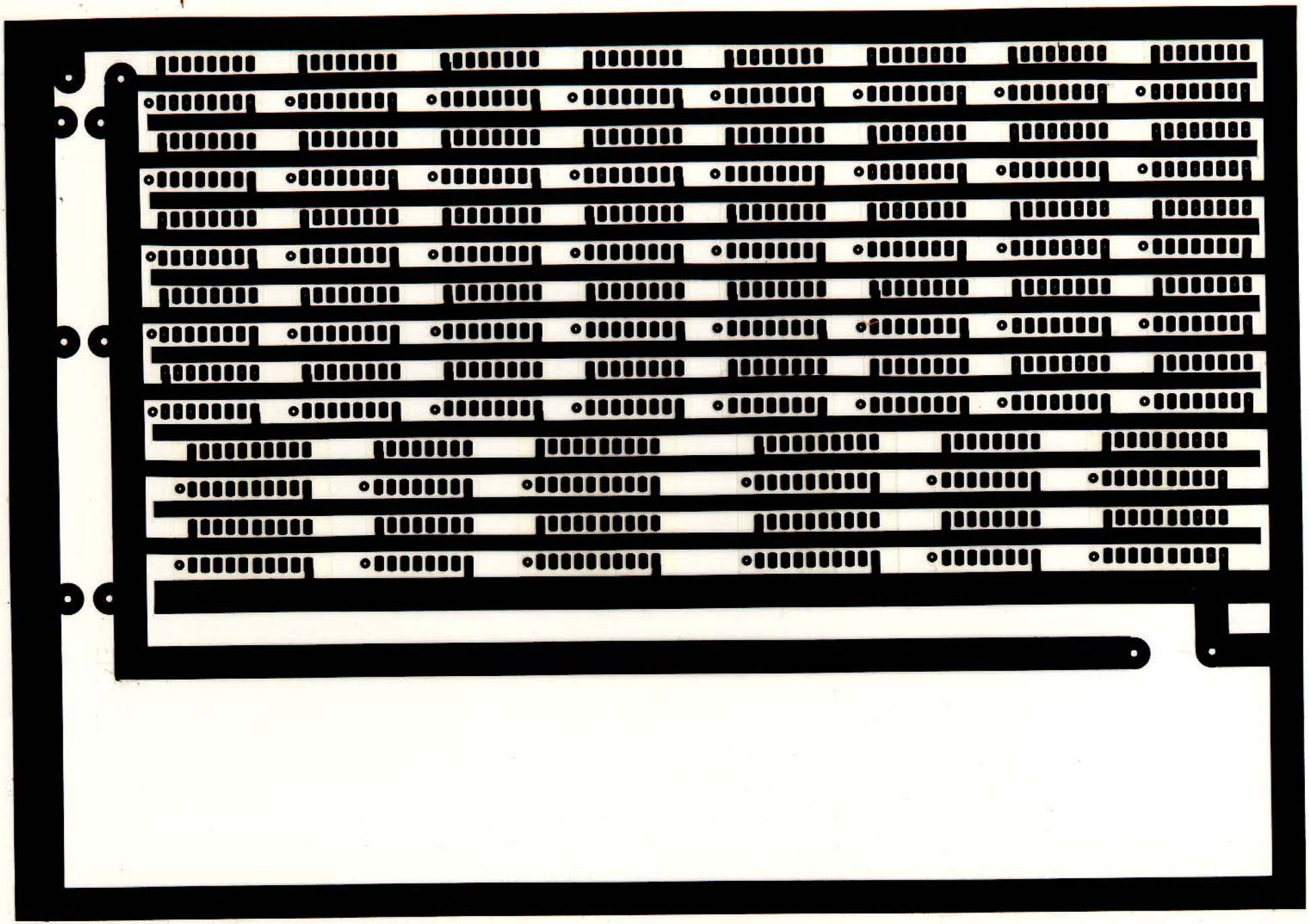


Memory Control/Bac TOP/Right 25-Nov-82 ABB



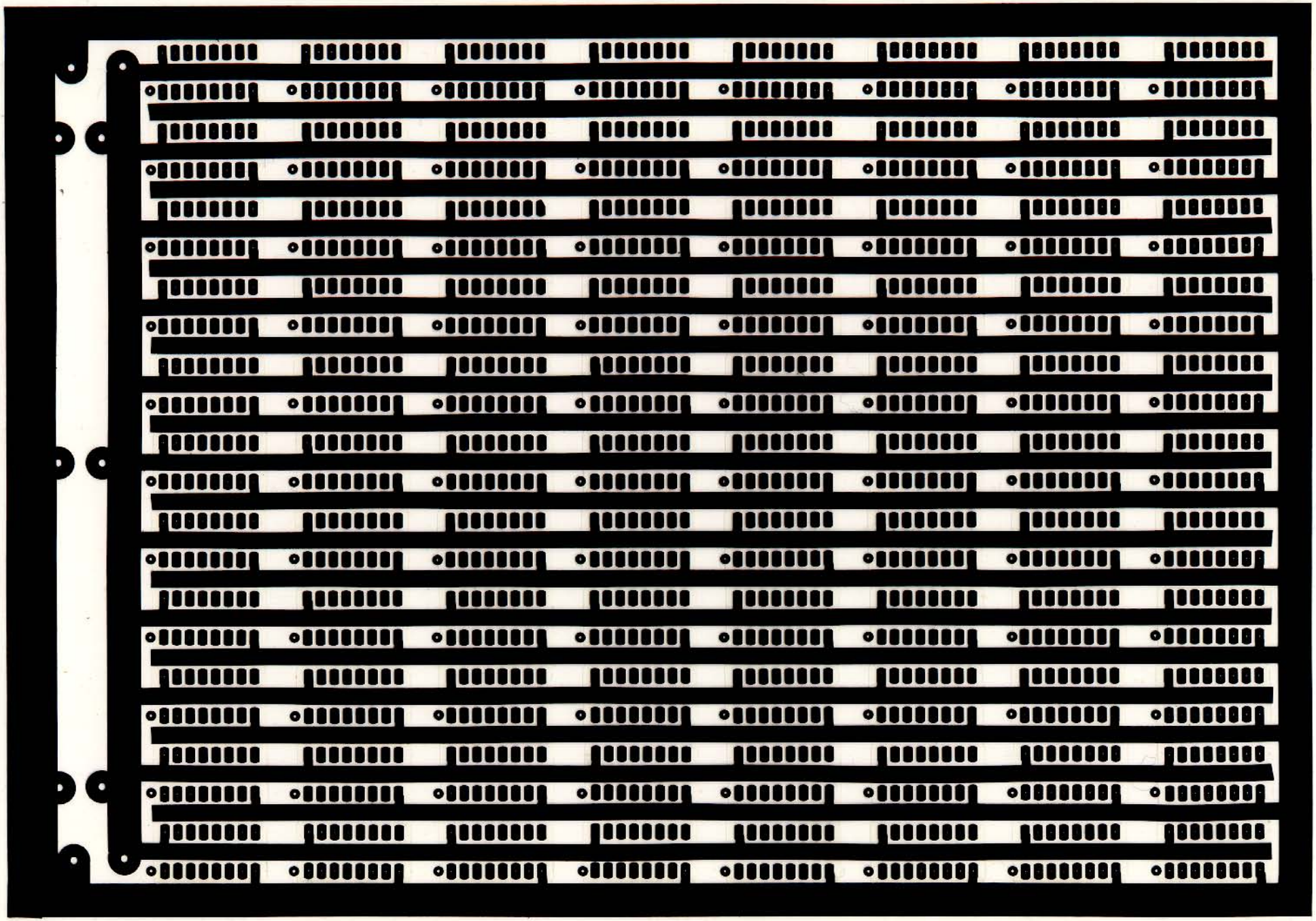




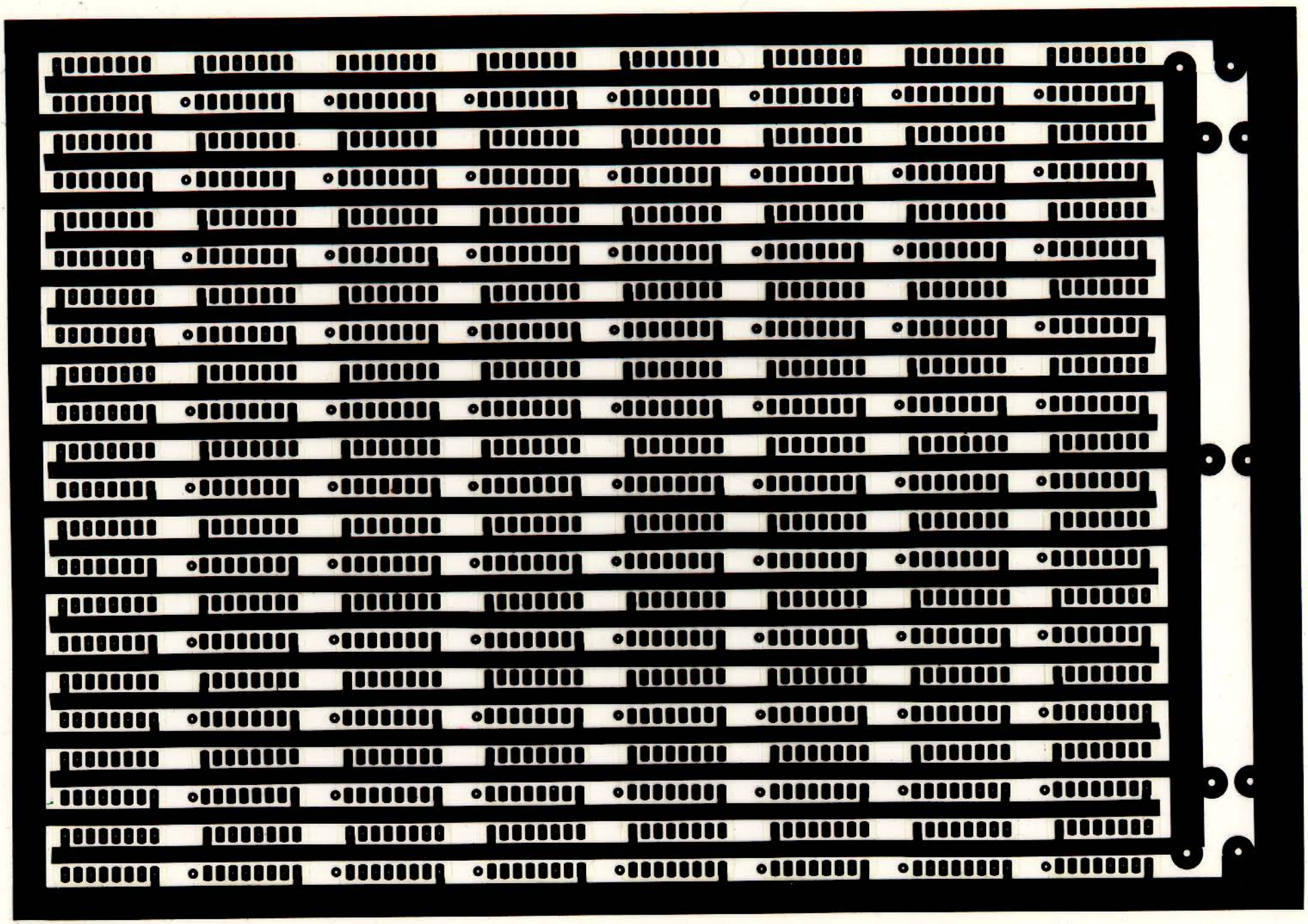


Bottom Left 2-M Byte Board
3 Sept 82 ARO

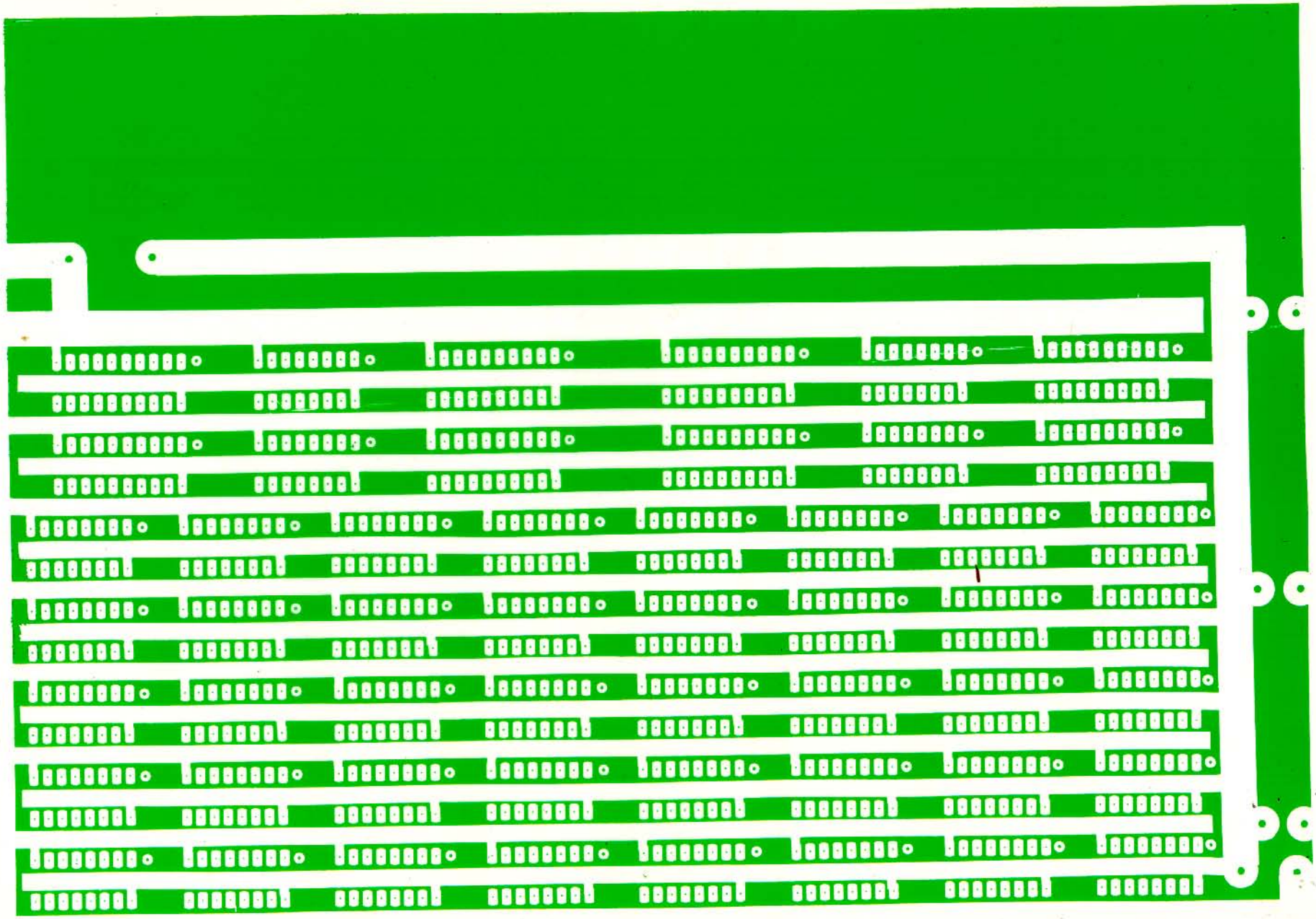
Top-Left Sub-Board 5 Sept 82 Rev

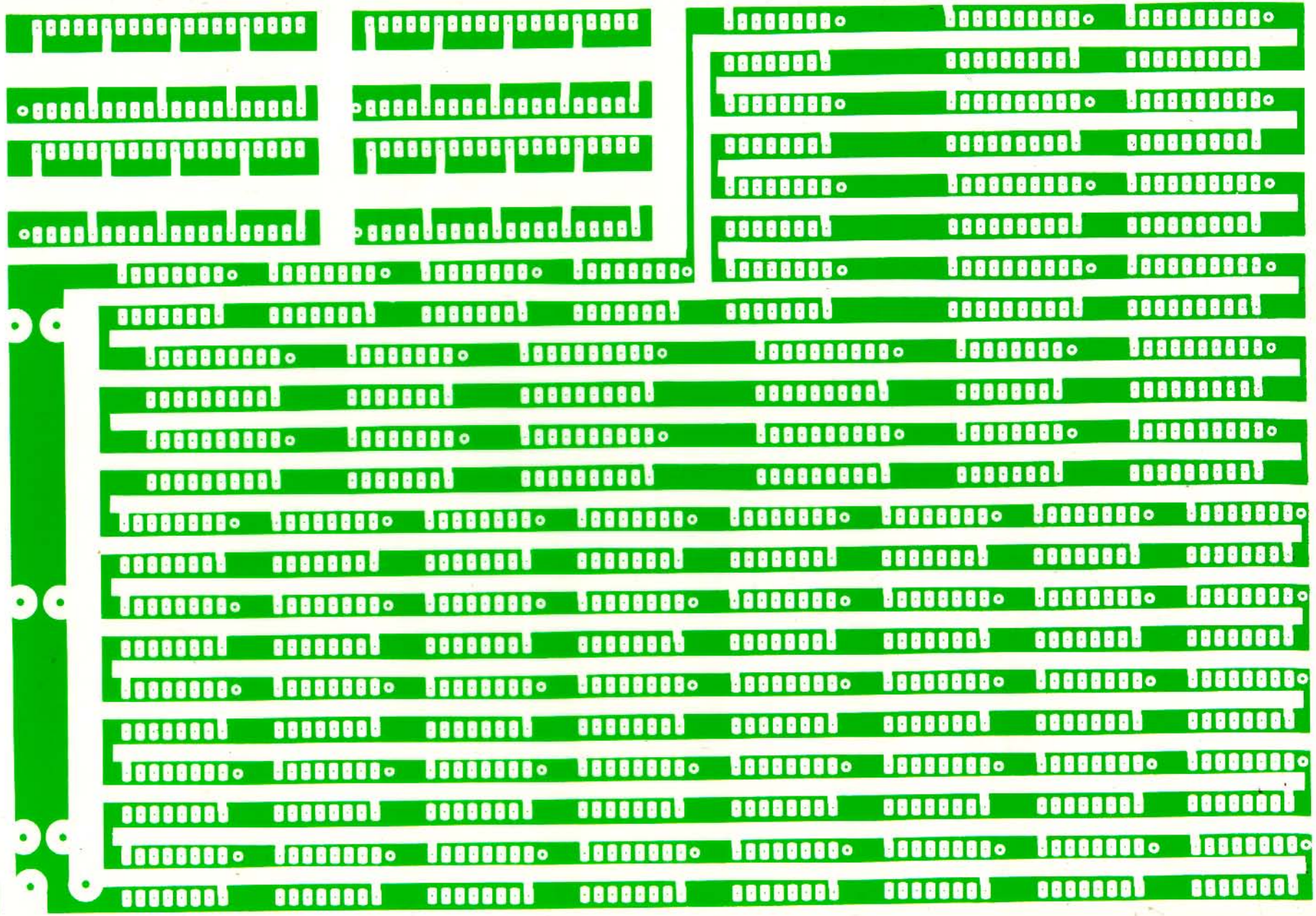


2 M-Byte Board Bottom-Right Sect.n
31 Aug 82 AD

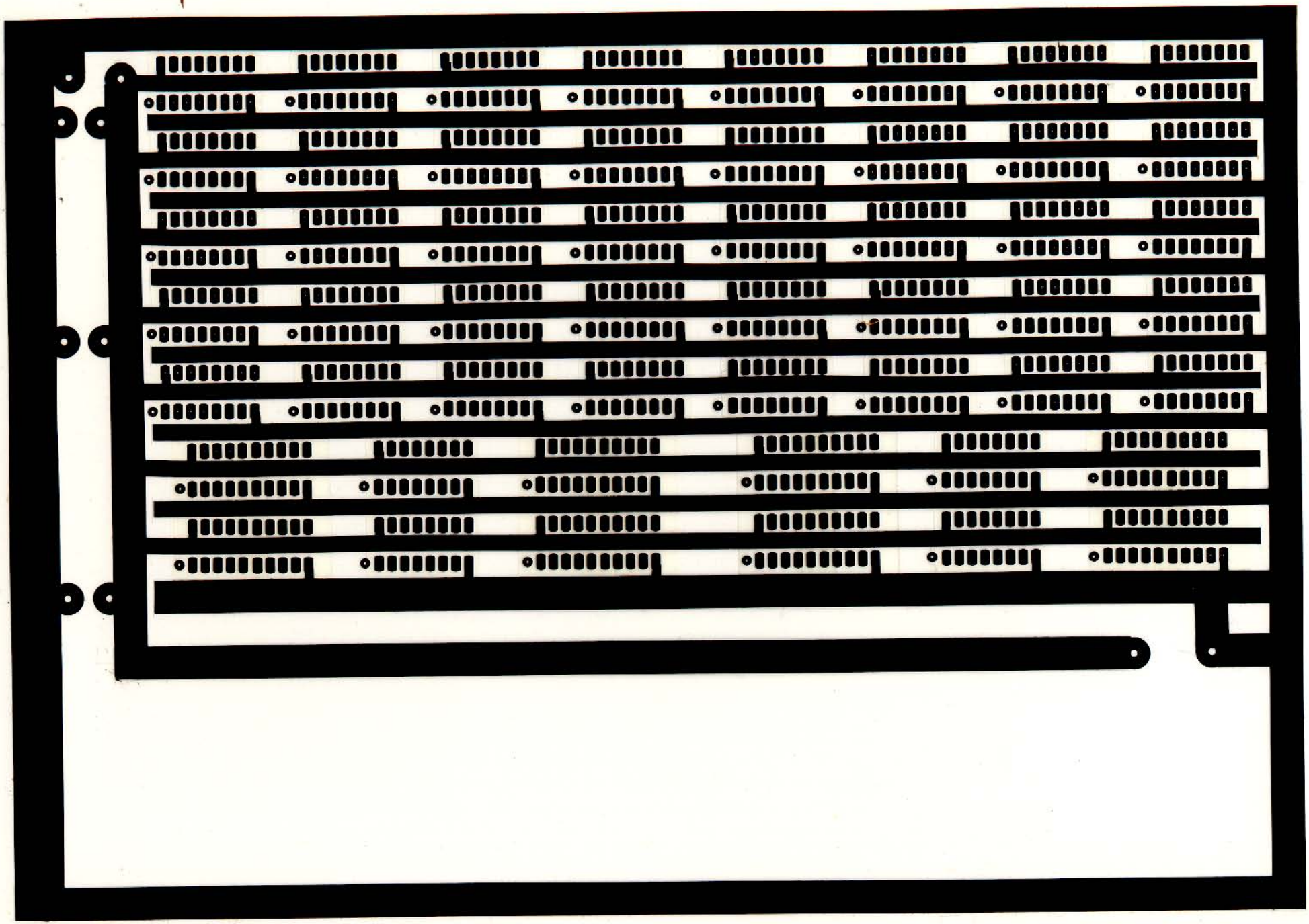


2 M-Byte Board Top-Right Section
31 Aug 82 AMD



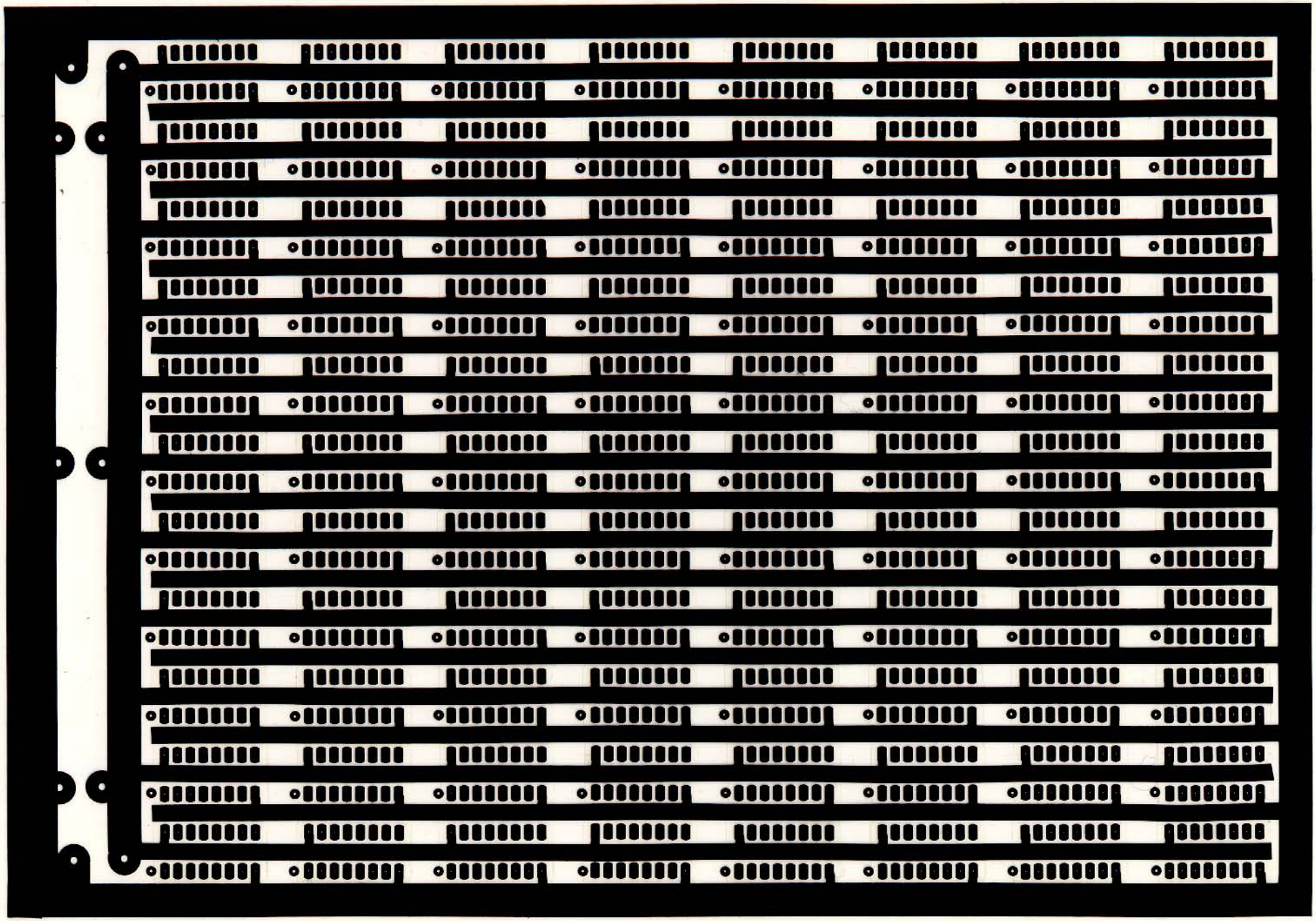


813, 660, 330
NOTES
FEED ↑ UP
MODEL 914, 720, 420, 2400

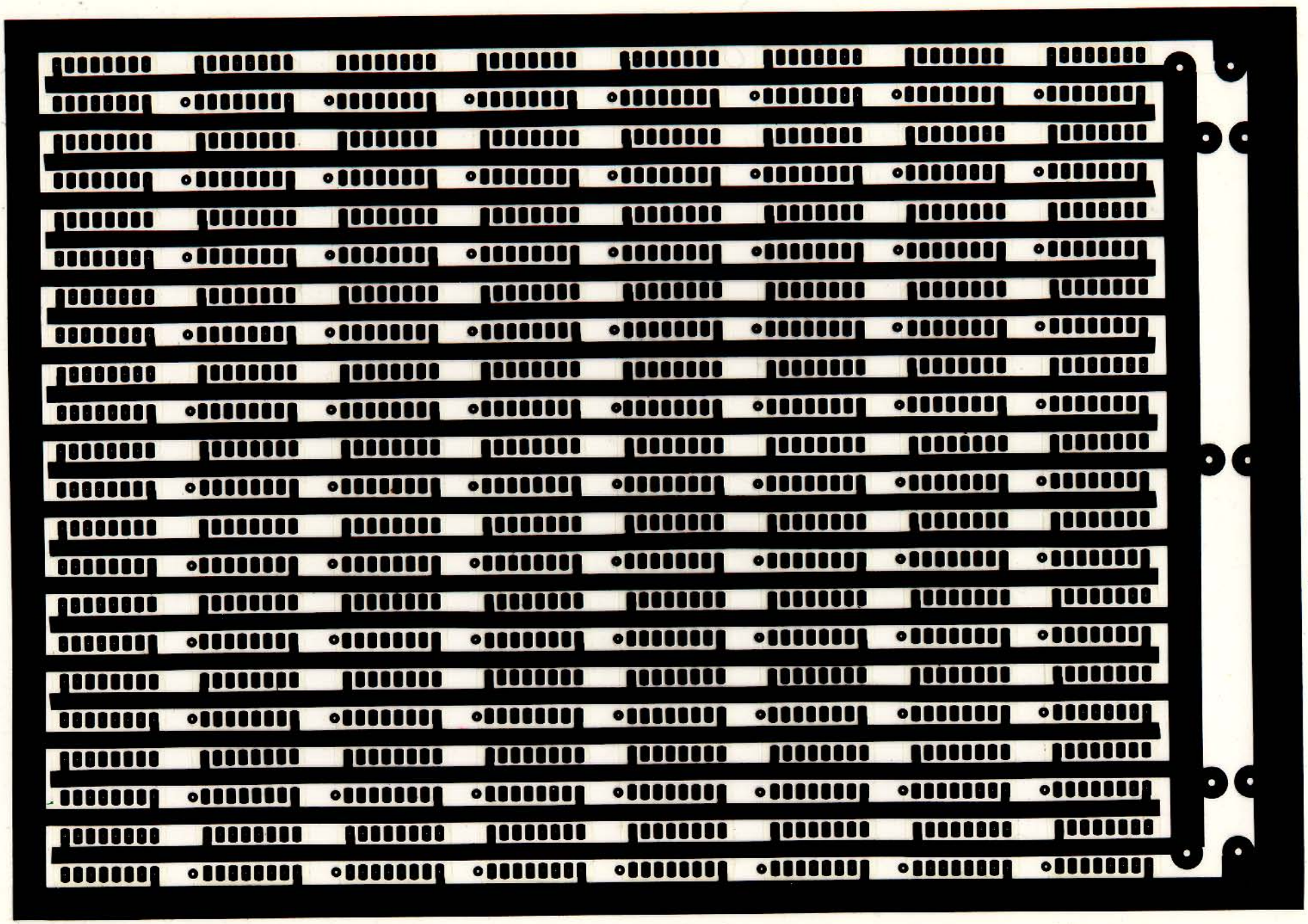


Bottom Left 2-M Byte Board
3 Sept 82 ARO

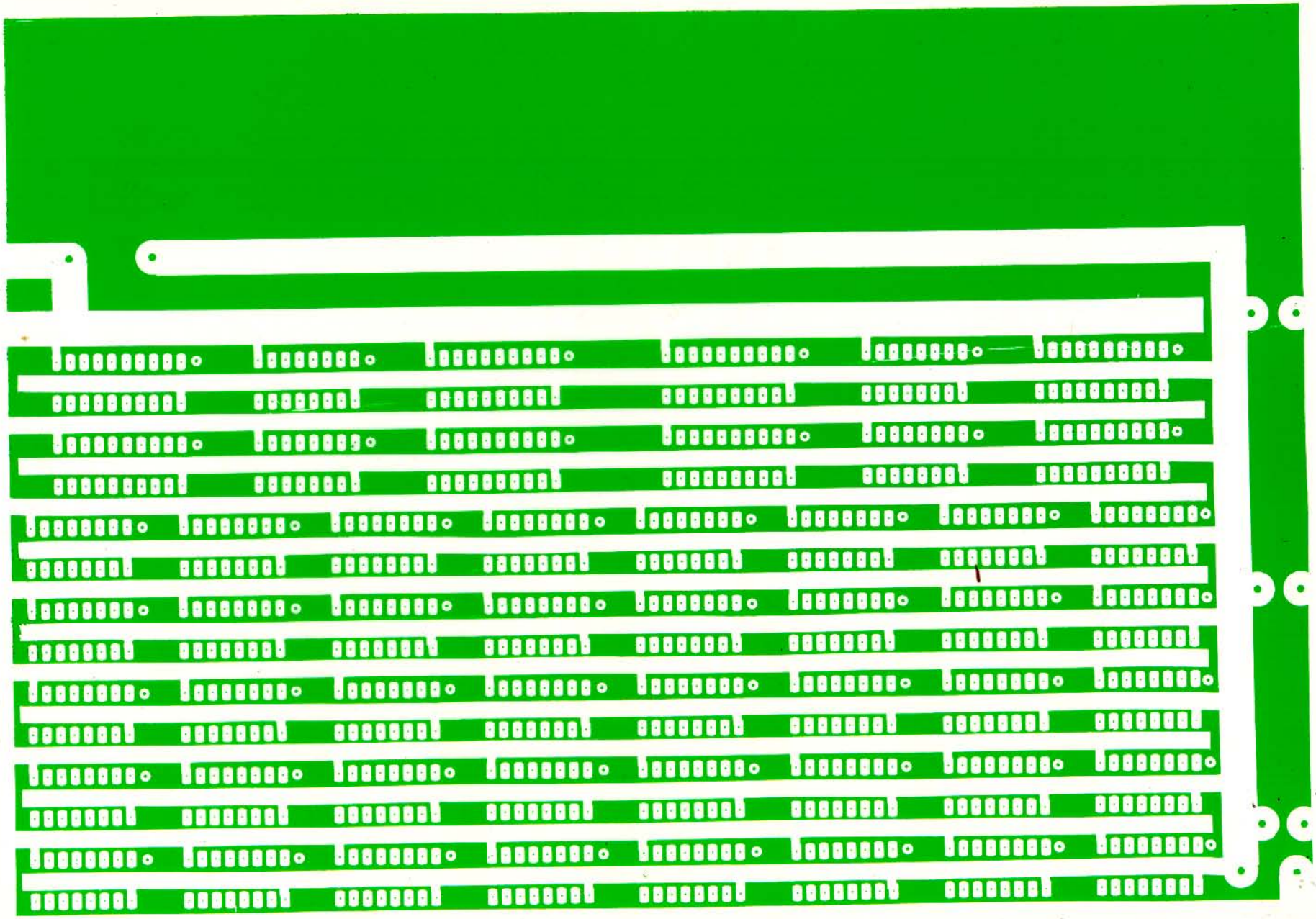
Top-Left Sub-Board 5 Sept 82 Rev

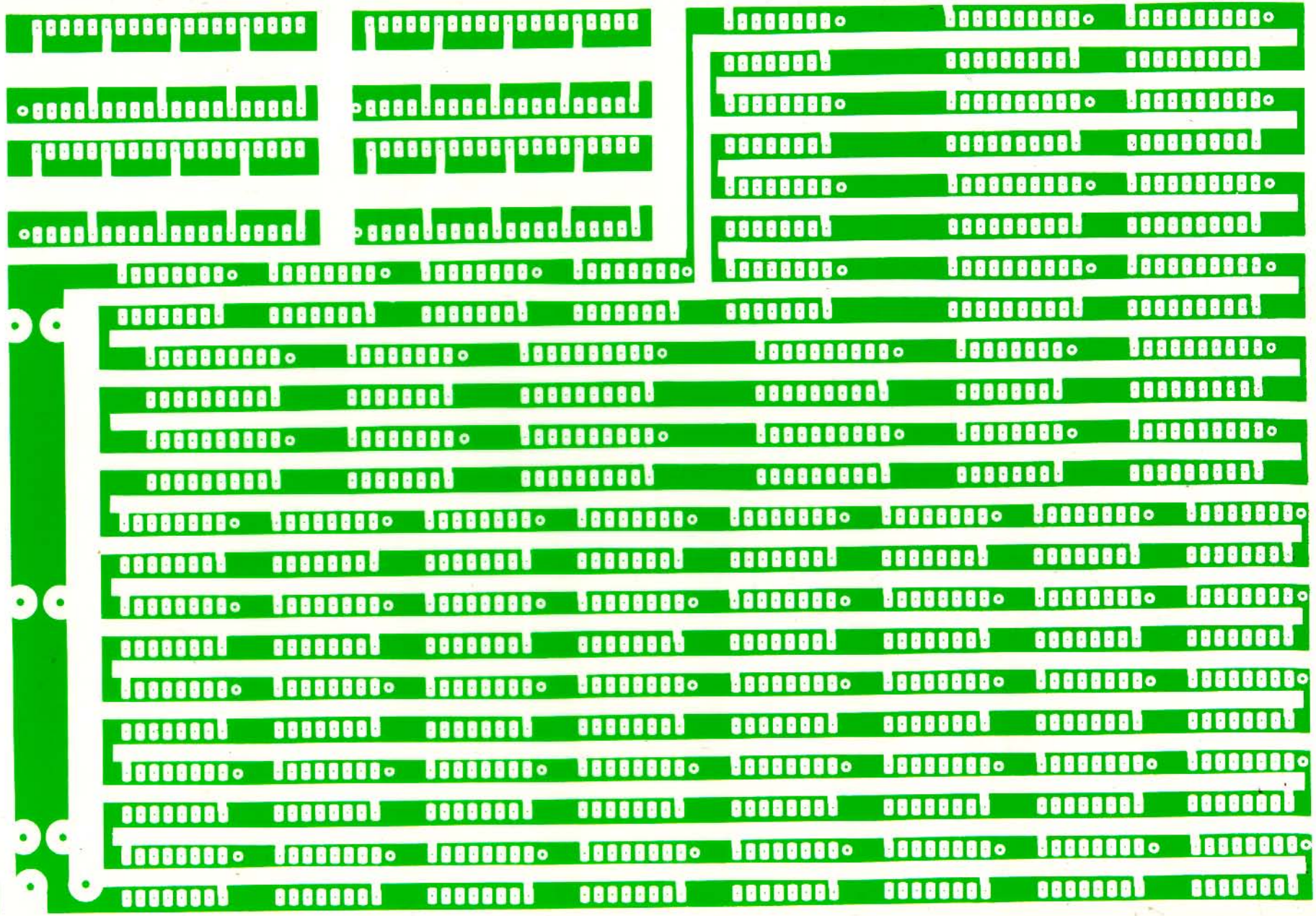


2 M-Byte Board Bottom-Right Sect.n
31 Aug 82 AD



2 M-Byte Board Top-Right Section
31 Aug 82 AMD



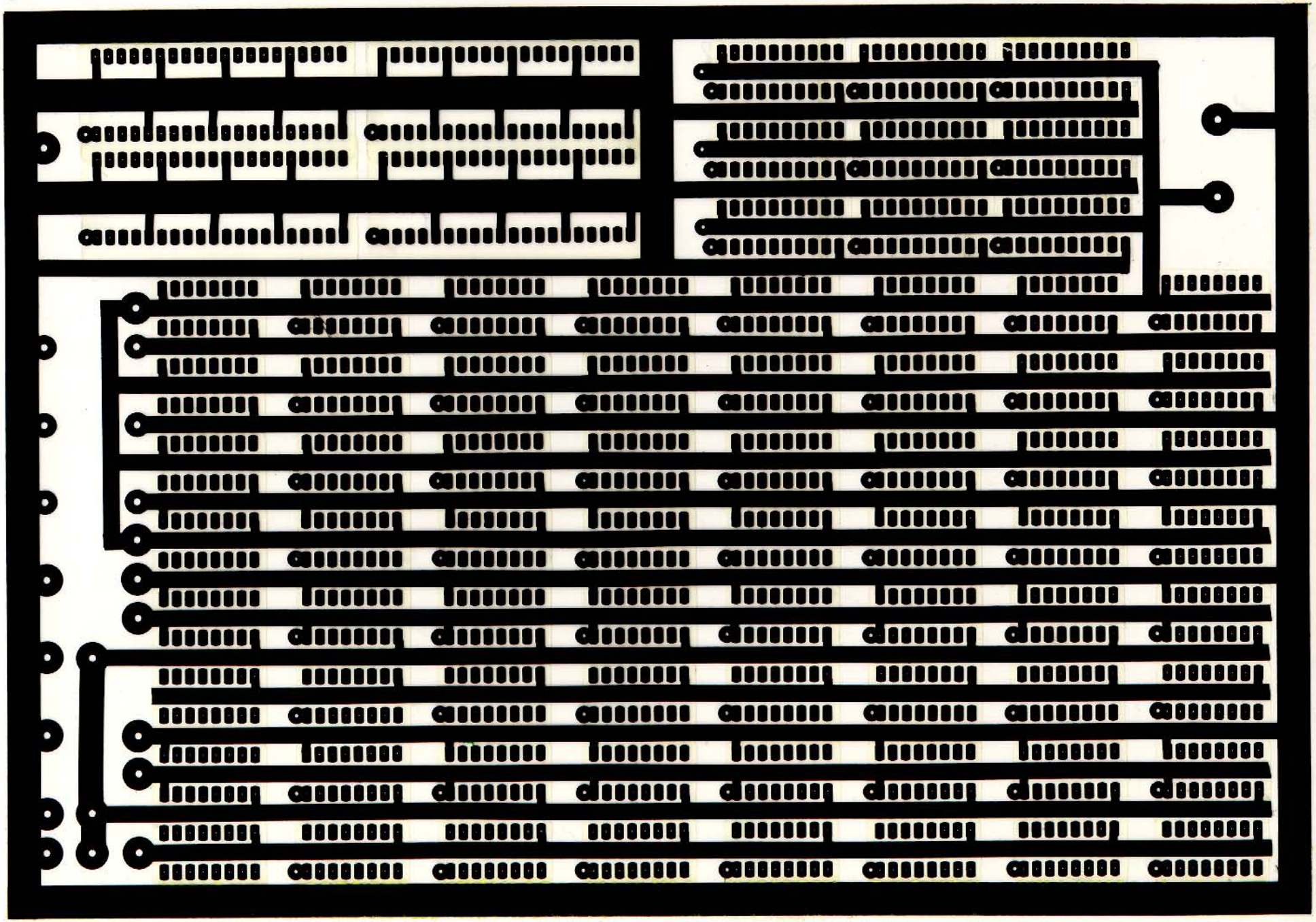


813, 660, 330
NOTES
FEED ↑ UP
MODEL 914, 720, 420, 2400

L1 Memory

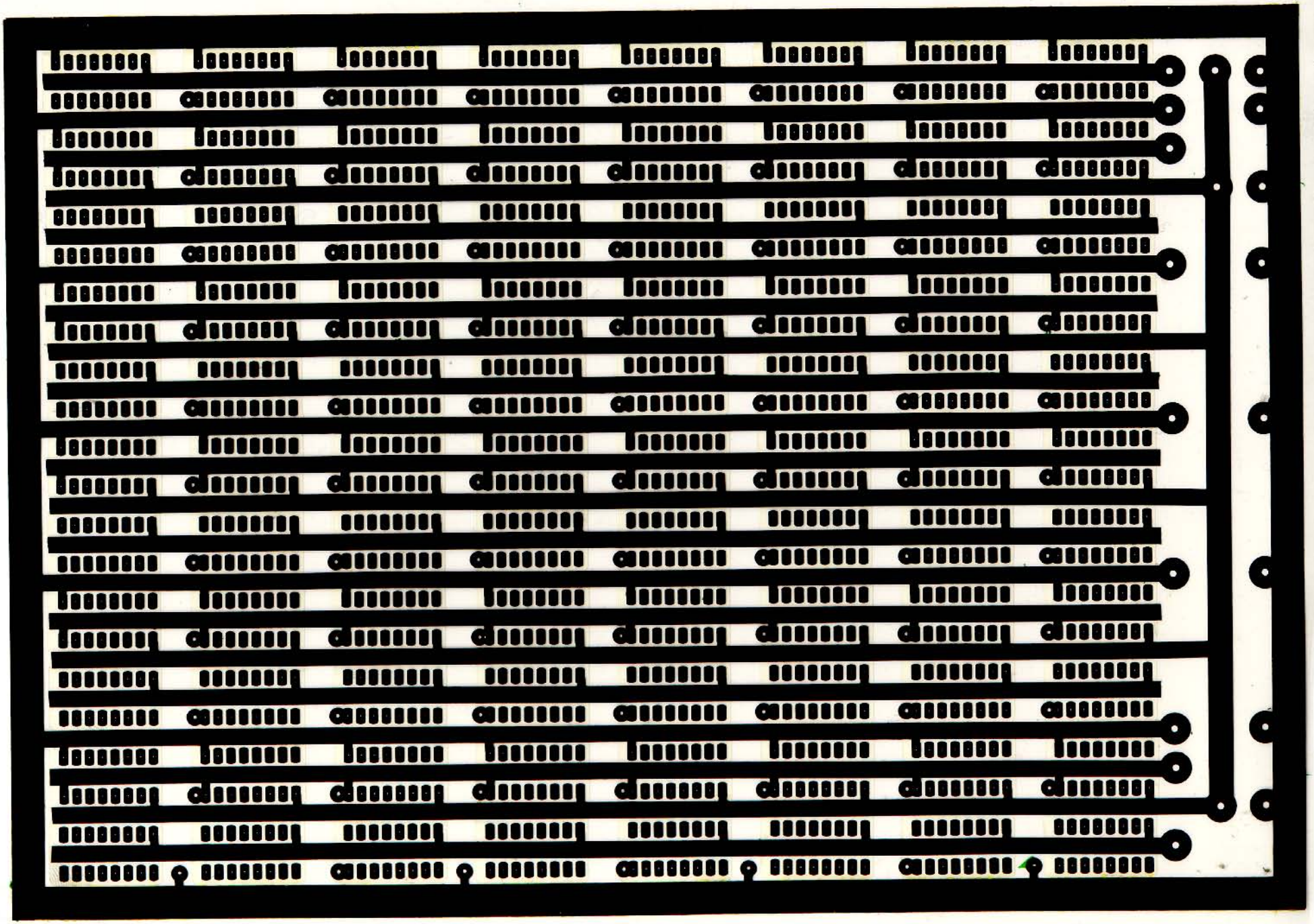
Gary
8-8-78

R1 Memory 22Feb78 ABD

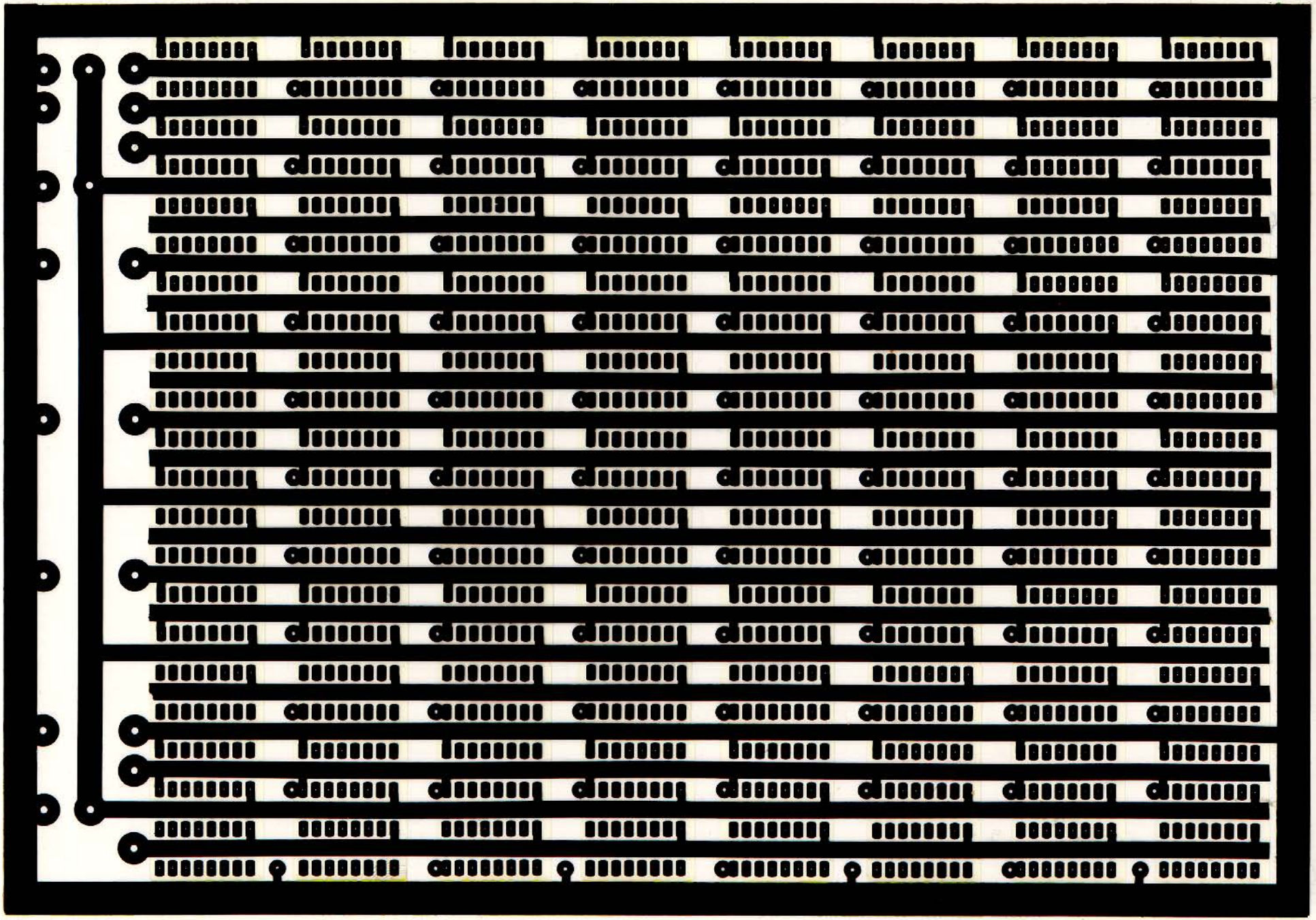


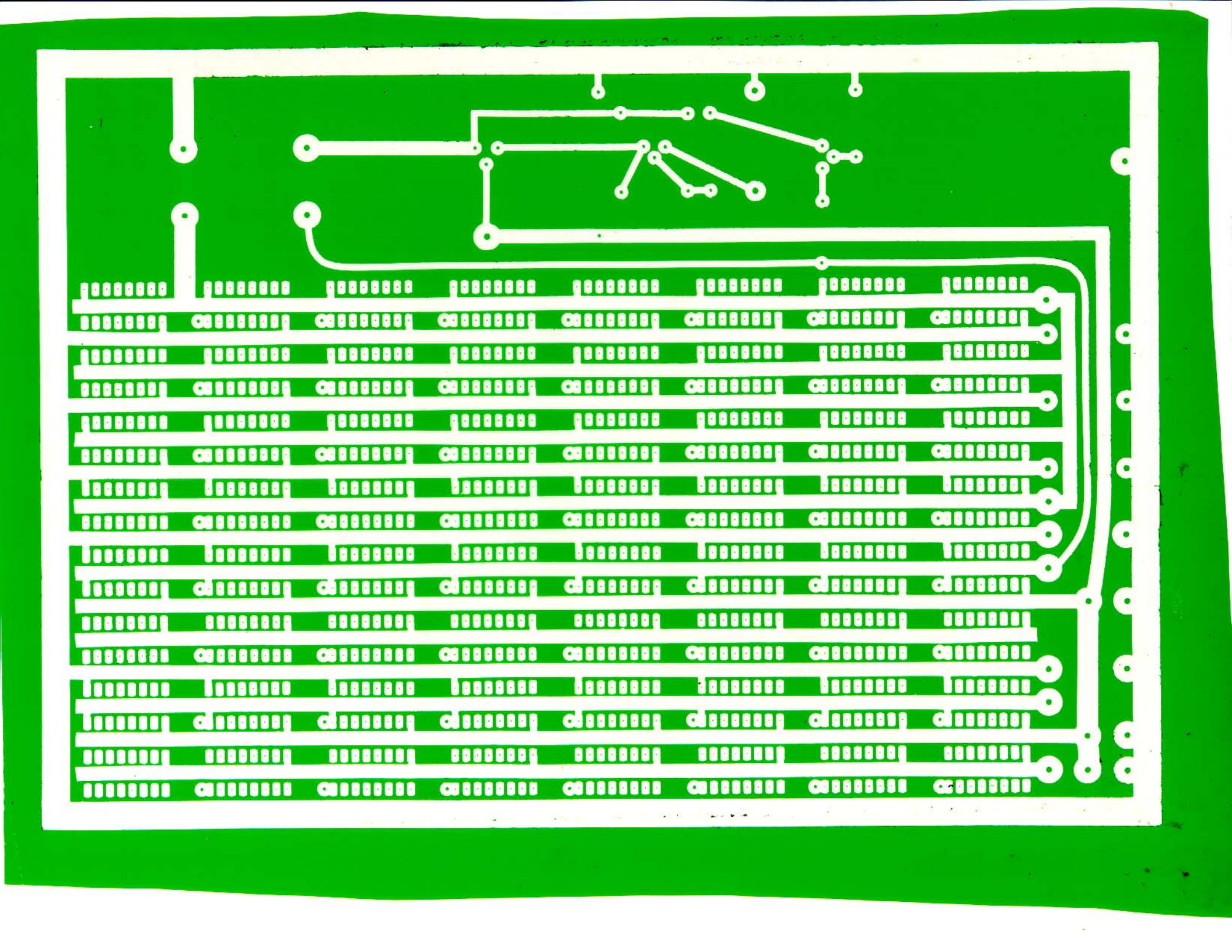
L2 Memory

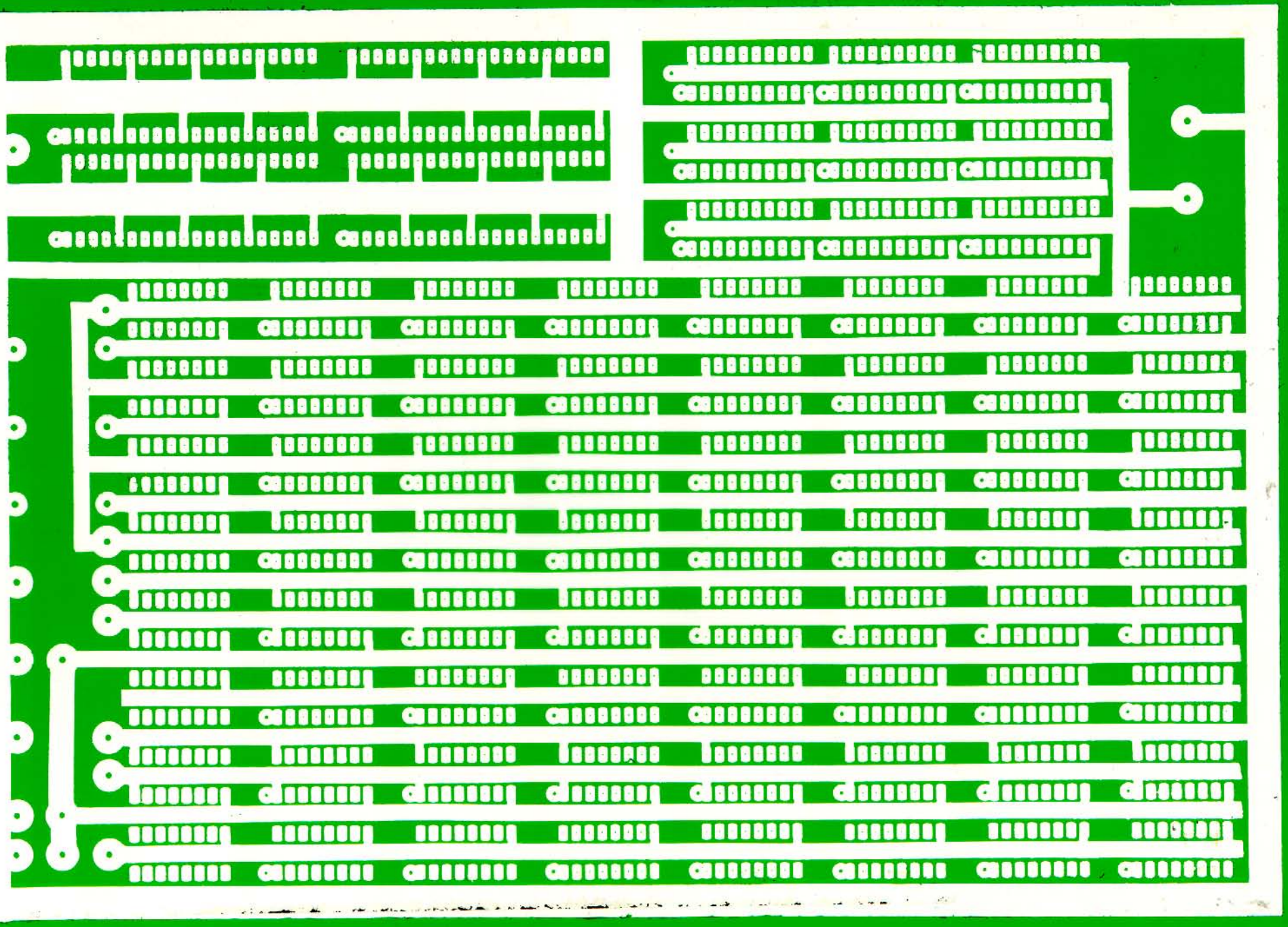
21 Feb 78
HCD

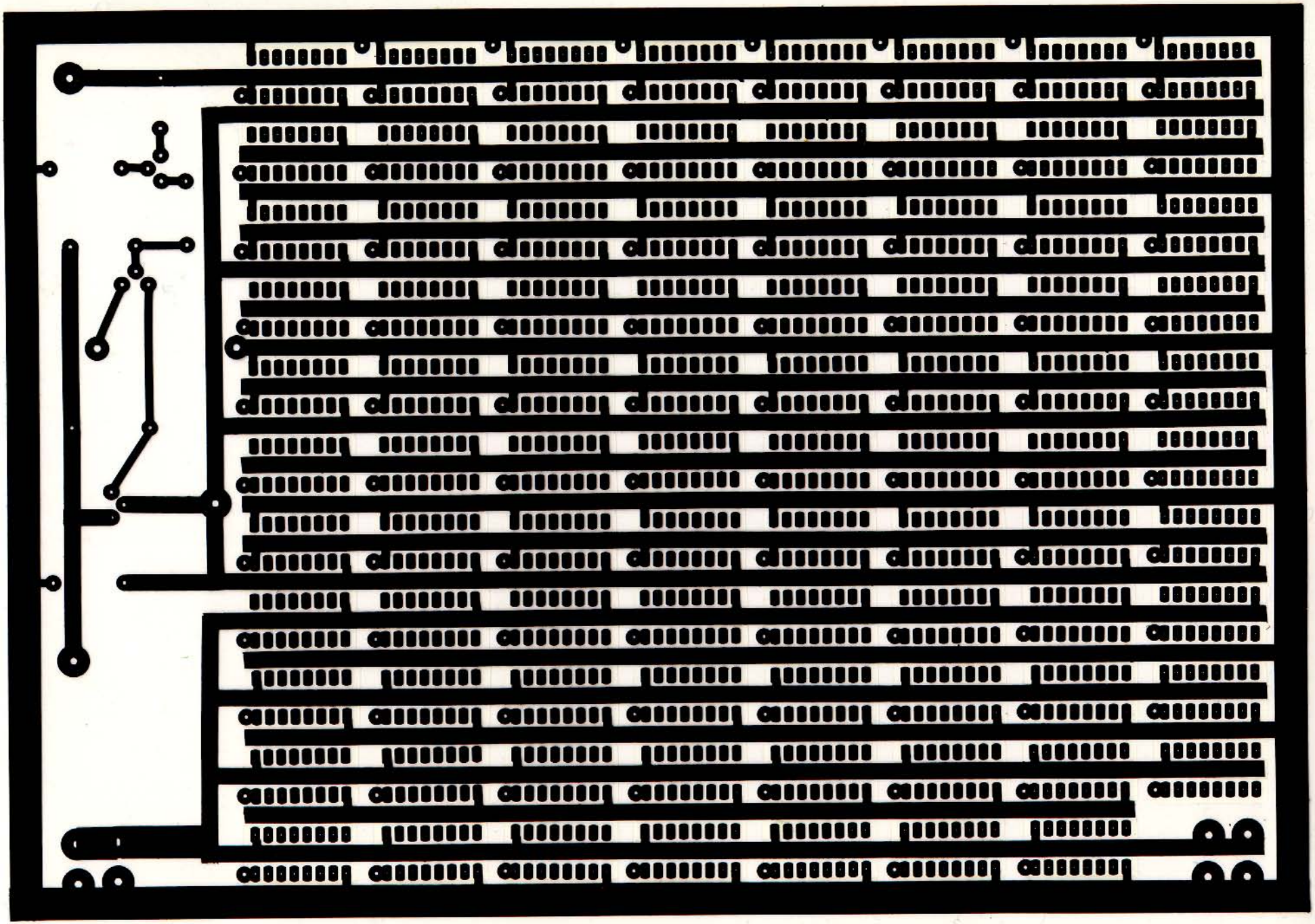


R2 Memory 22 Feb 78 ABB

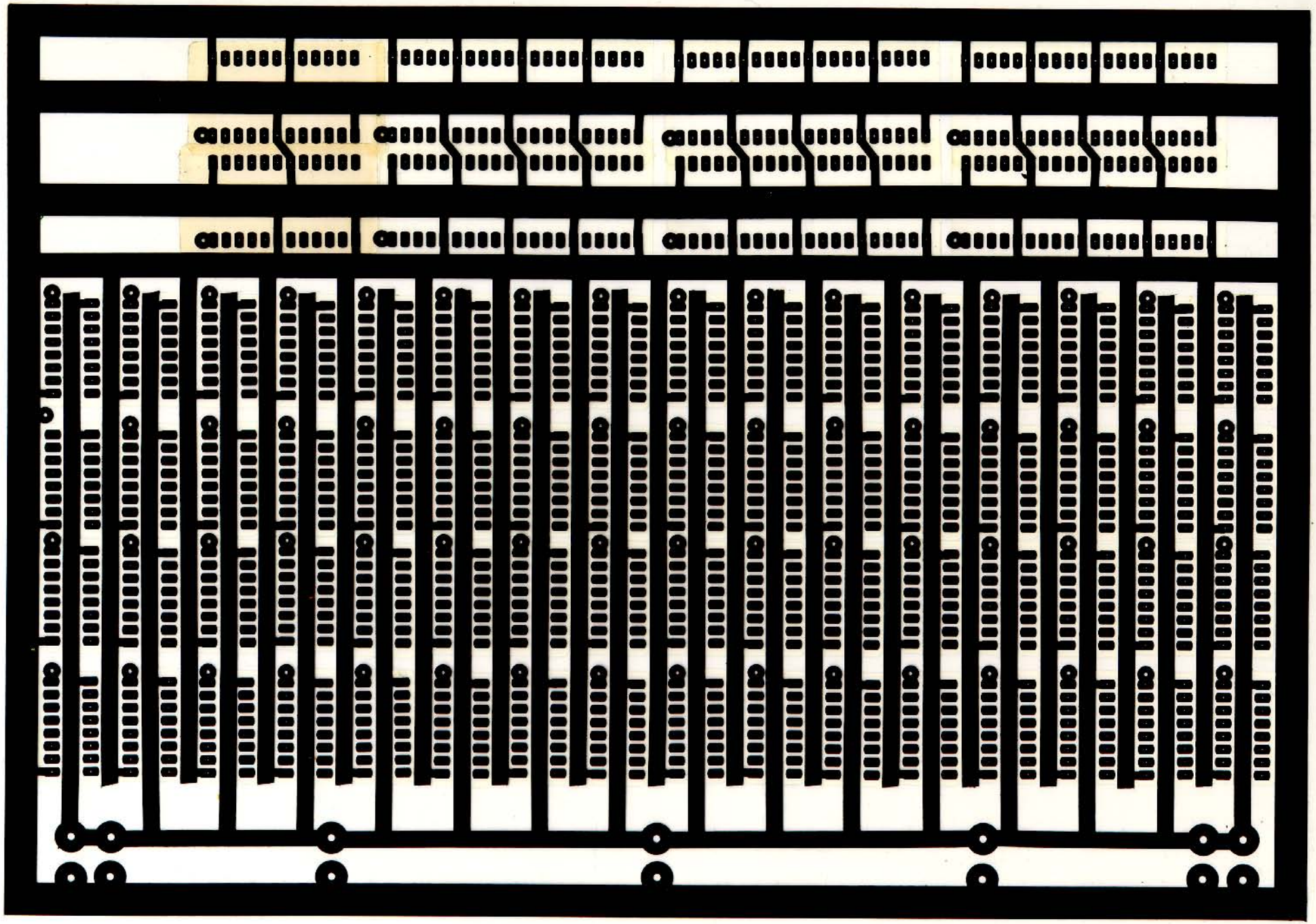




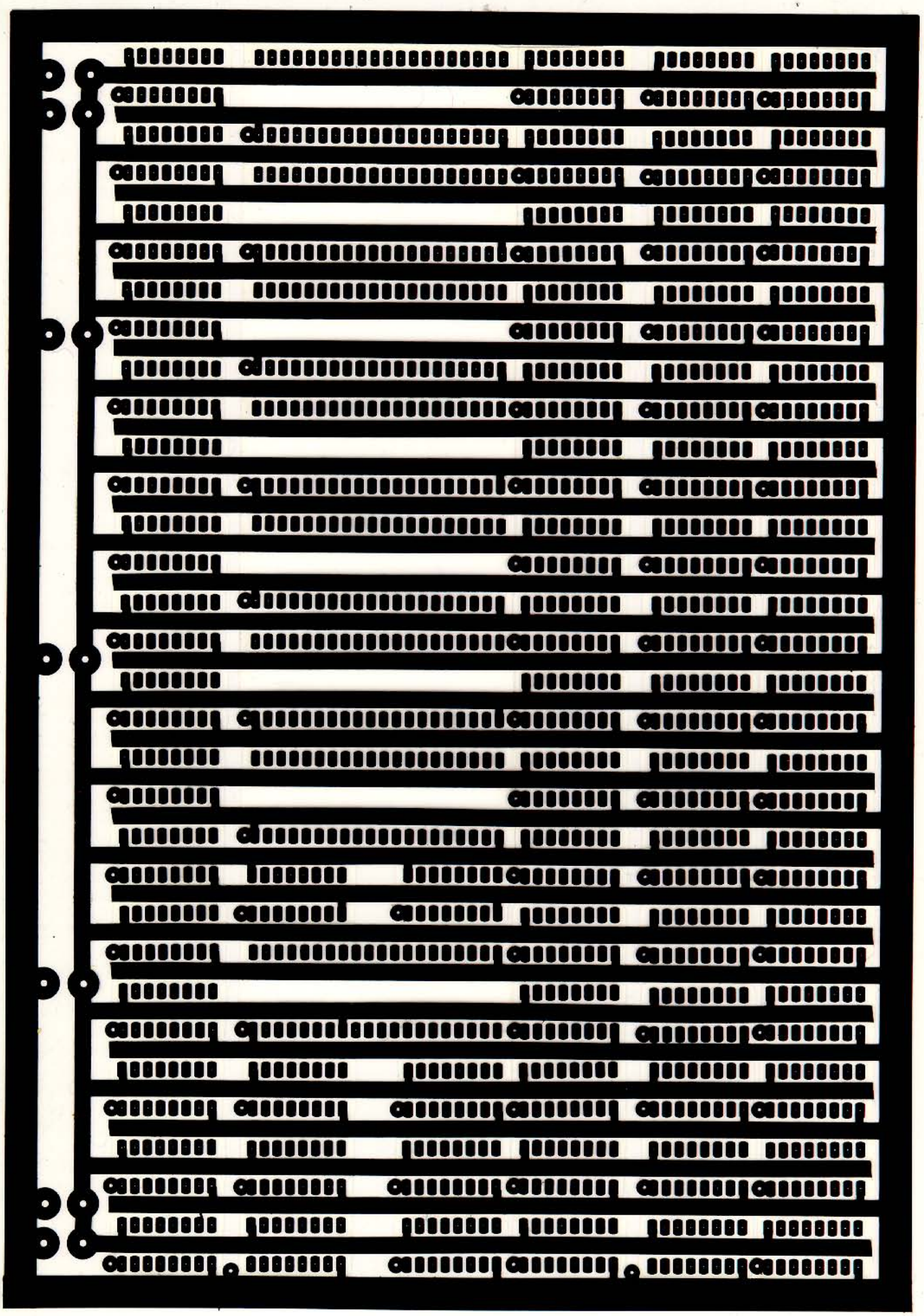


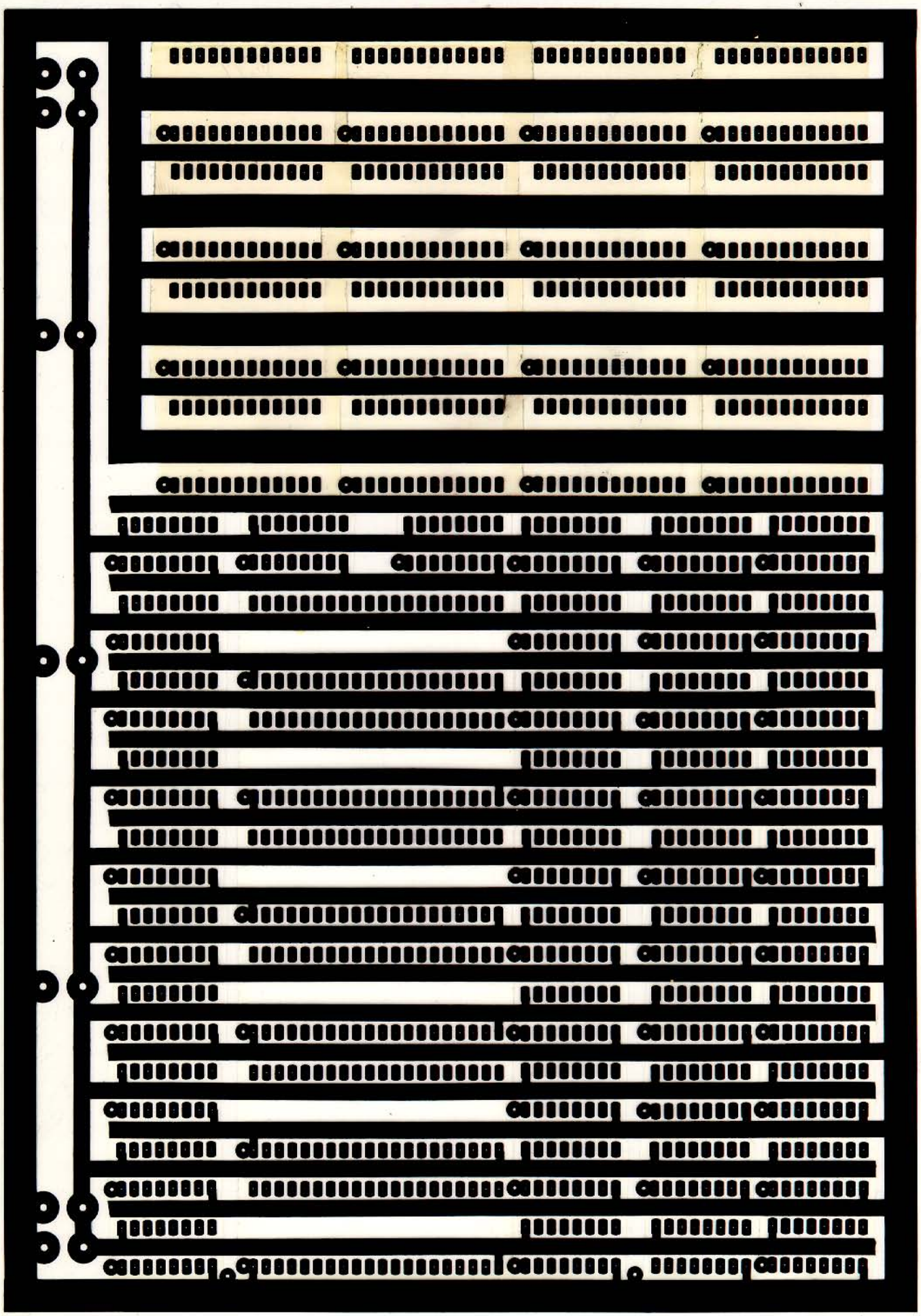


Keyboard/Display Memory

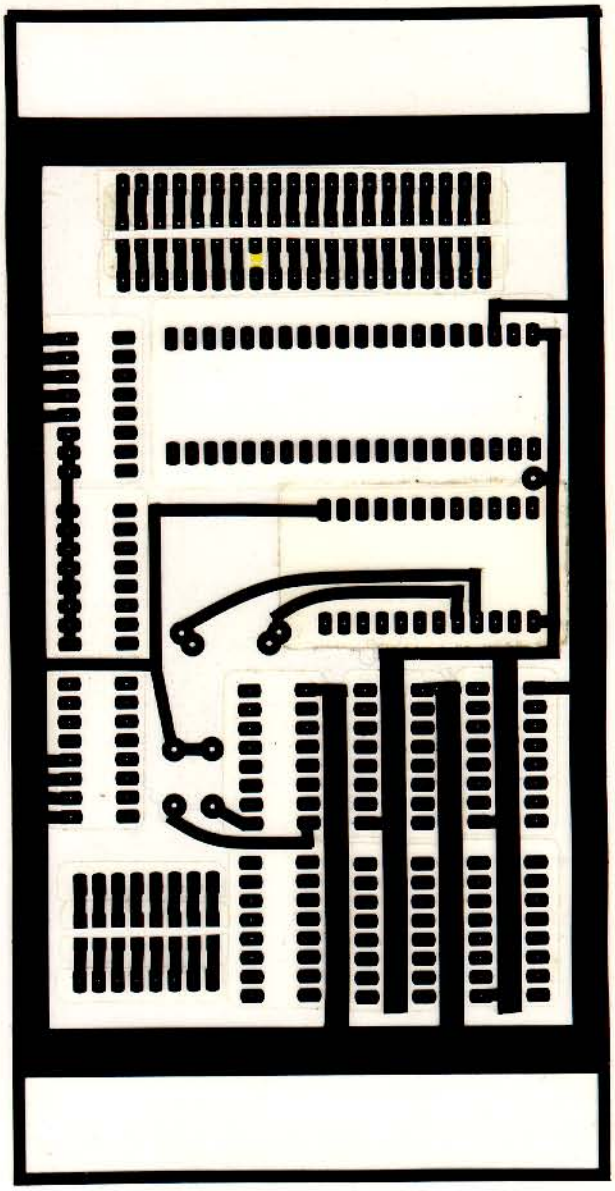


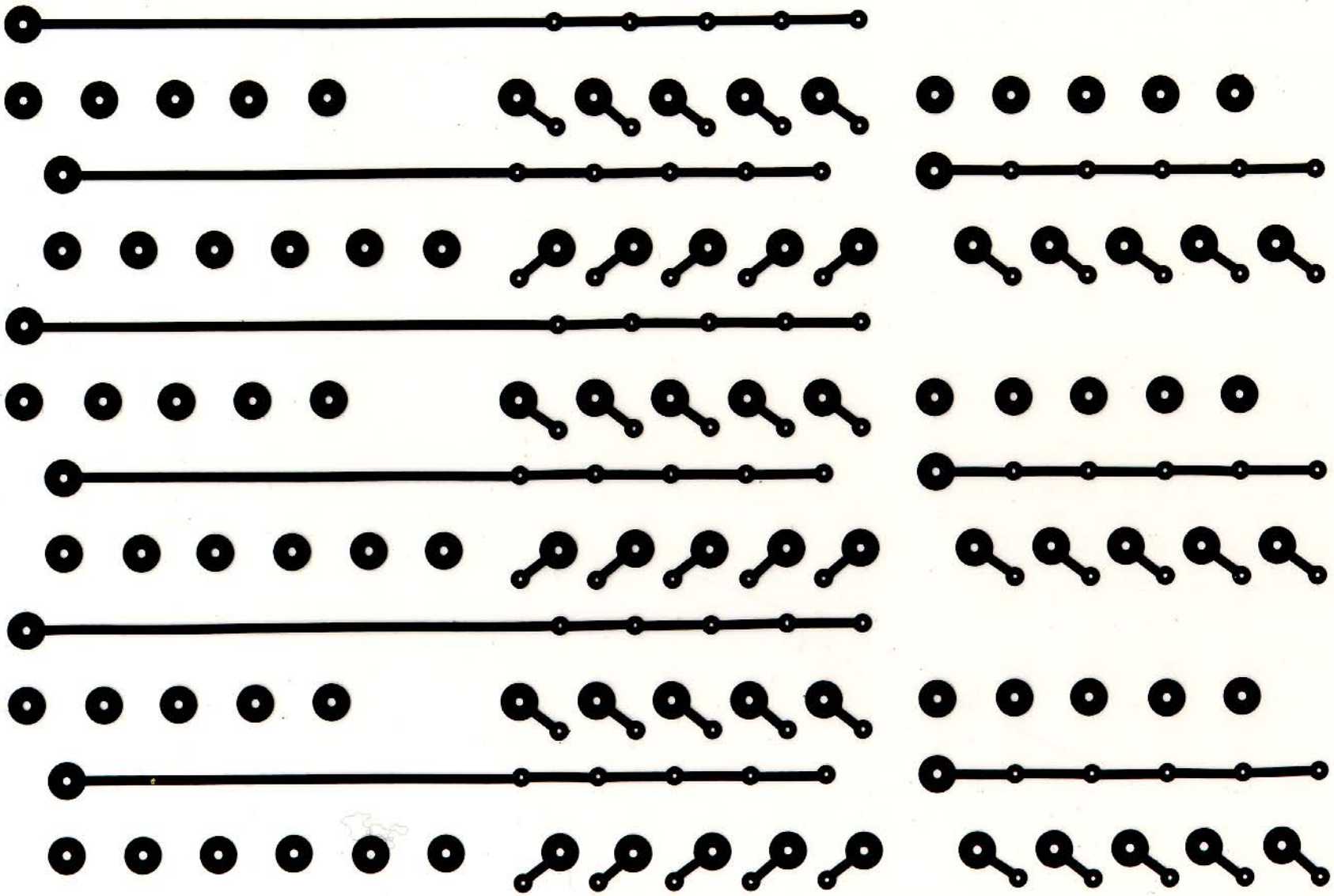
DSP Box I/O

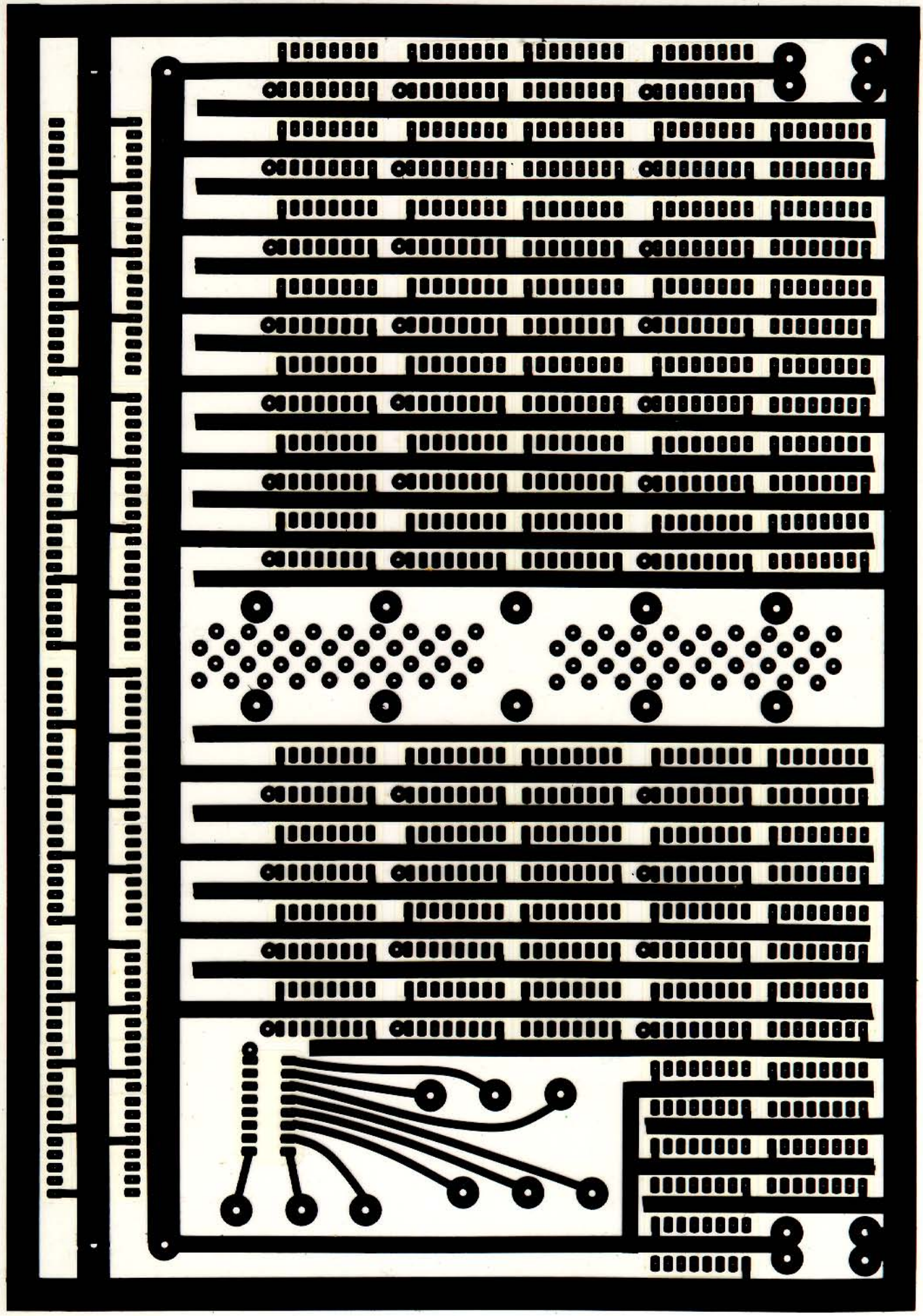


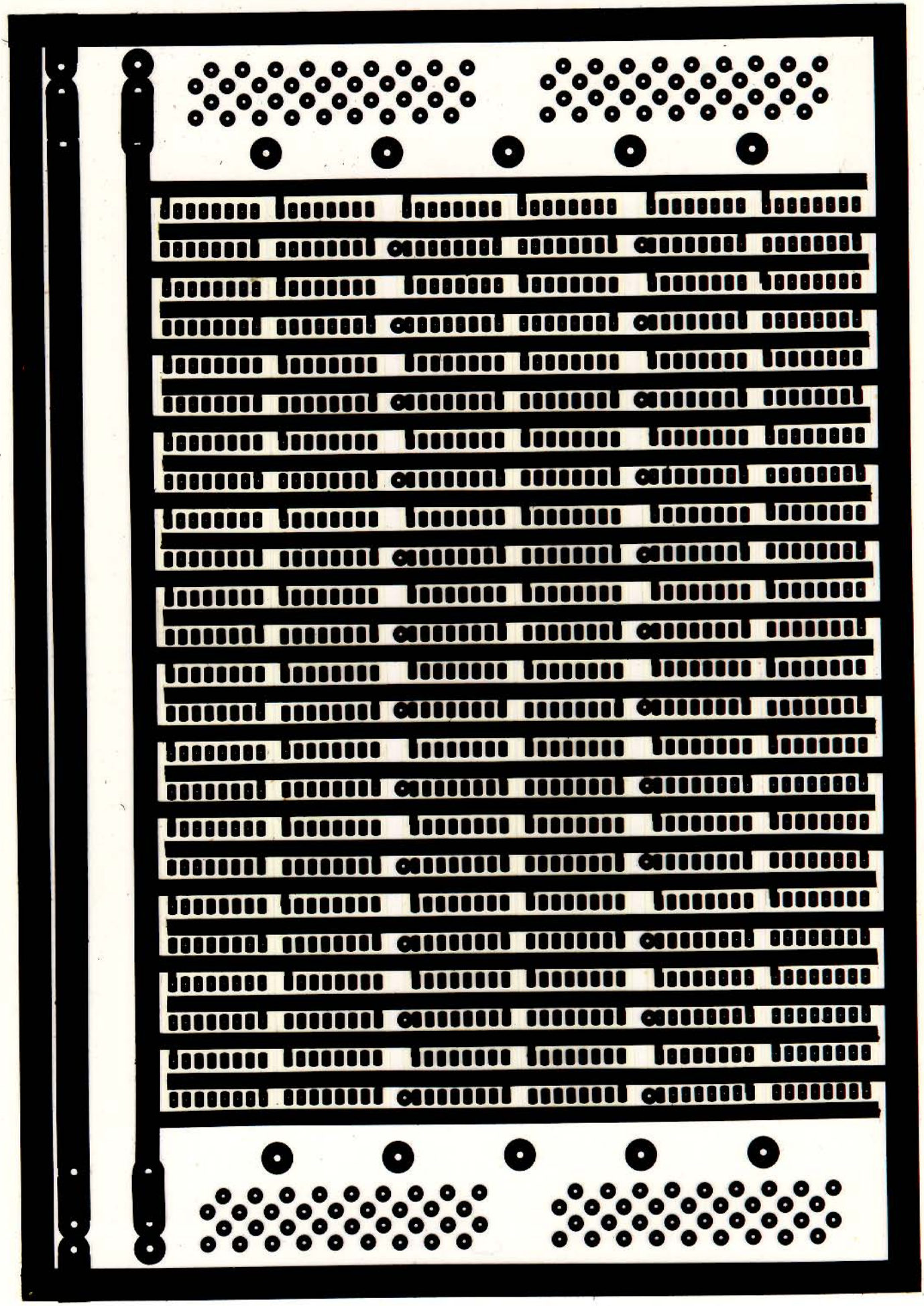


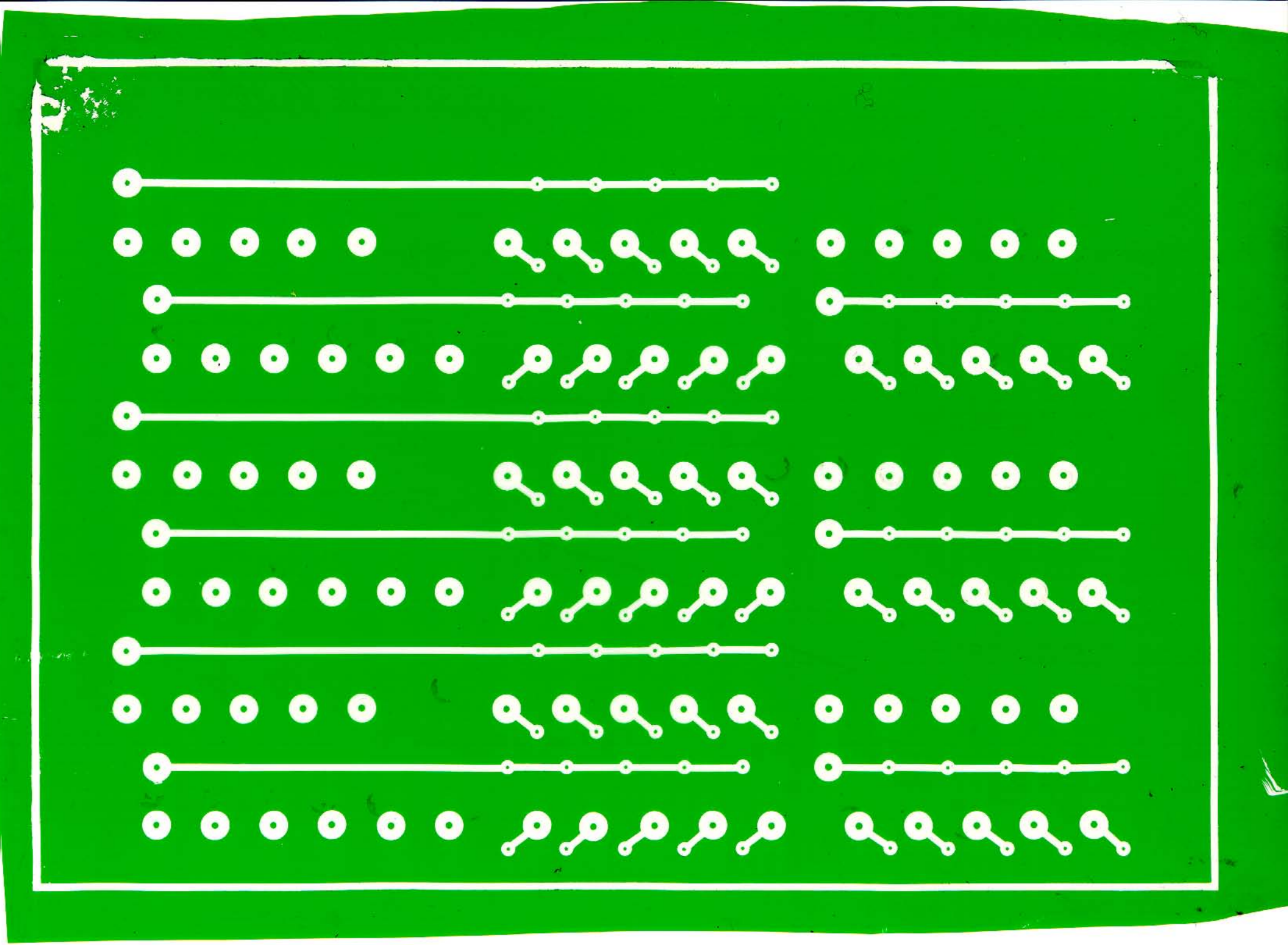
ROM

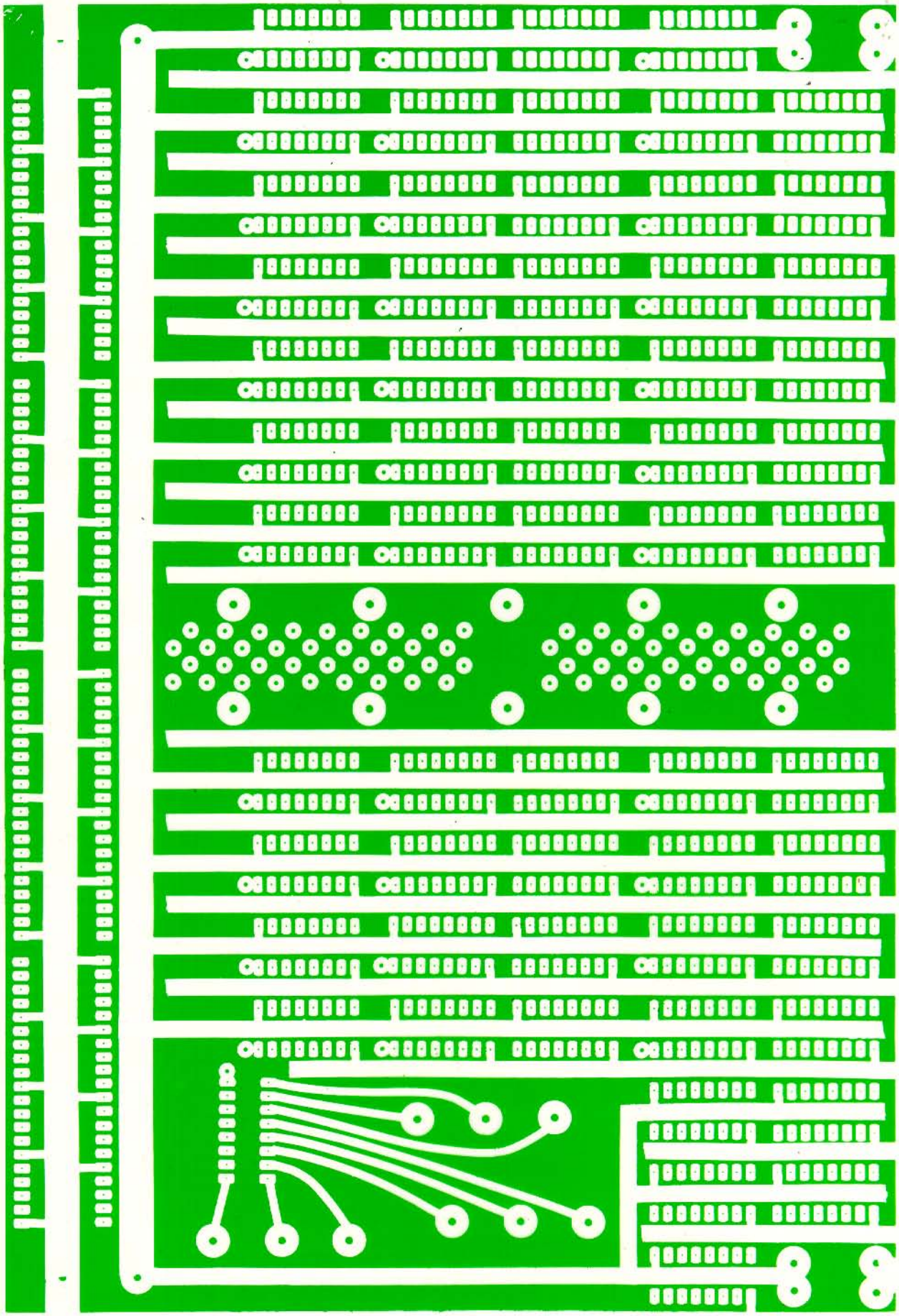


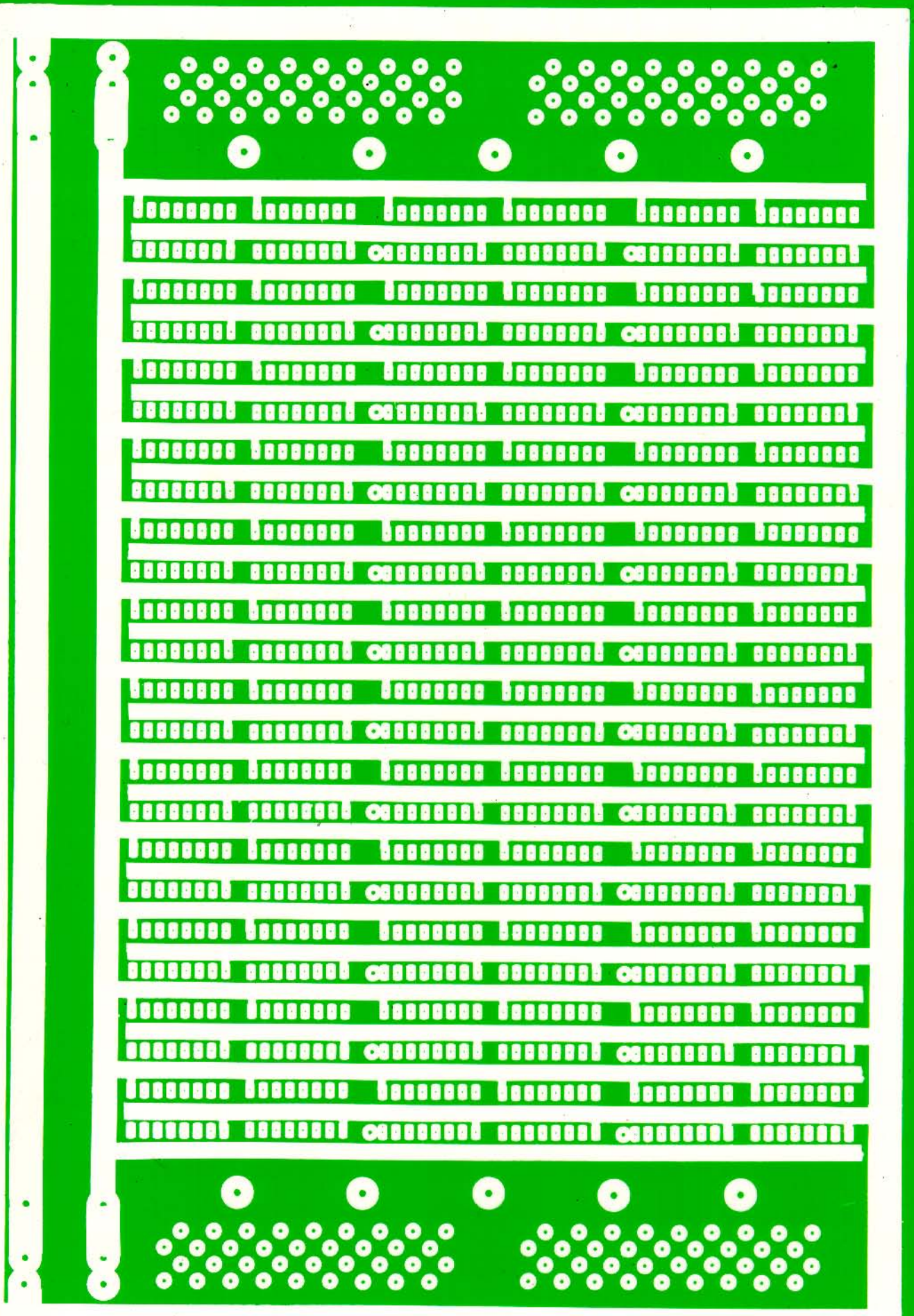


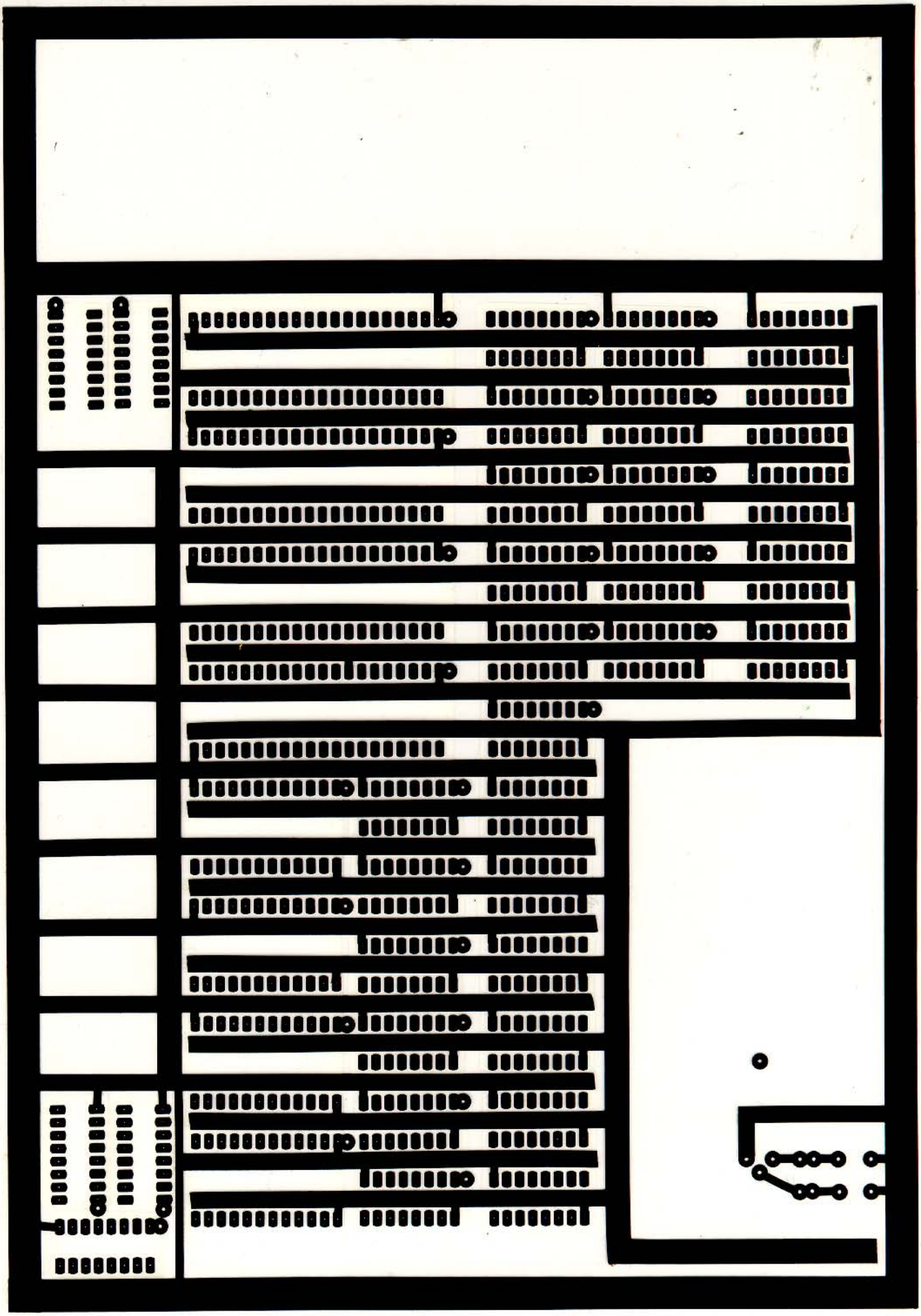


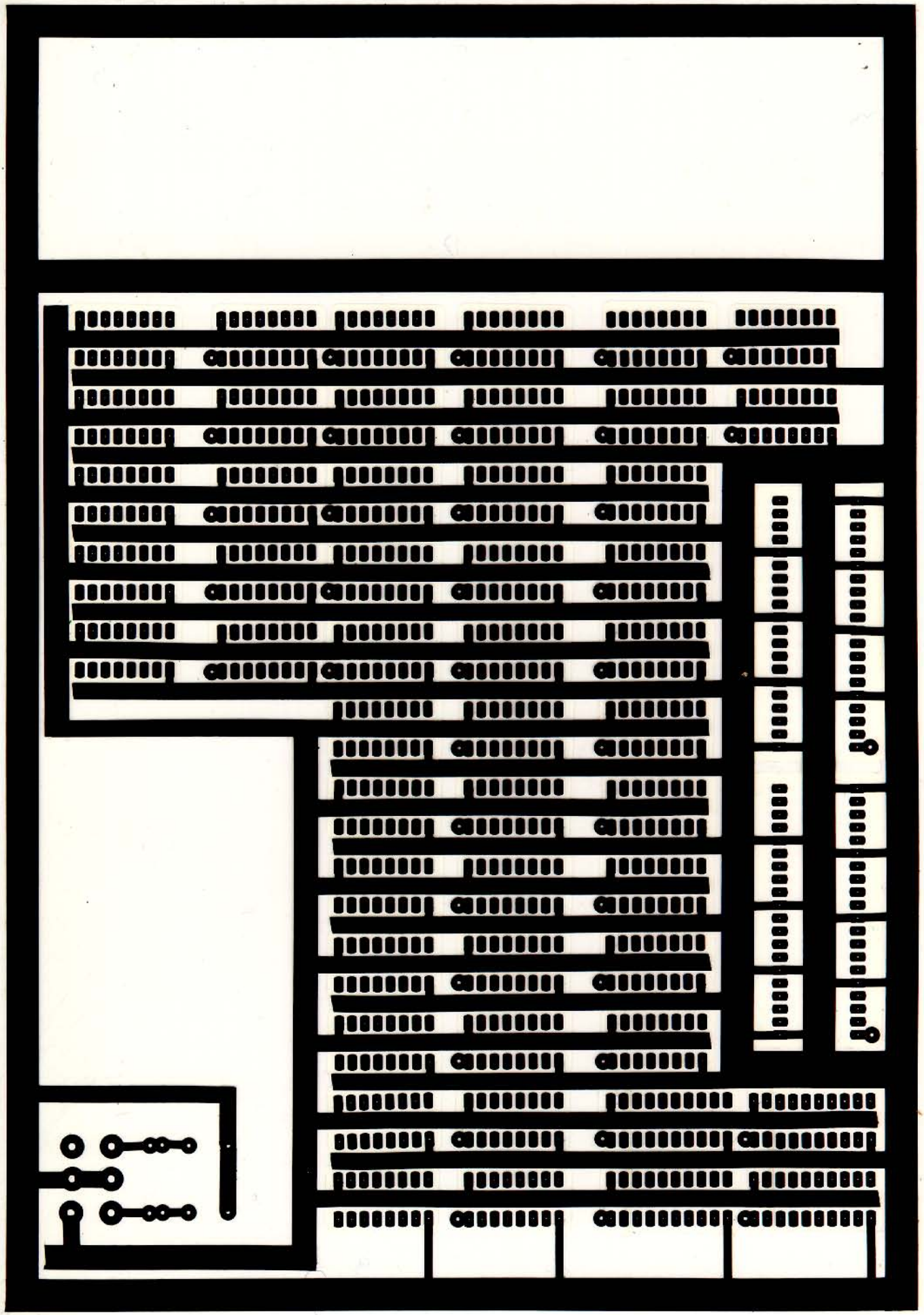


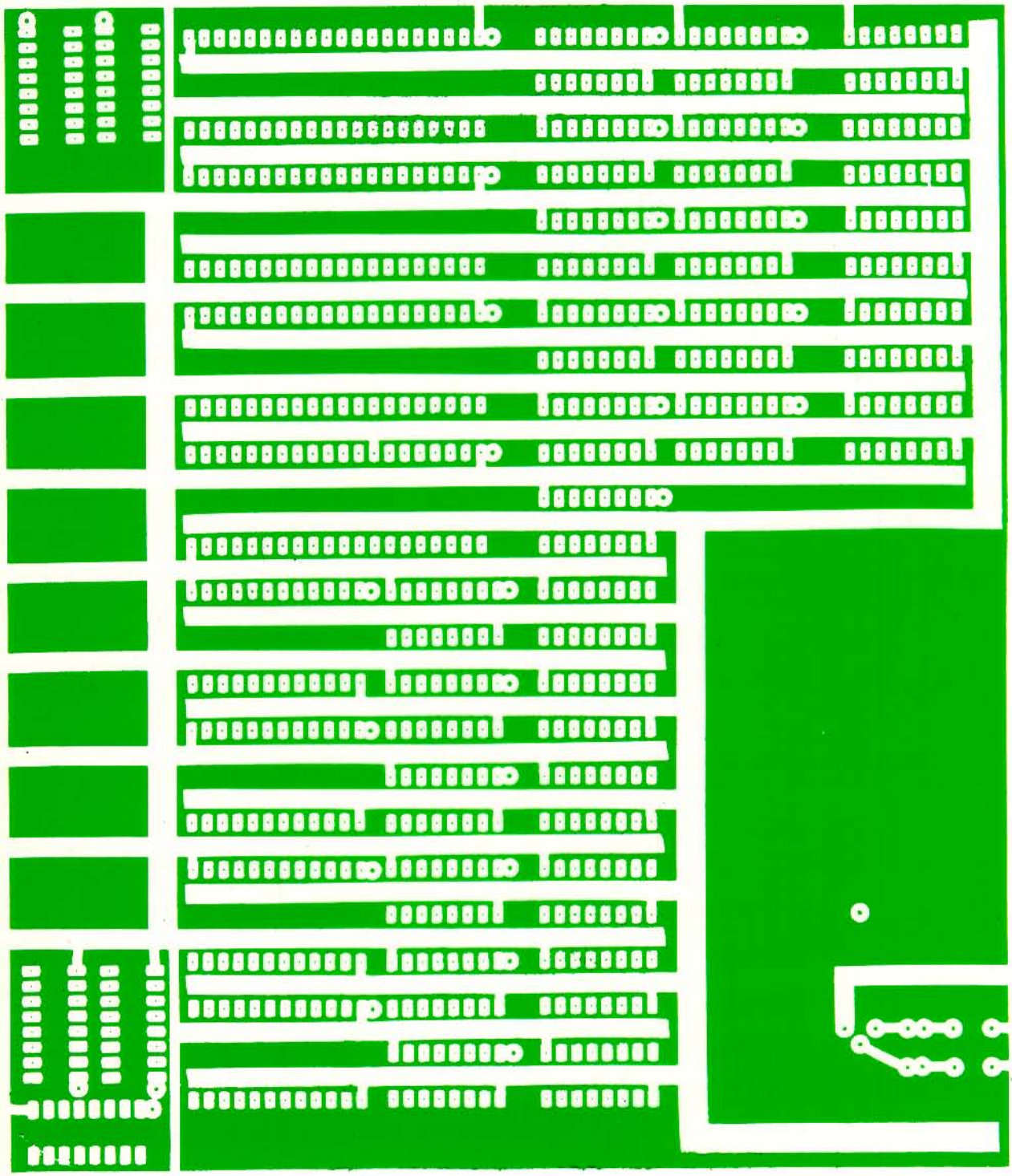


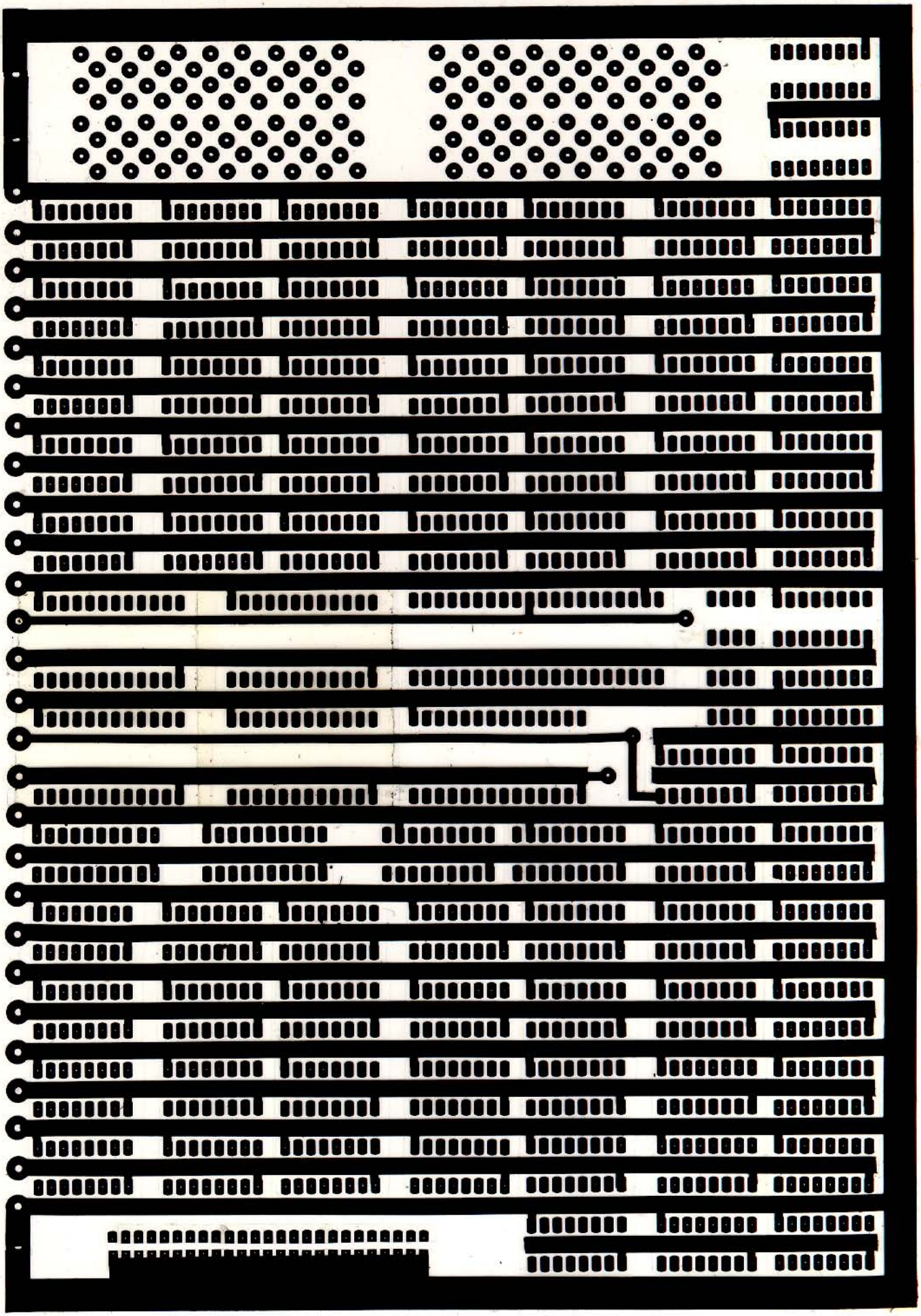


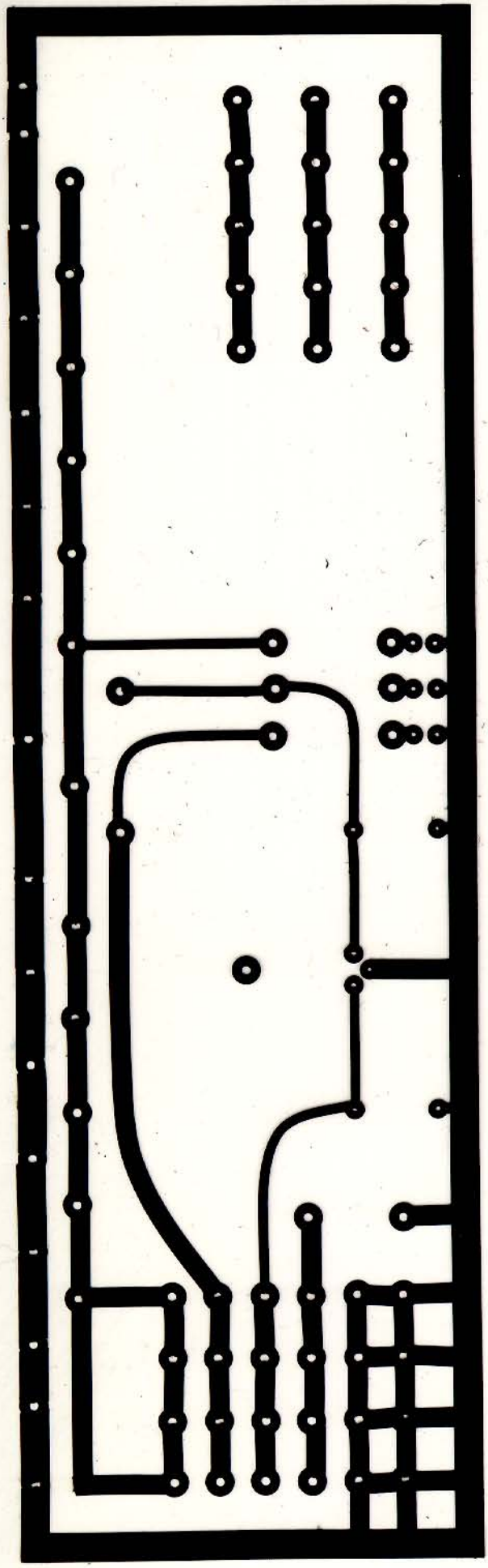


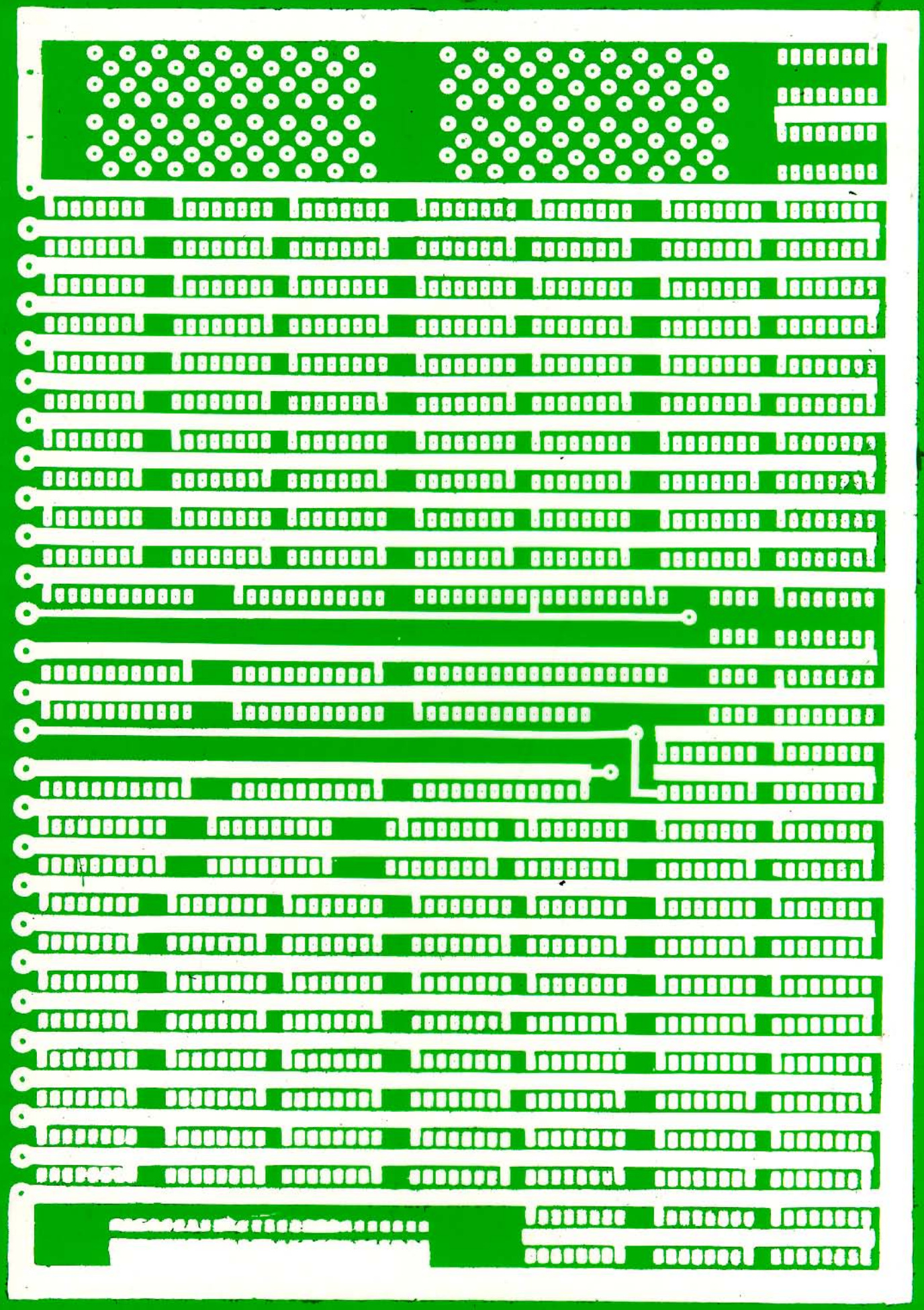


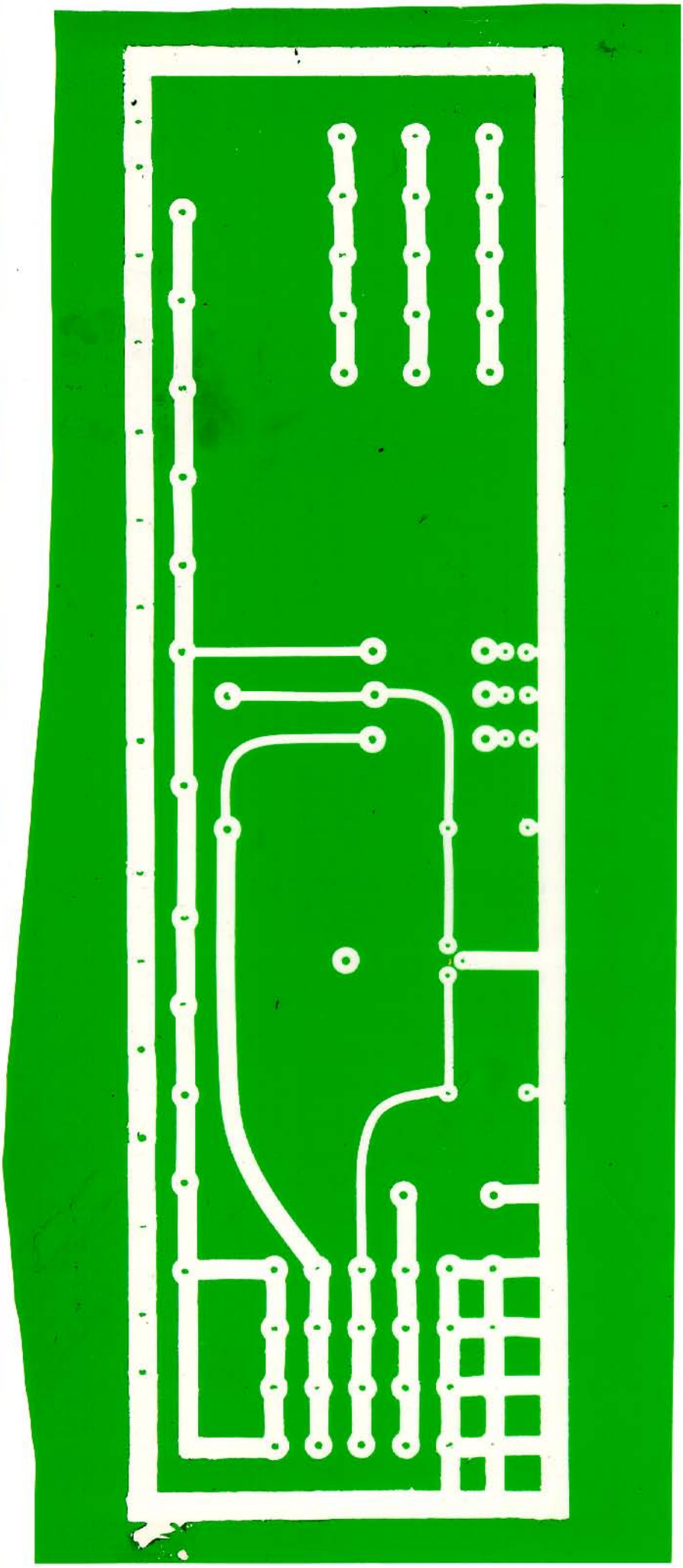


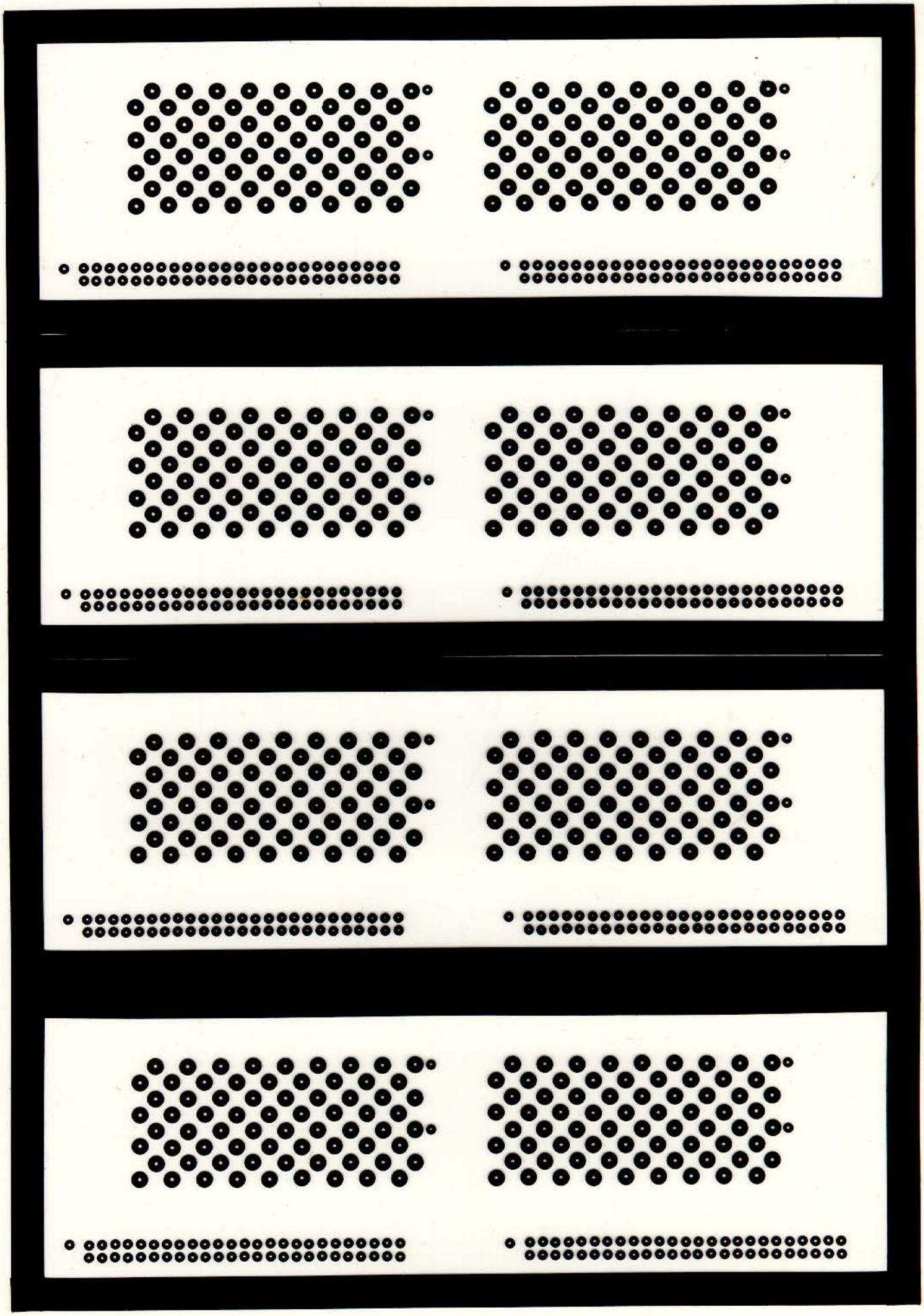






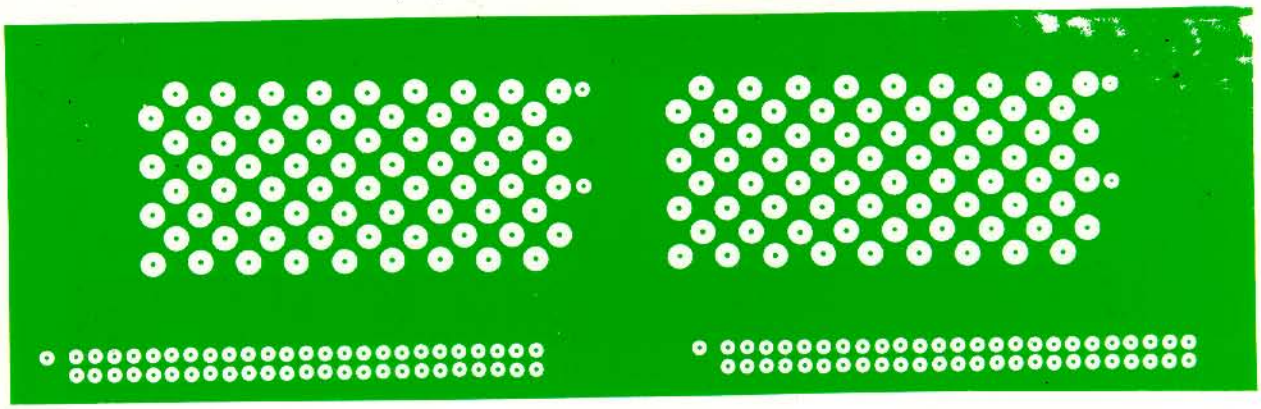


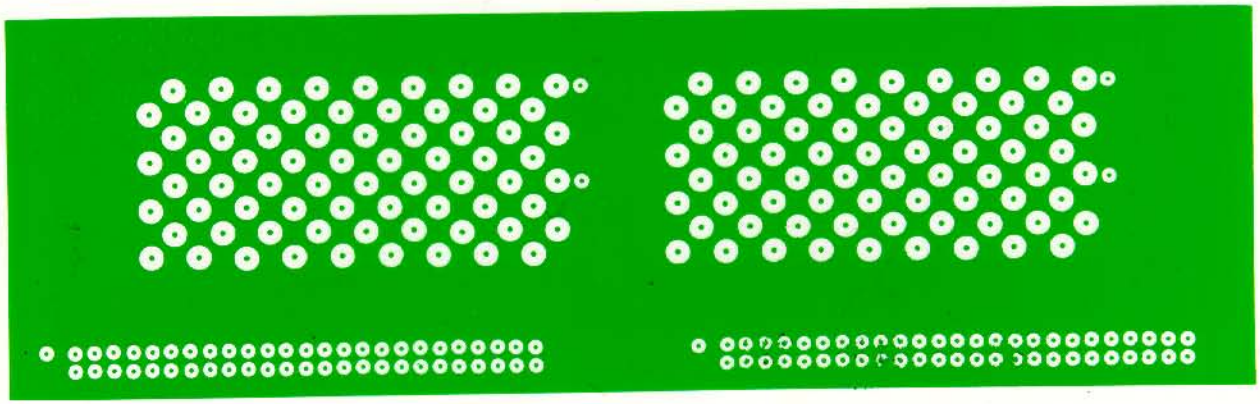


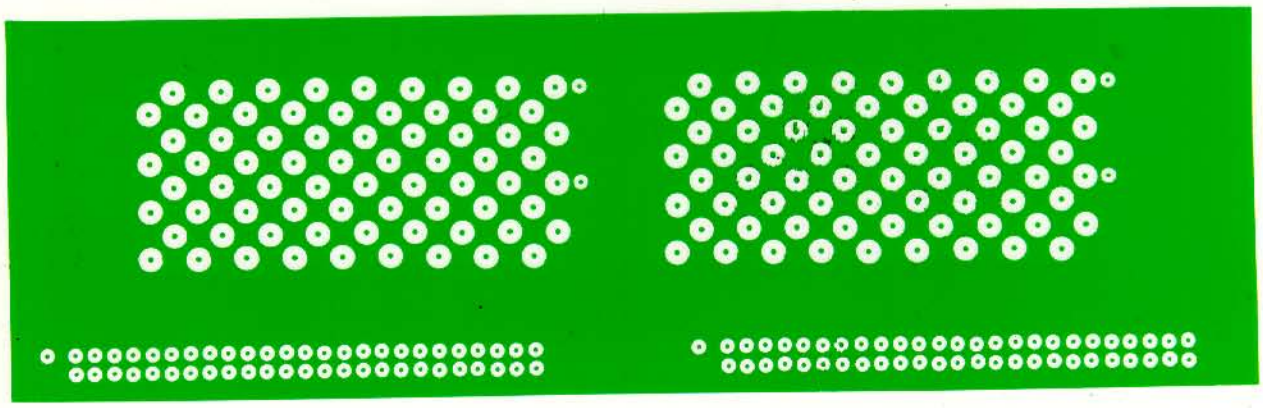


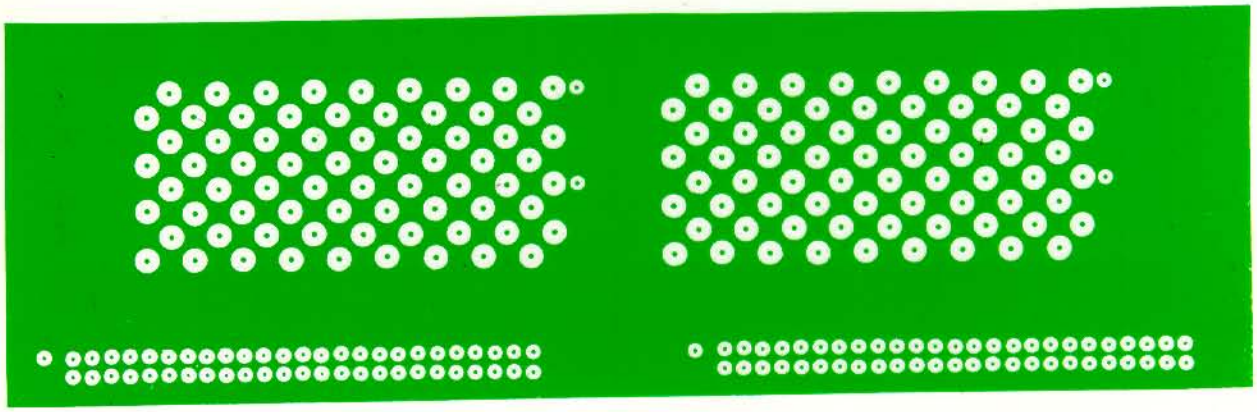
ARO
230287 BUS Data command

914, 720, 420, 2400









FEED ↑ UP
MODEL 914, 720, 520, 2400

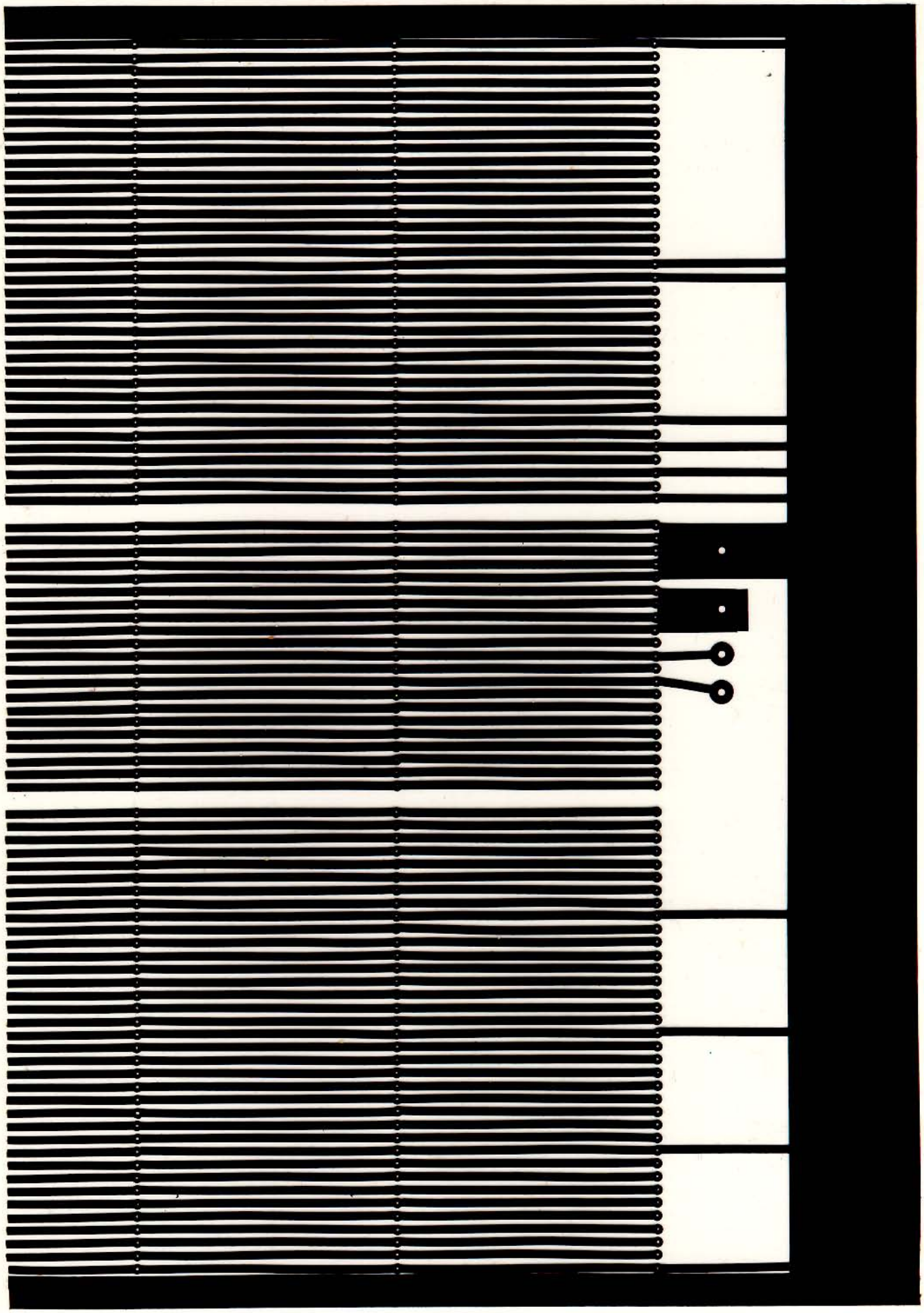
NOTES

FEED ↑ UP
MODEL 813, 660, 330

FEED ↑ UP
MODEL 914, 720, 420, 2400

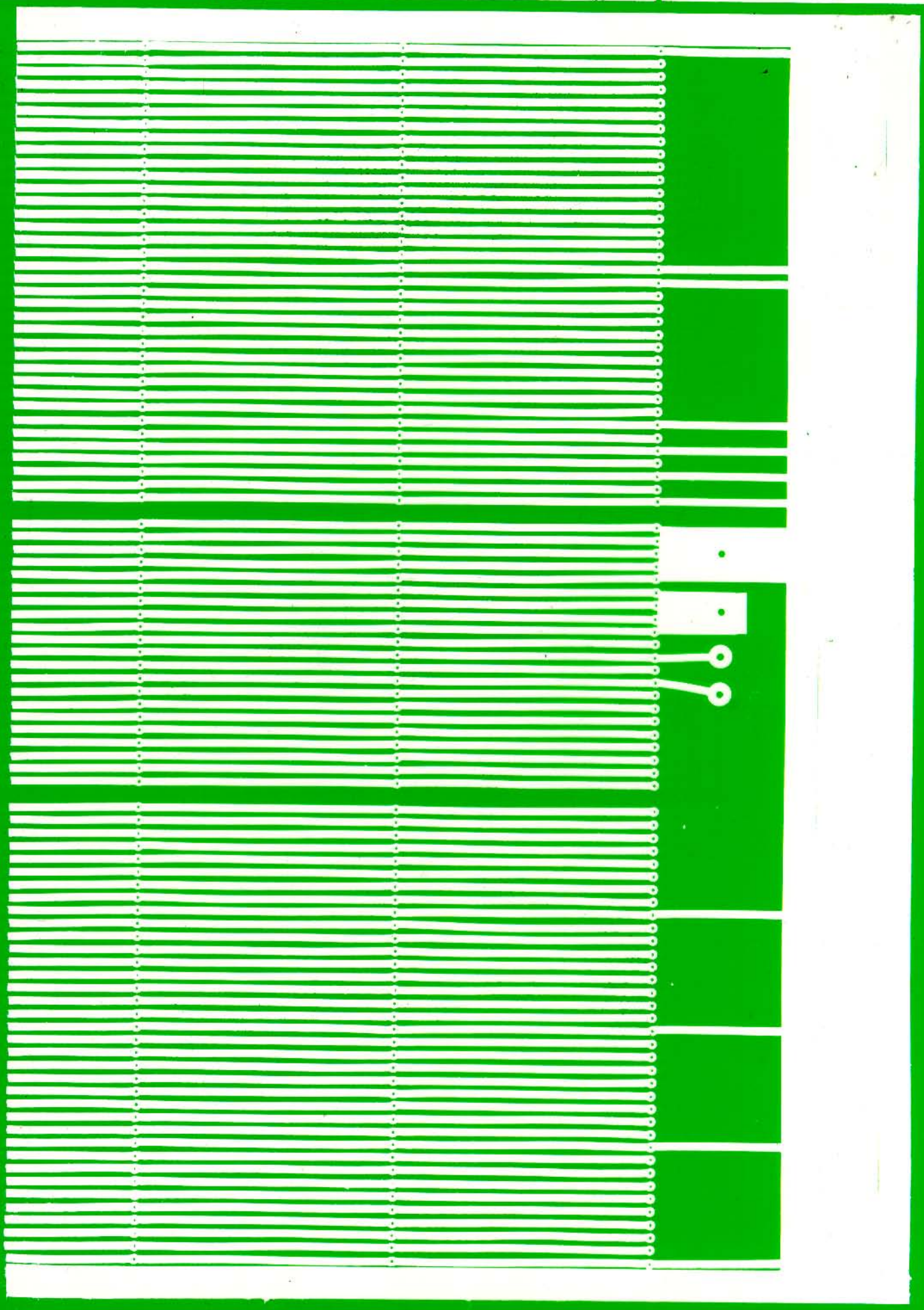
NOTES

FEED ↑ UP
MODEL 813, 660, 330



FEED ↑ UP
MODEL 914, 720, 420, 2400

NOTES



17 oct 81
APS Parallel Port - Programmable

FEED 1 UP
MODEL 813, 660, 300

FEED 1 UP
MODEL 914, 720, 420, 2400

Programmable Serial Port - 18081

PCB 1 UP
MODEL 813, 660, 330

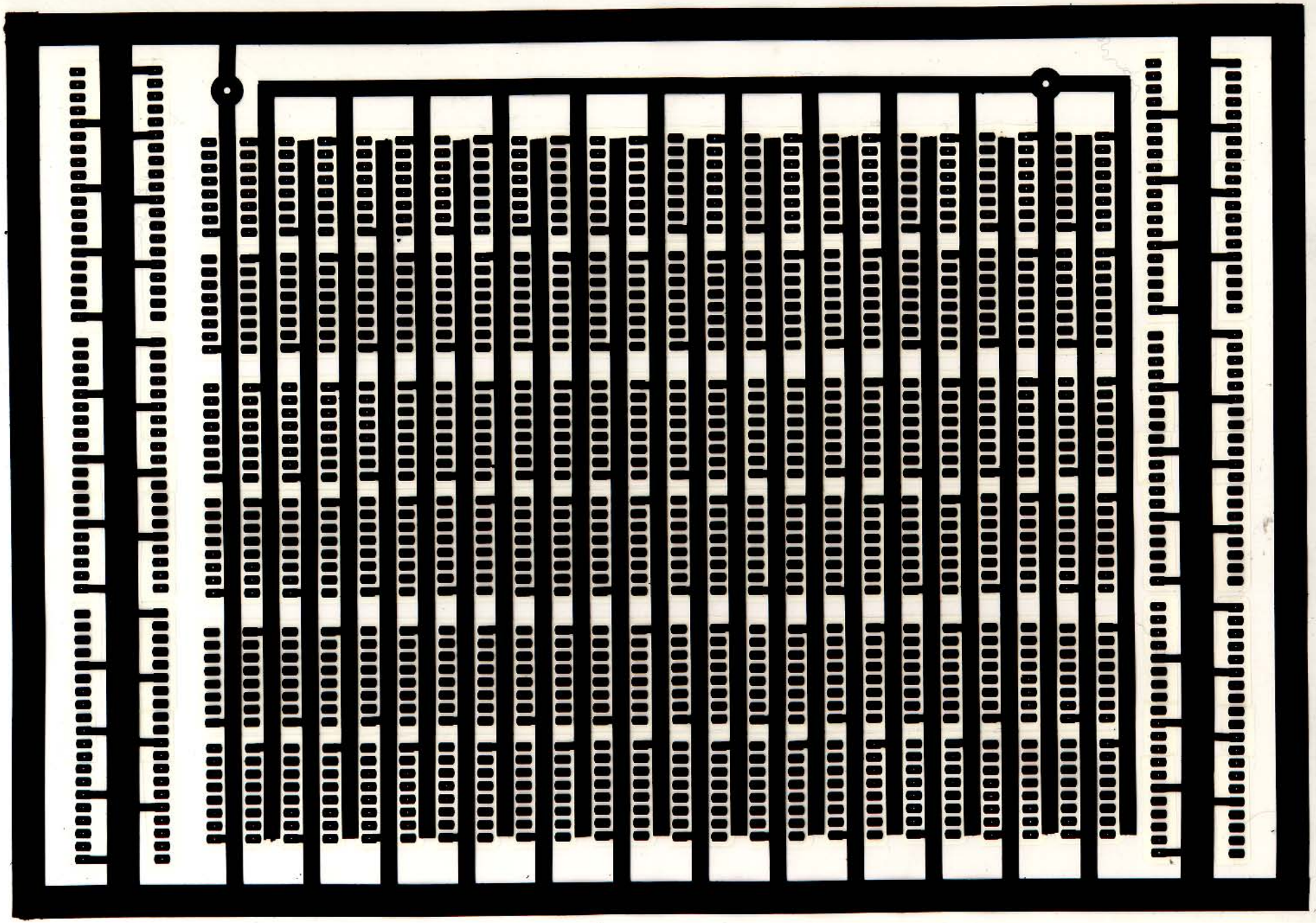
FEED ↑ UP
MODEL 914, 720, 420, 2400

NOTES

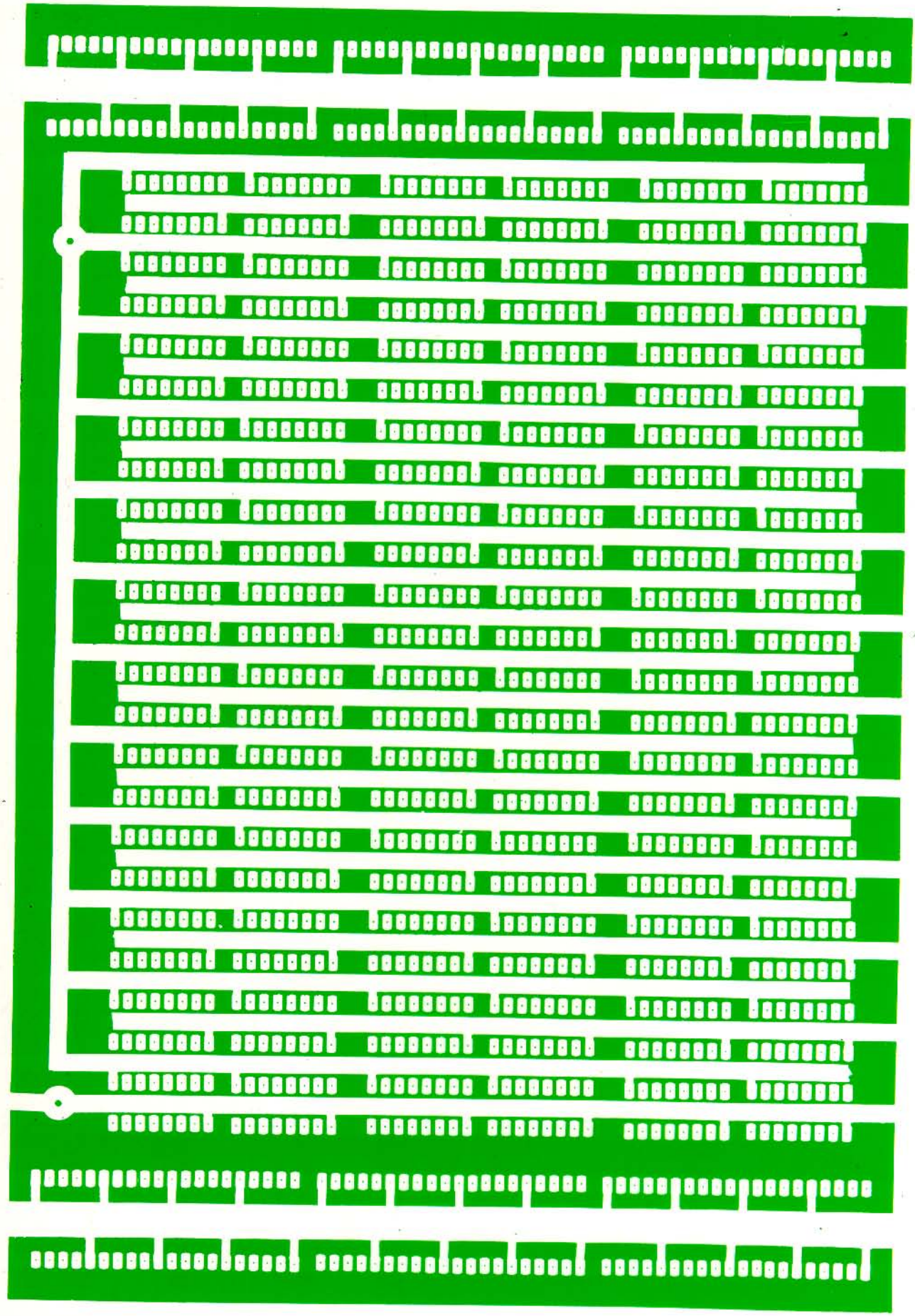
FEED ↑ UP
MODEL 813, 660, 330

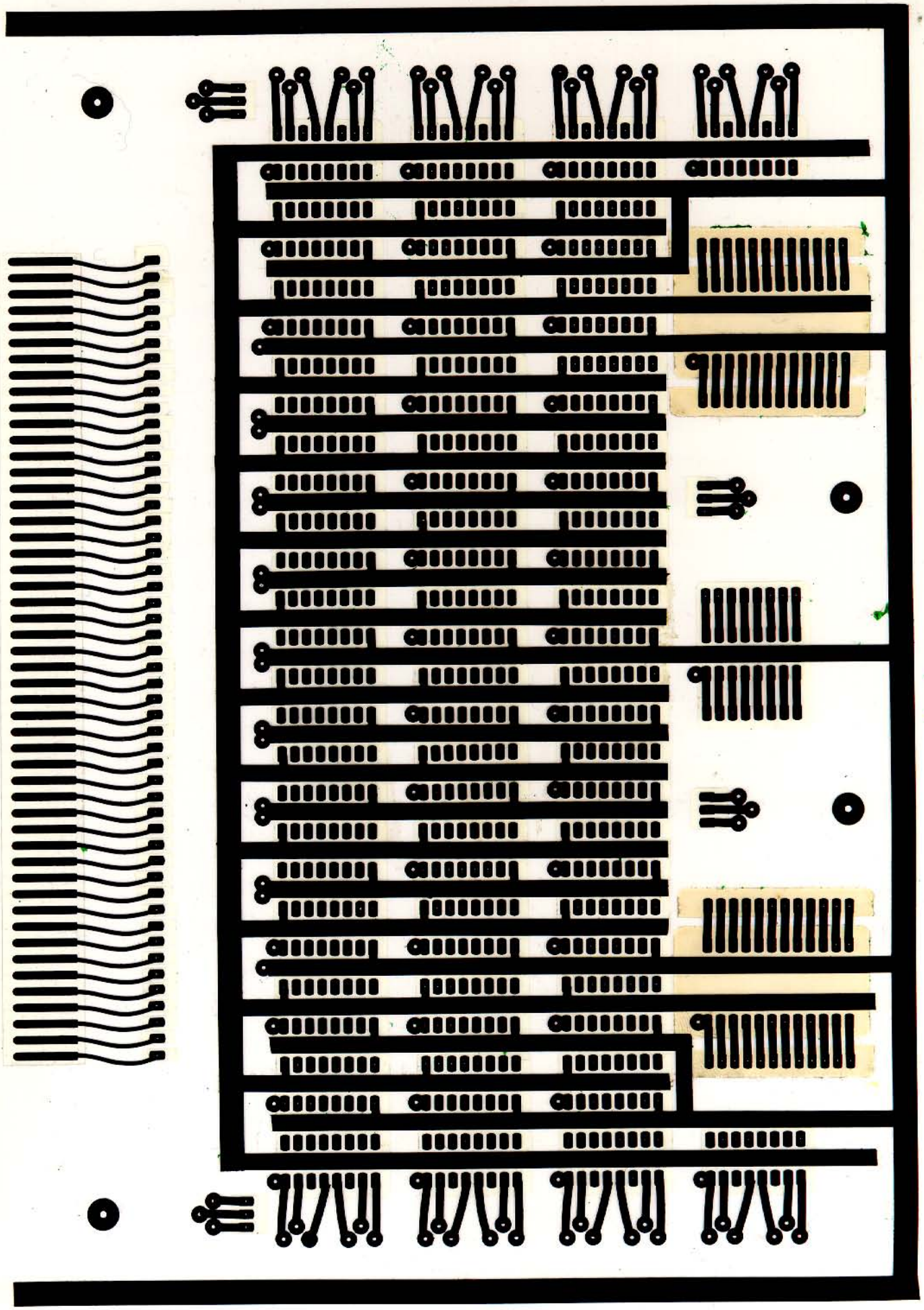
UNIBUS I/O - Interface

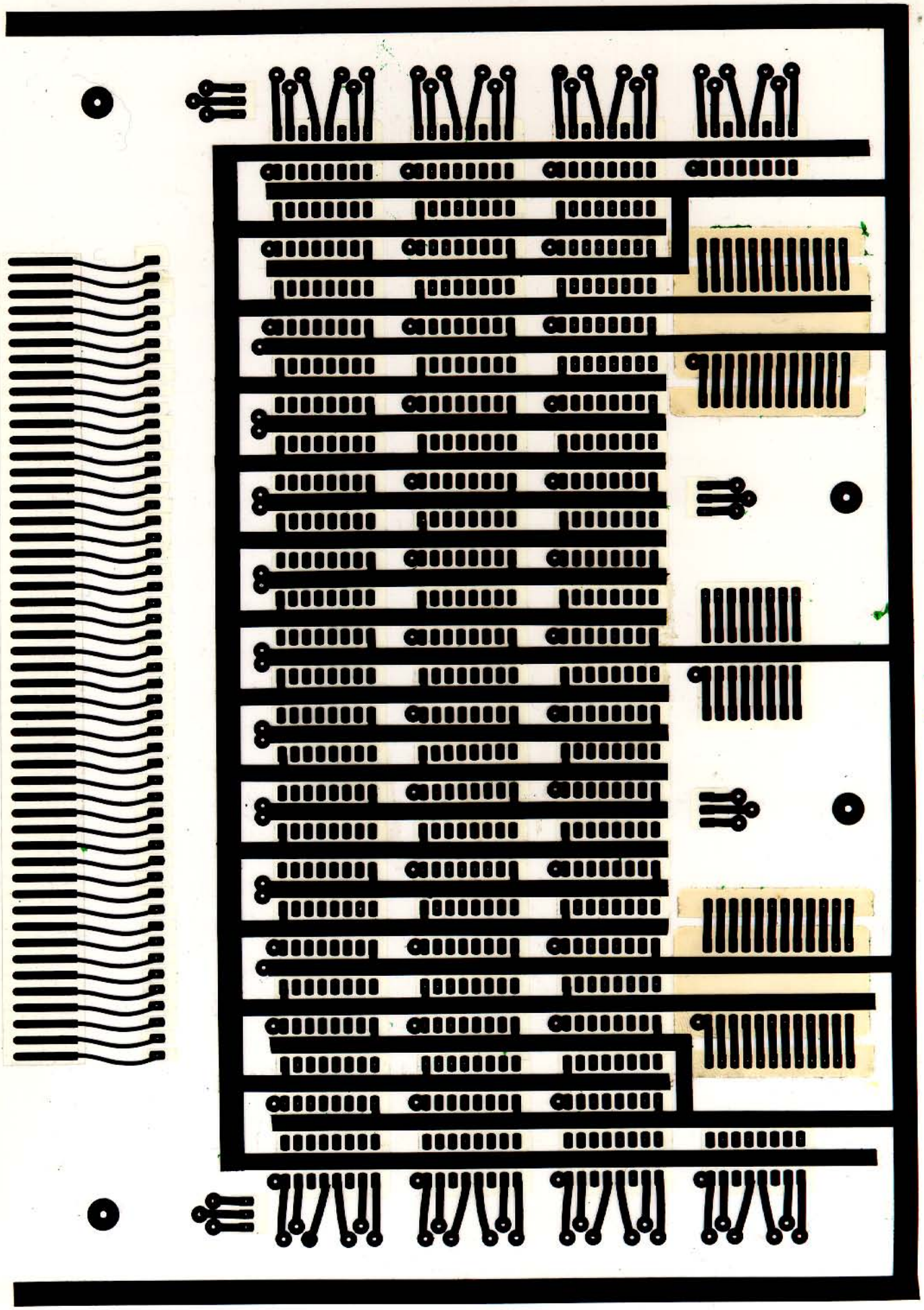
20048
RA

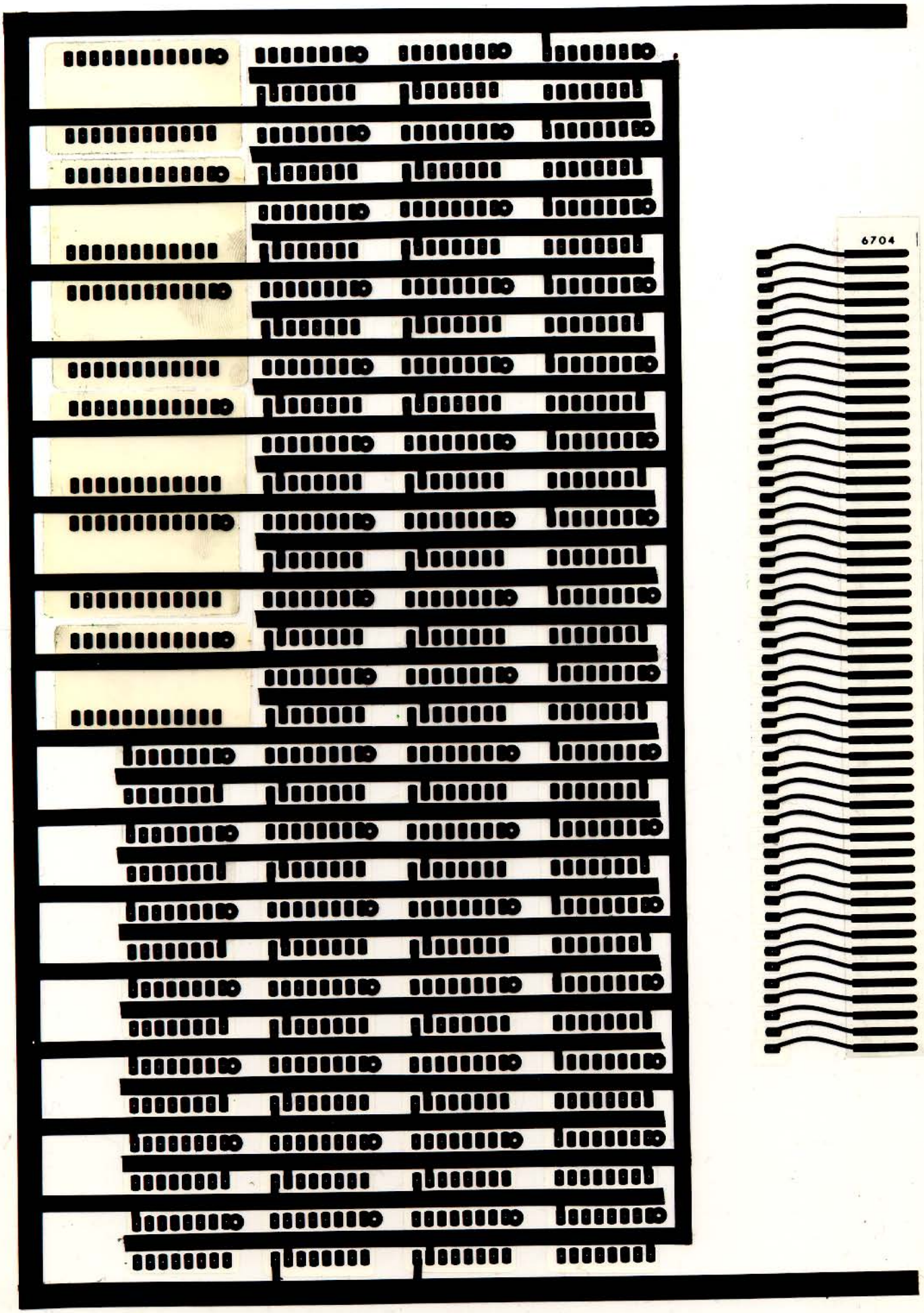


PROM Programmer Interface
T.p.b Button Positive
30-w-77 ARO





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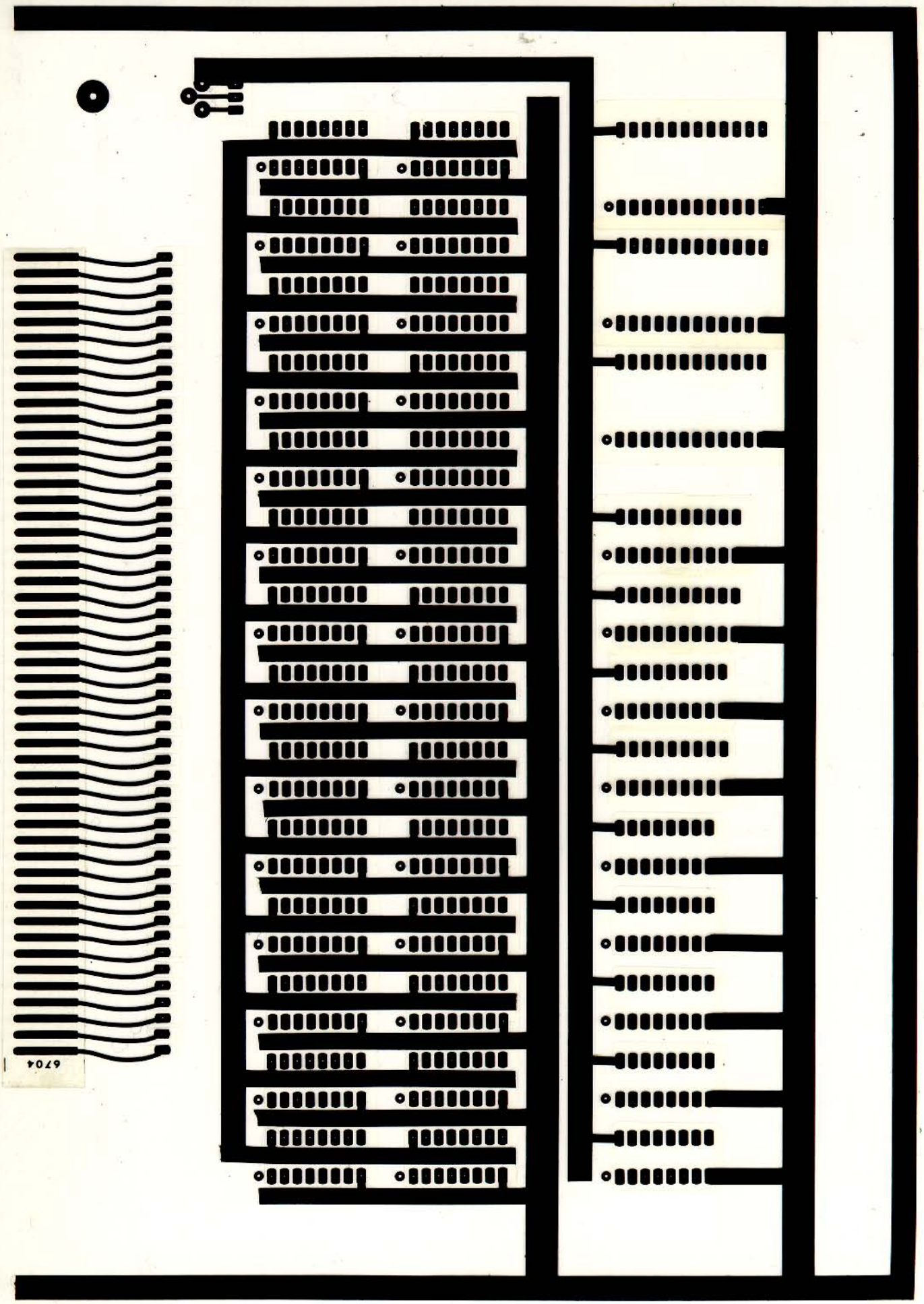
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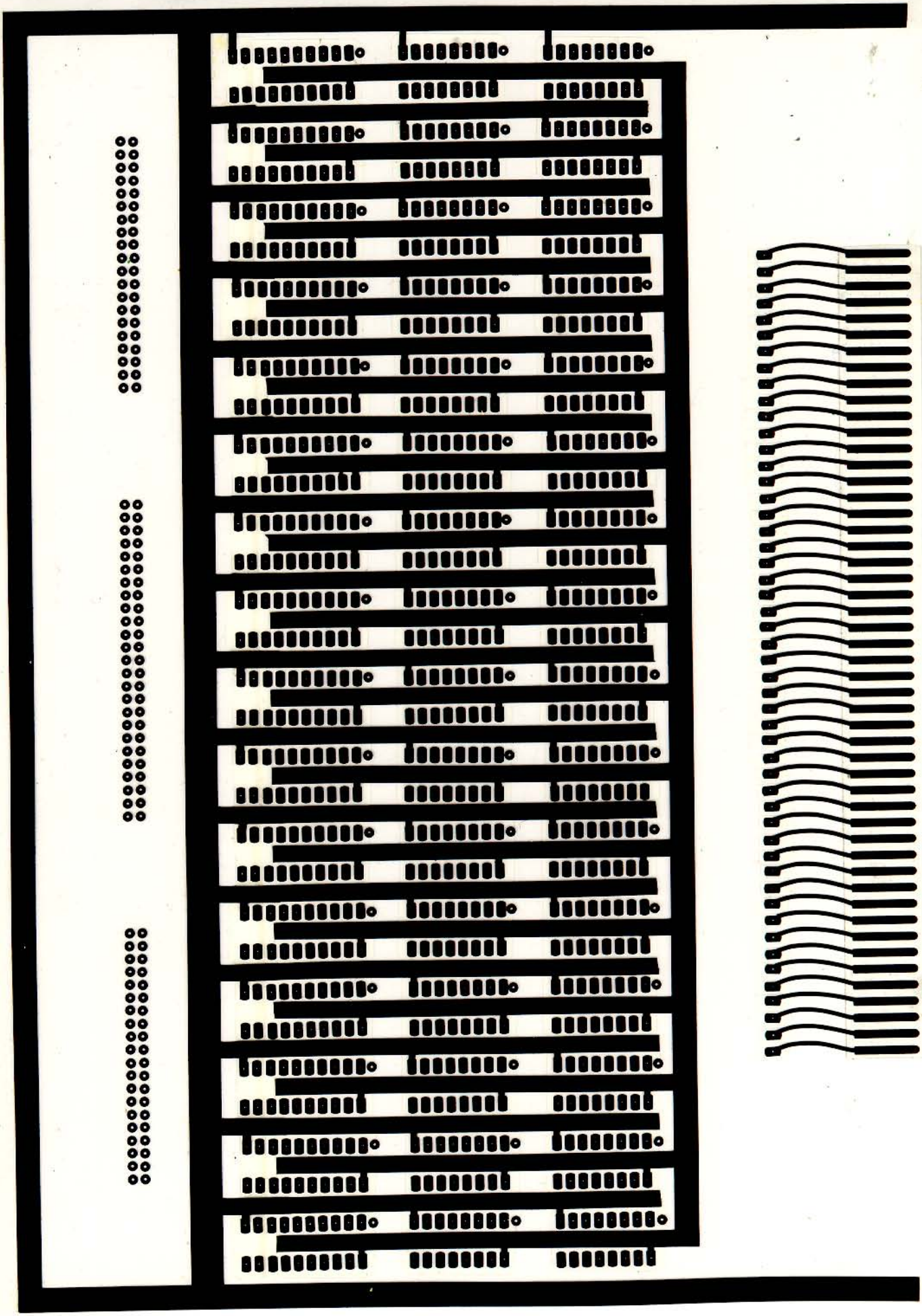

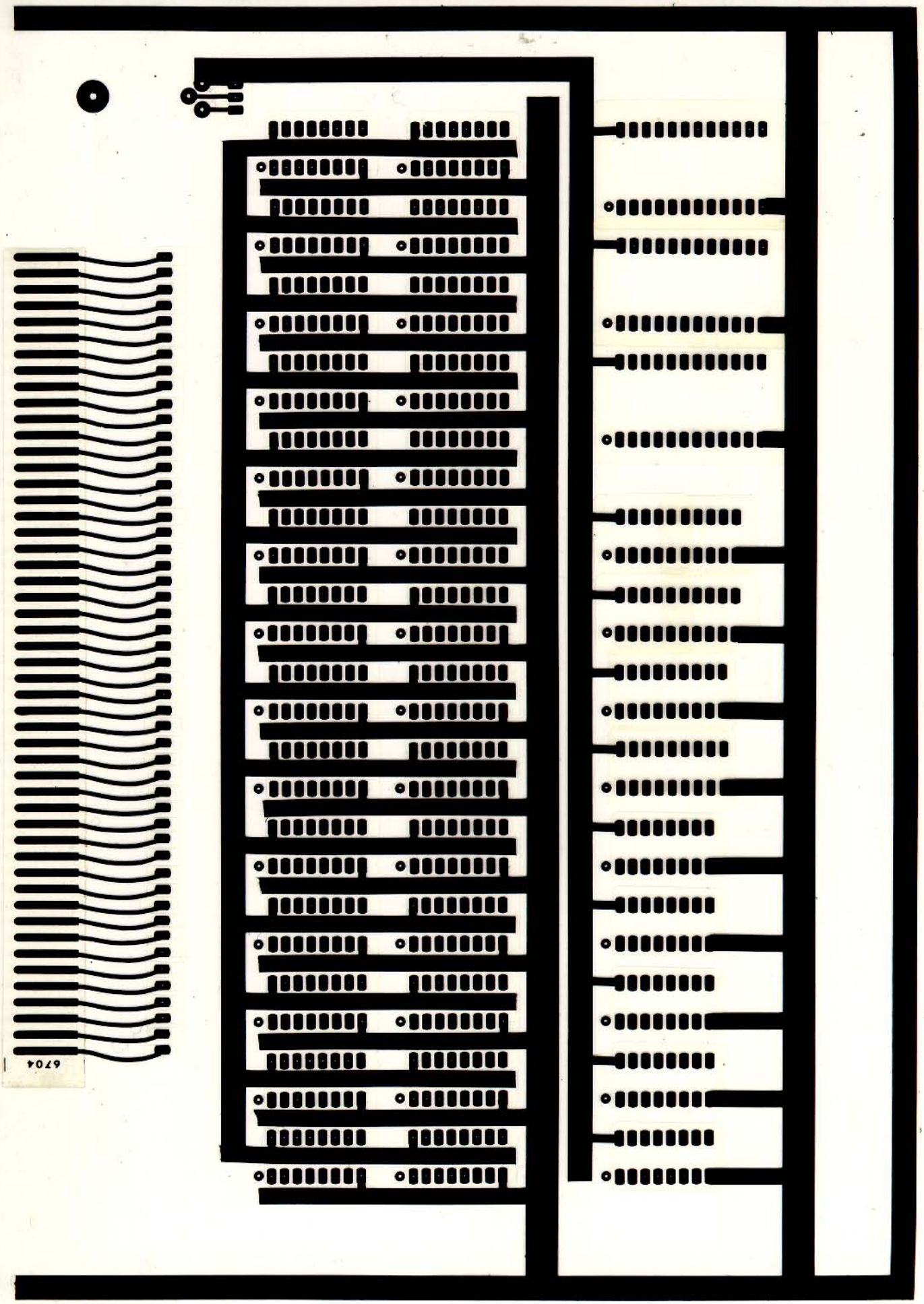
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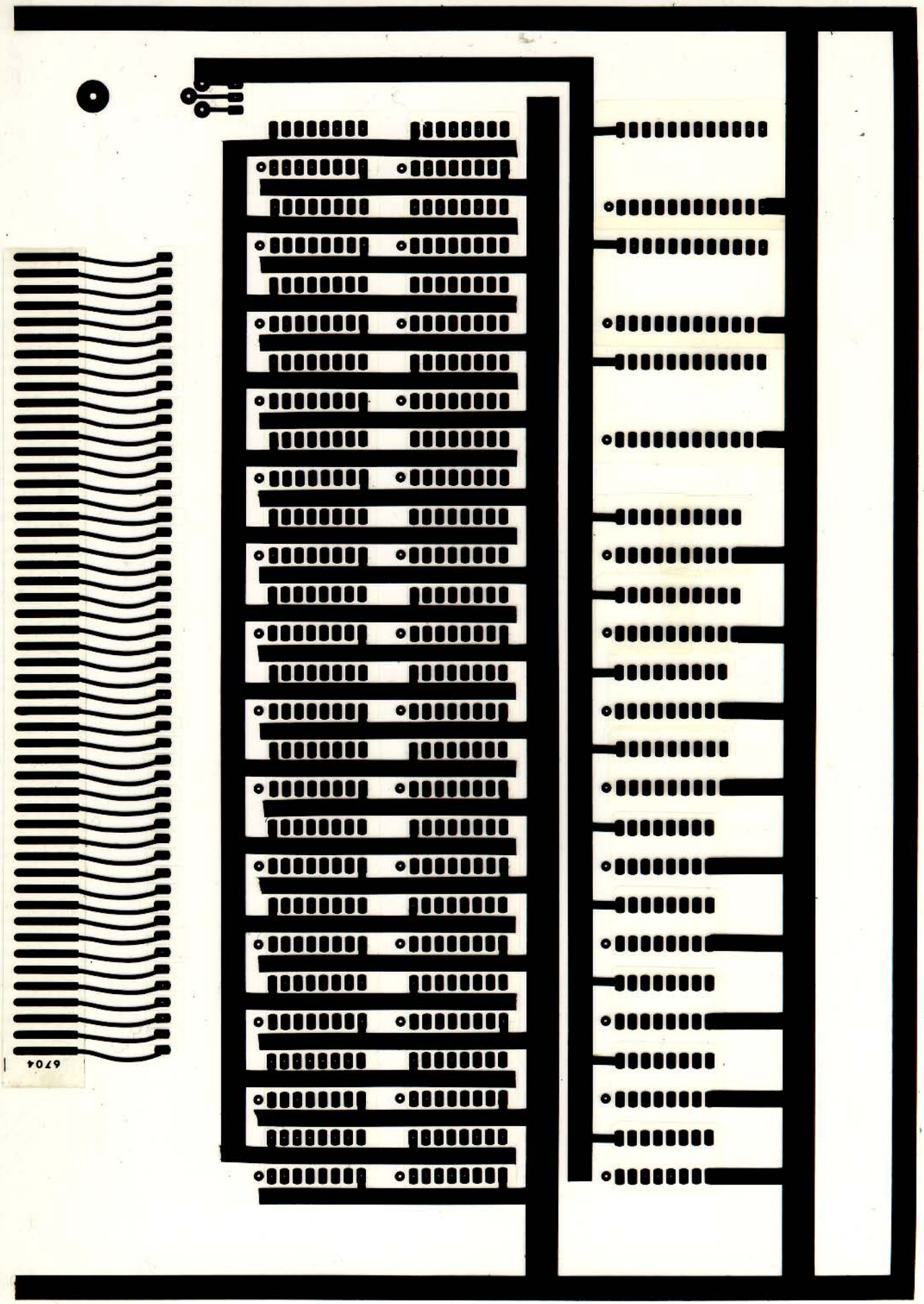
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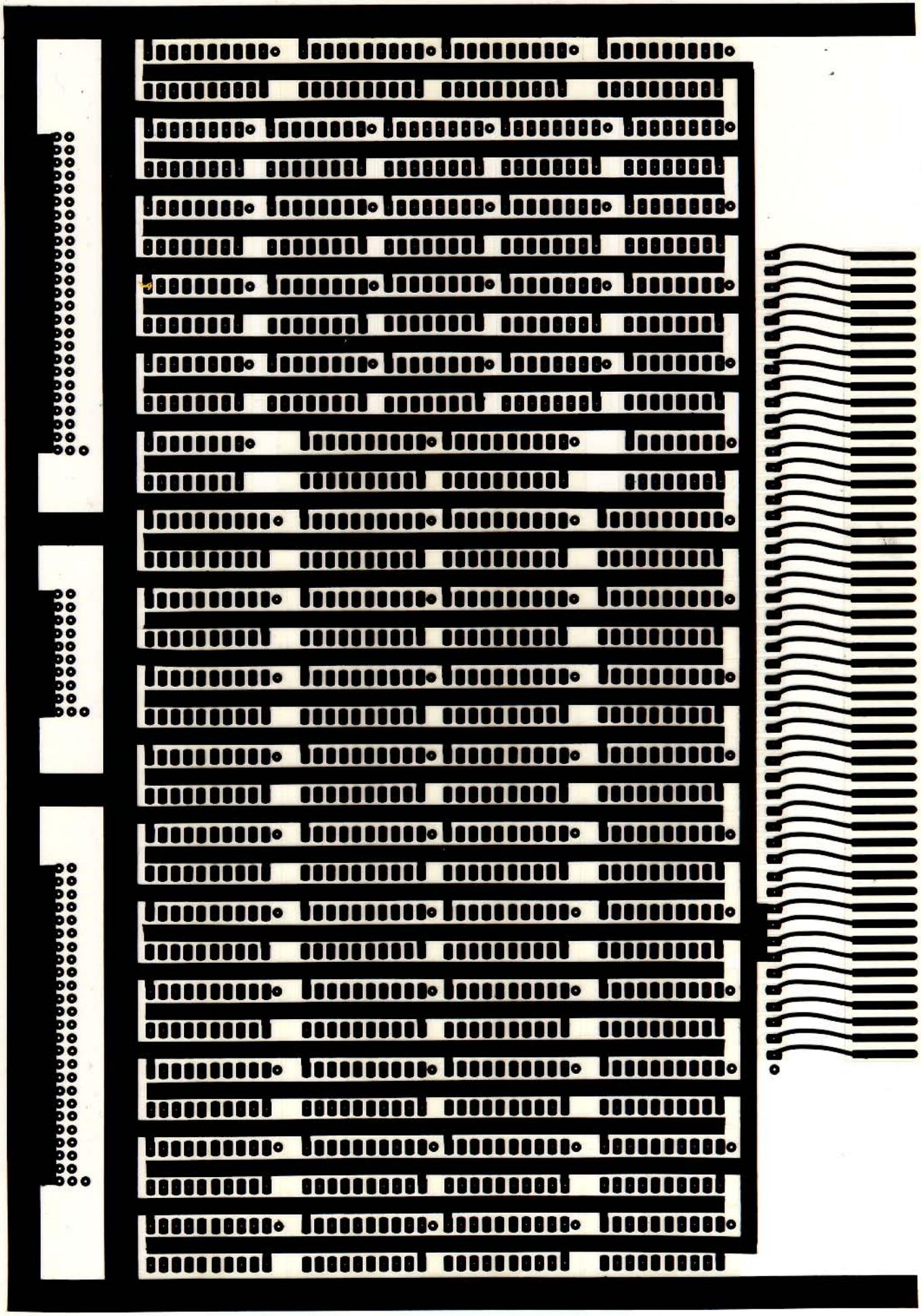
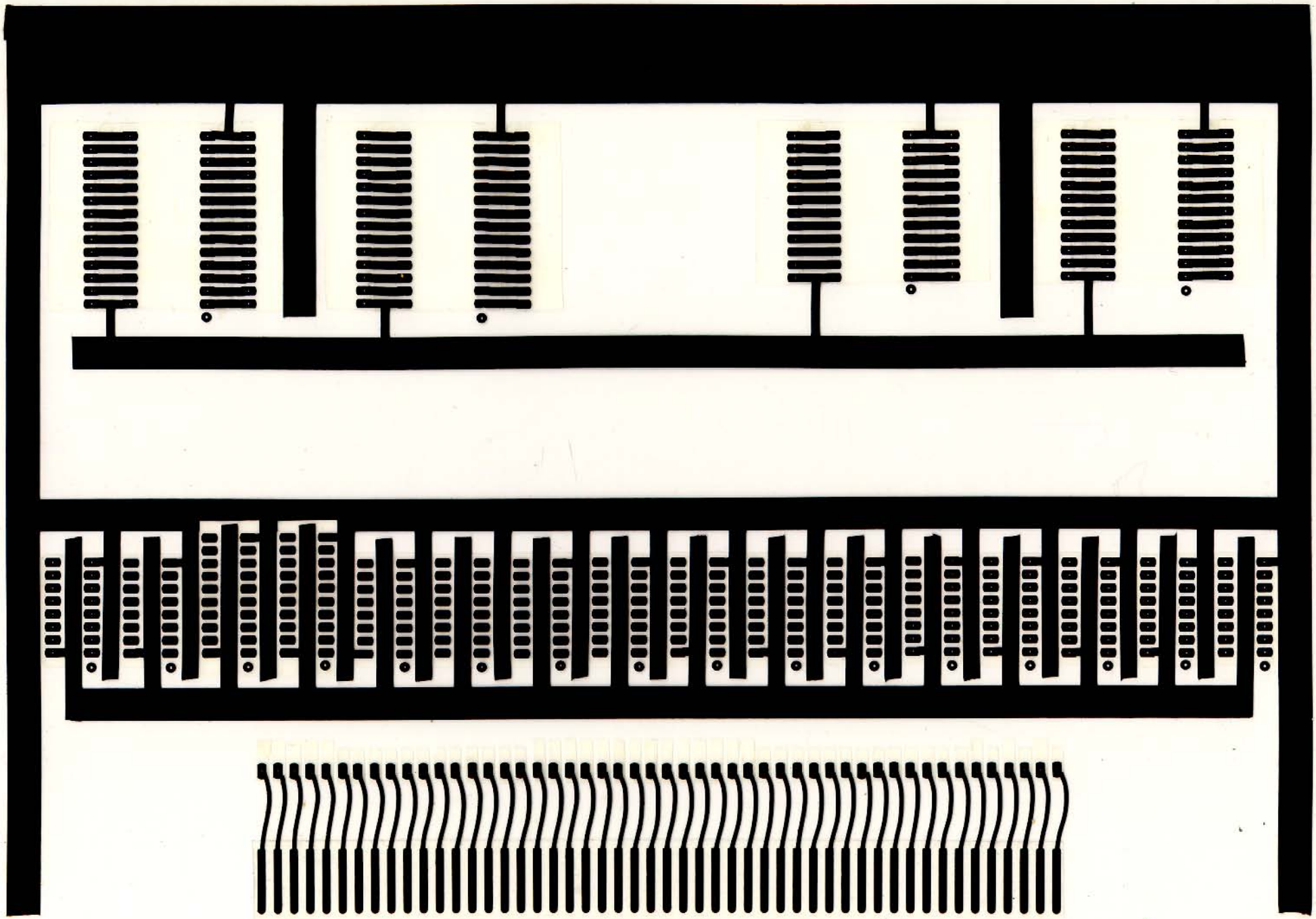
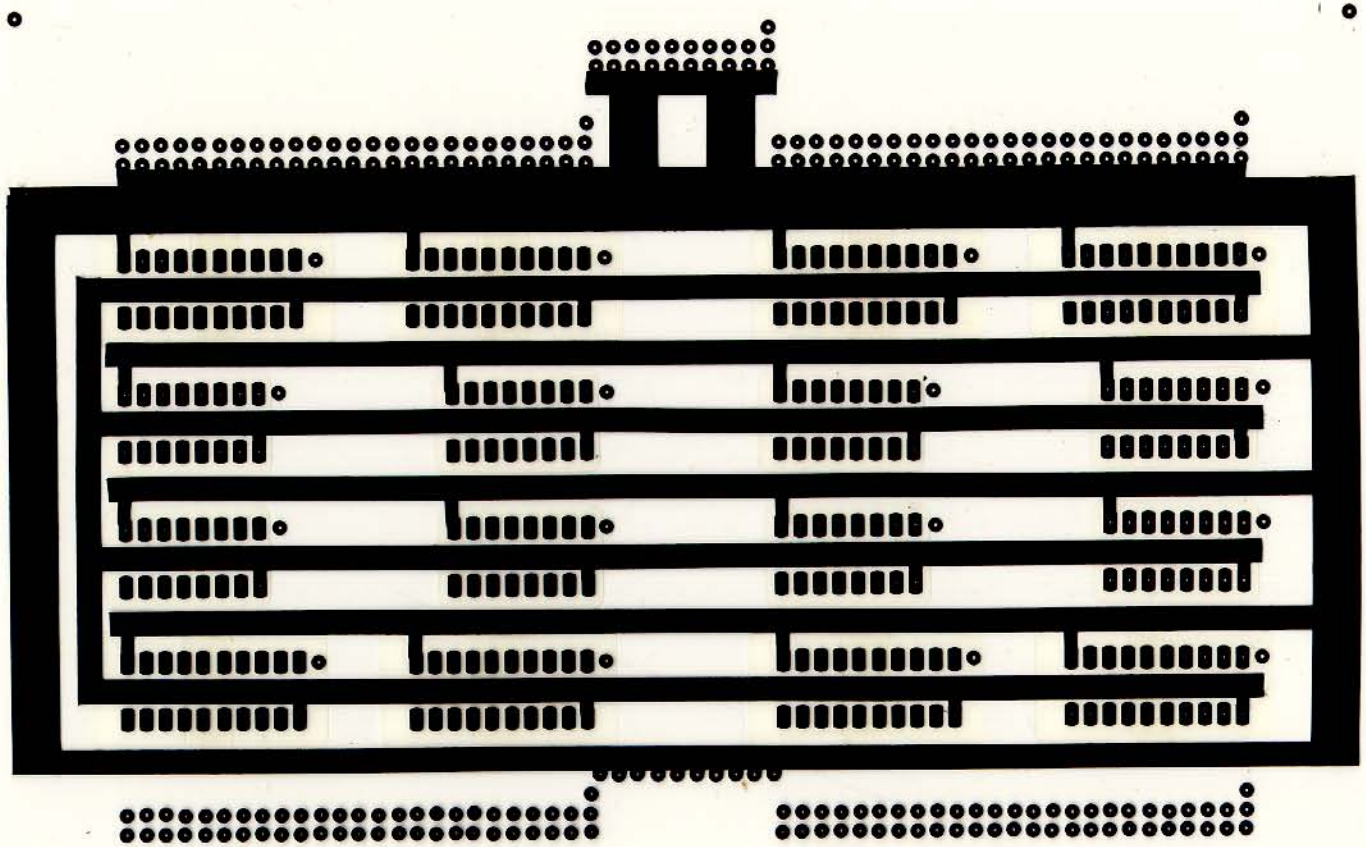


64K8 FRAM
ARO
15-Aug-83



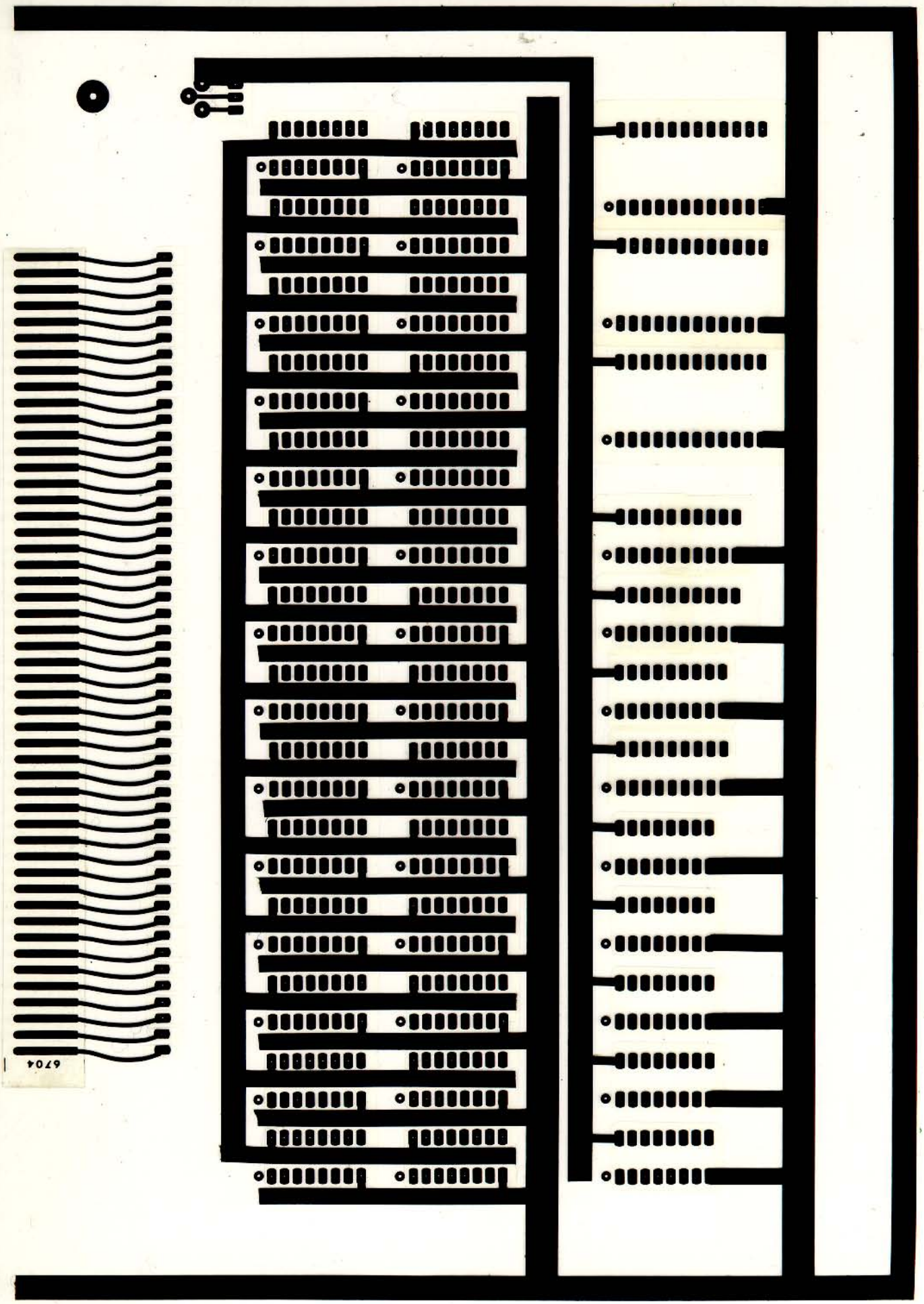
Eprom Programmer Board AG
27(16, 32, 32, 64, 128, 256) 14 Aug 83



General Purpose PRAM I/O Buffer

16-Aug-83

VAB3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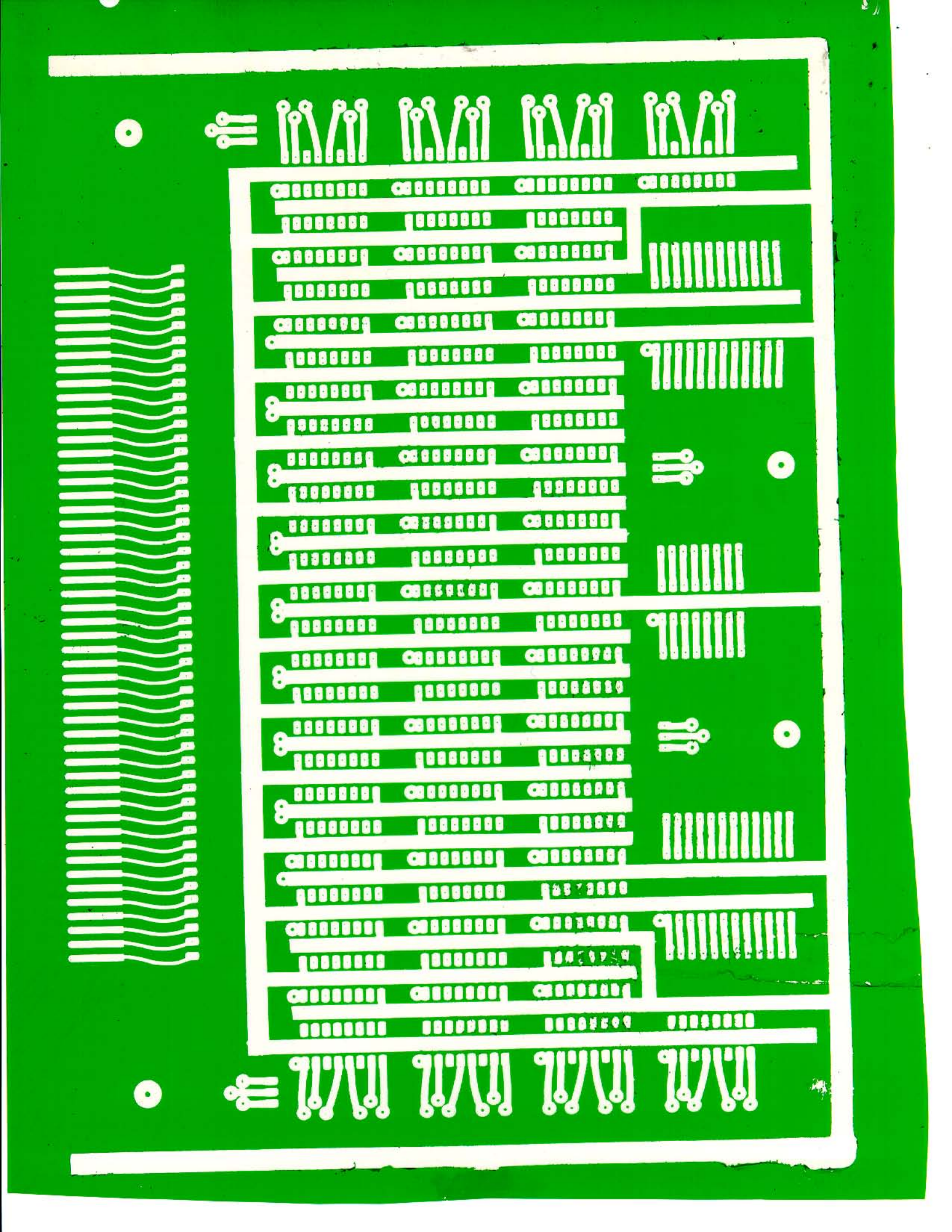

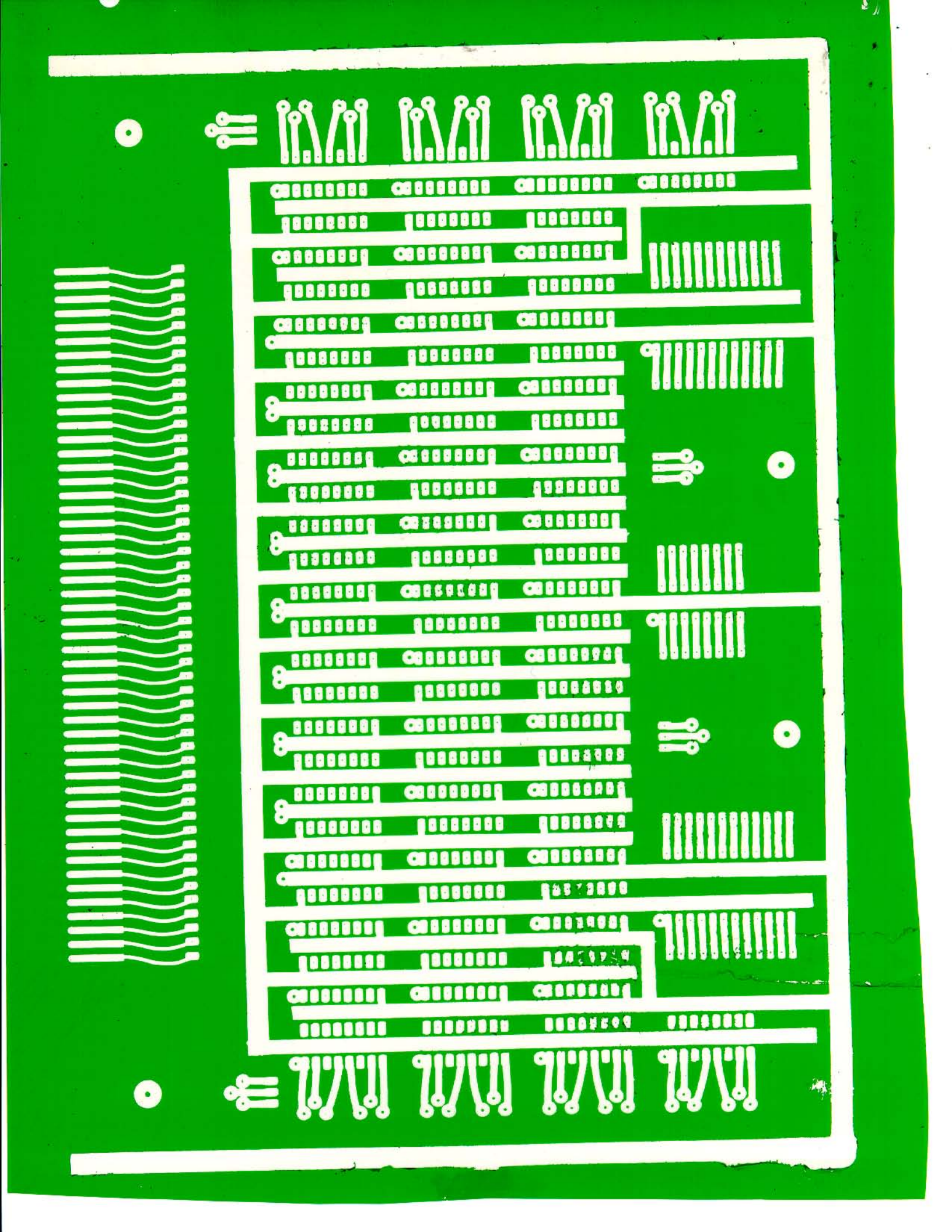

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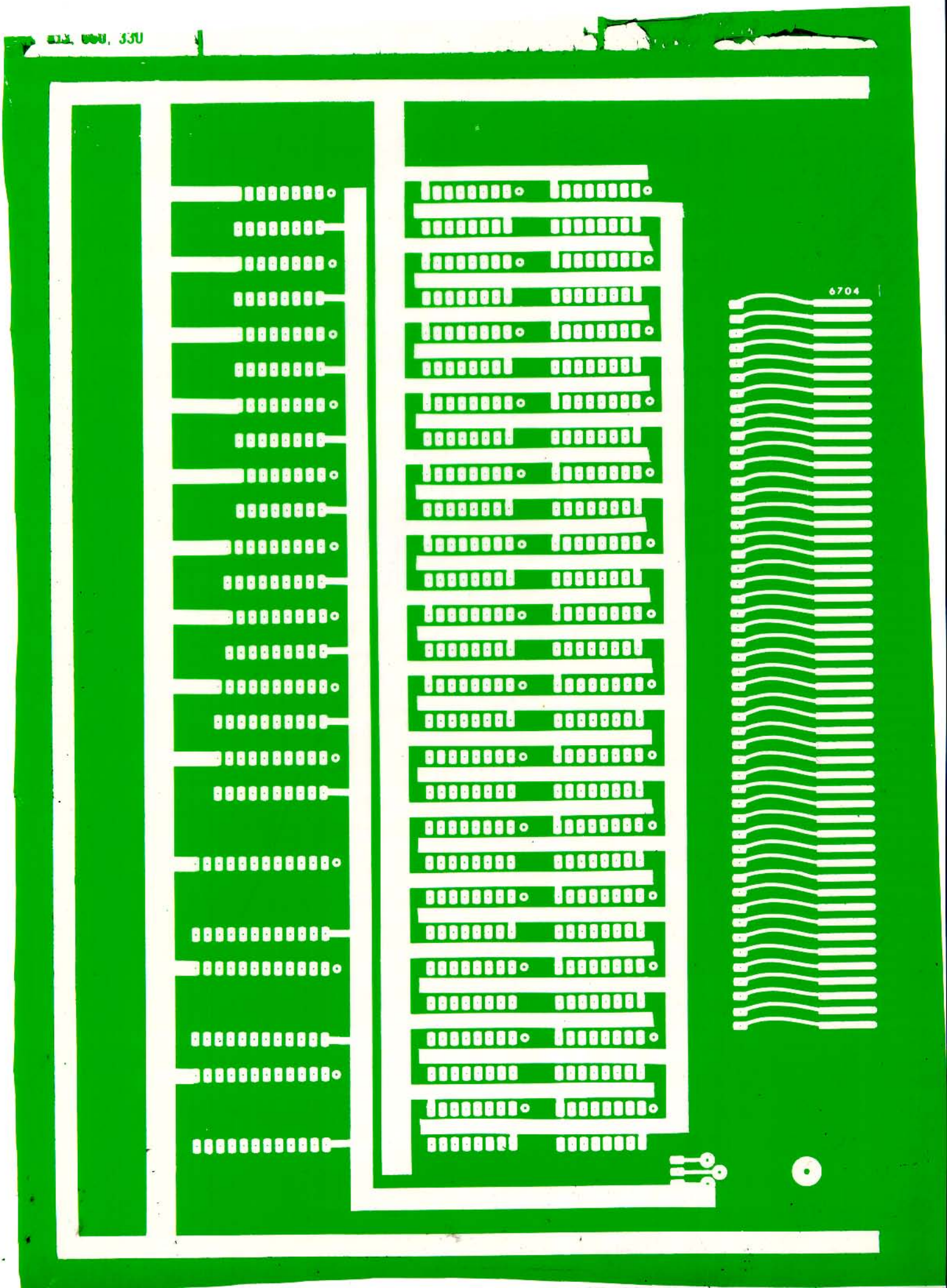
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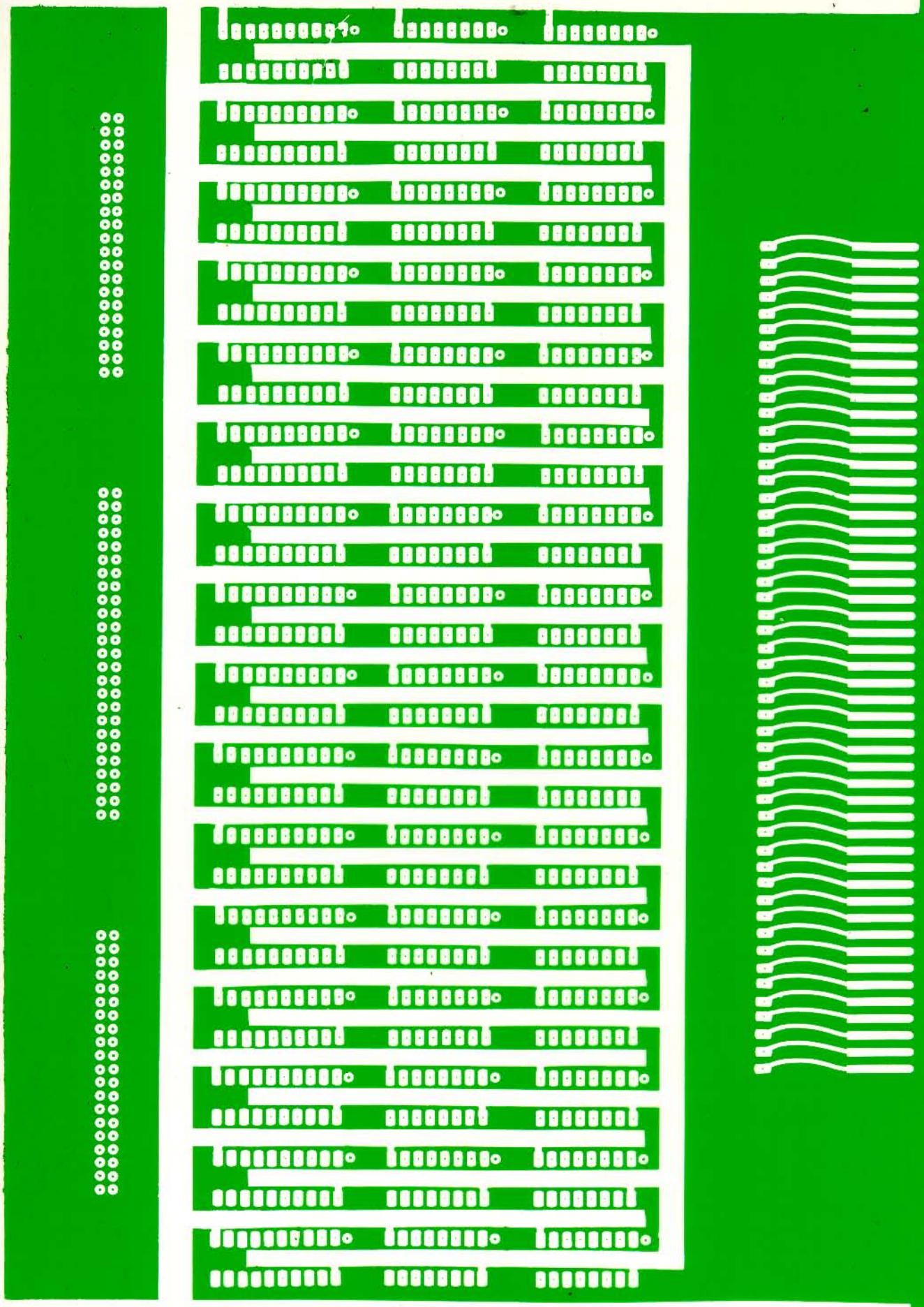

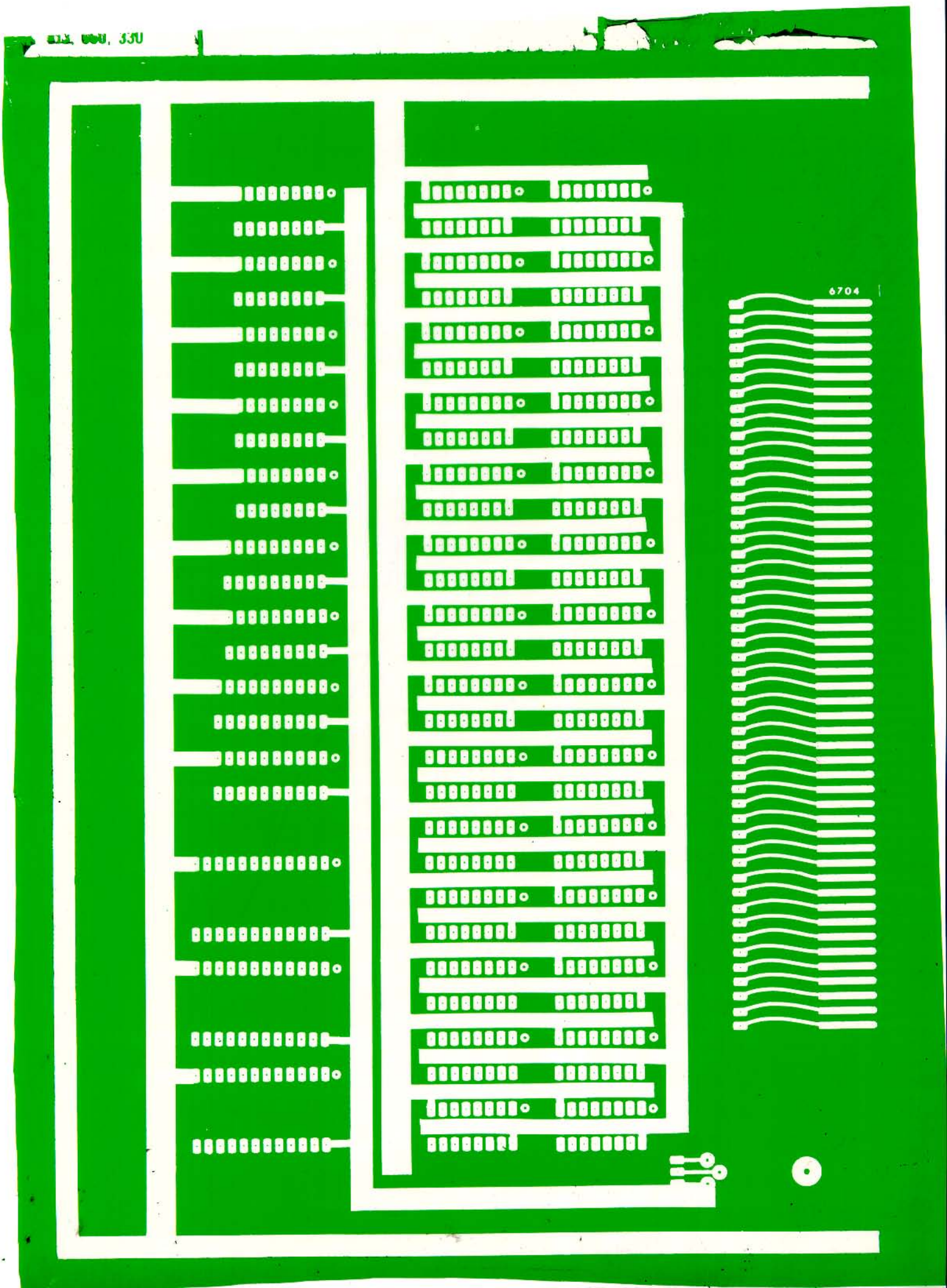
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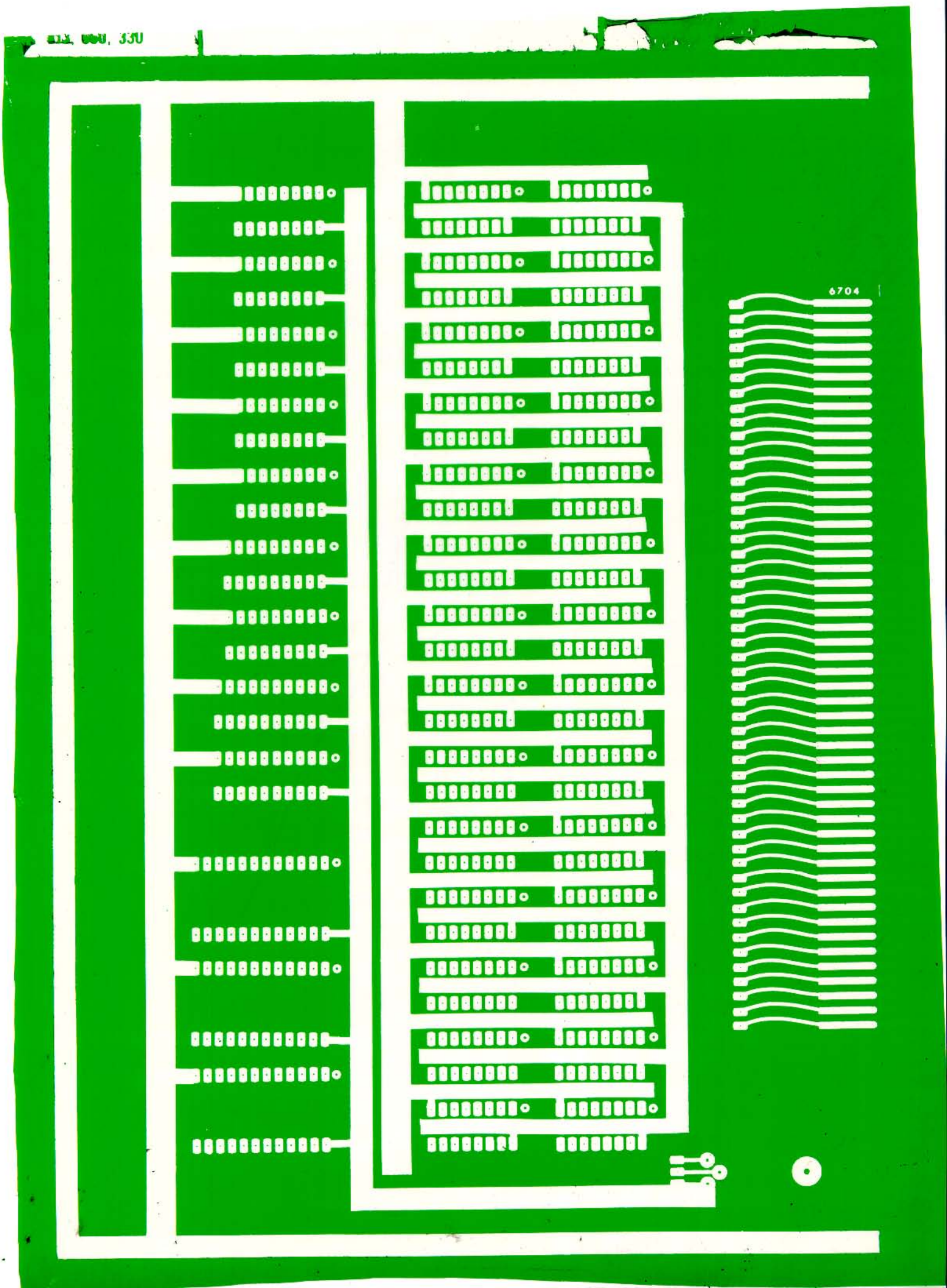
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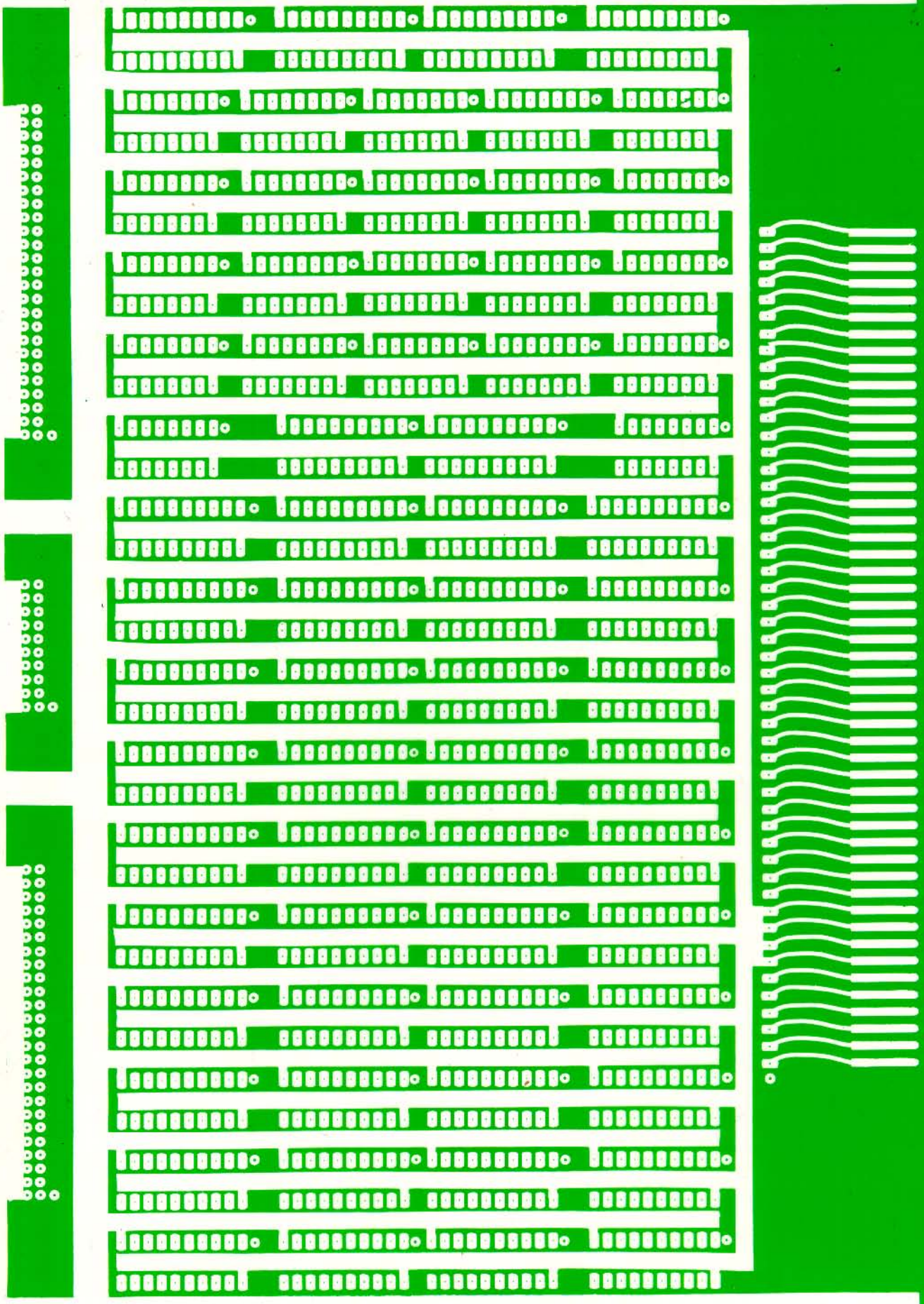

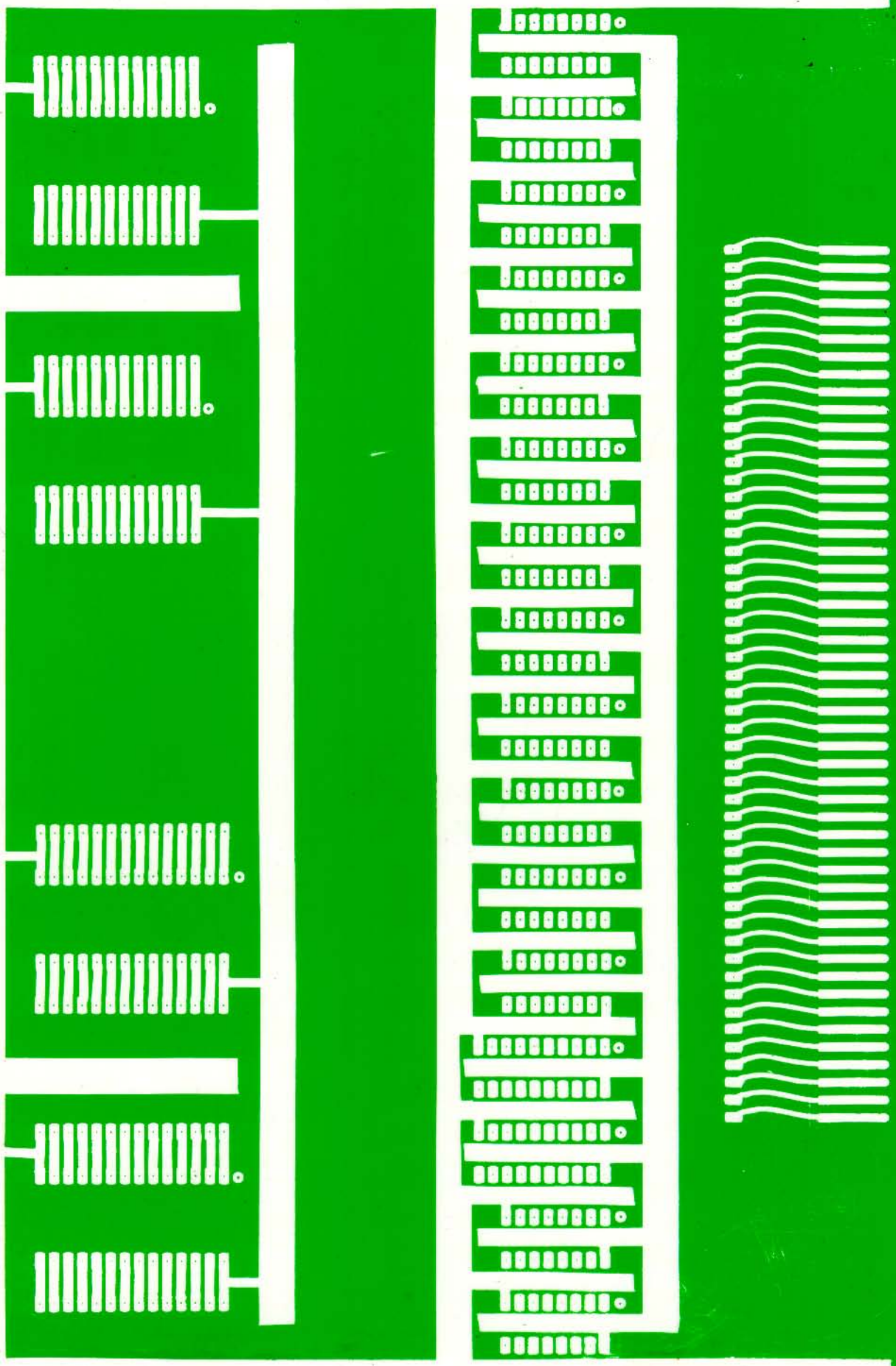

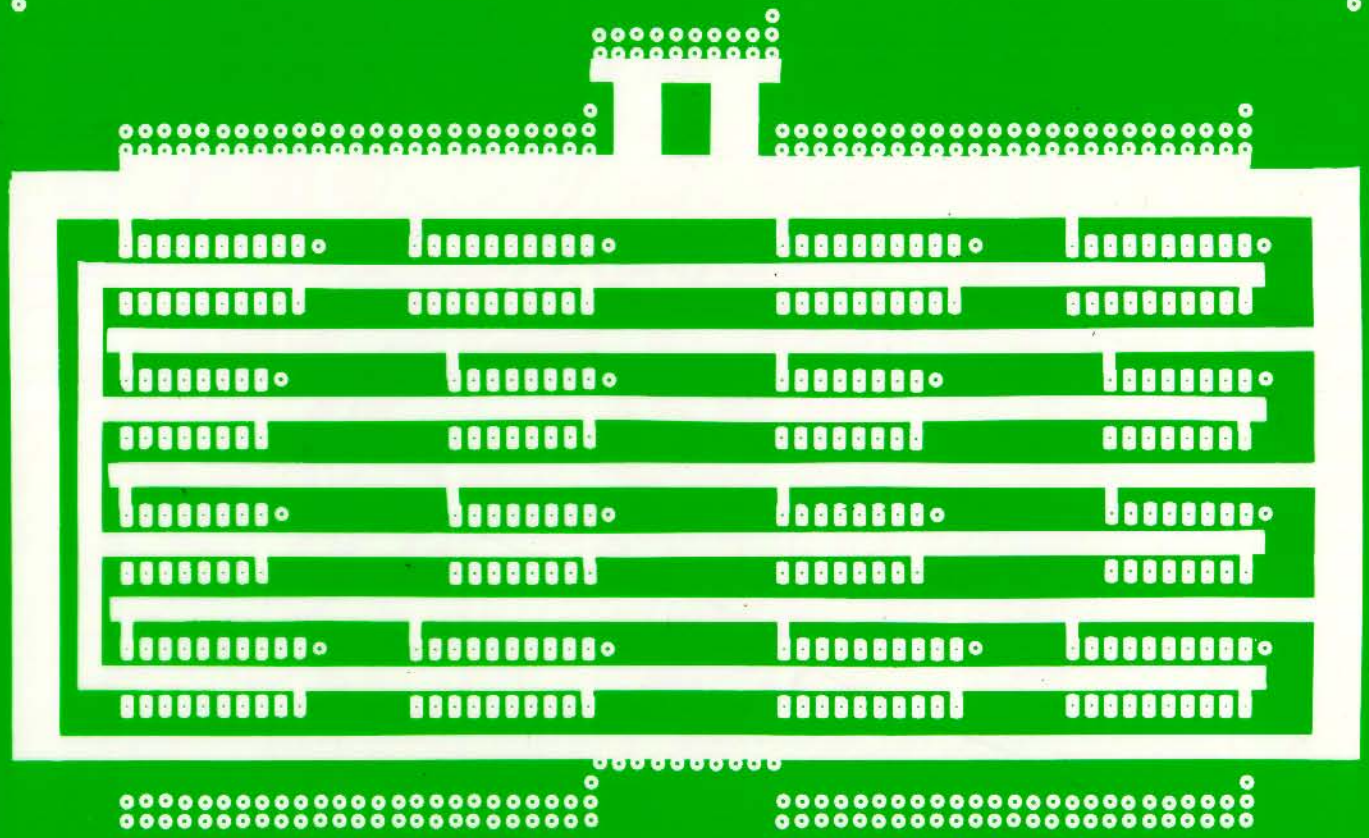

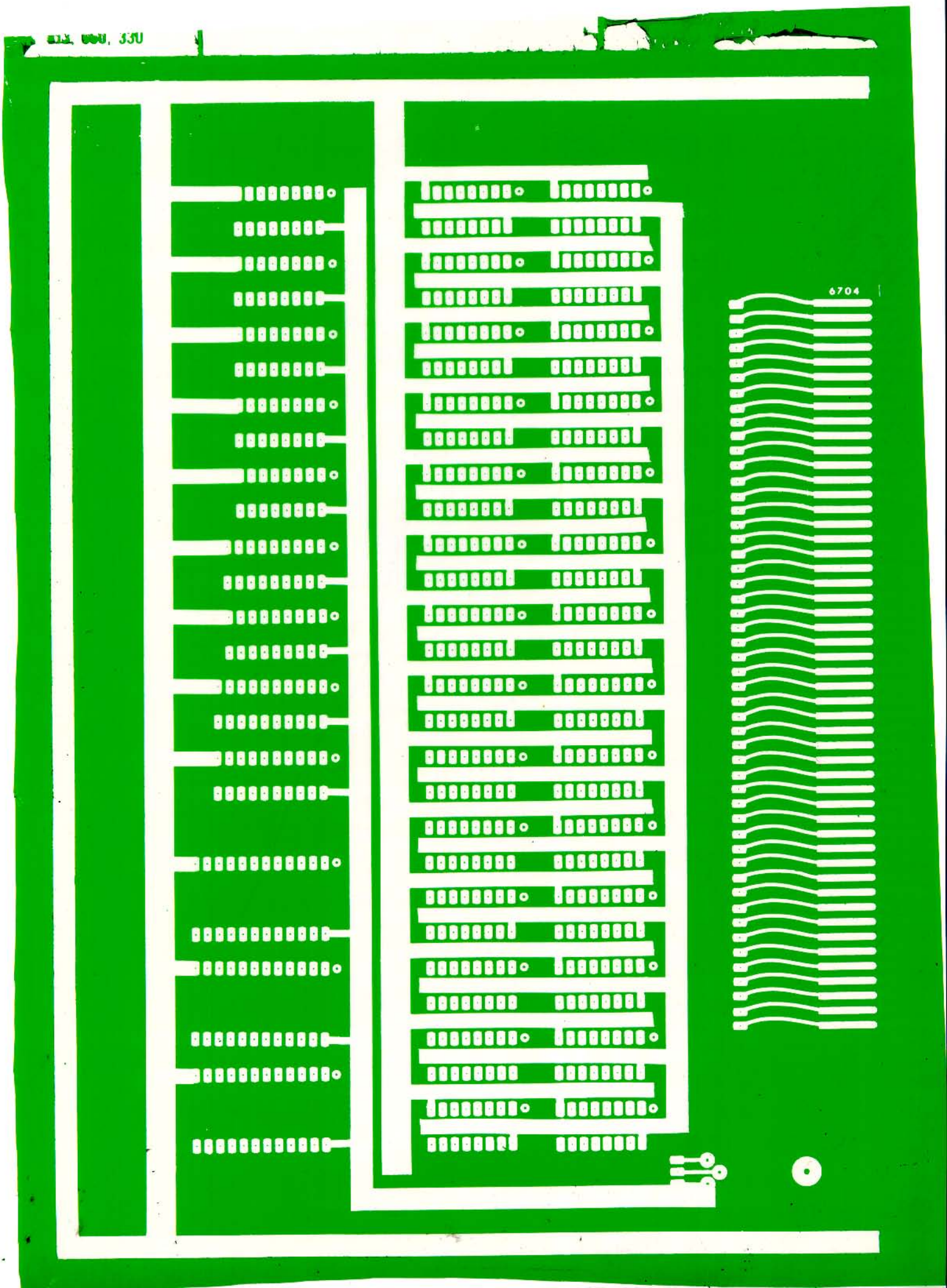
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NOTES

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